Low-Power Current-Mode 0.9-V Voltage Regulator

A. C. van der Woerd, W. A. Serdijn, R. H. van Beynhem, and R. J. H. Janse

Abstract—A design for a low-power integrated 0.9-V voltage regulator for load currents up to $140\,\mu$A is presented. The circuit contains no external components and it stabilizes the voltage of a single battery cell of 1.1–1.6 V with a PSRR $>$ 40 dB over a frequency range of up to 30 kHz. The regulating circuit operates a current level and accomplishes automatic load-current limiting. Its rms output noise is $< 4\,\mu$V over a frequency range of 10 Hz–8 kHz. The quiescent supply current is $\approx 40\,\mu$A.

I. INTRODUCTION

ANALOG equipment supplied by a single battery cell is becoming more prevalent. Further, more partial circuits are being integrated on one chip. Examples of this technology are hand-carried radiotelephones and hearing aids. The internal resistance of such a battery cell can increase to, say, $100\,\Omega$ by the end of its lifetime. The increase can easily give rise to instability caused by undesired couplings, especially if bypass capacitors are not allowed and if the system contains class-B operated circuits. The problems arising from these factors can be solved by supplying the most supply-sensitive parts of a device (such as microphone preamplifiers) via a voltage regulator with a sufficient power-source rejection ratio (PSRR) and excellent noise properties. Though there are excellent designs for voltage regulator circuits, they are more suitable to be employed for regulators used as building blocks than as partial circuits of completely integrated systems. Some of their characteristics exceed the demands of the above-mentioned applications, whereas other characteristics are not good enough. For example: common regulators demonstrate extreme accuracy, excellent temperature stability, and extremely low output impedance (not required), but they only operate effectively at 1.2 V and higher, produce too much output noise (typically 0.003% of the output voltage over a frequency range 10 Hz–10 kHz), and draw too much quiescent current for the proposed area of use here [1]. The regulator presented in this paper was originally designed for a general-purpose hearing aid chip [2]. For test purposes, it was integrated with other circuits on a master chip and it is intended to feed an arbitrary electret microphone with built-in JFET and an active telephone pick-up coil. A set of specifications is listed below:

General: As small a chip area as possible; no external components; short-circuit protection.

Detailed specifications:

Supply voltage: 1.1 V–1.6 V,
Output voltage: 900 mV $\pm$ 50 mV,
Load current range: 0–140 μA,
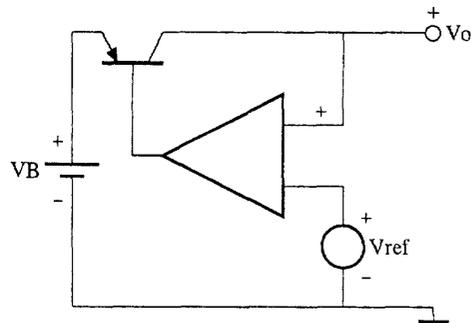
Fig. 1.   Traditional series regulator.

Noise voltage: $< 4\,\mu$V (100 Hz–8 kHz),
Temperature range 10°C–40°C,
Quiescent supply current: $< 50\,\mu$A.

II. THE DESIGN

Fig. 1 shows a traditional, basic series regulator circuit. A reference voltage (a combination of a diode voltage and a PTAT voltage [3]) is compared with (part of) the output voltage. The difference between the output voltage and the reference voltage is minimized by the loop gain. If voltages around 1 V and lower have to be regulated, this design is not very attractive because of problems associated with the design of the operational amplifier that must have input ranges near the negative rail. Although there are 1-V opamps with rail-to-rail input ranges [4], they are usually not low-power designs and draw too much supply current for hearing aid chip applications. Although a redesign based on the circuit shown in Fig. 1 and the principles given in [3] and [4] could be possible, we chose another basic design concept, a device that operates at current level and accomplishes automatic load current limiting. The basic circuit is shown in Fig. 2. Now the *current* through the reference source is amplified. With sufficient loop gain this current is minimized. Most voltage references need a small bias current and in those cases an extra current source has to be added (*Ibias*, dashed in Fig. 2). If the regulator loop gain is chosen to have a certain defined (limited) value L, the maximum load current will be automatically limited to $L^{*}Ibias$. It is clear that the voltage reference itself must then have a sufficiently low impedance.

Fig. 3 depicts a detailed block diagram of the circuit. Comparing this with Fig. 2, we observe that the voltage reference has been split into two parts: The reference voltage is composed of a Vbe generator and a (controllable) remaining part (Vrm). The current through the reference voltage source
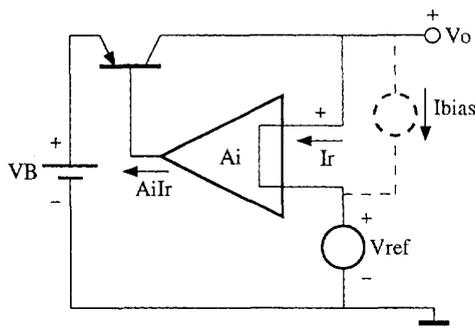
Fig. 2. Alternative series regulator.

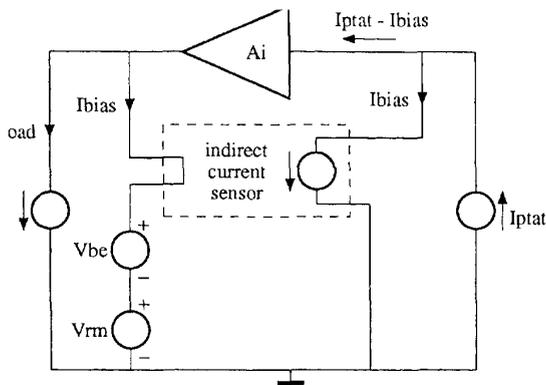Fig. 3. Detailed block diagram.

(*Ibias*) is amplified by a factor Ai. The resulting current $Ai^*(Iptat - Ibias)$ is fed back to the reference generator. Some calculation with the aid of Fig. 3 yields

$$Ibias = \frac{Ai^*Iptat - Iload}{Ai + 1}. \tag{1}$$

Hence, as soon as $Iload \geq Ai^*Iptat$, the reference voltage source is no longer biased and the regulation process ceases.

III. CIRCUIT DESCRIPTION

Fig. 4 depicts the circuit. Only one type of each n-p-n, v-p-n-p, and l-p-n-p have been used. Larger transistors were composed by parallel connecting of elementary devices. (The figures between brackets in Fig. 4 give the number of parallel-connected devices). $Q6$ and $Q7$ are l-p-n-p's; the remaining p-n-p's are v-p-n-p's. The circuit is biased by a conventional PTAT current source, comprising $Q8$ through $Q17$ and $Q21$ through $Q23$. The necessary start current ($Istart \approx 10$ nA) is delivered by a current source elsewhere in the system. $Iptat$ is used to bias the Vbe generator and the remaining part of the reference voltage Vrm, that also should be PTAT to accomplish some temperature compensation. $Q1$ and $Q2$ are connected as a voltage follower with offset $Vbe(Q2)$. Together with Vrm, which is passed on to the input of the voltage follower (the base of $Q2$), a low-ohmic reference voltage

$Vbe + Vrm(= Vo)$ is generated. The collector current of $Q1$ is indirectly sensed by $Q3$ and inverted by the current mirror $Q4, 5$. Hence, $Ic(Q5) \approx \cdot Ibias$. Then $Ic(Q5)$ is added to $Iptat$, and the summed current is inverted and multiplied by ≈ 30 by the amplifying current mirror $Q6, 7$. Finally, $Ic(Q7) \cdot Iload$ is fed back to the reference voltage generator.

IV. TEMPERATURE STABILITY

As the temperature dependence of Vbe is only reduced by 25%, the output voltage swing caused by temperature changes is about 45 mV ($10°$–$40°$C). It would be possible to achieve almost perfect temperature compensation and then the reference must be composed of a well-chosen *part* of Vbe and a PTAT voltage. However, because temperature stability demands were not stringent, we did not attempt to achieve this.

V. OUTPUT IMPEDANCE

The low-frequency output impedance Zo of the voltage follower amounts to:

$$Zo \approx \frac{2}{\beta_{Q1}} * \frac{1}{gm_{Q2}}. \tag{2}$$

In consequence of the current amplification accomplished by $Q6, 7$, the minimal low-frequency output impedance (at $Iload = 0$) of the complete circuit Zo' yields

$$Zo' \approx \frac{1}{15\beta_{Q1}} * \frac{1}{gm_{Q2}}, \tag{3}$$

with varying load current Zo' varies between the values, calculated from (2) and (3), respectively. With $Ic(Q2) \approx 3\,\mu A$ (see Fig. 4) and $\beta(Q1) = 45$, it follows $12\,\Omega < |Zo| < 370\,\Omega$ within the regulation range. (Note that the value of $|Zo|$ is not very important, as long as Vo remains between its specified limits, whereas the value of the $PSRR$ is of deciding importance).

VI. NOISE BEHAVIOR

The voltage Vrm could be simply realized by feeding a resistor with the PTAT current. However, as noise at Vrm appears at Vo, this would disastrously affect the circuit's noise behavior. Vrm is therefore derived from three saturated transistors ($Q18$ through $Q20$) with "forced beta." They are biased with $Ic/Ib = 8,9$ and 10, respectively, yielding a PTAT voltage $Vrm \approx 275$ mV. As the value of Vrm depends almost solely on Ic/Ib and a few large-signal parameters of the saturated transistors, noise on the PTAT current hardly penetrates into Vrm [5] and consequently, noise properties' demands are met.

VII. ACCURACY

As in the applied process, the tolerances in Vo depend directly on the absolute tolerances in Vbe, the correct value of Vo (= .90 V) generally has to be adjusted by trimming with on-chip fuses.
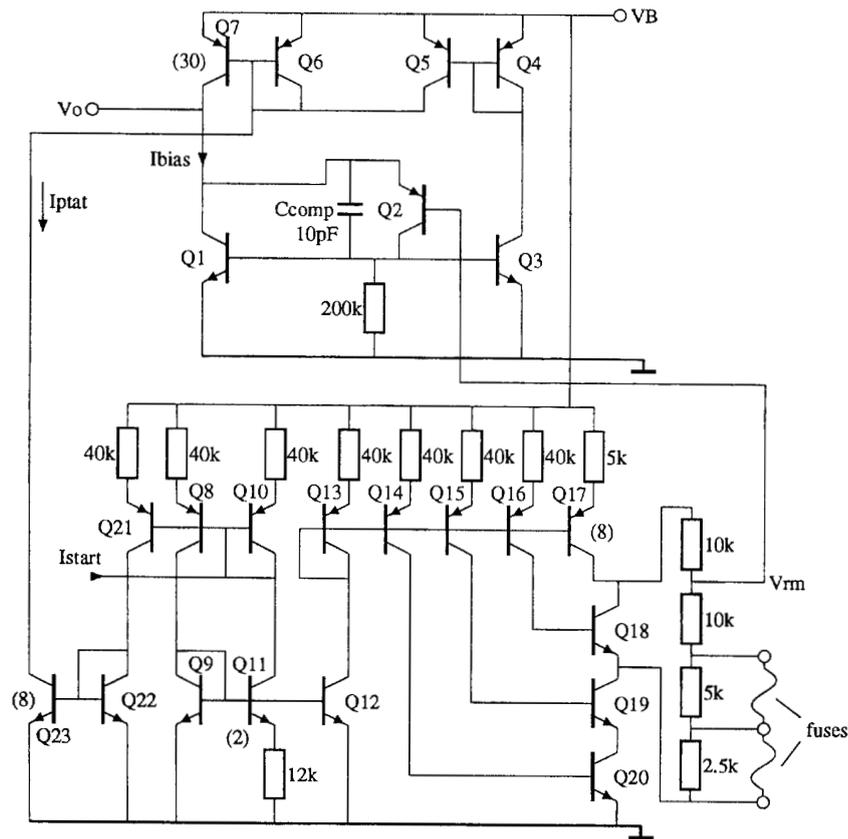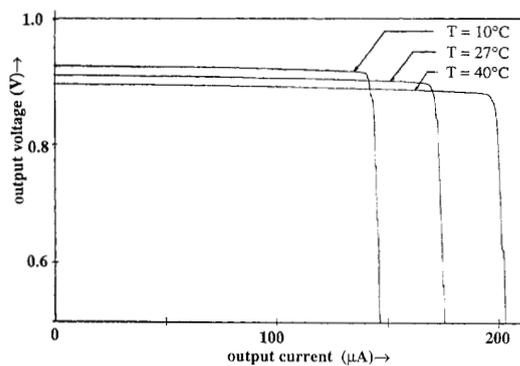
Fig. 4. Circuit diagram.

Fig. 5. Measured output voltage as a function of load current at different temperatures.

VIII. HIGH-FREQUENCY STABILITY

Without any frequency compensation, the circuit shows strong high-frequency peaking. This is caused because two dominant poles play a role in the loop comprising $Q1, 2, Q4, Q3, 5,$ and $Q6, 7$. Insertion of the pole-splitting capacitor $Ccomp$ (= 10 pF) assures stable operation at all relevant values of the output impedance. With this compensation, the loop has a dominant pole at ≈ 120 kHz.

IX. EXPERIMENTAL RESULTS

The following data are of measurements of an experimental BiCMOS master chip with typical β-values of 200 (n-p-n), 200 (l-p-n-p), and 45 (v-p-n-p).

X. MEASURED OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT AT DIFFERENT TEMPERATURES (FIG. 5)

We observe that the output voltage swing at a temperature swing of 30°C amounts to ≈ 45 mV, which agrees with theory. Further, the maximal load current that can be stabilized appears to increase when temperature increases. This temperature dependence is mainly caused by increasing loop gain owing to increasing PTAT-current. The remaining measurements were made at room temperature (27°C). Fig. 6 shows measured values of the PSRR with a supply voltage of 1.1 V (worst case). In all cases, the $PSRR$ remained > 40 dB over a frequency range 0–30 kHz. The measured rms *output noise voltage* amounted to $\approx 3.5 \mu V$ over a frequency range 100 Hz–8 kHz. The measured *output impedance* (Zo) as a function of frequency at different values of $Iload$ appeared to be < 50 Ω at any value of $Iload$ over a frequency range 0–40 kHz. Its measured low-frequency values were 13Ω and 46Ω at $Iload = 0$ and $140 \mu A$, respectively. Finally, the measured
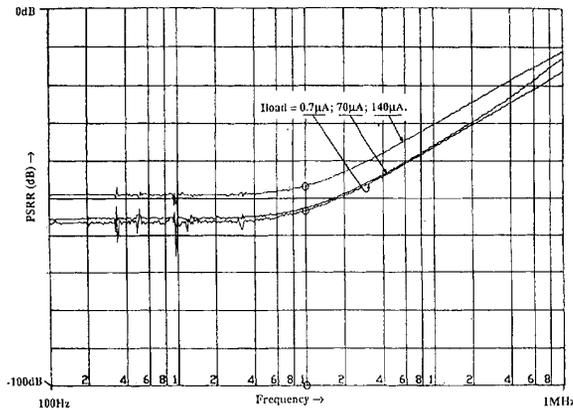
Fig. 6. Measured PSRR at different load currents.

Fig. 7. Microphotograph of part of the master chip employed.

quiescent supply current varied from $46\,\mu$A ($Iload = 0$) to $30\,\mu$A ($Iload = 140\,\mu$A).

Fig. 7 shows a microphotograph of part of the master chip employed. The voltage regulator circuit is situated on the part inside dashes. The same circuit was also integrated in an industrial full-custom BiCMOS process. Its area is about $0.135\,\text{mm}^2$.

XI. CONCLUSIONS

A low-power current mode .9-V voltage regulator has been presented. It is mainly suitable for use in fully integrated battery-supplied systems to stabilize the most supply-sensitive partial circuits (such as microphone input stages). The regulator shows very low output noise ($< 4\,\mu Vrms$ over 100 Hz–8 kHz) and a very large $PSRR$ (> 40 dB over 0–30 kHz).
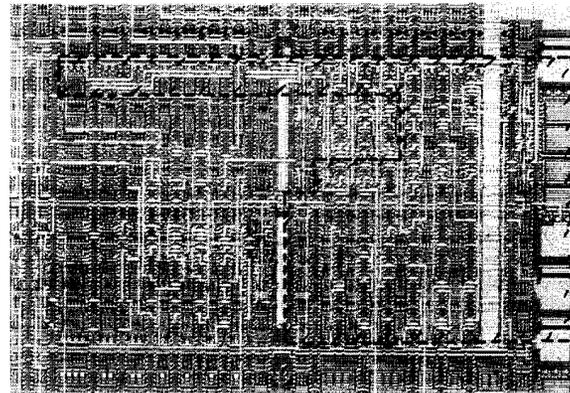
Its temperature stability is restricted, but meets the demands for applications in e.g., hearing aids. Its quiescent current is $< 50\,\mu$A at output currents varying from 0–140 μA.

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