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20 µm pitch Cu-to-Cu flip-chip interconnects through Cu nanoparticles sintering

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***Abstract*— This report demonstrates an innovative method to achieve large scale 20 µm pitch Cu-Cu direct bonding, utilizing lithographic stencil printing to transfer small-sized nano-copper (CuNPs) paste and employs a thermocompression method for CuNPs sintering to establish interconnections between copper-pillars and CuNPs bumps. Shear tests were conducted to characterize the bonding strength. High-throughput 20 µm pitch copper-to-copper direct bonding enables lower annealing temperatures for bulk-Cu to bulk-Cu bonding. Lithographic stencil printing is used to transfer the CuNPs paste, followed by sintering of the nanoparticles to establish interconnections. Shear tests and cross-section SEM were conducted to characterize the bonding strength and quality.**

Keywords—copper nanoparticles, flip chip, fine pitch, all-Cu interconnects

I. INTRODUCTION

Chiplet technology as a modular design approach has become integral to fulfilling 'More than Moore'. Microbump (µbump) interconnects play a key role in Chiplet to realize the 3D structure and must withstand higher current densities and temperatures, especially in high-performance computing systems. Due to low melting temperature of solder, the conventional Sn-based interconnects in 3D integration may cause issues such as remelting and electromigration failure under high current density [1]. Copper nanoparticle paste (CuNPs) presents an alternative to solder-based interconnects, due to its better electromigration resistance and high melting temperatures [2]. Furthermore, nano-Cu has compressibility, eliminating the need for chemical mechanical polishing (CMP) prior to bonding hence it is a cost effective approach. Therefore, executing high-precision fine-pitch nano-Cu patterns and investigating the sintering process is valuable for harsh environment applications[3].

In this study, we employ lithographic stencil printing (LSP) [4, 5] to implement an array of 20 µm pitch CuNPs bumps. A thin layer of photoresist serves as the stencil mask during CuNPs paste printing, which can be removed by lift-off process. Then, the thermos-compression bonding (TCB) process is utilized to integrate the CuNPs bumps to electroplated Cu microbumps to achieve Cu-to-Cu direct bonding. We developed the sintering parameter and examine the bonding strength using shear test.

II. MATERIALS AND METHODS

A. CuNPs paste Material

In this work, the CuNPs paste was synthesized by copper quasi-nanoparticles and organic solvent, which was in-house produced. The morphology of CuNPs was observed by a Hitachi Regulus 8230 scanning electron microscope (SEM), as shown in Fig. 1(a). Then, the size distribution of CuNPs was determined by counting on the SEM image and employing image processing software (ImageJ), as depicted in Fig. 1(b). As determined, the diameter of CuNPs ranges from 75 nm to 335 nm, with the majority falling within the range of 120~220 nm, constituting 72% of all measured nanoparticles. It can be observed that adjacent NPs tend to aggregate, which is due to the high activity of CuNPs.

B. Desgin of Interconnects Test Sample

We developed the LSP process to form 20 µm pitch CuNPs bumps. We designed and fabricated a interconnects test sample with photoresist stencil mask that intended for subsequent LSP process at the first stage, as Fig. 2 depicted. To start with, 1 µm thick dielectric layer was deposited on a 12-inch wafer followed by lithography and plasma etching to create 660 nm depth cavities. The cavity array had a diameter of 14 µm (Φ_1) and a pitch of 20 µm. Next, the prepared wafer was sputter coated with a TaN/Cu layer (10 nm/150 nm). Afterward, the CMP process

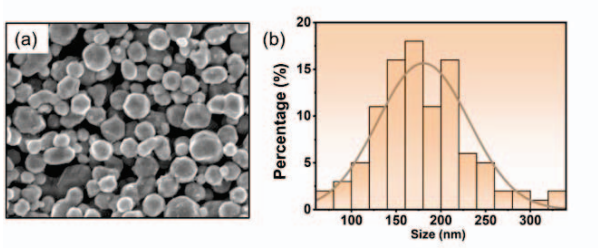

Fig. 1: (a) SEM image of copper nanoparticles in this study. (b) Size distribution of copper nanoparticles in (a).

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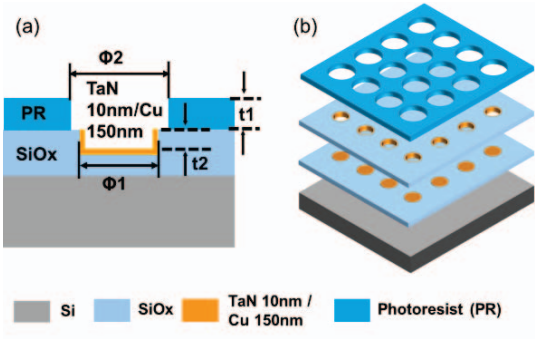

Fig. 2: (a) Schematics diagram of prepared bottom substrate by photolithography in (a) cross-section and in (b) 3D illustration.

removed the TaN/Cu layer from the field leaving TaN/Cu layer inside the cavity. Then, 1.6 µm photoresist was coated on the resulting wafer and then a hole array with 16 µm diameter (Φ_2 was patterned in 20 µm pitch by photolithography. The prepared wafer was diced into the test coupon of 35.1×33.6 mm, consisting of 3×3 chips using wafer dicing Disco DAD321.

In addition, we prepared a 7.2×7.2 mm top chip containing electroplated Cu microbumps of 2 µm height and 7 µm diameter (Φ_3) on 12 inch wafers to accomplish chip-to-substrate bonding in the subsequent step.

C. Photolithographic CuNPs Bumps Patterning

We conducted LSP experiments on the test coupon, as illustrated in Fig. 3. The CuNPs paste was employed by a silicon squeegee on the coupon and then was dried in an oven at 110 °C for 15 minutes (Fig. 3(a) and (b)). For the lift-off process, the

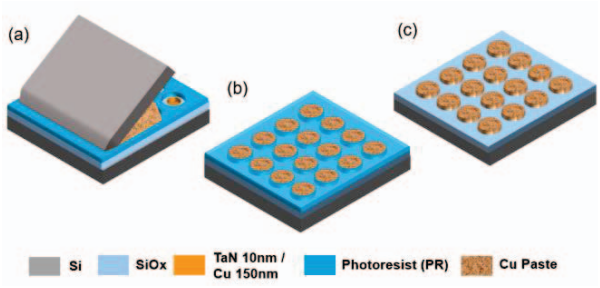

Fig. 3: A overview of the patterns transferring process using photolithography stencil printing.

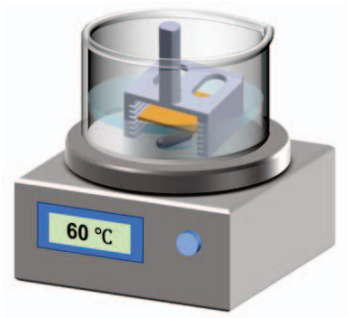

Fig. 4: A schematic of lift-off process. The carrier was specially designed and fabricated using 3D printing.

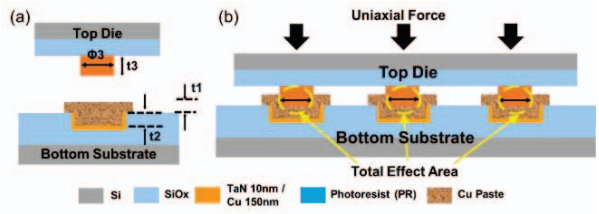

Fig. 5: (a) Schematics for bulk Cu microbumps for top to align with CuNPs patterned bottom chip. (b) Schematic representation of a bonded flip chip under uniaxial force, illustrating the total effective bonding area for pressure and shear strength calculation.

coupon was inserted in a specially designed carrier and was upside-down immersed in N-Methyl-2-pyrrolidone under agitation under 60 °C to strip the photoresist (Fig. 3(c)). The sketch of the lift-process is shown in Fig. 4. Finally, The resulting coupon was diced into 11.7×11.2 mm individual chips as the bottom substrate for the integration process.

D. Formation of Cu-to-Cu Interconnects

For the following TCB process, the flipped top chip and the CuNPs patterned bottom substrate were aligned with FC150 flip chip bonder (SET, Saint Jeoire, France), as depicted in Fig. 5(a). The FC150 bonder also performed a pressure-assisted sintering process in an ambient environment to integrate the top chip and bottom substrate as the same time. The stacked chips were bonded in-air at temperatures of 280 °C, 240 °C, 210 °C, and 180 °C, each with a pressure of 75 MPa applied for 15 minutes. Fig. 5(b) illustrates the schematic of bonded chips based on TCB parameters, which indicates the effective bonding area of bonded chips, as estimated as 1.55 mm^2 for each chip.

E. Characterization Methods

The microstructure of CuNPs was characterized by a Hitachi Regulus 8230 scanning electron microscope (SEM). The samples were inspected using a 3D profilometer (Keyence VK-X250) to image the CuNPs bumps after LSP process. The cross-section of sintered CuNPs was observed by using focused ion beam milling (SEM-FIB, FEI Helios G4 CX). The shear strength of the bonded flip chip was performed by Royce 650 Universal Bond Tester (Accelonix). The bond test were set up with the tool lift height of 50 µm and a shear rate of 5 µm/s.

III. Results and Disscussion

A. Characterization of Test Sample

We inspected the substrate covered by photoresist for further patterning study. The fabricated test sample for LSP process is illustrated in Fig.3. SEM images in Fig. 3(a) and (b) depict the resulting Si test coupon containing TaN/Cu coated holes. It is observed that the fabricated sample exhibits a pitch of 20 µm, an inner diameter of 14 µm, and an outer diameter of 16 µm. In Fig. 3(d), the surface profile of the photoresist opening cavity array on the test sample is analysed, and the profile is indicated by the pink line in Fig. 3(c), demonstrating the 3D surface topography of the test sample. The depth of the holes is estimated to be 2.1 µm using the 3D profilometer, corresponding to the sum of depths *t1* and *t2* in Fig. 5(a). *t1* and *t2* respectively representing the thicknesses of the cavity inside the dielectric layer and the photoresist covering on the dielectric layer. The etched cavities

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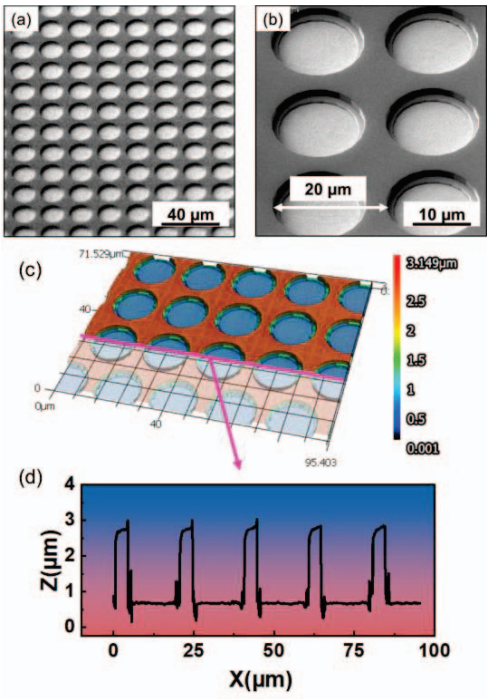

Fig. 6: (a) and (b) SEM images of test sample. (c) 3D optical image of surface. (d) surface profile of cavity array indicated by the pink line in (c).

contribute to the integrity of the CuNP pattern transferred in the next step.

B. *Characterization of Patterned CuNPs*

Fig. 7(a) shows a test coupon with a CuNPs bump pattern using the LSP approach, with the inset indicating a separate bottom substrate after dicing for subsequent flip-chip integration. The CuNPs pattern was defined by the photoresist stencil mask and was evaluated by the integrity of the CuNPs bump array and the height of bumps, which was derived from the determined thickness of photoresist. The integrity of the CuNPs pattern after the lift-off process is illustrated in Fig. 7(b), showing a well-preserved array of bumps. The photoresist between the bumps has been completely removed, leaving no excess material residue between adjacent bumps, and only retaining the opening pattern presented by the previous step of photoresist.

Fig. 7(c) and (d) show the 3D image and the height profile of bump array respectively. It can be observed that the pitch of bumps is 20 µm and the surface of CuNPs bumps is highly rough. The height of the CuNPs bumps was estimated from the average height of the profile to be approximately 1.8 µm, slightly exceeding the thickness of the photoresist (1.6 µm). This observation indicates a correlation between bump height and photoresist thickness, with the slight nanomaterials excess attributed to an additional layer of nanoparticles.

C. *Evaluation of Bonding Flip Chip*

Fig. 8(a) demonstrates a photo of a single stacked chip after in-air sintering using TCB approach. The alignment of flip chip was examined by an infrared microscopy, as shown in Fig. 8(b).

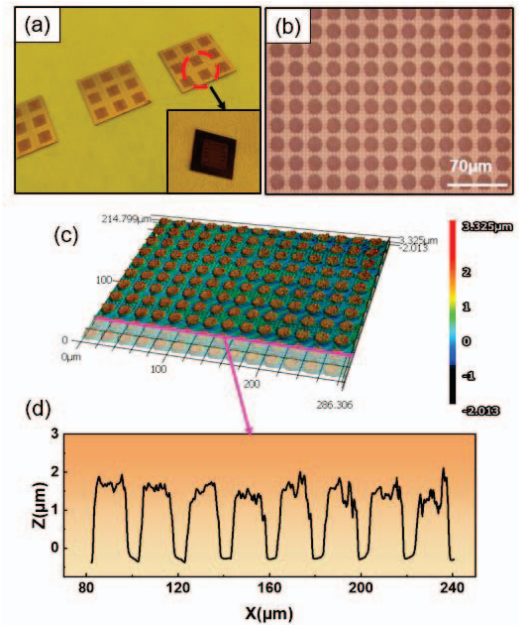

Fig. 7: (a) Test coupon with CuNPs patterns after lift-off process, with inset showing a single chip after dicing. (b) Optical image of the CuNPs bump array. (c) 3D image of bottom substrate and (d) height profile along the pink line in (c) of CuNPs bumps.

It can be seen that the misalignment of top and bottom dies is below ~1 µm, which is much lower than the estimated misalignment tolerance of 3.5 µm (Φ_1 /2 – Φ_3 /2). Hence, the bonding pressure of 75 MPa is feasible for chip-to-chip integration.

Fig. 9 displays the shear strength for bonded dies at different bonding temperatures under the same bonding pressure of 75 MPa and the same bonding time of 15 min in ambient. The sintering parameter of the design of experiments and the measured shear strengths are shown in the Table. 1. It is observed that the shear strength is insufficient to be obtained through bonder testing when the sample was sintered at 180 °C. When the stacked chips were bonded at 210 °C, the shear strength was measured to be 6 MPa, indicating the limits of acceptable mechanical integrity for the stacked chips. Therefore, the lowest sintering temperature of 210 °C can serve as the initial benchmark for determining sintering parameters in future studies. Increasing sintering temperature to 240 °C, it provided 26 MPa shear strength with a large increasing rate of 333%. Continuously raising the sintering temperature to 280 °C shows the higher shear strength of 38 MPa. It is evident that the standard deviation increases with higher temperatures, particularly notable at 280 °C, reaching up to 7 MPa. It assumed

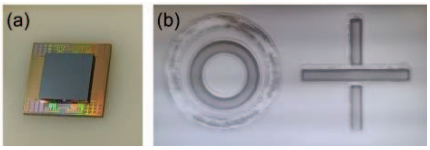

Fig. 8: (a) A photo of stacked die after bonding in air. (b) a infrared microscope image of the alignment marker on top and landing die.

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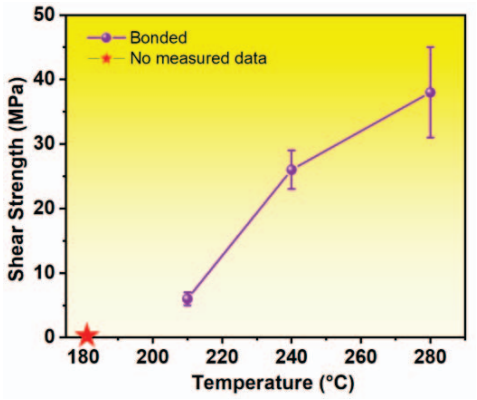

Fig. 9: Shear strength for the stacked dies with different bonding temperature under bonding pressure of 75 MPa and bonding time of 15 min after TCB process.

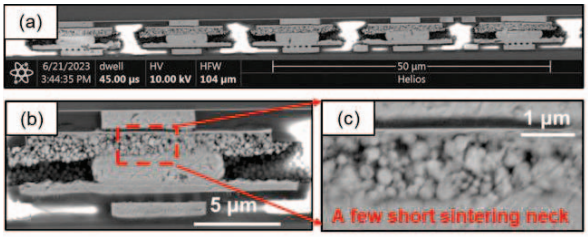

Fig. 10: SEM images of the cross section of the integrated chip with sintering parameter of 180 °C, 75 MPa and 15 min. (a) Distrbution of 20 µm pitch CuNPs interconnects, (b) one bonded bump featuring CuNPs and (c) an enlarged image illustrating bonding interface and the morography of nanoparticles, indicated in the red dashed box in (b).

to be that the higher temperature caused a worse warpage of substrate.

To further investigate the bonding results at the lowest bonding temperature of 180 °C, we polished the integrated sample for cross-sectional inspection, as shown in Fig. 10. It can be seen that the top chip and the bottom have been bonded successfully, and the alignment accuracy is sufficient for pitch level of 20 µm under bonding pressure of 75 MPa. At the lowest temperature, CuNPs agglomerate, only a few adjacent nanoparticles are slightly sintered, appearing short sintering necks. Meanwhile, there are some voids at the bonding interface. For the prepared CuNPs paste, organic compounds can only evaporate completely above 230 °C [1]. Therefore, a large amount of organic additives remain inside the CuNPs, hindering the sintering process at lower temperature.

TABLE I. SINTERING PROCESS PARAMETER

Parameter	Process Sample			
Pressure (MPa)	75	75	75	75
Temperature (°C)	180	210	240	280
Time (min)	15	15	15	15
Shear strength (MPa)	No data	6±1	26±3	38±7

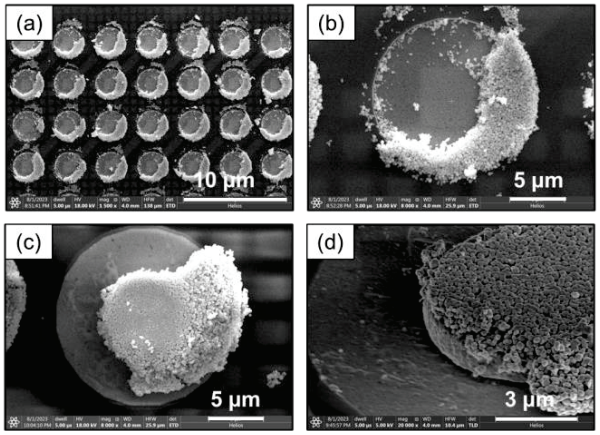

Fig. 11: SEM images of frature surfaces after shear test on the bottom substrate (a,b) and on the top chip (c,d). The sintering parameters were 240 °C, 75 MPa and 15 min.

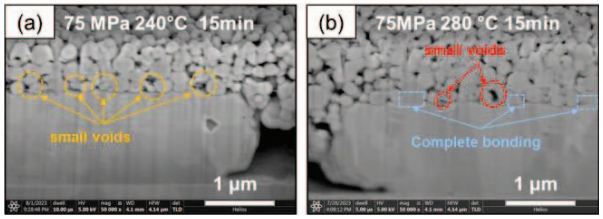

Fig. 12: SEM images of cross-section morphology with different bonding temperature at (a) 240 °C and (b) 280 °C.

D. Microstructrual analysis of sintered CuNPs

The surface of sheared samples is inspected to show the fracture morphology of CuNPs interconnects at a bonding temperature of 240 °C. First, the top views of the sheared-off bottom substrate are shown in Fig. 11(a) and (b), indicating adhesive fractures occurring for all interconnects at the interface between the sintered CuNPs and TaN/Cu-covered cavity surface. Fig. 11(c) demonstrates the fracture morphology of the top chip, which is capped with CuNPs. During the sintering process, enhanced copper diffusion occurs on Cu-Cu interface between the CuNP bumps and Cu pillars on the top chip, resulting in stronger adhesion compared to the bond between CuNPs and TaN/Cu pads. As a result, most fracture behaviour occurs between the CuNPs and the bottom substrate. Figure 11(d) shows that fracture occurs inside the CuNPs bump at the edge of the Cu pillar indicating presence of copper oxide in the interface of pillar and CuNP .

Next, the SEM cross section images of the sintered joint on sheared-off top chip were obtained using FIB to analyse the microstructure of sintered CuNPs and to examine the interface diffusion between CuNPs and Cu pillars at different bonding temperatures. At 240 °C, as shown in Fig. 12(a), sintering necks were formed between CuNPs and at the interface between the Cu pillar surface and CuNPs. The sintering neck length of this sample is significantly longer than that observed at 180°C, as shown in Fig. 10(c). In addition, there are some small voids at the interface, which are labelled by yellow dashed circles in Fig. 12(a). However, due to the weak sintering networking, the bonding strength was only around 26 MPa. Fig. 12(b) depicts a

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robust sintering network in the sample sintered at 280 °C, The number of interfacial voids decreases with increasing bonding temperature, and there are some intact bonding areas on the Cu-Cu interface. We believe that with proper copper oxide cleaning of Cu bumps, results will be much better and optimization is on-going.

IV. Conclusion and Outlook

In this work, the CuNPs paste was applied for the 20 μm pitch interconnects and the patterning process was feasible to enhance the integrity and bonding strength of flip chip integration applying for 3D integration. The array of CuNPs bumps were conducted for the subsequent bonding process and mechanical property characterization. The heights of patterning bumps are determined by the thickness of applied photoresist. Although the surface of bumps is highly rough, enabling integration of the top chip and bottom substrate without the need for CMP, and the sliding between the top and bottom chips after bonding was within alignment tolerances.

Mechanical performances were evaluated using die shearing test. The sample sintered at 180 °C did not form effective sintering neck, therefore, this stacked sample has no bonding strength. The sintering temperature of 210°C is defined as the minimum benchmark for sintering strength. As the temperature increases, the shear strength is improved from 6 MPa to 38 MPa, with a larger standard deviation due to warpage issues. Cleaning copper oxide prior to bonding may lower temperature threshold for sintering.

The fracture mode of all interconnects was adhesive and the fracture mainly occurred on the interface between TaN/Cu bottom substrate and CuNPs bumps. As the bonding temperature increases, the interfacial voids decrease, accompanied by the sintering neck increasing.

Furthermore, additional sintering parameters, such as pressure and time, need to be investigated to assess their effects. The comparing studies with conventional Cu-to-Cu bonding and solder joint flip chip integration will also be conducted for further study. This work confirmed the feasibility of LSP-patterned CuNPs for all-Cu interconnects approach. The updating samples will be involved for their electrical performance. Due to the limitations of bonding tool, this experiment was completed in-air. Future research will focus on improving methods in forming gas to prevent copper oxidation.

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References

[1] Christine Hau-Riege, YouWen Yau and Kevin Caffey. "Key metrics for the electromigration performance for solder and copper-based package interconnects." 2016 IEEE 66st Electronic Components and Technology Conference (ECTC). IEEE, 2016.

[2] Dai Ishikawa, Bao Ngoc An, Matthias Mail et al. "Analysis of Bonding Interfaces of Pressureless-sintered Cu on Metallization Layers." 2019 International Conference on Electronics Packaging (ICEP). IEEE, 2016.

[3] Shuaiqi Wang, Guisheng Zou, Yongchao Wu et al, "Patterned Cu Nanoparticle Film for All-Cu Interconnection Without Chemical Mechanical Polishing Pretreatment." IEEE Transactions on Components, Packaging and Manufacturing Technology 2023.

[4] Xinrui Ji et al, "Low Temperature Fine Pitch All-Copper Interconnects Combining Photopatternable Underfill Films." 2023 IEEE 73st Electronic Components and Technology Conference (ECTC). IEEE, 2023.

[5] Xinrui Ji et al, "Microstructural and micromechanical characterization of sintered nano-copper bump for flip-chip heterogeneous integration." Microelectronics Reliability, 2023.

[6] Liu, Xu, et al. "Study and Application of Nano Copper Sintering Technology in Power Electronics Packaging." 2021 IEEE 71st Electronic Components and Technology Conference (ECTC). IEEE, 2021.

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