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FROM SILICON TOWARD SILICON CARBIDE SMART INTEGRATED SENSORS

FROM SILICON TOWARD SILICON CARBIDE SMART INTEGRATED SENSORS

Proefschrift

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door

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Keywords: harsh environments, smart sensors, system integration, wide-band semiconductors, silicon carbide, MEMS, pressure sensors, particle sensors, suspended membranes, micromachining, SiC CMOS, monolithic integration

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List of Abbreviations

ADC ..... Analog to digital converter

AM ..... Amplitude modulation

a-SiC ..... Amorphous (nano-crystalline) silicon carbide

ASIC ..... Application-specific integrated circuit

BEOL ..... Back-end-of-line

BHF ..... Buffered hydrofluoric acid

BJT ..... Bipolar junction transistor

BS ..... Backside

BW ..... Bandwidth

CLK ..... Clock (signal)

CMOS ..... Complementary metal-oxide-semiconductor

CO ..... Contact opening

CR ..... Cleanroom

CTAT ..... Complementary to absolute temperature

CTE ..... Coefficient of thermal expansion

CVC ..... Capacitance to voltage converter

DCS ..... Dichlorosilane

DI ..... Deionized

DPF ..... Diesel particulate filter

DRC ..... Design rule check

DRIE ..... Deep reactive ion etching

EKL ..... Else Kooi Laboratory

ELM ..... Electrical linewidth measurement

EMI ..... Electromagnetic interference

epi ..... Epitaxy

FE ..... Field emission

FEM ..... Finite element modeling

FFT ..... Fast Fourier transform

FHG ..... Fraunhofer Gesellschaft (society)

FS ..... Frontside

FSM ..... Finite state machine

GaN ..... Gallium nitride

GF ..... Gauge factor

GFR ..... Gas flow ratio

GND ..... Ground (node)

HEMT ..... High electron mobility transistor

HF ..... Hydrofuoric acid

IC ..... Interconnect

ICE ..... Internal combustion engine

ICP ..... Inductively coupled plasma

IDE ..... Inter-digitated electrode

IDT ..... Inter-digitated transducer

IGBT ..... Insulated-gate bipolar transistor

IR ..... Infrared (electromagnetic radiation)

IoT ..... Internet of Things

IPA ..... Isopropanol (propan-2-ol)

ITO ..... Indium tin oxide

KCB ..... Kelvin cross bridge

KOH ..... Potassium hydroxide

LASER ..... Light amplification by stimulated emission of radiation

LiDAR ..... Light detection and ranging

LII ..... Laser induced incandescence

LPCVD ..... Low pressure chemical vapor deposition

LVS ..... Layout versus schematic

MEMS ..... Micro-electro-mechanical systems

MiM ..... Metal-isolator-metal

mono-SiC ..... Mono-crystalline silicon carbide

MOSFET ..... Metal-oxide-semiconductor field-effect transistor

MSM ..... Metal-semiconductor-metal

MSS ..... Microsoot sensor

NMOS ..... N-channel MOSFET

NMP N-methyl-2-pyrrolidone

PCB ..... Printed circuit board

PCM ..... Process control module

PEC ..... Photo-electro-chemical (etching)

PECVD ..... Plasma enhanced chemical vapor deposition

PM ..... Particulate matter

PMOS ..... P-channel MOSFET

PN ..... Particle number concentration

poly-SiC ..... Poly-crystalline silicon carbide

PGA ..... Pin Grid Array

PR ..... Photoresist

PSD ..... Power spectral density

PTAT ..... Proportional to absolute temperature

PVD ..... Physical vapor deposition

PZT ..... Lead zirconate titanate

RIE ..... Reactive ion etching

RT ..... Room temperature

RTP ..... Rapid thermal processing

SEM ..... Scanning electron microscope

Si ..... Silicon

SiC ..... Silicon carbide

SiP ..... System in package

SMD ..... Surface-mount device

SMU ..... Source measurement unit

SoC ..... System on chip

SOI ..... Silicon on insulator

SRAM ..... Static random-access memory

TCR ..... Temperature coefficient of resistance

TEOS ..... Tetraethyl orthosilicate

TFE ..... Thermionic field emission

TIA ..... Trans-impedance amplifier

TLM ..... Transmission line model

UV ..... Ultraviolet (electromagnetic radiation)

VLSI ..... Very large scale integration

ZIF ..... Zero insertion force (socket)

1

INTRODUCTION

1.1. MOTIVATION

SINCE it is obvious that Moore's Law in its classical way of scaling, which proved to be powerful over the last decades, is coming to an end, alternative routes toward technological progress are investigated [2]. One of the main fundamental reasons for this is that the smallest features size in newest technology nodes is approaching the level of only a few atom layers. As a result, the development and implementation of technology nodes based on a scaled-down version of the previous one, gets increasingly more expensive. An alternative approach to ensure technological progress of the microelectronics world and the semiconductor industry is described by a trend called 'More than Moore' (MtM) [3–5], based on diversification and integration. In terms of diversification, materials beyond silicon can be considered for the development of sensors and electronics, while the integration aspects comes to expression by combining different parts of a system in a smart and optimal way. Wide-band gap (WBG) materials, such as gallium nitride (GaN) or silicon carbide (SiC) are mature for power applications, but for other applications such as low voltage (Bi)CMOS, VLSI or sensor development are still in the research phase. By integrating electronics monolithically on a sensor chip, improved system performance can be obtained by having signal amplification close to the physical transducer. The integration aspects is strongly related to the packaging of microelectronic and microfabricated devices, for example when multi-physical sensors are considered. A recent example is the through polymer via enabling an optical channel through a package [6].

Parts of this Chapter have been published as book Chapter from *Sensor Systems Simulations: From Concept to Solution.* Springer International Publishing (2020) [1].

By investigating non-linear effects in MEMS structures the mechanical sensitivity can be boosted in a bulk micromachined and thus space limited chip. Furthermore, by the application of new materials, such as SiC, sensors and (low voltage) electronics can be yielded compatible with harsh environments and temperatures up to 500 °C. By investigating the monolithic integration of analog electronics with mature sensor technologies, the strengths of system integration can be implemented and exploited, resulting in more value from existing technologies. These two topics are examples of the 'More than Moore' concept.

The development of SiC based electronics to build op technologies for low-voltage CMOS, BJTs or BiCMOS for both analog and digital circuits is still pre-mature. That this development is still in the research phase is illustrated by the given that numerous research works focus on device simulation and model extraction for SiC CMOS. Furthermore, when looking over the literature that is available on SiC technology, one could notice a trend in shifting interest from from 6H-SiC to 4H-SiC. [7–10]

A shift can also be spotted in the junction formation from mesa etching on epitaxially grown layers to ion implantation techniques, which have been evolved during the last ten years. Another challenge on the physical level is the chemical/physical effects in ohmic contacts and the long term reliability and stability of metallization schemes [11]. So, even on the very basic physical level, significant changes have taken place, illustrating that the SiC electronics development is in its premature phase.

Additionally to the development of SiC electronics, compatibility of the fabrication processes is of utmost importance, when all-SiC ASIC + MEMS monolithic system integration is considered. A cleanroom flowchart for the processing of MEMS can be very different from a flowchart for the processing of electronics in terms of thermal budget, contamination and topography. Silicon carbide being a harsh environment compatible material, and thus an inert material, more fabrication steps involve high temperature processing compared to standard silicon technology.

1.2. SILICON TECHNOLOGY AND ITS LIMITATIONS

Silicon technology has been mature for decades for the fabrication of a broad range of electronics, ranging from BJTs, analog CMOS, BiCMOS to digital integrated circuits such as VLSI architectures. Based on this silicon technology, sensor technology is developed and implemented. By re-using existing technologies and process steps such as oxidation, patterning, wet- and dry etching and dopant formation big steps have been made and a powerful palette of fabrication methods has been available for decades. The term 'CMOS compatible' is very common in the field of sensors, which practically denotes

that the sensors considered can be processed within a CMOS process flow, reducing costs dramatically.

It should however be realized, that this implicit choice for silicon and CMOS compatible technology can have some dramatic drawbacks in the sensor design for certain applications. For numerous applications, silicon is not the first-choice material, but is still chosen for its earlier mentioned wide-spread availability and inherent low-cost. Furthermore, a CMOS compatible process flow might put restrictions to the sensor design, negatively influencing overall design freedom and compromising sensor performance. Surface and bulk micromaching techniques, such as Deep Reactive Ion Etching (DRIE), have been developed based on etching technologies from silicon CMOS processing, for example by extending etch times, applying cycling recipes or increasing etch power in case of plasma etching. This development has enabled the design and realization of Micro-Electro-Mechanical-Systems (MEMS) in silicon. Currently, the MEMS market covers application field such as Radar, Ultra Sonic, LiDAR, chemical-, magnetic-, imaging- and pressure sensors and has a value of around ten billion dollars [12].

A major field of application where silicon technology is not sufficient, is the field of harsh environments. Harsh environments are considered surroundings with high temperatures, corrosive species, vibrations or radiation. Silicon is in general not capable of being compatible with harsh environments. Firstly, because the electronic behavior is compromised at temperatures of 150 °C and beyond. This effect is caused by the intrinsic carrier density of silicon being several orders of magnitude larger than WBG counterpart materials, such as GaN or SiC. The intrinsic carrier concentration is increasing with increasing temperature and as soon as the intrinsic carrier density is exceeding the dopant concentration of the junctions defined by implantation, the electronic device fails in operation. It can thus be concluded that the electronic properties of silicon do not obey the high temperature requirements for harsh environments. The intrinsic carrier concentrations as function of temperature for silicon and the most common polytypes of silicon carbide is included in Figure 1.1. It can be seen from this Figure that the intrinsic carrier density for silicon is approaching typical dopant levels (1×10^{14} # /cm^3) for lowly doped regions, while the carrier density for 4H-SiC is around 13 orders of magnitude lower at the same temperature.

From a mechanical point of view, silicon is known to show plastic deformations under small loads from 500 °C and beyond, which limits the feasibility for the development of harsh environment microsystems. To maximize the compatibility of silicon based sensors with harsh environments, silicon on insulator (SOI) wafers are used and extensive packaging is typically required, resulting in higher cost and complexity. Interfacing

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a harsh environment physical transducer at high temperatures, typically involves fiber optics, because analog front-end electronics do not work at elevated temperatures for reasons described above.

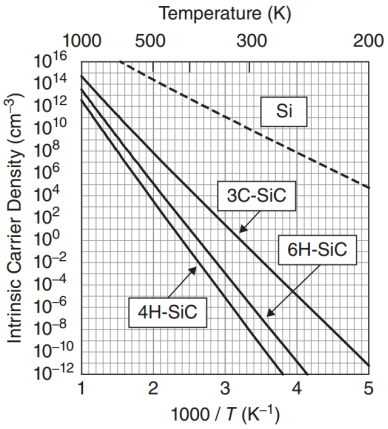

Figure 1.1: An overview of the intrinsic carrier concentration of silicon, compared with the most common polytypes of SiC. Source: [11].

1.3. WIDE BANDGAP SEMICONDUCTORS

Apart from the well-known silicon as semiconductor, many more semiconductors exist. Wide bandgap (WBG) semiconductors (WBS) are semiconductors with an increased bandgap compared to silicon. Well known examples are silicon carbide, gallium nitride (GaN) or gallium arsenide (GaAs). Both are so-called compound semiconductors, SiC being a group IV-IV semiconductor, while GaN and GaAs is a group III-V semiconductor. These group numbers denote the column of each of the compounds in the periodic table of elements. The wider bandgap manifests itself in the physical properties of the material.

1.3.1. POLYTYPES

Two main categories of SiC exist: α silicon carbide and β silicon carbide. When considering a mono-crystalline material, the structure is build-up in unit cells, the smallest cell is called a primitive cell. In the case of α silicon carbide, this primitive cell is hexagonal, typically denoted by an H. The two main polytypes which are commercially available in wafer form are the 4H-SiC and 6H-SiC. In these polytypes, the stacking sequence of the hexagonal bi-layer consisting of silicon and carbon atom repeating itself after 4 and 6 layers respectively [13]. Apart from α-SiC there is β-SiC. The most common polytype in

this category is 3C-SiC, showing an cubic primitive cell (also called a diamond unit cell structure), similar to silicon. The stacking sequence of the three most common polytypes are illustrated in Figure 1.2.

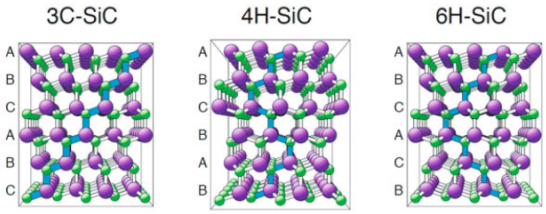

Figure 1.2: An overview three common polytypes. Note the the number of layers before the pattern repeats itself is denoted by the name of the polytype. Source: [14].

In addition to these mono-crystalline occurrences of silicon carbide, polycrystalline and nano-crystalline silicon carbide exist, from which polycrystalline-3C-SiC is most common, because it can be grown by CVD techniques [15]. Nano-crystalline SiC is often referred to as amorphous SiC (abbreviated as a-SiC, not to confuse with α-SiC) and can be used as passivation or isolation layer. Generally, it can be said that in existing silicon carbide technology, 4H-SiC and 6H-SiC is mainly occurring in wafer form and exploited for its excellent electronic properties, whereas poly-3C-SiC and a-SiC is primarily occurring in thin film deposition and strongly related to MEMS processing thanks to the lower cost and larger design flexibility.

1.3.2. PHYSICAL PROPERTIES

The unique physical properties are the result of the larger bandgap and the strong covalent bond between the silicon and carbon atom. A comparison has been made between silicon, silicon carbide and gallium nitride, with the latter two being common WBG semiconductors. The most important physical parameters are summarized in Table 1.1. It can be noted from this Table that the bandgap of silicon carbide is with 2.3 eV for 3C-SiC, 3.26 eV for 4H-SiC and 3.03 eV for 6H-SiC significantly larger than the 1.12 eV of Si. The larger bandgap dramatically reduces the electron-hole pairs caused by external thermal energy, which reduces leakage currents at elevated temperatures which is one of the majors issues with silicon technology in the application of electronics. The wider bandgap also influences the spectral band where the semiconductor can be used to detect the light, which is relevant when photodiodes are developed. As was mentioned before, silicon carbide shows a high electric breakdown field, 1.8 MV cm^{-1} to 3.8 MV cm^{-1} (depending on the polytype) compared to 0.3 MV cm^{-1} for silicon [16].

Table 1.1: Comparison of physical properties of Si, SiC and GaN. *=depends on polytype **sublimation temperature.

Figure	Unit	Si	SiC	GaN
Bandgap E_g	eV	1.12	3.0-3.6*	3.45
Maximum electric field	$V\,cm^{-1}$	$3 \cdot 10^5$	$2.5 \cdot 10^6$	$5 \cdot 10^6$
Relative dielectric constant ϵ_r	F/m	11.8	9.8	8.9
Thermal conductivity	$W\,cm^{-1}\,K^{-1}$	1.5	4.9	1.5
Electron mobility [17] [18]	$cm^2\,V^{-1}\,s^{-1}$	1500	1000	900
Electron saturation velocity [19]	$cm\,s^{-1}$	$10 \cdot 10^6$	$22 \cdot 10^6$	$25 \cdot 10^6$
Hole mobility [17] [18]	$cm^2\,V^{-1}\,s^{-1}$	100-500	40-100	150
Melting point [17] [20]	°C	1410	2830**	2400
Density	$kg\,m^{-3}$	2330	3210	6150
Young's modulus	GPa	62-202	390-690	398
Acoustic velocity	m/s	8415	13100	8044
CTE [17, 21]	$1 \times 10^{-6}\,°C^{-1}$	2.6	4.2	3.17

Further, SiC has a high chemical inertness making it an excellent material for transducers in corrosive environments, while it relaxes stringent packaging requirements. The high Young's modulus opens new design opportunities for the development of silicon carbide MEMS, looking into miniaturization of structures that have mechanically not been feasible in silicon MEMS. This aspect is especially exploitable, since it is known that silicon carbide exhibits a piezoresistive effect, both in mono-crystalline [22, 23] as in polycrystalline form [15, 24]. Silicon carbide is moreover known to have a high radiation tolerance, ideal for space applications [13] and a high acoustic velocity: $11.9 \times 10^3\,m\,s^{-1}$ for SiC vs $9.1 \times 10^3\,m\,s^{-1}$ for Si [25]. SiC has an added benefit over GaN, a high-quality native silicon oxide can be grown which can be used as excellent gate dielectric for the formation of SiC CMOS [11].

From the different WBG semiconductors, this work will focus on silicon carbide. Reasons for this are the availability in crystalline wafer form, as well as in polycrystalline and amorphous forms. In the EKL infrastructure, poly- and amorphous SiC can be deposited increasing compatibility and design freedom. Also the SiC CMOS integration prospect is an important advantage to opt SiC over i.e. GaN. A comparison between Si, SiC and GaN is further illustrated by Figure 1.3 in which the resulting applicable advantages are denoted.

1.4. OMNIPRESENT SENSORS

In the context of the current trend of the Internet of Things (IoT), it is inevitable that sensors will be even more omnipresent in our technological world. Since we are striving for ever more efficient usage of natural resources, time and energy, the integration of sensors and control systems in a broad range of systems can contribute largely to

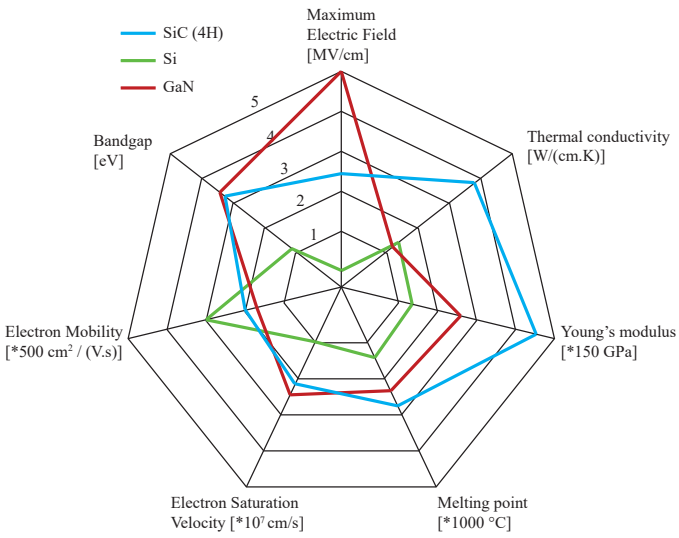

Figure 1.3: A comparison between the different physical properties of SiC and GaN compared to Si. The maximum electric field, bandgap and thermal conductivity properties of SiC favor its usage for power electronic application, where the increased electron saturation velocity enables an increased switching speed. The high Young's modulus and melting point are advantageous for robust MEMS applications. The reduced electron mobility limits however driving capabilities of SiC based CMOS. Reproduced and modified based on [26].

aid achieving these goals. In order to illustrate the immense scope of the sensor market, a tabulated overview is given in Table 1.2. Challenges are for example food security, pollution reduction and mitigation, global warming, growing demand for energy, health and well being. These challenges are translated into applications such as environmental sensing, air quality monitoring, sensors for combustion control (automotive and aviation), sensors for the smart grid and structural and mechanical health monitoring.

1.4.1. HARSH ENVIRONMENT SENSING

As was already mentioned in Section 1.3, SiC features unique physical properties. A high critical electrical field strength and a large thermal conductivity compared to silicon has resulted in the adoption of silicon carbide in power electronics (i.e. IGBTs and Power MOSFETs). As a result of these two physical properties, higher switching speeds are feasible, resulting in lower losses and more compact form-factors of power electronics in general. Larger voltages can be used and less stringent cooling requirements simplifies the packaging of these devices [27]. In addition, thanks to its larger bandgap, and inherent lower intrinsic carrier concentration at elevated temperatures, silicon carbide based active devices such as BJTs and MOSFETs keep showing electronic behavior, even

Table 1.2: An overview of field, applications and sensor classifications.

Field	Application	Sensor classification
Automotive	Exhaust gas monitoring Engine instrumentation Combustion monitoring Electrical drive monitoring Particulate filter monitoring	Temperature Humidity Gas species Vibrations, resonance Particulates
Aviation	Jet Engine Monitoring Structural health monitoring Mechanical health monitoring	Temperature, pressure, flow Stress, strain, pressure Vibrations, flow
Space	Navigation/position sensing	UV blind photo detectors
Earth monitoring	Gravimetry Ocean behavior Oil/gas well monitoring	Deviations in gravity Flow, pressure, temperature Sensing systems
Environment sensing	IoT distributed monitoring system	Particulates 10 nm - 10 µm VOCs Humidity CO, NO_x, SO_x UV index Occupation/traffic density Radiation level, etc.
Health/ sport/well-being	Monitoring *iv-vivo* Excitation	Blood pressure, heartbeat pH, salinity, etc. Pacemaker, neurostimulation
Food security	Measuring toxic substances	Heavy metals Pesticide residues, etc.
Industry	Process monitoring	Temperature, gas species pH value, Ion concentration Pressure Flow, radiation, etc.
Energy	Power grid sensors Offshore wind parks Nuclear Energy Monitoring	Current, Hall sensor EM fields Temperature Stress Strain
Communication	High frequency/RF sensors Antenna/base station monitoring	Temperature, strain Humidity

beyond 500 °C [11, 14, 28, 29]. In recent years, research has been conducted into the application of silicon carbide materials for the fabrication of sensors, mainly intended for harsh environments. Operation at elevated temperatures is the first possible aspect that defines a harsh environment. Temperatures beyond 200 °C can already be seen as harsh, silicon based electronics start to fail namely, but the temperature range can even go up to 800 °C. Alternative harsh environment conditions are the presence of corrosive species (gasses, liquids), high radiation exposure or large mechanical perturbations such as vibrations or pressures [14]. Properties such as a high Young's modulus, high acoustic velocity, high radiation hardness, high chemical intertness and the high melting point make SiC an interesting candidate for many different sensor implementations.

Wright et al. give an overview of different SiC based sensors, ranging from gyroscopes and gas sensors to pressure sensors, along with specific harsh environment applications, such as combustion control and space applications [13]. Senesky et al. discusses the application of SiC sensing structures and electronics specifically for the health and performance monitoring in aerospace systems [25].

1.5. SiC System Integration

To fully exploit the advantages of SiC sensors, they can be made 'smart' by the monolithic integration of SiC based electronics. From a measurement system's perspective it is highly desirable to have the read-out electronics, for example impedance read-out or signal amplification, physically as close as possible to the physical transducer, in order to minimize noise contributions originating from interconnect, EMI or parasitic impedances. These electronics do not necessarily have to be complex circuitry, an output-buffer or relatively simple differential amplifier can be of great value in terms of boosting signal power and enhancing the SNR. Fischer et al. [30] have written a review paper on the benefits and different technological levels on which the integration can take place. As will become clear later, this work focuses on SoC solutions using monolithic MEMS and IC integration by MEMS-last processing via layer deposition and surface micromachining. Furthermore, such a concept results in a measurement system where the read-out takes place directly in the electrical domain. The monolithic integration of read-out electronics omits the need for a sensor read-out based on optical fibers [31, 32]. When more extensive and complex SiC circuitry is considered, also circuits such as ADCs can be integrated.

Moreover, the usage of both a SiC sensing structure and SiC electronics in harsh environments convenience the packaging scheme. The advantages of monolithic integration lie in the nature of dealing with 'one-piece-of-substrate'. Integration on package level typically requires the combination of multiple dies, yielding a so-called System-in-Package (SiP) solution. Such an approach requires interconnects between different dies, by for example 3D packaging or wirebonding techniques [33]. SiP solutions are undesirable from a reliability perspective in case of the applications in harsh environments. Different CTEs of the used materials in a SiP in combination with extremely large temperature variations and vibrations will influence the durability and reliability of such an solution [34]. Rahman et al. shows the concept of monolithic MEMS + ASIC integration for pressure sensors in conventional Si technology [35].

1

1.6. OBJECTIVES

When applying the 'More than Moore' concept on the pathway from silicon toward silicon caride smart integrated sensors, two major challenges can be defined.

1. The investigation of inventive sensor structures and designs to get as much as possible from state-of-the-art silicon based sensor technologies. This can be done by studying non-linear effects in MEMS structures to boost the mechanical sensitivity of a mass/beam system. Additionally, system integration can be applied to improve the performance or to enable new functionalities of sensor systems. The first challenge is pursued in this work by the development of a high-sensitivity accelerometer, to be used as gravimeter. The design of this device is based on silicon technology, where bulk micromachining is mature, and is assisted by spiral resonators to quantify process variations in a pragmatic way.
2. The introduction of WBG semiconductors to the sensor field, thereby importantly extending sensor applications. This is especially relevant in the light of the IoT trend, where there is a growing demand for omnipresent and connected sensors for system optimization. In this trend, sensors are desired in surroundings where existing sensor technologies are not compatible with. This work will focus on SiC technology for availability and CMOS compatibility reasons, giving the possibility for monolithic integration. Despite postulated literature on SiC sensors, there are still gaps to fill [13, 25, 36].

The horizon goal of a monolithically integrated platform for MEMS sensors with ASIC front-end read-out electronics based on SiC CMOS is not shown yet. Such a platform would be the ultimate solution in the context of harsh environment sensing, because of reasons described in Section 1.5. From the two challenges mentioned above, the goals of this work are defined:

1. Stretch existing state-of-the-art Si technology in terms of inventive design choices (exploitation of non-linear effects), while balancing on the edge of fabrication feasibility.
2. Demonstrate and complement the current status of SiC sensor technology.
3. Implement different vacant SiC sensors to display the claimed benefits of SiC technology.
4. Develop SiC CMOS front-end read-out electronics, among other co-integrated active devices.

5. Perform goals 3 and 4 in such a way, that monolithic integration of the SiC MEMS sensors + SiC CMOS is achievable, thereby yielding the horizon target of smart integrated SiC sensors.

To further illustrate the goals and investigations presented in this thesis, a technology roadmap is included in Figure 1.4. The pathway toward integrated smart SiC sensors consists of three steps, SiC technology development, implementation of discrete SiC devices (both MEMS and electronics) and the integration of the SiC sensors with the SiC CMOS. Additionally, the development of inventive designs complemented with system integration in Si technology is illustrated.

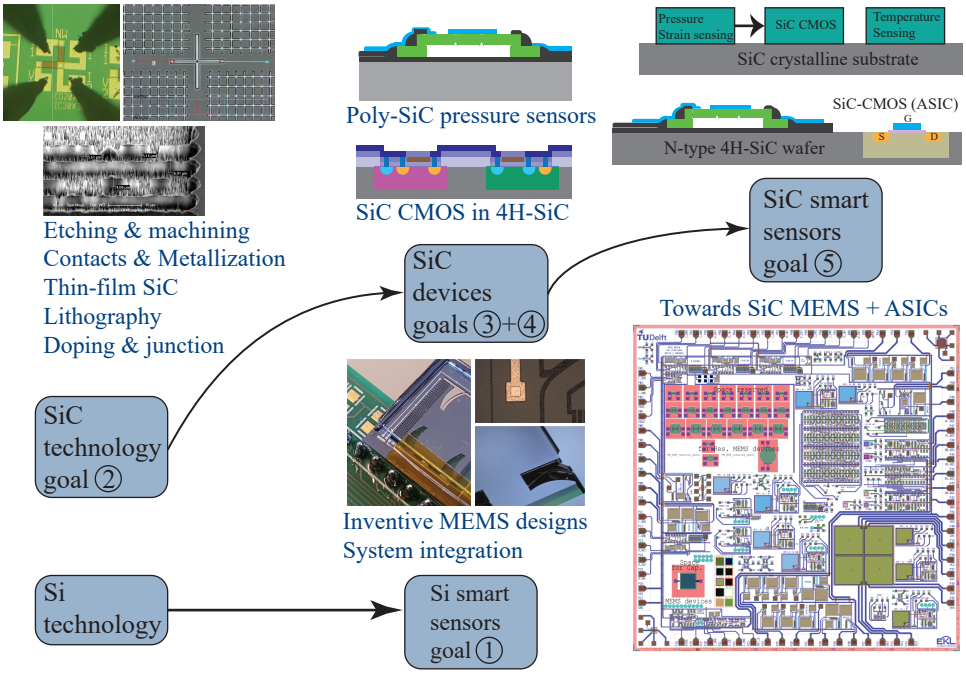

Figure 1.4: The technology roadmap illustrating the direction of this work.

1.7. ORGANIZATION OF THIS THESIS

Chapter 2 shows the design and characterization of bulk micromachined spiral resonators to quantify variation in the lateral dimension of beams etched from a silicon substrate by DRIE. The outcome of this work is used to aid the work as discussed in Chapter 3, in which the design, modeling and realization of a high resolution accelerometer is performed. This accelerometer is intended to be used as gravimeter and exploits

the non-linear buckling behavior of long slender Si beams. These beams show a near-zero spring stiffness at the operation point, boosting mechanical sensitivity of the compliant mass/beam system. An overview of the main cleanroom processes to fabricate SiC sensors is given in Chapter 4. This overview consists of both existing knowledge on SiC processing and performed experiments in the field of lithography, etching and laser ablation. Also, material definition for poly- and mono-SiC was reported, to enable SiC sensor design later in this work. In Chapter 5 a suspended heatable transparent membrane consisting of poly-SiC is demonstrated. This membrane functions as optical window to interface the tailpipe of an internal combustion engine powered vehicle. The optical interface enables the introduction of optical measurement techniques to measure particle mass and number concentrations. The future outlook would be a sensor based on the principles of optical scattering which is part of the on board diagnostics of a vehicle to monitor the performance of the (diesel) particulate filter. The objective of this work is to demonstrate that a transparent SiC membrane can stay clear from soot deposits by two modes of operation, self-cleaning (by oxidation) and contamination prevention (by thermophoretic repulsion). The harsh environment is reflected by the exhaust gas environment and the high temperature (beyond 500 °C) from which the oxidation process takes place. Additionally, an analysis on the application of impedance spectroscopy on an existing soot sensor (electrostatic) was performed and included in Appendix A. In Chapter 6 two different types of poly-SiC based surface micromachined pressure sensors are designed, modeled and realized. Both devices are designed in such a way, that they can be monolithically integrated with SiC CMOS electronics. The piezoresistive properties of poly-SiC are exploited by the implementation of self-sensing membranes, omitting the need for separate piezo resistors and thereby simplifying the fabrication flow. In addition, so-called Pirani gauges are demonstrated based on poly-SiC. These gauges exploit the TCR of in-situ doped poly-SiC. Suspended bridges are fabricated and their resistance upon known biasing conditions is a measure for the absolute pressure, via the heat loss mechanisms of the bridge. In order to work toward the horizon goal of smart SiC sensors, SiC CMOS technology was investigated in Chapter 7. In this chapter the the used technology is discussed and embedded in literature. Low-transistor count analog circuits for impedance read-out of sensors and temperature sensing circuits are designed, fabricated and characterized.

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2

BULK MICROMACHINED SILICON SPIRAL RESONATORS

In this Chapter a method is described to investigate lateral variations across a wafer of high-aspect ratio bulk-micromachined beams by DRIE. This work explores the prospects of the accuracy of high aspect ratio beams, as used for the gravimeter device as will be discussed in Chapter 3. Through wafer MEMS spiral resonators were designed, simulated, fabricated and characterized by measuring the eigenfrequency and corresponding mode shapes. Measuring the eigenfrequency and resulting spectral behavior of resonators on different locations on the wafer was performed by using an optical measurement setup. Two laser beams were used where one is modulated by the periodic movement of the center mass of the resonator. One of the beams is reflected back from the modulated resonator and this beam hits a photo diode. Variations in light intensity due to movement of the resonator provides a measurement signal correlated to movement of the center mass of the resonator. Preliminary measurements showed that measured eigenfrequencies are in correspondence with the simulations within a range of 0-10% deviation. Characterization of the oscillation frequency of the first eigenmode on wafer scale results in a eigenfrequency variation within 0.56 Hz.

Parts of this Chapter have been presented on the IEEE Sensors Conference (2017) [1].

2.1. INTRODUCTION

PROCESS variations can have an adverse effect on the expected operational performance of the designed MEMS devices. 'Process variation at every step in a process flow is an intrinsic part of life in the microfabrication world', which results in the fact that 'real process steps do not make exact replicas of the features on a mask' [2]. Process variations are apparent in steps ranging from lithography to depositions, to etching and will result in variations over the entire wafer. These can result in deviations from the desired behavior of the processed devices. More research is dedicated on characterizing the mechanism causing these variations, for example R.H. Poelma et al. on thin film characterization using electrostatic pull-in [3]. A simple method is considered, which could be used to measure process variation in nanoscale film thickness over the wafer. One of the goals of this research is to stretch the existing mature Si technology, by coming up with inventive sensors design, for example by exploiting non-linear buckling effects of bulk-etch slender beams for the development of a high-resolution accelerometer as is described in Chapter 3. The design of this gravimeter is based on long slender beams which are bulk etched from a Si substrate. Process variations will have a large influence on the anticipated beamwidth of this device of only 5 µm. To investigate the prospects on possible process variations and get some affinity with the feasibility boundaries of the through-wafer bulk etching, spiral resonators were investigated. The process flow considered in this work concerns bulk micromachining using deep reactive ion etching (DRIE), one of the most important processing steps in the fabrication of MEMS and microsystems [4]. Process variation of interest for this work are mainly deviations in lateral direction of through wafer etched structures. To quantify these variations a spiral resonator has been designed and fabricated. In this work we quantify DRIE process variations by measuring changes in the resonance frequency induced by beam width variations over the wafer.

2.2. DESIGN

The designed MEMS resonator has a spiral like structure to achieve a long effective beam length at a relatively small footprint. Optical microscopy can be used to quantify resonance frequency, the resonance frequency is low enough to be captured by camera and human eye. The spiral structure will function as a coiled up spring with a mass at its center. The starting material for fabrication is single crystal double side polished silicon wafer with a thickness of 500 µm. Table 2.1 lists the design dimensions, while Figure 2.1 shows the spiral-spring / mass system. The uncoiled spiral beam can be approximated

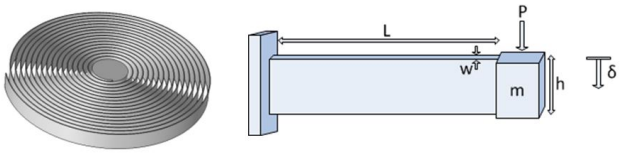


Figure 2.1: The designed mass/spring system and the straight beam approximation.

by a straight beam as shown in Figure 2.1. The out-of-plane deflection of the beam δ is given by equation 2.1, where P represents the force at the end of the beam, L the length of the beam, E the Young's modulus and I the second moment of inertia, which is described for this geometry by equation 2.2. The resulting spring constant is given by equation 2.3 in which w equals the beamwidth and h the height of the beam.

Table 2.1: Design parameters of the resonator.

Figure	Value	Symbol
Beamheight (wafer thickness)	500 µm	h
Beamwidth spiral	20 µm	w
Length of entire spring	183.84 µm	L
Number of turns	17	-
Center mass	0.996 mg	m
Resulting spring constant	0.017	k
Material	Anisotropic silicon	-
Expected out of plane frequency	20.85 Hz	f_0

$$\delta = \frac{PL^3}{3EI} \quad (2.1) \qquad I = \frac{wh^3}{12} \quad (2.2) \qquad k = \frac{P}{\delta} = \frac{Ewh^3}{4L^3} \quad (2.3)$$

FEM simulations were performed to determine the resonance frequency for multiple mode shapes. The first eigenfrequency is 29.436 Hz and the corresponding mode shape is depicted in Figure. 2.2, from which it can be noted that the center mass is displaced in the x,z-plane, thus in the wafer plane (in-plane). At 30.448 Hz the mode shape is found in which the center mass is oscillating orthogonal to the wafer plane (out-of-plane), which is also illustrated by Figure 2.2.

2.3. FABRICATION

A silicon oxide layer is deposited on each side of the 500 µm double side polished wafers, where the front layer is used as hard mask for the Deep Reactive Ion Etching (DRIE) process step while the backside layer is used as an etch stop layer. An additional aluminum layer is used at the backside to prevent helium leakage in case of cracks in the oxide landing layer. After the DRIE step was performed, the aluminum layer at the backside

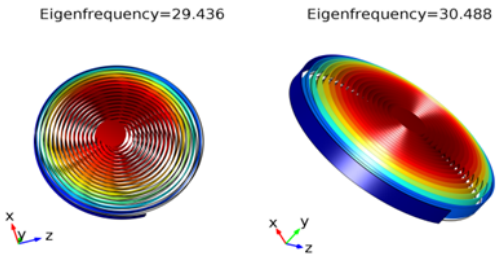


Figure 2.2: The first and second mode shapes corresponding to respectively eigenfrequencies of 29.436 Hz and 30.488 Hz.

was removed by a RIE etch step to release the resonator. The silicon oxide layers were removed by hydrofluoric acid (HF) vapor. During the processing, the sag of the center mass can be useful as a preliminary indication for the process variations. This sag can easily be measured using an regular microscope focusing on either the wafer or the center mass.

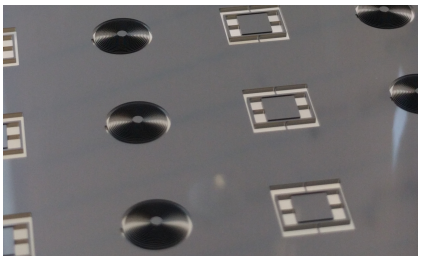


Figure 2.3: Realized spiral and torsional (not measured) resonators.

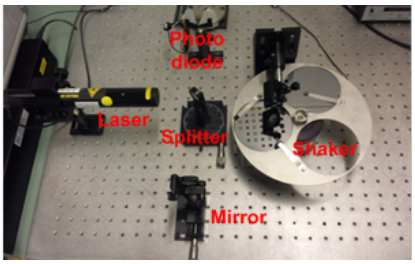
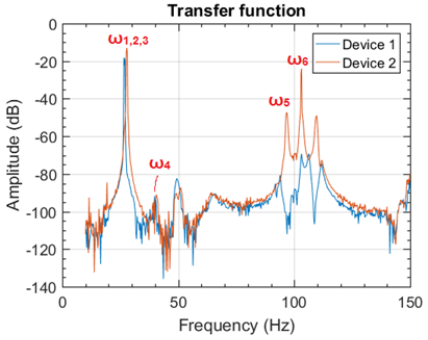


Figure 2.4: The used measurement setup.

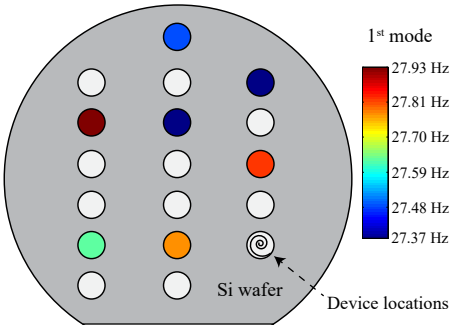
2.4. MEASUREMENTS AND CHARACTERIZATION

The resonators were characterized using a spectrum analyzer, a mechanical shaker and an optical read-out setup. The spectrum analyzer provides a source signal to a current source driving a mechanical shaker. This shaker forces a mechanical excitation with a certain frequency on the wafer with the resonators. The movements of the resonators are detected using an optical measurement setup, based on two interacting light beams resulting in a varying shadow effect. The photodiode detects the laser beam reflected by the resonator and sends the signal to a network analyzer. The detected light intensity varies caused by the movement of the resonator mass which results in variations of the measured signal. The optical setup uses a laser at a wavelength of 633 nm where the

beam passes through a beamsplitter. One beam is received by the photodiode via a mirror, whereas the other beam is modulated by the resonator under test. The light beam which is incident on the center mass of the resonator will be modulated by the motion of this center mass and reflected back toward the photodiode sensor. Depending on the position of the surface of this center mass during movements, the reflected light beam will either be aligned with the unmodulated light beam, or will be shifted resulting in not being detected by the photodiode. The photodiode will therefore measure a varying light intensity, depending on the position of the reflecting center mass of the resonator. This position will be determined by the movement of the resonator, caused by a mechanical excitation of the shaker. When the resonator starts to oscillate according to the excitation signal, the amplitude of the movement of the center mass will increase dramatically (resonating frequency) and the incident light beam will be modulated to a larger extend. In the current experiment we estimate that the displacement is too large so the setup is not operating in an interferometric mode. The current signal measured by the photodiode is converted to a voltage and fed-back to the spectrum analyzer, after which the transfer function is determined (| Received Signal/Source |).



(a) The transfer function of the measurement of two measured resonators.



(b) Color map of the measured first eigenmode across the wafer. The uncolored devices have not been measured.

Figure 2.5: Measurement results on the characterization of the spiral resonators.

2.4.1. MEASUREMENT RESULTS AND DISCUSSION

When characterizing the devices, the excitation signal from the spectrum analyzer is swept from 10 Hz up to 150 Hz. The amplitude of the bode plot of the transfer function between the transmitted excitation signal to the power amplifier of the shaker and the received signal from the current amplifier is shown in Figure 2.5a. The first unambiguous peak in the amplitude is located at 26.78 Hz and 27.78 Hz for devices 1 and 2

Table 2.2: Comparison eigenfrequencies in Hz.

Mode	Simulation	Meas. dev. 1	Meas. dev. 2
1st	29.436	26.78	27.78
2nd	30.102	-	-
3rd	30.448	-	-
4th	36.116	39.8	40.56
5th	94.924	93.9	69.66
6th	101.2	103.2	103.2

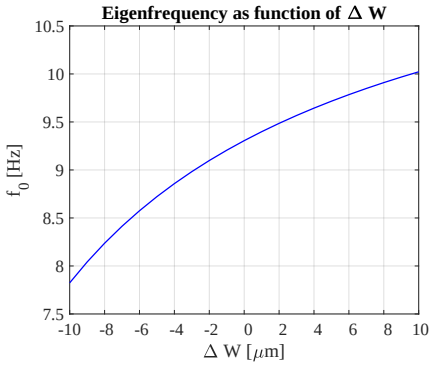
Table 2.3: Values used for the sensitivity analysis.

Figure	Value
E	130 GPa
w	20 µm
h	500 µm
L	183.84 mm
r	678.28 µm
Δw	−10 µm to 10 µm

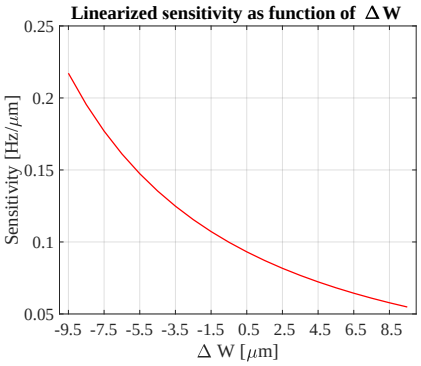
respectively. A comparison for the frequencies for the first, fourth, fifth and sixth mode shapes is included in Table 2.2. What is notable from this table is that the first three eigenfrequencies are within 1 Hz of difference from each other, which implies that the k/m ratio in plane and out of plane are for this operation region similar. Considering that the excitation signal is swept in step of 0.5 Hz, it will limit the spectral resolution. Furthermore can it be expected that the peak in the transfer function at about 27 Hz is a 'combined' oscillating mode, the 2nd and 3rd mode merge and are detected as one peak, because the first three modes fall within 1 Hz bandwidth. The resonator in this work was designed as a first iteration where the first three modes are close to each other. In some applications this phenomena is called veering (near crossing) where two vibration modes get close to each other using electrothermal and electrostatic actuation to form a band pass filter [5]. In this work, this was not the intended effect. Additionally, the first and second modes are in-plane while the third mode is in the out of plane direction. The movements are orthogonal which suggests that the stiffness in-plane and out-plane are similar where the difference in frequency could be attributed to the changing mass distribution due to the resonator beam movement. Additionally, the resonance frequencies of the first eigenmodes were characterized across the wafer. This result is graphically summarized by a color wafermap as included in Figure 2.5b from which can be concluded that the variation in the oscillator frequency of the first eigenmode equals 0.56 Hz.

2.4.2. SENSITIVITY ANALYSIS

A sensitivity analysis was performed to link a deviation in the frequencies of a specific eigenmode for different resonators to a variation in the lateral dimension of the beamwidth. The height of the beam is fixed to the wafer thickness and a possible variation in beam length can be neglected when taking into account the total length of the beam being in the centimeter range. This leaves the mass and the width w of the beams as the main process variations parameters, which will influence the resonance frequency. The sensitivity can be obtained by revisiting the analytical derivations. Cal-



(a) The eigenfrequency as function for the process variation Δw.



(b) The linearized sensitivity based on the plotted eigenfrequency.

Figure 2.6: Results of the sensitivity analysis.

culating the eigenfrequency from a beam with certain stiffness k and a mass m yields the following equation 2.4, where m_{eq} stands for the equivalent mass.

$$\omega_0 = \sqrt{\frac{k}{m}} = \sqrt{\frac{Ewh^3}{4L^3 m_{eq}}} \tag{2.4}$$

This 'equivalent mass' actually consists of the mass of the beam itself and the center mass 2.5.

$$m_{eq} = m_{beam} + m_{center} = \rho_{Si} hLw + \rho_{Si} hr^2 \pi \tag{2.5}$$

Combining equations 2.4 and 2.5 and adding a process variable Δw results in equationn 2.6. It can be concluded from this equation that both the stiffness coefficient k and the equivalent mass m_{eq} are affected by a the process variation Δw.

$$\omega_0(\Delta w) = \sqrt{\frac{k}{m}} = \sqrt{\frac{E(w+\Delta w)h^3}{4L^3(h\rho_{Si}(\pi(r+\Delta w)^2 + \frac{1}{2}L(w+\Delta w)))}} \tag{2.6}$$

Equation 2.6 was used to plot the eigenfrequency and the derived sensitivity to ΔW using MATLAB. For this analysis, an out-of-plane (second eigenmode) was used, in combination with the parameters as listed in Table 2.3. In Figure 2.6a the eigenfrequency is plotted as function of the lateral width. In Figure 2.6b the derivative of this eigenfrequency characteristic is plotted. The sensitivity around the operating point of a Δw of 0 is equal to $0.10\,\mathrm{Hz\,\mu m^{-1}}$, which is equivalent to $10\,\mathrm{\mu m\,Hz^{-1}}$.

2.5. CONCLUSION

Process variations in microsystem fabrication such as bulk- or surface micromachining is unavoidable and can result in deviations from the desired behavior of realized devices. In this work a simple resonator was designed, simulated and fabricated. A measurement setup is designed to identify the mechanical spectral behavior of the realized resonators. The two measurements showed that measured eigenfrequencies are in correspondence with the simulations within a range of 0-10% deviation. From the results it can be concluded that the mechanical structures and the measurement setup can be used to extract information on the (lateral) width of through wafer etched structures. Based on the analytical model a sensitivity analysis was performed using MATLAB, which resulted in a linearized sensitivity of $10\,\mu m\,Hz^{-1}$.

Revisiting our first goal as included in Section 1.6, it can be concluded from this Chapter that compact resonators can be realized by bulk micromachining of silicon substrates. The high aspect-ratio beams (functioning as springs) of the realized devices have a width of only $20\,\mu m$, while the height equals the wafer thickness of $525\,\mu m$. The experience on the realization of low-stiffness bulk micromachined structures will be used in the next Chapter for the development of a high-resolution MEMS gravimeter. The obtained results are for example used to correct for process variations during the lithography step, by adapting exposure energy, which results in a refined process control. Future work includes measurements of all realized devices in order to determine the process variation over the wafer and to determine the sensitivity more precisely. Another recommendation would be to design resonators where the resonance frequencies of the different eigenmodes are further displaced from each other.

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3

HIGH-RESOLUTION MEMS GRAVIMETER WITH INTEGRATED CAPACITIVE READOUT

Although commercially available gravimeters and seismometers can be used for measuring Earth's acceleration at resolution levels in the order of ng/$\sqrt{\text{Hz}}$ (g represents earth's gravity), they are typically high-cost and bulky. In this Chapter the design of a MEMS device exploiting non-linear buckling behavior is described, aiming for ng/$\sqrt{\text{Hz}}$ resolution by maximizing mechanical and capacitive sensitivity. High mechanical sensitivity is obtained through low structural stiffness. Near-zero stiffness is achieved through geometric design and large deformation into a region where the mechanism is statically balanced. Moreover, the device has an integrated capacitive comb transducer and makes use of a high-resolution impedance readout ASIC. The sensitivity from displacement to a change in capacitance was maximized within the design and process boundaries given, by making use of a trench isolation technique and exploiting the large displacement behavior of the device. Measurements demonstrate that the resonance frequency can be tuned from 8.7 Hz *to* 18.7 Hz *depending on the process parameters and the tilt of the device. In this system, which combines an integrated capacitive transducer with a sensitivity of* 2.55 aF nm^{-1} *and an impedance readout chip, the theoretically achievable system resolution equals 17.02 ng/$\sqrt{\text{Hz}}$. The small size of the device and the use of integrated readout electronics allow for a wide range of practical applications for data collection aimed at the IoT.*

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Parts of this Chapter have been presented on the IEEE Sensors Conference (2018) [2] and on the IEEE EuroSimE Conference (2018) [3].

3.1. INTRODUCTION

To exhibit what can be achieved by combining non-trivial design choices, system integration with mature Si sensor technologies, it was decided to develop a micro-machined gravimeter with integrated readout. Reasons for this application to illustrate our first goal is because measurements of Earth's gravitational field are becoming exceedingly important in building understanding of our planet's behavior, ranging from earth crust movement and volcanic eruptions, to oil- and water pocket exploration and detection [4]. From the field of gravimetry it is known that there are small variations in the gravitational force of the earth, typically caused by tides and ocean loading, local and global hydrology, volcanology, seismic activity and the presence of oil pockets. These variations are in the order of nano-g (ng) to micro-g (μg). The collection of data from a dense grid of sensors detecting deviations in the earth gravitational force can be used to predict not only locations of oil- and water pockets in water-scarce environments, but also the movement of tectonic plates in the field of seismology and earthquake predictions. To accomplish this, gravimeters with high sensitivities in the order of 1-100 ng/$\sqrt{\text{Hz}}$ are required for measuring the smallest changes in local gravitational acceleration [4]. However, commercially available high-end gravimeters and seismometers are typically large in form-factor, because rather extensive measurement techniques are used, i.e. falling masses. The underlying physical factors which complicate the development of relative and open-loop ng/$\sqrt{\text{Hz}}$ MEMS-based accelerometers, are the high mechanical sensitivity to be achieved and the displacement of a proof mass to be read out. High mechanical sensitivity in a relative MEMS-based accelerometer is directly related to the low resonance frequency of the structure, resulting in low stiffness and high mass requirements. The magnitude of the proof mass is limited by the available chip area, especially since miniaturization is typically one of the major advantages of MEMS technology. The low stiffness of the springs used is limited by process limitations, for example the minimum resolution for etching. Lastly, combining a large proof mass with low stiffness springs inherently requires mechanical robustness and reliability to be considered. Working out these challenges can thus result in a miniaturized, integrated, low-cost system capable of ng/$\sqrt{\text{Hz}}$ measurements that contributes to the recent advances in the Internet of Things (IoT) [5].

In mass/spring-based accelerometer implementations, there is an inherent trade-off between operational bandwidth and resolution [6]. The bandwidth which is of most interest to the field of gravimetry ranges from the µHz up to several Hertz, which corresponds to variations over a period of days down to intervals of seconds. Examples of such signals are secular deformation, seismic modes and ocean tides [4]. The price paid

by the increase in mechanical sensitivity, namely a lower bandwidth, is in line with the bandwidth requirements for the intended application field.

Recently, more research has been presented on the development of a miniaturized microelectromechanical system (MEMS) implementation of gravimeters by Middlemiss et al. [7]. Here a MEMS gravimeter has been fabricated using bulk silicon micromachining for the design which is based on the non-linear buckling of beams to enable high sensitivity reaching 40 μGal/$\sqrt{\text{Hz}}$. Since 1 Gal equals 1 cm s^{-2}, this sensitivity equals 40 ng/$\sqrt{\text{Hz}}$. The resonance frequency of the mass/beam system of this work is 2.3 Hz. The key feature of this work is the concept of exploiting non-linear buckling behavior to obtain low stiffness and thus high mechanical sensitivity within a micromachined structure. However, the design does not further exploit the IC technology for the readout of the motion. Instead, this work employs an optical shadow sensor with bulky dimensions as an intermediate step to the electrical domain. An integrated capacitive transducer, in combination with an on-board integrated ASIC, would lead to a significant reduction in cost, facilitate further miniaturization, and significantly improve noise level performance.

Li et al. [8] have fabricated a linear MEMS device that achieves 30 ng/$\sqrt{\text{Hz}}$ with a resonance frequency of 13.2 Hz. The competing value for the resolution was obtained by making use of a specially designed course/fine capacitive readout scheme. Nevertheless, the fabrication of this device is more complex, since the three dies need to be stacked to form the capacitive readout. This introduces fringe- and large parasitic capacitances resulting in high noise contribution and lower sensitivity. The device uses linear springs, which have to be much stiffer than in the self-limiting non-linear design of this work to prevent catastrophic damage over the entire deflection range. In contrast to this work, the use of non-linear near-zero stiffness springs enables further improvement in the achievable resolution. Depending on the capacitive readout ASIC employed, a system resolution even beyond ng/$\sqrt{\text{Hz}}$ would be feasible. Another advantage of non-linear springs which only locally show a near-zero stiffness, is that the dynamic range is not determined by the low spring constant alone. When an external force moves the non-linear spring out of its operating region, which is where it has minimum locally linearized stiffness, a deterministic response can still be measured despite the increase in stiffness.

Pike et al.[9, 10] presented a mass/spring based accelerometer with resonance frequencies ranging from 0.1 Hz to 12 Hz. Impressive resolution figures are presented, 2 ng/$\sqrt{\text{Hz}}$ [9] and 0.25 ng/$\sqrt{\text{Hz}}$ [10]. However, it should be mentioned that a closed-loop implementation is used, requiring more back-end signal processing. Additionally, the layer

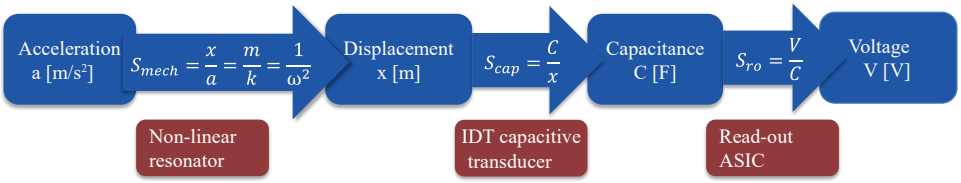

Figure 3.1: System overview of the gravimeter; note the different sensitivities between every physical domain.

based transducer design featuring gold bars and micro positioned transducer strips implies more extensive processing compared to the objectives of this work. In terms of miniaturization, the die size of 25 mm suggests room for improvement, especially for low-cost IoT applications. Compared to the work of Pike, this work specifically focuses on the development of an open-loop gravimeter exploiting standard CMOS compatible materials and technologies within a minimal die size.

The main drawback of state-of-the-art high-resolution accelerometers is thus the absence of a MEMS device capable of sub-Hz resonance frequency operation combined with an integrated readout scheme, while being fabricated in a CMOS compatible cleanroom and within a minimal die size. This combination would enable miniaturization, (monolithic) integration with electronics and low-power operation. Furthermore, it enables direct transduction from the mechanical domain to the electrical domain instead of going via the optical domain.

The objective of this work is to design, fabricate and qualify an extremely compact ng/$\sqrt{\text{Hz}}$ open-loop type inertial sensor, fully based on MEMS and ASIC technology, which could even be monolithically integrated. The mass/beam system is designed for optimized sensitivity, torsional stiffness and integration with a capacitive transducer, which can be directly wirebonded to a PCB containing the readout ASIC. To the best of our knowledge, this paper is the first in the literature featuring the combination of a non-linear MEMS device with an integrated bulk micromachined high-sensitivity capacitive transducer intended for high resolution acceleration measurements.

To achieve this objective, first a sensitivity analysis was performed over the different physical domains, as shown in Figure 3.1. By maximizing the sensitivity of each transduction, the noise of the subsequent stage in the sensor system is suppressed. By maximizing both the mechanical sensitivity and the capacitive sensitivity, and choosing a high resolution impedance readout scheme, a system resolution in the order of ng/$\sqrt{\text{Hz}}$ is aimed for, while keeping the operational bandwidth at 1 Hz.

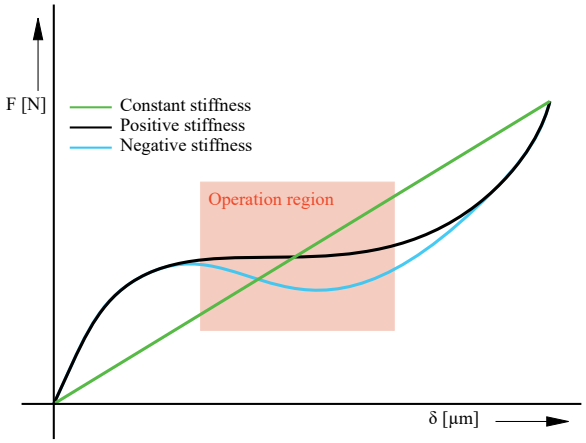

Figure 3.2: Mechanical beam force/displacement behavior showing: constant high positive stiffness (green), low local positive stiffness (black), and low local negative stiffness (blue).

3.2. DESIGN

Non-linear stiffness characteristic This work makes use of a non-linear effect which occurs in long slender beams, called buckling [11, 12]. If the geometry of the beams is designed properly, this buckling can result in a localized region where spring-softening occurs. Consequently, for certain displacement values the spring constant lowers, despite it being bounded by an increasing spring constant for displacements out of this range. This results in a local low-stiffness region in the force displacement graph, as shown in Figure 3.2.

A negative spring stiffness is not desired in this design, because multiple operating points would exist for the same reaction force applied causing snap-through to possibly occur, as is observed in bi-stable structures. Low stiffness of the beams results in high mechanical sensitivity which scales down the noise contribution in the mechanical domain, such as Brownian motion or environmental noise, and the noise sources in the subsequent capacitive and electrical domains, as illustrated in Figure 3.1.

Mechanical Design The design of the device structure is divided into modular parts: mass/beam structures including the electrodes and isolation trenches (Figure 3.3b-d). Concretely this means that the device consists of a multi-image mask of which different versions can be combined during the lithography step of the fabrication process. Advantages of this are the more efficient use of reticle space and more processing flexibility, because different versions of the design parts are available. For example, two

different trench widths are designed to ensure reliable filling of the isolation material later on.

The transducer structure consists of a proof mass, four slender beams, and four capacitive-comb electrodes, depending on the modular design options used. Different proof masses with different shapes and dimensions have been designed to be compatible with the different types of capacitive transducer structures. Three types of electrode dimensions have been designed to enable fine and coarse sensitivities. A minimum of four suspension beams are required to increase rotational and torsional stiffness. The beams are attached to the mass near the vertical axis of symmetry. This not only increases the rotational stiffness, but also makes the design more compact, because the beams require a certain length to combine the buckling effect with low spring stiffness.

The mass of the mass/beam system, being designed and fabricated planar, can travel over a distance in the order of millimeters, which is relatively large for a 10 x 10 mm^2 device. If the device is oriented vertically, the gravity force is in line with the displacement direction of the mass. The beams should be designed such that at this force they are pushed into the shape in which the buckling effect manifests itself and displays the constant stiffness region behavior Stopping structures have been designed to limit the deflection of the proof mass in case of high shocks to prevent self-damage.

Geometric optimization The dimensions and design parameters of the mass and beam are described in Figure 3 and have been determined iteratively using the known mechanical beam relation between them, originating from the beam theory of Timoschenko [13]. The parameters that were changed in the design to simultaneously obtain the correct resonance frequency and operating point at 1 g were: the sector angle of the beams, the rotation of the beams, the radius of the beams, the beam height and width and the value of the proof mass. The starting point is located at a beam height of 5 µm, which is the lowest beam height that can be fabricated. The beam radius and design angles determine the spacing each beam occupies, which affects the rotational stiffness. By reducing the radius to an optimum while increasing the mass width between two adjacent beams, the torsional stiffness increases. The spacing between the beams along with the radius are limited by the minimum device size. The resulting geometry of the interdigitated (IDT) design is included in Figure 3.3a. The design of the mass/beam system was evaluated using the force-displacement relation obtained through a finite element analysis (FEM) in COMSOL. In the simulations the length and thickness of the beam were 3588.4 µm and 5.4 µm, respectively. The radius and sector angles were 4000 µm and 0.8971 rad, respectively. The value range for the different parameters depends on

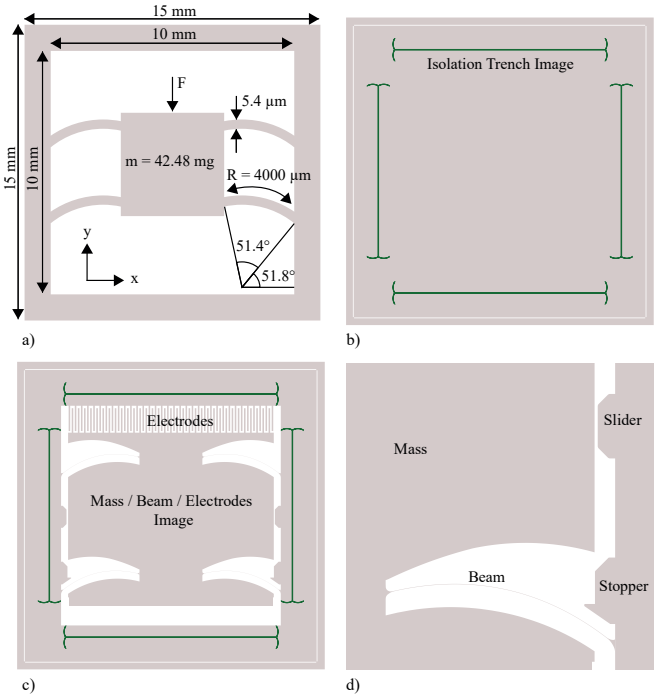

Figure 3.3: Geometrical design of the MEMS device. a) Geometry of the mass/spring system, b) Trench isolation image, c) Mechanical device with IDT electrodes, d) Designed slider and stopper structures.

the modular design.

The first simulation described covers the investigation of the force/displacement characteristic of the beams. The beams were modeled as 2D and 3D solid mechanics structures, with the inclusion of a non-linear solver. With the aid of prescribed displacement, the reaction forces were obtained. To transfer the reaction forces using the value of the proof mass, the y-axis was scaled to plot the acceleration values according to Newton's second law, as shown in Figure 3.4a. The spring stiffness derived is the first-order derivative of the force-displacement relation. The result is included in Figure 3.4, where the lowest value of the spring stiffness corresponds to the operating point around the acceleration force, which corresponds to the nominal 1 g gravitational acceleration.

To ensure convergence in the mechanical simulations of the large-displacement nonlinear design, a downward prescribed displacement is imposed on the proof mass in the physics section of the model. The displacement corresponding to the operating point then serves as the input to the resonance frequency analysis. The result is included in Figure 3.4c, which shows the resonance frequency dependency on displacement with

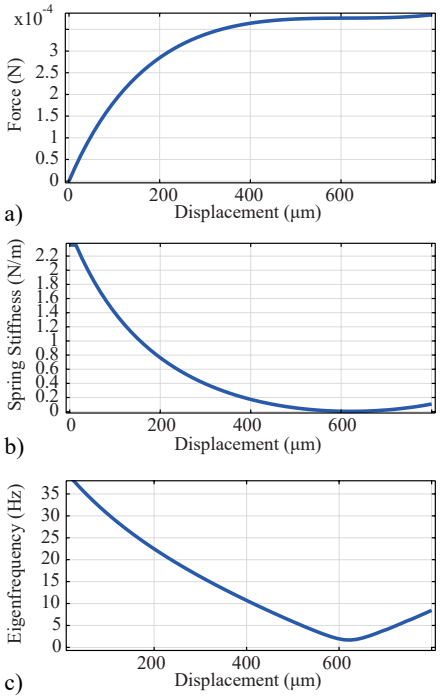

Figure 3.4: FEM simulation results on the non-linear spring design. a) Force vs. deflection of the proof mass in the y-direction, b) Stiffness as a function of displacement in the y-direction, c) Resonance (Eigen)frequency as a function of displacement.

the lowest resonance frequency reaching 1.68 Hz, which corresponds to the first eigenmode in the y-direction at the operating point as shown in Figure 3.4c. The resonance frequency analysis further showed a second eigenmode beyond 107 Hz.

Despite the high aspect ratio and the layout of the geometry, deflections besides those in the y-direction may cause a disturbance in the signal of interest due to a finite spring stiffness in unwanted directions. By maximizing the spring stiffness for the x- and z-directions, the risk of damage caused by plastic deformation instead of elastic deformation is minimized. This aspect is especially relevant in this work because the ratio of the mass-spring constant has been pushed to the limits of feasibility in order to obtain high mechanical sensitivity.

The FEM simulations conducted to obtain the spring constants in both the x- and z-directions were carried out in the same manner as for the y-direction, except that the direction of the prescribed displacement was changed to the x- and z-direction, respectively. The proof mass is first set to the deflection corresponding to the operating point (1 g) in the y-direction by a prescribed displacement imposed on the mass.

Consequently, the reaction forces and spring stiffness in the other directions were determined from the operating point at 1 g with a deflection around 800 µm. The lowest stiffness in the 1g operating point in the z-direction is 2×10^4 times higher than in the y-direction. To give an estimation of the error caused by the out of plane displacement, a displacement of 50 µm in the y-direction would result in a displacement of 3 nm at a tilting angle of 34°. The resulting capacitive error is then 1×10^{-3} %. The stiffness in the x-direction is initially similar to that in the y-direction and increases rapidly beyond a value of 1.2×10^5 N m^{-1} after 20 µm of displacement, due to spring stiffening. A tilt with respect to the vertical axis can be applied to the device, resulting in a decreased y-component acting on the proof mass. By doing so, the operating point and stiffness are changed accordingly. Thanks to the high stiffness in the z-direction, the response of the sensor is not compromised by the out-of-plane force. The amount of deflection and thus the spring constant can be varied in this way, providing a trade-off between bandwidth and sensitivity.

Design of the capacitive IDE transducer While aiming for maximum capacitive sensitivity, the sensitivity in terms of ΔC was determined. For this analysis, a simplification was used, in which a linear addition of parallel plate equivalents is used. See also equation 3.1 below.

$$\Delta C_{tot} = \frac{2N\epsilon_0\epsilon_r t(y_0 - y)}{d} \tag{3.1}$$

In which N equals the number of fingers, ϵ_0 the permittivity of vacuum, ϵ_r the relative permittivity, t the thickness of the structure (in this work wafer thickness), (y_0-y) the displacement in the y-direction and d the gap between the electrodes. It can be concluded from equation 3.1 that the change in capacitance is maximized by maximizing the number of fingers within the available design space and reducing the gap d between the IDT fingers.

The transducer is designed in such a way that it would be compatible with a bulk micro machined mass/beam system suspended in a frame of 10x 10 mm, which puts the first geometrical design constraint. The lateral comb drive structure helps to reduce damping caused by air surrounding the structure. This can be explained by the couette flow, occurring for lateral motion, being much less dissipative compared to the squeeze film damping. Thanks to the main objective of measuring mechanical signals in the sub 20 Hz range, the fluid inside the gaps has enough time to displace but also prevents the air to act like a spring which is storing and releasing energy at higher frequencies [14]. Additionally, the damping can be further reduced by using vacuum packaging.

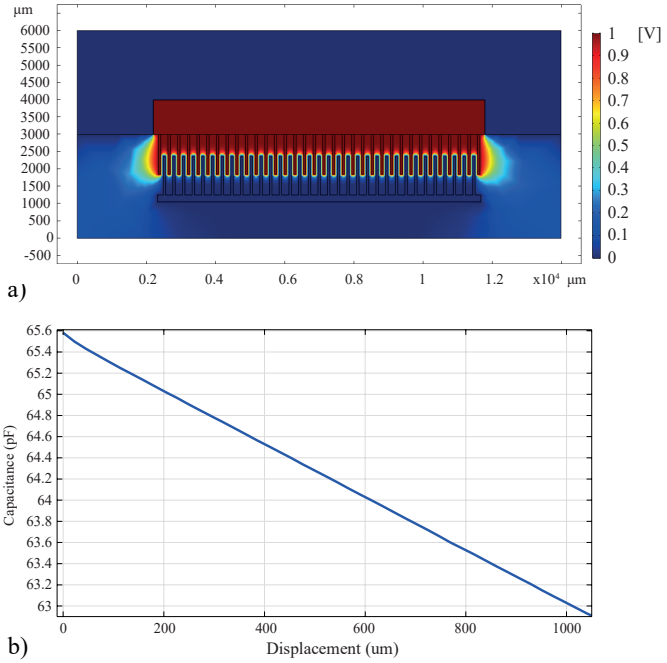

Figure 3.5: Results of the capacitive FEM simulations. a) The potential distribution across the IDT based on 1 V excitation, b) The resulting capacitance as function of the displacement.

Capacitive simulations have been performed in order to investigate the electric field distribution and verify that the absolute value of the electric field does not exceed the dielectric strength of air. To simulate the capacitive response, an interdigitated (IDT) electrode was placed across a second moving electrode. The capacitance/displacement behavior is included in Figure 3.5b. As can be concluded from this result, the capacitance varied from 35.58 pF to 33.47 pF. The values on the y-axis however show larger values for the capacitance, because the trench for electric isolation is also included in this value. From this result it can be concluded that the capacitive response as a function of deflection is highly linear with a large capacitive change per nm distance. Taking the first order derivative of the capacitance versus displacement characteristic in the linear region yields a sensitivity of 2.55 aF nm^{-1} in the displacement region of interest.

The high degree of linearity in the capacitive response can be explained by the large number of fingers. The non-linear effect of the fringing E-field on either side of the electrode array is suppressed by the large contribution to the total capacitance of the normal components of the field between the parallel 'fingers'. To illustrate this, the electric field distribution is included in Figure 3.5a, where the fringing E-field (boundary) effects are

visible. Additionally, it can be noted that the aspect ratio of the structure is high: The width of each finger equals only 70 µm, whereas the thickness of the structure equals the wafer thickness of 300 µm. The large width of each finger suppresses the non-linear effect caused by fringing fields at the beginning and end of the IDE finger array, while the large height of each IDE finger suppresses the fringing fields on front- and backside of the wafer.

Parasitic capacitances The IDT structure is fabricated from the same substrate as the mass/beam system. Therefore, an electrical isolation was required and was realized using trenches filled with a dielectric. As a result, parasitic capacitances between the main frame and the IDT electrode regions inevitably arise. Additional parasitic capacitances are caused by the metal traces connecting the different potential regions with the probe pads. Both sources of parasitic capacitances are illustrated in Figure 3.6a.
The dielectric material is silicon nitride (Si_3N_4) for both the trenches and interconnect parasitics. To analyze the parasitic capacitances an equivalent circuit model was made, based on the actual way of interfacing the sensor. This equivalent circuit model is included in Figure 5d illustrating the capacitances as these will appear across the connection pads. The subscript including an 'i' denotes a parasitic caused by the metal trace whereas a subscript including 't' denotes a parasitic caused by an isolation trench.

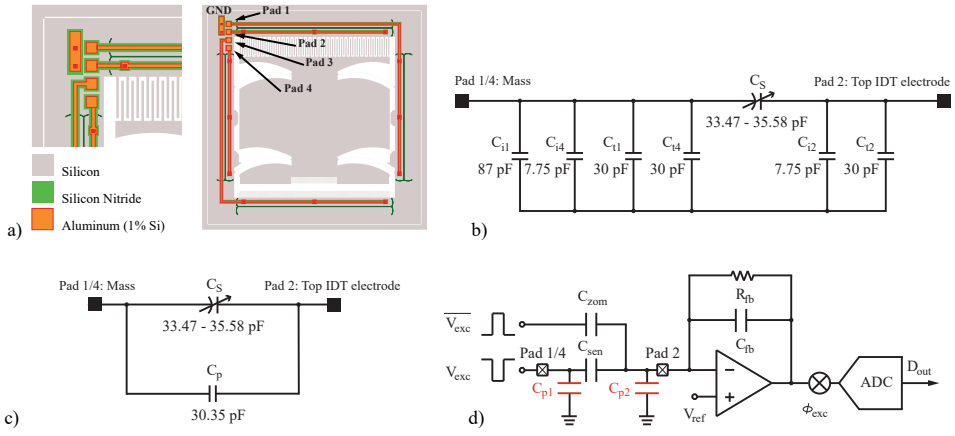

Figure 3.6: a) A schematic overview of the device including trenches and interconnects, b) The equivalent circuit, including lumped elements for parasitic capacitances caused by isolation trenches (denoted with subscript t) and interconnects (denoted with subscript i), c) The equivalent parasitic capacitance across the sense capacitor in case of floating GND, d) The topology of the high-resolution impedance read-out ASIC.

All the parasitics on either side of the sensor capacitance C_s can be simplified to one parallel capacitor by omitting the ground connection, reducing the total parasitic ca-

pacitance. The equivalent circuit in this case is included in Figure 3.6c. However, in this case the parasitic capacitance will be in parallel to the sense capacitance. This effect is undesired, because charge redistribution from the measurement signal over the parallel capacitor occurs. This would result in a worse system performance compared to the parasitic capacitance being connected to ground, as shown in Figure 3.6b. The best way of connecting the sensor is summarized by Figure 3.6d, thus including the connected ground.

To operate the capacitive sensor, a square-wave signal V_{exc} is applied, at a frequency higher than the corner frequency defined by R_{fb} and C_{fb}. Simultaneously, the zoom-in capacitor, C_{zom}, is excited by a signal, inversed V_{exc}, to cancel the baseline capacitance, thus maximizing the use of the capacitance to voltage converter's (CVC) available dynamic range. The sensing signal induced capacitance changes modulate the excitation current. The resulting amplitude modulated AM signal is then amplified and demodulated back to in-band. As the modulated sensing signal is processed by the amplifier in high frequency where the 1/f noise is not dominating, the noise performance of the CVC gets improved. Finally, the voltage signal is digitized by an analog-to-digital converter (ADC).

Fabrication considerations and geometry The displacement is read out using an IDT capacitive structure etched in the silicon substrate along with the mass/beam system. Since the electrodes are made from the bulk silicon, both electrodes of this transducer consist of low-ohmic silicon, which requires electrically isolated regions to facilitate the readout process. The target chip area of 10x10 mm^2 needs to be taken into account when designing the capacitive transducer for maximum sensitivity, which restricts for example the maximum number of fingers in the IDT array. The IDT has been designed with finger widths and air gaps of 70 µm and a capacitive sensitivity of 2.52 aF nm^{-1}. The overlap between the fingers starts at 1040 µm and decreases for increasing deflection.

Because both electrodes of the capacitive transducer are bulk-micromachined from the same substrate, electrical isolation is required. This is done by etching trenches nearly 100 µm deep and filling these with silicon nitride for isolation and mechanical connection purposes. Figure 3.8b shows a SEM image of the etched trench with a depth of 97.3 µm and width of 3 µm. Figure 3.8c-d show the SEM images of the trench before and after being filled with Si_3N_4 as isolator. The spring stiffness in unwanted directions (x- and z-direction) is at least two orders of magnitude larger with respect to the y -direction. Additional structures are included to limit large translation and rotations and to prevent electrodes from touching. Stopping structures are included in the design to

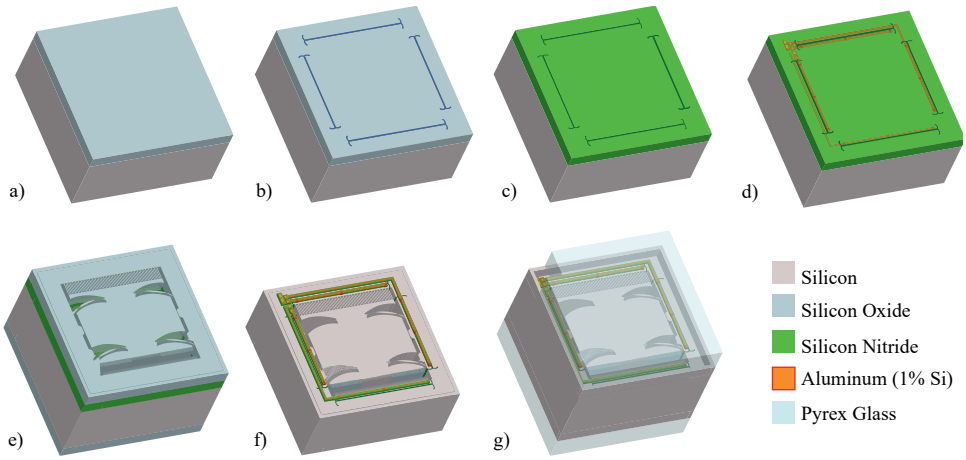

Figure 3.7: The process flow used during fabrication. a) Hard mask deposition, b) Trench isolation patterning, c) Trench filling with Si_3N_4, d) Metal interconnects on the front, e) Deposition of the landing layer stack, frontside hard mask deposition and patterning followed by bulk DRIE etching, f) Releasing the device by vapor HF of the landing oxide layer, g) The final packaged device.

prevent the electrodes from short circuiting in the lateral direction as a result of large forces. Figure 3.3d shows these structures.

3.3. FABRICATION

The fabrication of the inertial transducer was performed in a CMOS compatible cleanroom and using MEMS microfabrication starting with 4-inch p-type silicon wafers (300 µm thick) with a resistivity of 10 Ω cm. First, electrical isolation steps for separating the electrodes from the bulk were followed. The steps consisted of (1) etching silicon from the frontside through trench formation, (2) filling the trenches using low pressure chemical vapor deposition (LPCVD) silicon nitride (Si_3N_4) for electrical isolation and mechanical adhesion, and (3) etching the remaining silicon from the backside to complete the electrical isolation. The latter was achieved after the definition of the mass/beam structures in the silicon. After every pattern etching step, a cleaning procedure was performed to remove any organic material such as the photoresist or polymer used for wall passivation in the deep reactive ion etch (DRIE) etching process.

Figure 3.7a-c show the first electrical isolation step where a silicon oxide (SiO_2) masking layer was deposited on the frontside of the substrate, patterned using standard lithography and etched using reactive ion etching (RIE). Hereafter a DRIE step was performed to etch 100 µm deep trenches. Subsequently, the substrate was cleaned after which the SiO_2 masking layer was then removed using 1:7 Hydrofluoric acid (HF) wet etching. The

etched trenches were then filled with the isolation material in three steps. Each of these steps consisted of a deposition followed by a planarization without masking until the substrate was exposed. This method helps in minimizing the risk of voids forming and in achieving a more uniform surface, which is an advantage during the later contact metallization step. Prior to the last deposition step a boron implantation step was performed for ohmic contact formation with a dose of 1×10^{15} cm^{-3} at an energy of 20 keV. A cross-section of the device is schematically shown in Figure 3.8a, whereas SEM pictures of the etched trench and the filling process are included in Figure 3.8b-d. Because the Si_3N_4 layer is also used as isolation layer between metal interconnect and substrate, after the third deposition, no subsequent etching was performed, as illustrated by Figure 3.7c. The annealing step of the implantation was then carried out simultaneously with the last LPCVD deposition step at 800 °C. To connect the device to the outer world, contact openings were etched into the Si_3N_4 layer. Subsequently a 1 µm aluminum layer (Al) with 1% Si was deposited for metal interconnects and was patterned using standard lithography and inductively coupled plasma (ICP) etching for metals (Figure 3.7d). A microscope image of the realized interconnect is included in Figure 3.8f.

To complete the electrical isolation and define the mass/beam structures two DRIE etching steps were performed. The steps consisted of the deposition of SiO_2 masking layers at the frontside and backside, respectively. Starting with the backside, the masking layer was patterned with isolation trenches to complete the electrical isolation. This was achieved using standard lithography followed by RIE and DRIE etching steps. Similarly, the frontside was patterned with the mass/beam structures. The DRIE etching step was performed until a through-wafer etch was achieved. Figure 3.7e shows the resulting structure. The last steps were the removal of any unwanted materials such as the passivation layer by an oxygen plasma, the Al capping layer by ICP etching, and the SiO_2 hard masks by vapor HF etching. After the vapor etching, the devices were released manually through vibrations during which the released halo-structures detached from the substrate (Figure 3.7f). Figure 3.9a shows a picture of the device as it was realized using this procedure.

Packaging and integration of the readout ASIC After the dies were released in the cleanroom, packaging was needed to protect the proof mass from contaminants that could block the IDT structure. The packaging shields the mass/beam system from air flow, which may damage the device. Because the device is based on the concept of buckling using large displacement behavior, it is desired to use a packaging solution that allows visual inspection. The silicon die is therefore packaged on both sides using

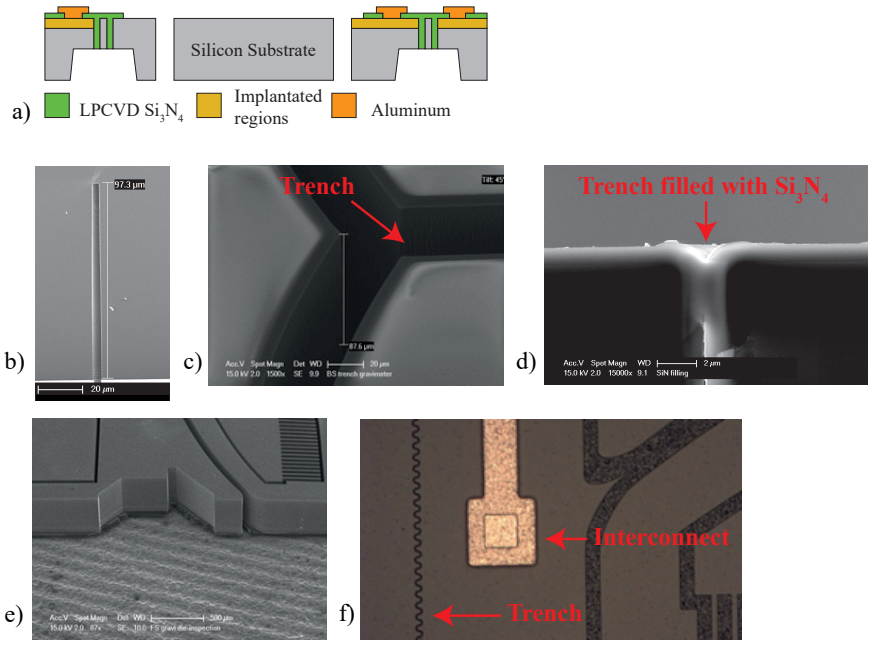

Figure 3.8: a) The cross section showing the trench isolation technique, b) Etched trench with a depth of 97.3 µm and a width of 3 µm, c) Top view of etched trench, d) Etched trench filled with SiN as the isolator, e) SEM image of the DRIE etched structures before release, f) A microscope image in which the metal trace and the isolation trench can be seen.

glass dies fabricated from a Pyrex wafer, as illustrated in Figure 3.7g. Because the sensor is bulk micromachined, the moving parts have the same thickness as the rest of the die, in this case the frame. To allow the mass to move freely within the glass-silicon-glass stack, silicon spacers are used to have a controlled and known separation between the mass/beam system and the outer glass dies. The stack of glass outer dies, spacers and MEMS-chip is glued together by ultraviolet (UV) curable Norland Optical Adhesive.

The readout ASIC has a measurement range of 80 fF. Although the readout ASIC has a 10 pF on-chip capacitance and a digital-to-analogue converter (DAC) to compensate the baseline and the parasitic capacitance of the sensor, such as the ones originating from the isolation trenches and interconnecting metal traces. To minimize the parasitic capacitance or inductance in the packaging scheme further, the sensor has been directly wire-bonded onto a PCB housing the ASIC and I/O to the DAQ system, as is displayed in Figure 3.9b. These wirebonds will introduce (minimal) parasitic capacitance and inductance, but since the variation in C around an equilibrium position is of main interest, these parasitics will not affect the measurement. The PCB has numerous options for capacitive readout, such as capacitance offset compensation and connections for bridge

readout. A die photograph of the high-resolution impedance read-out ASIC is included in 3.9c. The 'daughter PCB' housing the MEMS device and read-out ASIC installed on the I/O PCB is included in Figure 3.9d.

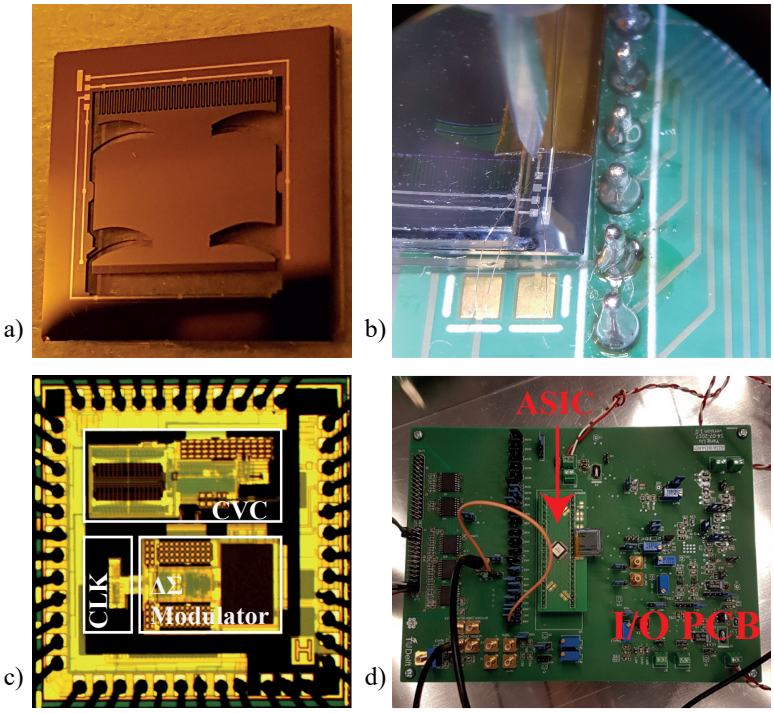

Figure 3.9: Packaging and integration of the fabricated MEMS device with the read-out system PCB and ASIC. a) Final device after release, b) Wirebonding of the with glass dies packaged MEMS device onto the PCB housing the read-out ASIC, c) Die photograph of the read-out, d) PCB in the measurement setup, along with the metal casing to shield the setup from EMI.

3.4. MEASUREMENTS AND CHARACTERIZATION

The devices were tested by clamping the PCB onto a manual tilting stage and increasing the tilt from a horizontal starting position. Accordingly Earth's gravitational acceleration of 1g is scaled with the sine of the tilt angle. As a result, bringing the proof mass to the 'biasing point' where low spring stiffness occurs can be performed in a highly controllable manner. As a test signal, the mechanical shaker from Brüel & Kjaer (model 4810) was used, exciting a sinusoidal signal in the frequency range of the first resonance frequency of the devices. This range was determined by observing the displacement amplitude of the proof mass while manually varying the excitation frequency. When the excitation signal passes the resonance frequency, resonance in the mass beam system is triggered

and the movement of the proof mass shows a periodic behavior.

The readout chip makes use of a Sigma-Delta-based ADC with a sample rate of 2 MS/s. The digital bitstream is decimated by averaging a specific number of bits, which returns to the concept of over-sampled data converters. By choosing the decimation factor, there will be a trade-off between the sample rate in the time domain and the resolution per sample. The decimation factor used here equals 1×10^4. Subsequently MATLAB was used to further analyze the measurement data. The first measurement result is illustrated in Figure 3.10a, showing two seconds from a five-second interval during a frequency sweep from 5 Hz to 9 Hz in the time domain. Despite the presence of noise and drift, the periodic signal of the resonance behavior can be clearly recognized. The noise was probably caused by interference from the surroundings, such as 50 Hz disturbance or Electromagnetic Interference (EMI) from the measurement equipment to the exposed wire bonds. When determining the average period of the time domain signal, it can be concluded that the frequency corresponds to the 8.7 Hz resonance frequency value.

Frequency domain: Tilt measurements After the time domain signal was analyzed based on the discrete sample, the PSD of the signal was derived by applying an FFT operation on the data. For the analysis of the mechanical spectrum of the sensor chip, the effect of different tilt angles was investigated in this series of measurements. The tilt of the sensor was varied from 23° to 34°. For every measurement a sweep of the mechanical excitation signal was performed while the capacitance was simultaneously sampled. The spectrum of the measurement results is included in Figures 3.10b-c. Here the resonance frequency can be clearly distinguished from the noise level, and is decreasing with increasing tilt angle. This response on the tilt angle can be expected from the combination of a fixed proof mass in combination with a softening spring. With increasing deflection, which is in turn caused by a larger tilt, a larger value for the gravitational force is working on the proof mass. The capacitive transducer is designed for device operation in line with the acceleration under test. Since we apply a tilt in this series of measurements, it can be expected that, due to the finite stiffness in the 'out-of-plane' direction, the magnitude of the capacitive response is influenced. The tilt measurements are used to identify the location of the resonance frequencies. In a final application, the tilt will be 90°, resulting in no 'out-of-plane' movement.

The tilt measurements show that the resonance frequency of the sensor is tunable by varying the tilt. As a result, the mechanical sensitivity, being a direct function of the stiffness and thus implicitly related to the resonance frequency, of the sensor is also

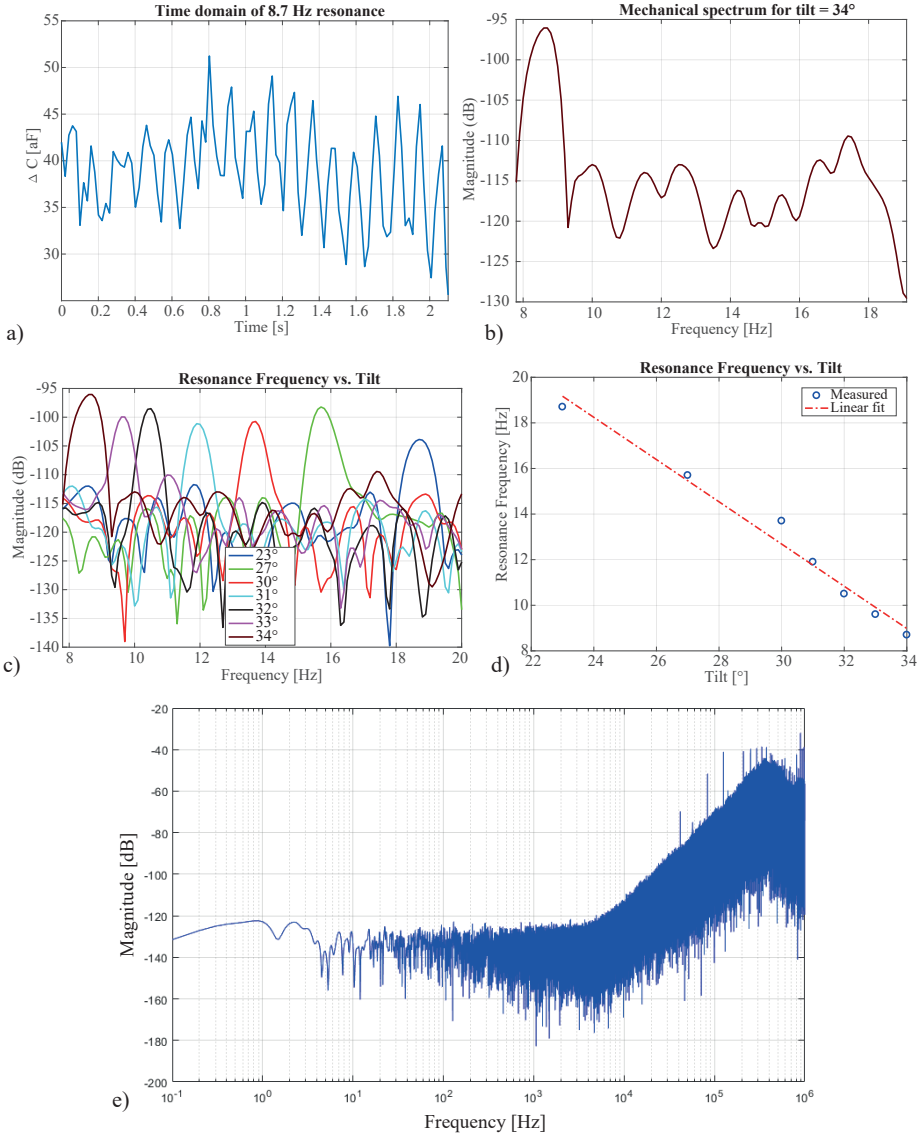

Figure 3.10: Measurements results in time and frequency domains and the noise floor of the CVC. a) Measurement during resonance of the device at a tilt angle of 34° (time domain), b) Measurement during resonance of the device at a tilt angle of 34° (frequency domain), clearly showing the resonance tone at 8.7 Hz, and c) Mechanical spectrum of the device for tilts ranging from 23° to 34°, d) Resonance frequency as a function of the tilt, e) Noise floor of the capacitive readout chip.

tunable. The lowest resonance frequency obtained with the fabricated sensor chip is 8.7 Hz with a tilt angle of 34°.

To further investigate the relation between the tilt angle and the resonance frequency, both figures are plotted against each other in Figure 3.10d. The plot in this Figure was obtained by taking the maximum values from Figure 3.10c. It can be concluded from this result that the resonance frequency is highly sensitive to the tilt angle. Every 1° of increased angle results in a drop in the resonance frequency by approximately 1 Hz, which is significant in this low frequency range. The degree of linearity can be explained by the simulation result included in Figure 3.4c. The resonance frequency equals the square root of the stiffness over the mass, the first one being simulated to show a linear behavior with deflection and the second one being constant. This measurement shows again that by applying a tilt to the sensor chip, a trade-off can be carried out over the dynamic range, in terms of the operational bandwidth and measurement range, and mechanical sensitivity.

Sensitivity analysis of the measurement system The minimum detectable acceleration is determined by transferring back the total noise in the measurement system to the input. The two noise sources considered in a capacitive accelerometer are the thermal-mechanical noise and the noise originating from the analogue front-end electronics [15]. Determining the input-referred resolution is done by dividing each noise contribution by the sensitivities applicable, in this case the mechanical- and capacitive sensitivities. The first one is dictated by the resonance frequency, whereas the second one is taken from the design of the IDT structure. The thermal-mechanical noise comes back to the derivation of the fluctuation-dissipation theorem [15], which basically means that the damping mechanism in the system produces a noise density based on the damping constant and temperature. In the design of this sensor, no additional damping was added, which means that the mass can move freely within its structure. The only damping available is that of the intrinsic damping of the material and that of the surrounding air. To analyze the thermal-mechanical noise, also called Brownian motion noise, the following derivation, which is already translated from force noise via displacement noise to acceleration noise, was used. The formula is described by Senturia [16].

$$a_n = \sqrt{\frac{4k_B T \omega_0}{mQ}} \tag{3.2}$$

where k_B is the Boltzmann constant, T the absolute temperature, ω_0 the angular reso-

nance frequency, m the mass of the proof mass and Q the quality factor, which is in this case determined with:

$$Q = \frac{f_0}{f_2 - f_1} \tag{3.3}$$

for which f_0 is the resonance frequency, and f_1 and f_2 are the −3 dB frequencies on either side of the tone.

Using the lowest resonance frequency obtained, 8.7 Hz, a mechanical quality factor for the structure of Q=12.43 is yielded and an input-referred system resolution value is obtained for a_n=4.03 ng/$\sqrt{\text{Hz}}$. Packaging of the resonator under vacuum will improve the quality factor, by reducing the damping by the (squeezed) air around the moving proof mass, in turn reducing the thermal noise contribution by a lower damping coefficient b.

The resolution of the capacitive readout scheme, including the current to voltage converter (IV-converter) and ADC, within a BW of 20 Hz is 0.137 aF/$\sqrt{\text{Hz}}$ (ASIC specification). With a capacitive sensitivity of 2.52 aF nm^{-1}(design), this corresponds to a displacement noise of 0.054 nm/$\sqrt{\text{Hz}}$. Using the lowest resonance frequency measured and the second derivative of the harmonic oscillation, the mechanical sensitivity equals:

$$S_{mech} = \frac{x(m)}{a(\text{m s}^{-2})} = \frac{1}{(2\pi 8.7)^2} = 3.35 \times 10^{-4}\,\text{m m}^{-1}\,\text{s}^{-2} \tag{3.4}$$

The resulting resolution in terms of acceleration is 1.62 m s^{-2}/$\sqrt{\text{Hz}}$. By normalizing this to values of a gravitational constant, a value of 16.54 ng/$\sqrt{\text{Hz}}$ is obtained.

Assuming that the noise contribution from the thermal mechanical noise and the electronic noise from the front-end are uncorrelated, both input-referred noise power sources can be added and taking the square root. This results is 17.02 ng/$\sqrt{\text{Hz}}$.

3.5. CONCLUSION

In this work, a bulk micromachined mass/beam system has been designed, simulated, fabricated, tested and characterized. The device was processed, packaged using glass dies, and wire bonded to a PCB containing a readout ASIC. The realized MEMS device with an integrated capacitive transducer was packaged and directly wire-bonded to a high resolution impedance readout system. By using the non-linear force/displacement characteristic of buckling beams, an operating point has been created with extremely low stiffness. The vertical displacement of the proof mass is readout by a capacitive transducer which is integrated into the same bulk micromachined silicon die. This is possible thanks to the trench isolation technique, which electrically separates both parts

of the silicon bulk while keeping lithographic lateral resolution. The presented concept shows the potential for an integrated platform of an extremely compact MEMS + ASIC gravimeter, both on the package level, or even a monolithically integrated CMOS in the MEMS device.

When combining the lowest resonance frequency of 8.7 Hz, the capacitive sensitivity and the experimentally characterized noise floor of the readout chip, the theoretically obtainable system resolution equals 17.02 ng/$\sqrt{\text{Hz}}$. This figure for the theoretically obtainable resolution shows that the integration of the non-linear buckling-based compliant mass/beam system with the bulk micromachined capacitive transducer yields a concept for a high resolution MEMS based accelerometer. The proof of concept is promising for future iterations to yield a low-power, miniaturized and integrated MEMS solution for high-resolution acceleration measurements. Although stoppers have been designed to make the device robust against shocks, robustness testing and more extensive packaging design is open for future research.

This brings us to the first goal as postulated in Section 1.6. The realized gravimeter illustrates what can be achieved by combining inventive design choices with state-of-the-art Si technology and the concept of system integration. The unconventional exploitation of non-linear effects of the long slender beams enables competing device performance in the field of high-resolution accelerometers. It can be concluded that existing silicon technologies gives ample room for novel high-impact transducer and sensor designs.

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4

Silicon Carbide Process Technology Development

When considering the difference in maturity level between silicon and silicon carbide technology, one can conclude that numerous challenges lay ahead. In order to make the transition from Si to SiC sensor technology, this Chapter demonstrates the current status of SiC technology and complements it with multiple experiments. Topics covered are lithography, etching, laser ablation, contact formation, metallization and concludes with a description of the modeling details of both 4H-SiC and 3C-SiC in polycrystalline form. It was found that lithography is rather straight-forward on 4H-SiC substrates and that even through-wafer alignment is feasible. Etching of thin-film 3C-SiC in polycrystalline form is possible with selectivities to PR up to 2.5. Deep etching of 4H-SiC substrates is highly challenging. Reasons for this are a relatively low selectivity and poor hard mask stability. Laser ablation experiments were carried out from which it can be concluded that through-wafer etching is feasible, but due to the nature of the ablation process, etch-depth control, surface finish, thermal loading and contamination should be further investigated. Based on literature, it was found that ohmic contacts require dedicated thermal processing yielding interface reactions between the metal-SiC. Ohmic contacts to polycrystalline SiC are achieved by hot-sputtering Al and Ti on lightly doped poly-3C-SiC layers. The materials properties that are relevant to this work are investigated for crystalline 4H-SiC and poly 3C-SiC. In the last Section, the refractive index and extinction coefficient of different poly-layers were characterized. The outcome of this Chapter is an important foundation for the design choices later in this work, when the development of SiC sensors is considered, along with the outlook to monolithic integration with SiC CMOS electronics.

4.1. INTRODUCTION

CURRENT fabrication methods of MEMS and microsystems are based on mature silicon technology, which came forth from active devices and CMOS, and has evolved to the term 'CMOS compatible'. The development of deep reactive ion etching (DRIE) extended fabrication possibilities to large extend, resulting a high level of maturity of silicon sensors [1]. In this work, the transition from silicon sensors to silicon carbide sensors is discussed. Further motivation and resulting challenges to go from Si toward SiC for harsh environment sensing is described in the Chapter 1 and by the book Chapter by Middelburg et al. [2]. In the last two decades, multiple books have been published specifically on the topic of silicon carbide physics and technology in the context of realizing microsystems and electronics. Examples are the books by Kimoto and Cooper [3], by Wijesundara and Azevedo [4], Cheung [5] and Choyke et al. [6]. These books provide a starting point regarding physical knowledge and give direction for concrete fabrication steps on different types of silicon carbide. However, before the design and realization of SiC devices, such as sensor structures and electronics, can be considered, practical implementation of this knowledge is of importance. Even more, while this results in a framework on which design considerations and choices will be based later in this work. Concretely bringing in practice the knowledge and practices as supplied by literature is what is aimed for in this Chapter, in order to build the so-called technological foundation, on which later realistic and implementable device designs can be based. Note that, especially in the case of silicon carbide technology, the fabrication possibilities and limitations are largely dictating device design, even more than currently the case for mature silicon technology in which ample possibilities exists thanks to a legacy of decades of process experience.

Reasoning in the context of the horizon objective of this research, monolithically integrated SiC MEMS devices with electronics, the different topics covered were determined. An essential processing step in on any SiC substrate is lithography, as will be covered by Section 4.2. The inertness of SiC in general implies already that etching of, especially mono-crystalline material, is non-trivial. Therefore, a relative large part of this Chapter is dedicated to investigation of etching on both crystalline 4H-SiC as polycrystalline 3C-SiC, as described by Sections 4.3 and 4.4 respectively. Exploratory laser ablation experiments were carried out and the resulting experiences are discussed in Section 4.5. Contact formation and metallization are addressed in Section 4.6 and this Chapter is concluded with the description of modeling parameters of different types of SiC in Section 4.7.

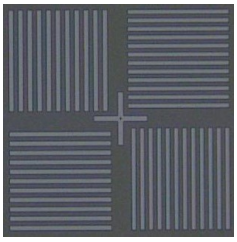
4.2. LITHOGRAPHY ON 4H-SIC SUBSTRATES

Performing lithography on 4H-SiC wafers appears to be similar to lithography on silicon wafers which has been standardized for decades. One of the aspect that is different is the reflectivity of the surface of the surface of the substrate. Because this basically comes back to tuning the interplay between exposure energy, development time and the number of development puddles, and because this tuning is also applicable in silicon technology, no special attention is given to this aspect in this section. A second aspect that needs to be taken into account for the lithography on silicon carbide substrates is the fact that the wafers are transparent, this simultaneously can introduce challenges and enable alignment through the wafer.

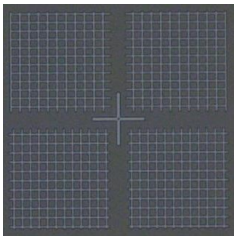
In the infrastructure of EKL, an ASML PAS5500 wafer stepper is used and initial tests showed that, despite the wafers being opaque in some parts of the visible spectrum, the wafer handling by the stepper is not giving any complications. Because the refractive index of silicon carbide is significantly lower compared to silicon (n_{SiC} = 2.64 vs n_{Si} = 3.42), and because the wafer stepper makes use of an interference pattern of the alignment markers, the automatic alignment is non-trivial. In order to investigate the issues described, lithography experiments are carried out on 4H-SiC substrates.

A feature that could be enabled is the backside (BS) alignment *through* wafer. By doing so, the stepper performs the BS alignment as if it would be a frontside (FS) alignment, by 'looking' through the wafer to the 'real' frontside of the wafer (which is now on the backside). The advantage of alignment trough the wafer is that no special BS alignment jobs need to be programmed. In combination with the mirror symmetric alignment markers, the exposures on both front side and back side of the wafer can be carried out without modifications to the alignment settings of the wafer stepper. Because normal alignment markers would be mirrored too when the wafer is flipped over for BS alignment, causing the alignment not to work anymore, so-called 'omni' alignment markers exist. These markers are mirror symmetric. Figure 4.1 shows both the regular alignment markers (Figure 4.1a) as the omni marker (Figure 4.1b) patterned on the photoresist (PR) on the 4H-SiC wafers. Details on the etching process is included in section 4.3. The wafer was coated with 3.1 µm AZ3027 photoresist (PR) and an exposure energy of 320 mJ cm^{-2} was used. The reason that a relatively thick PR layer was used, typically 1.4 µm is used for zero layer processing on silicon substrates, is because it is known that SiC is very hard material resulting is much lower etch rates and worse selectivity against PR compared to silicon zero layer processing. After development both the normal and omni markers are inspected with the Keyence, as is indicated in Figure 4.1. After inspection, the markers are etched using dry-etching techniques using the Alcatel GIR300, more details on the

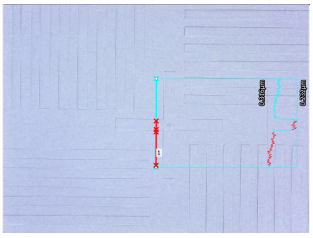
topic of 4H-SiC etching will be given in section 4.3. The reason that the Alcatel etcher was used, is that this tool would not give wafer handling issues as would be the case when the Trikon Omega etcher would be used.



(a) A picture of a standard alignment marker etched in the mono-crystalline SiC wafer.



(b) A picture of the omni marker, it can be noticed that the lines are replaced for a grid structure.



(c) Measurement of the etched depth of the normal alignment marker in 4H-SiC substrates.

Figure 4.1: Inspection of different types of alignment markers before and after etching and stripping. Note the high degree of contrast before etching for this semi-transparent wafer.

After etching, the wafer is stripped using and oxygen plasma and subsequently cleaned using the standard silicon cleaning. After the rinsing and drying step, the etched alignment markers are inspected using the Keyence VK-X250 confocal microscope. The measurement result is included in Figure 4.1c etch depth was measured to be 55 nm. The depth of these markers is significantly less compared to the aimed 120 nm which is used for silicon. With these markers in place on the wafer, the standard FS alignment was tested and gave no problems, even with the marker depth of 55 nm. The BS alignment by using the omni markers on the FS of the wafer, thus through the wafer, also worked trouble-free. This illustrates the high sensitivity of the interference based alignment system of the used wafer stepper, and would enable BS alignment without altering the standard wafer stepper job setup and settings.

To test the repeatability of the alignment, dedicated alignment tests are available within the stepper. In these test an alignment marker location is given on which one wants to perform the test. Then multiple (i.e. 10) scans are carried out on this specific marker. In every scan the chuck is moved and alignment is performed. The machine coordinates are registered in a test report reported by the wafer stepper, and after all scans have been performed, the shift of the machine coordinates, which can be directly translated to a shift in wafer coordinates, is listed. This can be used as statistical data about the reproducibility of the measurement. Because the omni marker has less effective area compared to the standard ASML alignment marker, the shift during these reproducibility tests is typically larger. The maximum shift for the omni markers was found to be 6 nm for the normal alignment marker only 3 nm. For the back side alignment proce-

dure *trough* the wafer, the values for these shifts were found to be 150 nm for both types of alignment markers, which is in the same range as the overlay specification of the stepper. The larger value for these shifts between different alignment repetitions can be explained by the fact that the light has to travel through the wafer in this case causing a bending of the light beam and thus translating to an error in the position of the alignment marker. Because the initial alignment markers are not etched deep enough (55 nm, as also described above), for redundancy reasons additional markers will be exposed which will be etched sufficiently deep. The marker positions of these redundancy markers is chosen such that also the global alignment works on these markers. All markers in this additional stepper job are the omni markers, because the standard alignment procedure works error-free with these markers and both FS and BS alignment through the wafer is feasible. The added alignment markers for this job are placed on the bottom and top of the wafer, in a row of three alignment markers. On the bottom side of the wafers, the three omni markers are shifted to the center of the wafer with 3 mm, because the SiC wafers carry wafer numbering by laser markings just above the flat. To make sure that the additional alignment markers and these markings do not interfere, the offset to this array has been given.

4.3. ETCHING 4H-SIC

For the development of SiC based MEMS sensors, the etching is an essential processing step. The availability of etch methods for SiC bulk materials directly determines if bulk micromachining of this material is a feasible way to go for cleanroom fabrication of microsystems based on this material. Due to the chemical inertness and robustness, thanks to the strong covalent bond between the silicon and carbon atom, the etching of SiC materials is non-trivial. Among the different types of SiC (bulk, thin film) and polytypes, it can be expected that especially for mono-crystalline SiC it is difficult to achieve high etch rates, inherently posing challenges to selectivity against masking materials. This section is dedicated to investigate the different types of etching mono-crystalline SiC bulk material.

4.3.1. TYPES OF SIC ETCHING

Before investigating one of the etch methods in detail, an overview of different methods is given. Mainly spoken, there are three different types of etching mono-SiC:

1. Reactive Ion Etching (RIE). Mainly done by using chlorine or fluorine based chemistries, whereby a high degree of anisotropy can be obtained.

2. Wet chemical etching using molten KOH in the temperature range of 400 °C to 600 °C. This type of etching is highly challenging because of the high temperature. Furthermore this type of etching is isotropic.

3. Photoelectrochemical (PEC) etching. This type of etching makes use of a KOH solution in combination with UV light and an electrical bias between the substrate and the solution. The type of etching is depending on the dopant concentration. Known disadvantages from literature are however a rough etched surface, poor etching uniformity of the wafer and the inability to pattern small-dimension features. In general it is easier to etch n-type layers than p-type layers with PEC etching [3].

Because wet chemical etching with molten KOH etches isotropic and because the high temperature poses realization challenges this technique will not be investigated further within this work. PEC etching might be a viable option, but also requires a dedicated setup and has known disadvantages. RIE on the other hand has the advantage of being anisotropic.

4.3.2. PHYSICS ON REACTIVE ION ETCHING

Yih et al. [7] describes the mechanisms and gasses used in general for the plasma etching of different kinds of SiC. Multiple tests are described, namely the etching of polycrystalline 3C-SiC layers, the etching of doped 4H-SiC and 6H-SiC. As masking material an aluminum mask was used. The gasses which were investigated for this etching are CH_4, SF_6, NF_3, $CBrF_3$ and CHF_3 and mixtures of these gasses. It was found that a combination of the gasses SF_6 and O_2 yields the highest etch rate. Metal masking layers provide clearly the highest selectivity, best is to use ITO, Cr or Ni. From the book [4] on the other hand it can be summarized that the presence of oxygen in the etching process has multiple functions. Firstly it is one of the main reactive components in the etching plasma by the following reactions:

$$Si + xF \rightarrow SiF_x \quad (4.1) \qquad C + yF \rightarrow CF_y \quad (4.2) \qquad C + zO \rightarrow CO_z \quad (4.3)$$

As can be concluded from the reactions above, the oxygen reacts with the carbon atoms to carbon monoxide, which is a volatile gas. Secondly, the oxygen reacts with the plasma to convert unsaturated fluoride connections to reactive F atoms. Regarding continuous etching of 4H substrates with RIE, it can be summarized from [8], that SF_6 with O_2 are needed as etch gasses, where the O_2 fraction ranges from 10 to 40%. The RF bias power ranging from 25 W to 100 W and the pressure ranging from 5 mTorr to 15 mTorr. The obtained etch rates within this work equal 0.27 µm min^{-1} to 0.75 µm min^{-1}.

The hard masks used were electroplated gold and nickel. The state of the art regarding anisotropic etching of SiC is provided by internal communications of the cleanroom equipment supplier SPTS. The Synopsis tool offered by this cleanroom equipment vendor uses SF_6 based chemistry and an etch rate of around 1.2 µm is obtained, with an uniformity of ± 3%. The selectivity to Ni is approximately 1/30, and the profile angle equals 89.5°, wafer temperature during etching equals 110 °C [9].

It can be concluded that SF_6 mixed with O_2 gives in general the highest etch rates. In order to yield the best selectivity values, it is generally described by literature that metal masking layers are to be used. A significantly lower etch rate is obtained by using chlorine and bromine based chemistries, which are on the other hand compatible with the CMOS compatible dielectrics SiO_2 and Si_3N_4 to be used as hard mask. Summarizing, it can be said that the following gasses are used for RIE etching of SiC: CHF_3, $CBrF_4$, CF_4, SF_6, NF_3, HBr. From these gasses, only the latter one uses a chlorine chemistry, while the others are fluorine based.

4.3.3. MASKING LAYERS

Since α-SiC is a very inert material, resulting in relatively low etch rates, the selection of the mask material is of utmost importance in order to yield selectivity values which enable fabrication of micro structures. The masking layer needs to be relatively inert for the chemical reaction with the gas, and thus only be influenced by the physical bombardment. When choosing a masking layer, there will be a trade-off between the selectivity and what is allowed in the available equipment. It is for example known that metal masking layers such as aluminum, copper and nickel have superior selectivity compared to silicon oxide. The disadvantage of most of these metals is, is that they are highly contaminating. Except for aluminum, copper and nickel are not allowed in the dry-etching equipment at EKL. Copper should be seen as last resort, because of the high degree of contamination. When copper is going to be investigated as hard mask, its diffusion constant into crystalline SiC and cleaning after etching should be investigated. Another disadvantage of using metal as masking layer is that the metal can sputter back, which results in an effect called micromasking. When the etching continues, a grass-like structure can be the results, caused by small metal flakes which locally function as micro mask against the plasma. At last, has the usage of metals as masking layer the disadvantage that a tool is used which is allowed to get contaminated. Furthermore, extensive cleaning steps are needed to prevent cross-contamination.

Table 4.1 summarizes the knowledge on masking layers for etching crystalline SiC. Since it is now known that for etching of c-SiC the gasses typically used are SF_6, possibly mixed

Table 4.1: Masking layers and selectivities if known.

Material	Feasibility [+;-;0]	Selectivity (if known)	Remark	Ref
Ti	-		Ethed by Cl and F chemistry	[10]
Pt	0		Etched by Cl and F chem., low ER	[11]
Ta	-		Etched by F chemistry	[12]
Co	-		Etched by F chemistry	
Al	+	4 [13]; 5-30 [3]	Etched by Cl chemistry	[3]
Mo	-		Etched by F chemistry	[12]
Pa	-		Etched by F chemistry	[14]
Ni	+	90 [13]; 50 [3]; 20-90 [8]; 30 [9]	Feasible by literature	[3]
Cr	+	25-35	Feasible by literature	[13]
AlN	+	16	Feasible by literature	[15]
TiO	-		Etched by F chemistry	[16]
TiN	-		Etched by F chemistry	[14]
Al_2O_3	0		Feasible in F chemistry	[17]
Zr	+		Mainly Cl chemistry etched	
Ge	-		Etched by F chemistry	[18]
Nb	-		Etched by F chemistry	[19]
Cu	0		Etched by Cl chemistry	[12]
SiO_2	+	0.8-3	Feasible by literature	[3]
SnO_2	+	6		[13]
ITO	+	22 [13] 10-20 [3]		[3]
GaN	+	50	Used by SPTS	[9]
PR	-	0.5	Etched by oxygen plasma	[3]

with O_2. This means that the masking layer should be as inert as possible to the fluorine based etch chemistries. By looking at the etch chemistries per available metal at EKL, one can already give a no-go to the masking layers which are etched in an fluorine based chemistry, namely Titanium, Tantalum, Molybdenum [12]. Platinum is etched by SF_6 based gas mixtures, thus also not sufficient as masking layer [11]. Silicon dioxide can be used as masking layer, although at poor selectivity of maximally 3. Within EKL there is experience with this materials as masking layer, even up to a thickness of 30 µm. The disadvantage is that by depositing PECVD SiO_2 stress is induced on the wafer. Deposition of 30 µm at once would result in to big stress levels. To circumvent this problem, phased deposition of PECVD SiO_2 could be performed, for example in steps of 5 µm. Additionally, it is important to mention that the selectivity figure is, in general, also dependent on the desired etch rate, which is in turn determined by the process parameters such as platen or bias power, in the case of ICP etching [13].

It can be concluded that the standard dielectrics such as SiO_2 can be used but give inferior selectivities compared to a metal masking layer. When a thick layer of such a dielectric is deposited, the stress and bow of the wafer should be taken into account. Metal masking layers show significantly better selectivity figures, where nickel is reported the

most selective option, which can furthermore be used in a fluorine based chemistry. Depending on the the used chemistry, contamination, available metals and other process parameter (such as stress considerations, aimed etched depth and hard mask thickness) a different metal hardmask might come out best. For all metal hardmask, micro masking is an issue which should be taken into account.

4.3.4. REACTIVE ION ETCHERS

In this section an inventory is made about the available RIE etchers which can be used for the SiC etching investigation. Among the possibilities is an Alcatel GIR300 etcher which can etch only 1 wafer at a time. Disadvantages are that there is no cooling of the wafer or chuck available. The Trikon Omega etcher is typically used to etch metals and polymers and has temperature control on the chuck. The SPTS Rapier is mainly used as Deep Reactive Ion Etcher (DRIE) but can also be used as continuous inductively coupled plasma (ICP) etcher. Two Alcatel Adixen AMS100 DRIE etchers are available that can etch cyclic (DRIE) and continuous. One is situated in Kavli Nanolab, in which metal masking layers are allowed.

Table 4.2: Available RIE etchers.

Equipment	Chemistry	Remark
Alcatel GIR300	F	Single wafer processing
Trikon Omega	Cl & F	Experience with PECVD SiC
SPTS Rapier i2L	F	Not suitable for mono-c-SiC
Adixen AMS100	F	Former DRIE tool EKL
Adixen AMS100 (Kavli)	F	Tests in this section

SPTS RAPIER I2L

The SPTS Rapier i2L is a dry-etcher which can work in four modes, as RIE, ICP RIE (additional coils are used), as classic Bosch process and as improved Bosch process. Key element for this machine is that certain conditions for anisotropic etching should be kept well at all times. From literature [13] it is known that for the etching of mono-SiC a gas mixture of SF_6 combined with O_2 works well. However, if O_2 is added to the etching process, silicon dioxide will be formed and will deposit on the walls of the reactor (resulting in a so-called 'dirty' process). For reason, mixing SF_6 with O_2 is not allowed in the Rapier i2L. When solely SF_6 is used on the Rapier, the etch rate will be mainly determined by the bias power (bombardment). The SF_6 will attack the silicon of the compound semiconductor. Moreover are metal hardmasks not allowed in the Rapier. In addition to these complications, it was found that the wafer handler of the tool did not

Table 4.3: Process conditions for the poly-Si/silicon nitride recipe for the Alcatel GIR300 etcher.

Figure	Value
CF_4	70 sccm
SF_6	10 sccm
O_2	10 sccm
Power	60 W
Pressure	0.05 mbar

Table 4.4: Etch rates for Alcatel GIR300, poly-Si/silicon nitride recipe.

Material	ER [nm min^{-1}]
Poly-SiC	69.9
SiN (Novellus)	120
SiN (LPCVD)	77.5
Poly-Si (LPCVD)	120
Photoresist	≈ 150
4H-SiC (C face up)	**17.3**

recognize the 4H-SiC wafers. Based on the impossibility to etch with O_2 and SF_6 mixtures it was decided that this tool is not further investigated regarding crystalline SiC etching.

4

ALCATEL GIR300

Etch experiments in crystalline SiC were carried out while etching the alignment marker in a 4H-SiC wafer. No wafer handling issues would occur with this etcher, because the wafer is loaded manually in the quartz holder. In contrast, the Trikon Omega has optical sensors for wafer handling which can not be switched off. A resulting lower etch rate and less optimal cooling are not considered as an issue here, since the alignment markers only need to be etched typically around 120 nm. The etching recipe which was used, was equal to the poly-Si/nitride recipe, of which the details are included in Table 4.3. Because initially no etch rate were known at all for the etching of 4H-SiC, the etch time needed to be estimated based on the known etch rates for other layers, mainly based on poly-3C-SiC, having an etch rate of 69.9 nm min^{-1}. It can be found in literature [20] that the etch rates for mono-crystalline β-SiC is around half of the etch rate of polycrystalline β-SiC. Since in this case 4H-SiC (α) is considered in its mono-crystalline form, we can at least divide the known etch rate for poly-3C-SiC by two. The chosen etch time was therefore equal to 3 min. In order to determine the etch depth, the etched alignment markers were inspected with the Keyence laser profiler VK-X250. Because the PR is also etched significantly in the Alcatel plasma etcher, the wafer was stripped by using a 40 °C acetone bath, after which a cleaning step took place. From the images of the optical microscope is was soon clear that the removal of the photoresist decreased the contract of the marker dramatically, although it was still visible. Looking into the surface profile of the etched markers, the etch depth was measured to be 51 nm to 55 nm. Averaging multiple measurements gives a value of 52 nm. The resulting etch rate is therefore 17.3 nm min^{-1}, which is one fourth of the etch rate for poly-3C-SiC.

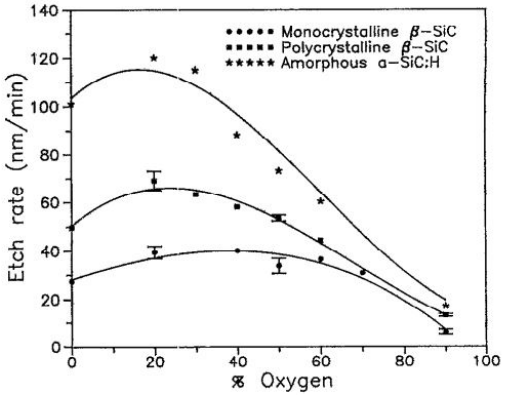
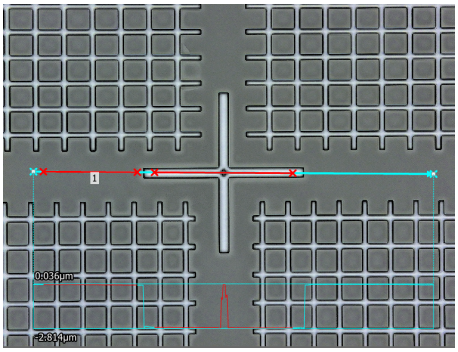


Figure 4.2: Comparison of different etch rates using a CF_4 + O_2 recipe. Source: [20].

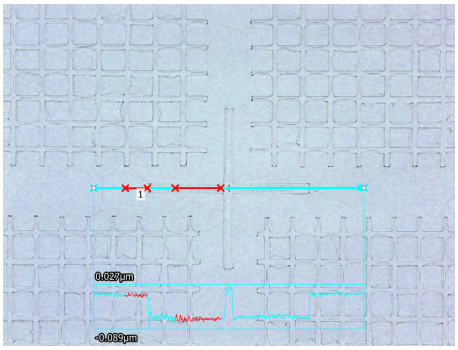
TRIKON OMEGA

Aluminum BS layer for wafer handling Because it was concluded from manual wafer handling tests on the Trikon Omega ICP etcher and the SPTS Rapier i2L that the SiC wafers are transparent for the wavelength used by these tools to detect the presence of the wafer, a thin layer of aluminum on the BS of the wafer was deposited to circumvent this problem. The reasons that aluminum is chosen above a different layer which is also in-transparent, for example PECVD deposited poly silicon, is that aluminum is already in-transparent in very thin layers (i.e. 50 nm), whereas poly silicon would need several micrometers before the light will not travel through. After the etching process the aluminum can be best removed by wet-chemical etching, because this type of etching is not damaging the crystal lattice on the surface of the wafer, in contrast to dry (plasma) etching which is more likely to do damage to the crystal on the wafer surface. Because during the process of deposition and etching of the AlSi(1%) layer, a small amount of poly silicon is formed, it is preferred to use a AlSi(1%) layer which is as thin as possible. A layer of only 50 nm thick is already dense enough to make the wafer in-transparent. Another concern could be the diffusion of aluminum into mono-SiC, even although the diffusion coefficient of aluminum is extremely low. Aluminum is known dopant for forming P-type SiC [3]. To mitigate any possible diffusion issues of the aluminum BS layer, deposition is preferably carried out at 50 °C. To be able to still use the BS alignment through the wafer, small squares of around 2x 2 mm can be etched in the aluminum layer on the location of the FS etched alignment markers. Because the wafer is considered as metal wafer, it has implications for which machines can still be used later in the process. One way to circumvent this problem is to first deposit a layer of around 2 µm of silicon oxide by PECVD. This should be done both on the FS as on the BS of the wafer,

because sputtering of AlSi(1%) results in a ring of around 5 mm of aluminum also on the FS of the wafer. This oxide will also passivate the mono-SiC in order to prevent damage to the crystal lattice.After the deposition of oxide and the sputtering process, the 5 mm wide ring on the edge of the FS of the wafer need to be etched away again, by using the Omega. If the aluminum has been etched away on the FS, the FS can be coated with 3.1 µm resist, after which exposure of the alignment markers can be carried out. Since aluminum is present now on the BS of the wafer, the Omega can be used to etch the alignment markers this time.



(a) Surface profile of the etched marker before PR removal. The measured depth equals 2698 nm.



(b) Surface profile of the etched marker after PR removal and cleaning the wafer. The measured depth equals 64 nm.

Figure 4.3: Alignment marker inspection before and after removal of the photoresist layer using the Keyence laser profiler.

Etching Etching recipes for the Trikon Omega already exist, although they are mainly intended for the etching of poly- and amorphous SiC. Etch rates of around 400 nm min^{-1} have been achieved in the past. In contrast to the SPTS Rapier, in the Trikon Omega O_2 can be mixed with SF_6 when etching crystalline SiC. In order to investigate the etching performance of the Trikon Omega, the alignment markers were etched in a 4H-SiC wafer. First, the SiC wafer is coated using standard positive PR with a thickness of 3.1 µm. After exposure and development the wafer is put in the Trikon Omega ICP etcher using recipe *SiCcdb*. As can also be seen in Table 4.5 the recipe used makes use of a combination of SF_6 with O_2 as reactive gasses in a ration of 1:1 with an acceleration power of 50 W. Experience from the past for this recipe yielded etch rates of 654 nm min^{-1} in the case of PECVD amorphous SiC. Based on literature the etch rate of mono-SiC is around three times as small as for amorphous SiC [20]. This would indicate an etch rate of approximately 200 nm min^{-1}. Based on this starting point, the expected time needed to

Table 4.5: Process conditions for the SiC etch recipe on the Trikon Omega.

Figure	Unit
SF_6	20 sccm
O_2	20 sccm
Acceleration power	50 W
Plasma bias power	500 W
Process pressure	50 mTorr
Platen temperature	10 °C

etch the alignment markers to a depth of 120 nm was estimated to be:

$$\frac{120\,\text{nm}}{200\,\text{nm}\,\text{min}^{-1}} \cdot 60\,\text{s}\,\text{min}^{-1} = 36\,\text{s} \tag{4.4}$$

To be sure to etch deep enough this time, the etch time was increased to 90 s, while keeping other parameters of the recipe constant. After etching, the wafer was inspected using the Keyence laser profiler, already before stripping the resulting PR. By inspecting the markers before and after the resist has been stripped, also the etch rate of the PR can be deducted. The measurement result of the alignment marker before stripping the resist is included in Figure 4.3a. Note that in this measurement result the partly etched PR is still on the wafer. As can already be concluded from the profile depth of 2698 nm, which is smaller than the 3.1 µm initial thickness of the applied PR, is that the selectivity to SiC with respect to PR is smaller than 1, which can be expected from literature. Two optical images of the alignment marker before and after stripping the PR and subsequently cleaning the wafer are included in Figure 4.3. It can clearly be noticed that the contrast is decreased dramatically after removal of the PR. To determine both the etch rate of mono-SiC and PR, the results are as follows:

$$ER_{PR} = \frac{th_{PRbefore} - (th_{PR+SiC} - th_{SiC})}{t} = \frac{3100 - (2698 - 64)}{1.5\,\text{min}} = 310\,\text{nm}\,\text{min}^{-1} \tag{4.5}$$

$$ER_{SiC} = \frac{th_{SiC}}{t} = \frac{64}{1.5\,\text{min}} = 42.67\,\text{nm}\,\text{min}^{-1} \tag{4.6}$$

4.3.5. ADIXEN AMS100 KAVLI

In Kavli Nanolab, located at the faculty of applied science, an Alcatel Adixen DRIE etcher is available. In this machine, metal masking layers such as chromium and nickel are allowed. The advantage of these metal masking layers is the high selectivity. Another advantage of this machine is the available build-in laser based endpoint detection. This

end point detection is based on the reflection of the bottom surface of the wafer. The laser beam must therefore be located in an etched structure, such as a square membrane. The laser spot has a diameter of around 5 mm in the center of the wafer. The lithography part needs to be defined in such a way that a to be etched structure falls within this spot. This tool will be used for the deep RIE experiments on 4H-SiC, which will be described in the next section 4.3.6.

4.3.6. DEEP RIE 4H-SIC

Before the wafers can be used in the EKL cleanroom, first additional cleaning steps need to be performed because these wafers come from 'outside'. The policy requires a cleaning+ method, which means effectively that 2x the 100% HNO_3 is used, afterwards the 65% HNO_3 at 110 °C and standard rinsing steps in between. Also for this process, an aluminum layer of 50 nm is sputtered on the BS of the wafer to to make it recognizable by various wafer handlers. A nickel hardmask will be deposited on the FS of the wafer and afterward be patterned with a etch test structure. Exposure should be carried per quadrant to use the rather expensive SiC carefully. The nickel hardmask is opened in a wet-chemical way and reactive ion etching can be performed on the crystalline 4H-SiC in Kavli.

Test structures For this test module different test structures are used, using the existing mask DRIE test. On this multi-image mask, multiple test structures are available, ranging from gratings, lines with varying widths, release test structures, round pillars, round vias, and release and cleave structures. Furthermore square membranes of 750 µm designed earlier will be tested. By using the test structures, the aspect ratio and the etch rate can be checked. Cells will be formed with the dimensions of 2x2 mm. In a square containing 9 2x2 mm, in the center one, one DRIE TEST image can be exposed. During the stepper job, this image occupies automatically the entire 6 x 6 mm space. In the three cells adjacent to the nine 2 x 2 mm cells, the test membrane and the contact openings can be exposed. The first test wafers will patterned with the first image of the DRIE TEST, consisting of gratings, lines and spaces. Since this entire image equals 6 x 6 mm, the membrane image will be placed in the middle of the three adjacent cells. To save costly mono-SiC, it was decided earlier to process by quadrant over the wafer. There have been made four jobs in which every time one quadrant is filled with test structures. The sizes of the gratings, lines and spaces image ranges from 2 µm up to 200 µm. The largest via diameter in image 9 is 100 µm.

Nickel Hardmask Evaporation Now the procedure for lithography and etching of the alignment markers is known, there can be focused on the type of hard mask for deep anisotropic etching of the mono-SiC wafers, for the final purpose to investigate to which extend bulk micro machining from mono-SiC is feasible. To achieve this, from literature it is widely known that the selectivity is an issue when choosing conventional masking layers. Masking layers providing workable masking materials are for example nickel or chromium. More details about the choice for masking layers can be found in section 4.3.3. Because nickel has the highest known selectivity compared to other masking layers, this metal was chosen for this experiment. Because the nickel sputter target is only available in the so called free slots, it was chosen to use the CHA evaporator for evaporation of the Ni layer on the mono-SiC substrate. The disadvantage of using the CHA evaporator compared to physical vapor deposition (PVD) using the Sigma sputter coater is that the thickness of deposited layers is significantly lower. The maximum feasible layer thickness for the CHA is around 300 nm per evaporation. To still yield a sufficiently thick masking layer, three deposition steps were performed. In this way the total layer thickness is around 900 nm. The deposition rate used was 3 nm min^{-1} and the purity of the Ni pocket equals 99.98%. With an etch selectivity of around 50, the etch depth which could be obtained by DRIE equals around 50 times 900 nm, 45 µm. Later thicker layers can be used when the nickel sputter target is available during the free slots.

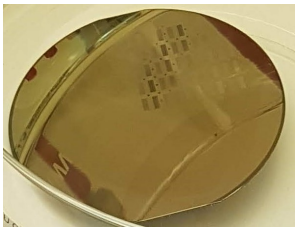
Patterning the Nickel Hardmask Layer In order to be able to pattern the nickel hardmask layer, the manual coating and developing need to be applied. The reason for this is that nickel is a so called red metal. Its diffusivity is high and the risk for contamination in active device processes is large. Because the CHA evaporator also contaminates the backside of the wafer, the EVG120 can not be used for coating and developing. Instead manual coating, developing and baking steps need to be performed. The two silicon test wafers with LPCVD TEOS and evaporated nickel are coating using the Brewer Science spinner with SPR3012 positive PR. The using recipe resulted in a layer thickness of 1.4 µm. Soft baking has been performed for 1 min at 95 °C and exposure using the ASML PAS5500 with 120 mJ. Subsequently, post-exposure bake has been performed for one minute at 115 °C and development with MF322 developer. A hard bake step has been performed for one minute at 115 °C.

Wet Etching Nickel Hardmask After evaporation, the nickel hardmask was coated and the described test images are exposed after which the wafer was developed. Wet etching of nickel can be done with numerous etchants. However, not all of them are suitable. Some etchants described by literature [21] do use a mixture of acetone and HNO_3,

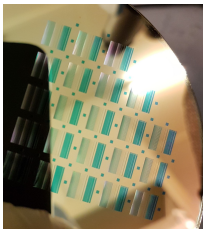
which is basically and oxidizer mixed with an organic compound, with risk for severe reactions. Other etchants described are for example $FeCl_3$, which is not preferred because it is a highly contaminating solution caused by the Fe content. Mixture with high HNO_3 concentrations are not preferred because they will attack the PR layer in a too large extend, and etching with just HF is a slow etchant. The mixture which is known to be a good candidate for nickel etching consists of phosphoric acid, nitric acid and ascetic acid diluted with water: $H_3PO_4 : HNO_3 : CH_3COOH : H_2O$ in the ratio 3 : 3 : 1: 1. Another good etchant known consists of nitric acid, ascetic acid, sulfuric acid and water: $HNO_3 : CH_3COOH : H_2SO_2 : H_2O$ in the ratio 5 : 5 : 2 : 28. In this case the water content can be varied to tune the etch rate. The expected etch rate for a solution which is around 2.4 times as strong, containing 10 parts of water, is equal to 10 µm min^{-1} at an temperature of 85 °C.

The etchant based on ascetic acid, nitric acid and sulfuric acid was manually mixed in the SAL lab. Based on previous experience, a low etch rate was expected. In order to increase the etch rate, 20 parts of DI water were used instead of 28 parts. After only 1 minute, the nickel color started to fade away, an a few seconds later the etch openings were 'landed' on the TEOS layer below. In Figure 4.4a the gradient between the etched nickel and the landed openings on the TEOS layer can be clearly noticed, thanks to the high contrast between both layers. In the case of the Si test wafer, the color of the TEOS layer appeared between green and pink. Since the first etch time was much shorter than expected, the prescribed dilution ratio with DI water was used. Instead of 20 parts of water, 28 parts were used. This was done by adding water to the (acid) etching solution. A procedure which is certainly not preferred because it is common practice to add the acid to the water, because of the exothermic nature of diluting acids. The second test wafer was etched using this diluted version of the first etching solution. This time the etch time was determined to be 7 minutes and 30 seconds. The center of the wafer changes color as first, which implies that the nickel layer is thicker on the edges. An important advantage of the diluted etch solution is that there is more control in the etched layer. The timing is less critical, which is even more advantageous in the case of manual etching, handing and rinsing in the SAL lab. Furthermore is it expected that the amount of under etch is less severe in the case of the slower etchant.

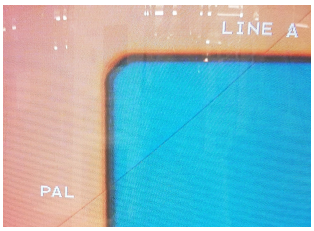
Sputtering a Ni Hardmask Layer In the Kavli infrastructure basically all equipment is seen as contaminated, whereas in EKL all equipment is seen as clean. To circumvent this discrepancy, on the BS of the SiC wafer a layer of 500 nm of silicon oxide is deposited using PECVD at 400 °C. The Trikon Sigma PVD Sputter tool was used to perform exper-



(a) The patterned nickel during wet chemical etching of the hardmask. Note that only the first quadrant has been exposed.



(b) Waferview of the etch openings, the color of the TEOS layer can be clearly seen.



(c) The underetch of after etching the Ni hardmask.

Figure 4.4: Etching the Ni hardmask layer.

iments with sputtering of a nickel hard mask layer. The main advantages of sputtering is that the layer can be deposited much faster compared to evaporation with the CHA. The sputtering of several µm requires only approximately 30 minutes including a target clean, whereas the maximum thickness of a nickel hardmask layer by evaporation is around 300 nm. The time needed for evaporation of 900 nm was at least 6 hours. Apart from the time, another advantage is that the side and the backside of the wafer stays clean, because shutters are used during deposition. Because of this, the EVG120 can be used for the coating and developing and no manual coating and developing is needed, enhancing processing convenience and control. Because there is still nickel on the front side of the wafer, red carriers need to be used.

Before the SiC wafer intended for etch experiments was coated with nickel, first the PVD recipe for nickel deposition was tested on silicon test wafers. When depositing layers with significant thickness, a stress in induced in the wafer. This stress originated from CTE mismatch and cohesion forces between different metal atoms. As a trial, two silicon test wafers were used to deposit nickel on and single side polished wafers of 525 µm um were used. The intended layer thickness is 5 µm, whereas the deposition temperature was set to 50 °C. At lower temperatures, the contribution of the CTE mismatch is contributing less to the induced stress and as a result a lower stress is expected. In order to analyze the stress in the wafer, a pre-measurement and a post measurement is carried out by the Flexus Stress measurement tool. This tool measures the bow of the wafer by using lasers. The bow is used as input to determine the stress, based on the thickness of the wafer, the thickness of the deposited layer and the Young's modulus of the substrate.

The measured bow and stress values of the first deposition test are included in Table 4.6. As is known from the lithography is that the maximum allowable bow for wafers in order to go without problem through the stepper is 200 µm. This experiments on the 525 µm

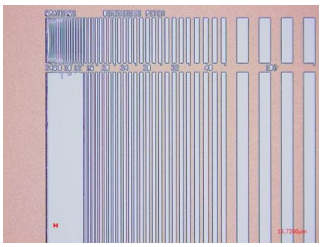
Table 4.6: Measured stress and bow values after nickel sputtering.

Wafer ID	Ni Th. [µm]	Stress [MPa]	Bow [µm]
5161	5	462	-223.41
5028	5	625	-301.52
5252	2	608	-119.62
5166	2	699	-138.19
2911 (SiC)	2	640	-136.37

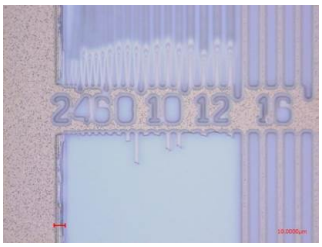
Table 4.7: Process conditions during nickel sputtering using the Trikon Σ.

Figure	Unit
Target power	5 kW
Film thickness	2000 nm
Gas flow 1 (Argon)	300 sccm
Base pressure	1×10^{-7} Torr
Temperature	50 °C

thick silicon wafers showed values for the bow of −232 µm and −301 µm, which is too large to be handled by the wafer stepper. Knowing that the SiC wafer has a thickness of 360 µm, it can be concluded that the effect of the deposited layer on the bow will also be larger, which might be compensated by a significantly larger value for the Young's modulus of SiC. For these reasons it was decided to deposit 2000 nm of nickel instead of 5000 nm. This reduction in hard mask thickness will of course subsequently influence the maximum etch depth of the SiC. The measured values for the bow are again included in Table 4.6 and are in the case of 2000 nm equal to −119 µm and −138 µm which is far below 200 µm. No issues which the wafer stepper are expected based on these values. A complete overview of the process conditions is included in Table 4.7. After initial tests on the silicon test wafers, the SiC wafer is coated with sputtered nickel of 2000 nm using the same recipe and process conditions as used for the silicon test wafers. The values for stress and bow after deposition were tested to be 640 MPa and −136.37 µm respectively, as also included in Table 4.6.



(a) The etched open lines.



(b) Zoon-in. Note that the smaller structures have been removed due to under etching.

Figure 4.5: Under etch after wet etching the nickel hard mask.

Patterning of Sputtered Ni-layer The exposure was done using the ASML PAS5500 wafer stepper, using a multi-image, multi-mask job. In the center of the wafer a square of 1x1 mm was exposed, which could be used for the end-point detection during the DRIE etch later in the process. The 1 x 1 mm square was exposed with 100 µm separa-

tion in the first quadrant from the origin of the wafer. Images 1 and 9 of the DRIE TEST masker were used, which include lines, spacing and grating, and vias with different dimensions in a darkfield exposure. After developing, the wafers were additionally hard baked at 120 °C for 15 minutes to increase adhesion of the PR layer. After the lithography step, the Ni hard mask was opened by using the same Ni etchant as before. Based on prior etch times, and knowing that this current layer thickness is around 3 times larger, the following ratio of acids and water was used: HNO_3 : CH_3COOH : H_2SO_2 : H_2O in the ratio 5 : 5 : 2 : 24. The volume was as follows for the same order: 166 mL : 166 mL : 66 mL : 800 mL, yielding a total volume of 1.2 L. The etch times for the Si test wafer was 7 min and for the SiC wafer, when using the same mixture, 11:30 [min:s]. An intermediate inspection has been done in between for the SiC wafer. However, Ni flakes were still visible and an additional 2:30 [min:s] of wet chemical etching was required. An explanation for the significantly longer etch time, might be that the etch rate is influenced by the wafer which was etched before in the same solution. As can be seen in Figure 4.5 the some under etch is visible. It can be concluded from this result that the smallest structures from the DRIE test mask are 16 µm which will survive the isotropic etching. This is because the separation between the two windows is smaller than two times the layer thickness. After the opening of the hard mask, the surface profile was measured using the Keyence lase profiler, including the still present PR layer. As a result a step of 3.05 µm was measured. Knowing that the Ni layer thickness equals 2176 nm, the resulting PR layer thickness equals 874 nm, which implies that approximately 500 nm of PR was etched by the Ni etch solution. This can be expected, since HNO_3 is present in this etch solution.

DRIE etching at Kavli Nanolab - I Based on recent literature from Lunet et al. [22] a recipe for the Alcatel Adixen AMS100 Bosch/DRIE etcher was formed. It is known, as also described earlier, that a combination of SF_6 and O_2 is to be used as reactive etch gasses. In the work described by Lunet et al. is was stated that a cyclic etch recipe would result in more vertical side walls. A low oxygen etch cycle was followed by a high oxygen content etch cycle. To start with the low oxygen content etch recipe was used as input to form an etch recipe in the AMS100. The 1:10 ratio of O_2:SF_6 was used, together with the 1:10 ratio of the platen:ICP power. The temperature chosen was 0 °C to make the resulting PR last longer as a masking layer, on top of the Ni. Because initial low pressure (5 µbar) gave problems in igniting the plasma, the pressure was set higher to 50 µbar. The recipe is saved in the Adixen tool as 'mono_sic_etch' and the step used is 'alpha_sic'. To save the hard mask and PR layer on the 3 quadrants which were not

processed, Kapton tape was applied to these three regions.

For a first test, an etch time of 30 °C was used. When measuring the etch windows with an KLA-Tencor D-120 stylus profiler, the etch depth of the test structures range from 2160 nm up to 2424 nm, where a dependency on the aspect ratio was visible. To give value on this number, it is important to verify if the Ni hard mask was etched. To determine the etch rate by DRIE, two layers have to be considered. The first layer is the PR layer which was initially 1.4 µm but was partly etched during nickel etching. The second layer, the nickel hard mask, which is in principle not affected during opening, but can be etched during DRIE. The Kapton tape was removed an the step height from PR which was untouched by DRIE. Knowing the step height before etching, the stepheight after etching and the PR thickness, the lower and higher limit of the etch rates can be determined. The determination includes the letters i for initial meaning before DRIE, and a meaning after the DRIE etch.

$$ER_{min} = \frac{th_{PR,Ni,i} - th_{PR,a} - th_{Ni-SiC,a}}{t} = \frac{3050 - 1185 - 2160}{30\,\text{min}} = 9.83\,\text{nm}\,\text{min}^{-1} \quad (4.7)$$

$$ER_{min} = \frac{th_{PR,Ni,i} - th_{PR,a} - th_{Ni-SiC,a}}{t} = \frac{3050 - 1185 - 2424}{30\,\text{min}} = 18.5\,\text{nm}\,\text{min}^{-1} \quad (4.8)$$

Optical inspection and images have been performed after the first DRIE etch tests, with the aid of a Keyence laser profiler. The pictures are included in Figures 4.8 and 4.9. The nickel hardmask seems to be sputtered back into the etch openings during the performed DRIE test. This effect is known as micromasking and highly undesired, because it can result in grass-like structures. Furthermore, in some of the etch openings, a thin layer of non-volatile reaction product still seems to be present. A reason for this could be that the substrate temperature, which was set to 0 °C, was actually too low for the reaction products to stay volatile.

DRIE etching at Kavli Nanolab - II After the first etch test with the DRIE etcher at Kavli, it can be concluded that the measured etch rate, around 10 nm min^{-1}, is not a feasible etch rate as starting point for the design of microsystems and mechanical sensors. Based on the process conditions of the initial designed recipe, some parameters were changed to improve the etch rate. The ICP power was increased from 850 W to 2000 W and the platen power was enlarged from 85 W to 850 W (1 to 10 ratio). The pressure was brought down to 14 µbar instead of 52 µbar, because it is expected that a lower pressure

Table 4.8: Process conditions for the first SiC etching in the Adixen AMS100 (Kavli).

Figure	Setpoint	Measured
Temperature	0 °C	n.a.
Valve position	14.9 %	n.a.
Pressure	n.a.	52 µbar
ICP power	850 W	849 W
Platen power	85 W	86 W (4 W reflected)
O_2 flow	20 sccm	20.2 sccm
SF_6 flow	200 sccm	201 sccm
Bias voltage	n.a.	13.8 V to 14.8 V
Inner wall temperature	200 °C	n.a.
Initial tuning value	400 W	n.a.
Initial load value	600 W	n.a.

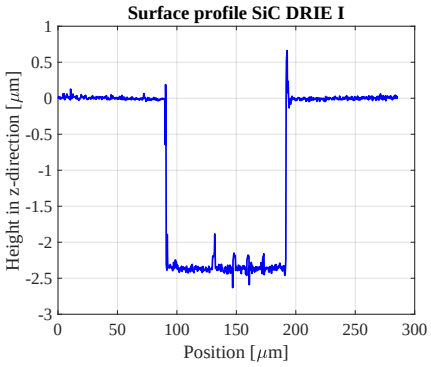


Figure 4.6: Surface profile by using the Keyence laser profiler (EKL) after the first DRIE etch test.

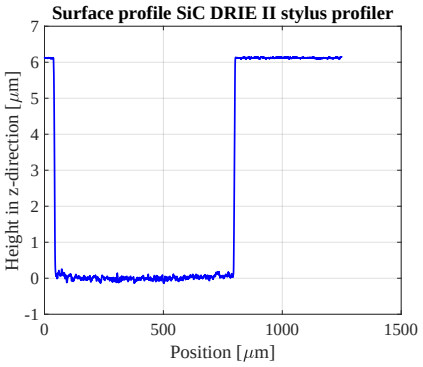
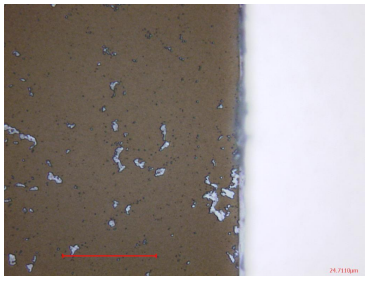
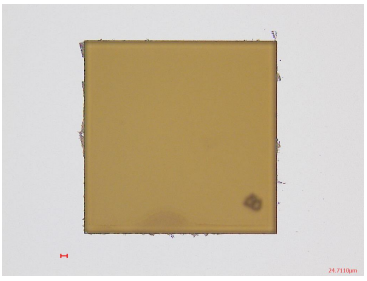


Figure 4.7: Surface profile by using the KLA Tencor profiler (Kavli) after the second DRIE etch test.



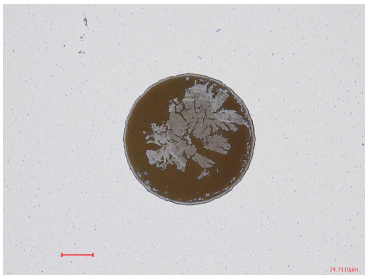
(a) Micromasking by back-sputtering of the nickel masking layer.



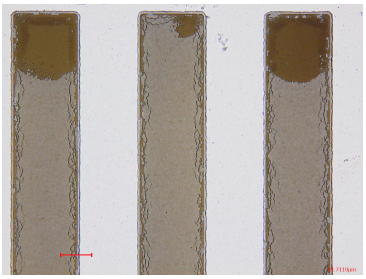
(b) A clean opened etch window, the color of the SiC substrate is clearly visible.

Figure 4.8: Optical image after the first DRIE tests.

will furthermore have a positive influence in the directionality and anisotropy of the etch. As a consequence, the reactive gasses stay a shorter time in the chamber. Based on the residues seen during the inspection with the optical microscope during after the



(a) In circular openings.



(b) In open lines of the test image.

Figure 4.9: Layers of non-volatile reaction products are still on the wafer.

first DRIE test, it was thought that the substrate temperature was initially set too low with 0 °C. Based on literature, the substrate temperature was increased to 25 °C. In this DRIE tool, the pressure in determined by a valve in the tubing from the pumps to the reaction chamber. By opening a valve in this tubing more, the resistance in this tubing will decrease, and as a result the pressure will be lowered. In order to 'tune' the pressure, a mapping had to be made from valve position to pressure, from which is was concluded that a certain saturation effect in the pressure takes place with increasing valve opening. The used etch time for this experiment was again 30 min and an overview of the other process conditions is included in table 4.9.

Table 4.9: Process conditions for the second iteration of SiC etching in the Adixen AMS100 (Kavli).

Figure	Setpoint	Measured
Temperature	25 °C	24.9 °C
Valve position	55 [%]	n.a.
Pressure	n.a.	14 µbar
ICP power	2 kW	2.002 kW
Platen power	200 W	205 W (5 W reflected)
O_2 flow	20 [sccm]	20.2 [sccm]
SF_6 flow	200 [sccm]	201.0 [sccm]
Bias voltage	n.a.	31.8 V
Inner wall temperature	200 °C	n.a.
Initial tuning value	400 W	n.a.
Initial load value	600 W	n.a.

To determine the etch rate again a surface profile has been made using the KLA Tencor D-120 stylus profiler. Because after inspection with the Keyence laser profiler, it turned out that the structures toward the outside of the wafer were more clean of residues and micro masking, as was described earlier, these structures were used for the profile measurements. The result of the surface profile measurements is an average depth of 6.1 µm. Again the Kapton tape was used during this etching cycle, enabling determination of

the Ni hardmask etch rate. The step height was again measured from the protected PR layer to the exposed nickel layer, as was also done in the first etch test. The PR layer is untouched during DRIE etch thanks to the Kapton tape, but was etched during the wet chemical etching during the opening of the nickel hardmask. The step height after the first etch test was equal to 1185 nm. The step height measured now was equal to 1300 nm, which implies that 115 nm of nickel hardmask have been etched away during the second DRIE test. With this data, the etch rate can be determined.

$$Th_{Ni-HM-after} = Th_{Ni-HM-0} + \Delta_{PRtoNI,1} - \Delta_{PRtoNI,2} = 2045\,\text{nm} \tag{4.9}$$

$$ER_{drietest,2} = \frac{depth_{cavity} - Th_{Ni-HM-after}}{t} = \frac{6100-2045}{30\,\text{min}} = 135.17\,\text{nm}\,\text{min}^{-1} \tag{4.10}$$

The selectivity (denoted by S) can be determined based on this data.

$$S = \frac{SiC_{etched}}{Ni_{etched}} = \frac{4055\,\text{nm}}{115\,\text{nm}} = 35 \tag{4.11}$$

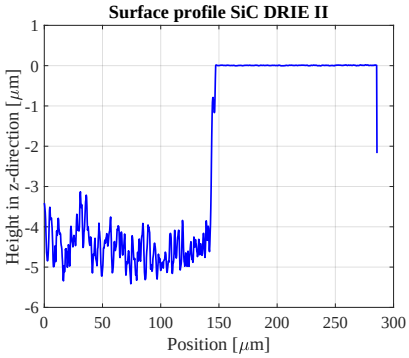
The calculated sensitivity is in line with the expectations based on literature. This means that with a nickel layer of 2 µm, an etch depth of 70 µm could be obtained.

After etching the Kapton tape was partly etched and difficult to remove. In order to clean the wafer thoroughly, the wafer was put in a oxygen plasma in the MEMS lab at EKL. 15 min of oxygen plasma was used at 500 W, but this appeared to be not sufficient. To better remove the remaining tape and its glue residues, an NMP solution was used in pure form. The wafer was immersed in the solution for 15 min, and the tape was removed with manual mechanical scraping. After the solution, still some glue and PR residues were present, which were removed by again a oxygen plasma for 15 min at 500 W.

Keyence inspection After the second etching test, the SiC wafer with the test structures was inspected using the Keyence laser profiler. Optical images were made, and the surface profile was measured. An optical picture showing the nickel hardmask, the openings of the etched test structures is included in Figure 4.10a. It can be seen that there is absolutely no reflection from the etch openings, which implies that the surface of the SiC is diffuse on the bottom of the etch openings. The surface profile, as is included in Figure 4.10b over one of the etch openings was determined and an stepheight of approximately 4.5 µm was determined.

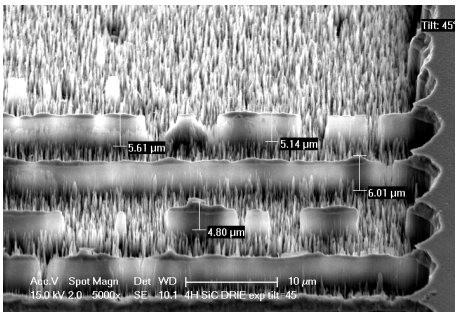


(a) Optical image after the second etch test using the Keyence laser profiler, note the high degree of contrast between the relatively shallow opening and the hardmask.

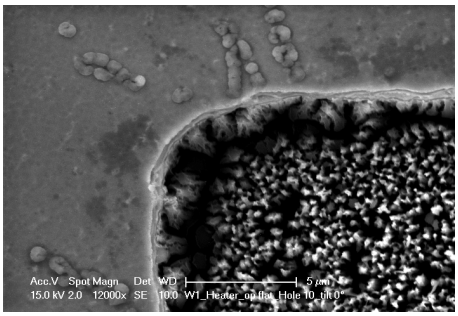


(b) The surface profile after the second etch test measured with the Keyence laser profiler.

Figure 4.10: Laser profiler measurements of the DRIE etched structures.



(a) SEM image of the grating, note the over etched Ni hard mask.

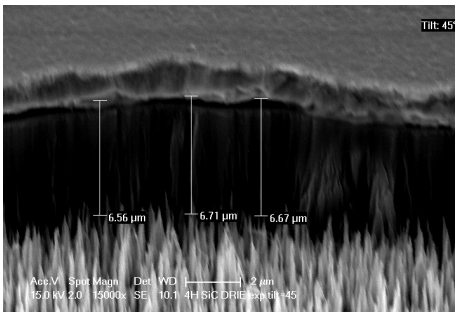


(b) SEM image without tilt, the SiC pillars are clearly visible.

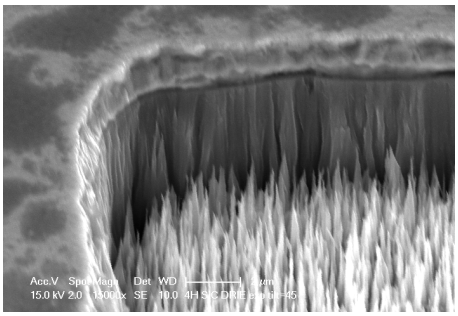
Figure 4.11: SEM images of the etched structures in the 4H-SiC wafer. Note the rough surface, most likely caused by micromasking.

SEM inspection After the second etching test at Kavli Nanolab, the inspection with the KLA stylus profiler, the required cleaning steps described above and the inspection with the Keyence laser profiler, it was decided to perform inspection with the SEM in CR100 at EKL using the Philips XL50. For more detailed inspection of the sidewalls, the hardmask, the etch depth and the surface morphology a tilt of 45° was applied to the wafer. The magnification was adapted according to the features under investigation. In Figure 4.11 two SEM images with lower magnification are included to give a better overview of the etch opening and hardmask combination. Most remarkable result is that the SiC in the etch openings has a very extreme topography. The carbide is highly spiked, and doesn't show a flat and smooth surface at all. In Figure 4.11a it can be seen

that the nickel hardmask was over etched during patterning by wet chemical etching. The narrow mask strips between the different gratings resulted in very thin free-standing carbide walls.

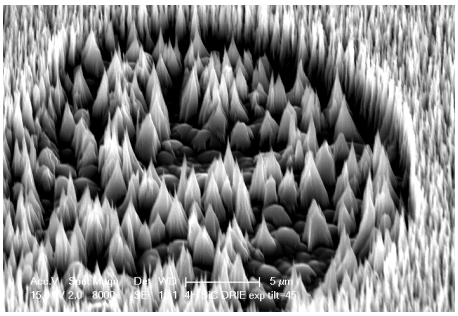


(a) SEM image of a circular etch opening, note the etch depth annotations.

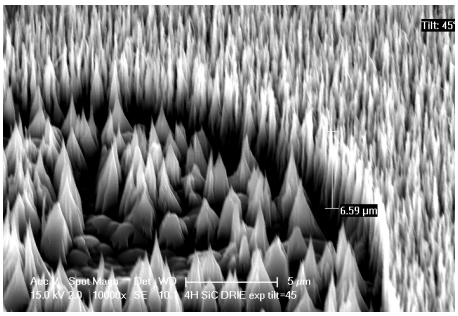


(b) An overview of the hardmask and sidewall. A high degree of orthogonality is achieved.

Figure 4.12: SEM images focusing on the hardmask and sidewall of the etch openings of the 4H-SiC wafer.



(a) A circular area inside the etch opening with different topography.



(b) An estimation of the height of the SiC 'pillar' by exploiting the deeper etched area.

Figure 4.13: SEM images of the cavity bottom in a circular etch opening of the 4H-SiC wafer.

In Figure 4.12 a more close view on the etched sidewalls is included. A high degree of orthogonality can be seen, i.e. sidewall angle being close to 90°. The measured etch depth from this image corresponds to the earlier measured profiles by the KLA stylus profiler and the Keyence laser profiler, respectively 6.1 µm and 5 µm. To measured etch depth up to the top of the spikes by the SEM equal approximate 6.7 µm. The lower measured etch depth by the Keyence can be explained by the high optical absorption and diffusivity of the surface. In one of the circular etch openings, a deeper smaller inner circle was visible, in which the free standing pillars had a different aspect ratio and height. This gave the opportunity to give an estimation for the height of the 'taller' pillars. This

measurement is included in Figure 4.12b, in which the scale bar denotes a height of approximately 6.59 µm. It can thus be concluded that the these pillars have a height with is similar to the etch depth measured during the Tencor stylus profiler. This implies that the etch depth can reach *locally* values up to 12 µm. In order to make this sure, a cross section should be made.

4.3.7. CONCLUSIONS 4H-SIC ETCHING

It can be concluded from this section that standard ICP etchers, such as the Alcatel GIR300 and Trikon Omega can be used to etch mono-crystalline 4H-SiC in a controlled and reproducible way up to etch depths of maximum several 100 nm. In this work only fluorine chemistries are used in combination with a masking layer of photoresist using these etchers on 4H-SiC. When a larger etch depth is desired, thick layers of standard dielectrics can be used, but still inferior selectivities are achieved compared to metal hardmasks. The usage of a metal hard mask is not trivial for different reasons, such as contamination, residual stress, patterning techniques and micromasking during etching. The metal selection is a function of the chemistry used during RIE. For fluorine based chemistries it was found that nickel is superior in terms of selectivity.

After the two etch experiments at Kavli Nanolab and the subsequent analysis of the result, it can be concluded that bulk etching to form smooth and homogeneous membranes from 4H-SiC by means of bulk etching in the infrastructure of TU Delft is highly challenging at this point in time. Although the etch rate is not dramatically low, namely around 130 nm min^{-1} and the selectivity with respect to the nickel hardmask according to literature, the biggest problem when performing this type of etching is the spiked surface that results after etching. It will be most likely that this effect is caused by micromasking, as a result of back-sputtering of nickel inside the etch openings. Future work would include performing Raman spectroscopy on the pillars to investigate its composition (Si versus C). The etched surface and thin free standing 3D structures might be applicable in applications where a high surface area is desired such as for gas- or chemical sensing. Further development of the metal masking layer, for example by using metal stacks, can reduce or prevent micromasking. Since the Kapton tape was etched significantly, it can be concluded that the organic material is etched by the plasma present. The loading effect, on mainly the oxygen content of the etching conditions, of the Kapton tape on the plasma during the RIE experiments can be investigated in future work, for example by etching without Kapton tape. A way to even further boost the etch rate might be to increase the platen power using, although this would compromise the selectivity to the nickel target.

4.4. ETCHING POLY-3C-SIC

Thanks to the polycrystalline structure and its main occurrence in thin-film form, the etching if this materials is less challenging compared to 4H-SiC in mono-crystalline form. Some time was taken to develop an plasma etch recipe on the Rapier DRIE etcher. This etcher has the advantage that the temperature can be lowered significantly, in contrast to the Omega etcher where the lowest temperature is 10 °C. This temperature is even difficult to reach caused by the slow cooling rate of the chiller attached to the chuck. Etch tests were performed with a cyclic recipe, also called a Bosch or DRIE process. These resulted in low etch rates and poor selectivity. The performance of the etch recipes was determined by patterning image 7 from the DRIE test mask in a 4 µm AZ3027 photo resist layer, 600 $mJ^2\,cm^{-1}$ and the DP-3 recipe were used subsequently for each exposure. The patterning was done on one quarter per etch test run, allowing for more efficient usage of wafers T13 and T14 with D-4-poly-SiC. To determine the etch rate of PR and poly-SiC, the stepheight was measured using the Dektak stylus profiler after the etching has been performed. Then the wafers were stripped by an oxygen plasma, and the stepheight was measured again. By doing so, the etch depth into the poly can be determined and hence the etch rate of poly. The ER of PR is yielded by correcting the stepheight after etching with the etch depth after stripping and subtracting the etch depth of the poly-SiC. The etch experience of different CR tools is summarized in table 4.10.

Table 4.10: Poly-SiC etch rates for different CR100 tools.

Tool	Recipe	Chemistry	ER_{SiC}	ER_{PR}
Omega	SiC_3MU (at 25 °C)	Cl/HBr	2.53 nm s^{-1}	5.72 nm s^{-1}
Omega	SiC_CDB (at 10 °C)	SF_6/O_2	n.a.	n.a.
Drytek	STD_SIN	Cl/HBr	2.79 nm s^{-1}	5.10 nm s^{-1}
Alcatel	SiN recipe	$CF_4/SF_6/O_2$	2.79 nm s^{-1}	n.a.
Rapier	LM recipe 0 °C	SF_6/O_2	1.21 nm s^{-1}	3.07 nm s^{-1}

Based on the SiC_cdb recipe from the Trikon Omega ICP etcher, an ICP recipe was formed on the Rapier. The same SF_6 and O_2 ratio was maintained. The etch rates of SiC were only around 1.15 nm s^{-1} and the etch rates of AZ3027 PR were 7.68 nm s^{-1} and 4.89 nm s^{-1} for a one and four minute etching time respectively. The low etch rate compared to the SiC_3MU recipe can be explained by the significantly lower temperature, namely 0 °C vs 25 °C. The lower sensitivity could be explained by the presence and possibly too large flow of oxygen. Suggestions to improve the polySiC etching performance of the Rapier as ICP etcher would be to lower the temperature even further, and decrease the oxygen concentration, while keeping the total gas flow constant. A lowering of the

platen temperature will result in a lower etch rate, but will in general favor the selectivity.

Table 4.11: Experimental poly-SiC etch recipes in the SPTS Rapier i2L in ICP mode.

	Recipe 1	**Recipe 2**	**Recipe 3**	**Recipe 4**
O_2	150 sccm	30 sccm	30 sccm	30 sccm
SF_6	150 sccm	270	270 sccm	270 sccm
Temperature	0 °C	−10 °C	0 °C	10 °C
ER poly-SiC nm s^{-1}	1.14	0.15	1.21	1.34
ER PR 3027 nm s^{-1}	4.89	0.51	3.07	3.57
Selectivity ($\frac{ER_{PR}}{ER_{SiC}}$)	4.29	3.4	2.53	2.66
ER 12XT	not used	not used	not used	4.23

Different etch recipes were investigated. The best result were obtained with 30 sccm of oxygen and 270 sccm of SF_6. Etching at −10 °C dramatically decreased the etch rate, and the selectivity was even worse compared to 0 °C. The new gas ratio was also tried at 0 °C and 10 °C, but no significant difference was measured in selectivity between both temperatures. The etch experiments on the Rapier are summarized in Table 4.11. To conclude, the most suitable recipe for etching the poly-SiC layer formed is the recipe based on a 10% oxygen concentration at 0 °C denoted by recipe 3. The selectivity is comparable with the same recipe at 10 °C but the lower temperature can in principle only favor selectivity, especially when future usage of 12XT photo resist is considered.

4.5. LASER ABLATION

Another way to micro machine 4H-SiC substrates is the usage of a so-called femtosecond light amplification by stimulated emission of radiation (LASER or laser) device. Within the precision and microsystems engineering (PME) group of the 3mE department of Delft University, such a device is available for cutting and micro machining processes on different materials, ranging from organic materials up to ceramics. The laser ablation techniques relies on a photo-chemical and photo-thermal reaction of the material to be ablated, caused by the high energy which is emitted on a small area. Examples of performing laser ablation methods for micromachining SiC, PZT and Pyrex exist in literature [23, 24]. One of the advantages is that no lithography is needed for this type of micromachining (thus omitting the need for reticle design), enabling quick and flexible prototyping. A resulting disadvantage is that, when wafer level processing is considered, processing each wafer is more time consuming compared to cleanroom processing based on etching.

To investigate what the performance would be of the laser available, an experiment was setup up, in which a square was programmed to be 'etched' of 400 µm in width. The

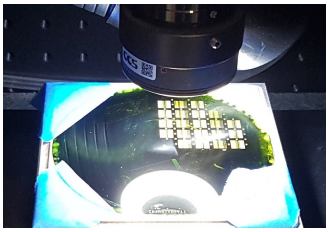


Figure 4.14: The 4H-SiC wafer on the chuck of the femtosecond laser in the PME department. Note the test structures earlier etched during 4H-SiC DRIE experiments.

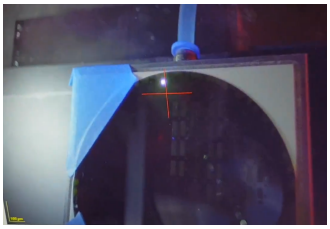
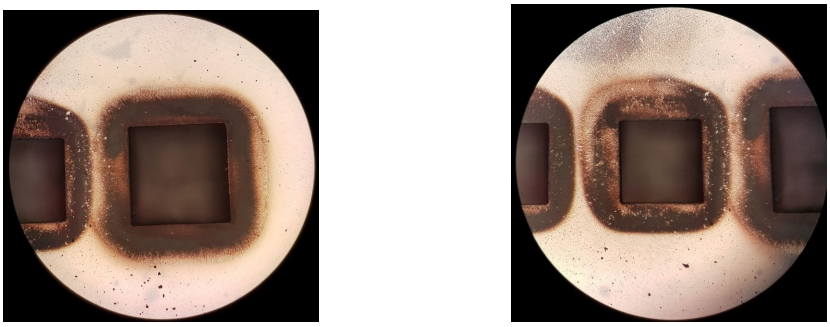


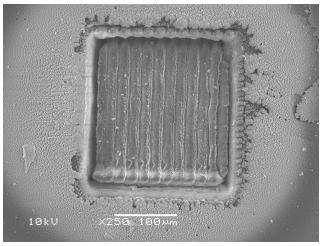
Figure 4.15: The laser ablation process through a video camera.

laser ablation is based on a 'writing' or 'scribing' action the laser which is emitting in a pulsed way. In order to control the laser ablation, different parameters must be set correctly, according to the material and desired etch depth and finishing. Important parameters which should be set are for example the line speed, the jump speed, the laser firing rate, the laser power and the burst power. Additionally, a hatch must be chosen determining the way the open etched area scribed by the laser. For this experiment, a Talon 355-15 femtosecond laser was used employing a 355 nm source while using a diagonal hatch. Images of the laser ablation process on the 4H-SiC substrate is included in Figures 4.14 and 4.15. The total time to run the programmed ablation equals 7 min. After the ablation step, it was surprising so notice that the program already resulting in complete through-etch of the wafer. Inspection was carried out using an optical microscope, of which the results are included in Figure 4.16. The thermal loading can clearly be distinguished from these images, and it furthermore obvious that there is a gradient of deposited excess material is available on the surface of the FS of the wafer.

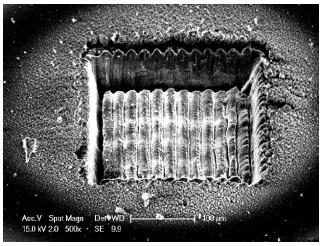


(a) **(b)**

Figure 4.16: Optical microscope inspection of the etched-through square holes though the 4H-SiC. Note the traces of the high thermal loading along the rims of the etched holes.



(a) Top view.



(b) Tilted view.

Figure 4.17: SEM images of the etched cavity featuring a resulting membrane as achieved by J. Mo. Source: [25].

After this preliminary experiment, J. Mo performed further investigation in optimization of the laser ablation program in such a way that a resulting membrane would exist, in contrast to the through etch performed earlier. The resulting cavity was inspected using SEM, see also Figure 4.17. As can also be observed from these images is the contamination of excess material and ablated particles. Note further that the bottom of the cavity shows significant topography, and that the cavity depth is much larger along the sidewalls.

4.6. METAL-SEMICONDUCTOR CONTACTS AND METALLIZATION

4.6.1. CONTACTS TO MONO-CRYSTALLINE SIC

Physics Schottky contacts are formed in such a way that a rectifying behavior is achieved. In numerous cases this is not preferred. An ohmic contact is not providing this rectifying behavior, and is within this application preferred. Generally an ohmic contact with a low contact resistivity is desired. For miniaturized devices, this implies that the contact resistivity ρ is very small, even in the order of $1 \times 10^{-6}\,\Omega\,\mathrm{cm}^{-2}$. Because no rectifying behavior is desired, the Fermi level of the metal used should lay in the case of n-type SiC on the level of the Fermi energy of the n-type doped material E_{Fn}, analog to this, for p-type SiC on the level of $\mathrm{E_{Fp}}$. See also Figure 4.18. As a result the following two statements can be made regarding the formation of ohmic contacts.

- For n-type 4H-SiC a metal is preferred with a work function lower than around 4 eV.
- For p-type 4H-SiC a metal is preferred with a work function higher than around 7 eV.

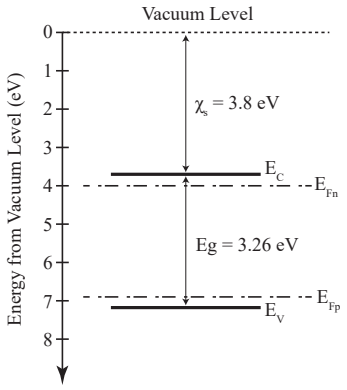


Figure 4.18: Band diagram of 4H-SiC, including the vacuum level. Reproduced from: [3].

What can be concluded from the analysis of the ohmic behavior is that it is typically caused by tunneling through the thin potential barrier. Depending on the temperature this effect is called Field Emission (FE) or Thermionic Field Emission (TFE). Furthermore, the contact resistivity reduces dramatically with increasing doping density. The best way to analyze the contact resistivity is making use of the so called linear transfer length method. When high temperature annealing is considered, it is important to keep in mind if silicides, carbides or both are formed during the process. Formation of carbides or silicides is not a warranty for ohmic contacts. As-deposited metal silicides or carbides usually results in contact showing Schottky characteristics. Annealing temperatures typically ranges from 900 °C to 1000 °C, which may result in surface roughening of the metal complicating a wire bonding process.

Ohmic contacts to n-type mono-SiC The work function ϕ of nickel is equal to 5.04 eV to 5.35 eV. If the n-type SiC is lightly doped, the Fermi level is between the center of the bandgap and the conduction band. As can also be deducted from Fig. 4.18, nickel will align with the Fermi level based on its work function. Therefore nickels forms an ohmic contact when sintering temperature is below 500 °C. On heavily doped n-type SiC nickel forms a good ohmic contact when sintering at higher temperatures is performed, for example beyond 700 °C. In general, contact resistivity reduces dramatically with increasing sintering temperature. Nickel forms no carbides during the sintering process. A carbon layer on the surface must be removed for adhesion reasons of subsequent metals. Optimum nickel thickness is about 50 nm to 100 nm, depending on a trade-off between surface roughening and contact resistivity. Nickel by itself does not form carbides. When sintering temperature is 600 °C, silicides are formed, but no ohmic contact is formed yet.

For ohmic contact formation sintering at temperatures beyond 600 °C is needed, carbon is accumulated at the interface and some carbon moves to the surface. Control of excess carbon is the reason why some alloys come into scope, such as Ni-Cr, Ti-, Ta- and W-based alloys. As-deposited ohmic contacts can be formed with nickel an titanium on n-type SiC if the dopant concentration is in the range of 1×10^{19} cm^{-1} to 2×10^{19} cm^{-1}, resulting in contact resistivities of $1 \times 10^{-3}\,\Omega\,\text{cm}^2$ to $1 \times 10^{-1}\,\Omega\,\text{cm}^2$, which can be lowered by high-temperature annealing. The contact resistivity is preferred to be as low as possible, it can be found in literature [26] that the contact resistance for a nickel contact on 4H-SiC with a N-type doping concentration of 1.5×10^{19} cm^{-3} results in a contact resistivity ρ_c of $7.5 \times 10^{-6}\,\Omega\,\text{cm}^2$, which is equivalent to $750\,\Omega\,\mu\text{m}^2$.

4

Al/Ti for p-type mono-SiC Contact resistivity is higher on p-type SiC which is formed by ion implantation compared to p-type SiC formed by epitaxial growth. Aluminum can be used as good ohmic contact to p-type SiC, given that sintering at 900 °C to 1000 °C is performed. However due to the low melting point, severe segregation of Al takes place. As solution a stacked structure can be used based on a combination of the metals Al(300 nm)/Ti(80 nm)/SiC [27, 28]. Forming an ohmic contact to an epi-layer with a dopant concentration of 1×10^{15} cm^{-3}, will be highly challenging because of the high contact resistance expected, even after a annealing process at 1000 °C for 2 min rapid thermal processing (RTP). Zetterling et al. [29] describe p-type contacts consisting of a stack of Ni/Ti/Al with thicknesses of 10/15/85 nm in combination with rapid thermal annealing in the range of 800 °C to 850 °C.

4.6.2. CONTACTS TO POLYCRYSTALLINE SIC

LITERATURE

When reading literature on contacts to SiC in general, it can be concluded that the majority of the research focuses on the ohmic contacts to α-SiC substrates, while the research in the field of β-SiC, especially in polycrystalline form, is limited. A literature survey has been performed on this topic, and the topics are included in Table 4.12. In summary it can be concluded that the two main metallizations used for interconnecting highly doped poly-SiC layers, are aluminum, nickel and titanium. The main disadvantage of nickel is that it is considered as red metal in cleanroom processing, resulting in a more extensive and complex processing requirements or even limitations to prevent contamination of other processes. In general it can also be stated that as-deposited metallizations typically result in rectifying contacts, while annealing by for example RTP results in ohmic contacts.

Table 4.12: Metals considered for poly-SiC contacts.

Metal	ϕ [eV]	T_{melt} [°C]	$R_{contact}$ [$\Omega\,cm^2$]	Reference
Al	4.06-4.26	660	2×10^{-4} (RT); 1×10^{-3} (400 °C)	[30–32]
Ni	5.04-5.35	1455	5×10^{-4} (RT); 1.5×10^{-3} (400 °C)	[30, 32–35]
W	4.32-5.22	3422	2×10^{-3} (RT)	[30]
(Cr)	4.5	1907	Adhesion layer on Ni	[33]
TiW	n.a.	n.a.	n.a.	[36]
Pt	5.12-5.93	1768	n.a.	[37]
Ti	4.33	1668	n.a.	[38]
TiN	4.2	2930	n.a.	[39]

CONTACTS TO POLY-3C-SIC EXPERIMENTS

To interface the poly-SiC crystalline layer, the contact resistance from metal to poly and the sheet resistance of metal and poly-SiC are of interest. To investigate the latter, ELM, TLM and Kelvin Cross bridges will be processed. In addition, some mechanical test structures can be processed simultaneously, namely longitudinal and transverse piezoresistors. First, zero layer processing will be carried out, followed by standard silicon cleaning. Then an layer for isolation and passivation will be deposited with a thickness ranging from 200 nm to 500 nm. This can be silicon oxide or an a-SiC (Figure 4.19a). In the latter case, the structure is closer to the material combination of the final pressure sensor. A disadvantage might be that patterning and etching are less convenient compared to the standardized silicon oxide layers. 1 µm poly-SiC is deposited on the isolation layer using LPCVD, where the aimed resistivity is equal to the poly-SiC layer for the final device, thus ranging from 0.01 Ω cm to 10 Ω cm (Figure 4.19b). The poly-SiC layer will be patterned using the IM8 SiC Mesa [SC] image from the OXMESA reticle, more information about this mask will be described in Chapter 6. The SiC mesas will be etched using the Trikon Omega (Figure 4.19d). As isolation layer over the mesa structures, both amorphous SiC and silicon oxide can be used. In both cases a thickness of 500 nm is anticipated (Figure 4.19e). Contact holes will be patterned on this isolation layer, and etched open using plasma etching (Figure 4.19e). As metallization layer, initially aluminum will be used with a thickness of 500 nm. Aluminum is a standard CMOS compatible metallization and therefore convenient to pattern and etch. Etching of the metallization can be done wet-chemically with aluminum etch or dry with the Trikon Omega (Figure 4.19f). In order to get ohmic contacts, it might be needed to perform an annealing or sintering step in the furnace stack C, in which metals are allowed. In Figure 4.19 the cross section of the processing flow of the electronic test structures and discrete piezoresistors is included.

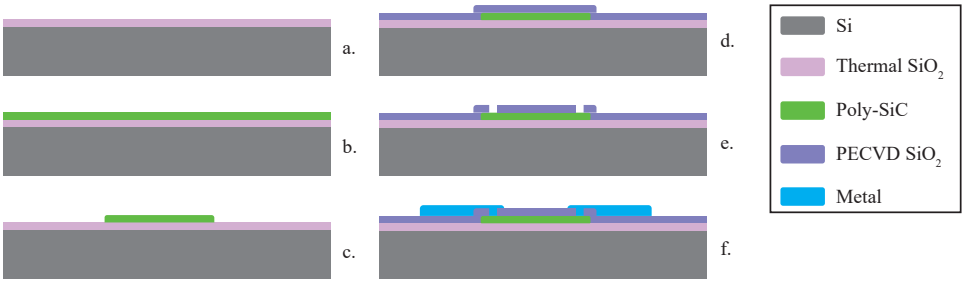
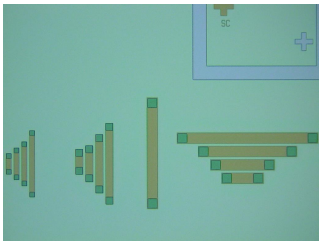


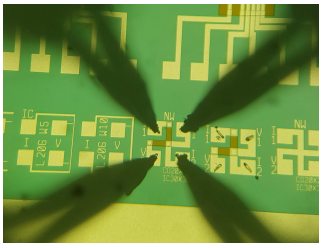
Figure 4.19: The flowchart used for fabrication the electronic test structures, using silicon oxide as isolation and passivation layer.

Standard zero layer processing was performed on wafers 11-13 and 15-17. Wafers 14 and 18 are intended for stress measurements and therefore do not need any zero layer. After the zero layer processing the six wafer for electrical measurements are thermally oxidized in furnace C1 to yield an oxide thickness of 500 nm, which was measured to be 506 nm to 511 nm. Layer D-1 was deposited on wafers 11-14, where a thickness of 1000 nm was aimed for. The sheet resistance values and resulting bulk resistivity values are included in the beginning of this section. Wafer 14 was used to determine the residual stress, after the BS was etched clean. Wafers 11 and 12 are coated with 4 µm photo resist to pattern the image 8 'SiC Mesa', which was exposed using 600 mJ cm^{-2}. Development with recipe DP-2 was performed. Both wafers are etched using the 0 °C LM_SiC recipe on the Rapier for 880 s. After etching, stripping and cleaning, the thickness was determined to vary from 818 nm (center W11) to 996 nm (near flat wafer 11). The Leitz MPV was used to accurately determine the thermal oxide thickness taking into account gradients over the wafer. The Dektak was used to determine the thickness of the stepheight of the SiC mesa. Subtracting both measurements yields the thickness of the poly-SiC layer. 500 nm of PECVD oxide was deposited with the Novellus, and image 4 CO's was patterned using 3.1 µm resist, 420 mJ cm^{-2}, a focus offset of 1 µm (half the resist thickness minus a constant) and DP-1 development. The thicker resist layer was chosen because of the high topography (1 micron mesa SiC strips). Typically 1.4 µm of resist would already be sufficient. The CO's were etched open by using the standard oxide recipe on the Drytek for 65 s. A microscope picture of the etched CO's is included in Fig. 4.20a. 1000 nm of AlSi(1%) was sputtered on wafer 12 at 350 °C and 500 nm of Ti was sputtered on wafer 11 at 350 °C. Different metallizations were used to investigate the effect on the contact resistance. The wafers were coated with 2.1 µm (thicker than nominal due to the topography of the SiC mesas). Image 5 IC was exposed using 270 mJ cm^{-2} and no focus offset. SP-1 development was performed and the metal was

etched using the Trikon Omega. 'Al1m350' recipe was used for etching the aluminum IC. Titanium was etched using a standard Ti etch recipe on the Omega. After inspection, the wafer were stripped and standard metal cleaning was performed. Wafers T11 (Ti) and T12 were taken from the cleanroom for measurements in the Cascade 33.



(a) A microscope picture of the test structures after the CO's have been etched.



(b) 4-point measurements on the square 20 and 30 micron Kelvin Cross Bridges for contact resistance determination.

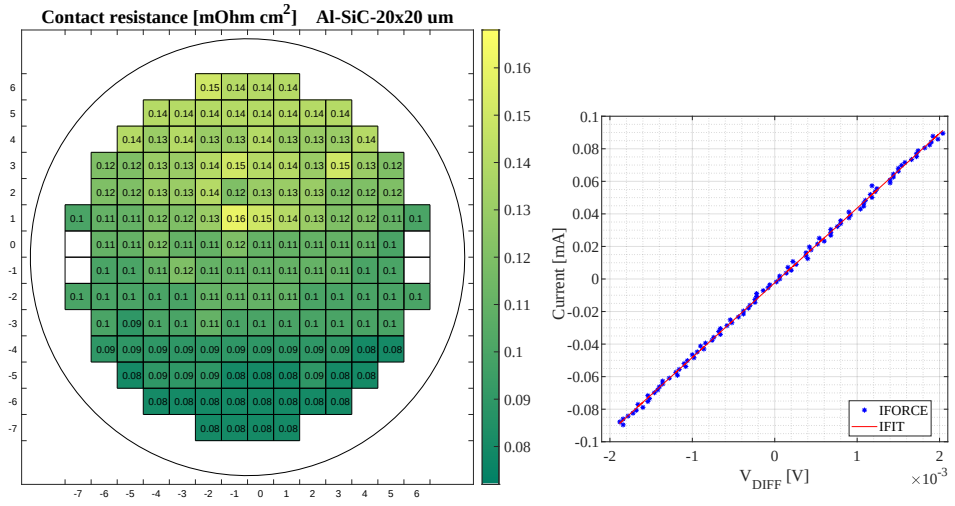
Figure 4.20: Realized electrical test structures.

CONTACT RESISTANCE MEASUREMENTS

After the fabrication of the test structures to determine the contact resistances the Kelvin Cross Bridges (KCBs) are measured using the Cascade 33 probe station. It was decided to perform a wafer scale measurement on wafers 11 (Ti) and 12 (Al). The system of macros and subsites was used to automatically measure both the 20x20 µm and 30x30 µm Kelvin Cross bridges. A microscope picture of the KCBs in the cascade in included in Fig. 4.20b. The software ICcap was used, making use of .mdl files. The force voltage was swept from -0.2 V to 0.2 V, while the current through these two terminals was measured simultaneously. The voltage over the contact resistance was measured by V_{plus} and V_{minus}. The raw data (.mdm files) analyzed using the MATLAB script. This script extracts the variables in which the length and width of the contact was stored, after which the specific contact resistance was calculated based on the contact resistance and area.

Aluminum Metallization The specific contact resistances based on the KCBs of 20 x 20 µm are included in Figure 4.21. What can be seen from the color wafermap is that there appears to be a gradient over the wafer from the bottom to the top of the wafer, where the specific contact resistance varies from 0.08 mΩ cm^2 to 0.15 mΩ cm^2. One specific die, close to the center of the wafer is standing out. The IV-curve of the die with the minimum contact resistance is included in Figure 4.21b. It can be concluded from the straightness of the curve that the contact behaves highly ohmic for these bias and temperature conditions. The specific contact resistances over the wafer for the KCBs of 30

x 30 µm KCB are included in 4.22 and vary from 0.10 mΩ cm^2 to 0.21 mΩ cm^2. Interestingly, the specific contact resistance is slightly higher compared to the 20 x 20 µm, which is not expected since any boundary/edge effects are suppressed more in a larger contact hole. The specific contact resistances measured for the AlSi(1%) sputtered at 350 °C range from 0.8×10^{-4} Ω cm^2 to 2.3×10^{-4} Ω cm^2.

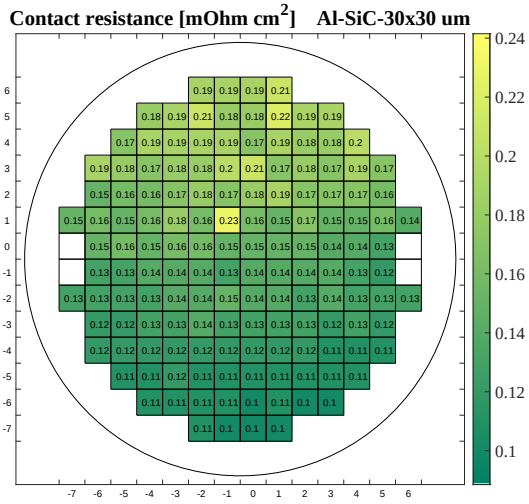


(a) Wafer scale measurements of the specific contact resistances for the 20 x 20 µm KCB with Al metallization.

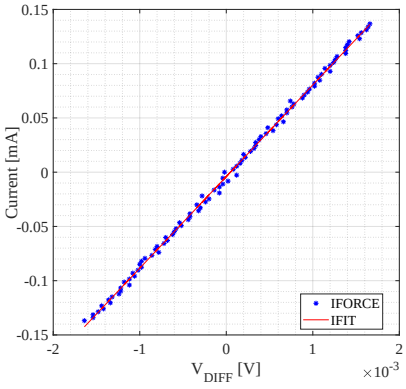
(b) The IV-curve for the minimum contact resistance (die -2,-7).

Figure 4.21: Specific contact resistance measurements of the 20 x 20 µm KCB with Al metallization.

Titanium Metallization The results for the specific contact resistances based on the KCBs of 20 x 20 µm are included in 4.23. Based on these results, there appears to be a slight gradient over the wafer from the bottom to the top of the wafer, where the specific contact resistance varies from 0.11 mΩ cm^2 to 0.18 mΩ cm^2. This gradient is smaller when compared to the Al-SiC contacts. The first die measured in the bottom left corner gives a wrong measurement result caused by misaligned probes damaging the probe pads. The IV-curve of the die with the minimum contact resistance is included in Figure 4.23b from which it can be concluded from the straightness of the curve that the contact behaves highly ohmic for these bias and temperature conditions. The specific contact resistances for the KCBs of 30 x 30 µm KCB are included in 4.24 and vary from 0.14 mΩ cm^2 to 0.22 mΩ cm^2. Similar to the measured contact resistance with Al metallization, the contact resistances for the 30 x 30 µm KCBs is larger compared to the 20 x 20 µm. The specific contact resistances measured for the titanium sputtered at 350 °C range from 1.1×10^{-4} Ω cm^2 to 2.2×10^{-4} Ω cm^2.

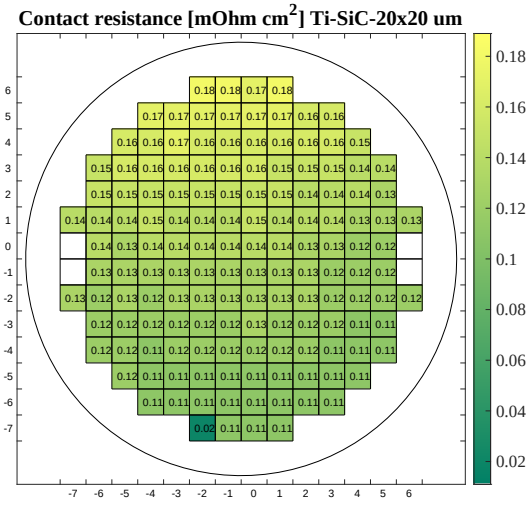


(a) Wafer scale measurements of the specific contact resistances for the 30 x 30 µm KCB with Al metallization.

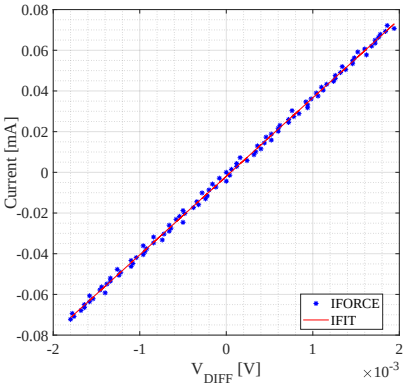


(b) The IV-curve for the minimum contact resistance (die -2,-7).

Figure 4.22: Specific contact resistance measurements of the 30 x 30 µm KCB with Al metallization.



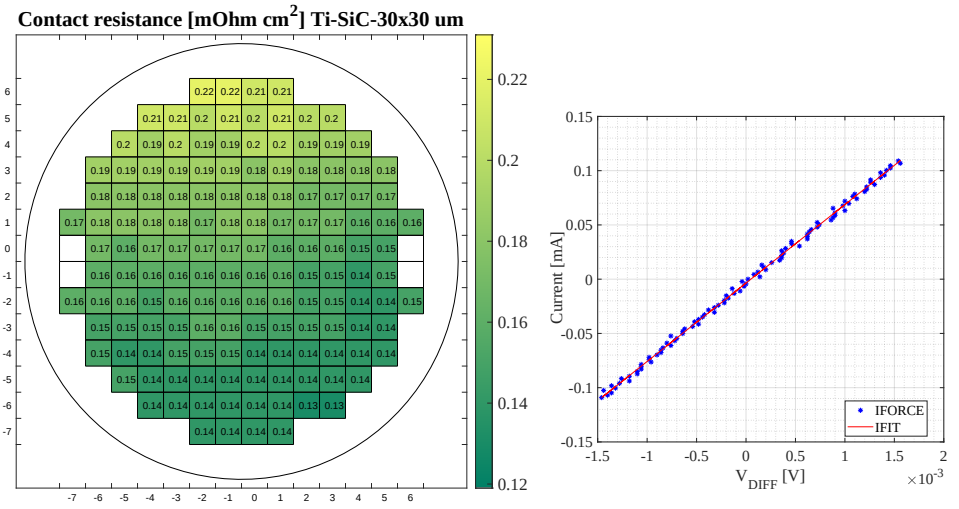
(a) Wafer scale measurements of the specific contact resistances for the 20 x 20 µm KCB with Ti metallization.



(b) The IV-curve for the minimum contact resistance (die -1,-7).

Figure 4.23: Specific contact resistance measurements of the 20 x 20 µm KCB with Ti metallization.

It can be concluded that the specific contact resistance for the Al sputtered at 350 °C is ranging $0.8 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$ to $2.3 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$. The specific contact resistance for the Ti sputtered at 350 °C ranges $1.1 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$ to $2.1 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$. The corresponding



(a) Wafer scale measurements of the specific contact resistances for the 30 x 30 µm KCB with Ti metallization.

(b) The IV-curve for the minimum contact resistance (die -2,-7).

Figure 4.24: Specific contact resistance measurements of the 30 x 30 µm KCB with Ti metallization.

mean and standard deviation of the specific contact resistances measured for the AlSi(1%) and titanium sputtered at 350 °C equal μ = 0.129 mΩcm^2, σ=0.0369 mΩcm^2 and μ = 0.149 mΩcm^2, σ=0.0307 mΩcm^2 respectively. Values given here are for contacting to doped poly-SiC layer D-1, having a bulk resistivity of 0.1 Ω cm. As-deposited titanium metallization can thus be used on D-1 without compromising the contact resistance. The contact resistance might be lowered by using an annealing step after the sputtering.

4.7. SiC Material Definition

To be able to perform multi-physical (FEM) simulations on SiC sensors and structures, physical properties are investigated in this Section.

4.7.1. Defining the Elastic Tensor of 4H-SiC in COMSOL

Although first order mechanical behavior can be estimated by using solely the Young's modulus and Poisson ratio, the true three-dimensional behavior of anisotropic SiC is described by the elastic tensor. 3C-SiC, 4H-SiC and 6H-SiC do all occur in single-crystalline form, where a diamond structure (3C) results in three independent elastic constants in the elastic tensor. 4H-SiC and 6H-SiC show a hexagonal (or Wurzite) structure with different stacking patterns and can be described by five independent elastic constants.

An anisotropic material can be defined in the physics section of the Comsol model by adding a new linear elastic material and defining this as anisotropic. Because in this work, mono-crystalline 3C-SiC is not used, we will focus here on the description of the most common polytype of SiC substrates, namely 4H-SiC.
The elastic tensor is typically denoted by a D matrix and is defined as follows, where σ is equal to the stress and ϵ is equal to the strain.

$$\sigma = D\epsilon \tag{4.12}$$

The elastic tensor of an anisotropic material can be given by its elastic coefficient in Voigt notation, which is commonly used in engineering [40, 41]. The known elasticity coefficients can be found in literature [3, 42] and are included in Table 4.13.

Table 4.13: The elasticity values for 4H- or 6H-SiC [3, 42].

Elasticity coefficient	**Value** GPa
c_{11}	501
c_{12}	111
c_{13}	52
c_{33}	553
c_{44}	163

Translating the elastic coefficients c_{11}, c_{12}, c_{13}, c_{33} and C_{44} depends on the amount of symmetry in the internal structure of the material. Generally speaking, it can be stated that the more symmetry is present, the simpler the structure of the stiffness tensor. Single crystalline 4H-SiC has a hexagonal (wurzite) structure and is a so called transversely isotropic material. This results in the occurrence of indeed five independent coefficients and symmetry transformations in the form of reflections about all three orthogonal planes. This means that c_{22}=c_{11}, c_{23}=c_{13} and c_{55}=c_{44}. As a result the elasticity matrix can be simplified to the following form.

$$\mathbf{D} = \begin{bmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ & c_{11} & c_{13} & 0 & 0 & 0 \\ & & c_{33} & 0 & 0 & 0 \\ & & & c_{44} & 0 & 0 \\ & symm. & & 0 & c_{44} & 0 \\ & & & 0 & 0 & (c_{11} - c_{12}/2) \end{bmatrix}$$

Calculating the equivalent of c_{66}:

$$\frac{c_{11} - c_{12}}{2} = \frac{501\,\text{GPa} - 111\,\text{GPa}}{2} = 195\,\text{GPa} \tag{4.13}$$

Filling out the elasticity matrix D (in GPa) yields:

$$\mathbf{D} = \begin{bmatrix} 501 & 111 & 52 & 0 & 0 & 0 \\ 111 & 501 & 52 & 0 & 0 & 0 \\ 52 & 52 & 553 & 0 & 0 & 0 \\ 0 & 0 & 0 & 163 & 0 & 0 \\ 0 & 0 & 0 & 0 & 163 & 0 \\ 0 & 0 & 0 & 0 & 0 & 195 \end{bmatrix}$$

4.7.2. MECHANICAL PROPERTIES OF 4H-SIC

In addition to the elastic tensor, Table 4.14 summarizes other physical parameters of crystalline 4H-SiC which are relevant for the mechanical behavior. It should be noted that for the determination of the Poisson ratio and the Young's modulus typically a tensile test for a material specimen is conducted. The slope of the stress/strain curve equals an elastic modulus, such as a Young's modulus. As a result, these two parameters are basically a first order (isotropic) approximation of the mechanical behavior of the crystalline material. The true three-dimensional anisotropic mechanical properties are represented by the elastic tensor as described above in Section 4.7.1. More details on the origin and derivation of the Young's modulus and Poisson ratio can be found in literature [3, 4, 42].

Table 4.14: Mechanical properties of 4H-SiC.

Figure	Value
Young's modulus E	390 GPa to 690 GPa [3] - 444 GPa [42] - 448 GPa [4]
Poisson ratio ν	0.21 [3] - 0.157 [42]
Mass density ρ	3.21 g cm^{-3} [3]
Bulk modulus K	213 GPa [42]
Shear modulus G	193 GPa [42]
Yield strength	21 GPa (at RT) 0.3 GPa (at 1000 °C) [3]

The Poisson ratio is used to describe a material's shrinkage or expansion by forces exhibited in transverse direction and is denoted by ν. Another important material parameter is the shear modulus commonly denoted by G, and is related to the Young's modulus E and the Poisson ratio ν. The shear modulus determines to which extend an objects shows the tendency to shear, when acted upon by opposing forces.

$$G = \frac{E}{2(1+\nu)} \tag{4.14}$$

The bulk modulus K measures the change in volume for a given uniform pressure, it can

also be called compressibility. Also K is related to the Young's modulus and the Poisson ratio ν.

$$K = \frac{E}{3(1-2\nu)} \tag{4.15}$$

4.7.3. Material Definition Poly 3C-SiC

In order to simulate SiC sensors by using FEM techniques, it was decided to start with the material definition based on a blank material. The bulk resistivity of the poly-SiC can be tuned by varying the ammonia gas flow rate [43]. The highest gauge factors reported in literature are obtained for a bulk resistivity of polycrystalline 3C-SiC of approximately 0.1 Ω cm [44, 45]. The corresponding gauge factors can be translated into a piezoresistive coupling value of -2.33×10^{-11} Pa^{-1}. Comsol expects a piezoresistive coupling value which is multiplied with the bulk resistivity. The piezoresistive coupling coefficient equals then -2.33×10^{-14} Ωm/Pa, which equals -2.33×10^{-14} m^4 s^{-1} A^{-2} in SI-units. By studying literature for which resistivity the gauge factor is maximal, a range from 10 to 110 S cm^{-1} comes forward [45], which corresponds to 1000 to 1.1×10^4 S m^{-1}. Based on the paper written by Hung et al. the best Gauge Factor of -2.1 was obtained with a resistivity value of 8.33 Ω cm, which corresponds to a conductivity of 12 S m^{-1} [32].

Table 4.15: Properties of poly 3C-SiC for FEM simulations.

Figure	Value
Young's modulus E	430 GPa [46]
Poisson's ratio ν	0.24 [46] 0.168 [43]
Density ρ	3.21 g cm^{-3} [3]
Relative permittivity	9.72 F m^{-1}
Piezoresistive coupling value	-2.33×10^{-11} Pa^{-1}
Hillock size max (poly)	41-140 nm [43]

4.7.4. From Gauge Factor to Piezoresistive Coupling Coefficient

Analog to the elastic tensor, also the relation between stress σ and a change in resistivity $\frac{\Delta\rho}{\rho}$ is described by a matrix, called the piezoresistive coupling matrix. In the case of a polycrystalline layer, this relation simplifies to:

$$\frac{\Delta\rho}{\rho} = \pi\sigma \tag{4.16}$$

Where π equals the piezoresistive coupling value. A well known Figure of Merit (FoM) to denote the amount of piezoresistivity is typically done by the Gauge Factor (GF), which

is defined as [44]:

$$GF = \frac{\frac{\Delta R}{R}}{\epsilon} = \frac{\frac{\Delta \rho}{\rho}}{\epsilon} + (1+2\nu) \tag{4.17}$$

Where R is the resistance of the piezoresistor considered, ρ is the resistivity, ν is the Poisson ratio and ϵ is equal to the strain of the piezoresistor. The resistance change can be split up in a change of bulk resistivity and change of the dimensions of the resistors caused by applied strain, represented by the first and second part of equation 4.17 respectively. The strain is defined as:

$$\epsilon = \frac{\Delta l}{l} \tag{4.18}$$

Where l equals the length of the piezoresistor in the direction of the strain. The stress is connected to the strain by Hooke's law by:

$$\sigma = E\epsilon \tag{4.19}$$

Combining equations above, yield the following relation between GF and the piezoresistive coupling coefficient [47]:

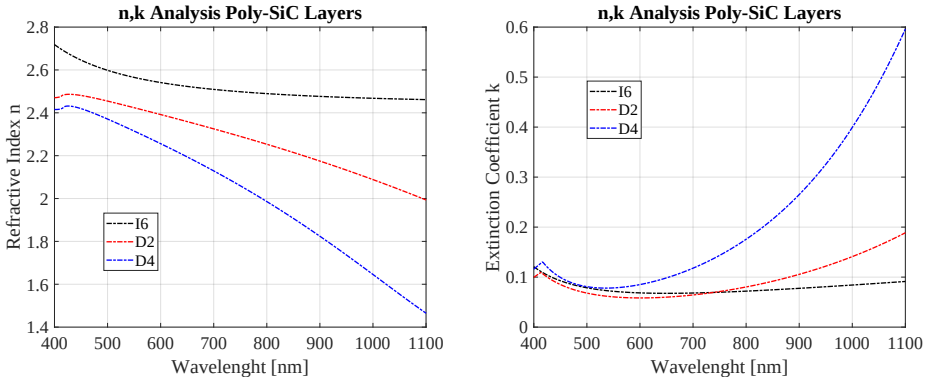
$$GF = E\pi + (1+2\nu) \tag{4.20}$$

The isotropic piezoresistive coupling value π using the Young's modulus as included in Table 4.15 and taking a GF of -10 based on literature [45] equals $-2.33 \times 10^{-14}\,\Omega\,\mathrm{m\,Pa^{-1}}$.

4.7.5. OPTICAL CHARACTERIZATION OF POLY 3C-SIC LAYERS

For the anticipated usage of poly-SiC for the development of optical poly-SiC membranes, as will be discussed in Chapter 5, the optical properties of three different poly-SiC layers were investigated.

The optical properties of intrinsic and doped poly-SiC layers are measured using variable-angle spectroscopic ellipsometry (J.A. Woollam M2000) on 1000 nm thick layers on 500 nm SiO_2 that is thermally grown on Si. Subsequent modeling in WVASE (J.A. Woollam) is used to derive the optical properties over the entire visible spectral range between 400 nm and 650 nm as index of refraction. The refractive index and extinction coefficient as modeled over the range from 400 nm to 1100 nm are included in Figure 4.25. It be concluded that the refractive index is reduced for increasing doping concentration. Furthermore that the increasing doping concentration results in a higher absorption in the IR, whereas this barely influence the opacity in the visible range.



(a) The refractive index n.

(b) The extinction coefficient k.

Figure 4.25: The n,k values for undoped ((I6) $\rho > 400\,\Omega\,\text{cm}$) and doped poly-SiC layers ((D2) $\rho = 20.56 \times 10^{-3}\,\Omega\,\text{cm}$ and (D4) $\rho = 3.36 \times 10^{-3}\,\Omega\,\text{cm}$). *Ellipsometry data analysis and model fitting was performed by M. Ghaderi (Chalmers University of Technology). The deposition and ellipsometry measurements were carried out by the author.*

4.8. CONCLUSIONS

When the second goal as listed in Section 1.6 is revisited, it can be concluded that this Chapter gives a demonstration of important fabrication steps for the realization of SiC (MEMS) sensors. Experiments were carried out to convert theory from literature in to recipes and processes in the EKL infrastructure. Findings on the different topics are given below.

Lithography Lithography has been performed on 4H-SiC substrates including zero layer processing where alignment markers are etched. Apart from a different reflectivity and corresponding coating, exposure and development cycle tuning, lithography on 4H-SiC substrates is straight forward and no problems were encountered. Alignment on the frontside can be done without any modifications. The transparency of the substrates enabled backside wafer alignment, where the markers were recognized through the wafer. This has the advantage, that standard frontside alignment can be used, even when the backside of the wafer is to be exposed on the condition that symmetric alignment markers are used.

4H-SiC Etching As can be deducted from literature, etching of bulk 4H-SiC is non-trivial. Standard etch recipes tailored for bulk silicon can not one to one be used to etch 4H-SiC. Standard plasma etchers, such as ICP etchers, can be used to etch trouble-free up to etch depths of several 100 nm, for example for etching alignment markers. To

have an indication of maximum performance of the available infrastructure, the best-known hardmask (Ni) was used in combination with known etch fluorine etch recipes and tuned such that a stable etch process is yielded. After different etch experiments it can be concluded that indeed an etch depth can be achieved ranging from 6 µm to 12 µm at high etch powers (2 kW) and relatively long etch times (30 min), but that severe micro masking occurred resulting in a spiked surface on the bottom of the etch openings. Future research should focus on the development of more stable hard masks and optimization of the etch recipes.

Poly-SiC Etching Etching of polycrystalline (3C-)SiC was carried out by using different cleanroom tools ranging from an uncooled single-wafer Alcatel GIR300 etcher to a SPTS Rapier i2L etcher in ICP mode. Multiple experiments were carried out based in SF_6/O_2 chemistry, in which different etch parameters were varied such as power, temperature and gas flow ratio. It was found that the best selectivity was achieved at etch temperatures 0 °C and 10 °C. Apart from the selectivity, the reproducibility (since no end-point detection is available) and homogeneity over the wafer were considered important aspects on which the etch performance was assessed. Because the poly-SiC layers considered in this work only appear in thin-film form, the etch rate itself was less of importance.

Laser Ablation Apart from classical cleanroom compatible reactive ion etching processes, micromachining by using the photo-thermal and photo-chemical interaction between crystalline SiC and a high power laser can be performed. Experiments were carried out using a femtosecond laser in the available infrastructure. In contrast to the expectations, etching-through a 360 µm thick 4H-SiC substrate for a square surface area of 400 µm width was performed already after an etch time of 7 min. Due to the nature of the laser ablation process, in order to make this technique feasible for fabrication of MEMS and microsystem, challenges lay in the control of the etch depth, the finishing of the ablated surface, the thermal damage to the bulk material and in cleaning considerations and removal of excess material after ablation.

Metal-SiC Contact and Metallization The formation of ohmic contact to crystalline SiC is based on the chemical reaction between SiC and the metal, where silicides and/or carbides are formed at high temperatures (500 °C to 1000 °C). This process is typically referred to as silicidation, and, when the self-aligning property is exploited (for example in CMOS technology), is sometimes denoted as salicides, an acronym of self-aligned silicides. The main challenges for ohmic contact formation to 4H-SiC is to find one

metal for both n-type and p-type SiC, due to the large bandgap. Because of the grain boundaries and the inter-bandgap traps between the valence and conduction band, the formation of ohmic contact to poly-SiC is less problematic, even when this poly-SiC layer is only lightly doped. This was illustrated by the formation of ohmic contact by sputtering Ti and Al at 350 °C without additional annealing steps. It can be expected, based on the consensus described in literature, that the contact resistance can be further brought down when annealing steps are performed. For all metallization schemes, long temperature stability in harsh environments should be taken into consideration.

SiC Elastic Properties Before any design phase of SiC devices is considered in which the mechanical behavior plays any role, the quantities describing the mechanical behavior of the material should be defined. As starting point the elastic tensor for 4H-SiC has been defined in addition to quantities describing the mechanical and electrical behavior of poly-SiC for the development of MEMS devices, for example pressure sensors.

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5

SiC Heated Window enabling Optical PM Sensing

To exhibit the added value of poly-SiC as building material for sensors, this Chapter discusses the design, realization and characterization of a heatable transparent poly-SiC windows which enable optical instrumentation to be used in PM sensors. Ensuring optical transparency over a wide spectral range of a window with a view into the tailpipe of an ICE powered vehicle, while exposed to the harsh environment of soot-containing exhaust gas, is an essential requirement for introducing optical techniques for long-term monitoring of automotive emissions. In the first operating mode, window transparency is periodically restored by pulsed heating of the membrane using an integrated resistor for heating to temperatures that result in oxidation of deposited soot 600 °C *to* 700 °C. *In the second mode, the membrane is kept transparent by repelling soot particles using thermophoresis. The same integrated resistor is used to yield a temperature gradient by continuous moderate-temperature heating. Realized devices have been subjected to laboratory soot exposure experiments. Membrane temperatures exceeding* 500 °C *have been achieved without damage to the membrane. Moreover, heating of membranes to* ΔT= 40 °C *above gas temperature provides sufficient thermophoretic repulsion to prevent particle deposition and maintain transparency at highly-concentrated soot exposure, while non-heated identical membranes on the same die and at the same exposure get heavily contaminated.*

Parts of this chapter have been published in Sensors MDPI (2019) [1], on the IEEE 29th International Symposium on Industrial Electronics (2020) [2] and on the OSA Optical Sensors and Sensing Congress (2020) [3].
Parts of this chapter are included in patent *Method for fabricating thin-film ceramic membrane structures.* Valorization Center Delft University of Technology, application number: **NL2024326**, The Netherlands, (2019).
Parts of this chapter are included in patent *Transparent micro-electro-mechanical membranes for enabling the optical measurement of properties of soot containing exhaust gas, and modes of operation for keeping their surface clear from deposits.* PRV, application number: **SE 1930413-8**, Sweden, (2019)

5.1. Introduction

Full characterization of exhaust gas is essential for meeting increasingly strict automotive emission requirements. State-of-the-art on exhaust gas sensing is based on devices in direct contact with the gas flow, such as electrochemical sensors for the measurement of gas composition [4] and electrical conductance (conductometric) sensors for particulate matter (PM) [5]. A more elaborated analysis on conductometric soot sensors in included in Appendix A, where impedance spectroscopy is applied to investigate enhanced data collection of existing measurement concepts. The next generation of sensors for compliance with emission requirements should be suitable for the measurement of soot particle number concentration (PN) in relation to their size distribution, which is difficult to achieve when using state-of-the-art accumulating conductometric soot sensors [6]. Optical techniques provide a more robust approach in the harsh environment of the soot-containing gas in the tailpipe of the combustion engine and would enable the non-contact collection of more information as compared to currently used techniques, but only on the condition that optical access to the particle rich gas flow is maintained. Therefore, a harsh environment compatible window is needed that stays clear of (soot) contaminants. The reduced light transmission over time through the window with the build-up of such light-absorbing layers of contaminants in its path of propagation has hindered the implementation of otherwise potentially promising optical approaches for measuring exhaust gas properties [7]. Figure 5.1 shows a typical vehicle's exhaust system including the particulate filter that need to be monitored, in which the location of the anticipated optical PM sensor is denoted. Such a PM sensor will be part of the so-called on-board diagnostics system (OBD) of ICE powered vehicles.

In literature, many optical (MEMS) gas sensors are reported. Gas composition can for example be analyzed using absorption spectroscopy and soot particle size distribution using angular scattering spectroscopy. Results of short-term exhaust gas composition measurement based on absorption spectroscopy have been reported using glass fiber probes for entering light into the exhaust system [8–11]. An optical window is also a functional part in a probe for Laser-Induced Incandescence (LII) studies on soot particles [12]. However, the duration of reported tests on actual exhaust gas does not exceed 30 minutes [13]. Therefore, approaches for restoring or maintaining window transparency are an essential prerequisite for the successful introduction of optical techniques for long-term, in-situ monitoring of exhaust gas emissions, as will be required by regulations.

The wall of the exhaust pipe is the colder part during normal operation of the combustion engine. Combustion results in a hot exhaust gas and, consequently, in temperature

gradients in the exhaust pipe, with a descending maximum temperature at the center of any cross-sectional area along the axial direction and a minimum at the wall. The radial temperature gradient causes the thermophoretic force that pulls the soot particles in the gas flow toward the colder inner wall surface. Thermophoresis (or thermo-migration or thermo-diffusion) can be explained by referring to the temperature dependence of the Brownian motion of gas molecules, which increases with temperature. In a highly simplified interpretation, gas molecules in between the particle and the center of the flow channel vibrate more vigorously as compared to those in between the particle and the colder wall, thus yielding a net force pushing the particle toward the wall. A more fundamental analysis of this phenomenon can be found in literature [14].

Thermophoresis is actually part of the operating mechanism of the conductometric PM sensor. A DC bias voltage of about 45 V is applied across two Interdigitated Electrodes (IDEs). Soot particles in the exhaust gas flowing along the sensor surface are pulled toward the sensor surface, because of the combined effect of the thermophoretic pulling force (due to the colder wall surface on which the sensor is mounted) [15] and the electrophoretic force (due to the electrostatic field) acting on charged particles [16]. As a result, soot particles are deposited and form dendrites (connected strings of particles) on the sensor surface, eventually bridging the two IDEs. Since carbon is electrically conductive, such a dendrite forms an electrically conductive path. The resulting decrease in resistance is used as a measure of PM [5].

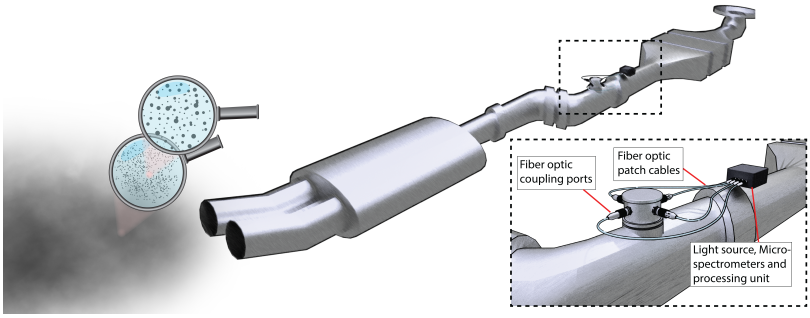


Figure 5.1: The position of the considered optical exhaust gas measurement system. Source: [17].

A window composed of an optically transparent intrinsic poly-SiC membrane with a diameter ranging from 100 µm up to 2000 µm is designed and realized in a CMOS compatible cleanroom. N-type doped poly-SiC heaters are fabricated on top of the membrane and two modes of operation are investigated for maintaining transparency. In the first mode (regeneration), window transparency is periodically restored by pulsed heating of the membrane using the integrated heater to temperatures that result in oxidation

(burning) of deposited soot (600 °C to 700 °C).

In the second mode, the membrane is kept transparent by continuous heating using the same integrated heater to result in a temperature increase, ΔT, of typically 40 °C to 100 °C relative to the temperature of the surrounding gas it is exposed to, which is typically 400 °C. The resulting thermophoretic force repels airborne soot particles in close proximity of the surface and prevents deposits on the membrane. Combined operation is envisaged, using mode two continuously for minimizing deposition and mode one at regular intervals for the removal of any remaining deposits. A typical system includes several windows mounted on the wall of the exhaust pipe, with some providing access of a light beam that is intended for interacting with the gas, and others for ensuring transmission of the resulting information-carrying modulated light to a detector.

Also in the existing conductometric PM sensors, integrated heaters are used to regularly heat the substrate up to a temperature of about 600 °C to periodically oxidize the soot, which is referred to as 'regeneration of the surface' [15]. This known mechanism for surface regeneration can in principle be directly implemented for periodically restoring window transparency. However, in the case of our optical transparent membrane, care should be taken of any remaining thin films. These films can for example originate from engine lubrication oil. In the case of light with a wavelength component λ, a residue with an (optical) thickness in the range λ \10 – λ \2 may cause interference that significantly affects the optical spectral transmission. Therefore, the presence and effect of such films need to be investigated for an assessment of the effectiveness of mode 1 operation for optical regeneration of the membrane surface.

Thermophoresis has been explored in conductometric PM sensors as a means for sensitivity control. A reduced sensitivity with increased temperature was confirmed [15]. Heating of membrane structures fabricated in silicon MEMS technology have been extensively reported in literature and usually involves a material combination of (poly)silicon, silicon-oxide and silicon-nitride with integrated resistive heaters. Applications are in devices that require only a few degrees of temperature above ambient temperature, such as thermal flow sensors [18], while heating is used in thin-film SnO_2-based gas sensors for setting the surface temperature for maximum sensitivity [19]. Hot-wire blackbody emitters have been fabricated for use in infrared (IR) optical applications [20]. Usually, the heated devices are fabricated on a membrane or ceramic substrate to limit heat loss due to thermal conduction to ambient and thus ensure power efficient operation.

The application of a regenerable optical window presented here imposes specific requirements. Firstly, the exhaust environment is generally considered a harsh environment, both from the thermal and the chemical perspective. Secondly, the membrane

material should preferably be transparent over the spectrum between the near-ultraviolet (UV) (220 nm) and mid-IR (5 µm). A conventional membrane material, such as SiO_2, does satisfy this requirement, while other materials, such as Si_3N_4, are less suitable. Poly-silicon (poly-Si) can only be considered a transparent material in the IR (and highly absorbing in the visible spectral range). The electrically conductive layers used for heater fabrication should preferably also be transparent.

Silicon-carbide (SiC) is a highly suitable building material for both the transparent membrane and the heater structure. As was already elaborately stated in Chapter 1, SiC has numerous advantages over silicon technology. Highly relevant to the application of heatable optical window considered here are its high chemical inertness, optical properties and high melting temperature [21–23]. Related to the topic of this Chapter, SiC has already been considered in literature for fabrication of hot-wire emitters operating at high temperatures [24].

Among the different forms and polytypes available, for the conception of the heatable suspended transparent windows, polycrystalline 3C-SiC will be used. The advantages of this material are that it can be conformally deposited in a LPCVD furnace, while in-situ doping is applied to control the doping and residual stress level of the resulting layer. The potential of the integration of the poly-SiC material deposition with silicon substrates, along with the silicon technology portfolio, is exploited. Intrinsic SiC can be considered a low-loss optical material in the spectral range between 400 nm and 2 µm. However, depending on doping concentration, doped SiC can be used as an optical material of reasonable performance in the spectral range between 400 nm and 400 nm. This restriction, as compared to the desirable UV-to-IR, limits the application to the visible. The index of refraction, n, and extinction coefficient, k, of SiC and wavelength dependencies thereof do depend of the flows of the different gasses during LPCVD. More information about the n,k of different poly-SiC layers can be found in Chapter 4.

5.2. DESIGN

A schematic drawing of the design of the optical window is shown in Figure 5.2. The structure is basically composed of a suspended optically transparent membrane. An electrically conductive layer on top is patterned into a resistor and can be used for heating of the membrane. The heater can be used for both for the surface regeneration in mode 1 and the thermophoretic repulsion in mode 2. The heater should preferably be optically transparent for effective use of the entire membrane area as window. In case of significant differences in optical transmission between the membrane- and the heater material, or differences in their wavelength dependencies over the spectral range con-

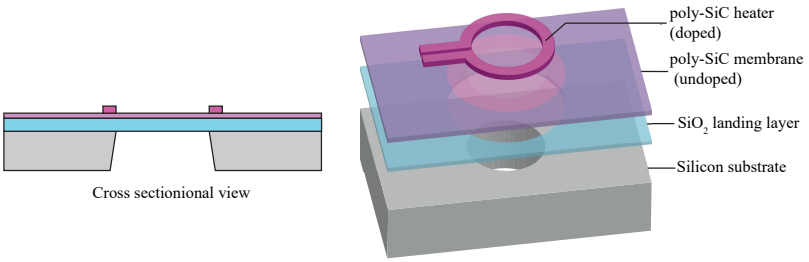
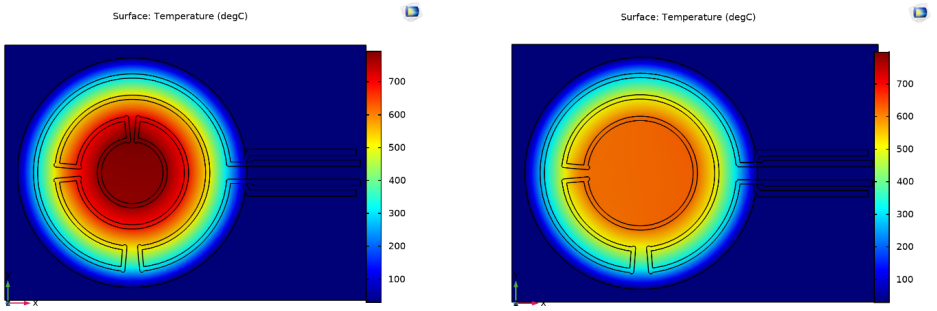


Figure 5.2: Schematic view of the basic structure of the transparent membrane and the heater. Note that the metallization is not included in this view.

sidered, a design that blocks the light at the position of the latter is to be used, to avoid a wavelength-dependent average transmission throughout the window area. The reduced area available as window due to opaque electrodes and heater is sometimes specified in optics in terms of the 'fill factor'. DRIE was used to bulk micromachine the silicon substrate.

The dimensions of the membrane result as a compromise between the minimum aperture required for passing a practical light beam, and the maximum diameter that can be sustained when considering residual stress in the layers that comprise the membrane and its thickness. The absolute value of the tensile stress is increasing with increasing dopant concentration in the poly-SiC layers considered. A small to moderate tensile stress is desired in order to achieve a flat, non-buckled membrane. The SiO_2 layer functions as landing layer for the through-wafer etch, and its thickness was chosen to be 2 µm. In order to yield a membrane with minimal optical extinction, its thickness should be kept to a minimum. On the other hand, a larger thickness results in a higher mechanical strength, which is required considering the application in an automotive exhaust environment. The membrane layer thickness was designed to be 500 nm. The diameter of the windows ranges between 50 µm and 2000 µm.

A uniform temperature profile is desirable for optimum operation of the transparent window, with minimum membrane area occupied by the heaters. Moreover, power efficiency should be considered. Heat diffusion from the membrane to the surrounding rim implies that the outer part of the heater should be at a certain distance from the rim, which makes a compromise between a uniform temperature profile and low power dissipation inevitable. 3D finite element analysis (FEA) was used to analyze the geometry of the heater and membrane, based on the measured material properties and at realistic flow conditions. The layout was optimized for uniform temperature at a given power dissipation and drawn in layout editing software.



(a) Lateral temperature distribution on a MEMS window for 4 heater loops.

(b) Three loops at 3 W.

Figure 5.3: Simulated temperature distributions. *FEM simulations performed by M. Ghaderi (Chalmers University of Technology).*

LPCVD is used for deposition of an intrinsic SiC film and a highly doped SiC film. The sheet resistance of the deposited films was measured using a four-point Kelvin measurement. Based on the large difference between the resistivities of the intrinsic SiC (about 440 Ω cm) and the highly doped SiC layer ($\rho_{\mathrm{HIGH}} = 3.36 \times 10^{-3}$ Ω cm) it can be calculated that the current densities in these layers differ by three orders of magnitude. Based on the large separation of the electrical bulk resistivity between the intrinsic and the highly doped version of the poly-SiC layer, it was decided that a passivation layer in between the heater and membrane layers is not necessary, thus favoring fabrication convenience. These values were included in the Finite Element Model (FEM) for analyzing the different heater designs at realistic conditions and the results are shown in Figure 5.3. The Temperature Coefficient of Resistivity (TCR) of the undoped SiC is not considered in these simulations, which limits the validity of the simulation results to the lower operating temperature range. The membrane diameter was kept constant at 1000 µm with a constant heater trace width of 20 µm and the temperature profile of a heater with a different number of turns is shown in Figure 5.4.

At a constant injected power of 3 W, the structure with more heater loops generates a higher peak temperature at its center. Most implementations are based on four-loop heater designs, for a peak temperature in excess of 700 °C over a diameter exceeding 400 µm.

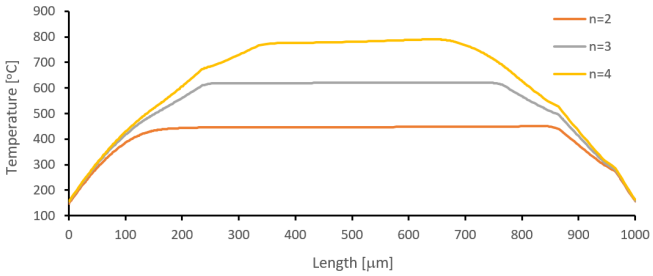


Figure 5.4: Temperature profile along the diameter of the membrane at 3 W injected power for a different number of heater loops with a heater width of 20 µm. *FEM simulations performed by M. Ghaderi.*

5.2.1. Mask Design

The mask design described in this section is performed by M. Ghaderi (Chalmers University of Technology) in close collaboration with the author.

5

The mask design is based on a diesize of 10 x 10 mm and on the usage of the ASML PAS5500 wafer stepper. The available reticle space of 21 x 21 mm in combination with a 10x10 die results in four images:

1. Heater
2. Cavity
3. Metal
4. Contact opening

The contact opening image is in principle not needed, because the metal will only be patterned at the desired locations, while only one metallization layer is needed. In case that for isolation purposes between the structural poly-SiC layer and the metal interconnect a dielectric is still required, the image for the CO is available.

Cavity sizing The cavities which will be etched through the wafer have been designed with different opening sizes, namely 100 µm, 200 µm, 240 µm, 500 µm, 1000 µm and 2000 µm. These opening sizes are based on the available space, the FEM simulations and the realization possibilities when considering DRIE etching processes.

Heater design The heaters are designed according to the size of the suspended membrane. For the smaller membranes, mainly circular plain and meander shaped circular heaters have been designed. Because of the relative small area and thus distance to the membrane center, this design yields in a homogeneous temperature distribution. For the 2000 µm membranes, a more complex heater was designed, to guarantee homogeneity along the membrane, see also Figure 5.5. In devices M3 and M13, additional

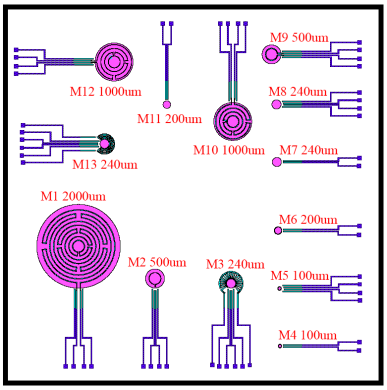


Figure 5.5: Topcell of the mask design, including the annotated membranes with different sizes.

poly-electrodes have been designed to be able to apply an external electric field, in order to study the effects of electrophoresis.

Metal Metals considered are AlSi(1%) and titanium. Probe pads have been designed based on standardized sizing. For some devices, four electrical connections are designed, where 2 are used to inject power into the heater (i.e. constant current), while the other two connections enable voltage measurements yielding a Kelvin measurement during operation to monitor the impedance of the heater. The metal traces are designed such that the distance between the metal/CO interface and the electrode (to supply E-field) or heater is equal. Two devices have been designed including two additional metal traces to interconnect the poly-electrodes which will be used to study the effects of electrophoresis, denotes as devices M13 and M3 in Figure 5.5.

5.3. FABRICATION

5.3.1. POLY-SIC CHARACTERIZATION

The resistivity, the residual stress, the deposition rate and the optical properties of the deposited poly-SiC layers using furnace F3 are verified in this section. Standard SSP, P-type, 525 µm wafers were deposited with different poly-SiC layers, ranging from undoped poly-SiC to doped layers with different doping gradation. The poly-SiC is deposited by LPCVD where the precursor gasses can be tuned. The ratio between the two precursor gasses is denoted by the Gas Flow Ratio (GFR). This influences the basic properties of the poly-SiC layer. Additionally, ammonia can be added during deposition, resulting in nitrogen doping (n-type).

The two layers of used are investigated by depositing approximately 1000 nm on different test wafers. For each layer two test wafers were used with 500 nm thermal silicon oxide, and two bare Si wafers. The bare wafers are used to determine the total residual stress, after the backside has been etched clean. The wafers with 500 nm thermal oxide are used to determine the resistivity and the deposition rate. The undoped layer will be used as structural layer for the optical membrane, while the doped poly-SiC will be used for forming the heater structure. The two layers chosen for the fabrication of the devices are the intrinsic layer I-6 and the doped layer D-4. These annotations relate to the layer definition used by Morana [25], who previously investigated poly-SiC deposition by LPCVD in the EKL infrastructure. The choice for these two layer types has been made because the intrinsic layer has the highest resistivity, and the 'spacing' of the anticipated resistivities between both layers is maximized to minimize leakage currents through the membrane. The measured results are summarized in Table 5.1. The bulk resistivity was determined based on the determined realized layer thickness.

$$\rho = R_{sheet} \cdot th \tag{5.1}$$

Table 5.1: The used layers with deposited poly-SiC layers to determine the optical properties.

Layer ID	GFR	Resistivity	Stress	Dep. rate
I-6 (0 sccm NH3)	6.5	439.8 Ω cm	65 MPa (Tens.)	12.22 nm min^{-1}
D-4 (4.0 sccm NH3)	5.0	0.003 369 Ω cm	503 MPa (Tens.)	10.71 nm min^{-1}

5.3.2. Wafer processing

The intrinsic SiC layer is to be used as optical window, while the highly doped layer is patterned to form the heater structure. The poly-SiC is deposited by LPCVD where the precursor gas flows can be tuned. The ratio between the two precursor gasses, SiH_2Cl_2 and 385 sccm of Ethyn C_2H_2 (5% in H_2), is denoted by the Gas Flow Ratio (GFR). The GFR essentially determines composition of the SiC layer and its physical properties. For the intrinsic (undoped) carbide the GFR is chosen such that a maximum resistivity is obtained. More details on the deposition of the polycrystalline SiC layers are reported by Morana et al. [25]. Practical implementation of SiC as a material for a transparent window requires a wavelength-independent index of refraction, n, for wideband index matching to air or dielectrics such as SiO_2 that are often used for surface coating, and low values for the extinction coefficient, k, for low-loss optical transmission. Based on the optical poly-SiC layer characterization as discussed in Section 4.7.5 it can be concluded that the index of refraction, n = 2.4 ± 0.2 and extinction coefficient, k < 0.1.

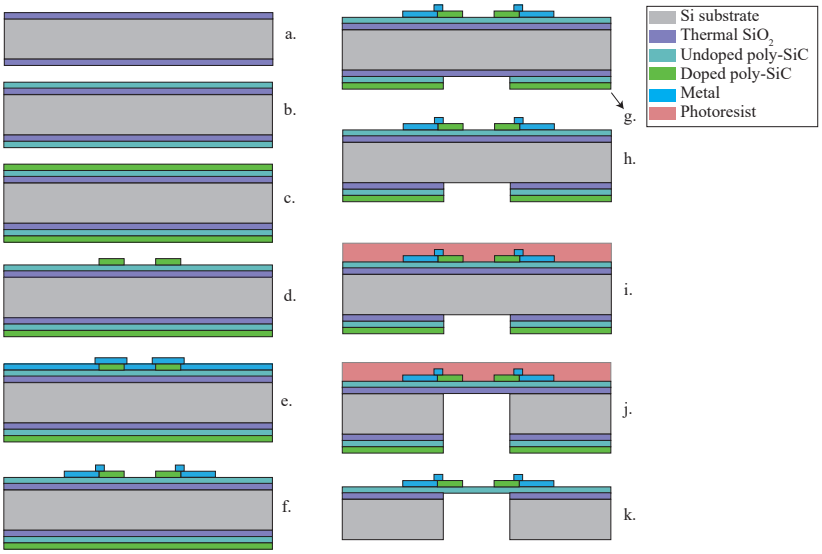
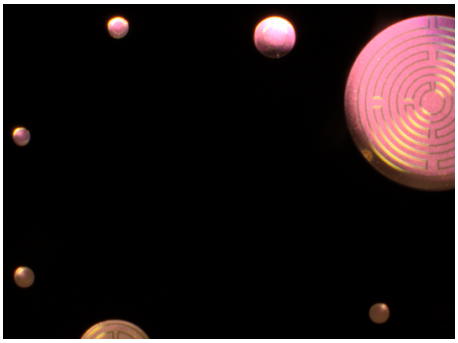
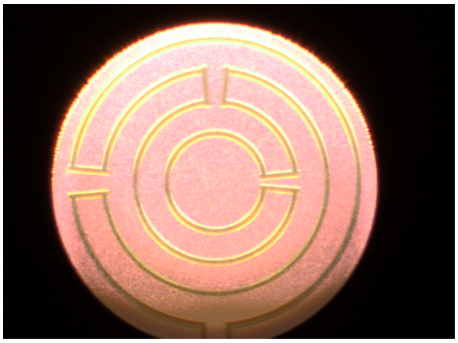


Figure 5.6: Schematic flow of the fabrication process.

Device fabrication starts with the growth of 2 µm of SiO_2 by thermal oxidation of a silicon wafer, which is intended as etch-stopping (landing) layer during through-wafer etching and hardmask at the backside (BS) for definition of the DRIE cavity etching (Figure 5.6a). In addition, this layer provides some thermal isolation between the substrate and the subsequently deposited poly-SiC layers. After thermal oxidation, two poly-SiC depositions by LPCVD followed (Figure 5.6b-c) using the already characterized intrinsic and highly doped poly-SiC layer. The residual stress for the intrinsic layer was measured to be 65 MPa and for the highly doped layer 503 MPa. Such moderate tensile stress levels ensure flat membranes without buckling. The next step is the coating of the frontside (FS) of the wafer with 4.0 µm AZ3027 photoresist (PR) and applying lithography. A timed etch was used for the definition of the heater structure out of the doped poly-SiC layer. A DRIE etcher (SPTS Rapier) in ICP mode was used (Figure 5.6d). The etch recipe is based on an SF_6/O_2 mixture at 0 °C to enhance selectivity between the PR and poly-SiC. After the heater structures were formed, standard wafer cleaning was performed followed by metallization. For five wafers 500 nm AlSi(1%) was deposited and on another set of five wafers 500 nm pure titanium (Ti) was deposited (Figure 5.6e). Both depositions were carried out at 350 °C to yield the best metallization quality and low contact resistance. Lithography was performed and the patterned AlSi(1%) and Ti were etched using a plasma etcher (Trikon Omega) at 25 °C, after which the wafers were stripped cleaned (Figure 5.6f).



(a) Inspection of membranes which are etched-through with an optical microscope using backlight.



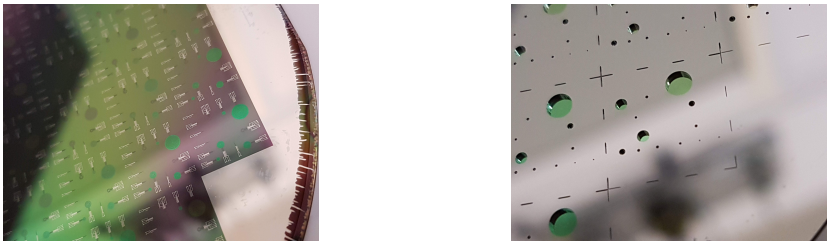
(b) The 1000 µm membrane.

Figure 5.7: Inspection with an optical microscope using backlight only.

The hardmask on the BS, which is composed of the thermal oxide layer and the two poly-SiC layers, was opened in phases. First backside lithography is performed and the poly-SiC was etched with an Omega ICP etcher (Figure 5.6g). The thermal oxide was subsequently opened using wet-chemical etching with 1:7 BHF (Figure 5.6h). The frontside of the wafer was coated with photoresist for protection of the metallization and to give structural support to the membrane layer once the DRIE process reaches the landing layer (Figure 5.6i). Etching through the wafers was done with an SPTS Rapier DRIE etcher (Figure 5.6j). Because both poly-SiC and thermal oxide are transparent in the visible range, visual inspection using an optical microscope with backlight illumination can be used to see which of the membranes are open, see also Figures 5.7a and 5.7.

Due to the stress mismatch between the 500 nm poly-SiC membrane (moderately tensile) and the 2 µm thick silicon oxide landing layer (compressive), the membranes are buckled right after the DRIE process and before the removal of the SiO_2 landing layer. In order to supply mechanical support to the membrane, a so-called stress-relief layer can be applied. In this work, a photoresist layer is applied on the frontside of the wafer, as is indicated in Figure 5.6i. Photoresist has no residual stress in the layer itself, but mainly strengthens the membrane. In cases where the buckling is even more of an issue, stress compensation can be performed with this stress relief layer, for example by using silicon oxide or another dielectric comprising similar stress direction as the used landing layer.

For the wafers with AlSi (1%) interconnect (IC), the oxide etching was achieved in vapor HF. Four cycles of 300 s each was used to give a successful result (Figure 5.6k). The wafers with aluminum IC were spray-coated after this release step to enable the removal of



(a) Frontside view. **(b)** Backside view.

Figure 5.8: Membranes with integrated heaters and Al interconnect after vapor HF release.

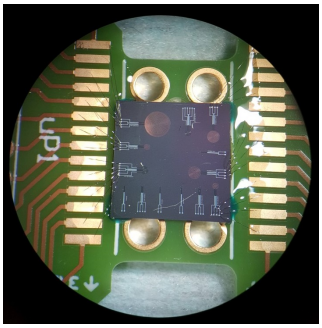
the dicing foil from the thin membranes in an acetone rinse during final dicing and packaging. For the wafers with Ti interconnects, wet-chemical etching with 1:7 BHF was used to remove the thermal oxide landing layer, after the FS was protected again by a spray coated PR layer and subsequent baking steps. Figure 5.8 shows the result after completion of wafer processing.

5.3.3. PACKAGING AND WIREBONDING

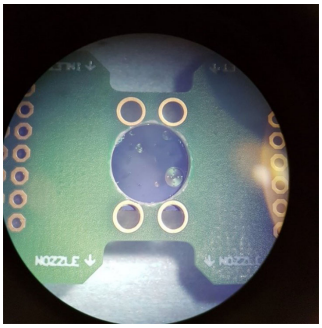
When dicing the other wafers, the blue standard foil was used in combination with the spray coated photoresist on the FS of the wafers. The stack of PR and dicing foil protect the membranes from the intense water jet which is used to cool the dicing saw. The foil was removed by pouring the diced wafer in a bath of acetone. In this bath the spray coated PR dissolves, and the dies are released from the dicing foil. The dies were afterwards rinsed with IPA. Wafers are diced into $10 \times 10\,\mathrm{mm}^2$ dies and subsequently bonded on a printed circuit board (PCB) with a 9.5 mm hole by using thermal curable glue. The dies are aligned in such a way that all membranes on the die can be simultaneously illuminated and inspected, as shown in Figure 5.9. Initial experimentation is limited to exhaust gas at room temperatures, which a PCB can withstand. Wire bonding with aluminum wire was applied for the chips with AlSi (1%) IC, whereas bonding with gold wire was used for the chips with Ti IC. UV curable glue was applied below, on and around the bonding wires for mechanical support during transportation and measurements.

5.4. MEASUREMENTS AND CHARACTERIZATION

This section discusses the electrical and thermal characterization of the realized devices, as preparation on the soot particle deposition experiments.



(a) Frontside view.



(b) Backside view.

Figure 5.9: Dies bonded on a test PCB.

5.4.1. Oven calibration measurements

In order to heat the optical windows up to well-defined, predictable and measurable temperatures the injected amount of power should be linked to temperature. Because it is expected that the DC resistance of the heaters is a function of temperature, an oven calibration is carried out. The PCB with soldered wires is put in an oven while the temperature in the oven is ramped up in steps of 10 °C while simultaneously the DC resistance is measured. The temperature at the location of the silicon die is measured with a thermocouple. Both the thermocouple and Keithley SMU read-out was done using LabView. The voltage used for reading out the resistance was 200 mV in order to prevent self-heating. An overview of the used equipment in included in Table 5.2 and a schematic overview of the measurement setup is included in Figure 5.10.

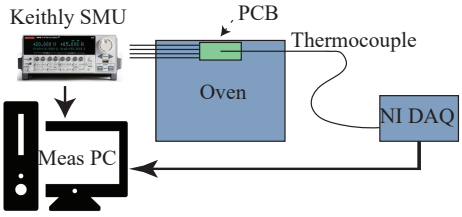


Figure 5.10: A schematic overview of the oven calibration setup.

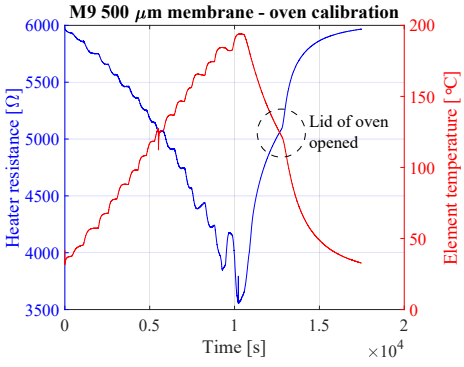
Equipment	Model/make
Oven	Lindberg/Blue M tube furnace TF55035A
Thermocouple	Omega K-type
SMU	Keithley 2420
Software	LabView

Table 5.2: Oven calibration equipment.

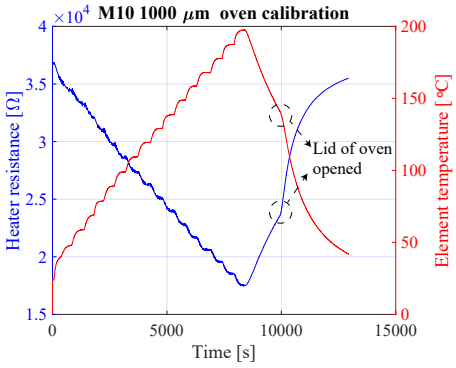
Based on the initial heating tests, it was found that membranes M9 and M10 were most promising based on the mechanical robustness and thermal homogeneity over the membrane. The step-wise increase of the temperature was done to have well-defined coarse steps in the ramping temperature. This would help linking the measured impedance data to the temperature data, in case the relation between both would have been weak.

The maximum temperature equals 195 °C, which is about the maximum that the materials of the prototype can be exposed to.

In Figure 5.11a the measurement results on the 500 µm membrane are included. The stepwise increasing temperature is clearly visible, along with the consistently decreasing resistance. As can be noted are the temperature and resistance measured both during ramping up the oven temperature as during cooling off. The spike in the measured temperature around 5500 seconds is the result of the thermocouple falling out of the oven. The discontinuity of the slope in both the measured resistance during the cooling off phase is caused by the lid of the oven being opened.



(a) The time domain results with the step-wise increasing temperature and the decreasing resistance for M9.



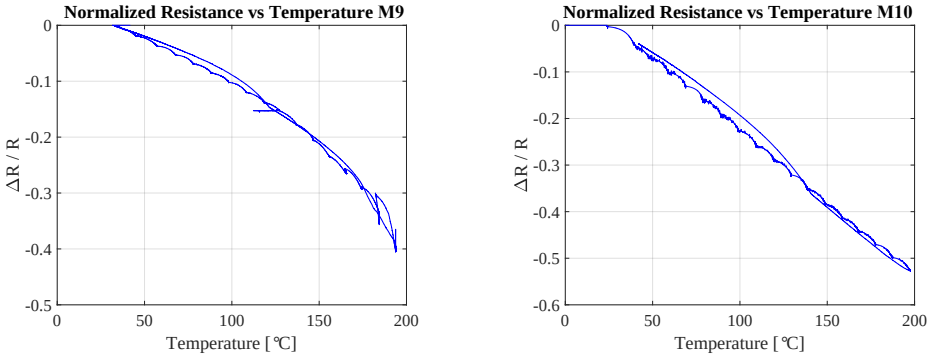
(b) The time domain results with the step-wise increasing temperature and the decreasing resistance for M10.

Figure 5.11: The results of the oven calibration measurements on the 500 µm and 1000 µm membranes

Similar to the measurements carried out on M9, the 500 µm membrane, the calibration measurements were carried out on the 1000 µm membrane M10. In Figure 5.11b the time domain measurement is included. What can be concluded from this result is that the resistive response as function of the temperature is much more linear. Again here the slope change is visible caused by opening the lid of the oven, during the cooling cycle. Additionally, the performance of the temperature control of the oven appears to be better in this case, compared to the calibration measurement on M9.

At last, to be able to compare the resistance vs temperature behavior with the state-of-the-art in the literature, for both oven calibration measurements, the resistive behavior is normalized and plotted against temperature in Figure 5.12. This is done for membrane M9 in Figure 5.12a. Clearly distinguishable is the step-wise increase in the temperature and the smoother decrease in temperature. Additionally lay both ramps not exactly on top of each other. Both effects indicate that still a temperature difference ex-

ists between the thermocouple and the silicon substrate. In general it can be said that a decreasing resistance is yielded when temperature is increased. The high degree of linearity as was seen in the time domain plot, becomes apparent too in the normalized resistance vs temperature plot of the oven calibration on M10, included in Figure 5.12b. Based on a linear fit and corresponding histogram (not included here), the linearization described the behavior of the heaters within 10 Ω of the measured data. Furthermore shows the histogram a Gaussian distribution, indicating that this linear fit is a legitimate way of describing the thermal/resistive behavior.



(a) $T_0 = 31\,^{\circ}\mathrm{C}$. **(b)** $T_0 = 24\,^{\circ}\mathrm{C}$.

Figure 5.12: The normalized resistance over the temperature for M9 and M10 as a result of the oven measurement.

TCR determination

Resistance as function of temperature for (semi)conductors is typically defined as:

$$R = R_{ref}[1 + \alpha(T - T_{ref})] \tag{5.2}$$

Where R is the resistance at temperature T in °C, R_{ref} the resistance at the reference temperature, α the temperature coefficient of resistance and T_{ref} the reference temperature.

Rewriting gives the TCR, denoted as α:

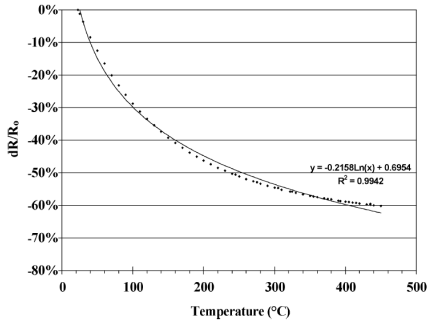
$$\alpha = \frac{1}{R_{ref}} \frac{R - R_{ref}}{T - T_{ref}} \tag{5.3}$$

The definition of the TCR is thus basically the slope of the resistance/temperature characteristic normalized to the resistance at the reference temperature.

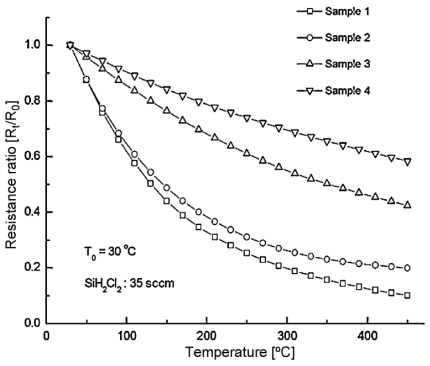
The measured TCR's are in the same order of magnitude and in the same direction as

Table 5.3: TCR of the oven calibration.

Heater	α [°C^{-1}]	T_{ref} [°C]
M9	-0.0023	31
M10	-0.0033	36



(a) The measured normalized resistance by [26], TCR of $-0.0053\,°C^{-1}$ for poly-SiC with 1.34 Ω cm.



(b) The measured normalized resistance [27], TCR of $0.002\,°C^{-1}$ for poly-SiC with 1.34 Ω cm.

Figure 5.13: Measured resistance change with increasing temperature reported in literature.

reported in literature. Hung et al. reports a TCR of $-0.0053\,°C^{-1}$ at 25 °C which decreases to at $-0.0019\,°C^{-1}$ at 400 °C. The poly-SiC layer used in this work was deposited at 1050 °C using n-type doping, resulting in a resistivity of 1.34 Ω cm. The TCR measured over temperature by this work is included in Figure 5.13a. Additionally, it can be mentioned from the work by Hung et al. that a layer with a higher resistivity, results in a larger TCR. A layer with a resistivity of 4.15 Ω cm showed a TCR of $-0.0069\,°C^{-1}$ at 25 °C and decreases to $-0.0031\,°C^{-1}$ at 400 °C.

Noh et al. [27] performed an extensive analysis on the TCR as function of the doping concentration, and used very similar methods for the poly-SiC deposition as used in this work. The main conclusions from this work were that the resistance decreased with increasing temperature. Secondly, that the magnitude of the TCR (absolute value) of doped layer smaller is compared to lowly doped poly-SiC. Thirdly, that the linearity of the TCR should be better in highly doped layers. From the experiments described, layer 4 comes closest to the layer used in this work for the heater formation. Different gass flow ratio's were used compared to this work. The absolute DCS, Ethyn and ammonia flow in [27] were resp. 35, 9 and 1 sccm, yielding a GFR of 4. In this work the DCS, Ethyn and ammonia flows used are 80, 16 and 3 resp., yielding a GFR of 5. When correcting the ammonia flow from [27] for the difference in the sum of the DCS and Ethyn flow,

the effective ammonia flow in this work is approximately 1.5 sccm. The resistivity of [27] for layer 4 equals 0.036 $\Omega\,cm^{-1}$. The $\frac{\Delta R}{R}$ of the results of [27] is included in Figure 5.13b. The measured resistivity of this layer by Noh et al. is around 10 times larger to what was measured in this work, which can be explained by the larger ammonia flow, although the decrease is more dramatic than one would expect. A detailed comparison is not straight forward, since not all recipe details are known. The TCR measured by Noh et al. equals −1957 ppm /°C which equals 0.002. Concluded from literature can be that:

- The resistance goes down with increasing temperature, yielding a negative TCR. This corresponds to the findings in this work.
- The absolute value of the TCR is a function of the doping concentration and thus the resistivity. The lower the resistivity, the smaller the TCR in absolute value, but with a larger linearity.
- The drop in resistance over a temperature range from 20 °C to 200 °C is around 50-60 %, which corresponds to the findings in this work.
- The TCR measured in this work is in the same order of magnitude as reported in literature [26] [27]. The reported TCR by Noh et al. is with 0.002 close to the measured values in this work.
- The resulting average TCR (α) measured over different heater structures equals α= -3289 ± 89 ppm $°C^{-1}$. The uncertainty is assumed to be due to non-linearity only.

5.4.2. Infrared calibration

Based on the calibration measurements, the settings and parameters of the available FLIR thermal camera can be verified. The equipment used for this measurement setup is included in Table 5.4 and a schematic overview of the measurement setup is included in Figure 5.14. The emissivity was determined by linking the oven calibration measurements with the measured impedance data. The 2x lens enabled a resolution in the order of 50 µm. The power injected was delivered by the Keithley SMU, which was controlled via LabView on the measurement PCB.

Membrane M10 - 1000 µm

The heater on the membrane is biased using a constant current, because it was determined in section 5.4.1 that the TCR of the poly-SiC bulk material is negative. A constant voltage biasing would therefore result in an unstable system, since the injected power

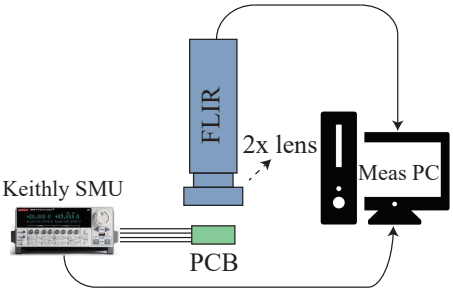


Figure 5.14: A schematic overview of IR camera measurement setup to inspect the thermal behavior of the membranes.

Equipment	Model/make
IR camera	FLIR A325sc
Lens IR camera	T197214 close-up 2x lens
Emissivity used	0.8
SMU	Keithley 2420

Table 5.4: Equipment measurements thermal camera.

is described by equation 5.4, in which $R \propto -T$, i.e. TCR < 0. When a constant voltage biasing is used, and the resistance is decreasing with proceeding time, the injected power increased causing instability. This effect was observed in initial measurements where the temperature increased dramatically in a very sudden way, causing damage to the membrane, by a formed rip near the stem of the heater, indicating a hotspot. A microscope image of this rip is included in Figure 5.18.

$$P_{injected} = \frac{V_{bias}^2}{R(T)} \tag{5.4}$$

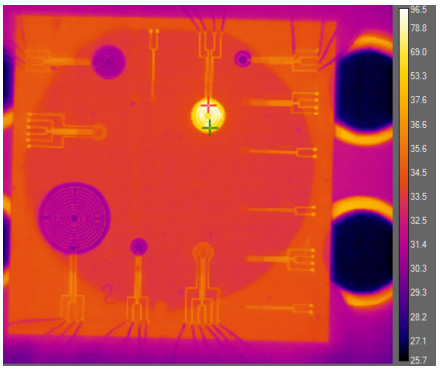
Now, if $R \Rightarrow 0$, $P_{injected} \Rightarrow \infty$.

When a constant current biasing is used, the injected power will decrease if the resistance of the heater is decreasing with increasing membrane temperature, resulting in an inherently stable system, which is illustrated by equation 5.5.

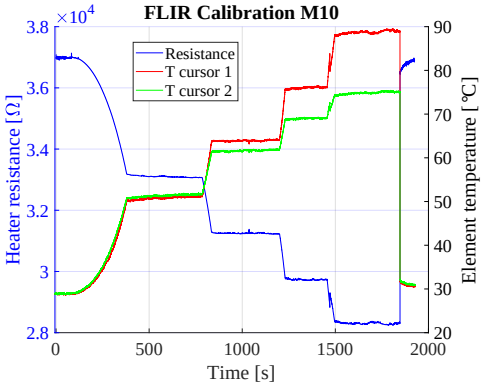
$$P_{injected} = I_{bias}^2 R(T) \tag{5.5}$$

Now, if $R \Rightarrow 0$, $P_{injected} \Rightarrow 0$.

The heater on membrane M10 was biased such that a steady-state temperature were reached of 96.5 °C. Despite the stable way of operation when using current control, the temperature was still non-uniform eventually resulting in a hotspot. The cursor locations and the heat map are shown in Figure 5.15a, cursor one (red) is located near the 'stem' of the heater, while cursor 2 (green) is located toward the outer region of the heater. The measured temperature and DC resistance is included in Figure 5.15b. The non-uniformity is apparent by comparing both temperature cursor traces. The non-uniformity increases as the temperature increases. An explanation of the non-uniformity, or even hot-spot areas can be that the leakage currents through the mem-



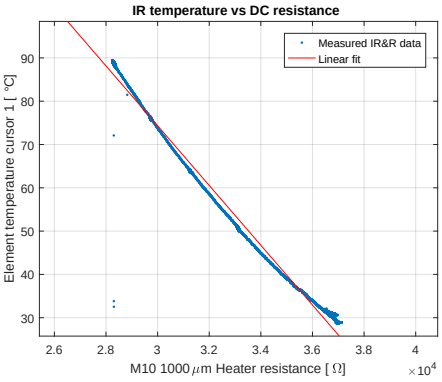
(a) The cursor locations used to obtain the temperature data.



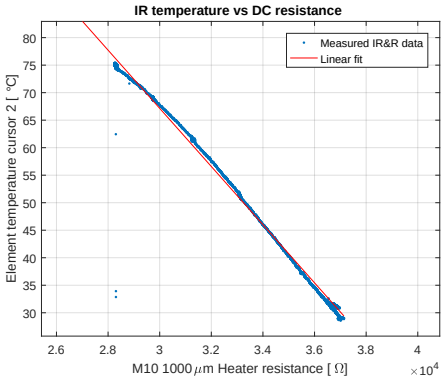
(b) The measured resistance and temperature by the two different cursors in the time domain. Note that the colors of the temperature traces correspond to the colors of the cursors.

Figure 5.15: FLIR calibration measurements on M10.

brane are larger than anticipated during the design phase. The reason that these parasitic currents, and thus the hot-spot areas, are largest near the stem of the heater is caused by the electric field between two neighboring heater traces being maximum in these areas. The increased leakage currents will be discussed in Section 5.4.2. The small heat capacity of the membrane is illustrated by the rapid decrease in temperature when then biasing is switched off at around t=1800 s.



(a) The measured data points in DC resistance against temperature for M10 for cursor 1.



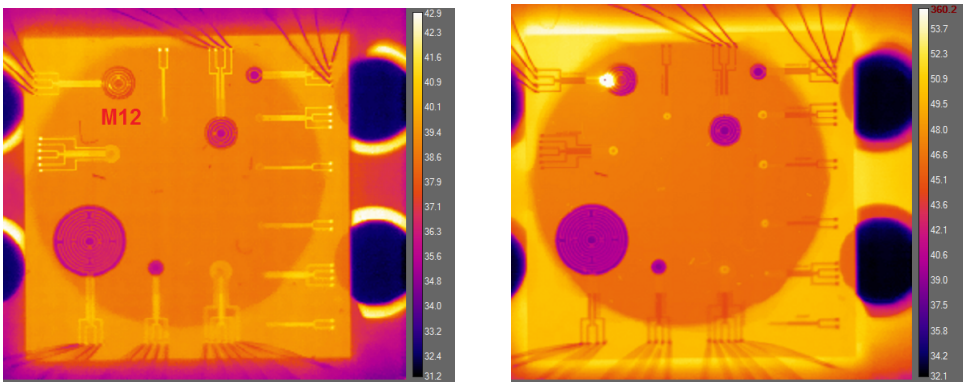
(b) The measured data points in DC resistance against temperature for M10 for cursor 2.

Figure 5.16: DC resistance versus measured temperature for both cursor locations.

When plotting the temperature as function of the measured resistance for cursor 1 and cursor 2, Figs. 5.16a and 5.16b are yielded respectively. What is apparent from these results, is the high degree of linearity of both characteristics, enabling a linear fit. Secondly, the reproducibility of the measured data is considered good, because in these plots a stepwise ramping up and sudden cooling down are included. When the resulting graphs are observed, it is obvious that the temperature/resistance characteristics for both ramping-up and ramping down lay on top of each other. This indicates further that no hysteresis effects appear, thanks to the low thermal (500 nm thin membrane) capacitance and large out-flux of heat to the surrounding air.

MEMBRANE 12 - 1000 µm

Membrane M12 was measured with the FLIR thermal camera, while the current was ramped up. At the start of the ramp, it can be seen from Figure 5.17a that the heating is homogeneous and the entire heater is contributing to the increase in temperature. When the temperature increases, 1 hotspot starts to arise at the stem of the heater structure, see also Figure 5.17b. The hotspot is glowing which can be seen by the naked eye, which implies a temperature of 500 °C. The highest temperature measured with the FLIR was just below 400 °C. The discrepancy can be explained by the size of the hotspot in relation to the finite resolution of the FLIR with the 2x zooming lens of 50 µm. Images of the glowing hotspot are included in Figure 5.19.



(a) M12 at starting of current ramp.

(b) M12 at temperature beyond 360 °C at the hotspot.

Figure 5.17: The different on homogeneity while heating M12.

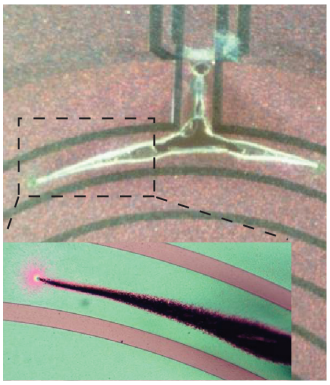


Figure 5.18: Microscope inspection of the ripped M1 membrane including zoom-in.

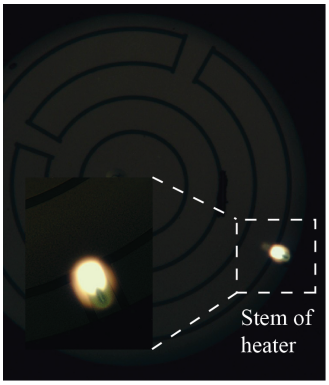


Figure 5.19: The glowing hotspot on M12.

Leakage Currents and Resistivity Undoped Poly-SiC

The increasing degree of non-uniformity of the temperature while increasing the injected power needs to be investigated. The non-uniformity eventually results in thermal hotspots between the feeding electrodes around the stem of the heaters. It is likely that this hotspot is caused by parasitic current flowing through the membrane. This is investigated based on the physics of semiconductors. The resistivity of an (intrinsic) semiconductor equals:

$$\rho = \frac{1}{e(\mu_n n + \mu_p p)} \tag{5.6}$$

Where e is equal to the elementary charge, μ to the mobility and n and p to the free electron and hole concentration. Because we are investigating the membrane, which was intended to be undoped, the resistivity equation simplifies to.

$$\rho = \frac{1}{n_i e(\mu_n + \mu_p)} \tag{5.7}$$

Because in an intrinsic semiconductor $n_i = n = p$. To investigate the resistivity behavior as function of temperature, an estimation was done based on available data from literature. The intrinsic carrier concentration as function of three different temperatures was put in our model, based on Kimoto et al. [21]. The intrinsic carrier concentration shows a strong positive dependency on the temperature, which should lower the total resistivity.

From literature [21] it can be further concluded that the mobility is in general decreasing with increasing temperature, caused by scatting effects on atomic level. The mo-

bility is typically described by $\mu \propto T^{-n}$, where T is equal to the temperature, and n is determined by the doping concentration. For lightly doped 3C-SiC, it was reported by [21] that an n of 2.6 could be used. The mobilities are retrieved from [23], being 750 $cm^2 V^{-1} s^{-1}$ and 40 $cm^2 V^{-1} s^{-1}$ for electrons and holes respectively. Note that the decreasing mobility works against the increasing intrinsic carrier concentration, and would increase the resistivity of the poly-SiC layer. There is thus in an interplay between an increasing intrinsic carrier concentration and decreasing mobility as temperature increases. This effect is supported by literature [28].

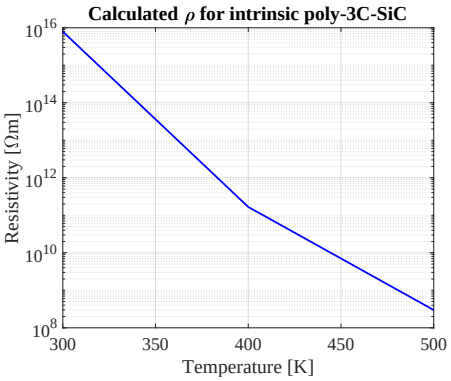


Figure 5.20: The approximated resistivity versus temperature for the intrinsic membrane layer as function of temperature.

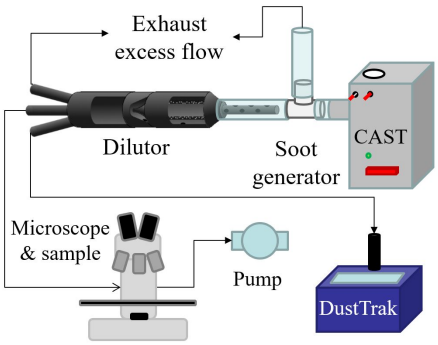
Using the values described above, the resistivity as function of temperature is included in Figure 5.20. Although the mobility is a decreasing function of the temperature, the large increase in intrinsic carrier concentration is the dominant effect in the resistivity as function of temperature. The decreasing resistivity can explain why the large parasitic currents are mainly present at elevated temperature, and result in the observed hotspots among different inspected membranes. The resistivity drops 5 orders of magnitude when the temperature is increased from 300 K to 400 K.

5.5. PARTICLE MEASUREMENTS

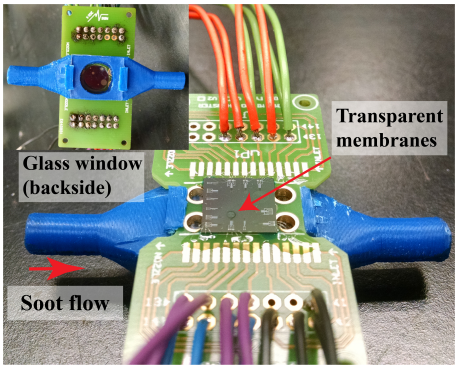
5.5.1. SETUP

Actual validation of the interaction between the fabricated windows with soot-containing gas is carried out by in-situ measurements of opacity using an optical microscope and an aerosol conditioning setup (Figure 5.21a). A Jing MiniCAST 5201c creates a reproducible lognormal soot distribution with a mean geometric diameter near 80 nm by burning propane. The size distribution of the soot used for these experiments is in-

cluded in Figure 5.22. A vacuum pump and a mass flow controller are used to pull flow through the 3D printed sample holder housing at a flow rate in the range 100 cm^3 min^{-1} to 1000 cm^3 min^{-1}, see also Figure 5.21b for more details on the flow housing and the interface PCB. The housing constrains the PCB and slide glass to create an optical path for observation of soot deposition through transmission mode optical microscopy.



(a) The measurement setup to generate a reproducible soot containing gas flow for testing the optical SiC windows. *Modified image based on original from D. Bilby (Ford Motor Company).*



(b) The die including different poly-SiC membranes mounted in the 3D-printed housing.

Figure 5.21: The measurement setup used for characterization of the realized SiC windows.

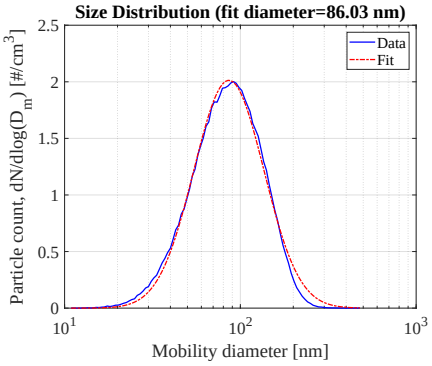


Figure 5.22: The size distribution of the CAST program 2 soot. *Reproduction based on data from D. Bilby (Ford Motor Company).*

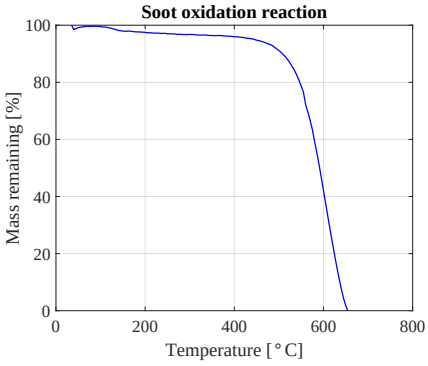


Figure 5.23: The normalized mass reduction caused by regeneration as function of temperature. *Reproduction based on data from D. Bilby (Ford Motor Company)*

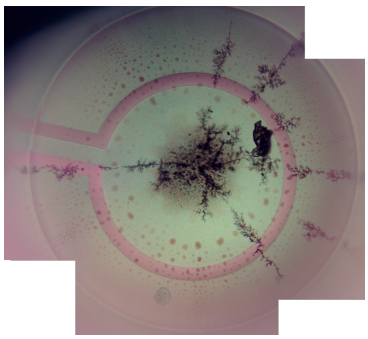
Samples were exposed at the backside of the membrane. A Vickers optical microscope fitted with a Dino-Lite eyepiece USB camera was used for periodic imaging with constant exposure levels to enable observation of soot accumulation on heated and un-

heated membranes. A Keithley 2420 Source Measurement Unit (SMU) was used to drive the heater at constant voltage or constant current and data acquisition is based on Labview. Soot-rich flow was diluted and the actual soot concentration was measured using an AVL microsoot sensor and TSI DustTrak. The nominal heater resistance at room temperature for the 1000 µm diameter membrane is $R_o = 36.85\,k\Omega$ at 298 K. The heater resistance is correlated with window temperature via oven and infrared camera calibration experiments as described in Section 5.4.1.

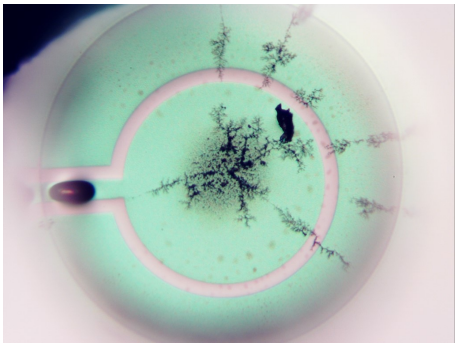
5.5.2. MODE 1 - REGENERATION

It is known from literature that the soot oxidation reaction is an abrupt function of temperature, with the onset to combustion at about 500 °C to full combustion at 700 °C, depending somewhat on operating conditions [29], as illustrated by Figure 5.23.

The devices were designed for surface regeneration (mode 1) over the entire membrane area. However, as was already determined after the infrared calibration as described in section 5.4.2, the temperature dependence of the free carrier concentration in the intrinsic SiC membrane results in a localized increase of leakage current at the warmer parts of the membrane and, consequently, in a further increase of localized heating. These hotspots were used here for the surface regeneration experiments. The hotspots result from a higher-than-expected leakage current between the intrinsic SiC layer and the doped SiC at elevated temperatures and is due to the temperature dependence of the free-carrier concentration in the intrinsic layer. To achieve the uniformly distributed and high-peak temperature profile required for mode 1, dielectric isolation between membrane and heater needs to be included for future iterations.



(a) M9 before regeneration, note the soot dendrites being in the region around the hotspot.



(b) M9 after regeneration, note that the soot dendrites are removed, but that damage has been done at the hotspot area.

Figure 5.24: Regeneration experiment on membrane M9.

Regeneration experiments were carried on membrane M9 with a diameter of 500 µm. Soot dendrites have been grown on and in the region around the hotspot, as is visible in Figure 5.24a. This soot is deposited by diffusion, showing a dendrite structure. This represents a realistic deposition scenario and the dynamic effects during deposition, caused by the flow and resulting turbulence, are included in the soot deposition pattern. Because of the finite resistivity at elevated temperatures of the membrane layer, regeneration should be performed by exploiting the available hotspot. The current was ramped-up, even up to temperatures where the membrane start glowing at the hotspot. This glowing results in a local permanent change of the material, which appears to be a buckled region. The reason why this membranes was pushed beyond the point of glowing (and consequent permanent material change) is that the soot particles were still too far away from the hotspot. Due to the large temperature gradient from the center of the hotspot to its surroundings, the hotspot was heated up far above the 'start-glowing' temperature, in order to bring the soot deposited regions above 500 °C.

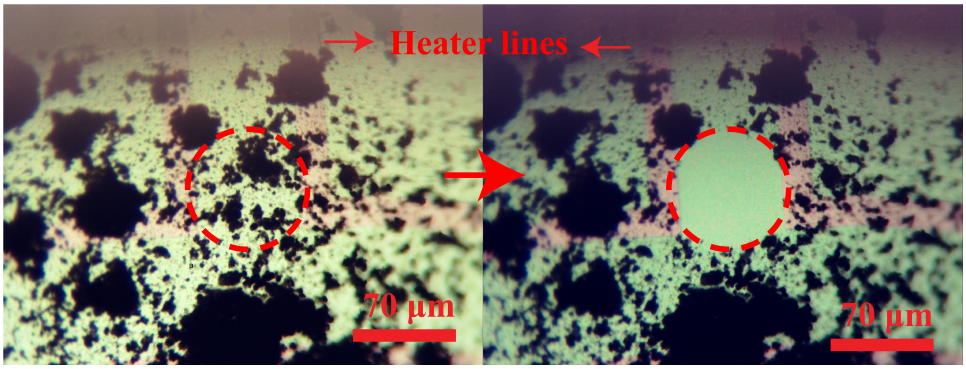


Figure 5.25: The hotspot on membrane M1 before (left) and after (right) the regeneration process, note that the soot is locally removed at the hotspot without permanent deformation of the membrane.

Figure 5.25 shows the result of regeneration experiments exploiting membrane M1. Based on the experience with the soot by diffusion from the regeneration experiment on membrane M9, the soot on this membrane is deposited by impaction, rather than by diffusion in the in-line flow soot accumulation setup. The impaction was carried out by pointing the outlet of the diluted soot rich gas at an angle of approximately 60° to the backside of the membranes. The advantage of impaction is the higher soot deposition rate. The heater current was slowly ramped up until the regeneration process was observed. The regeneration time for reaching the situation shown in Figure 5.25(right) from that in Figure 5.25(left) is typically 5 minutes. During the regeneration experiment, the heater resistance was continuously measured by the SMU and the resistance

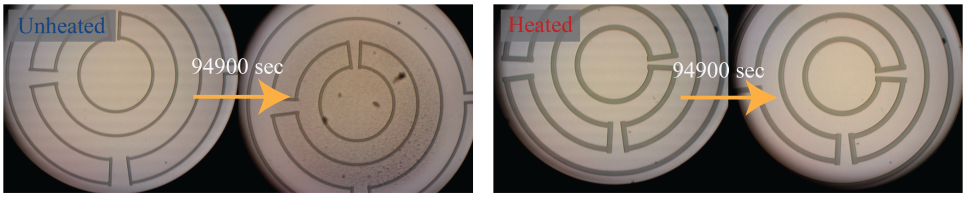


Figure 5.26: Contamination prevention by using thermophoretic repulsion on membranes M10 (right) and M12 (left). The microscope images indicate that the heated 1000 µm membrane stays transparent after constant exposure to a soot rich gas flow over a period of 94 900 s, in contrast to the unheated 1000 µm. Note that these picture are taken from the frontside of the die, thus the soot is inspected through the membrane.

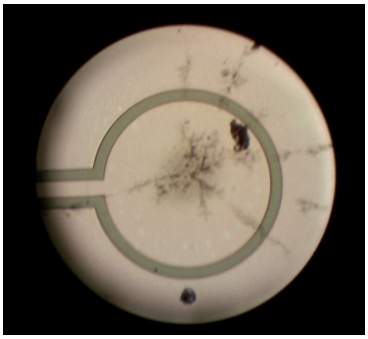
was very stable at a value of 14 kΩ. Power dissipation for a hotspot of about 40 µm is 30 mW, which is equivalent to 6 µW µm^{-2}, as compared to 0.95 µW µm^{-2} used in the full-membrane area simulations.

5.5.3. MODE 2 - CONTAMINATION PREVENTION

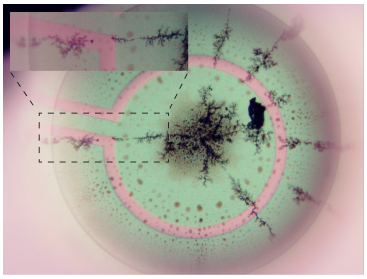
After successfully restoring local transparency at hotspot locations by soot oxidation, the effect of thermophoretic repulsion as an approach for contamination prevention (mode 2 operation) was investigated. The deposition of soot to the non-heated windows is based on diffusion and Van der Waals forces acting on the soot particles. The comparison of the heated and non-heated windows after soot exposure for several hours will function as qualitative results on the working of thermophoresis to keep the windows clean. The cast setting equals program 2, corresponding to a mean particle size of 80 nm, as was also used for the regeneration experiments. The temperature of the gas was equal to standard room temperature. Pictures before the experiment were taken to account for any residues and particles already present on the membranes due to packaging and transportation.

The thermophoretic repulsion is initially tested by comparing membranes M10 and M12, which both have a diameter of 1000 µm but featuring a different heater design. The flow rate used for this measurement is set to 0.1 L min^{-1}, translating to a lateral flow of 20 mm s^{-1}. The entire die was exposed to the soot-rich gas for a total exposure time of 94 900 s. From this exposure time, only 14 hours were done with the adjusted flow rate which enabled soot deposition. The heated 1000 µm membrane was biased with a fixed current, resulting in a membrane temperature of 70 °C.

After the exposure, microscope inspection was performed from the frontside while using backlight, thereby inspecting any deposition through the transparent membrane. Images were taken from both the heated as the non-heated 1000 µm membranes and a comparison is included in Figure 5.26. It can be concluded from this result that even



(a) Soot deposited on the unheated 500 µm membrane function as reference after 94 900 s, note that these picture are taken from the frontside of the die, thus the soot is inspected through the membrane.



(b) Deposited soot after on the backside of 500 µm membrane after 94 900 s exposure including zoom-in. Note the grown typical soot dendrites and the focal plane being way below the surface of the BS of the substrate. Note further that some brown circular residues are visible from the dicing process.

Figure 5.27: Membrane inspection after the first thermophoresis experiment.

the relatively small temperature difference of 40 °C of the membrane with respect to the temperature of the exposed gas, results in a convincing difference in the amount of deposited soot. The unheated membrane shows a significant amount of deposited soot, while no soot contamination could be seen on the heated membrane. It can further be noticed that most soot is deposited in the center of the non-heated membrane, while there is a ring shaped area where the window stay clear. This could be explained by the flow behavior of the gas relating to the high aspect ratio of the structure.

On the same die, the 500 µm membrane was not heated during exposure and a microscope picture is included in Figure 5.27a. The known dendritic behavior of soot deposition is indicated by this image, which functions further as unheated reference membrane that supports the working of the thermophoretic repulsion. Inspection from the backside was performed subsequently, using an optical microscope and both front- and backlight illumination. The result of the 500 µm membrane is included in Figure 5.27b. The shape of the grown soot dendrites can clearly be distinguished, which indicates that the soot is indeed deposited in a realistic scenario. Further it can be seen that the focal plane is below the surface of the backside of the die.

A second experiment was carried out to further investigate the contamination prevention by thermophoretic repulsion. Again the 1000 µm wide membranes M10 (heated) and M12 (unheated) were used, but from a different die as during the first experiment. To verify the biasing conditions of the heater, the temperature profile of the membrane was measured using the IR camera and SMU. The result is in correspondence with the calibration measurements carried out as included in Section 5.4.2.

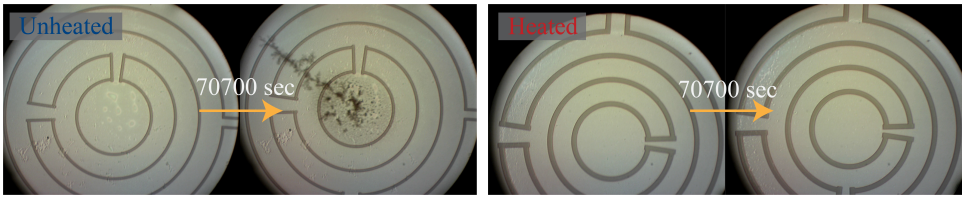
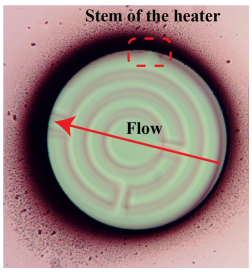
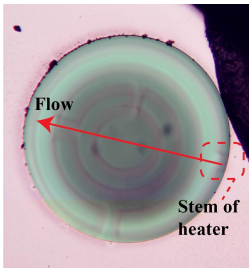


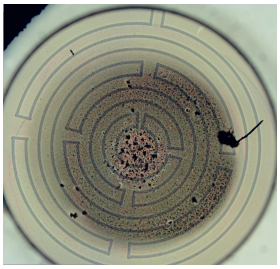
Figure 5.28: Contamination prevention by using thermophoretic repulsion on membranes M10 (right) and M12 (left). The microscope images indicate that the heated 1000 µm membrane stays transparant after constant exposure to a soot rich gas flow over a period of 70700 s, in contrast to the unheated 1000 µm. Soot deposition can be clearly distinguished on the backside of the unheated membrane and a large soot dendrite has formed.



(a) Heated 1000 µm diameter membrane (free of deposition). However, significant soot deposition has occurred around the cavity opening.



(b) Unheated 1000 µm diameter membrane (deposition on the membrane) and somewhat reduced deposition on the cavity edge as compared to the heated case.



(c) Deposited soot on the unheated M1 after the second contamination prevention experiment.

Figure 5.29: Post exposure backside inspections (focal plane on the substrate) after the second thermophoresis experiment.

Membranes M10 (heated) and M12 (unheated) were used to have two equally sized membranes for comparing the effect of the thermal gradient between the membrane and the used soot-rich gas. Figure 5.28 (left) show the images taken from the unheated membrane at t=0 s and t=70700 s respectively. Aerosol flow was 100 cm min^{-3} and soot concentration was between 10 mg m^{-3} to 12 mg m^{-3} to exaggerate the amount of soot and be have increased deposition on the windows which are not heated. During the exposure time, pictures were taken at fixed intervals, which enable data processing later. The heater was powered such that the resistance equals 30 kΩ, which corresponds to membrane temperature of 63 °C at the stem of the heater and 51 °C at the other end of the heater. Figure 5.28 (right) show the images taken from the heated membrane at t=0 s and t=70700 s respectively. As can be concluded from these images, the heated membrane stays clear from soot deposition in case of a temperature gradient between the membrane and the soot-rich gas of around 35 °C. Although this temperature gradient is

rather small, it is shown to be sufficient for an effective repulsion of soot.

Closer inspection by optical microscopy of the backside of the structure, as shown in Figure 5.29a, reveals a significantly higher amount of soot deposition downstream the soot-containing gas flow and near the heated membrane opening. This effect is most likely the result of turbulence at the ridges of the etched gap and is not related to the thermophoretic repulsion. Note that the combined thickness of the wafer and PCB results in a recess of about 2 mm at the membrane position that extends perpendicularly to the flow direction, resulting in a turbulent flow close to the window. The reduced local flow velocity at passage of the gap is likely to result in an increased downstream particle deposition.

5.6. Conclusion

The SiC MEMS optical membranes fabricated in this work provide preliminary validation of their suitability as transparent MEMS platform with a view into the soot-containing exhaust gas. Restoring window transparency by heating at about 600 °C (mode 1 operation) has been essentially demonstrated. Although mode 1 operation was limited to small hotspots, the results show effective removal of soot from the window, thus restoring its transparency. Moreover, thermophoresis for maintaining a transparent window (mode 2 operation) has been demonstrated for heating to 35 °C above the soot-containing gas temperature. High temperature survivability was shown by the regeneration tests, where no permanent material change was observed, nor shifts in the device performance from an electrical or mechanical point of view. Elipsometry measurements and subsequent model fitting were performed to derive the n,k values of the used poly-SiC, verifying the favorable optical properties.

Surface regeneration was demonstrated by oxidation of severe soot contamination by impacted soot. Regeneration was achieved for a hotspot area of about 1000 μm^2 in less than 5 minutes, without any permanent damage or deformation to the membrane. Power dissipation for a hotspot of about 40 µm is 30 µW, which is equivalent to 6 $\mu W\,\mu m^{-2}$, as compared to 0.95 $\mu W\,\mu m^{-2}$ used in the simulations. The difference is mainly due to the small spot diameter, an improved agreement in case of full-membrane heating is expected. Visual inspection showed that transparency was restored after the regeneration. The occurrence of hotspots during deposition implies that a dielectric isolation layer between the membrane and heater poly-SiC layers is required for a larger and more homogeneously heated membrane.

Multiple facets of the poly-SiC windows still need to be investigated, before this concept can be introduced as platform for optical instrumentation in the tailpipe of ICE

powered vehicles. Future work includes the assessment of the mechanical robustness and chemical inertness of the poly-SiC membranes in an industrial measurement setup and high-temperature packaging of the device. Also the effectiveness of thermophoretic repulsion with increased temperature should be validated over a range of temperature differences. To make sure that the membrane temperature is sufficiently elevated for effective thermophoretic repulsion in all gas temperature conditions, a co-integrated temperature sensor would be desirable. This can be implemented by designing a poly-SiC thermistor on the membrane. Finally, the optical properties of the poly-SiC membrane, such as the spectral transmission should be measured as function of membrane temperature.

The results of this Chapter matches with the third goal as described in Section 1.6. Optical particle sensors that can operate on a long term while having the contamination under control can be seen as one of the vacant harsh environment SiC sensors. The presented MEMS windows enable the development of an optical PM sensor for improved performance of automotive PM sensors. The presented SiC windows have furthermore potential for the development of optical instrumentation in other harsh environment applications.

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6

Silicon Carbide Surface Micromachined Pressure Sensors

In addition to the application of SiC in particle sensors, this Chapter focuses on the design and fabrication of surface micromachined pressure sensors, designed in a modular way for the integration with analog front-end read-out electronics. Poly-3C silicon carbide was used to fabricate free-standing high topography cavities exploiting surface micromaching. The poly-SiC was in-situ doped and the membrane itself is used as piezoresistive element, thereby forming a so-called self-sensing membrane, easing fabrication. After sacrificial release, the cavity is sealed by conformal deposition of poly-SiC whereby the reference pressure of the absolute pressure sensor is determined. Measurements were carried out ranging from $100\,\mathrm{kPa}$ *down to* $10\,\mathrm{Pa}$ *at room temperature. The Wheatstone bridge yields a logarithmic response of* $1.1\,\mathrm{mV\,bar^{-1}\,V^{-1}}$*. A square* $300\,\mu\mathrm{m}$ *device exhibits a logarithmic impedance behavior yielding a response of* $\Delta R/R$ *of* $1.6\times10^{-3}\,\mathrm{bar^{-1}}$*. Additionally, based on the developed process technology, microbridge-based poly-SiC Pirani gauges were realized and measured to operate from* $25\,^{\circ}\mathrm{C}$ *to* $750\,^{\circ}\mathrm{C}$ *with sensitivities ranging from* $6.42\,\Omega\,\mathrm{Pa^{-1}}$ *to* $1.1\,\Omega\,\mathrm{Pa^{-1}}$*. The realized pressure devices are a first step toward a SiC ASIC + MEMS platform for intended operation in harsh environments, such as industrial process monitoring, combustion control or structural health monitoring. The future outlook of the integration concept is extended functionality by front-end transducer read-out, signal amplification and communication.*

Parts of this chapter have been published in IEEE Sensors Journal (2020) [1] and [2].

6.1. INTRODUCTION

PRESSURE sensors are present in numerous applications, which makes them an ideal candidate to consider for monolithic integration with state-of-the-art SiC CMOS processes. Pressure sensors intended for harsh environments can for example be used for combustion monitoring to improve efficiency and reduce emissions of unwanted combustion products [3]. Additionally, they can be used to monitor pressures in geothermal wells and turbines [4, 5].

A pressure sensor which can be fabricated in such a modular way that it can be incorporated in the back-end-of-line (BEOL) part of a CMOS process run, would enable a platform on which the physical pressure transducer is monolithically integrated with the front-end CMOS read-out electronics. From a measurement system's perspective, it is highly desirable to have the read-out electronics, for example impedance read-out or signal amplification, as close as possible to the physical transducer, in order to minimize noise contributions originating from interconnect, EMI, or parasitic impedance. Another advantage of the integrated electronics is that the the read-out is performed directly in the electrical domain. Examples exist in literature where the read-out of membrane deflection is done using optical fibers [6]. Moreover, because of the inertness of silicon carbide, the usage of both a SiC sensing structure and SiC CMOS electronics relaxes the requirements on the packaging of bare dies.

Numerous pressure sensors intended for harsh environments have been reported in literature. Beker et al. [4] write on a surface micromachined circular concentrically matched capacitive pressure intended for measurements on geothermal wells. The substrate material used was silicon, but the structural layer is poly-crystalline SiC. Chen et al. [7] uses a poly-SiC substrate enabling an all-SiC device. Hung et al. [8] did a comparative study on both mono-crystalline and poly-crystalline SiC and concluded that the gauge factor in the case of a piezo-resistive pressure sensor implementation is significantly larger for 3C-SiC. Eickhoff et al. [9] used SOI substrates to isolate the different poly-SiC piezoresistive elements on the (silicon) membrane. Fonseca et. al [10] uses a rather classical approach to make their devices compatible with elevated temperatures, in this case 400 °C, namely the usage of ceramic materials. Fricke et al. [11] claim pressure sensor operation at 800 °C by making use of platinum strain gauges in a sapphire substrate. Jin et al. [12] write on the capacitive surface micromachined capacitive structures on a standard silicon substrate, resulting in a pressure sensor for in-cylinder pressure measurements on 574 °C. Lalinksy et al. [13] show an active device based pressure sensor, a high electron mobility transistor (HEMT) in AlGaN/GaN technology on a silicon substrate. Okojie et al. [14, 15] showed a fully-mono-crystalline-SiC implemen-

tation based on the piezoresistive effect. Thanks to full exploitation of the electronic and mechanical properties, the devices in these two works show operation up to 600 °C resp. 800 °C. Jiang et al. [6] described an optical pressure sensors based on an Fabry-Perot cavity. The read-out is done with an optical fiber to interface the harsh environment. Recently, Sun et al. [16] reported on an AlGaN/GaN HEMT based pressure sensor with a high sensitivity figure of 22.8%, which is however not constant for the entire measurement range. This work illustrates that advances in the field of WBG semiconductor sensors are still performed. Table 6.1 summarizes the literature on the various harsh environment compatible pressure sensors. One can conclude from this table that the majority of the harsh environment pressure sensors work with non-SiC substrate materials such as Si, SOI, Sapphire or another ceramic. In general, the high temperature compatibility of the silicon substrate based devices is compromised, except for the work of Jin et al., which uses a capacitive surface micromachined implementation and claims operation up to 574 °C. The three implementations based on 4H-SiC and 6H-SiC respectively do not describe the etching process or the way the membrane was fabricated or formed.

When focusing on the solely SiC based pressure sensors, it becomes clear that recent progress has been made in this field. Hoogerwerf et al. reports on a mono-crystalline based pressure sensor using a sealed reference cavity [23]. Despite the structure being fully crystalline silicon carbide based, the proposed design relies DRIE etching of crystalline SiC in combination with wafer bonding and is less suited for integration with SiC CMOS. Moreover results such an implementation in double the substrate costs.

A pressure sensor formed by laser scribing bulk 4H-SiC was reported by Nguyen et al. [24] resulting in a rather large required membrane area of 5 x 5 mm^2, due to the rough surface finish of such an ablation method. Although the electrical and mechanical properties of the crystalline SiC are fully exploited, the design relies on die-bonding with epoxy to a chip carrier in order to form an absolute pressure sensor. Also, from a miniaturization perspective, a membrane formed by laser scribing is undesirable, especially taking into account the high area cost of a SiC CMOS wafer.

Research into the piezo resistive properties of in-situ doped polycrystalline 3C-SiC was recently published by Phan et al. [25] and it was reported that gauge factors (GFs) up to -10 can be achieved [26], comparing to 20.8 for crystalline 4H-SiC [27]. Although the gauge factors which can be obtained by the usage of polycrystalline in-situ doped 3C-SiC are significantly lower compared to the mono-crystalline counterparts, the usage of polycrystalline has significant advantages, especially in the context of monolithic integration with SiC CMOS. Bulk micromachining of crystalline SiC can be performed, but is not trivial since it requires metal masking layers when depths exceeding several

Table 6.1: An overview of harsh environment pressure sensors in literature

Substrate	Transduction	Membrane thickness	Sensitivity	Pressure range	Temp.	Ref
Si	capacitive SiC-poly	2 µm circular R = 120 µm	1.03 fF kPa^{-1}	0 MPa to 1.4 MPa	180 °C	[4]
poly-SiC	capacitive SiC-poly	2.8 µm	272 μV/psi	5 MPa	574 °C	[7]
Si	piezoresistive poly&c SiC	15 µm	177 mV/V.psi	0.5 MPa	25 °C to 450 °C	[8]
SOI	piezoresisive 3C SiC (poly)	100 µm	3.5 mV/V.bar	0.35 MPa	200 °C	[9]
Ceramic	LC tank w. antenna	100 µm	-141 kHz/bar	10 MPa	400 °C	[10]
Sapphire	Pt strain gauges	200 µm	10 μV/V.bar	3 MPa	800 °C	[11]
Si	poly-SiC capacitive	2.7 µm	7,2 fF/psi	n.a.	574 °C	[17]
Si	AlGaN/GaN HEMT	1.9 µm	n.a.	1 MPa	n.a.	[13]
6H-SiC	Piezo resistive	50 µm, circular R=600 µm	32.5 μV/V.psi	1.4 MPa	600 °C	[14]
4H-SiC	Piezo resistive	50 µm	n.a.	1.38 MPa	800 °C	[15]
6H-SiC	Piezo resistive	n.a.	200 μV/bar	12 MPa	400 °C	[18]
Si	capacitive, mono-3C-SiC	0.5 µm, circular R = 400 µm	7.7 fF/torr	146 kPa to 235 kPa	400 °C	[19]
SiC wafer	Capacitive cavity	18 µm	10.6 kHz kPa^{-1}	200 kPa	600 °C	[20]
GaAs	Res.Tunnel Diode	1 µm	6 kHz kPa^{-1}	1 kiloPa to 50 kiloPa	RT	[21]
Si	piezoresistive 3C-SiC poly	30 µm	3.9 mV/psi	83 kPa	RT	[22]
SiC	SiC Fabry-Perot cavity	50 µm circular R=1.5 mm	n.a.	0.1 MPa to 0.9 MPa	RT	[6]
GaN	HEMT - ΔI_D	5 µm diameter = 700 µm	22.8% (non-linear)	0.01 kPa to 96 kPa	25 °C to 100 °C	[16]

µm's need to be etched, due to the otherwise poor selectivity [27–31]. The significant research interest in SiC and other wide bandgap materials is illustrated by a novel opto-electronic coupling mechanism that was recently reported by Nguyen et al. [32, 33]. This coupling mechanism is used to boost the gauge factor by using illumination of SiC, thereby generating a gradient of charge carriers. The same effect is exploited by Li et al. in the application of 3C-SiC nanowires which are illuminated with UV-light to enhance piezoresistive behavior [34]. These works illustrate the importance of further investigation of novel concepts of piezoresistive materials and sensors.

Using thin-film polycrystalline 3C-SiC omits the need for the rather complex bulk mi-

cromachining. Moreover, the process flow can be designed such that it fits in the back-end processing of a SiC CMOS technology, and that the sensor can be fabricated on different types of substrates, enabling prototyping on well-available and cheaper silicon substrates. In the latter case, the influence on the mechanical design of the different coefficients of thermal expansion (CTEs) need to be taken into account. Surface micromachining thin-films results in a higher degree of design flexibility, since membrane dimensions can be chosen freely regardless of the substrate thickness. Moreover, because the formation of an absolute pressure sensor based on a reference pressure inside a sealed cavity is more easily achieved in a surface micro machined, thin-film based solution.

Capacitive surface micro machined pressure sensors exploiting poly-SiC are reported in literature. Beker et al. realized a surface micro machined capacitive pressure sensor featuring a cavity with a reference pressure from polycrystalline SiC. However, operation up to only 180 °C was demonstrated [4]. Chen and Mehgregany have realized a capacitive surface micromachined pressure sensor showing operation up to 574 °C for in-cylinder measurements [35]. The disadvantage of specifically capacitive surface micromachined pressure sensors is that a second electrode is needed for the actual capacitor, requiring additional processing steps in the back-end module and hindering integration ability with SiC CMOS. Piezoresistive pressure sensors using poly 3C-SiC have been fabricated by Chien-Hung et al. [8], but the design proposed relies on bulk etching of silicon substrates, which is undesired for the scope of this work.

Phan et al. used thin-film SiC for the fabrication of a suspended membrane of only 200 nm, forming a pressure sensor [36]. The layer was interfaced using nickel electrodes and its n-type doping concentration was 1×10^{16} cm^{-3}. A unique property of this device was that no separate piezo resistors were designed to transduce the stress in the membrane to the electrical domain. Although the device described in this work was fabricated on silicon substrates and relies on bulk etching of this substrate, the concept of a self-sensing membrane eases fabrication significantly, since it reduces the number of processing steps. This concept will be applied in this work to a pressure sensor which is fully surface micro machined, omitting the need for bulk etching and while maintaining the advantages of using poly-SiC.

Therefore, the goal of this paper is to develop a modular pressure sensor that can be integrated monolithically with SiC CMOS based on 4H-SiC substrates, as schematically illustrated by Figure 6.1. This means that the fabrication of the device must fit inside the back-end fabrication of a SiC CMOS technology, implying challenges regarding thermal budget, contamination and metallization. In order to comply with this goal, this work

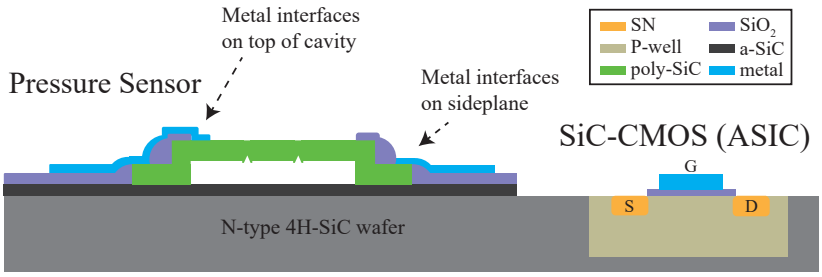


Figure 6.1: A conceptual representation of the possible monolithic integration of the designed MEMS pressure sensor with SiC-CMOS.

will focus on the usage of intrinsic and in-situ doped n-type polycrystalline thin-film 3C-SiC. Besides, the concept of a self-sensing membrane will be investigated. The high degree of modularity is a third important starting point of the design. By varying the membrane thickness, shape, length, width and the dopant concentration of the membrane layer freely, the device can be tailored to specific device performance related to different applications.

6.1.1. APPLICATIONS

The aim is to develop the pressure devices in a modular way, that it the design can be tailored to a specific application. Applications for harsh environment pressure sensors are for example combustion monitoring in internal combustion engines (ICE) in automotive and heavy duty vehicles [35]. Stringent regulations on the emission of pollutants and fuel economy results in more elaborated combustion control [37]. The combustion control is required due to varying intake air qualities, deviations in the fuel used, aging and wear of components of the engine [38, 39]. In-cylinder pressure monitoring could enable direct monitoring of the combustion process, thereby compensating for variations between cylinders and allowing for a better overall combustion efficiency. The in-cylinder environment can be seen as harsh, high pressures are combined with high temperatures, corrosive species and vibrations [40]. Combustion monitoring and control is also important in gas turbine engines (aviation) and rocket engines (space) [5, 41]. Harsh environment pressure sensing can be applied in the oil industry, where pressure sensors are used for monitoring the conditions in and/or around oil reservoirs [41, 42]. The environment in oil wells is typically harsh because of the elevated temperature and the presence of corrosive species such as dissolved salts. An overview of different application fields is given in Table 6.2 and in Figure 6.2.

Table 6.2: Some application fields for harsh environment pressure sensors with the corresponding pressure- and temperature range.

Field	Pressure	Temperature
Medical	69 mbar [17]	50 °C
Oil wells	35 bar	250 °C [42]
Combustion engine	0 bar to 100 bar [17, 43]	574 °C [43]; 200 °C to 450 °C [3]
Geothermal wells	14 bar [4]	350 °C [5]
Gas turbine engines	1 bar to 100 bar[35, 44]	−50 °C to 650 °C [3, 5, 17]
Industrial gas turbines	345 bar	450 °C to 600 °C [17]



Figure 6.2: An overview of the pressure sensor market. Source: [45].

6.2. DESIGN

The design is based on a surface micromachined sealed cavity created by a suspended membrane made of polycrystalline 3C-SiC layers. In order to come to this design, different design options were considered, as is summarized in Appendix A. The polycrystalline SiC will be deposited by using a low pressure chemical vapor deposition (LPCVD) furnace. The cavity holds a reference pressure inside which is created during the sealing process of the released membrane and after the removal of the sacrificial layer. The membrane consists of a stack of an intrinsic poly-SiC layer and a piezo resistive in-situ n-type doped poly-SiC layer. The piezo resistive layer will directly be used to transduce the pressure-induced strain of the membrane into a resistance variation. Electrodes will be patterned directly on top of the cavity, enabling four point resistance measurements. A schematic drawing of the proposed design is displayed in Figure 6.3.

6.2.1. ANALYTICAL DEVICE MODELING

The design of the device is bounded by cleanroom fabrication feasibility aspects, such as the maximum poly-SiC layer thickness of 5 µm due to the deposition process. The theory

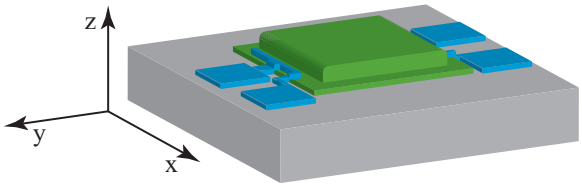


Figure 6.3: A schematic drawing of the design of the pressure sensor.

of Meleschenko [50] can be used to link a uniform pressure on a square membrane to the maximum deflection (typically in the center in the case of a square membrane), as described by equation (6.1).

$$P = E\frac{h^4}{a^4}[g_1\frac{w_0}{h} + g_2(\frac{w_0}{h})^3] \tag{6.1}$$

In which, P is the pressure in [Pa], E the Young's modulus, h the thickness of the membrane in [m], a half of the width ($2a$ = membrane width), w_0 the maximum deflection of the membrane in [m], and g_1 and g_2 are constants that include the Poisson ratio ν. Using 0.168 for the Poisson ratio of poly-SiC, g_1 and g_2 can be determined:

$$g_1 = \frac{4.13}{(1-\nu^2)} = 4.25 \tag{6.2}$$

$$g_2 = \frac{1.98(1-0.585\nu)}{(1-\nu)} = 2.15 \tag{6.3}$$

Using equation (6.1), it can be seen that the pressure is linearly linked to the maximum deflection w_0 as long as the first term within the square brackets is much smaller than the second term, which is the third power of the ratio between the maximum deflection and thickness of the membrane. As reported in literature [22, 51], to satisfy this condition typically a value of 0.2 is employed for the w_0/h ratio. This would allow the second term to be only 4% of the first term, thus ensuring a linear dependence between the pressure and the maximum deflection. In this case the maximum deflection would be equivalent to the 20% of the membrane thickness at most. Using equation (6.1) for a membrane thickness of 2.7 µm and a membrane width of $2a$ = 300 µm results in a maximum pressure for linear deflection of 39.14 kPa with a corresponding deflection of 540 nm. The maximum stress which occurs at the center of the edge of a square membrane (x=+/-a) is given by equation (6.4). Based on this equation, the maximum pressure for linear deflection results in a maximum stress of 1.21×10^8 N m^{-2}. When a pressure of 100 kPa is considered, the maximum stress by equation (6.4) is 3.08×10^8 N m^{-2}.

Table 6.3: Design parameters.

Symbol	Quantity	Value
E	Young's modulus	430 GPa [52]
ν	Poisson ratio	0.168
w_0/h	Linearity constraint	0.2
2a	Membrane width	300 µm
h	Membrane thickness	2.7 µm
σ_c	Critical stress	3.16 GPa [53]
ρ	Density LPCVD SiC	3.18 kg m^{-3} [54]

$$\sigma_{max} = P(\frac{a}{h})^2 \tag{6.4}$$

In harsh environments, a relevant parameter is the pressure beyond which yielding starts to occur, also called burst pressure, which is determined by the critical stress σ_c and given by equation (6.5).

$$P_B = \frac{\sigma_c}{(\frac{a}{h})^2} \tag{6.5}$$

By substituting the design parameters as summarized in Table 6.3 in equation (6.5), a burst pressure of 1.02 MPa is obtained. This in the case of a free standing membrane where the deflection is not limited by the cavity height. The resonance frequency of the membrane should be considered for applications where the dynamic behavior is of importance. This frequency can be expected to be high, thanks to the high stiffness of the used polycrystalline SiC material and the relatively low mass of the membrane itself. The resonance frequency is given by equation (6.6).

$$f_r = 1.65\frac{h}{a^2}\sqrt{\frac{E(1-\nu^2)}{\rho}} \tag{6.6}$$

which gives a resonance frequency of 79 MHz.

6.2.2. FINITE ELEMENT MODELING

Based on the proposed design, finite element analysis (FEA) was performed using COMSOL. The poly-3C-SiC material was defined from a blank material. The piezoresistive coupling matrix relates the mechanical stress σ to a change in resistivity $\frac{\Delta\rho}{\rho}$ as expressed by equation (6.7) [25]. Note that for a polycrystalline material, as used in this work, the piezoresistive coupling matrix can be simplified to a scalar, since the piezoresistive properties are not dependent on the directions of the crystal, resulting is an isotropic piezoresistive coupling coefficient.

Table 6.4: Simulation parameters.

Quantity	Value
Membrane width	300 µm
Membrane thickness	2.7 µm
Contact thickness	1 µm
Contact length	180 µm
Contact width	2 µm
Reference pressure	20 Pa
Piezoresistive coupling coefficient	-2.33×10^{-11} Pa^{-1}
Residual stress	487 MPa

$$\frac{\Delta\rho}{\rho} = \pi\sigma \tag{6.7}$$

The gauge factor is linked to the piezo resistive coupling value via the Young's Modulus as described by equation (6.8).

$$GF = E\pi \tag{6.8}$$

In which E is the Young's modulus. From literature it can be concluded that the highest gauge factors are obtained for a target bulk resistivity of polycrystalline 3C-SiC of approximately 0.1 Ωcm [25, 26]. Considering a gauge factor of -10, a piezoresistive coupling value of -2.33×10^{-11} Pa^{-1} is obtained. COMSOL expects a piezo resistive coupling value which is multiplied with the bulk resistivity. The piezoresistive coupling coefficient equals then -2.33×10^{-14} Ω m Pa^{-1}, which equals -2.33×10^{-14} m^4 s^{-1} A^{-2} in SI-units. The cavity will be sealed at 80 Pa and 860 °C. Applying gas laws of Gay-Lussac and under the assumption of constant volume , a value of about 20 Pa is obtained when the cavity is at 25 °C. Other simulation parameters used are reported in Table 6.4.
Although the geometry can be varied freely within the process boundary conditions, a square membrane with a side length of 300 µm with a thickness of 2.7 µm was modeled. Because the membrane itself is used as piezo resistive sensing element, the dimensions and positioning of the electrodes is largely influencing the sensitivity of the device. The length of the electrodes was designed such that they align with the regions of maximum stress. Two design options are considered, one where the electrodes are deposited directly on top of the membrane and one where the electrode is formed on the 'sideplane', right next to the cavity. For sensitivity reasons, the first option is highly preferred, but requires the metal to be deposited over one additional flank. Both design options are illustrated in Figure 6.1, the electrode on top of the cavity and on the side plane on the left and right side respectively. In the simulation, the electrodes positioned directly on top of the cavity are considered. A line of symmetry was added to reduce computational

load. Aluminum was chosen as material for the electrodes, while the membrane itself is based on the poly-SiC.

The reference pressure inside the cavity was modeled by applying a boundary load on the bottom of the membrane, while the simulated pressure was applied by a boundary load on the outside of the cavity, thereby yielding a pressure difference. Fixed constraints were used to bound the device as if it would be processed on a wafer. Additionally, a boundary load was applied to the membrane to account for the residual stress in the poly-SiC which was characterized during fabrication. A parametric sweep was used to investigate the membrane response in which the pressure was swept from 10 Pa to 100 kPa. The y- and z-components of the stress tensor at the maximum pressure of 100 kPa is included in Figure 6.4, from which it can be seen that the electrodes match the regions of maximum stress. As expected, due to the uniformly applied pressure and to the small thickness of the layer the stress in the z-direction is uniform.

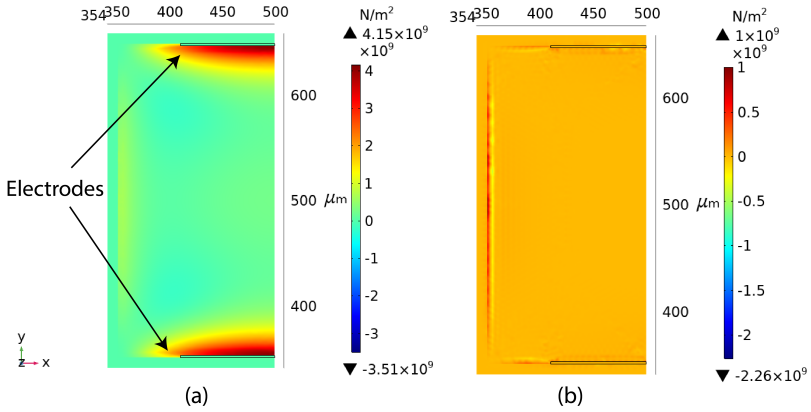


Figure 6.4: (a) The stress tensor in y-direction at 100 kPa; (b) The stress tensor in z-direction at 100 kPa.

The simulated displacement in the minus z-direction with an applied pressure of 100 kPa equals 1.2 µm whereas the simulated deflection at 39.15 kPa (that is the maximum pressure for linear deflection) equals 540 nm, which is equal to the analytical derivation. The piezoresistive multi-physics module was used to study the piezoresistive response of the membrane. $\frac{\Delta R}{R}$ was determined by using the base resistance at zero pressure difference (P=20 Pa) and plotted against the swept pressure using a logarithmic x-axis, as shown in Figure 6.5. The simulations reveal that $\frac{\Delta R}{R}$ is a logarithmic function of pressure from approximately 30 kPa. When the gauge factor is calculated back based on the derived volumetric strain, the gauge factor of -10 is obtained, verifying the simulation.

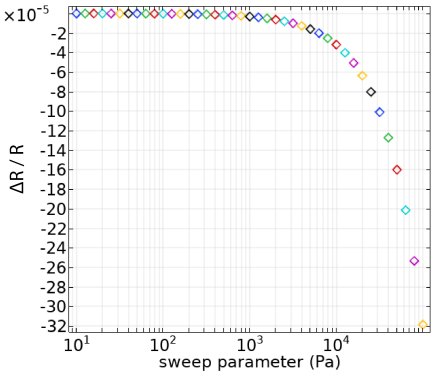
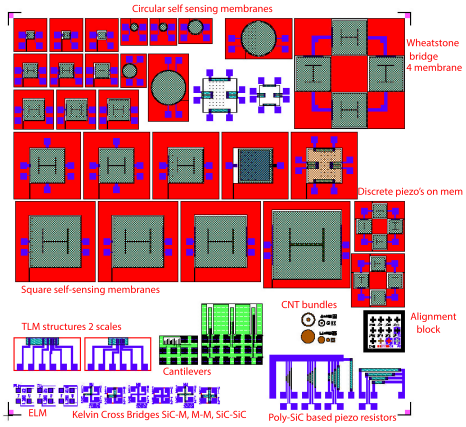


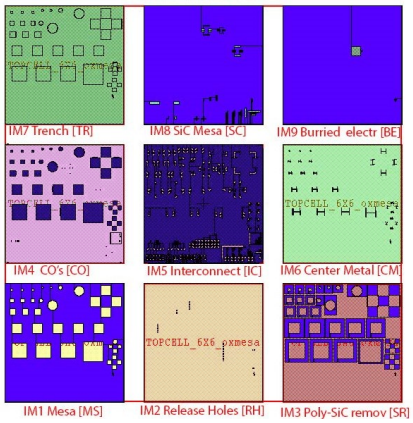
Figure 6.5: $\frac{\Delta R}{R}$ as function of the swept pressure to investigate the piezo resistive behavior.

6.2.3. MASK DESIGN

A mask design was designed based on a die size of 6 x 6 mm. An overview of the nine mask images is included in Table B.2 in Appendix B. Six images are required for the fabrication of the cavity based pressure sensor, while the other three were dedicated to test structures and options to modify the process to yield a modified design. Test structures considered are for example Kelvin Cross Bridges (KCBs) to characterize the ohmic behavior the metal-semiconductor contacts.



(a) The designed mask with the different pressure devices.



(b) An overview of the 11 layers on the oxmesa reticle.

Figure 6.6: The combined and separated layers of the oxmesa reticle.

Square pressure cavities having widths of 100 µm, 200 µm, 300 µm, 500 µm, 750 µm and 1000 µm were designed, each with an electrode width of 5 µm and 10 µm, thereby en-

abling a more conservative interconnect approach and an electrode design optimized for maximum sensitivity. Additionally, circular membranes were designed with diameters of 100 µm, 200 µm and 500 µm with 7 µm wide electrodes have been designed. For every pressure cavity design, both a version with electrodes on the cover of the cavity and electrodes on the side plane have been designed, in order to minimize the risk of non-continuous metal deposition due to the step height of the cavity. Based on the 500 µm and 200 µm square cavities, half Wheatstone bridges have been designed. The length of the electrodes is matching the region of maximum stress to maximize the piezoresistive response, which was determined by FEM simulations. An optional 'center metal' layer was included in the mask design to increase $\frac{\Delta R}{R}$, but was not used in this work. An overview of the topcell of the mask design is included in Figure 6.6a.

6.3. FABRICATION

6.3.1. POLY-SIC LAYER CHARACTERIZATION

The silicon carbide considered is polycrystalline 3C SiC which is deposited by Low Pressure Chemical Vapor Deposition (LPCVD). Because of the uncertainty that the grain boundaries bring, and the sensitivity to unintentional doping by any residual Nitrogen, the layers based on the known recipes need to be extensively characterized. Even more, since the reproducibility and batch homogeneity were never developed for the available poly-SiC recipe. Starting point of for the depositions are the work carried out by Morana [55, 56].

Thickness determination Because of the polycrystalline structure, the usage of the Leitz spectrophotometer to determine the thickness of the deposited layers is not feasible. The thickness was determined by depositing the poly-SiC layers on wafers with silicon oxide below. This oxide may be PECVD (Novellus) or thermal. After deposition of poly-SiC, the wafers are coated with a thicker (at least 3 µm) resist layer and any mask with large enough openings can be exposed. The openings should be large enough that the stylus of the Dektak Stylus profiler can go through. After exposure the poly-SiC layer is etched while landing on the underlying silicon dioxide layer. To verify if the etching of the poly-SiC layer landed on the oxide, the oxide thickness can be measured inside the openings. When this value is lower than before the poly-SiC deposition, the etching time is sufficient. The oxide in the openings is etched away using 1:7 BHF. Thanks to the thermal step at 860 °C PECVD oxide undergoes a densification, significantly reducing the etch rate. After the oxide has been etched away in the openings, the stepheight can be measured again. Subtracting the known oxide layer thickness yields the poly-

SiC layer thickness. Optional additional intermediate stepheight measurements can be applied to determine the etch rate and selectivity with respect to photoresist for the development for dry SiC etch recipes.

Resistivity determination The resistivity of the layers is characterized by using a Resmap 4 point measurement tool. The measured wafer must have an oxide layer below the carbide layer to isolate the conducting silicon substrate from the poly-SiC layer on top. This oxide may be PECVD or thermal oxide. Typically, a layer thickness of 500 nm or 1 µm is used. This measurements yield sheet resistance values which are converted to resistivity values by multiplying with the layer thickness, typically in cm.

$$\rho = R_{sheet} \cdot t \tag{6.9}$$

Table 6.5: Measured resistivities, residual stresses and deposition rates for different poly-SiC layers. Note that the layers indicated with I are non-intentially doped (intrinsic). A negative residual stress value indicates compressive stress.

Layer ID	Resistivity	Res. stress	Dep. rate
D-1	0.0984 Ω cm to 0.1126 Ω cm	314 MPa	7.2 nm min^{-1}
D-4	3.37×10^{-3} Ω cm	503 MPa	10.71 nm min^{-1}
I-6	439.8 Ω cm	65.0 MPa	12.22 nm min^{-1}

Stress determination Note that a negative value for the measured stress means a compressive stress, where the molecules of the film are pushing/pressing against each other. This results in a negative bow of the wafer, where the center of the wafer will be 'elevated'. For the formation of membranes, it is desired to use layers having tensile stress, in which grains are pulled away from each other. The wafer will get a positive bow in this case, where the edges of the wafer is elevated. The stress is determined by deposited poly-SiC layers on bare Si wafers, thus without any oxide or dielectric layer. These wafers undergo a 'zero' or reference measurement before the poly-SiC layer is deposited. It is important to monitor the stress of the wafers during the process because this influences the specifications and behavior of the resulting membranes. The stress measurements will be carried out before deposition of amorphous SiC with the Flexus 2320S. Before the stress measurements can be performed, the backside of the wafers need to be etched clean from conformally deposited poly-SiC. The characterization data on the deposition rate, the resistivity and the residual stress is included in Table 6.5.

6.3.2. FOCUS OFFSET ON HIGH TOPOGRAPHY STRUCTURES

Since the wafers considered in this project exploit high topography structures (mesas covered with poly) the focus offset needs need to be set correctly. Especially because the resist layers used have significant thickness, > 4 µm, to be able to etch through the poly. A negative focus offset will lay the focus point to a higher point with respect to the wafer surface. A less negative value means thus that the focus point is deeper into the PR in this case. As a rule of thumb the focus point should be in the center of the photoresist, in case a thicker photoresist is used.

$$\text{focus offset} = \frac{th_{PR}}{2} - \Delta_{height} \tag{6.10}$$

Because the locations where the height leveling sensor of the stepper takes its values, and the post processing of these value are not fully known, some deviation from the rule-of-thumb 6.10 should be accounted for. See examples below.

- 5 µm cavity, 3.1 µm PR: focus offset = $\frac{th_{PR}}{2} - \Delta_{height}$ = 1.5 - 5 = −3.5 µm
- 5 µm cavity, 6 µm XT PR: focus offset = $\frac{th_{PR}}{2} - \Delta_{height}$ = 2.5 - 5 = −2.5 µm
- 7 µm cavity, 10 µm XT PR: focus offset = $\frac{th_{PR}}{2} - \Delta_{height}$ = 5 - 7 = −2 µm

6.3.3. FEASIBILITY SiN SEALING

Initially, furnace E4 for poly-SiC deposition was unavailable for the second sealing step. To still be able to experiment with the concept of sealing of the release holes at LPCVD under pressure, furnace E2 was used for the deposition of 2 µm silicon nitride. This thickness was chosen based on the measured size of the etched release holes. A total membrane thickness of 3 µm is yielded. The total deposition time to yield the 2 µm layer equals 270 min using recipe '4INCHST'.

To inspect cross sections of the cavities, it was decided to saw the wafers in four pieces, while cutting through the cavities. This was carried out for wafer P1 and P3, thus the unsealed and sealed cavities. The wafers were stuck on the standard dicing foil compatible with the dicing tool. A maximum rotational saw speed was used, while using smallest sawing speed through the wafer. An optical microscope picture of a diced cavity is included in Figure 6.7. Clearly visible is the SiN layer on top, the amorphous silicon carbide layer and the opened cavity with part of the sidewalls and cover still present. Note that the structural layer of the cavity consists of 700 nm poly-SiC and 2 µm of silicon nitride.

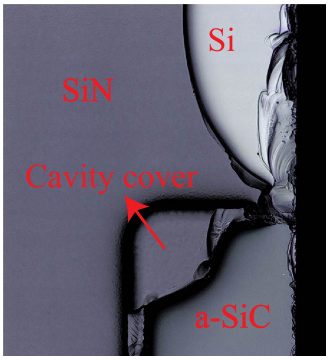


Figure 6.7: A microscope picture of a diced cavity.

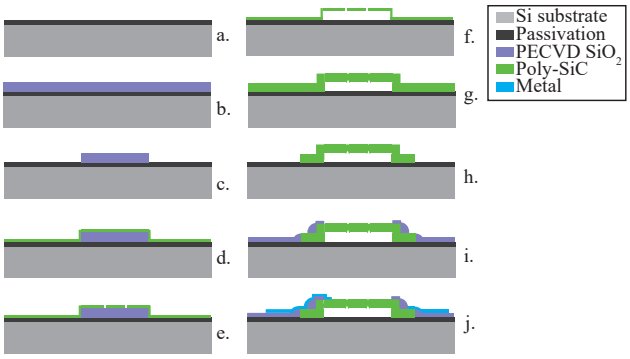
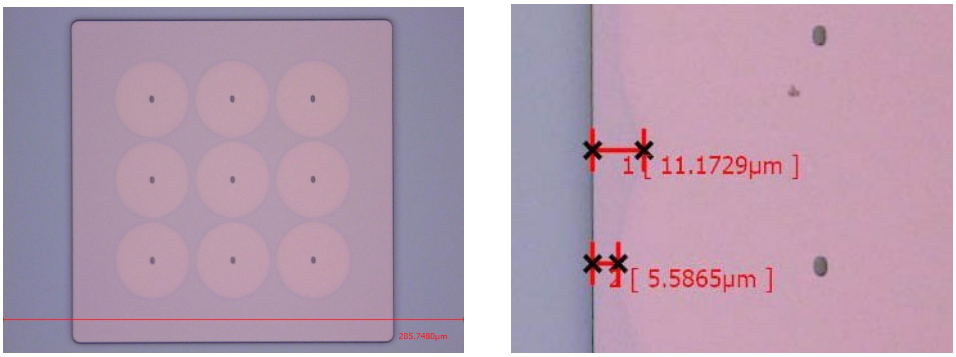


Figure 6.8: The process flow used during fabrication.

6.3.4. ALL-SIC DEVICE FABRICATION

A schematic illustration of the process flow is reported in Figure 6.8. A layer of low-stress amorphous SiC with a thickness of 720 nm was deposited by plasma enhanced chemical vapor deposition (PECVD), this served to electrically isolate the device from the silicon substrate (Figure 6.8a). Furthermore functions this layer as etch barrier during the sacrificial etch. The bulk electrical resistance of the amorphous SiC layer is in the order of MΩcm. Subsequently, a layer of 2.5 µm SiO_2 was deposited by PECVD from which the mesa structures will be formed (Figure 6.8b). By using a photoresist (PR) layer of 4.0 µm lithography of the mesa structures was performed, subsequently they were etched by using a standard SiO_2 plasma etch recipe in a RIE etchter (Figure 6.8c).

After the mesas have been patterned, the first intrinsic poly-SiC layer of 700 nm was deposited by LPCVD. Dichlorosilane (SiH_2Cl_2) and acetylene (C_2H_2) were used as precursor gasses with flow rates of 123 sccm and 18.85 sccm, respectively in a hot-wall LPCVD furnace operating at a deposition temperature of 860 °C (Figure 6.8d). More information on the poly-SiC recipe used is given by Morana et al. [56]. With a four probe Kelvin sheet resistance measurement tool, the bulk resistivity of the intrinsic SiC layer was measured to be 439.8 Ωcm. Characterizations of the doped piezoresistive poly-SiC layer performed by using high resolution scanning electron microscope and atomic force microscopy revealed a grain size of 145±7 nm. Due to the high topography of the patterned structures, MicroChemicals 12XT-20PL10 chemically amplified PR was used to cover the entire cavities. A PR thickness was achieved of 7 µm by manual spin coating. The release holes are oval shaped and have a width of 2 µm and a length of 4 µm, the shape can be tuned by exposing the image with circular release holes multiple times with lateral offset steps. It is important that the width is maximum half the target thickness of the second SiC



(a) After the first vapor HF releasing step.

(b) After all vapor HF release steps, note the scalloped TEOS near the edge of the cavity.

Figure 6.9: Releasing the sacrificial material.

deposition in order to ensure sealing of the cavities. The release holes were etched in the instrinsic poly-SiC using a customly developed plasma etch recipe based on SF_6 and O_2 and performed at 0 °C in a DRIE etcher (Figure 6.8e). The sacrificial SiO_2 was etched by using vapor HF, the removal was step-wise monitored by optical microscope inspections. This was possible thanks to the optical transparency of the poly-SiC layer. This is shown in Figure 6.9a where circular shapes centered at release holes are clearly visible. These indicate the removal of the SiO_2 (Figure 6.8f).

A scanning electron microscope (SEM) image of the release hole after sacrificial etch is included in Figure 6.10 (left). After the sacrificial oxide was etched away completely, the second poly-SiC layer was deposited. This time, ammonia was added during the deposition as N-type dopant. This recipe used 80 sccm dichlorosilane (SiH_2Cl_2), 16 sccm and acetylene (C_2H_2) and 1.5 sccm ammonia (NH_3), targeting a bulk resistivity of 0.02 Ωcm. Although this bulk resistivity is lower than simulated, and than would be ideal for maximum gauge factors, this recipe was chosen to make sure that ohmic contact are formed for the initial experiment. In general a small to moderate tensile stress is desired for the realization of flat, non-buckled membranes. The residual stress was measured and found to be tensile with a magnitude of 487 MPa.

After the poly-SiC:N deposition, the total stack of 2.7 µm consisting of the intrinsic and doped poly-SiC layer around the cavities was etched, while landing in the isolating passivation layer. In order to minimize the area where parasitic currents through the intrinsic poly-SiC could occur, the 700 nm thick intrinsic poly-SiC layer was etched away, while landing on the isolating amorphous SiC. After patterning, the poly-SiC stack was etched using the same procedure as was used to etch the release holes (Figure 6.8h).

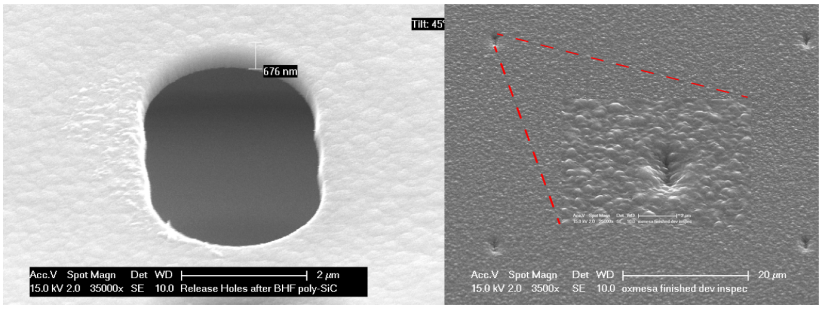


Figure 6.10: SEM images of the release hole: After sacrificial etch (left) and after sealing (right).

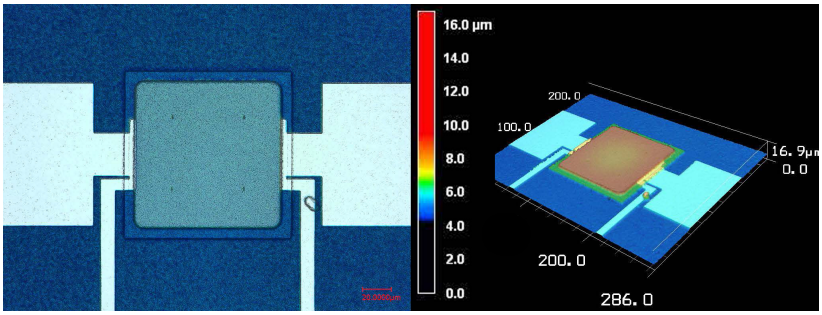


Figure 6.11: An optical microscope picture (left) and a height map (right) of a finalized 100 µm device.

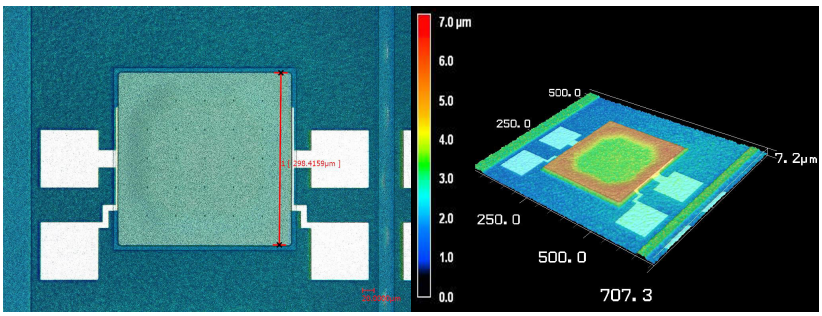


Figure 6.12: An optical microscope picture (left) and a height map (right) of a finalized 300 µm device.

To isolate and passivate the functional poly-SiC layer, a layer of SiO_2 of 500 nm was deposited on the wafers. This SiO_2 was etched at the locations of the electrodes and on top of the membrane. Otherwise, the SiO_2 layer would affect the mechanical properties of the poly-SiC stack (Figure 6.8i). In order to form the electrodes, metal traces and probe pads, 1000 nm of AlSi(1%) was sputtered at 350 °C. The AlSi(1%) was etched using a chlorine based recipe in an inductively coupled plasma (ICP) metal etcher (Figure 6.8j).

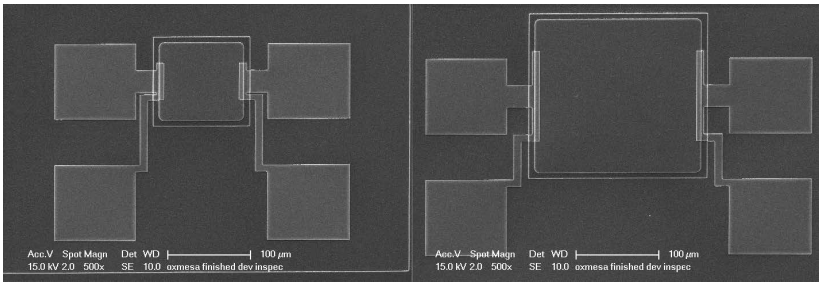


Figure 6.13: SEM images of the 100 µm and 200 µm square cavities.

The completed devices were inspected by a SEM and a Keyence VK-X250 3D laser scanning confocal microscope. Figure 6.11 shows an image of the optical inspection (left) with the height map (right), where the deflection towards the substrate by the atmospheric overpressure can be noticed. SEM images of the complete devices are included in Figure 6.13. The continuity of the metal traces over the step heights was inspected as indicated in Figure 6.14.

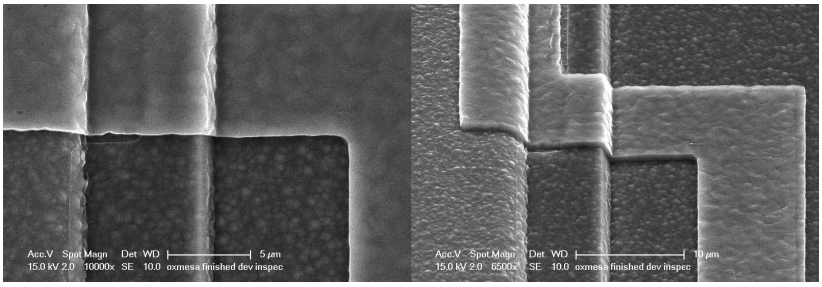


Figure 6.14: SEM images of the step coverage of the metal to cavity contact; without tilt (left), with a tilt of 45° (right).

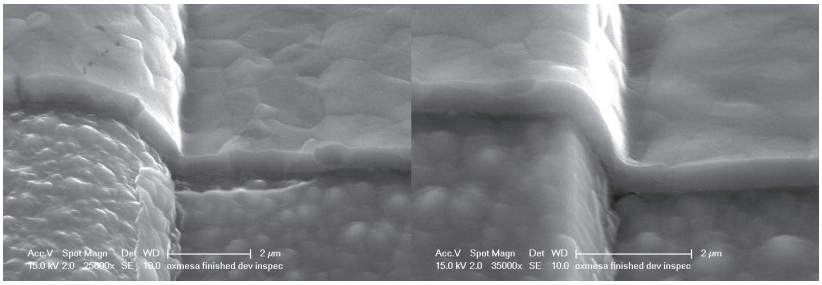


Figure 6.15: Zoom-in SEM images of the step coverage of the metal to cavity contact, stepping over the cavity (left) and from the poly-SiC layer back to substrate level (right).

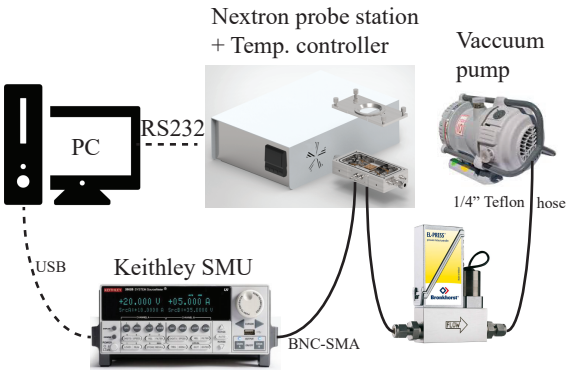


Figure 6.16: A schematic overview of the pressure measurement setup.

6.4. MEASUREMENTS AND CHARACTERIZATION

After cleanroom fabrication, the wafers were diced whereafter the pressure devices were characterized.

Pressure Setup The pressure setup consists of a Nextron MPS-CHH microprobe chamber with a ceramic chuck. This chamber can be pumped down, while electrical measurements can be carried out using four available probe needles with a 20 µm rhodium coated tip. The vacuum is arranged via a BocEdwards XDS-10 scroll pump connected to a Bronkhorst EL-PRESS pressure controller. This controls the pressure inside the chamber by adjusting the flow. The pressure controller houses a reference pressure sensor and is controlled using a personal computer (PC). The resistance of the pressure devices under test is measured using a Keithley 2612B source measurement unit (SMU) enabling a four probe Kelvin measurement. A schematic overview of the measurement setup is shown in Figure 6.16.

Single Device Initially the square-shaped membrane with 300 µm side length was measured. The membrane was biased with a constant voltage of 1 V, while the current over the force pair and the voltage over the sensing pair were measured using the SMU. Simultaneously, the microprobe station was pumped down from atmospheric pressure down to 10 Pa. The resistance- and pressure was measured using a sample rate of 1 sample /s and the entire measurement lasted for 131 s.
$\frac{\Delta R}{R}$ was determined by using the membrane resistance at 100 kPa as base resistance R and with $\Delta R = R_{measured} - R$. Figure 6.17 shows $\frac{\Delta R}{R}$ against absolute chamber pressure. Due to the high pump speed at the start of the pumpdown in this measurement,

the result is noisy between 1×10^4 Pa and 1×10^5 Pa. Based on this result it can be seen that the response starts to become unambiguous from 1×10^4 Pa and below, whereas the most sensitive region is between 1×10^2 Pa and 1×10^3 Pa, where the resistance response is logarithmic. The resistance vs. pressure behavior can be explained by the decreasing absolute pressure in the microprobe station, resulting in a smaller pressure difference ($P_{ref} \approx 20$ Pa). As a result of the reduced pressure difference, the strain and thus stress on the membrane is reduced. The measured increase in resistance of the membrane while reducing the strain on the membrane is in agreement with reported negative gauge factors for poly-SiC [25, 26].

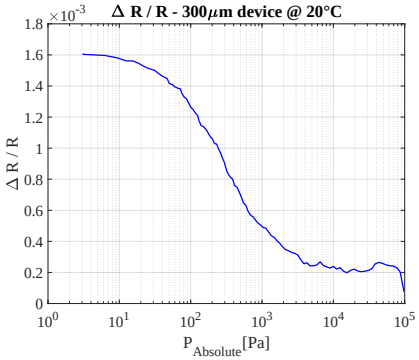


Figure 6.17: $\frac{\Delta R}{R}$ versus pressure in semi-logarithmic scale for the measured single square membrane of 300 µm. The base resistance was taken at the start of the pump down at 100 kPa.

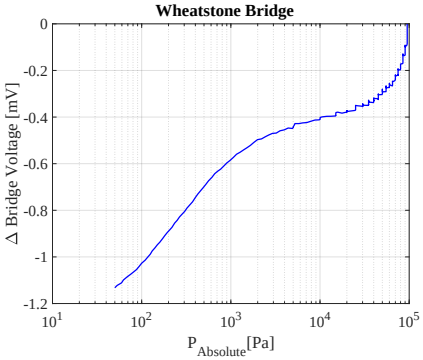


Figure 6.18: The normalized deviation in the bridge voltage as function of pressure.

The logarithmic behavior of $\frac{\Delta R}{R}$ as function of pressure sensor resembles the simulated behavior as included in Figure 6.5, although the result shows that the measurement range of the realized device is shifted to smaller pressures. The measured $\frac{\Delta R}{R}$ of -1.6×10^{-3} bar^{-1} (decreasing resistance with increasing absolute pressure) is different from the value as simulated in Section 6.2.2 of -3.23×10^{-4} bar^{-1}. In order to investigate this discrepancy, the gauge factor can be determined based on the measured $\frac{\Delta R}{R}$ by using the following equation:

$$\mathrm{GF} = \frac{\frac{\Delta R}{R}}{\epsilon} \tag{6.11}$$

In which ϵ equals the strain, which is determined using the volumetric strain as available from our numerical model yielding to 1.64×10^{-5}. Using equation 6.11 with a measured $\frac{\Delta R}{R}$ of -1.6×10^{-3} bar^{-1} results in a calculated gauge factor of -91. This value is much higher than reported gauge factors in literature for poly 3C-SiC. Eickhoff et al. [26] re-

ports for example a GF of -10 for n-type doped poly 3C-SiC, whereas Yasui et al. [57] reports a GF of -2.1 for such a layer. In addition, Strass et al. [58] reports a GF of -5 for randomly nitrogen-doped poly-SiC. Although the derived value of -91 for the gauge factor is unrealistically high compared to literature, it suggests that the gauge factor used in the simulation is higher in reality. The simulation was furthermore based on the Young's Modulus and Poisson ratio as reported in literature. The actual values of these two properties might differ, which can be another reason for the discrepancy between the simulated and measured sensitivities.

Wheatstone Bridge The Wheatstone half-bridge consisting of two non-released and two released square membranes having a side length of 200 µm was measured. The individual pressure devices of the Wheatstone bridge feature 7 µm wide electrodes through 5 µm contact holes on the sideplane of the membrane. The purpose of the non-released membranes is to function as dummy devices which experience identical circumstances as the sensing membranes. The bridge was biased using a constant voltage of 1 V, while the bridge voltage was measured using the two other probe needles at the sensing pads. In order to read out the Wheatstone bridge, a dual channel configuration was set for the SMU. Channel A was used to deliver a constant voltage, while channel B was used to continuously measure the bridge voltage as indicated in Figure 6.19. In a similar way as for the characterization of the single device, the bridge voltage was continuously measured while pumping down the probe station. Data were acquired with a sample rate of 1 sample /s and the entire measurement ran for 249 s.

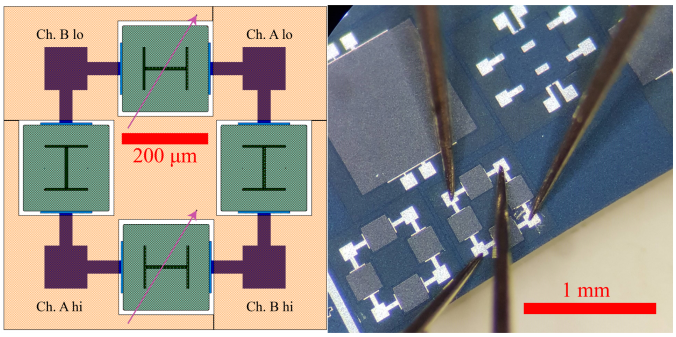


Figure 6.19: The Wheatstone bridges connections to the SMU; schematically (left) and through microscope (right).

The offset voltage present at 100 kPa and corresponding to 617.9 mV was subtracted from the measured bridge voltage, resulting in the Δ bridge voltage against pressure as shown in Figure 6.18. As can be seen from this results, the bridge voltage is decreasing

with decreasing pressure when pumping down from atmospheric pressure. This can be explained by the operation of the Wheatstone bridge; at $t = 0$ two out of four pressure devices experience a large overpressure and the bridge is essentially out of balance. As time passes the absolute pressure is decreasing and thus the pressure difference is decreasing. The resistance of the released device is getting closer to the resistance of the non-released devices and the bridge becomes more balanced. In the data analysis, the absolute value of the bridge voltage was plotted for convenience. The maximum bridge voltage difference at 50 Pa equals 1.1 mV. In the pressure range from 100 kPa down to 2000 kPa, the bridge voltage difference shows a linear response, which is followed by a straight line in between 50 Pa and 1 kPa, which shows that the bridge voltage is a logarithmic function of the pressure. The difference in measurement range between the single device and the Wheatstone bridge can be explained by the different geometry of the (individual) devices. The Wheatstone bridge consists of four square membranes having a side length of 200 µm, while for the single device the side length is 300 µm. The measurement range of the smaller devices is shifted to larger pressures, as is indicated by the absence of saturation in the measurement result of the Wheatstone bridge. To give an indication of the stability of the bridge voltage, a temperature sweep was performed at constant (atmospheric) pressure, resulting in a deviation of 0.19 mV when the temperature is varied from 25 °C to 125 °C.

6.5. PIRANI GAUGES IN POLY-SIC

The work on the Pirani gauges was performed by J. Mo in collaboration with and under supervision of the author. Parts of this section have been included in [59] and [2].

Motivation Based on the fabrication process used for the surface micromachined pressure devices, Pirani gauges were modeled, designed and fabricated. The motivation for this work is that, since the operation mechanism of Pirani gauges is in the thermal domain, a higher degree of redundancy is achieved, when both the mechanical and thermal based pressure device are integrated, thereby yielding a multi-physical pressure sensor. The available process to fabricate the mechanical pressure devices, as described earlier in this Chapter, is used as starting point for the design of the Pirani gauges. By re-using the poly-SiC deposition, etching and releasing steps, the design and fabrication of the Pirani gauges is greatly aided, since development of these processing steps have already been performed. In order to design a Pirani gauge that is capable to work in at elevated temperatures while showing high sensitivity over a large dynamic range, a MEMS Pirani gauge based on the micro-bridge structure in SiC is implemented.

Background Mechanical, thermal conductivity and ionization based gauges are the three major types of pressure sensing in vaccuum applications. Pirani gauges are categorized to the thermal conductivity type and have the advantages of a high robustness, low cost and good miniaturization and integration potential, mainly thanks to the surface micro machining. A disadvantage is the sensitivity to the gas species. Miniaturized Pirani gauges have been reported in literature [60–64]. Moreover, research has been conducted to apply new materials and technologies on the concept of Pirani gauges to enhance the performance and extend the functionality, also in the light of compatibility with monolithic integration with integrated circuits [61, 63, 65].

Modeling and Design The heat losses in a Pirani gauge are given by:

$$Q_{total} = Q_{gas} + Q_{solid} + Q_{radiation} + Q_{convection} \tag{6.12}$$

Of these heat losses, Q_{gas} is pressure dependent. The Pirani gauge is biased with known injected power, and the cooling rate is determined by the amount of molecules around the beam, hence the air pressure. This in turn influences the temperature of the beam, which is read-out using the thermal coefficient of resistance (TCR). The TCR value of the poly-SiC layers used is thereby largely influencing the sensitivity of the Pirani gauge. Apart from poly-SiC, Pirani gauges in poly-Si [60, 61, 64–66], platinum [62] and gold have been reported [67].

An analytical model has been derived based on a suspended micro heater structure, taking into account all heat losses. For this analytical model, the TCR values of the different layers need to be determined. Experiments were carried out from 25 °C to 200 °C. The results for layers D1, D2 and D4 are included in Table 6.7. It can be concluded from these results that the TCR is negative and increasing with decreasing dopant concentration, as is in correspondence with results and literature described in Chapter 5 and reported by Morana [55]. The absolute value of the TCR as included in Table 6.7 is significantly lower compared to the results from Chapter 5. This discrepancy can be explained by the leakage current at elevated temperature through the membrane layer of non-intentionally doped poly-SiC of the devices described in Chapter 5.

In addition to this analytical model, the microbridge structure was analyzed by using FEM. More details on the analytical and FEM modeling of the realized Pirani gauges can be found in [59]. Based on the modeling it was concluded that the largest dynamic range is achieved by making the suspended heater as long as possible, while having a minimum gap size. The effect of thermal buckling of the beam, thus the beam touching the substrate by thermal expansion, thereby inhibiting device operation, was investi-

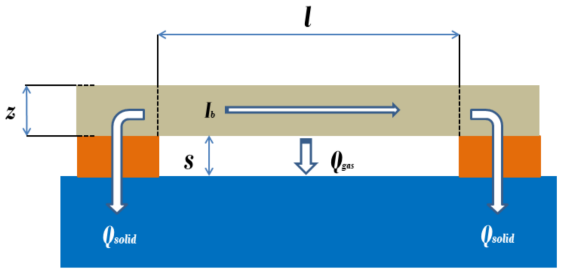


Table 6.6: A schematic representation of the suspended micro heater as Pirani gauge, including the annotated design parameters.

Layer ID	TCR ppm /°C
D1	−1770.0
D2	−1080.0
D4	−586.4

Table 6.7: The measured TCR for poly-SiC layers D1, D2 and D4 layers based linear fittings from 25 °C to 200 °C.

gated too. The nominal device has less than 600 nm deflection up to 500 °C, which is smaller than the gapsize. Suspended heaters with different geometries are included in the design for different sensitivities and pressure ranges.

Fabrication Fabrication of the suspended micro bridge structures is based on surface micro machining on silicon wafers. Only three photolithographic steps are needed to fabricate the device. A schematic illustration of the process flow is reported in Figure 6.20. 300 nm Si_3N_4 was deposited as additional isolation between the metal and substrate (Figure 6.20a). In contrast to Si_3N_4, SiO_2 is isotropically etched during the release step, resulting in under etch of the metal probe pads, possibly making unwanted contact to the substrate. The usage of the silicon nitride layer prevents this from happening. PECVD TEOS is used as sacrificial material (Figure 6.20c), on which *in-situ* doped poly-SiC is deposited (Figure 6.20d).

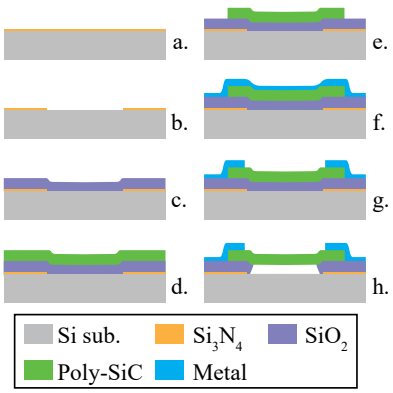


Figure 6.20: The process flow used during fabrication.

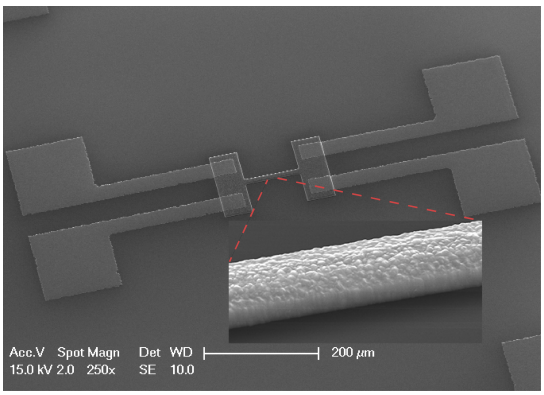


Figure 6.21: SEM image of a Pirani gauge with a length of 150 µm (w=10 µm and s=2 µm) including zoom-in.

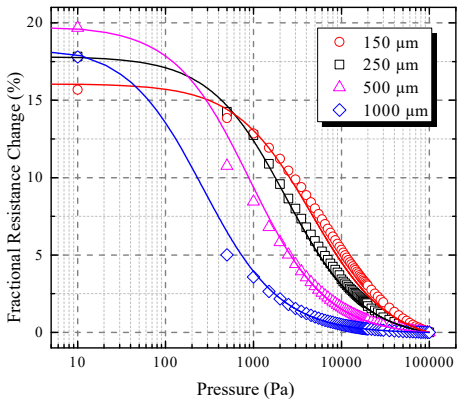
More information on the poly-SiC deposition process can be found in Section 6.3.1. The micro bridge is patterned by lithography and a subsequent plasma etch (Figure 6.20e). Aluminum and titanium are sputtered to form electrical contacts to the micro bridge structure, and a 400 °C annealing step was performed (Figure 6.20f-g). The micro bridge structures are finally released using vapor HF (Figure 6.20h). The realized micro bridges were inspected by using a SEM, as is illustrated by Figure 6.21. Note the shadow below the micro bridge indicated that the structure is fully released. The longest Pirani gauge that was fabricated had a length of 1000 µm. Although this geometry is most likely to demonstrate the highest (vertical) deflection among the different designs, stylus profiler measurements revealed no measurable deflection after realization.

Measurements The identical measurement setup was used for the characterization of the Pirani gauges, as was used for the surface micro machined mechanical membranes described in Section 6.4. The controller of this setup can change the pressure in steps of 500 Pa while the internal pressure sensor has a resolution of 10 Pa. Because Pirani gauges are most sensitive in the pressure range below 20 kPa, the range from 10 Pa to 100×10^5 Pa is split into three parts. For each part, a different pressure step is defined. For each of the points, the measurement was paused for 200 s so that the pressure in the micro-chamber can fully stabilize whereafter the electrical measurement is performed.

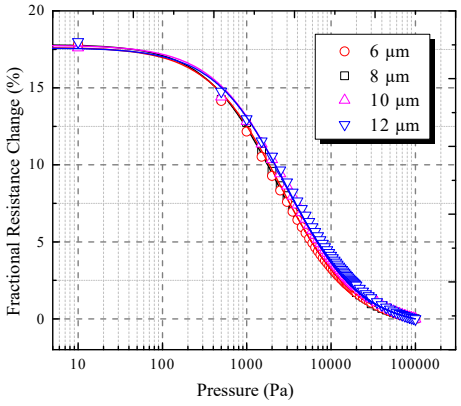
To study the effect of the variation in the geometry on the performance, a Pirani gauge with a length of 250 µm, a width of 8 µm, a thickness of 2 µm and a gap size of 2 µm is taken as a reference device. The reference device was biased with a constant current of 600 µA. The gauge resistance ranges from 4978.3 Ω to 6060.0 Ω from the lowest pressure set-point of 10 Pa to 100 kPa, which corresponds to a maximum resistance deviation of 17.8%. The Pirani gauge shows a response to the pressure change without hysteresis, since a symmetrical shape of the pressure vs. resistance curve was observed.

Room temperature measurements were carried out to verify the effects of different geometries. Figure 6.22a shows the measurement results for Pirani gauges with different lengths. Since Pirani gauges with various dimensions have different initial resistance, the output resistance is expressed with the factional resistance change $R_{fractional}(P)$ as shown in equation 6.13. In the result Figures, the scattered data points are obtained with the measurement setup, and the continuous curves are fitted based on the analytical model as derived in [2]. From the fitting data, the reference gauge has the highest sensitivity of 0.47 Ω Pa^{-1} at around 10 Pa.

$$R_{fractional}(P) = \frac{R_0 - R_{filament}(P)}{R_0} \cdot 100\% \tag{6.13}$$



(a) The fractional resistance change versus pressure for micro bridges with a lengths of 150 µm, 500 µm, 1000 µm and the nominal length.



(b) The fractional resistance change versus pressure for micro bridges with a widths of 6 µm, 10 µm, 12 µm and the nominal width.

Figure 6.22: Room temperature measurements.

It can be concluded from this result that increasing the length, shifts the curve to the left because Q_{gas} takes a larger proportion in the total heat transfer. From 150 µm to 1000 µm, the maximum sensitivity increases from 0.13 Ω Pa^{-1} to 16.76 Ω Pa^{-1}. It is worth mentioning that the maximum sensitivity of each gauge is at 10 Pa, which implies that the gauge is still sensitive below 10 Pa.

Moreover, measurements were carried out to verify the effect of the bridge width on the performance. Micro bridges with a widths of 6 µm, 10 µm, 12 µm and the nominal width were measured, of which the measurement results are included in Figure 6.22b. The slight left shift of the response curves is in agreement with analytical modeling, and from the measurements it was confirmed that the narrower Pirani gauges are more power efficient when compared to their wider counterparts. When comparing for example the 6 µm wide gauge with the 12 µm, the narrower gauge consumes 56.2% less power compared to its wider counterpart, while achieving a similar fractional resistance change.

From the response curves for different gap size, as included in Figure 6.23, it can be concluded that the highest sensitivity is achieved with the smallest gapsize, as can be expected from the physical operating mechanism. It can further be noted that the Pirani gauge with the smallest gap size is saturating at a higher pressure compared to the nominal and 1 µm gapsize. The measurement setup was not capable of performing measurements below 10 Pa.

In general, the experimental results align with the prediction of the analytical model qualitatively: longer beam will have a larger sensitivity in low pressure range, and the

gauge with a smaller air gap has a larger sensitivity near the standard atmospheric pressure. However, numerically, the experimental results do not match the analytical results. From the measurement, the reference gauge shows a 17.8% fractional resistance change, while the analytical model and COMSOL simulation both predict only 0.16% of fractional resistance change. A possible reason for this discrepancy could be that the material properties of poly-SiC as used for the modeling, such as thermal conductivity, are currently literature-based which might deviate from the properties of the deposited layers.

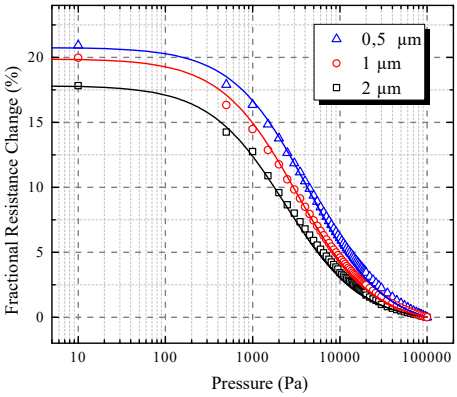
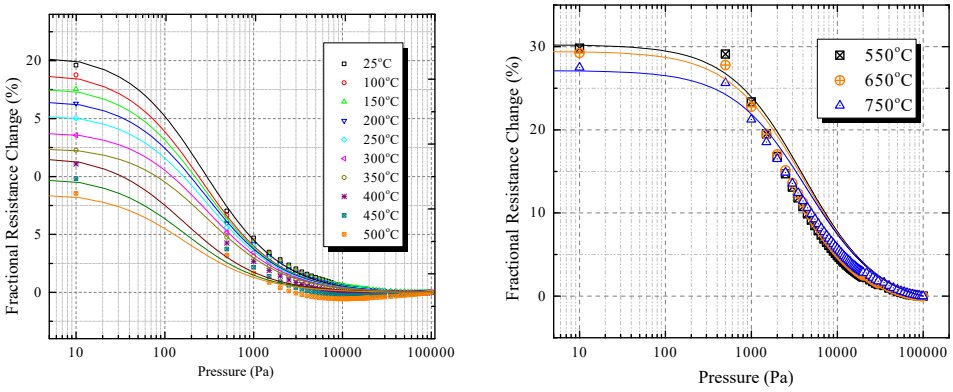


Figure 6.23: The fractional resistance change versus pressure for micro bridges with a gapsizes of 0.5 µm to 2 µm.

Measurements at elevated temperatures are carried out by using the available hotplate in the micro probe station. The 1000 µm Pirani gauges with aluminum metallization were characterized at temperatures from 25 °C to 500 °C. The result of this measurement is summarized by Figure 6.24a, from which it can be concluded that the fractional resistance change reduces, while the maximum sensitivity decreases from 17.63 Ω Pa^{-1} at 25 °C to 6.15 Ω Pa^{-1} at 500 °C, which was measured to be caused by a decreasing TCR for an increasing temperature.

For characterization beyond 500 °C, the realized devices with Ti metallization were measured. The reason for this is the higher melting point of Ti of 1668 °C compared to 575 °C for Al with 1% Si. The measurement results at 550, 650 and 750 °C are given in Figure 6.24b. Even at these temperatures, the device demonstrates a repeatable response to pressure change. The maximum sensitivity can still be obtained at 10 Pa, which is 1.35 Ω Pa^{-1} at 550 °C, 1.23 Ω Pa^{-1} at 650 °C and 0.81 Ω Pa^{-1} at 750 °C.

Dynamic effects of the Pirani gauges was investigated by determining the response time, i.e. the time it take before the output is settled after an abrupt change in pressure. The



(a) While using Al metallization in the range from 20 °C to 500 °C.

(b) While using Ti metallization in the range from 550 °C to 750 °C.

Figure 6.24: High temperature characterization of the 1000 µm long gauge (w=8μm, z=2μm, s=2μm).

Pirani gauge was subjected to an abrupt pressure increase from 5 kPa to 20 kPa at temperatures from room temperature up to 700 °C. The measured response time within a 5% tolerance band equals 3 s. No dependency on the temperature was observed. It can be concluded that the Pirani gauge exhibits successful operation up to 750 °C, which is promising in the context of future monolithic integration with SiC CMOS technologies.

6.6. CONCLUSION

Surface micromachined absolute pressure sensors have been designed and realized based on the self-sensing and Pirani concepts, while enhancing device and processing flexibility to make integration with SiC CMOS possible. Intrinsic and in-situ doped polycrystalline SiC was used as functional material and its bulk resistivity and residual stress were measured. Finite element modeling was applied to verify the desired mechanical and piezo resistive behavior and the results were in correspondence with the analytical modeling. Ohmic behavior of the contacts between lowly doped poly-SiC and titanium and AlSi(1%) was verified by measuring test structures. A single pressure device of 300 µm was measured and a logarithmic response of $\frac{\Delta R}{R}$ was measured yielding a full range response of -1.6×10^{-3} bar^{-1}, where the sensitivity is maximum between 1×10^2 Pa and 1×10^3 Pa. The reported negative gauge factors were confirmed by the measurements and the response is larger than the value simulated.

A half Wheatstone bridge was measured and the difference in bridge voltage over the full range equals 1.1 mV. Upon decreasing pressure starting from atmospheric pressure it is shown that the bridge voltage difference shows a linear response down to 2000 Pa

and behaves logarithmic below this pressure. It can be concluded that the concept of a self-sensing membrane is successful and can be used to realize surface micromachined pressure sensors, of which the functional material is solely polycrystalline SiC. Thanks to the modular design the device can be tailored to different applications by tuning the pressure range of maximum sensitivity. The convenient processing is beneficial for future integration with SiC CMOS, for example for impedance read-out, analog to digital conversion or signal amplification.

Future work on the piezoresisitive cavities involves characterization of the devices at temperatures beyond room temperature. Future work on the Pirani gauges involves characterization of the devices at temperatures beyond room temperature. Additionally, a different ratio of the intrinsic to doped layer can be chosen to optimize the piezoresistive performance. Stability of the devices and ohmic contacts for extended periods of time at high temperatures and in harsh environments is also considered as future work. Long term (more than six hours) stability of the realized Pirani gauges at high temperatures is still to be investigated.

In addition to the surface micromachined cavities, suspended microbridge structures functioning as Pirani gauges have been modeled, designed, realized and measured. Poly-SiC layers with different doping concentrations were characterized and based on the TCR characterization, the optimal doping concentration was determined. The MEMS Pirani gauges in SiC are fabricated with a surface micro-machining technique by means of a three-mask process. The cleanroom fabrication was based on the existing process flow of poly-SiC on silicon oxide sacrificial material. The use of SiC combines favorable properties such as a useful TCR, high mechanical stiffness, and compatibility with high temperatures and harsh environments. The realized Pirani gauges can achieve a length of 1000 µm without any mechanical supporting structure to prevent buckling. At room temperature, the gauge with reference geometry showed a maximum sensitivity of 0.47 $\Omega\,\mathrm{Pa}^{-1}$ and a fractional resistance change of 17.8%. High-temperature characterization on the 1000 µm long beam revealed the desired operation even up to a maximum temperature of 750 °C. These results illustrate the potential of poly-SiC Pirani gauges for applications at high temperatures and in harsh environments. However, beyond 750 °C, the resistance of some devices increased while the pressure was decreasing. The future work will include a closer investigation into the undesired device performance beyond 750 °C. In such an analysis the temperature dependency of the TCR, the possible buckling and radiative losses at high temperatures need carefully to be taken into account.

Revisiting the third goal of Section 1.6, one could remark that the presented sensors in this Chapter are not the very first harsh environment compatible SiC-based pressure de-

vices. However, when taking the fifth goal into account, namely the integratability with SiC CMOS technologies, the presented concepts for both pressure sensors are beneficial in the light of the challenging integration of the MEMS fabrication flow in the BE CMOS fabrication flow, as already discussed before. Examples are the surface micromachining which reduces the dependency on the type of substrate. Also the self-sensing concept and the similarity between the Pirani and piezoresistive pressure sensor fabrication flow will be benefits for future CMOS integration.

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7

INTEGRATED SIC-CMOS ELECTRONICS

As second key step toward the goal of smart integrated SiC sensors, this Chapter moves the focus from discrete SiC sensors to SiC electronics. This Chapter discusses various SiC CMOS based devices and electronics, resulting in the design of a multi-project die. A large variety of circuit- and device-designs have been integrated on this die. Among numerous other devices, a resistive read-out circuit, two capacitive read-out circuits and various different temperature sensing circuits have been designed. The circuit simulations relied on pre-mature LT Spice models based on measurements of single PMOS and NMOS devices. Channel length modulation was not taken into account in these models. The layout was started from scratch and was based on the available design rules. Effort was taken to efficiently use the available die area and output pins. The circuit designs from three different independent researchers are integrated on two different 10 x $10\,\mathrm{mm}^2$ *die designs, along with three different process control modules (PCMs). The layout was verified using a design rule checker in K-layout and eight wafers were fabricated in the facilities from Fraunhofer IISB Erlangen, Germany. Back-end processing is anticipated where the second metal layer is to be fabricated in the EKL facilities. Wafer scale measurements were prepared on the four and six probe PCMs. Dicing of the mono-SiC wafers was experimented and performed successfully. Measurements of single 10 x* $10\,\mathrm{mm}^2$ *dies was prepared by PGA64 packages and a designed interface PCB.*

7.1. INTRODUCTION

IN contrast to power electronics from crystalline SiC, low voltage SiC CMOS can still be seen as immature and being in the research phase. In order to realize harsh environment compatible smart integrated sensors with the physical transducer, such as a cavity or Pirani bridge to measure absolute pressure, monolithically integrated with read-out electronics, a SiC CMOS technology is required. The usage of (integrated) SiC CMOS is economically sensible when high-temperature applications (> 300 °C) are considered, in which advanced packaging of the SiC sensor with Si CMOS does not suffice. The CMOS technology considered would ideally work at relatively low voltages, enabling low-power operation and compatibility with state-of-the-art silicon technology based back-end electronics. The availability of front-end CMOS electronics would enable for example impedance read-out, signal amplification and communication circuitry to be integrated as close as possible to the MEMS sensor, reducing noise contributions and enabling read-out directly in the electrical domain. Monolithically integrating electronics with MEMS based sensors results in a platform which can operate entirely inside a harsh environment an on which front-end read-out can be directly performed. When the piezo resistive pressure sensor as described in Chapter 6 is considered, it is evident that it would be preferable to read-out the resistance change on the same chip with a tailored circuit delivering 'strong' output voltage. Such a circuit can be designed such that it is capable of sourcing long interconnection cables leading from the harsh environment to an environment where back-end signal processing can take place. Without on-chip electronics, the impedance change need to be read-out via long cables, which adds to the total resistance and additional noise should be taken into account due to electromagnetic interference (EMI).

In literature, SiC-based electronics are reported both based on epi-stacks and implanted regions. Coarsely, one could say that epi-stacks, which are selectively etched to form isolated mesa structures, are used for bipolar junction transistor (BJT) based electronics, whereas implanted doped regions are typically used for CMOS. The research group at KTH Sweden focuses on circuits based on BJTs. Zetterling et al. has recently reported an overview of the available building blocks to design BJT based circuitry [1].

For the design and fabrication of the SiC CMOS, a collaboration with Fraunhofer IISB, Erlangen, Germany is started. The technology originates from experience of the research group with power devices (power diodes and MOSFETs) and photodiodes. This process uses mono-cystalline 4H silicon carbide and is intended for harsh environments. The V_{dd} considered for this technology equals 20 V, which can be considered low for analog front-end electronics and digital building blocks.

In recent years, various electronic devices and circuits have been postulated in literature. Lanni et al. reports successful operation of n-p-n bipolar junction transistors based on selectively etched epi-stacks of 4H-SiC, from which OR/NOR gates were realized and measured up to 500 °C [2]-[3]. Hedayati et al. has shown an eight bit digital to analog converter based on R-2R current steering topology and an two stage operational amplifier (opamp), in similar SiC BJT technology, both showing operation up to 500 °C [4]-[5]. It is claimed by them that the BJT technology based on the selective (mesa) etching of epitaxial layer favors reliability, since no gate oxide is present that typically degrades upon long-term exposure to high temperatures. Digital building blocks designed in an automated design flow such as counters, finite state machines (FSMs), ring oscillators, shift registers and D-flip flops are realized in the Raytheon technology and their operation was tested and confirmed up to 300 °C by Kuhns et al. [6]. In literature, multiple works can be found based on the technology from the Raytheon institute. This institute is a defense contractor that used to run a SiC CMOS process called HiTSiC. However, the SiC activities of this institute are currently shut down. Rahman et al. reports on voltage and current references designed in the 15 V 1.2 µm HiTSiC process [7]. In the same technology, a SiC CMOS linear voltage regulator based on a two-stage operational amplifier feedback loop was reported, exhibiting operation up to 400 °C [8]. The technology used in this work is developed by Fraunhofer during the last years based on their experience with photodiodes and power devices. This is illustrated by work carried out on high-voltage discrete MOSFET devices [9], SiC junction barrier diodes [10] and photodiodes [11]. Recently, a six-transistor static random-acces memory (SRAM) cell was designed and realized by Abbassi et al. (University of Arkansas) based on the Fraunhofer SiC CMOS technology [12]. The smallest gate length used in this work equals 1 µm and the SRAM-cell showed successful operation up to 300 °C.

7.2. THE FRAUNHOFER SIC CMOS TECHNOLOGY

The FHG SiC CMOS technology is based on 4H-SiC substrates in which N-well (NW), P-well (PW), shallow-N (SN) and shallow-P (SP) regions are implanted. The electrical activation of dopants in crystalline SiC requires annealing at temperatures beyond 1500 °C [13] which is one of the reasons why SiC CMOS processes cannot (yet) be performed at EKL. Because the SiC CMOS technology from FHG is based on the experience with power electronics, it is optimized for low contact resistances. Ohmic contact formation to crystalline SiC is not trivial and requires particular metals for work function matching, as was also discussed in Chapter 4, after which rapid thermal processing (RTP) is required to form silicides. The analog circuits will be designed based on LT Spice models,

which include the influence on the device parameters caused by elevated temperatures of 25, 75, 150, 225 and 300 °C. The gates are formed from poly-Si with a thickness of 500 nm. A summary of the used SiC technology is included in Table 7.1.

Table 7.1: FHG technology summary.

Figure	Value
Die size (topcell)	15 x 30 mm^2
Lithographic resolution	0.8 µm
V_{dd}	20 V
Silicides	AlTi (p-type); NiAl (n-type)
Metal 1	700 nm aluminum
Gate oxide	50 nm (thermal)
Poly Si thickness	500 nm
Field Oxide (FOX)	400 nm
N-epi	5×10^{14} # /cm^3 to 8×10^{14} # /cm^3
N-well	3×10^{15} # /cm^3
P-well	1×10^{17} # /cm^3

7.2.1. DOUBLE WELL PROCESS

The Fraunhofer SiC CMOS run will be carried out on 4H-SiC 100 mm wafers with epitaxial layers. There has been chosen to opt for a so-called double well process, where N-epitaxy is used in combination with an N-well and a P-well which are separately and parallel to each other implanted, yielding separated P- and N-wells. In a double well process, the N-epitaxy doping concentration is typically lower than the N-well dopant concentration, because the implanted N-well is used to yield a higher degree of uniformity and dopant concentration control over the wafer. The used doping concentrations are summarized in Table 7.1.

Alternatively, a single well process could have been used, where only an P-well is implanted, and the N-epitaxy is used for the PMOS devices, causing PMOS characteristics to be influenced by the epi-doping. In a triple well process, a P-epitaxy is used, in which an N-well and P-well are implanted (the P-well can then be placed inside the N-well). The main advantage of such a triple well process is that the NMOS and PMOS devices are isolated from the substrate and can therefore be differently biased. Additionally enables a triple well process the fabrication of for example lateral UV diodes. At the time when the decision on this technology aspect had to be made, FHG had no experience yet with the characterization of UV sensors in a triple well process, hence an additional motivation for the double well process.

Another consideration related to the well formation, is the implantation energy associated with the N-well implantation. In the standard FHG process flow, an implantation

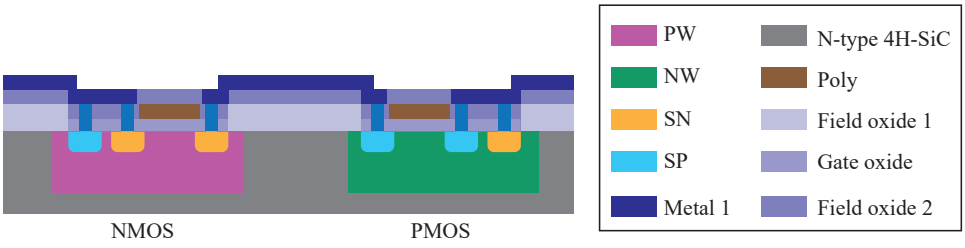


Figure 7.1: A cross section of the FHG process. Reproduced from [14].

energy of 860 keV is used, which requires a hardmask. The reason for this high implantation energy is that this N-well implantation step results then in a larger junction depth, which is required for a triple well process. Because in this work a double well process is used, this implantation energy can be decreased below 500 keV allowing photo resist to be used as masking material, thereby speeding up the fabrication process.

7.2.2. BODY CONTACT

Because the structure of the doping concentrations, as illustrated by Figure 7.1, the entire substrate will be biased at V_{dd} once the source of one PMOS is connected to the V_{dd} (N-well is biased at V_{dd} and sets the entire substrate to V_{dd}). The bulk contact will thus be biased at any condition at V_{dd}. The initial LT Spice models were derived by FHG from measurements on single devices, only for the scenario in which the bulk was connected to the source, in principle limiting the validity of these models to this scenario. When circuits are considered where the source is not connected to V_{dd}, the threshold voltage is affected due to the different source biasing, also called the body effect. This can for example occur in the case of a PMOS based differential pair. Mitigating circumstances are in this case the large value of V_{dd} and the possibility to externally bias the circuit differently by sourcing or sinking a current or by applying a voltage bias on the gate of the biasing transistor on top of the differential pair.

7.2.3. OHMIC CONTACTS

The ohmic contacts are formed by using a self-aligned silicidation process, also called a salicidation process. After the contact openings are opened 50 nm of the dedicated metal is sputtered and patterned by using lift-off. Experiments have been performed to use a salicidation process with solely NiAl to interface both n- and p-type SiC. Although good ohmic contacts were achieved with the NiAl salicides on n-doped regions, the NiAl salicides fail to do so on p-doped regions, based on the measured specific con-

tact resistance ρ_c that ranges from $0.2\,\Omega\,cm^{-2}$ to $2\,\Omega\,cm^{-2}$. Based on these results it was concluded that two different metals are required for respectively n- and p-type SiC, as already implied by the large bandgap of mono-4H-SiC.

NiAl (2%) is used to make ohmic contact to n-type SiC, achieving a specific contact resistance ρ_c of $1\times10^{-3}\,m\Omega\,cm^{-2}$ to $5\times10^{-3}\,m\Omega\,cm^{-2}$. TiAl is used to make ohmic contact to p-type SiC with a specific contact resistance ρ_c ranging from $0.15\,m\Omega\,cm^{-2}$ to $0.25\,m\Omega\,cm^{-2}$. The aluminum content in the metallization sputtered is used as catalyst for the silicidation as it binds to carbon forming Al_4C_3 which is removed by any type of wet chemistry. The first rapid thermal annealing (RTP) step is carried out at 980 °C for 20 min. Caro's acid is used to etch away the unreacted metallization, which consists of a mixture of hydrogen peroxide with sulfuric acid. Thereafter, a second thermal step at 980 °C is performed.

After the silicides have been formed, regular metal deposition can be performed using sputtering. Aluminum is the standard metallization material for M1. Thanks to the silicides (enabling a non-rectifying contact) that have already been formed, a metal with a higher melting point than aluminum, such as titanium, can be used without problems for applications beyond 300 °C. Although the melting temperature of titanium is higher, the relative large residual stress complicates the usage of this metal as gate material. After the metal has been deposited and patterned, an alloying step is performed at 450 °C for 30 min in the presence of forming gas and at atmospheric pressure. The forming gas used is 5% H_2 in N_2. The backside of the wafer is considered nickel contaminated after the contacts have been formed, resulting in additional measures to prevent contamination when further processing in the EKL facilities is considered.

7.3. CIRCUIT DESIGN

The circuit designs and simulations were performed in collaboration with Sining Pan (Electronic Instrumentation Laboratory).

This Section describes the topology and circuit design of the different parts of the SiC CMOS die. Each circuit will be designed as modular building block, meaning that the it is free standing in terms of connections (output pins or probe pads). Also, although tailored to a a certain input impedance range, each circuit can be used freely for reading out different sensors. The modularity is furthermore reflected in the layout, as will be discussed later. Among other circuits which will be designed for the process control modules, circuit model derivations and other experimental devices the five main circuits to be designed are listed below. An example of devices with a more experimental character are photodiodes based with an anode of graphene.

1. Resistive read-out based on a relaxation oscillator. This circuit can be used to read-out piezoresistive pressure sensors.
2. Thermistor based temperature sensors: Thermistors are designed and read-out using a relaxation oscillator.
3. 4 transistor and 5 transistor based proportional to absolute temperature (PTAT) circuits to measure (absolute) temperatures.
4. A capacitive read-out intended to read-out capacitive MEMS sensors. This circuit uses a clocked comparator and a unit-capacitor to measure the capacitance under test.
5. Relaxation oscillator based capacitive read-out.

7.3.1. RELAXATION OSCILLATOR BASED RESISTIVE READ-OUT

Although the intended modularity of the read-out circuit would allow to read-out different resisitive based sensors, as starting point for the design the cavity based pressure device is used as described in Chapter 6.

One of the differences between silicon and silicon carbide is the significantly lower carrier mobility μ which influences the driving capabilities of SiC CMOS MOS devices. The mobility of electrons and holes is largely determined by the donor respectively acceptor concentrations and the temperature. With increasing dopant density the mobility of charge carriers decreases (for both n-doped and p-doped). And for increasing temperature the mobility also decreases (for both n-doped and p-doped). At room temperature the electron and hole mobilities in intrinsic 4H-SiC equal 1000 $\mathrm{cm^2\,V^{-1}\,s}$ and resp. 120 $\mathrm{cm^2\,V^{-1}\,s}$, which already implies that the driving capabilities of PMOS transistors with equal size are significantly smaller compared to NMOS transistors [13]. The reduced mobility values of charge carriers in the channel of SiC CMOS designs is mostly expressed at elevated temperatures and increased doping levels, thereby negatively influencing driving capabilities. In realistic bias conditions, the mobilities of the technology used in this work equal at 20 V gate source voltage 18 $\mathrm{cm^2\,V^{-1}\,s}$ to 20 $\mathrm{cm^2\,V^{-1}\,s}$ for the NMOS, while the hole mobility for PMOS under the same conditions only equals 3 $\mathrm{cm^2\,V^{-1}\,s}$ to 6 $\mathrm{cm^2\,V^{-1}\,s}$ [14]. Because of the limited driving capabilities, it would be desirable to connect high ohmic loads to the output stages of the circuits designed. To give a quantitative estimation, it would be best if the resistance is around 100 kΩ. To increase the equivalent sensor resistance, multiple pressure sensors can be cascaded.

The read-out circuit proposed is a continuous-time comparator based relaxation oscillator. Advantages of this implementation are the low transistor count and the possibility

to tune the resonance frequency with an off-chip capacitor. The output signal will be a frequency which is dependent on the RC time constant. By doing so, the measured resistor is in the feedback loop of the circuit, and the capacitor can be put off-chip. As can be derived from solving the differential equations for the comparator based relaxation oscillator, the oscillation frequency is determined by:

$$f_{osc} = \frac{1}{2\ln(3)RC} \tag{7.1}$$

The designed circuit consists of 18 transistors, of which 12 are used for the comparator and 6 for the output buffers of the oscillator itself, assuming external biasing currents. The target specifications are listed in Table 7.2.

Table 7.2: Target specifications of the resistive readout circuit based on the relaxation oscillator.

Figure	Value
Temperature range	20 °C to 400 °C
Input range resistance	0.5 kΩ to 100 kΩ
Bandwidth	1 kHz
Area	3 mm^2 × 3 mm^2
Transistor count	12 (comp.) + 6 (output stages)

CIRCUIT SIMULATION

Based on the models delivered by FHG, LT Spice simulations were performed to aid the circuit design. The schematic of the relaxation oscillator is included in Figure 7.2. The two feedback loops can be identified, where a resistive divider is used to bias the inverting terminal of the comparator with half the V_{dd}. C_3 refers to the off-chip capacitor, while R_3 represents the sensor resistance. The reference voltage is set to half the V_{dd}. The three inverters are included to give the circuit more driving capabilities, which also explains the large PMOS width of the last output stage. Component X1 represents the analog comparator, of which the schematic is included in Figure 7.3, which is based on a PMOS differential input pair followed by a common-source amplifier. The sizing of the current mirror was based on the added widths of the NMOS currents in the entire comparator. A transient simulation was performed up to 20 ms, in which the resistance values are swept from 80 kΩ to 100 kΩ. The circuit is biased with a V_{dd} of 20 V and the comparator is biased with a current of 100 µA. The output voltage 'drive 2' is plotted in Figure 7.4, from which it can be concluded that the output frequency is a function of the RC-time constant, hence the swept resistance value R3. The time period of the output signal equals 4.67 ms which is in close correspondence with the analytical derivation for the time period of 4.39 ms.

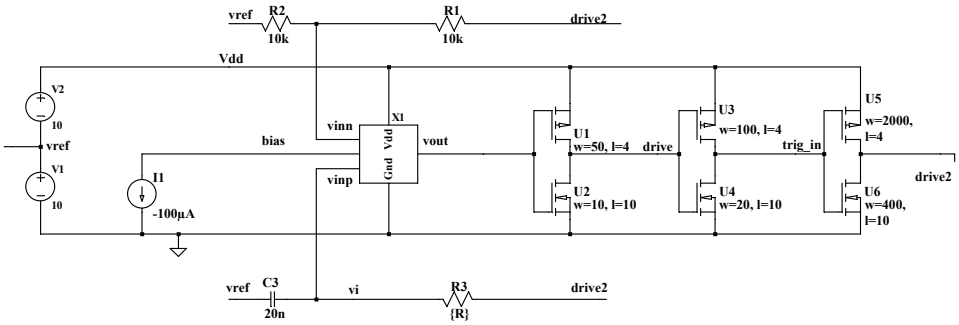


Figure 7.2: The schematic of the relaxation oscillator used for the piezoresistive pressure sensor read-out. Note the two equal resistors in the top feedback loop, and the combination of the off-chip capacitor C_3 with R_{meas} in the lower feedback loop.

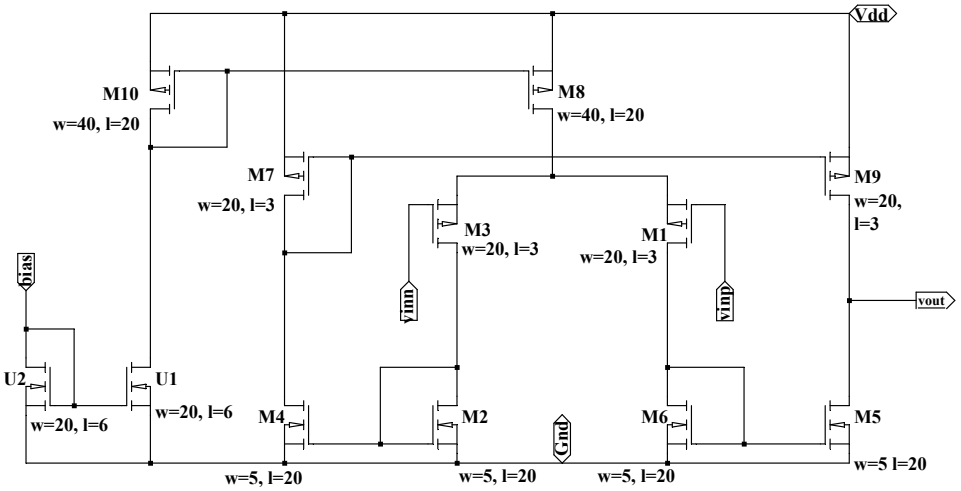


Figure 7.3: The schematic of the comparator used for the relaxation oscillator.

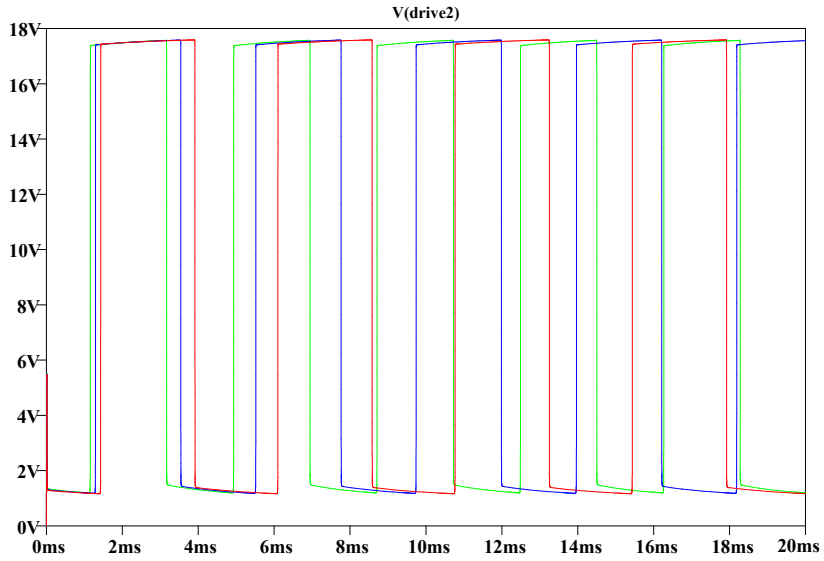


Figure 7.4: The simulated output voltage for R_{meas} of 80, 90 and 100 kΩ with C_3 of 20 nF at a temperature of 25 °C.

Although the designed circuit still works for R_{meas} values much below 100 kΩ, it would be best to read-out a total piezo resistive load of more than 100 kΩ. The designed circuit in LT spice is still converging for resistive loads of 10 kΩ and even for 1 kΩ, but at a significantly decreased amplitude of the output voltage. Although this effect is undesired and reveals the limit of of the driving capabilities of the output stages, the output signal is not fully reaching $\frac{-V_{ref}}{2}$ anymore, as long as the signal is symmetrical and continuous around the reference voltage, the frequency of the output signal can be determined.

7.3.2. THERMISTOR BASED TEMPERATURE SENSING CIRCUITS

The comparator based relaxation oscillator is re-used to read-out a thermistor based temperature sensor. When considering a thermistor, it should be noted that silicon carbide exhibits a negative TCR, thus yielding a decreasing resistance with increasing temperature. This is in correspondence with the TCR of n-type doped poly-crystalline SiC determined earlier in Chapter 5. The target specifications on the temperature sensing circuit are included in Table 7.3.

Possible layers to design the thermistors in are included in Table 7.4. Designing thermistors in any WELL-layer is undesired because a large voltage dependency of the resistance is yielded. This is due to depletion region width modulation. The x-WELL layers

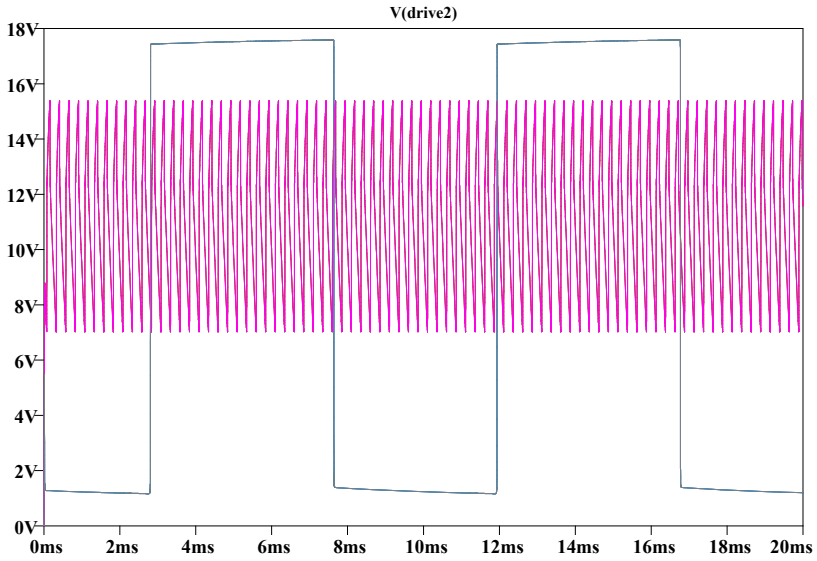


Figure 7.5: The simulated output voltage for R_{meas} of 100 kΩ (grey) and 1 kΩ (pink), C_3 of 40 nF, and at temperatures 25, 200 and 350 °C. Note the difference in amplitude between the low an high ohmic load. No influence of the temperature on the output frequency was observed.

Table 7.3: Target specifications of the thermistor based temperature sensor circuits. *The accuracy is further determined by the number of trimming points.

Figure	Value
Temperature range	20 °C to 400 °C
Resolution	0.5 °C
Accuracy*	1 °C
Bandwidth	1 kHz
Thermistor resistance	100 kΩ @ 25 °C
Transistor count	12 (comp.) + 6 (output stages)

are typically lowly doped, see also Table 7.4 yielding a large depletion region width compared to the SN and SP implantations. The depletion region width of the WELL-layers vary according to the bias voltage present. Thermistors will therefore be designed in the SN and SP layers.

Although the relaxation oscillator circuit is re-used, it will be fabricated specifically for the thermistor, removing the need for analog multiplexers of switches. Based on characterizations performed by FHG it is known that the SP layer shows a stronger temperature dependency up to 200 °C, because for the SN implantation both effects of decreased mobility by lattice scattering and the generation of free carriers work against each other below that temperature.

Because the relaxation oscillator has already been designed for the resistive read-out,

Table 7.4: Possible implantation layers for the thermistor design.

Layer	Doping concentration	Sheet resistance
N-well	5×10^{15} #/cm^3	n.a.
P-well	1×10^{17} #/cm^3	n.a.
N+	3.5×10^{19} #/cm^3	1.1 kΩ @ RT- 200 °C [14]
P+	4.5×10^{19} #/cm^3	40 kΩ @ RT; 10 kΩ @ 200 °C [14]

and because the thermistor based temperature sensing circuit is basically a combination with the designed thermistors, no additional simulations are carried out for this section. The thermistors will directly be designed during the layout phase and the target resistivity of both SN and SP thermistors is 100 kΩ. The thermistors will be included in both a two point and four point (Kelvin) measurement configuration in the PCM modules, enabling full characterization with reference measurement equipment such as source measurement units (SMUs).

7.3.3. PTAT BASED TEMPERATURE SENSING CIRCUITS

4 transistor constant g_m PTAT In addition to the thermistor based temperature sensing circuit, a PTAT temperature sensing circuit was designed. The schematic of this circuit is included in Figure 7.6. V_{GS} is a complementary to absolute temperature (CTAT) voltage, whereas V_{PTAT} a PTAT voltage. The PTAT effect occurs best at bias conditions that bring the MOS devices in weak inversion. An advantage of this 4 transistor PTAT circuit is that it is self-biased, not requiring external biasing currents. To investigate the performance of the 4T PTAT circuit a DC operation point simulation was carried out and the PTAT voltage was plotted against the simulated temperature, as is included in Figure 7.7. Although the PTAT voltage does not exhibit a linear relationship with temperature, the design is still included in the layout design. The simulated PTAT behavior can be explained by the immaturity of the delivered models.

5 transistor diode-based PTAT In addition to the 4T PTAT, a 5T diode-based PTAT is designed. In contrast the the 4T version, this circuit requires an external biasing source. The schematic of the designed circuit is included in Figure 7.8. Although no converging simulation was achieved, the circuit is included in the layout design.

7.3.4. UNIT-C BASED CAPACITIVE READ-OUT

In the context of smart integrated SiC sensors, a capacitive front-end read-out is a valuable addition to the SiC CMOS chip. Such a circuit would for example enable the read-out of a capacitive IDT structure as used in for the silicon gravimeter (see also Chapter

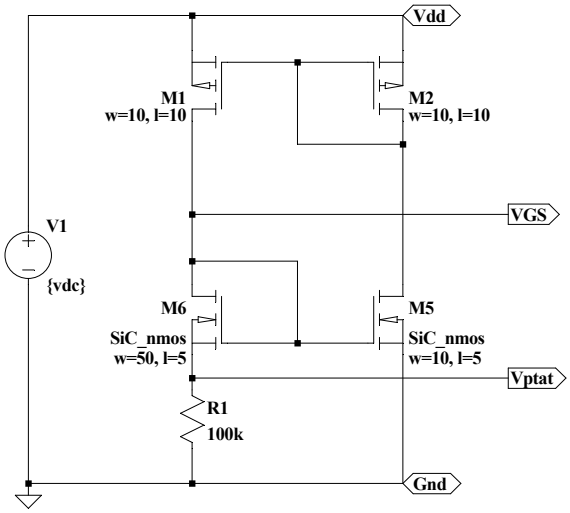


Figure 7.6: The schematic of the designed 4T PTAT.

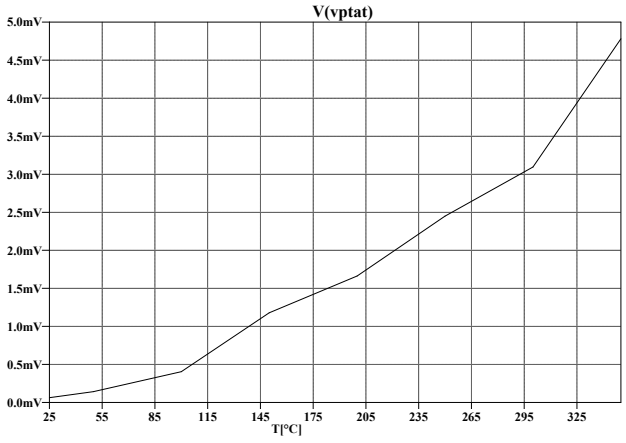


Figure 7.7: The simulated PTAT voltage as function of temperature.

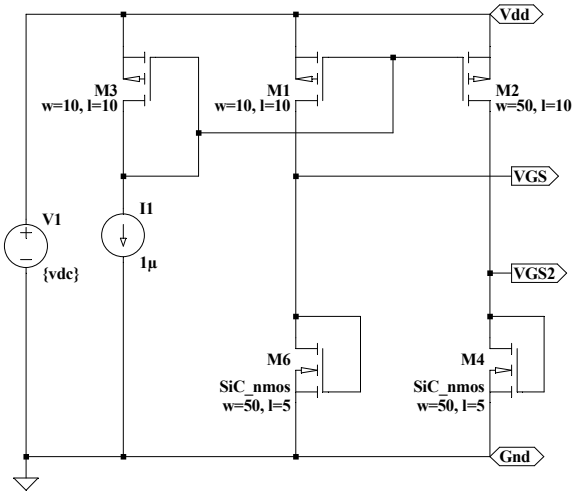


Figure 7.8: The schematic of the designed 5T PTAT.

3) or a capacitive pressure sensor, as was included in the design (see also Chapter 6). The circuit considered here is based on a unit-capacitor in combination with a counter and a clocked comparator. As starting point for the design of this read-out circuit, the sensor capacitance of the designed capacitive surface micromachined pressure device is used. Since the surface micromachined pressure device can be simplified to a parallel plate capacitance, it can be approximated by:

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \tag{7.2}$$

Filling out this formula for the smallest cavity height (without deflection) and knowing that the membranes vary from 100 µm to 1000 µm and that the cavity height ranges from 2.5 µm to 8 µm, the ideal range of measurable capacitance ranges from 11 fF up to 3.5 pF. Due to the large sizing of the transistors, a resolution of 100 aF is not feasible in the technology. The limiting factor is basically the charge injection caused by the passing gates which are used to transfer the charge from the sensing to the unit capacitor.
The size of the unit-C determines the maximally achievable resolution of the read-out circuit, and thereby determines the lower limit of the measurement range. The resolution is however limited to the charge injection caused by the gate capacitance of the pass gates M2 and M3. The gate capacitance was in the order of 30 fF. Taking into account the very conservative design rules of the technology used, the contribution of parasitic capacitances elsewhere in the circuit, for example originating from metallization traces and M1-poly cross-overs, it was decided to design a unit capacitance of 1 pF. This unit

capacitance equals basically the goal limit of the achievable resolution of the capacitive read-out, assuming that no oversampling is applied. To put this value in perspective, in a 180 nm technology a unit capacitance is 5 fF, when scaling and extrapolating this value a unit capacitance of 150 fF is obtained.

Table 7.5: Target specifications capacitive read-out based on unit-C circuit topology.

Figure	Value
Temperature range	20 °C to 400 °C
Capacitive meas range	1 pF to 100 pF
Resolution	1 pF
Accuracy	-
Bandwidth	1 kHz

CIRCUIT SIMULATION

The designed circuit has a clock with frequency of 500 Hz and an additional 'charge' signal which is used to control the initial conditions of the discharge capacitor. The basic operation of the capacitive read-out is the comparison between the capacitor to be sensed and the unit capacitor determining the resolution of the read-out circuit. Pass gates are connected between the ground and the unit capacitor and between the unit capacitor and the capacitor to be measured. These pass gates are controlled by digital logic generating non-overlapping signals based on the two clock signals. A clocked comparator compares the voltage over the sensed capacitor with the common mode voltage, yielding the number of counts before the sensed capacitor is discharged as measured for the sensed capacitance.

The schematic of the capacitance sensing circuit based on a unit-C is included in Figure 7.9. C_1 and C_2 represent the sensor capacitance and the unit capacitance respectively. Between both capacitors is M2 located, functioning as pass gate. To minimize the effect of charge injection, the NMOS transistors M2 and M3 are designed with minimal length and width, while taking into account robustness and minimizing the risk of any short channel effects. The length and width equal 5 µm and 10 µm respectively. Because M2 is performed in the BE processing in the EKL infrastructure, the size of the unit-C can be varied by changing the oxide layer thickness. By doing so, an optimum can be found between the achievable resolution and the limit caused by parasitic capacitances.

Component X1 is a clocked comparator of which its schematic is included in Figure 7.10, note that the output stages consist of 2 NOT and 2 NAND gates. A transient simulation of 50 ms was performed, in which a sensor capacitance of 10 pF is discharged with a unit-C of 1 pF. The voltages over the sensor capacitance, unit capacitance and the digital output signal are included in Figure 7.11. It can be seen from this Figure that the voltage

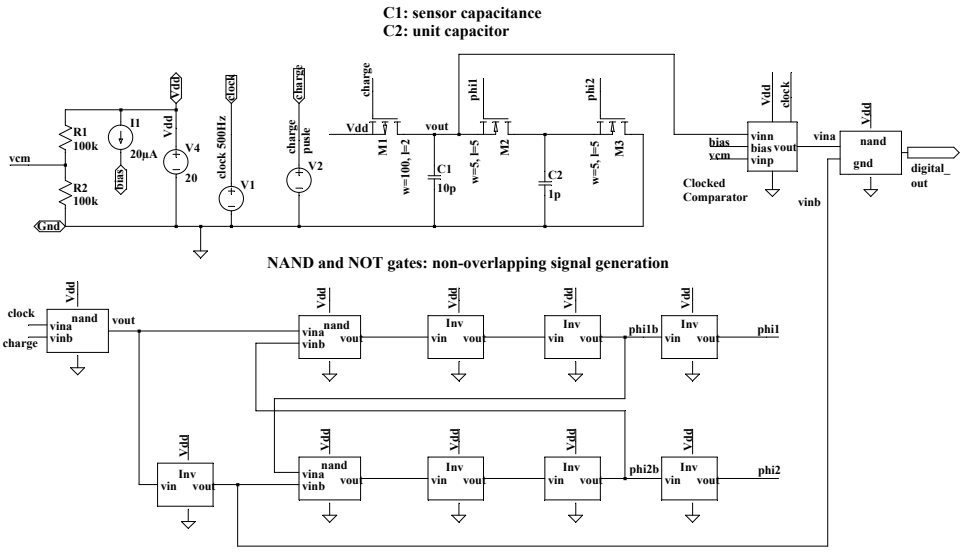


Figure 7.9: Schematic of the unit-C capacitance sensing circuit.

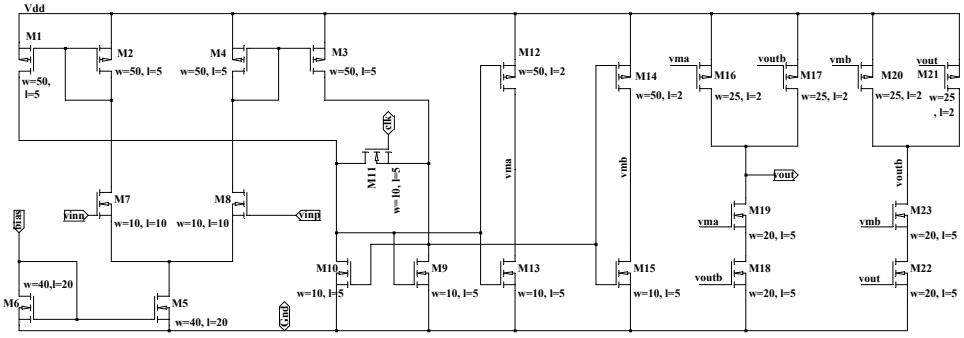


Figure 7.10: Schematic of the clocked comparator.

over the unit capacitor alternates continuously between the voltage over the sensing capacitor and ground, thereby discharging the sensing capacitor. The digital output signal (black line) is giving a count of the number of discharge cycles. Note further that as soon as the voltage over the sensor capacitance drops below the reference voltage at the input of the clocked comparator, the output voltage settles at V_{dd}.

7.3.5. RELAXATION OSCILLATOR BASED CAPACITIVE READ-OUT

In addition to the unit-C tank based capacitive read-out, the relaxation oscillator, since its output frequency is determined by the RC-time constant, can be used as capacitive

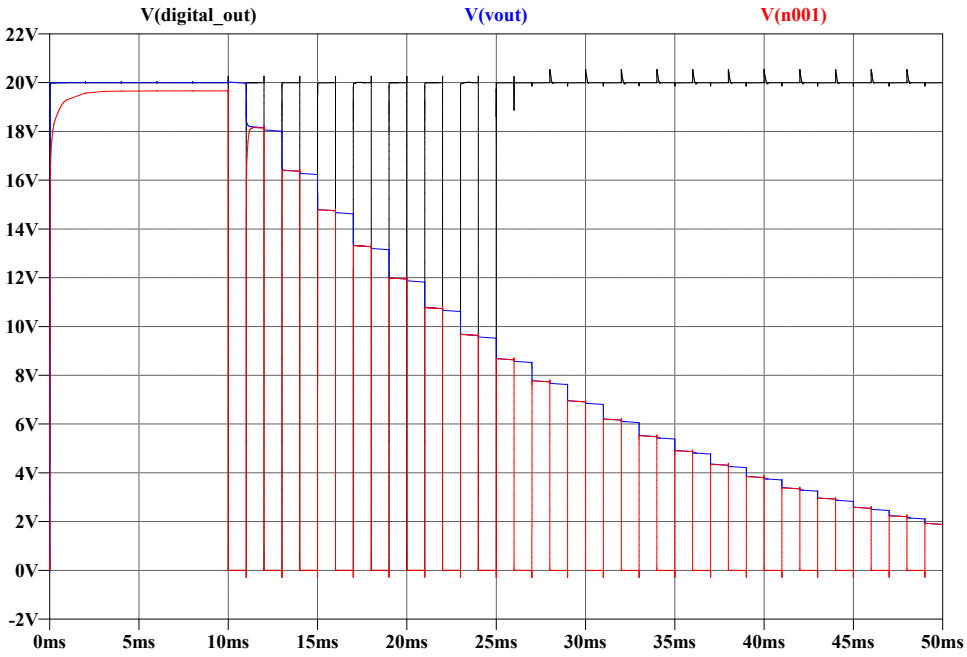


Figure 7.11: Simulation result for the capacitive simulation, the blue line represents the voltage over the sensor capacitance which is continuously discharged. The red line is the voltage over the unit capacitor and the black trace is the digital output signal. Note that once the voltage over the sensed capacitance drops below half the V_{dd}, the digital output signal settles at V_{dd}.

read-out circuit. In this case, the three resistors of the two feedback loops are off-chip, while the capacitor is the measured capacitance. The resistance in the lower feedback loop should be reduced to maintain the RC time constant and thus the same output frequency, because the capacitance is much smaller compared to the off-chip capacitor in the resistive read-out application.

7.4. CIRCUIT LAYOUT

In this section the details and design considerations of the layout design will be discussed. The layout was designed using L-edit, Tanner EDA from Mentor Graphics. The circuits designs from three researchers was integrated on the multi-project die.

7.4.1. LAYER OVERVIEW

According to the communicated design rules of FHG, a 'unit' NMOS transistor has been designed. A standard inverter was used to determine the width of both the NMOS and PMOS transistors. The ratio between N and PMOS was determined to be 4, where the

Table 7.6: Overview of the minimum pin-count.

Block	Cnt	Remarks
Resistive read-out relaxation oscillator	5	V_{in-}; V_{in+}(comp); drive2(output); I1(bias); V_{ref};
SN & SP Thermistor circuits	8	V_{in-}; V_{in+}(comp); drive2(output); I1(bias); V_{ref} (shared);
4T PTAT	1	V_{PTAT}
5T PTAT	4	V_{gs1}; V_{gs2}; I_{SRC}; I_{SNC}
Capacitive read-out unit C-tank	6	CHRG; CLK; I_{SRC}; I_{SNC}; V_{CM}; I_{SNC}; DGT
Capacitive read-out relaxation oscillator	5	V_{in-}; V_{in+}(comp); drive2(output); I1(bias); V_{ref};

PMOS is thus four times as wide as the NMOS. In this case, the switch over voltage in a standard inverter is 8 V at a V_{DD} of 20 V. Interestingly, when the PMOS/NMOS ratio is increased to 10, the switch over frequency equals only 10 V. At smaller PMOS/NMOS ratios the switch over voltage is thus much more sensitive, while at higher ratios a saturation effects occurs. The overview of the layers used in the circuit layout is given below. The align layer will be used for the alignment markers, followed by the NW and PW layers, the SN and SP layers. The active layer denotes where the 400 nm field oxide will be etched away. The poly layer denotes the poly-silicon layer used for gate formation and cross-overs in M1.

1. Align
2. NW
3. PW
4. SN
5. SP
6. Active
7. Poly
8. $CO_{M1\text{-}active}$
9. $CO_{poly\text{-}M1}$
10. M1
11. $VI_{M1\text{-}M2}$
12. M2
13. BO

There has been chosen to use poly for cross-overs with M1, instead of using M2 for this. The advantage is that the circuits do work without M2 back-end processing upon arrival from Germany, but the larger sheet resistance value of the poly layer should be taken into account, especially when long interconnect traces are considered. In a later stage, the interconnect in poly can be 'overdone' in M2, thereby reducing the sheet resistance. $CO_{M1\text{-}active}$ relates to the contact openings from M1 to the active regions, typically NW, PW, SN and SP. $CO_{poly\text{-}M1}$ denotes the contact holes from M1 to the poly silicon layer. VI denotes the via's between M1 and M2 metallization, whereas BO defines the open bondpad regions, in case a scratch protection layer is used in the back-end processing. An overview of the minimal required pins per sub-circuit in given in Table 7.6, assuming that the V_{dd} and GND are already supplied.

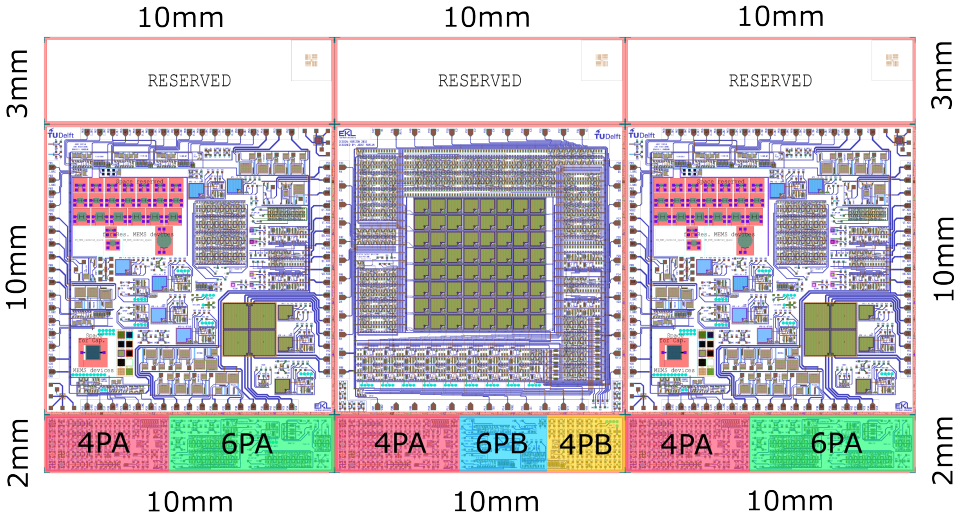


Figure 7.12: Topcell of the designed layout. Note the three different dies in A-B-A configuration, along with three different PCM designs giving room to 4 and 6 probe structures enabling wafer-scale characterization of test structures and (sub-)circuits.

7.4.2. TOPCELL

The topcell consists of an rectangular shape of 15 x 30 mm, in which 3 dies are identified of 10x 10 mm^2. 3 rectangles below are allocated for process control modules (PCMs) of 2 x 10 mm^2. There are different versions of 4 probe (4P) and 6 probe (6P) PCMs, annotated by versions A and B. The rectangles above the three dies are reserved for FHG, in which the alignment markers are placed. The three 10 x 10 mm^2 dies are identified as A-B-A, yielding two different designs, resulting in more dies of design A. Because die A houses many different circuits, the pin-out density is increased to 68 pins. During wirebonding in the standard packages it is determined which pins need to be connected. An overview of the topcell is included in Figure 7.12.

7.4.3. RELAXATION OSCILLATOR BASED RESISTIVE READ-OUT

Based on the simulated schematic, the layout of the relaxation oscillator was made. The comparator was designed first, as indicated in Figure 7.13. Because the left PMOS of the differential pair requires a crossover between M1 and POLY, the right PMOS of this differential pair has the same crossing to have resistance matching between both the current paths of the differential pair. Note further the presence of the current mirror on the left bottom of the circuit. Apart from a positive current which can be fed in to the circuit, the current sink path is routed to an outer pin, giving the possibility to sink a cur-

rent from the circuit in case the current mirror is not working correctly. A third biasing option would be to use voltage biasing on the common gates of the mirror circuit.

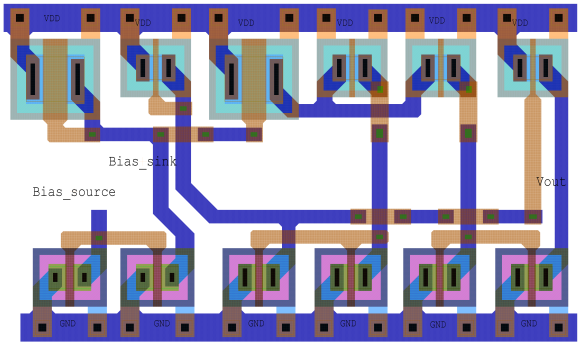


Figure 7.13: The layout of the comparator.

The relaxation oscillator is designed based on the continuous-time comparator. The large output stage is implemented by using a fingered layout-structure. When the standard way of designing the MOS devices would be used, the geometry would become very inconvenient for high density chip integration. The resistors are used to generate an on-chip reference voltage of V_{dd} divided by 2. The other two resistors are the resistors in the 'fixed' feedback loop of the circuit. The sensor resistance and the off chip-capacitor are not indicated here. The layout of the relaxation oscillator is depicted in Figure 7.14. To anticipate for the testing phase, adjacent to the relaxation oscillator on die A on-chip calibration resistors are integrated that can be connected via wirebonds. Alternatively, an off-chip RC components can be used.

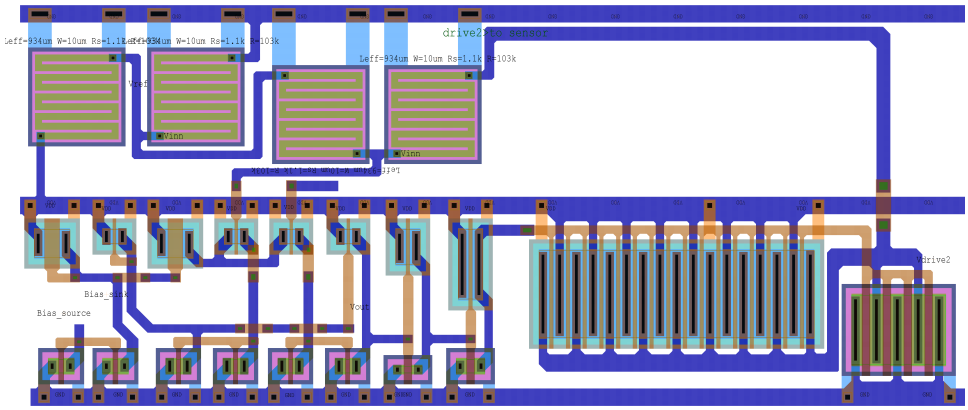


Figure 7.14: Layout of the relaxation oscillator.

Reference voltage In the layout of the relaxation oscillator, V_{ref} can be applied externally by an additional pin or by using two resistors in series. To facilite the second option, two 100 kΩ resistors are designed and included on the top left side of the relaxation oscillator, see also Figure 7.14. This large resistance value of 100 kΩ has been chosen to reduce the total standby power consumption of the chip, because the relaxation oscillator is designed four times on die A.

Calibration In order to be able to calibrate the resistive read-out, some known on-chip resistive loads are designed in the reserved space for the MEMS devices. These resistors are included in the PCM too, where they can be characterized both in two- and four probe measurements. The test resistors can be interfaced in M1 (for example when a contact aligner mask is used to connect different resistive devices to the read-out circuit per die) or by wirebonds, since six bond pads are included. The reserved space for pressure sensors and other resistive MEMS devices is approximately 3 x 4 mm^2.

7.4.4. THERMISTOR BASED TEMPERATURE SENSING CIRCUITS

Based on the relaxation oscillator as described above, two different thermistor based temperature sensing circuits have been designed, based on SN and SP thermistors respectively. The thermistors are on the same location as the piezo resistive sensor structures. The pin for the reference voltage is shared with the resistive read-out circuit, because all three circuits use a reference voltage equal to V_{dd} divided by two. The thermistors were designed based on the sheet resistance values communicated by FHG and described in the design section. The magnitude of the thermistors was determined to be 100 kΩ. Since the TCR of SiC is known to be negative and since the driving capabilities are limited, the designed resistance values yield a safe margin. Similar to the resistive read-out, the capacitor C_3 must be off-chip. An overview of the pins allocated for both the SN and SP thermistor based temperature sensing circuits is given in Table C.1, Appendix C.

7.4.5. PTAT TEMPERATURE SENSING CIRCUITS

The 4 transistor and 5 transistor PTAT circuits are designed, based on their circuit designs. The 5T PTAT makes use of a current mirror, where both the source and sink pins are routed out. In order to yield a PTAT voltage output, pin number 55 needs to be connected to an off-chip resistor.

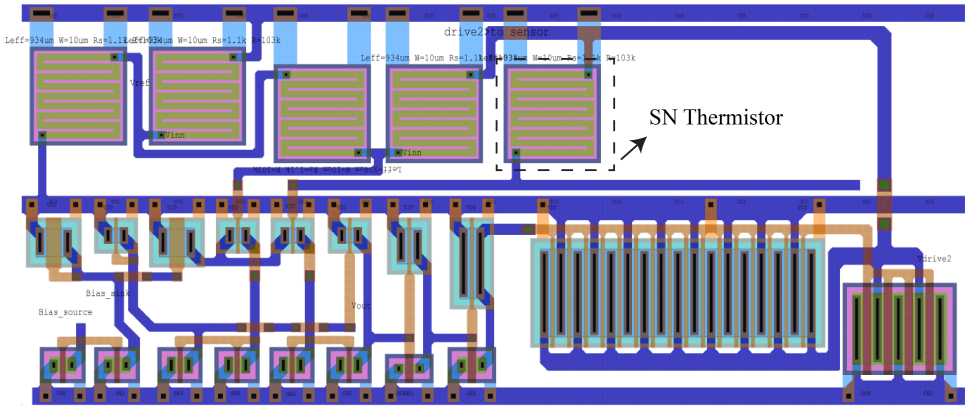


Figure 7.15: The layout of the relaxation oscillator with the SN based thermistor.

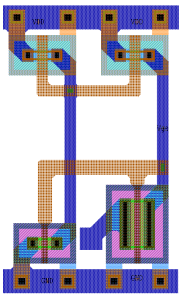


Figure 7.16: Layout of the self-biased 4T PTAT.

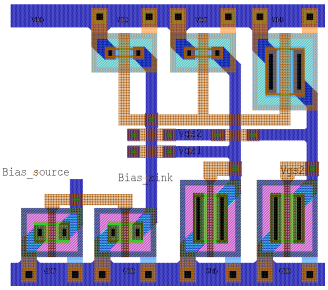


Figure 7.17: Layout of the 5T PTAT requiring external biasing.

7.4.6. UNIT-C BASED CAPACITIVE READ-OUT

Clocked comparator First, the clocked comparator was designed, where the differential pair with the current mirror can be identified on the bottom left of the circuit (Figure 7.18). The pass gate between the differential pair stage and the digital output stages is not connected to the ground with the guard ring. This can be recognized by the SN implantations being connected to the source pins of the differential pair transistors, instead of the ground. The last two stages of the clocked comparator are basically two NAND gates. The layout of the clocked comparator is included in Figure 7.18.

The unit capacitor was designed to be 1 pF based on two circular 500 fF MiM capacitors. To minimize charge injection effects, the pass gate transistors are designed with minimum length and width and are located close to the unit-C. The two 100 kΩ resistors are used to generate a reference voltage of half the V_{dd}, note the large SN implantation connecting the guard rings of these resistors to ground. On the left side of the layout, the

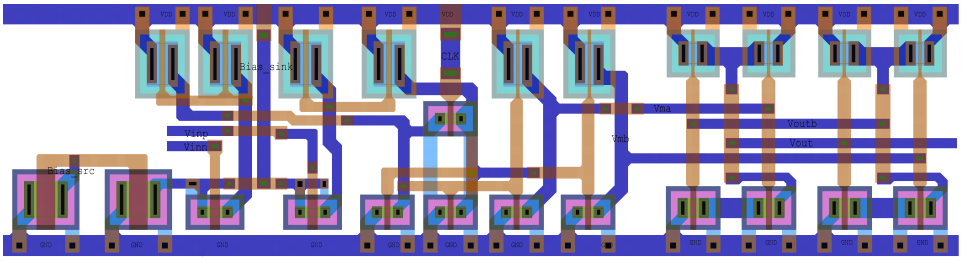


Figure 7.18: The layout of the clocked comparator.

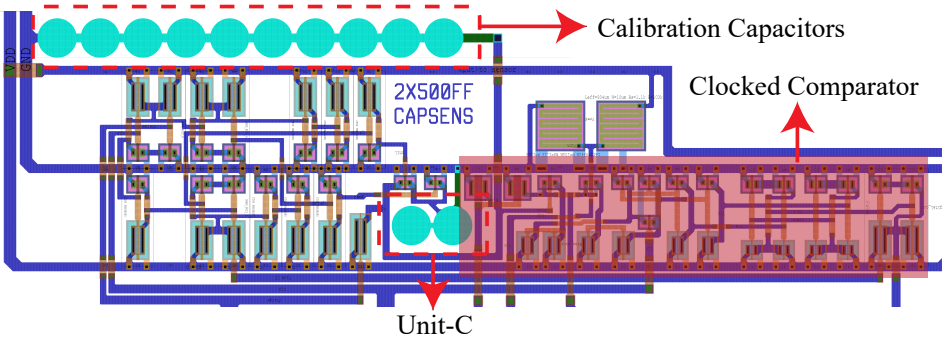


Figure 7.19: The layout of the unit-C read-out circuit.

digital part is included. External traces are used to carry the signals between different parts of the circuit. The width of these traces is increased to reduce total resistance, as well as the size of the contact openings to poly crossovers.

Calibration capacitors The unit-C capacitive read-out circuit can be characterized using on-chip test capacitors which are included in the reserved space for MEMS devices. The area reserved for capacitive MEMS devices is 1500 x 1633 µm, and an array of five 500 fF, yielding a total capacitance of 5 pF is included in this area, as annotated in Figure 7.19. Additionally, are these testing capacitors included in the PCM allowing separate characterization. The test MiM capacitors are interfaced by M1 and M2. The unit capacitor of 2 times 500 fF implies a digital output signal of five pulses.

7.4.7. RELAXATION OSCILLATOR BASED CAPACITIVE READ-OUT

In addition to the usage of the relaxation oscillator for the (piezo-)resistive MEMS devices and the thermistors, this circuit is included too for the purpose of capacitive sensing. Instead of the capacitor, in this topology the resistor is designed to be off-chip, and the capacitor is represented by the on-chip MEMS device. Also for this circuit, calibra-

tion capacitors are included in the design, namely ten times 500 fF adding up to 5 pF.

7.4.8. EXPERIMENTAL DEVICES AND TEST CIRCUITS

Strain gauges For health monitoring applications, strain gauges have been designed on the top left of the die. The geometry of these strain gauges is based on the available literature on the known gauge factor performance of mono-crystalline 4H-SiC [15].

MOS Devices with Metal Gates To investigate the performance of MOSFETs with metal gates, such devices have been designed and integrated on die A.

Test Squares for BE Processing In order to inspect the different layers during the back-end processing, for example while landing during a dry plasma etch, a rectangle with square openings in different layers is included on die A. The squares are big enough that the spotsize of the Leitz spectro-photometer can fit in. The annotations are drawn in the poly layer instead of M1, because part of the batch will not get M1 when they return from FHG.

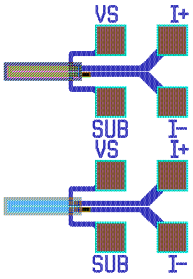


Figure 7.20: The layout of the SN and SP strain gauges.

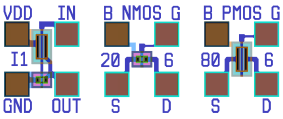


Figure 7.21: MOS devices with metal gates.



Figure 7.22: Squares with different layer openings to enable in-line process monitoring during back-end processing.

4P PCM structures The differently scaled NMOS and PMOS devices used in the analog circuits are separately included in the 4P PCM blocks. Additionally, the 500 fF and 2 pF capacitors are included as well as the 2000 µm output buffer and two current mirrors. An overview of the 4P PCM circuits is included in Appendix C.

6P PCM stuctures The clocked comparator, the time-continuous comparator, the relaxation oscillator and a stacked current mirror are included in the 6P PCM. The stan-

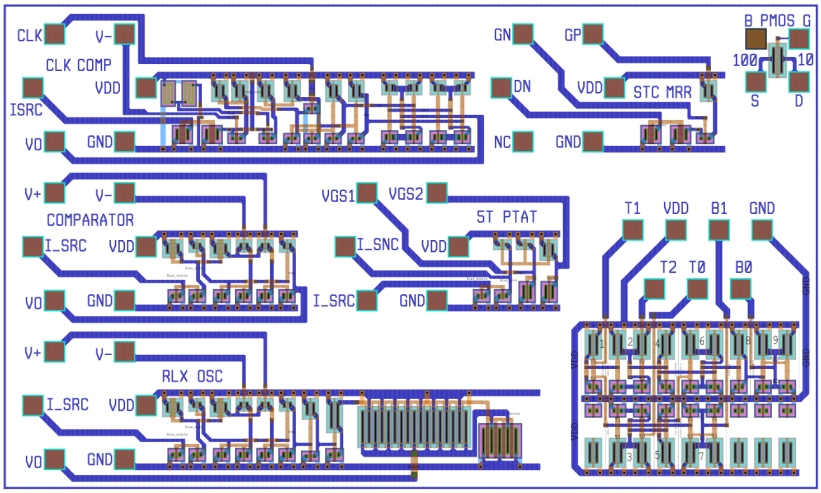


Figure 7.23: The 6 probe PCM.

dardized 6 probe configuration was maintained, enabling automated wafer scale measurements. The PCM is included in Figure 7.23. An overview of the 6P PCM circuits is included in Appendix C.

7.5. FABRICATION AND TECHNOLOGY ASPECTS

The fabrication of the designed multi-project die is carried out by FHG in its facilities in Germany. Close collaboration on intermediate fabrication decisions was maintained. It was for example decided to maximize the lithography steps in the contact aligner, because 4-inch compatibility of the wafer stepper got increasingly limited during the course of the fabrication. Moreover, it became clear by intermediate experimental results on ohmic contact formation, that the single-metal option for both n-type and p-type SiC would not be feasible due to too large contact resistances.

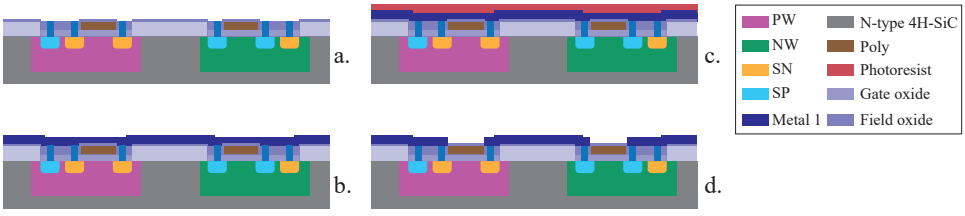


Figure 7.24: The process flow used during M1 fabrication in EKL.

7.5.1. SPLIT BATCH

To achieve the monolithic integration of the MEMS sensors with the SiC CMOS, the fabrication steps of the MEMS sensors need to be carried out at EKL. Because of contamination rules and thermal budget of aluminum (M1), the substrates that are going to be processed in EKL must come without M1. Out of the eight wafers that are going to be delivered by FHG, three wafers have poly and M1 interconnect, whereas the five other wafers only have the poly layers. The five wafers without M1 of the 'split-batch' are taken out of the process after the silicidation has taken place. The principle is that the metal used to for salicides (TiAl and NiAl) is fully reacted with the mono-SiC in the COs. The metal that has not reacted is etched away after the annealing salicidation process in a wet-chemical way. The three wafers which do come with M1, can thus not be used for BEOL MEMS processes that require high temperature steps, such as poly-SiC deposition (taking place at 860 °C in EKL). To still make use of the reserved MEMS area, devices that can be fabricated at a low thermal budget can be integrated.

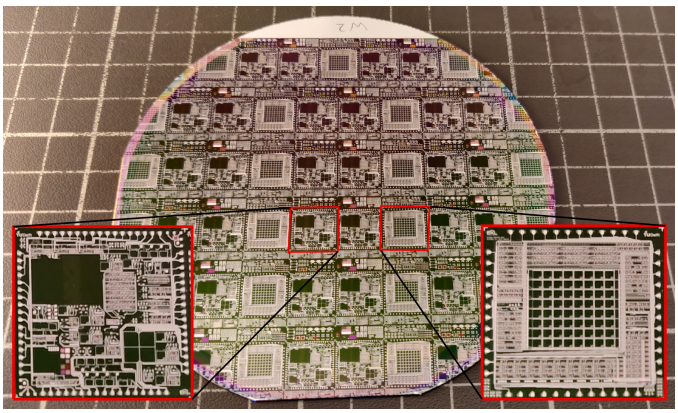
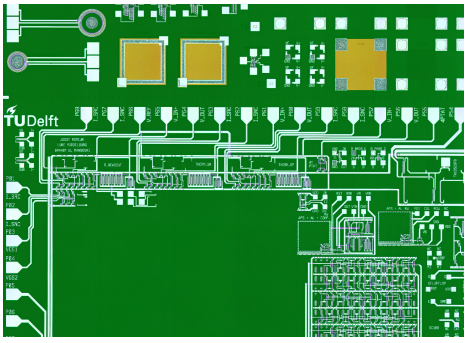


Figure 7.25: An waferview image after finalization of M1 fabrication. Note the zoom-ins of both die A (left) and die B (right).

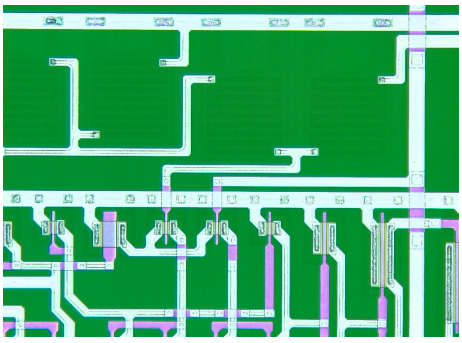
7.5.2. M1 FABRICATION EKL

One out of the five wafers was directly metallized in EKL based on the original M1 design. A multi-image reticle was designed based on both TUD and FHG designs. For the cleanroom fabrication, contamination aspects need to be taken into account, since 'red' metals were used for the silicidation process. A schematic illustration of the process flow is reported in Figure 7.24. As first step were the wafers cleaned twice in the SAL lab, using 99% HNO_3 and corresponding rinsing steps in between, where after the wafer is considered as semi-clean. Subsequently, 675 nm AlSi(1%) was sputtered on the

SiC process wafer and on two test wafers, that are used to characterize the lithography and dry-etching steps later on in the process. After sputtering, the wafers are coated with 2.1 µm AZ3012 PR, and the wafer were exposed with the nominal 340 mJ cm^{-2} and a focus offset of −1 µm. The alignment of the SiC wafer was highly non-trivial, due to the different locations of the ASML alignment markers and the different die pattern on the wafer. A custom exposure job was made, and, because no two opposite markers were present in the correct field of view of the automatic prealignment of the wafer stepper, the prealignment was performed manually. The wafer coordinates of a recognizable structure close to the original marker position were programmed as marker, that was used to manually align on using the manual prealignment recovery menu of the stepper. Standard single-puddle development was performed, no residues and no overlay offset was observed. The AlSi(1%) was etched by the Trikon Omega plasma etch tool, using a standardized recipe that makes use of endpoint detection. Due to the transparency of the substrate, a wafer handling error occurs during the unloading process, which can in turn be solved by using the manual mode of this tool. A picture of the wafer after finalization of M1 fabrication is included in Figure 7.25. Furthermore, results of inspection by using the Keyence profilometer are included in Figure 7.26, from which can be seen that the implanted SP and SN regions are only visible by laser inspection. The topography coverage of the M1 layer into the CO regions appears to be good.



(a) Inspection of the topleft of die A.



(b) Inspection of (part of) the relaxation oscillator. The faded pattern of the implanted SN and SP regions are made visible by laser inspection.

Figure 7.26: Inspection of the SiC CMOS wafer after finalization of the M1 fabrication using the Keyence Profilometer. These images are a combination of the optical and laser inspection.

7.5.3. DICING AND PACKAGING

Dicing experiments are successfully carried out on a 4H-SiC test wafer by using a dedicated dicing blade and the Disco dicing tool, as illustrated by Figure 7.27.

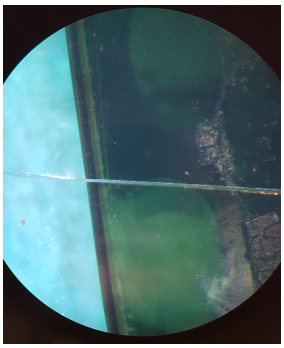


Figure 7.27: A dicing cut through a mono-SiC substrate, note the transparency of the SiC substrate.

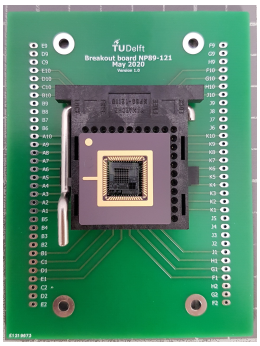


Figure 7.28: The PCB design to interface the SiC CMOS dies via headers array, ZIF socket and the PGA64 package. *The PCB has been designed by D. Kaandorp (Electronic Instrumentation Laboratory). Example die from J. Romijn in Si technology.*

In addition to wafer scale the characterization, the 10 x 10 mm dies can be wirebonded in a PGA64 package for flexible measurement setup design. This package has an outer ring of 64 pins, arranged in a grid of 10 x 10 pins with a spacing of 2.54 mm. A PCB was designed that houses a zero insertion force (ZIF) socket in which the PGA package can be placed. The PCB will feed the sockets pins to two headers arrays of 32 pins. A picture the die-package-PCB interface is included in Figure 7.28. Because the designed circuits and devices will be characterized at DC or within a low electrical bandwidth (< 10 kHz) no coaxial wiring such as BNC, SMA or triax was required to connect the PCB.

7.6. PRELIMINARY MEASUREMENT RESULTS

After M1 fabrication has been performed, preliminary measurements have been conducted. For these measurements, a Cascade (automatic) probe station has been used, in combination with an Agilent 4156c SMU. This omits the immediate need for dicing and packaging and has the merit of enabling automatic waferscale measurements. The temperature can be varied up to 200 °C while using up to seven needles to interface the probe pads. For characterization at temperatures beyond 200 °C, a different setup needs to be used, for example based on the Nextron micro probe station. However, the topic of characterization beyond 200 °C falls outside the scope of this thesis due to time constraints.

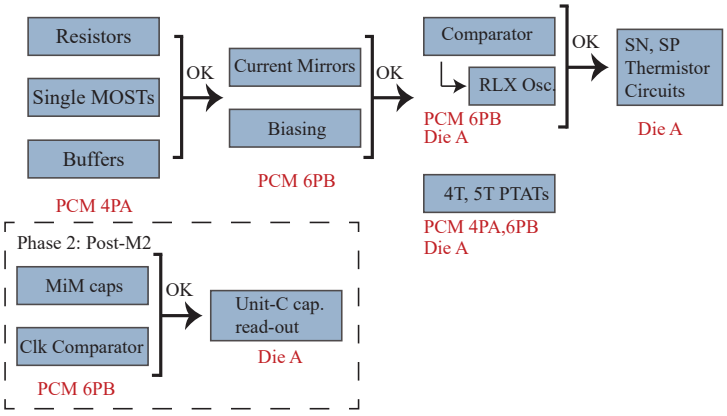


Figure 7.29: A schematic overview of the measurement plan to characterize the designed discrete devices, PCMs and circuitry. Die positions are annotated in red.

In the measurement phase, a 'bottom-up approach' is followed, starting from the discrete devices as included in the PCM modules. A schematic illustration of a measurement plan is included in Figure 7.29. The two main building blocks for the relaxation oscillator (used for resistive read-out) and the unit-C capacitive sensing circuit are respectively the continuous time- and clocked comparator. In order to assess the performance of the unit-C based capacitive sensing circuit, the MiM capacitors need to be present, thus requiring M2 metallization. The MiM caps need to be characterized initially to know their exact value for the unit-C and calibration capacitors present on die A.

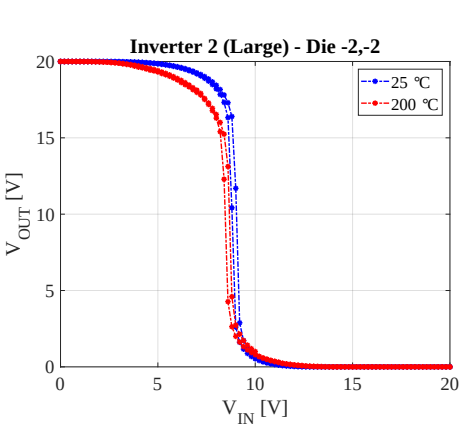
7.6.1. PROCESS CONTROL MODULE

The process control module (PCM) consist of many test structures, devices and subcircuits. A selection of the most relevant PCM contents is included in Appendix C. The characterization of discrete devices and structures such as resistors, MOSFETs and inverters can be performed on wafer scale in an automated way.

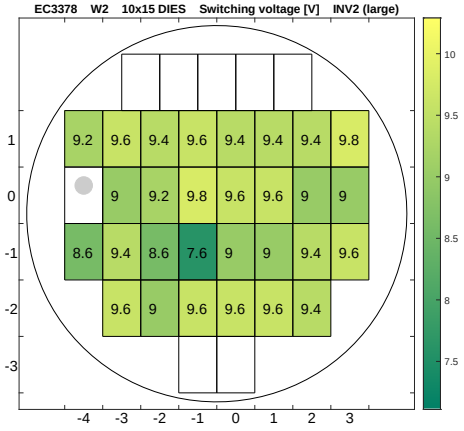
INVERTERS

Two different inverters have been included in the PCM-4PA: A smaller version (L=6 µm; W_P=80 µm, W_N=20 µm) and a larger version (L=6 µm; W_P=160 µm, W_N=40 µm). The input voltage is varied from 0 to 20 V while the output voltage is measured with a high-input impedance SMU. Ideally, the switching voltage would equal 10 V. In the analysis, this switching voltage is determined by determining where the current through the inverter is maximum. The input is varied from low to high and subsequently back to low,

to investigate any hysteresis effects. The input-output characteristic is included in Figure 7.30a and it can be concluded that the output swings fully from rail-to-rail, while hardly any hysteresis can be observed.



(a) The input-output characteristic for the larger inverter on die -2,-2 (L=6 µm; W_P=160 µm, W_N=40 µm) for both 25 °C and 200 °C.



(b) The measured spread of the switching voltage over the wafer for larger inverter on 25 °C, μ = 9.28 V; σ = 0.455 V.

Figure 7.30: Inverter characterization on PCM-4PA.

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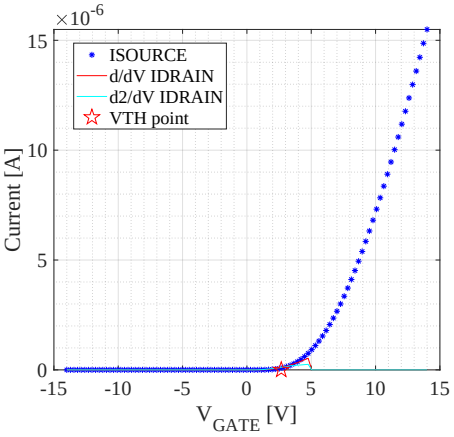
The wafermap shows a rather constant switching voltage over the wafer, as also illustrated by the standard deviation as reported in the caption of Figure 7.30b, except for one device and one broken device. The measurements results of the smaller inverter inverter are included in Figure D.1 in Appendix D. The waferscale result shows slightly more exceptions where the switching is voltage is in the range of 7.6 V to 8.6 V. In these cases, a weaker PMOS appears to be the cause, which is also represented by a decreasing 'high' voltage already before the switching voltage. The mean and standard deviation of the smaller inverter are μ = 9.26 V, σ = 0.652 V.

Waferscale measurements on both inverters were also performed at 200 °C to investigate operation. It was concluded that both inverter types are still fully operational at this temperature. A slight shift in the switching voltage was observed, as illustrated by μ = 9.19 V; σ = 0.360 V values of the waferscale measurements of the larger inverter at 200 °C. The input-output characteristic of the device at die -2,-2 is included in Figure 7.30a, where the slight shift can also be observed. Moreover, the 'high' level is decreasing already before the switching voltage. The wafermaps of both the smaller and larger inverter measured at 200 °C are included in Figure D.2 in Appendix D.

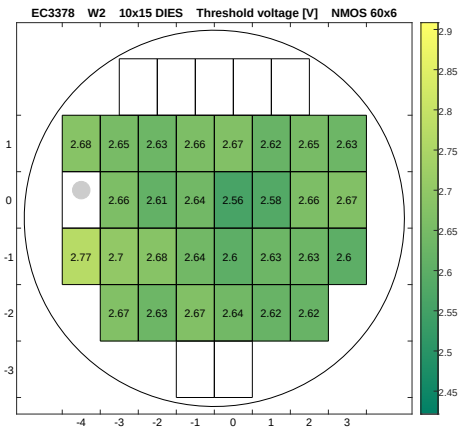
NMOS CHARACTERIZATION

In order to characterize the NMOS devices, a constant V_{DS} is applied of 0.2 V for the NMOS transistors, while the V_{GS} is varied from −15 V to 15 V. The threshold voltage is determined by determining the first- and second order derivatives of the drain current I_D with respect to V_{GS}. A tangent line is made where the second order derivative of $_{GS}$ is maximum. The intersection point with the x-axis the then identified as threshold voltage. During the measurements, both the source and drain current are measured, which should of course be equal. The current through the gate (I_{GATE}) and guard ring (I_{SUB}) are both measured to be zero for all the differently sized NMOS devices.

The I_D-V_{GS} curve for an NMOS transistor is included in Figure 7.31a. The first and second order derivatives of the drain current with respect to V_{GS} are included to illustrate the used method to determine the threshold voltage, that is annotated by a red star symbol. The variation of the threshold voltage over the wafer is illustrated by Figure 7.31b. The corresponding mean and standard deviation figures for the NMOS with this geometry equal $\mu = 2.64$ V and $\sigma = 0.0400$ V.



(a) The I_D-V_{GS} curve for an NMOS transistor (L=6 µm, W=60 µm).



(b) Waferscale, $\mu = 9.26$ V, $\sigma = 0.652$ V.

Figure 7.31: Characterization of the 60 x 6 µm NMOS as present on PCM-4PA.

To summarize the measurement results of all the analyzed NMOS devices, the mean and standard deviation of the wafer scale NMOS measurements are included in Table 7.7, in addition to the W/L ratio, the length, the width and the current at for an V_{GS} of 10 V. As can be expected, the mean threshold voltage is relatively constant for the different device geometries, where there appears to be a trend that the mean threshold voltage varies more for W/L ratios below 3.33. The observation that the threshold voltage is

stable even up to W/L ratios beyond 40 is beneficial for analog circuit performance. The drain current for a V_{GS} of 10 V for the smallest measured NMOS transistor equals 0.35 µA, while the NMOS measured exhibits 30 µA. Although the measured threshold voltages are constant, the threshold voltage deviates significantly from the circuit models. The threshold voltage as included in the circuit models equals 5.47 V at 25 °C, which is 2.87 V beyond the measured values.

Table 7.7: NMOS characterization results. **Current at 10 V of die -3,-2.

W/L	Width [µm]	Length [µm]	$\mu - \sigma$ - V_{TH} [V]	I_{Dmax}** [µA]	Remark
0.5	10	20	2.58 - 0.0354	0.35	PCM-4PB
1	10	10	2.55 - 0.0391	0.75	PCM-4PB
1.7	10	6	2.73 - 0.158	1.3	PCM-4PB
2	10	5	2.76 - 0.0990	1.6	PCM-4PB
2	40	20	2.91 - 0.0167	1.4	PCM-4PB
2	20	10	2.88 - 0.0360	1.4	PCM-4PB
3.33	20	6	2.61 - 0.171	2.2	PCM-4PA
4	20	5	2.57 - 0.0488	3.0	PCM-4PB
6	60	10	2.61 - 0.0287	4.2	PCM-4PB
6.7	20	3	2.56 - 0.0447	5	PCM-4PB
10	60	6	2.64 - 0.0400	7.5	PCM-4PA
10	50	5	2.58 - 0.0304	7.0	PCM-4PB
12.5	50	4	2.58 - 0.0299	9.0	PCM-4PB
42.7	250	6	2.62 - 0.0347	30	PCM-4PA

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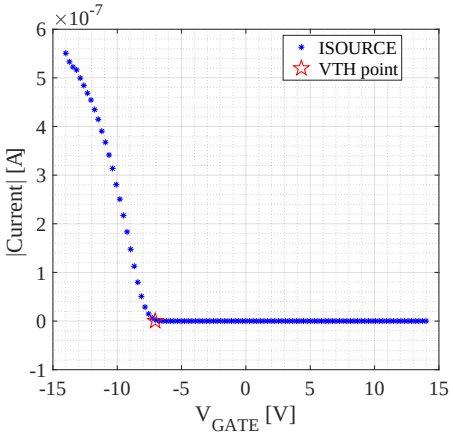
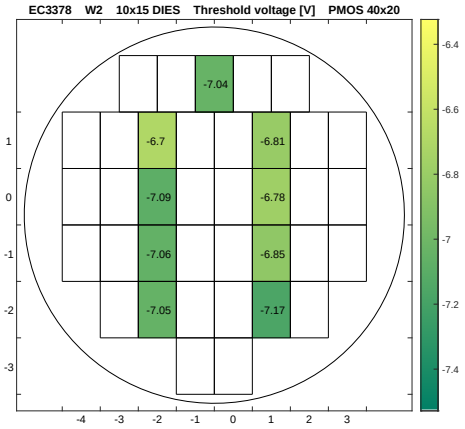
PMOS CHARACTERIZATION

Similar to the characterization to the NMOS devices, the PMOS devices are analyzed. A different DUT is used to control the SMU, since the PMOS is investigated in different biasing conditions. The V_{GS} is varied from −15 V to 15 V, although the mode of operation of the PMOS lays in negative range. After initial measurements, it was found that the drain current does not reach its maximum value for the applied biasing conditions, because the SMU switches over too early to the next measurement point. This effect manifested itself by a saturation effect for larger absolute V_{GS} voltages. The DUT used for the analysis of the PMOS was modified by increasing the delay per measurement point to 100 ms and by increasing the V_{DS} from 0.2 V to 2 V. The observed saturation effect and noisy drain current for larger absolute V_{GS} are indications that the driving capabilities of the PMOS are very limited ('weak'). Moreover, the rather large threshold voltage can introduce voltage headroom problems in the designed analog circuits.

The I_D-V_{GS} curve for an PMOS transistor is included in Figure 7.32, from which can be seen that the threshold voltage is around −7 V. When the waferscale result is considered, the variation in this threshold voltage can be considered small with σ = 0.166 V. To summarize the measurement results of all the analyzed PMOS devices, the mean



(a) The I_D-V_{GS} curve for an PMOS transistor (L=20 µm, W=40 µm).



(b) Waferscale, $\mu = -6.95$ V; $\sigma = 0.166$ V.

Figure 7.32: Characterization of the 40x20 micron PMOS as present on PCM-4PB for $V_{DS} = 2$ V.

and standard deviation of the wafer scale PMOS measurements are included in Table 7.8, in addition to the W/L ratio, the length, the width and the current at for an V_{GS} of -14 V. It can be concluded from this Table that the mean and standard deviation of the threshold voltage do not appear to be depending on the geometry of the PMOS devices. Additionally, the I_{Dmax} is not in line with all W/L ratios. More research is advised on the optimal measurement and biasing conditions for the PMOS devices. Similar to the NMOS devices, the threshold voltage of the PMOS devices differs substantially from the value as expected based on the circuit model. The threshold voltage for the PMOS that is included in the circuit model is -4.18 V, which is approximately 2.42 V lower than the measured values.

Table 7.8: PMOS characterization results. **Current at -14 V of die -2,-2.

W/L	**Width** [µm]	**Length** [µm]	$\mu - \sigma$ - $\mathbf{V_{TH}}$ [V]	$\mathbf{I_{Dmax}}$** [µA]	**Remark**
1	10	10	-6.48 - 0.322	0.01	PCM-4PB
2	40	20	-6.95 - 0.166	0.55	PCM-4PB
6.7	20	3	-6.60 - 0.185	0.24	PCM-4PB
10	50	5	-7.03 - 0.167	0.016	PCM-4PB
10	100	10	-6.71 - 0.167	0.043	PCM-4PB
12.2	25	2	-6.37 - 0.157	0.42	PCM-4PB
13.3	80	6	-6.75 - 0.221	5	PCM-4PA
25	50	2	-6.51 - 0.272	0.32	PCM-4PB
33.3	200	6	-6.72 - 0.213	23.5	PCM-4PA
41.7	250	6	-6.56 - 0.292	20	PCM-4PA
50	100	2	-6.32 - 0.330	0.29	PCM-4PB
83.3	500	6	-6.60 - 0.109	26	PCM-4PA

SHEET RESISTANCE - VDP

Van der Pauw (VDP) structures are included in the PCM for determination of the sheet resistance values of the SN, SP, PW, NW, poly and M1 layer. The voltage across the VDP structure is varied from −200 mV to 200 mV, while the current through the structure is measured. Simultaneously, the voltage drop over the VDP structure is measured with two other needles (Kelvin measurement). From these results, the sheet resistance can be determined by using equation 7.3 in which R_{MEAS} represents the measured resistance. This equation is basically a scaling with a correction factor to account for radial current flow and can only be used if design and realization of the VDP structure meets certain requirements.

$$R_{sheet} = \frac{\pi}{ln(2)} \cdot R_{MEAS} \tag{7.3}$$

The results on the sheet resistance measurements are based on automatic wafer scale measurements and the VDP structures for the SN, SP, PW, NW, poly and M1 layer are present on the PCM-4PA and therefore present on every die. The mean and standard deviation for the measured sheet resistances for all layers are included in Table 7.9. The measurements on the SP, NW and PW structures resulted in non-unambiguous results, since no voltage drop was measured over the structure. For the SP and PW, this can be explained by the design of the device in combination with the used biasing conditions. The current that is intended to flow through the VDP cross can flow directly to ground via the substrate. The p-implanted regions form a forwarded biased diode to the substrate, which is connected to ground again with an SN (n-type) guard ring. Investigation of the measurability of the SP, NW and PW VDP structures is considered as future work.

Table 7.9: Sheet resistance results based on wafer scale measurements of VDP structures on PCM-4PA.

Layer	μ - R_{sheet}	σ - R_{sheet}	R_{sheet} Target
M1	0.0500 Ω	0.0085 Ω	0.0394 Ω
Poly	14.0 Ω	0.139 Ω	14.0 Ω
SN	1.03 kΩ	0.009 28 kΩ	1.1 kΩ

CONTACT RESISTANCE - TLM

In order to determine the contact resistance, transmission line measurement (TLM) structures are included in the PCM-4PA. TLMs are based on a variation between two contacts, between which the resistance is measured of the layer of interest. A linear fit is performed through the data points, and the contact resistance is derived by dividing the intersect point with the y-axis by two (two contacts are present in the current path). In this section, the contacts to M1 are considered to NW, PW, SN, SP and poly. For the same

reason as described above in the discussion on the VDP structures, the measurements on the PW and SP based TLMs do not result in useful data. The results on the NW, SN and poly are summarized in Table 7.10. The measured contact resistances are in line with the expected results and the comparison between the NW and SN results is in line with the dependency on the dopant concentration.

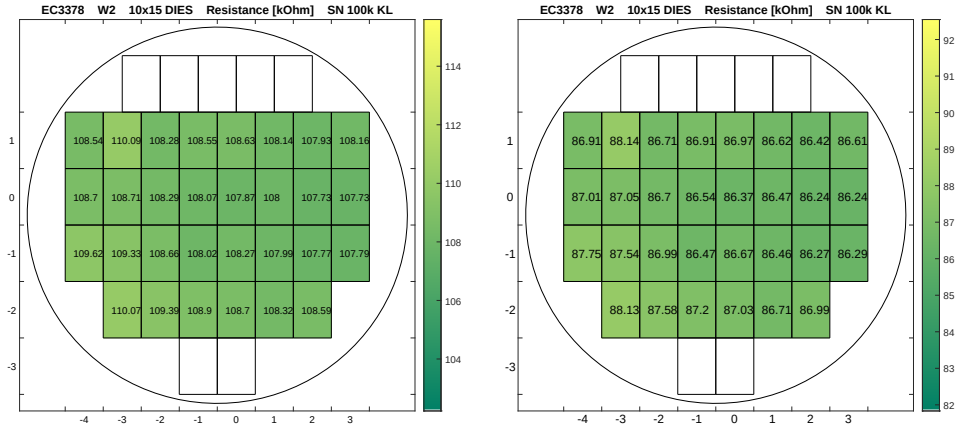
Table 7.10: Contact resistance results based on wafer scale measurements of TLM structures on PCM-4PA based on square contacts of 20 x 20 µm.

Layer	μ - $\mathbf{R_c}$	σ - $\mathbf{R_c}$
NW-M1	1.75 mΩ cm^2	0.0533 mΩ cm^2
SN-M1	0.331 mΩ cm^2	0.0480 mΩ cm^2
Poly-M1	0.058 mΩ cm^2	0.0406 mΩ cm^2

MONOLITHIC RESISTORS

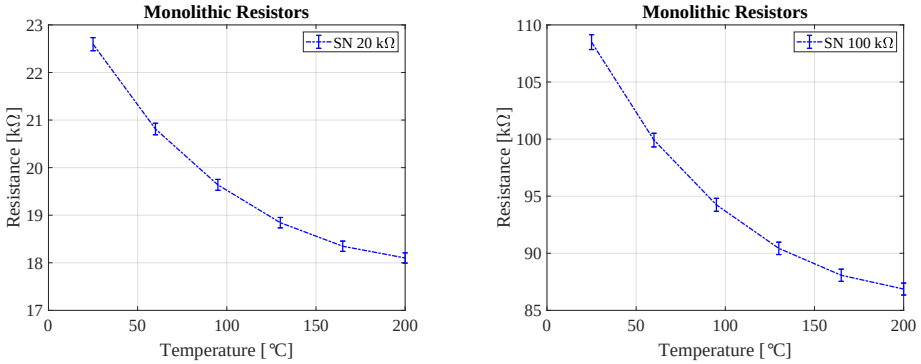
The designed monolithic resistors are essential for the operation of the designed circuits, they are for example present in the feedback loop of the relaxation oscillator or because they are used to generate on-chip reference voltages. Both a four-point (Kelvin) as a two-point version of the 20 kΩ and 100 kΩ resistors are included in PCM-4PA. The two-point versions are included because the circuits do 'see' the resistors in this way, the contact resistance do add up in this case, but would not be measured in a Kelvin measurement. The latter one will however result in an accurate measurement of the resistance of the serpentine monolithic resistive structure itself.

SN resistors The SN resistors are characterized from 25 °C to 200 °C to investigate the temperature dependency and to assess their feasibility as thermistors. The Kelvin measurements revealed mean (wafer scale) measured resistances of 22.60 kΩ and 108.5 kΩ for the 20 kΩ and 100 kΩ resistors at 25 °C respectively. The measured values are close to the designed values, taking into account the uncertainty in the communicated sheet resistance values and the process variations present. The non-Kelvin (2-point) measurement revealed mean (wafer scale) measured resistances of 23.12 kΩ and 109.6 kΩ for the 20 kΩ and 100 kΩ resistors at 25 °C respectively. As can be expected, these measured values are slightly larger compared to the Kelvin structures due to the added contact resistances. The results of the waferscale measurements of the 100 kΩ resistors (4-point) for 25 °C and 200 °C are included in Figure 7.33. In correspondence with other wafer scale measurements, a small gradient of the measured resistances is visible over the wafer. As can be expected based on the known negative TCR, the resistance of the SN resistors is decreasing with increasing temperature. The temperature behavior of the SN resistors is represented more explicit by Figure 7.34.



(a) T = 25 °C. **(b)** T = 200 °C.

Figure 7.33: Comparison of the wafermap of the Kelvin-measured monolithic SN resistors of 100 kΩ for different temperatures.

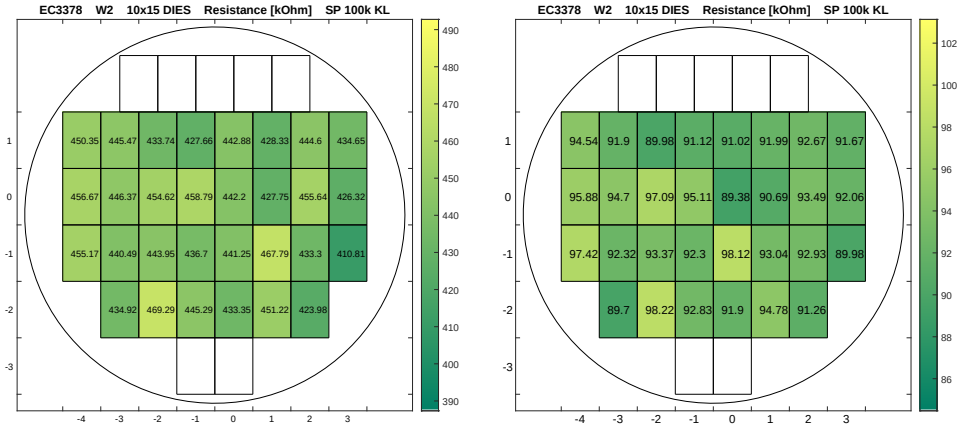


(a) For the 20 kΩ thermistor. **(b)** For the 100 kΩ thermistor.

Figure 7.34: Temperature behavior the the monolithic resistors. The data points represent the mean resistance of 30 waferscale measurements, while the error bar represents 1σ.

SP resistors Similar to the SN resistors, the SP resistors were characterized from 25 °C to 200 °C. The wafer scale measurement results at 25 °C and 200 °C are included in Figure 7.35. It can be concluded from this result that the measured resistance is a much stronger function from the temperature and that the spread over the wafer is appears to be rather random, unlike the SN resistors where the resistors varied in a more gradual way. The design of the 100 kΩ SP resistor was based on the sheet resistance values as communicated by FHG, as also described in Table 7.4 (40 kΩ @ RT; 10 kΩ @ 200 °C). Because it was known right from the start that the SP layer exhibits a strong tempera-

ture dependency, the SP resistor was designed to be 100 kΩ for the lowest sheet resistance value available, namely 10 kΩ at 200 °C, which approximately one fourth of the room temperature value. This corresponds well with the measurement results, which are summarized by Figure 7.36. From the resistance/temperature graph it can be concluded that the SP resistor is indeed roughly four times smaller compared to its value at 200 °C, which is with 90 kΩ in acceptable agreement with the intended value.



(a) T = 25 °C. **(b)** T = 200 °C.

Figure 7.35: Comparison of the wafermap of the Kelvin-measured monolithic SP resistors of 100 kΩ for different temperatures.

7

CURRENT MIRROR CHARACTERIZATION

Separate current mirrors are included in the PCM blocks, that will be measured to test their performance. Of particular interest is the mirror based on two NMOSTs with a length and width of 6 µm and 20 µm respectively and on a PMOST with length and width of 20 µm and 40 µm, because this mirror is used in the continuous time comparator (on which the resistive read-out is based). In contrast to the configuration of the current mirror in the comparator, the gate voltage of PMOS M10 can be controlled manually.
The injected current into the drain of NMOS U2 was kept constant, whereas the voltage on the gate voltage on the PMOS was varied from 8 V to 18 V, which translates to a V_{GS} on the PMOS gate of −2 V to −12 V. Simultaneously, the current through the VDD is measured, thus the mirrored current. This sweep was performed for injected currents of 1 µA, 100 nA and 10 nA. The result of this measurement is included in Figure 7.37. It can be concluded from this results that for a large gate voltage on the PMOS (small absolute voltage), the current is dictated by the NMOS transistors. With increasing voltage, the current is pinched by the PMOS. The transistion voltage for a bias current of 1 µA equals

10 V. For a bias current of 100 nA, this transition voltage equals approximately 12 V. The measurement for a bias current of 10 nA yields a transition voltage of 13 V.

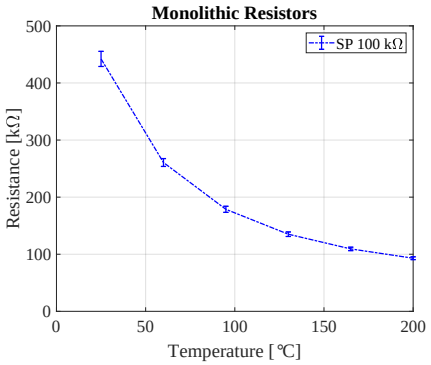


Figure 7.36: Temperature behavior the 100 kΩ monolithic SP resistor. The data points represent the mean resistance of 30 waferscale measurements, while the error bar represents 1σ. Note that the spread decreases significantly with increasing temperature.

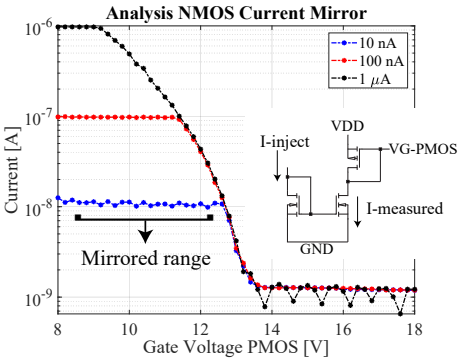


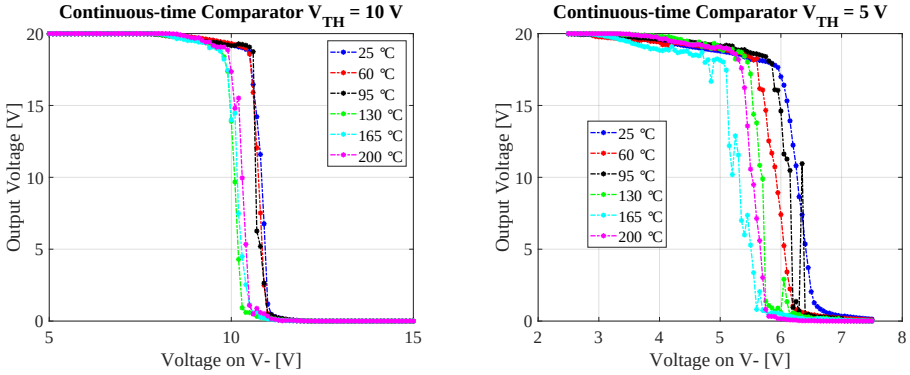
Figure 7.37: Characterization of the NMOS current mirror based on the PMOST with length and width of 20 µm and 40 µm. The gate voltage on the PMOS was varied for three constant injected currents. The ranges where the current is 'mirrored' can be clearly distinguished.

The transition voltage of the mirrored current behavior is of importance for the operation of the comparator circuit. The input transistors of the differential pair should ideally operate in their saturation regime, where they exhibit a linear sensitivity to the applied V_{GS}. The voltage on the node where sources of both input transistors come together should ideally be large, thereby resulting in a large V_{DS} of the input transistors while bringing them in the saturation regime. The transistion voltage indicates the voltage drop over the PMOS transistor of the current mirror when the circuit is biased with a certain current. As a result, the bias current directly influences the voltage headroom of the differential input pair. From these results, it can be concluded that for a decreasing bias current, the voltage drop over PMOS M10 is reduced. It can be concluded from this Section that the large threshold voltage of the PMOS transistor negatively influences rail-to-rail output behavior of the comparator.

7.6.2. CONTINUOUS-TIME COMPARATOR

The continuous-time comparator is the main building block for the relaxation oscillator that is used for the resistive read-out circuit. This comparator is located both on PCM-6PB and on die A. Single-die measurements were carried out on the PCM-6PB version by using the Cascade 33 probe station to interface the SiC wafer. The voltage on the inverting terminal was sweeped from 5 V to 15 V while the voltage on the non-inverting

terminal was set to a constant value of 10 V, functioning as threshold voltage. The circuit was biased with a constant current of 1 µA and the output voltage was measured for different temperatures ranging from 25 °C to 200 °C in steps of 35 °C. The used biased current resulted in a voltage drop of 4.97 V over the NMOS of the current mirror at 25 °C and in a drop of 2.74 V at 200 °C.



(a) For a V_{TH} of 10 V. **(b)** For a V_{TH} of 5 V.

Figure 7.38: The output signal of the continuous-time comparator for temperature from 25 °C to 200 °C.

The measured output voltage of the comparator is for different temperatures is included in Figure 7.38a. It can be clearly seen that there is an offset voltage of the comparator with respect to the threshold level of 10 V and that this offset is not constant for all temperatures. Generally speaking, the offset voltage reduces with increasing temperature. The weakness of the PMOS is again expressed by the reducing output voltage already before the switching point. It is envisaged as future work to investigate the cause of this offset and if different bias conditions could reduce this offset level.

A similar characterization has been performed for a threshold voltage of 5 V, whereby the input voltage on V- is sweeped from 2.5 V to 7.5 V. The result of these measurements is included in Figure 7.38b. For this operating conditions, the reducing output from the 'high' level before the switching moment is even more expressed. Additionally, the switching from 'high' to 'low' is less abrupt when using this decreased threshold voltage level.

7.6.3. CLOCKED COMPARATOR

Analog to the continuous time version, the clocked comparator was characterized. Thanks to the different topology, the compromised voltage headroom due to the large channel resistance of the PMOS appears to be less problematic here. The clocked comparator

under test was the version as included in the PCM-6PB. Due to the limited amount of pins (six), two SN 20 kΩ resistors were designed to bias the input of the non-inverting input terminal to $\frac{V_{DD}}{2}$. These 20 kΩ resistors were chosen, because the limited area between the supply and ground rail did not allow the integration of the 100 kΩ resistors be included. As a result, more power is consumed to generate the reference voltage on the V+ terminal, functioning as threshold voltage.

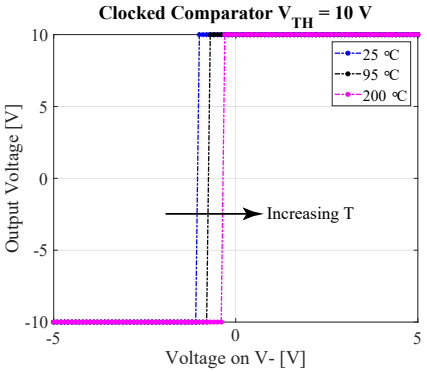


Figure 7.39: The output signal of the clocked comparator for temperature from 25 °C to 200 °C.

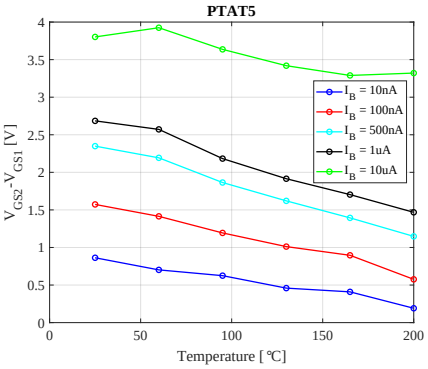


Figure 7.40: The measured V_{GS2}-V_{GS1} (V_{PTAT}) for temperatures ranging from 25 °C to 200 °C for different bias currents.

7

The circuit was designed for a square clock signal alternating between ground and V_{DD}. The clock was generated by an Agilent 6613C signal generator that did not allow an offset voltage of 10 V when a V_{PP} is used of 20 V. To circumvent this, the ground was set to −10 V and the VDD to 10 V. The circuit was biased with 1 nA and, similar to the continuous-time comparator, the voltage at the input terminal was ramped up from −5 V to 5 V. The clock signal used initially was 100 kHz to achieve an accurate reading of the offset voltage. Measurements were carried out at 25 °C, 95 °C and 200 °C. The input/output voltage characteristic is included in Figure 7.39. It can be concluded from this result that a solid rail-to-rail output signal can be observed and that the switching behavior is more abruptly compared to the continuous-time comparator. Another difference is that the output voltage is steady at its high- resp. low level, whereas in the continuous-time version, the output voltage is deviating already before the switching moment.

The results further indicate that the clocked comparator works at least up to 200 °C, while even demonstrating a lower offset voltage. The cause of this offset is seen as topic for future research. A possible explanation could be that the reference voltage is not exactly equal to $\frac{V_{DD}}{2}$, due to mismatch of both restive paths from the SN 20 kΩ resistors to the ground and V_{DD} rails.

7.6.4. PTAT5

The PTAT5 circuit measured was included on PCM-6PB and requires only an external current biasing source. The bias current was swept in a logarithmic way from from 10 nA to 10 µA to investigate different bias conditions. This current is negative in sign since the current sink bias connection was used. The current source connection (that was included in the circuit for redundancy reasons) was set to 0 V to make sure that the NMOS devices of the current mirror are not conducting and would disturb the biasing. V_{GS1} and V_{GS2} are measured with varying temperature. The difference between both voltage should be a PTAT voltage. Initial measurements show that V_{GS2} is larger than V_{GS1} as is expected from the differently scaled PMOS devices. The result for a selection of bias current is included in Figure 7.40. Although a linear trend of the measured voltage difference is observed with increasing temperature, the slope is negative, thus CTAT instead of PTAT. The results show that the most linear behavior is achieved for bias currents in the range of 0.5 µm to 1 µm. The voltage change over this temperature range equals for example 1.20 V for the bias current of 500 nm, while a smaller bias current results in a smaller voltage change over temperature. A preliminary conclusion is therefore that the implementation of a standardized circuit in silicon technology, is not trivial for this experimental 4H-SiC CMOS technology.

7.7. CONCLUSION AND FUTURE OUTLOOK

The fourth goal as discussed in Section 1.6 is implemented by the designed circuit and devices in this Chapter. Achieving CMOS circuitry in mono-SiC as starting point for the development of ASICs is a key step toward smart integrated sensors in SiC technology. One way to make SiC sensors smart, is to (monolithically) integrate electronic circuits that can read-out the impedance change of for example the pressure sensors as discussed in Chapter 6. Different essential circuits for (MEMS) sensor read-out were designed, such as capacitive and resistive read-out, in addition to thermistor and PTAT temperature sensing circuits.

Because the circuit design was based on preliminary circuit models, the transistor count per circuit has to be minimized to let the model uncertainty not hinder circuit operation. To improve the understanding of the SiC technology used, a broad range of different MOS devices was included in the PCM modules. Apart from what has been described in this work, photo diodes (of different designs) and digital building blocks such as memory cells, logic gates and even an ADC were included. The layout was performed manually based on documented design rules and features all circuit designs of the multi-project effort.

It can be concluded that due to the smaller mobility values in mono-SiC, the design rules are more conservative compared to state-of-the-art silicon CMOS technologies. As a consequence, larger MOS devices are needed as compared to conventional Si CMOS. These increased geometries do come however at a price, larger parasitic capacitances, which in turn limit operational bandwidth of the circuits. Integration of larger MOS devices results typically in a multi-fingered layout structure in a conventional V_{dd} and GND railed design. Larger circuits cause the interconnect (mostly in M1) to bridge larger on-chip distances. To enhance conductivity of this interconnect, generating an additional trace in M2 on top of the M1 traces or poly-crossovers results that both traces would be in parallel, thereby importantly reducing the equivalent sheet resistance.

Major part of the fabrication was carried out in the facilities of Fraunhofer IISB, with M1 fabrication carried out at EKL. Characterization of the VDP and TLM structures resulted in respectively sheet resistance and contact resistance figures that were in correspondence with earlier experience by FHG. The temperature characterization of the designed on-chip resistors does exhibit resistance values that are in line with the design of the serpentine structures at room temperature. Among SN and SP resistors, the SP versions show a larger resistance change over temperature, a property that favors the usage of SP resistors as thermistors.

Measurements further reveal that both NMOS and PMOS devices are operational. However, the measured threshold voltages are not in correspondence with the circuit models, the measured $V_{TH,N}$ is around 2.87 V lower than the theoretical one while $V_{TH,P}$ is 2.42 V larger than the value included in the circuit model. In general, the large $V_{TH,P}$ is disadvantageous in analog circuitry, since it compromises the available voltage headroom. The operation of the designed current mirrors was verified, whereby the large voltage drop over the PMOST was standing out. The corresponding limited driving capabilities were thereby shown during the characterization of the continuous-time comparator.

Both differently scaled inverters do work as expected at both 25 °C and 200 °C. At this temperature a slight decrease in switching frequency was observed. The continuous-time comparator was tested successfully in the temperature range from 25 °C to 200 °C, whereby the offset voltage exhibits a decreasing trend with increasing temperature. The clocked comparator works as expected in the range from 25 °C to 200 °C with a more abrupt transition between the two digital levels as compared to its continuous-time counterpart. The PTAT5 circuit was measured, but did not perform as expected, even though a linear voltage dependency was measured as function of temperature. The working electronic circuitry up to 200 °C in 4H-SiC, both in the analog and digital do-

main, is an promising starting point for further development of smart integrated SiC sensors.

With the main building block (comparator) of the relaxation oscillator working, future work still includes testing and characterization of this oscillator that enables on-chip resistive read-out. The verified operation of the building block of the unit-C read-out (clocked comparator) is a good starting point to further characterize this capacitive sensing circuit. For these measurements, M2 metallization is required to implement the MiM capacitors. Regarding the technological aspects, the accuracy of the circuit models would be in need of further improvement, especially when analog circuit design is aimed for. Furthermore, the discrepancy of the threshold voltage, the limited driving capabilities and the origin of the offset voltage in the two comparator types are topics for future investigations. Finally, long-term harsh environment compatibility testing is also seen as future work.

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8

CONCLUSIONS AND RECOMMENDATIONS

THIS chapter summarizes the main conclusions that can be derived from the work in this thesis, while considering the goals as postulated in Section 1.6 which are illustrated by Figure 1.4.

8.1. SILICON BULK MICROMACHINED DEVICES

When bulk micromachining of silicon wafers is pushed to the limits of feasibility, as is for example illustrated by the realized gravimeter, process variations start to play an essential role. When bulk micromachined beams are to be realized with widths of only several micrometers, variations on the width of only tens of nanometers start to become highly significant. Based on this realization, bulk micromachined spiral resonators were designed and realized on wafer scale. It can be concluded that wafers scale fabrication resonators featuring high aspect-ratio beams (functioning as springs) with a width of only 20 µm can be performed. Measurements showed that measured eigenfrequencies are in correspondence with the simulations within a range of 0-10%. The deviation in reference frequency among different resonators can be used to quantify the variations in through-ethed beamwidth, caused by the process window.

To demonstrate what can be achieved by combining inventive design choices with state-of-the-art Si technology and the concept of system integration, an integrated miniaturized MEMS gravimeter was developed. High mechanical sensitivity can be achieved by exploiting non-linear buckling behavior of long slender bulk-micromachined silicon beams. The high mechanical sensitivity results in this case in a resonator with a small

operational bandwidth (sub 10 Hz) which is in line with the application as gravimeter. In addition to the challenges in the design and realization of the mechanical design, system integration aspects were exhibited as enablers for smart integrated sensors. The lateral isolation makes the integration of the bulk micromachined capacitive transducer possible, while maintaining the advantages of lithographic resolution. The integration of the non-linear buckling-based compliant mass/beam systems with the bulk micromachined capacitive transducer leads to a concept for a high resolution MEMS based gravimeter. The sensitivity of the integrated capacitive read-out transducer was tested to be 2.55 aF nm^{-1}. Combining the lowest resonance frequency, the capacitive sensitivity and combined noise sources in the system, a theoretical system resolution of 17.02 ng/$\sqrt{Hz}$ is achieved. The proof of concept is promising to yield a low-power, miniaturized and integrated MEMS solution for high-resolution acceleration measurements. In conclusion, it can be mentioned that that existing Si technologies gives ample room for novel high-impact transducer and sensor designs.

Recommendations regarding Integration

- In order to enhance fabrication convenience of the gravimeter, a larger die size would give room for a larger mass, relaxing the constraint on the beam width.
- Next-level integration would be on die level, where the impedance read-out ASIC is integrated with the gravimeter die, thereby yielding a System-in-Package (SiP) solution. Such a concept would further improve system performance, thanks to reduced parasitic impedance caused by wirebonds and resulting noise caused by electromagnetic interference (EMI). Monolithic integration of the ASIC with the MEMS device would require compatibility of fabrication processes of the MEMS and silicon CMOS technologies. Furthermore would this require the availability of a silicon CMOS process that is sufficiently mature to design the precision analog impedance read-out circuit in.

8.2. POLY-SIC SENSORS

The usage of polycrystalline SiC offers significant benefits over monocrystalline SiC, especially for the fabrication of MEMS and microsystems. Throughout multiple projects, properties of different versions of poly-crystalline SiC were characterized such as bulk electrical resistivity, residual stress, deposition rate, optical transmission and refractive index. There is a large degree of control on the properties of the poly-SiC layers, aiding design freedom. On the other hand, keeping the process variation under control

maintains demanding.

The unique combination of high temperature compatibility, transparency and electrical conductivity was exploited for the realization of suspended heatable poly-SiC windows with a thickness of only 500 nm. These windows are intended to be used as first step toward optical measurement techniques to measure the particle mass- and number- concentration in the tailpipe of an internal combustion engine powered vehicle. These windows were demonstrated to stay clean upon soot exposure when heated. Furthermore, the self-cleaning property by thermal oxidation of carbon contamination was shown, without permanent visual deformation or damage of the membrane. The regeneration experiments beyond 500 °C without observable damage illustrates the high temperature compatibility of the 500 nm thin membrane. Successful presentation of both the contamination prevention by thermophoretic repulsion as the thermal oxidation of carbon contamination is a key step toward the application of optical instrumentation for exhaust gas monitoring. In addition to the application in particle sensors, the concept of the transparent harsh environment compatible window can be used for other optical sensors, such as gas sensors.

Contacts that show an ohmic behavior at RT can be made on lightly to moderately doped poly-SiC layers by hot-sputtering only, using AlSi(1%) or titanium. AlSi(1%) contacts show ohmic behavior up to 500 °C, whereas the contact resistance for the Ti/SiC interface starts differ (maximally a factor of 2) across opposing biasing directions, suggesting Schottky behavior from 100 °C and beyond. Absolute pressure sensors were designed and realized based on a self-sensing concept. The reported negative gauge factors in literature were confirmed. Successful operation of the realized absolute pressure sensors was shown, featuring the self-sensing membrane concept. A single pressure device was characterized and a logarithmic response of $\frac{\Delta R}{R}$ at varying pressure was measured. The characterized half Wheatstone bridge behaves linear from atmospheric down to 2000 Pa and behaves logarithmic below this pressure.

In addition to the piezoresistive pressure sensors, Pirani gauges were realized to yield physical orthogonality, i.e. having the possibility of two different transducer types to measure pressure. The TCR of different poly-SiC layers was characterized and it was concluded that the TCR is negative and increasing with decreasing doping concentration. The largest measured absolute value for the TCR occurred for a lowly doped poly-SiC layer (0.75 sccm NH_3). The use of poly-SiC combines the favorable properties such as a useful TCR, high mechanical stiffness and compatibility with high temperatures and harsh environments.

The realized Pirani gauges can achieve a length of 1000 µm without any mechanical sup-

porting structure to prevent buckling. Gauges with dissimilar geometries were characterized at room temperature and a 1000 µm long gauge was measured from RT up to 750 °C. The gauge shows a reproducible response to varying pressure. Mechanical buckling whereby the suspended beam touches the substrate did not manifest itself during characterization up to 750 °C.
In conclusion, the electrical, optical, mechanical and thermal (TCR and high temperature operation) properties of poly-SiC were exploited for the realization of three harsh environment sensors. Significant advantages related to microfabrication are the in-situ doping, the relaxed requirements on annealing, the tensile residual stress, the conformal deposition and the good etch-ability. The harsh environment compatibility is illustrated by repeatable operation beyond 600 °C for the PM sensors and Pirani gauges.

Recommendations regarding Poly-SiC Sensors

- Due too the negative TCR, leakage current starts to occur through the membrane layer of the optically transparent SiC windows. A trade-off exists between maximum transparency (minimum extinction in the window layers) and the mechanical and electrical performance. It can be concluded that a dielectric layer is required between the heater and membrane layer to prevent leakage currents and undesired self-heating of the membrane layer caused by these parasitic currents.
- Due to fabrication complication in the time frame of this work, one iteration of the piezoresistive absolute pressure sensors was realized. Although operation was confirmed at room temperature, abnormalities were measured at elevated temperatures. Modifications in the fabrication process should be investigated to improve device performance, such as additional annealing steps, different etch times, tuned doping concentrations and layer thickness variations.
- Although workable reproducibility was achieved in terms of achieved poly-SiC layers, the nature of the deposition process makes these layers prone to variations induced during the deposition process.
- Performing lithography over high topography structures is non-trivial. The usage of dedicated chemically amplified photoresist extends fabrication feasibility compared to traditional photoresist. Nevertheless, the maximum cavity height is still limited by the lithography step when spin coating is used. Investigation to use different patterning techniques could increase the achievable maximum cavity height.
- Although the longest Pirani gauge exhibits desired device behavior up to 750 °C,

some of the gauges showed abnormal device behavior beyond this temperature. Although more research into this effect is needed, explanations could be mechanical buckling, a sign change of the TCR and self-heating effects due to Joule heating, causing the temperature of the gauge to be poorly defined.

- Harsh environment assessment of the realized devices in terms of corrosive environments and long-term high-temperature operation.

8.3. SiC CMOS Electronics

Although in the field of power electronics, the usage of crystalline SiC is mature, the development of low-voltage high-density analog and mixed signal SiC CMOS can be seen as premature. Only a few institutes worldwide have realized SiC CMOS circuits in technology nodes ranging from 1.0 µm to 1.2 µm. In collaboration with Fraunhofer IISB, a multi-project SiC CMOS chip was designed, fabricated and tested. From the circuit design phase, it can be concluded that the immature circuit models imply a minimum transistor count for the used topologies. This reasoning is amplified by the high-substrate and process cost, requiring careful risk management. This also explains the conservative design rules communicated, based on which the layout was designed from scratch. Nevertheless, effort was taken to efficiently use the available die area and output pins. Due to smaller mobility values in mono-SiC compared to Si, much larger devices are required to drive output pins or feedback loops compared to to state-of-the-art silicon CMOS technologies. The larger geometries do come however at a price, larger parasitic capacitances, which in turn limit operation bandwidth of the circuits. Integration of larger MOS devices results typically in a multi-fingered layout structure in a conventional V_{dd} and GND railed design. Because of the immaturity of available SiC CMOS technologies and the physically lower mobility of charge carriers in crystalline SiC, miniaturization is not (yet) one of the targets when designing SiC CMOS circuitry.
The preliminary characterization reveals technological parameters that are in line with results as expected based on earlier experience with FHG, the circuit models and the available literature. The threshold voltage deviations and the large voltage drop over the channel of the PMOS devices are standing out and could complicate (analog) circuit performance. The temperature dependency of the monolithic resistors enables their usage as thermistors. The normal and clocked comparator versions are tested successfully up to 200 °C. While these two circuits are the main building blocks of the relaxation oscillator and unit-C discharge circuit, the results on the two comparators are a promising outlook for the resistive- and capacitive read-out circuits. Moreover, measurements indicate that the inverters are operational from 25 °C to 200 °C and that the PTAT5 volt-

age show a linear relation with temperature, although its behavior is CTAT. A preliminary conclusion is therefore that the implementation of a standardized circuit in silicon technology, is not trivial for this experimental 4H-SiC CMOS technology.
The added value of SiC CMOS circuitry comes mainly from operational compatibility at temperatures far beyond 200 °C, which is beyond the operating regime of state-of-the-art silicon electronics. This favorable property and the demonstrated results in this thesis are an important basis for further development of the integrated smart silicon carbide sensors for harsh environment applications.

Recommendations regarding SiC CMOS development

- Further investigations in the technological parameters are recommended to form an elaborated basis for comprehensive understanding of SiC CMOS circuit behavior.
- Long term stability and reliability of SiC CMOS electronics are still subjects for future research. Known potential failure mechanisms are ohmic contacts, metallization and gate oxide stability upon extended exposure to elevated environmental temperatures.
- The accuracy of the circuit models would be in need of further improvement to enable more effective circuit designs.
- Development of Layout versus schematic (LVS) checks for the Fraunhofer SiC CMOS technology.

A

APPENDIX-A

A.1. IMPEDANCE SPECTROSCOPY ON A RESISTIVE PM SENSOR

A.1.1. MOTIVATION AND BACKGROUND

In addition to the research toward optical measurement techniques for soot mass- and number concentration measurement, extended functionality of existing soot sensors is explored in this section. The resistivity particulate matter sensor is a simple device that transducers the presence of soot through impedance change across inter-digital electrodes (IDEs). Information provided by impedance spectroscopy at frequencies ranging from 100 Hz to 10 kHz is investigated. Resistive PM sensors, also referred to as conductometric soot sensors, encompass a category of devices composed of inter-digitated electrodes (IDE) supported on ceramic substrates. Upon exposure to a soot containing gas flowing over the sensor surface, soot particles are deposited and a conducting path is formed between the IDE. As soot accumulates on the IDE, the sensor develops an idiosyncratic response; there is a long period of time where the device displays no signal because soot has not yet bridged the IDE. It is notable that this behavior creates ambiguity about the presence of soot aerosol. The amount of time that it takes generating the signal is inversely proportional to the cumulative amount of soot on the IDE. Thus, lower soot concentrations require longer delay times for generation of a signal and confirmation of a DPF leak. Following verification of DPF health, subsequent measurements may

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Parts of this Appendix have been presented on the IEEE 29th International Symposium on Industrial Electronics (2020) [2]

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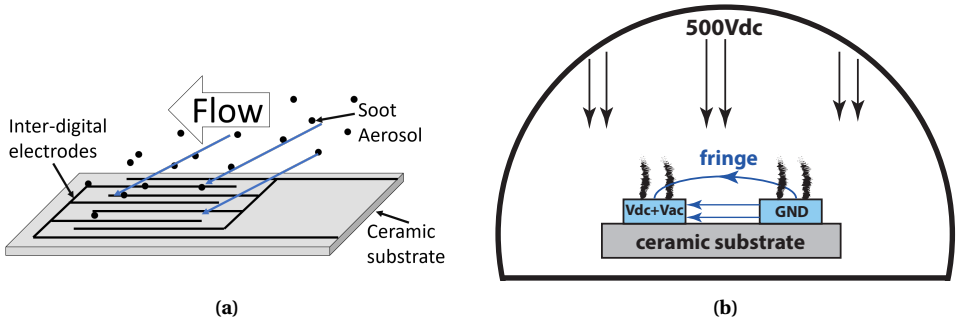

Figure A.1: a) Schematic diagram of resistive PM sensor construction; the inter-digitated electrodes are supported by a ceramic substrate. The electrodes are held at different electrical potential, and the electric field between the electrodes and metal housing enables electrophoretic soot capture. b) Schematic diagram of electric field orientation around an IDE pair including in-plane and normal components. Soot particles move along field lines and are captured on the electrodes. The particles assemble into dendrites which also follow field lines.

be performed after burning off accumulated soot via an integrated heater.

It is desirable to decrease the amount of time required for diagnosing a leaky DPF at a given soot concentration in order to increase the frequency of DPF characterizations and to decrease exposure to damaging contaminants [3] while electrical potential is active on the IDE. Acceleration of the response time of resistive PM sensors has been investigated through optimization of applied bias [4]. Increased bias leads to increased electrostatic soot capture and therefore faster response. Unfortunately, increased bias also leads to Joule heating of the deposited soot bridges [5]. As the deposited soot undergoes self-heating it creates a thermophoretic force that reduces deposition, leading to a limitation in sensitivity enhancement with increased bias [6]. Response time reductions have also been investigated through application of small device modifications and alternative measurement modes such as capacitance [7] and parallel resistance [8]. Despite these efforts, the presence of the typical delay in the shape of the signal in resistive soot sensors is inevitably caused by the way of operation.

Therefore, the goal of this section is to explore the potential of impedance spectroscopy for measuring the full IDE impedance over a frequency range between 100 Hz and 10 kHz in an attempt to achieve improved sensitivity, a reduced response time or additional information on the PM size distribution.

A.1.2. MODELING

In this section the interaction between the particle-containing gas flow and the sensor structure is modeled. The structure used in this work is a modified version from a com-

mercially available resistive soot sensor with IDE fingers. The bare substrate with the IDE's is put in a custom-made flow housing to which an optional high voltage can be applied, yielding a vertical electrical field with respect to the surface of the substrate. This vertical electrical field is intended to verify the effect on capacitive soot sensitivity. Images of the used sensor are included in Fig. A.3b, including the assembled structure with flow housing to which a high-voltage can be applied for generating a controllable vertical electric field. A more schematic representation of the sensor structure and flow housing is shown in Fig. A.2. As can be noted, there are two different electrical fields: a lateral field between the IDE fingers and a vertical electrical field with respect to the electrodes introduced by the high voltage, applied to the housing. For simplicity both field are drawn orthogonally. To investigate the behavior of soot deposition and deposited dendrites as function of the orthogonal electric field, the magnitude of both fields can be varied. In addition, the IDE structures can be excited with both DC bias voltages as well as AC sinusoidal voltages by using an impedance analyzer.

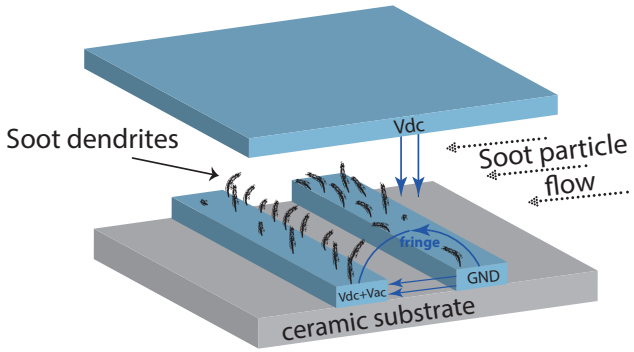

Figure A.2: 3D drawing of the concept of free-standing soot dendrites on the IDT fingers, bending in the fringe components of the horizontal electric field.

The simple equivalent circuit model considered for modeling is a parallel resistor and capacitor, where the resistor is a lumped element representing the distributed resistivity between the electrodes, while the parallel capacitor is a lumped element representing the distributed capacitance between the electrodes. It should be noted that models based on quantized, kinetic descriptions of dendrite growth, such as those in [9] and [6] are available for predicting the dynamic behavior of resistive PM sensors. Nevertheless, the simple RC-section is chosen here, because it allows a description of the sensor performance in electrical parameters. The raw impedance data $|Z|$ and θ is mapped on this equivalent circuit and can be used to evaluate which component is more suitable for measuring deposited soot.

A

The proposition explored here is that the physical mechanisms of the changes in IDE resistance and capacitance are different in nature. The increased capacitance over time is assumed to result from gradual vertical dendrite growth on top of the electrodes, while the resistance is reduced by dendrites which are growing in-plane in the lateral direction. The change of these two passive elements over time can be used for indirect experimental validation of the proposition.

PARALLEL RESISTANCE

The parallel resistance is determined by the grown soot dendrites between both IDE's. Each dendrite crossing the IDEs can be considered as a resistance much smaller than the air bulk resistivity. Although the resistance of each crossing dendrite is different, one could state that the resistance can be described in terms of statistical parameters and there would be an average dendrite-bridge resistance R_o.
After the first bridge results $R = R_o$ and after the second bridge formed in $R = \frac{Ro}{2}$.
During deposition, these resistive bridges are continuously formed, resulting in an increasing number of equal-value resistors in parallel, thus a linearly increasing conductance. For a large number of bridges and a constant interval between subsequent bridges, the change of total measured parallel resistance R is described by the following equation.

$$R_{eq} = \frac{R_0}{n} \tag{A.1}$$

Where R_{eq} is equal to the equivalent measured resistance, R_0 to the average dendrite-bridge resistance and n to the number of dendrites.

PARALLEL CAPACITANCE

Soot particles flowing over the flow housing that contains the substrate with the IDE structure are subject to several forces, such as thermophoretic forces and gravitational forces, but also to electrostatic forces. As a result, a proportion is deposited on the sensor surface and contributes to the growth of dendrites in a direction that is, amongst others, influenced by the local electric field. With the dendrites being on top of the IDE electrodes, the tip of the dendrites are assumed flexible and can move in the varying fringing electrical field lines of the lateral electrical field, caused by the AC excitation on the IDE. By doing so, the charge is moving in the electrical field, thus contributing to the relative permittivity, thereby increasing the measured parallel capacitance. The growth and movement of the soot agglomerate and dendrites increases the relative permittivity. To calculate the effect of the dendrites on the ϵ_r the polarization P needs to be determined.

$$P = \frac{dp}{dV} = \frac{dq \cdot x}{dV} \tag{A.2}$$

Here dV stands for the volume portion of the airspace over the sensor, including the dendrite, carrying a charge of dq. As the dendrites bend due to the time-varying local electric field because of the AC excitation, the dV section moves by x in the fringing fields of the electric field across the IDE fingers.

$$dq = N \cdot dV \cdot q_{avg} \tag{A.3}$$

Where N represents the number of the grown dendrites on top of the IDE fingers and q_{avg} represents the amount of charge per soot dendrite. The displacement of the dendrite, and its dV section, is due to electric force and depends on its mechanical rigidity, which can be expressed as an effective stiffness K_{eff}.

$$F_E = qE = K_{eff}x \tag{A.4}$$

Substituting the equations above the polarization becomes:

$$P = Nq_{avg}x = \frac{Nq_{avg}^2 E}{K_{eff}} \tag{A.5}$$

The resulting relative permittivity can be calculated from electric displacement.

$$D = \epsilon_0 E + P = \epsilon_r \epsilon_0 E \tag{A.6}$$

$$\epsilon_r = 1 + \frac{Nq_{avg}^2}{\epsilon_0 K_{eff}} \tag{A.7}$$

The relative permittivity increases with the number of the dendrites growing over the IDE and the square of the average charge of the dendrites. This increase in effective permittivity results in a measurable increase in the IDE's capacitance.

A.1.3. EXPERIMENTAL

The influence of electric field strength and orientation on the resistive PM sensor is investigated through optical microscopy and impedance spectroscopy. Soot aerosol is generated with a Jing miniCAST 5201c which burns propane in a diffusion flame to reproducibly create a particle size distribution with a mean geometrical mobility diameter near 80 nm. The aerosol is subsequently diluted with nitrogen in a Dekati FPS 4000

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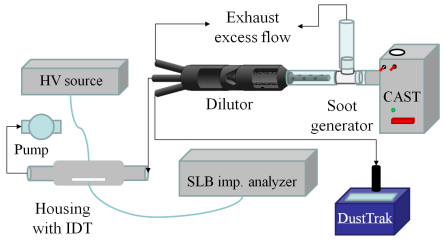
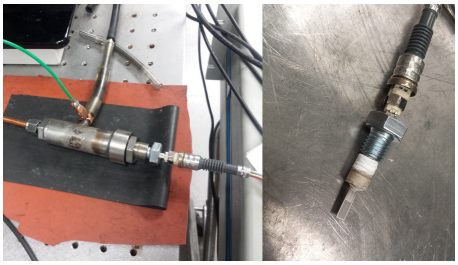


(a) This setup allows for independent control of aerosol concentration and flow.



(b) The sensor within its flow housing. Note the high voltage (HV) connection to the housing and the isolating pad (left). The ceramic IDE structure along with its mountable holder (right).

Figure A.3

Table A.1: Overview of the different E-fields on and around the sensor element.

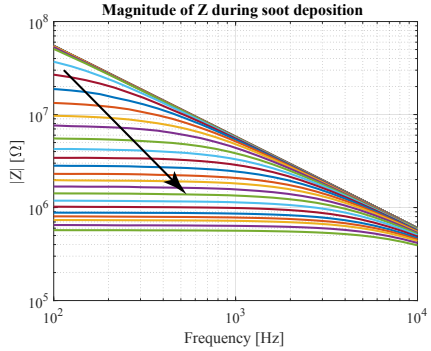
V	**Amplitude** [V]	**Field**	**Gap**	**E-field** [$\mathrm{V\,m^{-1}}$]
AC	3	horizontal	45 μm	6.67×10^4
DC	40	horizontal	45 μm	8.89×10^5
HV	500	vertical	2.5 mm	2×10^5

dilutor before being drawn by downstream pumps through the PM sensor flow housing. Soot concentration is monitored by a DustTrak II model 8530 and is on the order of 0.5 $\mathrm{mg\,m^{-3}}$ to 1 $\mathrm{mg\,m^{-3}}$. The PM sensor used for impedance analysis is constructed from components of a commercially available automotive PM sensor. It is constrained in a metal flow housing that forces aerosol-laden flow to pass through the sensor and across the IDE. Both resistive PM sensors used in this study allow for application of in-plane and normal electric field components by adjusting the IDE and metal housing electrical potentials. Impedance analysis is performed with a Solartron 1260 analyzer, and concurrent electrical biasing of the metal flow housing is applied with a Stanford Research Systems PS365 HV power supply. DC bias measurements during optical microscopy are performed with a Keithley 2420 source-measure unit in addition to the aforementioned HV power supply. The raw impedance data is mapped on the equivalent model parameters, c.q. parallel capacitance and resistance. A schematic overview of the measurement setup is included in Figure A.3a.

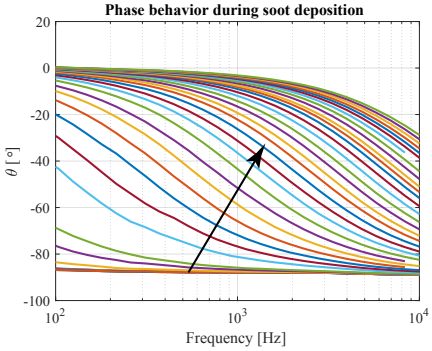
A set of conditions which affect the relative electric forces that define dendrite freedom of motion in the device are defined. A small AC bias of 0.5 V or 3 V is applied across the IDE while simultaneously applying either a small or large DC bias of 0 V, 5 V or 40 V, across the IDE. At the same time, an out-of-plane bias of either 0 V or 500 V is applied.

The magnitude of the impedance $|Z|$ and the phase shift of the impedance θ plots are

included in Figure A.4. The $|Z|$ plot implies a parallel RC network, where the response starts purely capacitive. When deposition time increases, the pole shifts towards higher frequencies, thus showing-up in the magnitude part of the bode plot. The reduction of the magnitude response at low frequencies reveals the almost exponential reduction of resistance at the onset of dendrite bridging. The measured phase response is almost flat −90° at t=0 min, after which the pole is pushing the phase shift to higher frequencies. The gradual increase of the phase in time at higher frequencies reveals the gradual change in capacitance with soot buildup.



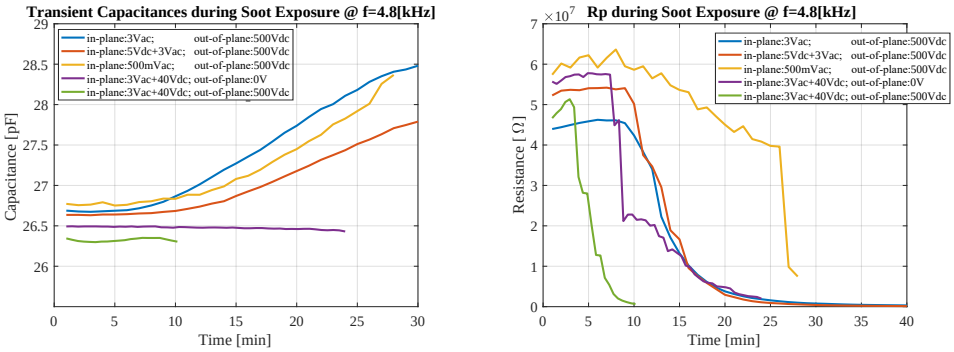
(a) $|Z|$ for an in-plane IDE voltage of 3 V_{AC} and a voltage applied to the housing of 500 V_{DC}. The arrow indicates the direction of progressing time, while the time between each trace equals 1 minute.



(b) θ of Z at an IDE voltage of 3 V_{AC} and a housing voltage of 500 V_{DC}. The arrow indicates the direction of progressing time, while the time between each trace equals 1 minute. These plots show that the PM sensor behaves as a parallel resistor-capacitor circuit.

Figure A.4

The parallel resistance and capacitance at a frequency of 4.8 kHz are plotted over time, as included in Figure A.5. As shown in this Figure, the extracted resistance and capacitance evolve differently over time as a function of applied electrical potentials. R and C data was plotted at a single frequency of 4.8 kHz, because the data beyond this frequency provided better fitting with our equivalent circuit model. At low frequencies parasitic components results in a deviation from the modeling based on a parallel RC circuit. The amount of time that the sensor spends in the pre-bridge state varies over a range of minutes depending on the applied electrical biases. The in-plane bias plays an important role directing dendrite orientation orthogonal to the IDE fingers; strong in-plane bias causes dendrites to more readily connect the two leads of the IDE. The out-of-plane bias helps bring more particles in for capture, too. Thus, the fastest drop in resistance occurs for high in-plane and high out-of-plane bias. Moderate delays before resistance drop occur when large in-plane bias is paired with no out-of-plane bias or



(a) Extracted capacitance of the resistive PM sensor as a function of time and applied bias conditions. Samples with strong in-plane bias show suppressed capacitive response. Samples which develop capacitance increase over time exhibit typical resistive PM sensor response: delay followed by signal increase.

(b) Extracted resistance of the resistive PM sensor as a function of time. Soot bridges grow at a rate proportional to soot capture, directed by in-plane bias. Larger out-of-plane bias leads to much faster soot capture, and simultaneous large in-plane bias leads to inter-electrode directed dendrite growth. The resistance drops fastest for large out-of-plane and large in-plane bias. Resistance decreases slowest for the smallest in-plane bias

Figure A.5

when moderate in-plane bias is paired with out-of-plane bias. The slowest resistance decrease response occurs for low in-plane bias. These behaviors are consistent with the idea that both soot capture and dendrites follow electric field lines.

The impedance-derived capacitance traces also have strong variation with applied bias. However, it is notable that not all of the samples exhibit changed capacitive response as soot dendrites form. When large in-plane bias is applied, no change in capacitance is observed despite the evidence of dendrite formation in the dropping resistance. Similarly, when no out-of-plane bias is applied there is no change in capacitance. In samples where changed capacitance is observed, the time trace shows typical resistive PM sensor behavior that includes delay before capacitance rises. A smaller rise in capacitance is observed when increased DC bias is applied between the IDEs and when less AC bias is applied between the IDEs. This behavior can be rationalized with the model: in order for capacitive response to occur in the resistive PM sensor, dendrites must move in response to the applied AC bias. This means that there will be an inherent delay while dendrites grow before a response can be observed. Additionally, the presence of dendrites does not guarantee that they have freedom of motion to participate in capacitive signal generation. When large in-plane DC bias is applied, the dendrites are constrained by electrical forces and cannot move in response to small in-plane AC bias, so no capacitance change can be measured. Similarly, when the inter-electrode bias is small, den-

drites do not stand out of the IDE plane unless an out-of-plane bias is applied; when dendrites primarily lay in contact with the substrate plane they are not free to move in response to small AC bias, so no capacitive change is observed. Under conditions where dendrites are free to move, increasing in-plane DC bias reduces the dendrite freedom of motion in response to small AC bias, resulting in reduced change in capacitance. Further, attenuated in-plane AC-bias provides a smaller electrical force to displace the dendrites and generate dipoles, so the capacitive response is smaller.

A.1.4. CONCLUSIONS ON RESISTIVE SOOT SENSORS

Impedance spectroscopy has been applied to an IDE structure on a ceramic substrate, with an out-of-plane additional electrode to enable the application of a vertical E-field. Several combinations of horizontal and vertical E-fields are applied by electrically biasing the IDE and out-of-plane electrode, and the influence on deposited soot dendrites is studied. Approximate analytical expressions were derived and have resulted in an equivalent circuit model.

The raw impedance data supports the equivalent circuit model of a parallel capacitor and resistor. In all cases was an increasing capacitance observed with a vertical electrical field. In general it can be concluded that the capacitance increases in a gradual way, in contrast to the rather sudden reduction of the parallel resistance value caused by dendrite formation. The exponential signal shape of the resistance, along with stochastic noise in dendrite growth, is typically undesired for accurate characterization of a DPF leak level, as the sensor is then treated as a switch rather than delivering a quantitative sensor signal. Whether or not the capacitance increases, depends on the magnitude of the vertical E-field compared to the magnitude of the lateral E-field, a larger vertical field is demonstrated to be advantageous. The operation of the resistive PM sensor therefore relies not only on the electrical and self-assembly behavior of dendrites, but also on their freedom of motion. It remains to be investigated whether the observed effects are sufficiently pronounced and repeatable for practical use.

Future work includes investigation of Micro-Electro Mechanical System (MEMS) technology for the fabrication of more repeatable cells, where the opposing electrodes both consists of an IDE. Additionally, the effect of spacing between the IDE fingers and the relative position of both sets of IDEs can be investigated.

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B

APPENDIX-B

B.1. SUPPORTING INFORMATION CHAPTER 6

In order to define a specific pressure sensor structure, different options are considered in this Appendix. The basic pressure sensor structure was chosen using a PUGH matrix. The different pressure sensor structures considered are:

1. **All mono-c-SiC bulk with piezo resistors in SiC epitaxy**: Bulk micromachined mono crystalline membrane with piezo resistors from doped epi-layers.

2. **Wafer bonding after cavity etch & thinning**: Etching a cavity in the bulk and thinning down a mono-c SiC wafer with epi layers.

3. **Photo electrochemical (PEC) etched membranes in mono-c-SiC**: Using PEC etching where dopant selective etching is used to under etch epi layers, which can be used as membranes.

4. **Vertical piezo resistors from mono-c-SiC**: ICP etching and sealing with LPCVD carbide again where vertical piezo resistors are formed along a reference cavity.

5. **Substrate cavity poly-SiC capping**: Etching a cavity in the bulk and capping again with poly or amorphous SiC.

6. **Mesa's from silicon oxide with poly-SiC**: Using mesas of SiO_2 as sacrificial blocks and covering them with an poly-SiC doped membrane. Read out can be both piezo resistive and capacitive.

7. **Custom SiCOI wafer underetch**: Oxidize a SiC wafer and subsequently deposit poly-SiC and underetch the poly-SiC to form suspended membranes.

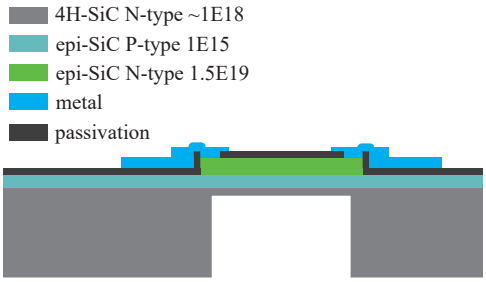


Figure B.1: Pressure sensor based on bulk etching SiC wafers with piezo resistors selectively etched in SiC epitaxy (option 1)

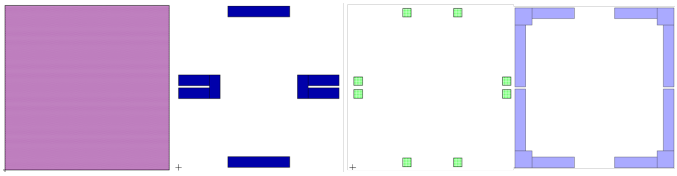


Figure B.2: As an example: A mask design for possible realization of mono-c-SiC based pressure sensor with epi piezo resistors. Four images from left to right: membrane, the piezo elements, the contact openings and the interconnect. The piezo elements are laterally offset w.r.t. the membrane to align the regions of maximum stress.

PUGH matrix In order to make a statistically funded decision on the pressure sensor structure, a PUGH matrix is used as included in Table B.1. The implementation based on the LPCVD poly-crystalline SiC on top of silicon oxide mesas has the highest score. This is mainly caused by the in-house development compatibility, the omission of complex crystalline SiC ethcing. Furthermore, no epi-layers are needed which need to be delivered by external suppliers.

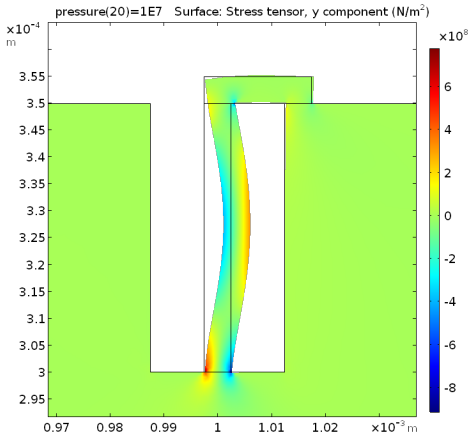


Figure B.3: The stress tensor in the y-direction for 10 MPa based on a FEM simulation of an implementation of vertical piezo resistors etched from a mono-crystalline SiC. Two trenches are etched in this example, of which one trench is sealed at a reference pressure. Varying pressure is measured by deflection of this vertical membrane acting as piezo resistor.

Table B.1: Weighted PUGH matrix for the selection of the pressure sensor design. Score ranging from -3(large negative effect) to 3 (large positive)

		Option						
Criteria	Weight (1-5)	1	2	3	4	5	6	7
In house development	5	-2	-1	1	3	3	3	3
Novelty	3	0	2	2	3	0	-1	1
Integration possibilities	4	3	0	1	2	3	2	-2
Requires SiC epitaxy	4	-3	1	-3	0	3	3	3
Cost in mono-c-SiC wafers	3	0	-3	0	0	0	0	0
Complexity in design	1	-1	-2	-2	-2	2	2	2
Complexity in fabrication	5	-2	-2	-1	-3	-2	1	0
New processes required	4	0	-1	-3	2	0	1	1
Modularity	4	2	-1	-1	1	2	2	1
Weighted net effect		-13	-24	-20	27	39	51	32

B

Table B.2: Different images for the surface micromachined piezoresistive pressure sensors.

Layer nr.	Layer name	Abbrevation	Explanation	Field
1	Mesa	MS	Pattern oxide mesas	bright
2	Release holes	RH	Pattern release holes	dark
3	Poly SiC remove	SR	Remove poly SiC where no mem	bright
4	Contact holes	CO	Pattern the CO's	dark
5	Interconnect	IC	Metallization for all structures	bright
6	Center Metal	CM	Center metal to bridge the mem. Neg. resist is used with double patterning	dark
7	Trench	TR	Pattern trench for other process, no MS and SR then	dark
8	SiC mesa	SC	SiC mesa for res. meas. and piezo R structures	bright
9	Buried electrode	BE	Electrode for capacitive sensor	bright

C

APPENDIX-C

C.1. SUPPORTING INFORMATION CHAPTER 7

Table C.1: Pad numbers for the SN (top) and SP (bottom) thermistor based temperature sensing circuits

Pad	Name
63	I_SRC
62	I_SNC
66	V_REF (shared)
61	V_IN+ (off-chip cap. between P65 and P66)
60	V_OUT
59	I_SRC
58	I_SNC
66	V_REF (shared)
57	V_IN+ (off-chip cap. between P61 and P66)
56	V_OUT

Table C.2: Pad numbers for the relaxation oscillator based resistive read-out

Pad	Name
68	I_SRC
67	I_SNC
66	V_REF (shared)
65	V_IN+ (off-chip cap. between P65 and P64)
64	V_OUT

Table C.3: Pads for the PTAT circuits

Pin No.	Name	Circuit
55	4PTAT	4PTAT
01	I_SRC	5PTAT
02	I_SNC	5PTAT
03	V_GS1	5PTAT
04	V_GS2	5PTAT

Table C.4: Pin-numbers for the unit-C based capacitive read-out

Pin No.	Name
18	CHRG
19	CLK
20	I_SRC (shared)
21	V_CM
22	I_SNC
23	DGT_O

Table C.5: Pin-numbers for the relaxation oscillator based capacitive read-out

Pin No.	Name
11	I_SRC
12	I_SNC
13	V_REF
14	V_OUT
15	V_IN+

C

Table C.6: 6 probe PCM devices

Device	Remark
Clocked comparator	V_{ref} made on chip
Comparator	Continuous time
Relaxation oscillator	-
5T PTAT	External biasing required
Stacked mirror 40 x 20 µm	-

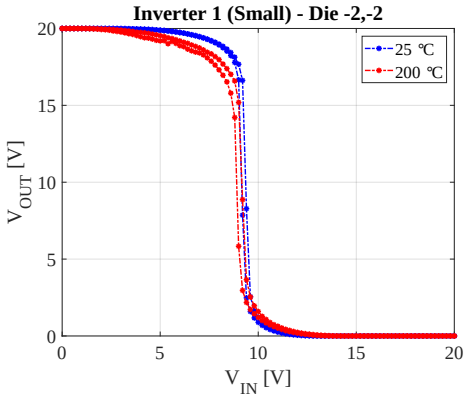
Table C.7: 4 probe PCM devices

Device	Remark
SN 20 kΩ	Meandered resistor 2 point
SN 20 kΩ Kelvin	Meandered resistor 4 point
SP 20 kΩ	Meandered resistor 2 point
SP 20 kΩ Kelvin	Meandered resistor 4 point
SN 100 kΩ	Meandered resistor 2 point
SN 100 kΩ Kelvin	Meandered resistor 4 point
SP 100 kΩ	Meandered resistor 2 point
SP 100 kΩ Kelvin	Meandered resistor 4 point
4T PTAT	Self-biased PTAT
Current mirror 40 x 20 µm	-
Current mirror 20 x 6 µm	-
Buffer 2000 µm PMOS	-
100 fF MiM	Capacitor after M2
500 fF MiM	Capacitor after M2
2 pF MiM	Capacitor after M2

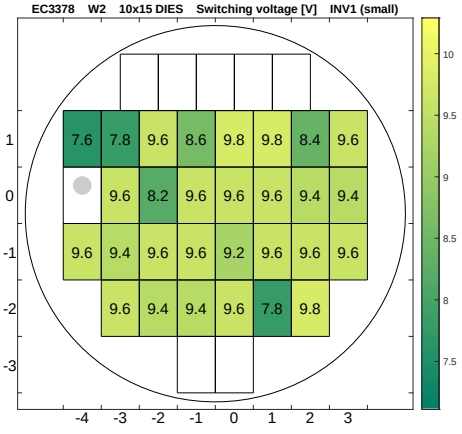
D

APPENDIX-D

D.1. SUPPORTING MEASUREMENT RESULTS SiC-CMOS

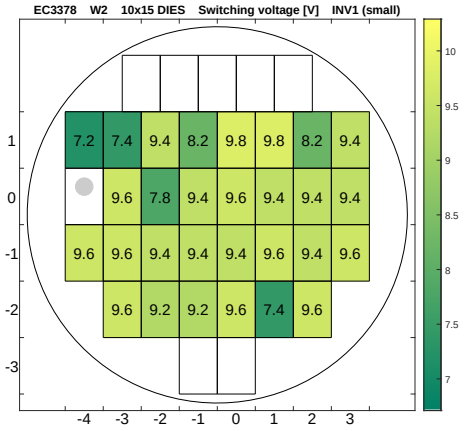


(a) The input-output characteristic for the smaller inverter on die -2,-2 (L=6 µm; W_P=80 µm, W_N=20 µm) for both 25 °C and 200 °C.

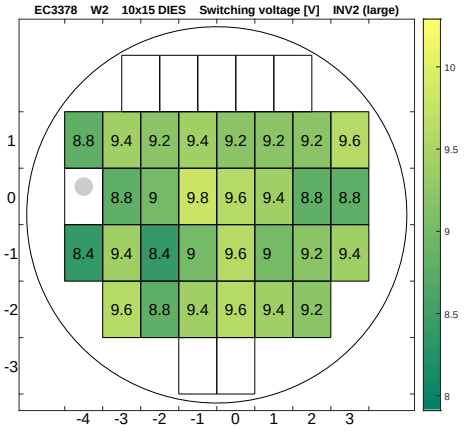


(b) The measured spread of the switching voltage over the wafer for smaller inverter on 25 °C, μ = 9.26 V; σ = 0.652 V.

Figure D.1: Inverter characterization on PCM-4PA.

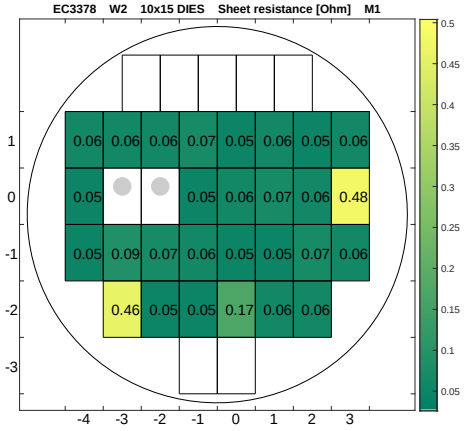


(a) The measured spread of the switching voltage over the wafer for smaller inverter on 200 °C, μ = 9.12 V; σ = 0.775 V.

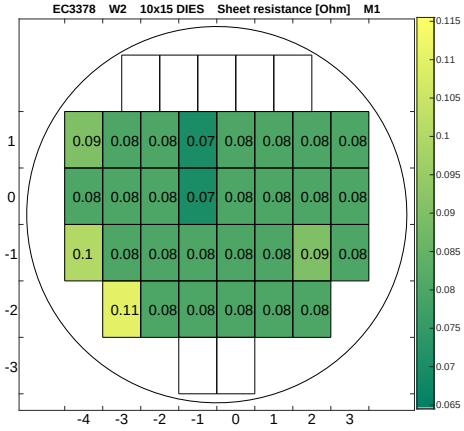


(b) The measured spread of the switching voltage over the wafer for larger inverter on 200 °C, μ = 9.28 V; σ = 0.455 V.

Figure D.2: The waferscale results of both the smaller and the larger inverter measured at 200 °C.

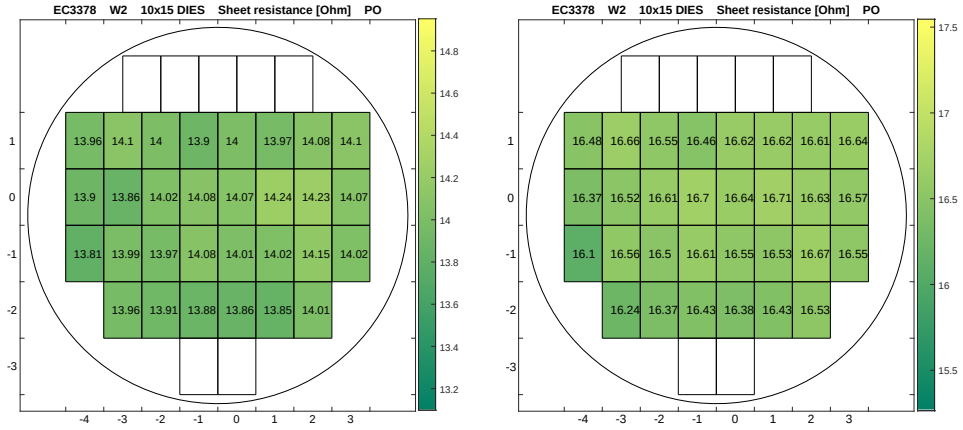


(a) At 25 °C, μ = 0.0925 Ω; σ = 0.109 Ω.



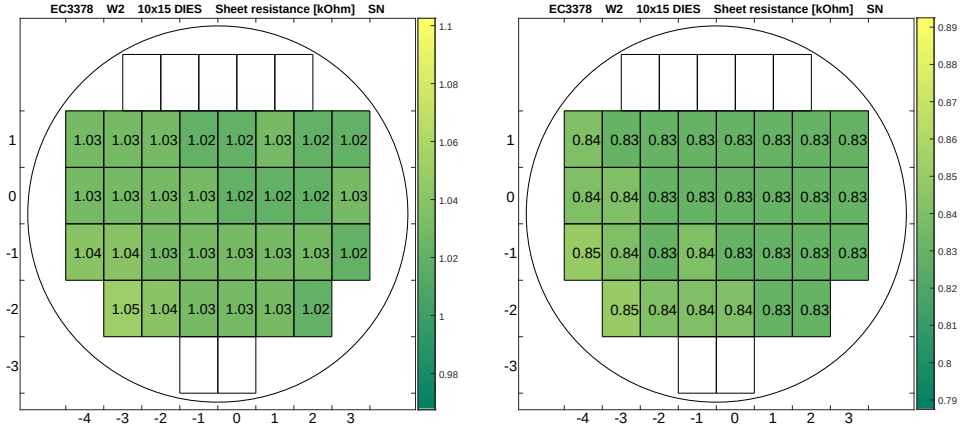
(b) At 200 °C, μ = 0.0817 Ω; σ = 0.007 47 Ω.

Figure D.3: The waferscale results of the M1 sheet resistance using the Van der Pauw structures.



(a) At 25 °C, $\mu = 14.0\,\Omega$; $\sigma = 0.106\,\Omega$. **(b)** At 200 °C, $\mu = 16.5\,\Omega$; $\sigma = 0.137\,\Omega$.

Figure D.4: The waferscale results of the poly sheet resistance using the Van der Pauw structures.



(a) At 25 °C, $\mu = 1.03\,\text{k}\Omega$; $\sigma = 0.00730\,\text{k}\Omega$. **(b)** At 200 °C, $\mu = 0.834\,\text{k}\Omega$; $\sigma = 0.00621\,\text{k}\Omega$.

Figure D.5: The waferscale results of the SN sheet resistance using the Van der Pauw structures.

SUMMARY

This thesis describes the possibilities and challenges of the pathway from silicon toward silicon carbide smart integrated sensors. The aspect 'smart' is in this work reflected by the system integration aspects. Those aspects can be the integration of multi-domain sensing structures, read-out electronics or temperature sensors. The research toward extended functionality of sensors in state-of-the-art silicon technology and the exploration of the application of wide bandgap semiconductors can both be seen as realization of the More than More trend, described by diversification, the introduction of novel materials and integrated process development.

In Chapters 2 and 3 bulk micromachining on silicon wafers is exploited to create structures with geometries on the edge of manufacterability. The resonance frequency of spiral resonators is measured on wafer scale. The effect of a deviation on the resonance frequency on the beamwidth is investigated for the application in process monitoring. To realize a high-resolution accelerometer which can be used as gravimeter, a non-linear buckling based compliant mass/beam system is realized by bulk micromachining silicon wafers. The realized long thin beams are used to achieve an almost zero stiffness at the operation point and have a width of only 5 µm. A high mechanical sensitivity is achieved, thereby boosting the input-referred system resolution. Reading out the displacement of the mass is done by an capacitive read out structure based on interdigitated electrodes. Both polarities of the transducer are electrically isolated by trenches filled with silicon nitride in combination with a backside etch. The mechanical design of the mass/beam systems is verified by optical transmission measurements. The devices with integrated electrical read-out are directly wirebonded onto a PCB interfacing an precision impedance read-out chip. Operation of the capacitive displacement read-out is confirmed and the lowest resonance frequency measured equaled 8.7 Hz. Together with the noise floor of the read-out chip, a theoretically obtainable system resolution is derived of 17.02 ng/$\sqrt{\text{Hz}}$.

Chapter 4 summarizes the differences between Si and SiC technology regarding some major fabrication steps typically required to yield microsystems and electronics. Lithography experiments on mono-crystalline 4H-SiC wafers are performed. Despite the transparency of the SiC substrates, no problems are encountered. Thanks to this transparency

of the substrates, alignment *through* the wafer is even achieved. Etching of mono-crystalline 4H-SiC is investigated and etch experiments are conducted based on available knowledge. Standard plasma etchers can be used to etch trouble-free up to etch depths of several 100 nm. Deep etching into 4H-SiC substrates is attempted, but it is concluded that the etch rate could be considered low for bulk micromachining with only 135.17 nm min^{-1}. Additionally, micromasking occurred due to instability of the required metal hard mask. Etching of poly-SiC layers is performed using different plasma etch tools, and custom recipes using fluorine based chemistries are developed at 0 °C and 10 °C. Bulk micromachining by using laser ablation methods is also investigated. Etching completely through a 360 µm 4H-SiC substrate for a square surface area of 400 µm width is performed in 7 min. Due to the nature of the laser ablation process, in order to make this technique feasible for fabrication of MEMS and microsystems, challenges lie in the control of the etch depth, the finishing of the ablated surface, the thermal damage to the bulk material and the contamination control of ablated debris. The physics behind the formation of ohmic contact to mono-crystalline SiC is summarized. Silicidation at high temperatures (500 °C to 1000 °C) is typically required to achieve ohmic contacts and due to the large bandgap, in general two different metals are required to interface n- and p-type SiC. Contacts are made to different poly-SiC layers using AlSi(1%) and pure titanium. Ohmic behavior is observed both for lowly doped and highly doped poly-SiC layers and already after annealing at 450 °C.

The application of poly-crystalline SiC layers is exhibited in the context of optical particle sensors in Chapter 5. An optically transparent heatable suspended poly-SiC membrane is designed, realized and characterized. The heaters consist of doped poly-SiC which are directly patterned on the membrane layer. Keeping a clean window to interface the particle containing gas stream in the tailpipe of a vehicle is an important requirement to introduce optical instrumentation in an automotive application. Two modes of operation to keep the poly-SiC windows clear from soot contamination are investigated and successfully exhibited. Contamination prevention is achieved by thermophoretic repulsion: a thermal gradient between the gas flow and the window prevent soot particles from depositing. Self-cleaning is shown by heating (part of) the membrane to temperatures beyond 500 °C, causing the deposited particles to oxidize.

Surface micromachining of thin-film poly-SiC layers is applied to design and realize piezo resistive self-sensing absolute pressure sensors. The self sensing concept is used as starting point to convenience the fabrication process of this MEMS device for future monolithic integration with front-end read-out electronics. Sacrificial oxide is etched and the resulting cavities are sealed by LPCVD on a reference pressure. The concept of a

self-sensing membrane is successfully shown and can be used to realize surface micromachined pressure sensors, of which the functional material is solely poly-SiC. In addition to the surface micromachined cavities, suspended microbridge structures functioning as Pirani gauges have been modeled, designed, realized and measured. Poly-SiC layers with different doping concentrations are characterized and based on the TCR characterization, the optimal doping concentration is determined. Gauges with different geometries are characterized at room temperature. A 1000 µm long gauge is measured up to 500 °C and successful operation is achieved. The piezoresistive devices show operation between 20 Pa to 100 kPa, whereas the Pirani gauges show operation between 10 Pa to 100 kPa. The characterizatoin of the Pirani gauges imply operation at even lower pressures. The design of the piezoresistive devices can be modified to shift the measurement range to the over-pressure regime by varying device geometry, while the optimal operation regime of the Pirani gauges is in vacuum conditions.

To introduce the smart aspect to the designed SiC MEMS devices, a multi-project SiC CMOS chip is developed in collaboration with Fraunhofer IISB, as described in Chapter 7. Based on premature circuit models, discrete electronic devices are designed and combined into different PCM modules. Additionally, different resistive- and capacitive read-out circuits are designed based on a clocked and continuous-time comparator. These read-out circuits are intended to interface (SiC) sensors, that could be integrated monolithically in a later stage. PTAT and thermistor based termperature sensing circuits have also been integrated. Based on a hierarchical layout structure, the circuit layout was performed while taking into account the conservative design rules. Major part of the fabrication was performed by Fraunhofer, with M1 fabrication in EKL. The characterization phase shows that the technological parameters are in-line with earlier runs and the available literature. However, the threshold voltages of the NMOS and PMOS devices differs significantly from the circuit models. The inverters, clocked and non-clock comparators are measured to be fully operational in the temperature range of 25 °C to 200 °C. These measurements are a promising outlook for the resisitive and capacitive read-out circuits. The temperature dependency of the monolithic resistors enables their usage as thermistors. The working electronic circuitry up to 200 °C in 4H-SiC, both in the analog and digital domain, is an promising starting point for further development of smart integrated SiC sensors.

SAMENVATTING

Deze thesis beschrijft de mogelijkheden en uitdagingen van het traject van silicium naar silicium carbide slimme geïntegreerde sensoren. Het aspect 'slim' wordt in dit werk weerspiegeld door de apsecten van systeemintegratie. Deze aspecten kunnen zijn; de integratie van multi-domein sensor structuren, uitlees elektronica of temperatuursensoren. Het onderzoek naar uitgebreide functionaliteit van sensoren in state-of-the-art silicium technologie en het verkennen van de toepassing van *wide-bandgap* halfgeleiders, kunnen beide worden gezien als realisatie van de *More than Moore* trend, beschreven door diversificatie, de introductie van nieuwe materialen en de ontwikkeling van geïntegreerde processen.

In hoofdstukken 2 and 3 is microfabricage van silicium substraten verkend om structuren te creëren met geometrieën op de rand van produceerbaarheid. De resonantiefrequentie van spiraal vormige resonatoren is gemeten op wafer niveau. Het effect van een afwijking in de resonantie frequentie op de spiraalbreedte is onderzocht voor toepassing in procesmonitoring. Om een hoge-resolutie versnellingssensor te realiseren welke gebruikt kan worden als gravimeter, is een niet-lineair knikkend en volgzaam massa/veer systeem gerealiseerd door gebruik te maken van microfabricage van silicium wafers. De geëffectueerde lange dunne balkjes zijn gebruikt om een stijfheid te bereiken welke in het werkpunt nul benadert en hebben een breedte van slechts 5 µm. Een hoge mechanische gevoeligheid is bereikt, waardoor de systeemresolutie (gerefereerd naar de input van het systeem) wordt opgevoerd. Het uitlezen van de verplaatsing van de massa is gedaan door gebruik te maken van een capacitieve uitlezing gebaseerd op interdigitated elektroden. Beide polariteiten van de transductor zijn elektrisch geïsoleerd door gleuven gevuld met silicium nitride in combinatie met een etsstap aan de achterkant van het substraat. Het mechanisch ontwerp van de massa/veersystemen is geverifieerd door optische transmissie metingen. De versnellingssensoren met geïtegreerde elektrische uitlezing zijn direct afgemonteerd op een PCB, waarna draadverbindingen zijn aangebracht. Dit PCB vormt tevens de interface naar een precisie impedantie uitleeschip. De werking van de capacitieve uitlezing van de verplaatsing is geverifieerd en de laagst gemeten resonantiefrequentie is 8.7 Hz. In combinatie met de ruisvloer van de uitleeschip, een theoretisch beschikbare systeemresolutie van 17.02 ng/$\sqrt{\text{Hz}}$ is afgeleid.

Hoofdstuk 4 vat de verschillen tussen Si en SiC technologie samen wat betreft enkele belangrijke fabricage stappen, typisch vereist om microsystemen en elektronica te fabriceren. Lithografie experimenten zijn uitgevoerd op monokristallijne 4H-SiC substraten. Ondanks de transparantie van de SiC substraten zijn er hierbij geen problemen ondervonden. Uitrichting door de wafer is zelfs bereikt, met dank aan de transparantie van de substraten. Het etsen van monokristallijn 4H-SiC is onderzocht en ets experimenten zijn uitgevoerd, gebaseerd op beschikbare kennis. Standaard plasma etsers kunnen worden gebruikt om probleemloos enkele 100 nm's diep te etsen. Diep ets experimenten in 4H-SiC substraten zijn ondernomen, er kan echter geconcludeerd worden dat de bereikte ets snelheid van 135.17 nm min^{-1} laag is voor microtechnologie van substraten. Daarnaast vond micro maskering plaats ten gevolge van instabiliteit van de metalen maskerlaag. Etsen van poly-SiC lagen is uitgevoerd gebruik makend van verschillende plasma ets machines. Toepassingsspecifieke ets recepten zijn ontwikkeld daarbij gebruik makend van fluorchemie bij 0 °C en 10 °C. Microtechnologie van substraten door laser ablatie methoden is tevens onderzocht. Het volledig dooretsen van een vierkante oppervlakte van 400 µm door een 360 µm 4H-SiC substraat is succesvol uitgevoerd in een tijdbestek van 7 min. Om deze techniek uitvoerbaar te maken voor de fabricage van MEMS en microsystemen liggen er, door de aard van het laser ablatie proces, uitdagingen in de controle van de ets diepte, de afwerking van het afgesmolten oppervlak, de thermische schade aan het bulkmateriaal en de controle van de vervuiling van afgesmolten puin.

De fysica achter de vorming van ohmse contacten naar monokristallijn SiC is samengevat. Silicidatie bij hoge temperaturen (500 °C-1000 °C) is typisch vereist om ohmse contacten te realiseren en door de grote bandgap zijn er over het algemeen twee verschillende metalen vereist om n- en p-type SiC te koppelen. Contacten zijn gemaakt naar verschillende poly-SiC lagen gebruik makend van AlSi(1%) en puur titanium. Ohms gedrag is geobserveerd voor zowel laag gedoteerde en hoog gedoteerde poly-SiC lagen en reeds na uitgloeiing bij 450 °C.

De toepassing van polykristallijne SiC lagen is getoond in de context van optische deeltjessensoren in hoofdstuk 5. Een optisch transparant verwarmbaar vrijhangend poly-SiC membraan is ontworpen, gerealiseerd en gekarakteriseerd. De verwarmers bestaan uit gedoteerd poly-SiC welke direct gepatroneerd zijn op de membraan laag. Het behouden van een schoon membraan om de deeltjesrijke gasstroom in de uitlaatpijp van een voertuig te kunnen interfacen, is een belangrijke vereiste voor de introductie van optische instrumentatie in een automotive toepassing. Twee manieren van gebruik om de poly-SiC membranen vrij te houden van roet contaminatie zijn onderzocht en suc-

cesvol aangetoond. Preventie van contaminatie is bereikt door thermoforetische afstoting: een thermische gradiënt tussen de gasstroom en het membraan voorkomt depositie van roetdeeltjes. Zelfreiniging is aangetoond door verwarming (een gedeelte) van het membraan tot temperaturen van boven de 500 °C, resulterend in oxidatie van de gedeponeerde deeltjes.

Oppervlak gebaseerde microfabricage van dunne-film poly-SiC lagen is toegepast om piezo resistieve zelf-uitlezende absolute druksensoren te ontwerpen en realiseren. Het concept van zelf-uitlezende membranen is gebruikt als uitgangspunt om het fabricageproces van deze MEMS-sensor eenvoudiger te maken voor toekomstig monolithische integratie met front-end uitleeselectronica. Opofferingsoxide is geëtst en de resulterende holle ruimten zijn geseald door LPCVD bij een referentiedruk. Het concept van een zelf-uitlezend membraan is succesvol aangetoond en kan worden gebruikt om druksensoren te effectueren, middels oppervlak gebaseerde microfabricage, waarvan het functionele materiaal uitsluitend poly-SiC is. Naast de gesealde holte-gebaseerde druksensoren, vrij hangende microbrugstructuren werkend als Pirani meter zijn gemodelleerd, ontworpen, gerealiseerd en gemeten. Poly-SiC lagen met verschillende dopingconcentraties zijn gekarakteriseerd en gebaseerd op de karakterisatie van de TCR, de optimale dopingconcentratie is bepaald. Meters met verschillende geometrieën zijn gekarakteriseerd bij kamer temperatuur. Een 1000 µm lange microbrug is gemeten tot 500 °C en succesvolle werking in dit tempetuurbereik is behaald. The piezoresistieve sensoren werken tussen 20 Pa tot 100 kPa, terwijl de Pirani meters werken tussen 10 Pa tot 100 kPa. De karakterisatie van de Pirani meters impliceren zelfs werking bij een nog lagere druk. Het ontwerp van de piezoresistieve druksensoren kan worden aangepast door de meetrange te verschuiven naar het overdruk domein middels variatie in de geometrie, terwijl het optimale meetbereik van de Pirani meters in het het vacuüm domein ligt.

Om het slimme aspect te introduceren bij de ontworpen SiC MEMS-sensoren, is er een multi-project SiC CMOS chip ontwikkeld in samenwerking met Fraunhofer IISB, zoals omschreven in hoofdstuk 7. Gebaseerd op niet-uitgekristalliseerde circuit modellen zijn discrete elektronische componenten ontworpen en gecombineerd tot verschillende PCM-modules. Verder zijn er verschillende resisitieve en capacitieve uitlees schakelingen ontworpen gebaseerd op een geklokte en continue-tijd comparator. Deze uitlees circuits zijn bedoeld voor het uitlezen van (SiC) sensors, welke in een later stadium monolithisch geïntegreerd zouden kunnen worden. PTAT en thermistor gebaseerde temperatuur meet circuits zijn tevens geïntegreerd. Gebaseerd op een hiërarchische layout structuur is de circuitlayout uitgevoerd terwijl de conservatieve ontwerpregels in acht

zijn genomen. Het grootste gedeelte van de fabricage is uitgevoerd door Fraunhofer, waarbij M1 fabricage is uitgevoerd in EKL. De karakterisatiefase demonstreert dat de technologie parameters in lijn zijn met eerdere uitvoeringen van het proces en met de beschikbare literatuur. Echter, de drempelspanning van de NMOS en PMOS componenten verschillen significant van de circuit modellen. Testen laten zien dat de inverters, de geklokte en niet-geklokte comparatoren operationeel zijn in het temperatuurbereik van 25 °C tot 200 °C. Deze metingen geven veelbelovende vooruitzichten voor de resistieve en capacitieve uitlees elektronica. De temperatuurafhankelijkheid van de monolithische weerstanden maakt het gebruik hiervan als thermistors mogelijk. De werkende elektronische schakelingen tot 200 °C in 4H-SiC, zowel in het analoge als het digitale domein, zijn een veelbelovend startpunt voor de verdere ontwikkeling van slimme geïntegreerde SiC sensoren.

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List of Publications

Journal Papers

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PATENT APPLICATIONS

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