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Spin Wave Threshold Majority Gate

Arne Van Zegbroeck[1], Florin Ciubotaru[2], Pantazis Anagnostou[3], Fanfan Meng[4], Christoph Adelmann[5], Said Hamdioui[6], and Sorin Cotofana[7]

***Abstract*— Current Spin Wave (SW) state-of-the-art computing relies on wave interference for achieving low power circuits. Despite recent progress, many hurdles, e.g., gate cascading, fan-out achievement, still exist. In a previous work, we introduced a novel SW phase shift based computation paradigm and demonstrated that an n-input Threshold Logic Gate (TLG) can be implemented with $n+1$ phase shifters operating on the same SW. In this paper we further develop this concept by introducing a phase shift amount reading method by means of parametric amplification. We make use of 3-input Majority Gate ($MAJ3$) as discussion vehicle and introduce a novel majority function evaluation approach which postpone the threshold related calculations to the gate output readout stage. Subsequently, we verify this principle by means of micromagnetic simulations and discus the results. Finally, we utilize the proposed $MAJ3$ gate to implement a collection of representative logic circuits from the EPFL Combinational Benchmarking Suite and evaluate and compare their area, energy consumption, and Energy Area Product (EAP) with the ones of $7\,\mathrm{nm}$ CMOS technology node based counterpart implementations. Our estimations indicate that $\frac{EAP_{CMOS}}{EAP_{SW}}$ average value is 5.25 and 2.2 for a SW transducer feature size of $20\,\mathrm{nm}$ and $30\,\mathrm{nm}$, respectively.**

I. Introduction

With the introduction of large language models such as GPT-3, GPT-4, copilot, gemini, etc., the public has gotten access to advanced AI systems that can be asked questions that they can solve for you. What a lot of people do not realize is the massive amount of power that is required for training or even for a single "prompt" to be fulfilled when compared to, e.g., a Google search. For training, chat GPT-3 consumed $1.287\,\mathrm{MWh}$ [1] and in order to serve its user base it needs an approximate amount of $564\,\mathrm{MWh}$ per day [1]. With these systems projected to grow in userbase over the coming years, their power consumption would only increase making them economically unsustainable to maintain without serious price increases. At the same time further transistor scaling to increase power efficiency is harder then ever as short channel effects, power density and gate tunneling are coming into play [2]. Various solutions like changing to a different FET architecture have already been implemented and novel technologies that fully depart from the CMOS architecture, commonly referred to as beyond-CMOS technologies, have also been proposed. These technologies explore new avenues for data processing and storing in a power efficient manner. Among these technologies, spintronics has been successfully utilized for low power electronic circuit implementations [3], non-volatile efficient memory [3], and neuromorphic computing [4]. Spin Waves (SWs) based computing is a disruptive spintronics sub-domain with great potential for fast, small, and efficient circuits working with waves instead of currents. SWs are local perturbations of the magnetization of a magnetic material that travel in wave like manner and their interference provides support for novel computation avenues, circuits, and architectures. Current state of the art encodes binary information into the SW phase, i.e., given an arbitrary SW in phase with the reference carries a logic 0 and a 180° phase shifted SW a logic 1. When an odd number of same amplitude and frequency SWs coexist into the same waveguide they interfere constructively and/or destructively which provides the natural mechanism for majority voting. Following this principle, different 3-input Majority gate ($MAJ3$) designs have been proposed [5], [6] and experimentally validated [7]. As $MAJ3$ gates and inverters form a universal gate set, and logic value inversion can be obtained by relocating the gate output position, any Boolean function can be implemented by means of $MAJ3$ gates. However, the road from gate to circuit is not straightforward as it is in CMOS circuits. Gate cascading and fan-out achievement requires SWs to charge and back conversions, which may result in significant energy consumption overheads. In recent work we pursued a different SW computing avenue and introduced a novel SW based Threshold Logic Gate (TLG) [8], which goes beyond SW computation state of the art by relying on SW phase shifts instead of SW interference. In this paper we introduce a TLG based 3-input Majority (SWTL $MAJ3$) gate implementation, discuss its output readout mechanism, and evaluate the implications of utilizing such a gate for the implementation of representative logic circuits from the EPFL Combinational Benchmarking Suite. Our estimations indicate that when compared with $7\,\mathrm{nm}$ CMOS counterpart

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[1]Arne Van Zegbroeck is with Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, 2600 AA Delft, The Netherlands a.g.e.vanzegbroeck@tudelft.nl

[2]Florin Ciubotaru is with IMEC, 3001 Leuven, Belgium florin.ciubotaru@imec.be

[3]Pantazis Anagnostou is with Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, 2600 AA Delft, The Netherlands

[4]Fanfan Meng is with IMEC, 3001 Leuven, Belgium

[5]Christoph Adelmann is with IMEC, 3001 Leuven, Belgium

[6]Said Hamdioui is with Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, 2600 AA Delft, The Netherlands

[7]Sorin Cotofana is with Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, 2600 AA Delft, The Netherlands

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implementations in terms of Energy Area Product (EAP) the $\frac{EAP_{CMOS}}{EAP_{SW}}$ average value is 5.25 and 2.2 for a SW transducer feature size of 20 nm and 30 nm, respectively, which clearly indicates that, if transducer technology will advance as expected, the proposed SWTL $MAJ3$ gate can open avenues towards the practical realization of ultra low-power circuits able to outperform CMOS counterparts.

The presentation is organized as follows: Section II provides brief inside on Spin Waves, Threshold Logic, and our previous work. In Section III we present the adaptation of the threshold logic function to allow for the utilization of the phase to intensity converter reported in [9] to determine the gate output value. Afterwards we present simulation results to confirm the working of the phase to intensity converter in collaboration with the phase-shifters. Section V presents an analysis of the implications of our proposal at the circuit level and its capability to provide circuit and architecture implementations able to outperform the CMOS counterparts, and Section VI closes the presentation.

II. Spin Wave Threshold Logic Gate

As mentioned in the introduction, SWs are local perturbations of the magnetization of a magnetic material that travel in wave like manner [10], [11]. Current state of the art for SW based computing relies on the interference of two waves. If we arbitrarily assign a wave to represent logic 1, then the 180 ° phase shifted version of that wave represents logic 0. If a logic 1 SW and a logic 0 SW interfere they combine destructively, while same phase SWs combine constructively. With this principle a majority voting gate can be constructed by having an uneven number of inputs. If there are for example three inputs, i.e., a 3-input Majority gate ($MAJ3$), if two of the inputs are opposite, they cancel each other out and the resulting output is determined by the value of the left over input. While the gate structure is rather simple, problems arise regarding cascading such $MAJ3$ devices to form larger circuits when all three inputs are the same, the resulting SW has a larger amplitude than the one of the input SWs, which is breaking computation with devices down the line. Additionally, such a $MAJ3$ device require three RF generators, which results into a significant electronic hardware overhead. Recently, instead of relying on SW interference, we proposed to use SW phase shifting as a fundamental computation mechanism and introduced SW Threshold Logic Gates [8].

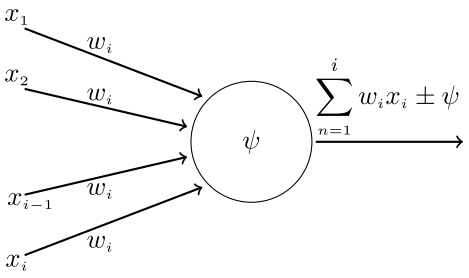

Fig. 1. Basic threshold logic gate.

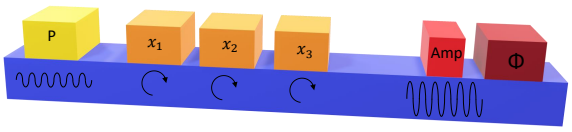

Fig. 2. SW based threshold logic majority device with amplifier for readout.

A Threshold Logic Gate (TLG) is in essence a McCulloch-Pitts neuron model, with no implemented learning, for more information see [12]. The gate multiplies each input with its corresponding weight, adds them up, subtracts a threshold value, and determines the output value by means of a sgn function, as depicted in Figure 1. We can constrain the gate inputs to binary values and impose (1) at the output in order to produce output binary values. Note that weight values can assume integer values.

$$F(x) = sgn(f(x)) = \begin{cases} 1, & f(x) \geq 0 \\ 0, & f(x) < 0 \end{cases} \tag{1}$$

TLGs are more powerful that Boolean logic gates and as such TLG circuit implementations require less gates, as indicated by the Full Adder implementation example of the sum bit (2) and the carry out bit (2).

$$C_{out} = sgn(x_1 + x_2 + C_{in} - 2) \tag{2}$$

$$Sum = sgn(x_1 + x_2 + C_{in} - 2C_{out} - 1) \tag{3}$$

Note that in this paper we seek the implementation of 3-input majority function, which is the same as the C_{out} calculation (4).

$$MAJ3 = sgn(x_1 + x_2 + x_3 - 2) \tag{4}$$

Note that $MAJ3$ together with inverter form a universal gate set thus any Boolean function can be implemented by means of them, e.g., the Full Adder outputs can be implemented as indicated in Equation (5) and (6).

$$C_{out} = MAJ3(x_1, x_2, C_{in}) \tag{5}$$

$$Sum = MAJ3(\overline{C_{out}}, MAJ3(x_1, x_2, \overline{C_{out}}), C_{in}). \tag{6}$$

In our previous work we disregarded the gate output readout mechanism, which we discuss in the next section after introducing our device model.

III. Threshold Logic Majority Gate

The proposed device architecture is depicted in Figure 2. It contains an RF generator (P), three phase-shifters (x_i), and a readout transducer (Φ). An amplifier transducer (Amp) is placed before the readout element. This amplifier is necessary to modulate the SW amplitude depending on its phase compared to the reference by means of parametric amplification. We shortly introduce this concept, but for more information on this matter we refer the reader to [9]. In essence, the component that is along the waveguide magnetization axis, in our case the x component oscillates at double

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the SW frequency. This occurs because a SWs magnetization vector does not move in a circular motion around its axis, but in an elliptic motion. So, when a SW is travelling on a waveguide, on any point on that waveguide with SW, applying an external excitation on the x-axis with double the frequency of the SW, creates two new SWs that are locked to the original SW. Their wavelength and frequency is the same, but their phase depends on the phase difference between amplified and input SW. The amplification follows a sinusoidal form as presented in Equation (7).

$$I = A_0 + (A_{s,0} + A_a) * A_a * cos(\Delta\phi_{sp} - \pi/2), \qquad (7)$$

with $A_0 = ((A_{s,0} + A_a)^2 + A_a^2)/2$, $A_{s,0}$ being the amplitude of the original SW, and A_a being the amplitude of both the created signal and idler wave. In this way, if the input SW is phase shifted by a certain amount by the phase-shifters, the amount of amplification changes which we can read out. To verify this behaviour we present our simulation results in the next section.

IV. Simulation Results

We utilized *mumax*^{3} [13] to simulate the spin-wave propagation and demonstrate proper device functionality. The considered magnetic waveguide is $20\,\mu\mathrm{m}$ long, $1\,\mu\mathrm{m}$ wide, and $50\,\mathrm{nm}$ thick discretized into 2048 by 256 by 4 cells, respectively. Each of these values were utilized in the earlier work of Bracher et al. [9], except for the thickness for which we found $50\,\mathrm{nm}$ a more appropriate value. On each edge we increase the damping parameter α to stop SWs from reflecting on the edges. We considered the following material parameters: magnetic saturation $140 \times 10^3\,\mathrm{A/m}$, $3.5 \times 10^{-12}\,\mathrm{J/m}$ exchange constant, and a Gilbert magnetic damping of 0.005, all values for YIG from [9]. We extracted the dispersion relation depicted in Figure 4, which clearly displays the different SW modes. We further extracted the numeric dispersion relation and selected 3.3 GHz for input SW frequency as at this frequency only a single wavelength exists in mode 1 and no SW of higher modes would be generated. At $3.3\,\mathrm{GHz}$ we have a wavelength of $277\,\mathrm{nm}$ and a wave velocity of $308\,\mathrm{nm/ns}$. The SW generating transducer is placed at $x = 5\,\mu\mathrm{m}$ and is $100\,\mathrm{nm}$ wide and is simulated by applying an equally sized external magnetic field with a strength of $1\,\mathrm{mT}$. A snapshot image of the z-component (out-of-plane) of the magnetization recorded at $29.3\,\mathrm{ns}$ is presented in Figure 3, demonstrating the wave propagation in the waveguide.

The phase-shifters centers are positioned at $x_1 = 5.5\,\mu\mathrm{m}$, $x_2 = 7\,\mu\mathrm{m}$, and $x_3 = 9\,\mu\mathrm{m}$ and each phase-shifter is $500\,\mathrm{nm}$ wide. The amplifier center is positioned at $x_a = 10\,\mu\mathrm{m}$ and it is $200\,\mathrm{nm}$ wide, and finally we position a $100\,\mathrm{nm}$ readout region with its center at $11\,\mu\mathrm{m}$. We start with verifying the working of the phase-shifters by applying a $1\,\mathrm{mT}$ field along the waveguide long axis on the phase-shifters which results in the wave phase shifting by 18° per shifter as depicted in Figure 5.

Subsequently, we turn on the amplifier after $29.29\,\mathrm{ns}$ of the SW with the shifters, which results in the formation of a signaler and idler wave which interfere with the running SW and amplify it with a strength depending on the phase shift. We then take the average amplitude of the SW (here we used the time interval between 38 and $41.5\,\mathrm{ns}$) and plot this value for different phase-shifter activation configurations in Figure 6. We can see a clear separation when turning on an extra phase-shifter and instead of applying a negative phase shift to account for -2 in Equation (4) and then checking the rotation angle, we can just set the readout threshold at 0.93. If the output signal is below, we read out a logic 1, otherwise we read a logic 0. As we read-out a voltage depending on the SW amplitude height, the thresholding operation translates into reading out the output voltage and comparing it with the established threshold value.

V. Circuit Level Analysis

As we demonstrated the SW Threshold Logic $MAJ3$ (SWTL $MAJ3$) gate full functionally it is of interest to get a glimpse on the potential impact of our proposal at the circuit level. To this end we consider a collection of representative logic circuits from the EPFL Combinational Benchmarking Suite [14]. Figure 7 summarizes the estimated energy, area, and area-energy product for both CMOS and SWTL $MAJ3$ based implementations of the benchmark circuits. The CMOS circuits are synthesised by means of commercially available tools and a $7\,\mathrm{nm}$ CMOS technology node. For the SW implementations we utilized MIG synthesis to determine the required $MAJ3$ count and assume the transducer power consumption values reported in [15].

For circuit area estimation we considered that each SWTL $MAJ3$ gate consists of 3 RF and 3 DC transducers. Assuming that each transducer occupies an area of F^2 and are separated by an inter port distance equal to F the total area of a SWTL $MAJ3$ device is $24\,\mathrm{F}^2$, i.e., $0.0216\,\mu\mathrm{m}^2$ and $0.0096\,\mu\mathrm{m}^2$ for F of $30\,\mathrm{nm}$ and $20\,\mathrm{nm}$, respectively.

The power consumption of the SWTL MAJ3 based implementations is determined by the power consumption of the utilized RF and DC transducers as SW propagation is free of charge in terms of power consumption. However, due to the current state of developments no experimental data are available. Some building blocks of the SW $MAJ3$ threshold logic gate were demonstrated experimentally, e.g., internal magnetic field control by DC voltages using magnetoelectric effect [16], or SW amplitude tuning by the relative phase difference between the traveling wave and an amplifier [9]. Moreover, we note that the underlying effects were demonstrated in large devices and using transducers that are not optimized for efficient energy consumption. It is clear the current based transducers, e.g., inductive antennas cannot be power effective [17], but, it is suggested in [18] that Magnetoelectric (ME) cells can potentially bring transducers power consumption into competitive ranges.

In view of the above, no realistic energy consumption figures can be derived for SWTL $MAJ3$ based implementation. threshold logic using the experimental data. Thus, we determine per circuit RF and the DC transducers energy consumption upper bounds that make SW implementations

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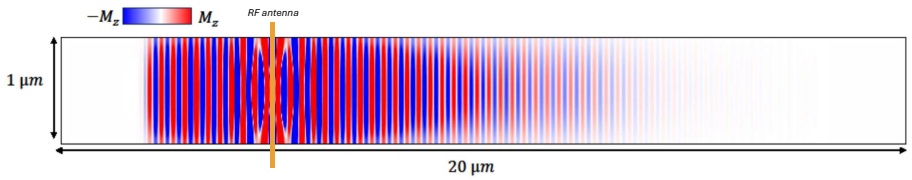

Fig. 3. Out-of-plane magnetization oscillation pattern snapshot.

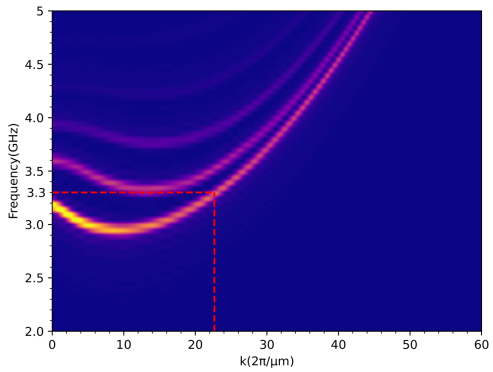

Fig. 4. YIG waveguide dispersion relation.

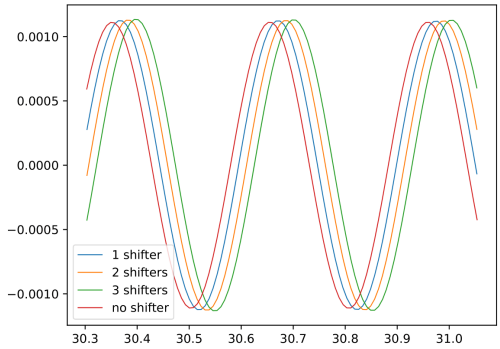

Fig. 5. Spin-wave signal at the output when turning on 1, 2, or 3 shifters.

able to outperform the CMOS counterparts in terms of energy consumption. As one can observe in Figure 7 the upper-bounds depend on the circuit complexity, the more complex the circuit the larger, thus more practically unachievable they are, which also imply that the larger the circuit the more advantageous the SW computing paradigm becomes. $\frac{EAP_{CMOS}}{EAP_{SW}}$ values range from 1.9 to 20 and from 0.8 to 9 for a feature size F of 20 nm and 30 nm, respectively. On average $\frac{EAP_{CMOS}}{EAP_{SW}}$ value is 5.25 and 2.2 for a feature size F of 20 nm and 30 nm, respectively, which clearly indicates that, if transducer technology will advance as expected, the proposed SWTL gate can open an avenue towards the practical realization of ultra low-power circuits able to outperform CMOS counterparts.

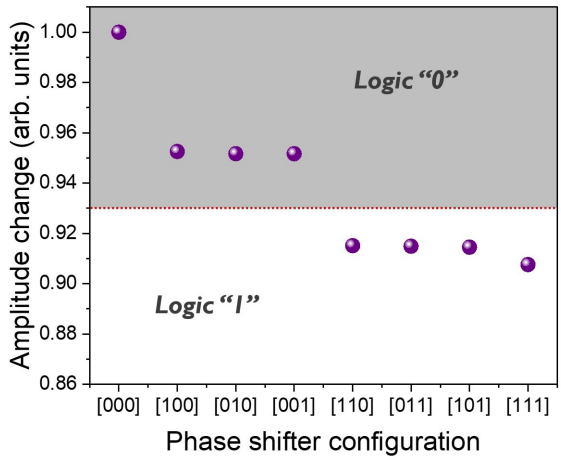

Fig. 6. Average relative amplitude between 38 ns and 41.5 ns. The relative amplitude for every gate input combination is presented while the red line determines the threshold value that discriminates the gate output logic value.

VI. Conclusions

In this paper we further developed the recently proposed Threshold Logic (TL) inspired Spin Wave (SW) device concept that relies on SW phase rotations for computation instead of SW interference. We assumed the implementation of a 3-input Majority gate as discussion vehicle and demonstrated its correct behaviour by means micromagnetic simulations. We introduced a method to embed the threshold processing into the readout stage instead of considering it as a gate input. To evaluate the potential circuit level impact of our proposal we utilized the proposed $MAJ3$ gate to implement a collection of representative logic circuits from the EPFL Combinational Benchmarking Suite and evaluate and compare their area, energy consumption, and Energy Area Product (EAP) with the ones of 7 nm CMOS technology node based counterpart implementations. Our estimations indicated that $\frac{EAP_{CMOS}}{EAP_{SW}}$ average value is 5.25 and 2.2 for a SW transducer feature size of 20 nm and 30 nm, respectively, thus SW based circuitry can potentially outperform state of the art CMOS counterparts.

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Circuit description	In	Out	CMOS			Spin-wave logic				EAP_{CMOS}/EAP_{SW}	
			Energy (fJ)	Area (μm^2)	EAP_{CMOS} (fJ × μm^2)	RF transducer energy (aJ)	Phase shifter energy (aJ)	Area (μm^2) F=30 nm	EAP_{SW} (fJ × μm^2) F=30 nm	F=30 nm	F=20 nm
Simple control unit for an arithmetic logic unit	7	26	0.23	4	0.93	0.68	0.22	1.85	0.43	2.1	4.8
Look-ahead XY routing function	60	30	0.27	3.92	1.09	0.31	0.10	4.70	1.30	0.8	1.9
11-bit integer to 4-bit mantissa/3-bit exponent float	11	7	0.72	6.47	4.66	0.88	0.29	4.38	3.16	1.5	3.3
Standard decoder function	8	256	0.26	12.43	3.32	0.22	0.073	6.56	1.75	1.9	4.25
Priority encoder	128	8	7.50	20.39	153.01	2.29	0.76	17.66	132.59	1.15	2.6
Context-adaptive variable-length coding	10	11	2.87	21	60.46	1.24	0.41	12.46	35.88	1.7	3.8
Controller (serial bus)	147	142	3.26	33.78	110.44	0.73	0.244	24.10	78.81	1.4	3.2
Blind Round Robin arbiter	256	129	24	191.5	4.5×10^3	0.87	0.29	147.46	3.5×10^3	1.3	2.9
Barrel shifter	135	128	46.20	81.5	3.7×10^3	4.09	1.36	60.89	2.8×10^3	1.3	3
128-bit adder	256	129	82.43	76.4	6.2×10^3	53.6	17.88	8.29	683.72	9	20.1
Memory controller	1204	1231	9.9×10^2	1074.8	1.06×10^6	6.1	2.03	876.57	8.6×10^5	1.2	2.75
Maximum finder in 4 x 128-bit in uts	512	130	1.9×10^2	111.6	2.1×10^4	20.3	6.77	51.53	9.9×10^3	2.1	4.9
Boolean function approximating the sinus trig. function	24	25	8.5×10^2	185.23	1.5×10^5	51.0	17.02	89.94	7.6×10^4	2	4.6
Majority voting of 1001 bits	1001	1	5.7×10^2	410.59	2.3×10^5	25.99	8.66	119.38	6.8×10^4	3.4	7.7
64-bit square (b=a2)	64	128	26.9×10^2	702.46	1.8×10^6	62.51	20.83	233.17	6.2×10^5	3	6.8
32-bit logarithm with base 2	32	32	14.2×10^3	1161.9	1.6×10^7	148.27	49.42	519.22	7.4×10^6	2.2	5
64-bit combinational multiplication of unsigned integers	128	128	7.4×10^3	1023.4	7.6×10^6	98.48	32.82	407.82	3×10^6	2.5	5.6
128-bit square -root integer approximation	128	64	$15.\times10^4$	1237.2	1.8×10^8	2017.80	672.60	410.03	6.2×10^7	3	6.8

Fig. 7. List of circuits with their description including the number of their primary inputs and outputs. The estimation of Energy, area, and energy-area product (EAP) estimates for CMOS and SWTL are presented. EAP for SWTL implementations is calculated for a feature size of 30 nm, whereas EAP_{CMOS}/EAP_{SW} ratio is estimated for both 30 nm and 20 nm feature size values.

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