Model and Design Differential Power Processing

P-DPP PV2VB architecture

Author
Taian Liu - 5523893

TU Delft
Faculty EEMCS
SET3901

Delft, Date: 26-09-2023
Sustainable Energy Technology

Model and Design Differential Power Processing

P-DPP PV2VB architecture

by

Taian Liu

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Tuesday September 26th, 2023 at 13:00.

Student number: 5523893
Project duration: November, 2022 – September, 2023
Thesis Committee:

Dr. Jianning Dong,	TU Delft, Assistant Professor, DCE&S
Prof. Ivan Gordon,	TU Delft, Professor, PVMD
Dr. Patrizio Manganiello,	TU Delft, Assistant Professor, PVMD &Main Supervisor
Afshin Nazer	TU Delft, PhD candidate, PVMD & Daily supervisor

An electronic version of this thesis is available at .

TU Delft

Abstract

Photovoltaic (PV) systems are often exposed to mismatch conditions caused by partial shading, different mounting angles, dust accumulation, cell degradation, etc. Among various techniques, PV to Virtual Bus Parallel Differential Power Processing (PV2VB P-DPP) has been proposed to overcome the mismatch among PV strings.

This thesis focuses on the dynamic behavior of the PV2VB P-DPP configuration in order to analyze the system stability and design appropriate controllers. Configuration needs to control two different types of converters: 1- P-DPP converters (inner control loop) and 2- the Central Converter (outer control loop). Moreover, since the selection of capacitance for the virtual bus is a tradeoff between several factors, such as cost, stability, reliability, current ripple, and so on, this thesis provides a methodology to identify an acceptable range for the capacitance of the virtual bus.

This project used the state space representation to model the system owing to its simplicity and ability to provide a uniform and convenient starting point for linearization, stability evaluation, control design, and simulation. Since the system's large signal model is nonlinear and difficult to work with, we linearized the state space equations (to achieve the small-signal model of a PV2VB P-DPP system consisting of any number of strings and converted them into the Laplace form to perform system analysis and controller design. Considering Gain and Phase Margin as the main design criteria, proportional control (K_p) and integral control (K_i) were tuned for PI controllers using the SISO-tool MATLAB toolbox for a PV system consisting of two PV strings. The system stability depends on two main aspects: the value of the virtual bus capacitor (C_{VB}) and the voltage magnitude in the virtual bus (v_{VB}). The complete developed model has been implemented in MATLAB.

For the simulated PV2VB P-DPP system, a gain margin of 15.7 dB, a phase margin of 121 degrees, and a settling time of 0.8 s have been achieved for the outer control loop (central converter) by setting K_i and K_p to $5s^{-1}$ and 0.5, respectively. On top of that, a gain margin of infinity dB, a phase margin of 91.2 degrees, and a settling time of 1 ms have been achieved for the inner control loop (DPP converter) by setting K_i and K_p to $10s^{-1}$ and 0.1, respectively Finally, it is shown that the virtual bus capacitor should be selected within the range $50\mu F$- 5mF, in order to make the system, have higher stability margin. However, the final selected value of capacitance for the virtual bus is equal to 1.2 mF owing to other constraints, such as the expected ripple current.

- Delft, 19^{th} September 2023
- Taian Liu

Acknowledgements

This report is the final assessment of my master's program in Sustainable Energy Technology (SET) at the Delft University of Technology. The thesis title is Modeling and Design of PV to Virtual Bus Parallel Differential Power Processing Configuration for Photovoltaic Applications. My Electrical and Electronic Engineering background shaped me into a solid foundation for power electronics. In the Set program, I focused on Wind, Storage, and Solar; then, I realized that mismatch conditions, such as shading, can significantly impact the PV system, especially the urban area. Therefore, I became curious about how g differential power processing can tackle PV system shading issues to maximize efficiency.

I would like to express my deepest appreciation and gratitude to all those who have supported and contributed to the completion of this thesis project.

First and foremost, I would like to thank my daily supervisor Afshin Nazer, for their invaluable guidance, expertise, and continuous support throughout this research endeavor. His insightful feedback, encouragement, and unwavering dedication have been instrumental in shaping this work. In particular, one regular progress meeting lasted over seven hours to resolve an error code. Secondly, I would like to thank Dr. Patrizio Manganiello, the supervisor of this project. He shares expertise and gives constructive suggestions. His unwavering support and encouragement provided a much-needed moral boost throughout this journey. Moreover, I would like to thank Dr. Jianning Dong and Dr. Prof. Ivan Gordon for being part of my Msc thesis committee.

Finally, I would like to thank my parents and friends for their financial and mental support during 2 years study in TU delft.
Taian Liu
Delft, September 2023

Contents

List of Symbols

I_{mpp}	Maximum Power Point current
I_{sc}	short-circuit current
V_{mpp}	Maximum Power Point voltage
V_{oc}	Open-Circuit Voltage
AC	alternating current
BLC	(bridgeless converter
DAB	dual active bridge
DC	direct current
DMPPT	distributed maximum power point tracking
DPP	differential power processing
FPP	full power processing
GM	gain margin
KCL	kirchhoff Current Law
KVL	kirchhoff voltage Law
MIC	modulue integral converter
MIMO	multiple-input-multi-output
MISO	multiple-input-single-output
MMCI	modular Multilevel Cascade Inverters
MPP	maximum power point
MPPT	maximum power point tracking
P-DPP	parallel differential power processing
PM	phase margin
PV	photovoltaic
PV2PV	PV to Bus
PV2PV	PV to PV
PV2PV	PV to virtual bus
S-DPP	series differential power processing
SLC	string level converter
SP-DPP	series and parallel differential power processing
TCT	total cross tied

1 Introduction

1.1 Background and Motivation

Since the Industrial Revolution, people's life has changed radically. In the agricultural sector, farmers use fertilizers and pesticides to increase yields to manufacturing techniques, from manual to mechanical production. In the transport system, from the use of animals to the replacement of steam engines. The advent of the steam engine facilitated trade, accelerated urbanization, and connected the regions in a way that had never been done before. Developments throughout this period laid the foundations for the modern industrialized society we live in today.

Since the Industrial Revolution began, energy consumption has grown exponentially. Figure 1 shows the global primary energy consumption from 1800 to 2022. It is noted that the energy demand has increased rapidly since the 1950s. The main reasons for this increase in energy consumption are economic development, population growth, and technological developments[1]. As shown in Figure 1, most energy is provided by fossil fuels. In the future, there are two ways to tackle growing demand. One way is to continue exploiting fossil fuels like oil and natural gas to meet growing demand, but it has two main problems. The first one is that fossil fuels are a finite resource that will one day be depleted. The second problem is that when fossil fuels are burned, they release large amounts of carbon dioxide, a greenhouse gas, into the air. Greenhouse gases trap heat in our atmosphere, causing global warming and increasing the probability of extreme weather, such as heat waves and floods. Another way is to supply energy with renewable energy like hydro, wind, biomass, and solar. Compared with fossil fuels, renewable energy is cleaner and more sustainable than fossil fuels[2]. Among renewable energies, solar energy has overwhelming potential compared with other renewable as shown in Figure 2.

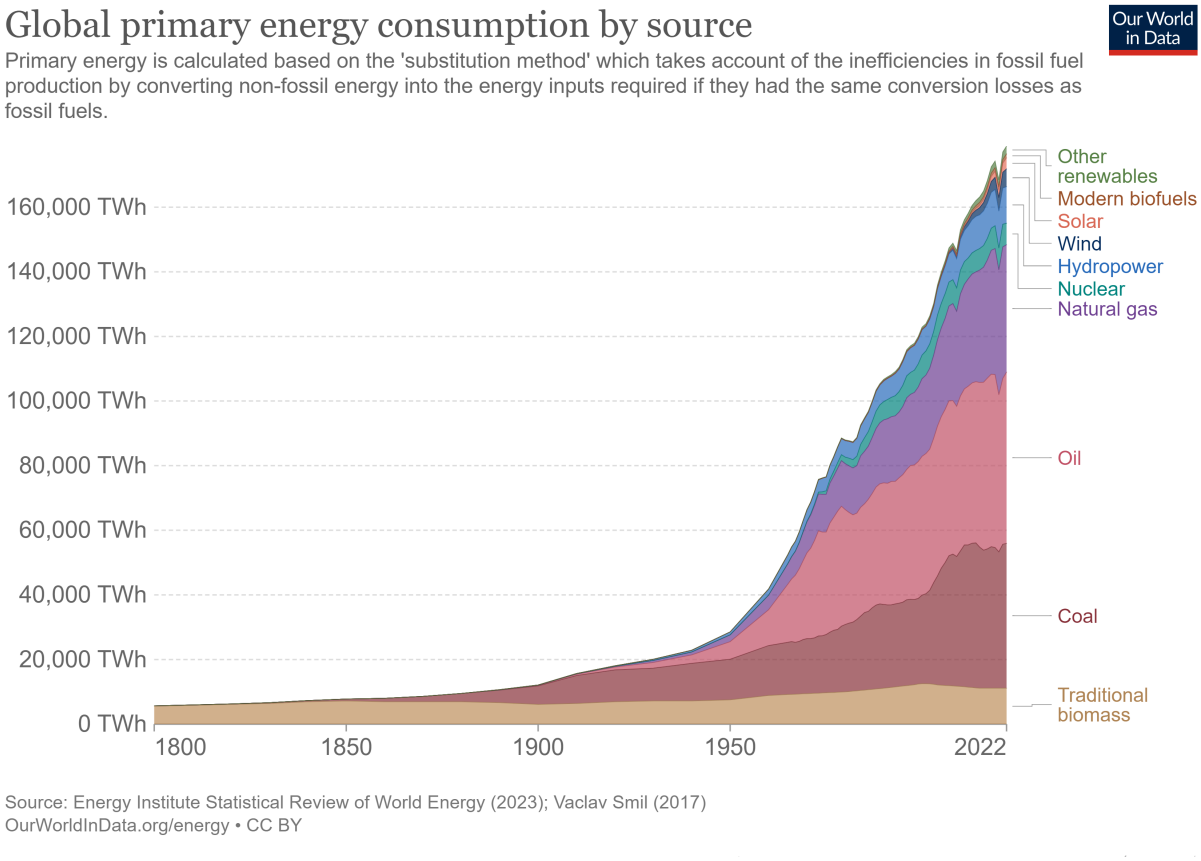


Figure 1: Global primary energy consumption by source [3]

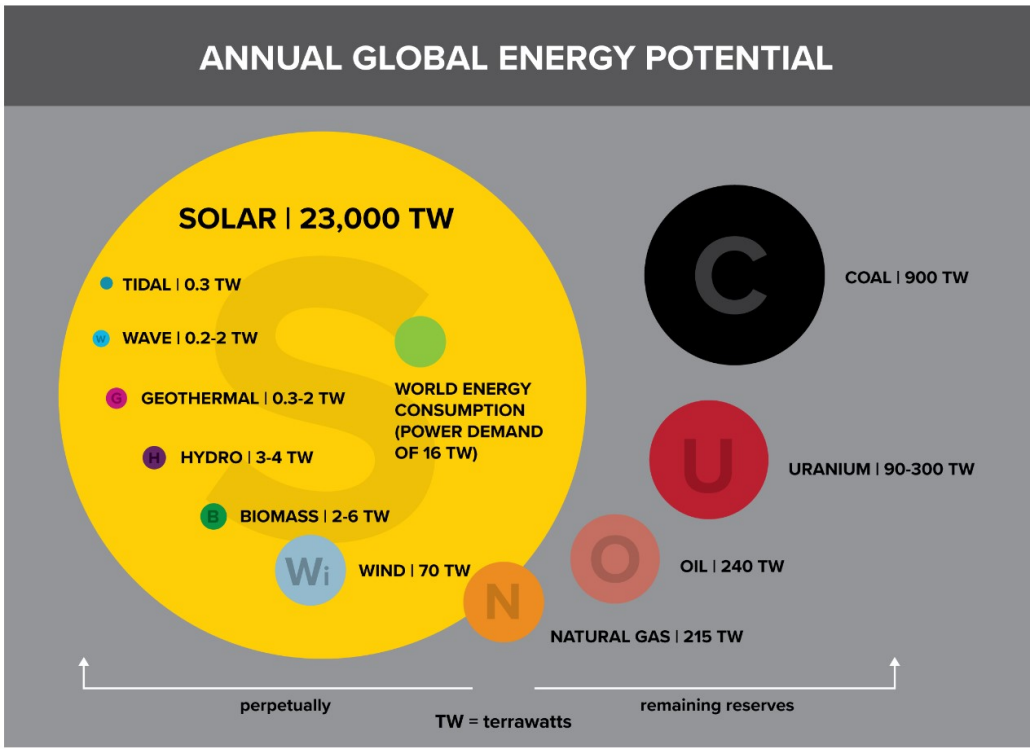


Figure 2: Annual global energy potential [4]

Compared to fossil fuels, PV systems have several advantages:(i) free energy from the Sun, (ii) no carbon emission when generating power, (iii) low-maintenance costs, (iv) silent, (v) easy to install. However, solar energy has a few downsides:(i) low efficiency, (ii) weather dependence, (iii) intermittent power generation, and (iv) occupying a substantial amount of space. Therefore, providing a high-efficiency PV system that harvests as much energy from the Sun is critical to increasing the rate of return.

The PV cells are traditionally connected in series to form strings of cells, hereby called PV submodules. Then, the PV submodules, usually three, create PV modules with connected three bypass diodes in parallel available in markets. Following, PV modules are connected in series to form a PV string. PV strings can be expanded by paralleling them and creating PV arrays. Figure 3 shows a typical PV module schematic containing 60 cells connected in series with three bypass diodes. Notably, partial shading, panels at different tilt angles, dust accumulation, or cell degradation leads to mismatched conditions. This thesis considers shading the main reason for the mismatch condition. Hot spots or mismatch losses can occur, for instance, if a PV cell is shaded by a leaf falling from a tree (shown in Figure 4). The earliest approach to solve the problem is Bypass diodes conventionally parallel with the PV sub-module. Although the bypass diodes provide a new path for the current and reduce the probability of hot spots, there will still be mismatch losses. In other words, in the example shown in Figure 4, the PV module loses one-third of the power even though a leaf covers only a single PV cell[5].

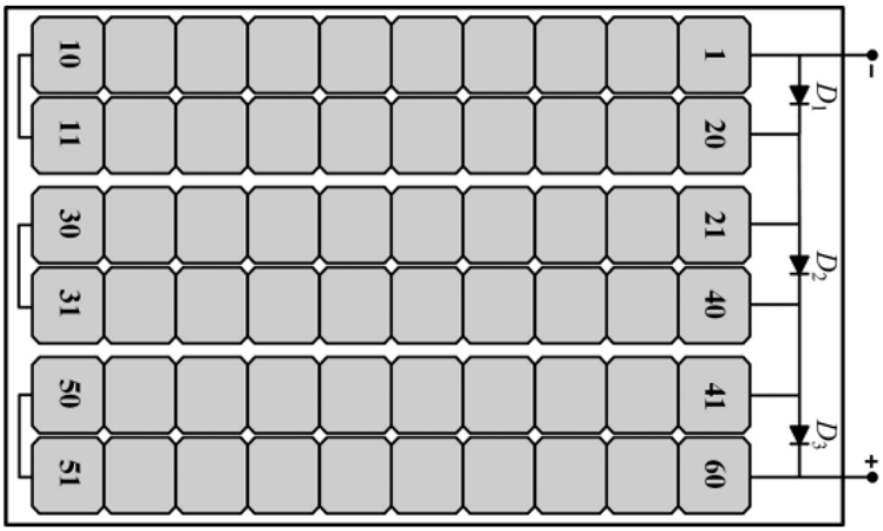


Figure 3: Schematic representation of a 60-cell PV module with 3 bypass diodes

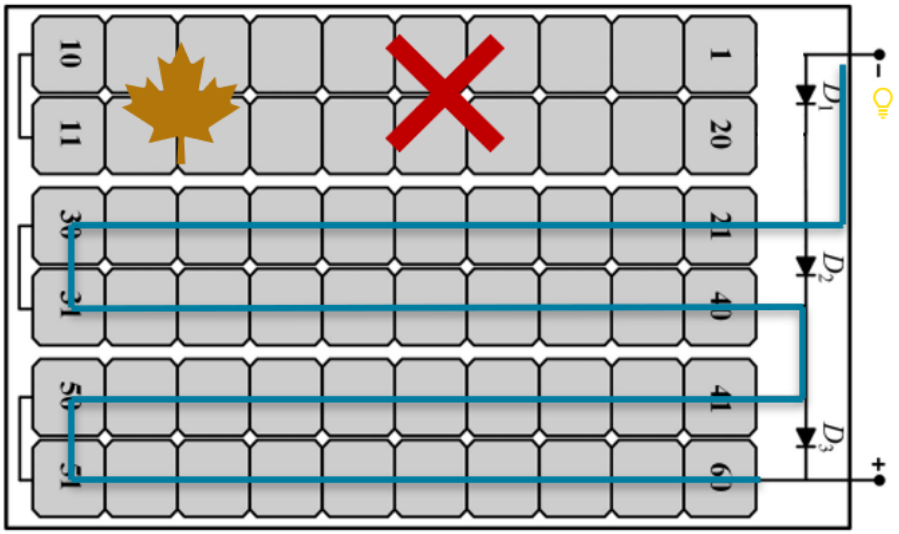


Figure 4: A leaf causes shading on PV cells (marked by the red 'X'). The blue line indicates an alternate path for current, addressing power loss due to shading. Enhancements are suggested for its alignment with active diode D1 and visibility. The figure illustrates shading effects and the proposed solution

The mismatch between PV strings is a critical challenge in PV systems. Because shading effects can lead to differences in the performance of individual PV strings, this mismatch results in uneven power generation, reducing the overall efficiency of the PV system. Addressing this issue is essential to ensure consistent energy production, optimize system performance, and achieve the full potential of PV energy conversion.

A novel parallel differential power processing (P-DPP) configuration, called PV to Virtual Bus (PV2VB), has been introduced by the Photovoltaic Materials and Devices group to minimize mismatch-related losses among PV strings. The configuration allows the use of blocking voltage semiconductors, so not only does it help to reduce the cost of switches, but it also enables designers to use MOSFETs instead of IGBTs. Compared with IGBTs, MOSFETs work at higher frequencies, reducing the volume and cost of passive elements[6].

This configuration needs a virtual bus as an input for all P-DPP converters. In other words, like the power exchange central, the capacitor dispatches the power from one string to another. Therefore, using capacitors at the Virtual Bus

is crucial to transfer energy among PV strings. The design of such a virtual bus is not trivial since it must deal with conflicting requirements. For instance, a more significant capacitance allows the store of more energy and will lead to a more stable virtual bus voltage. However, the capacitance is limited by cost and safety considerations. Furthermore, a high virtual bus voltage reduces the required capacitance because the maximum allowable voltage ripple increases, and more energy can be stored. Therefore, more energy will be used during the transient response, making the system more resilient to changes in operating conditions. Besides, the conduction losses of the DPP converters will be decreased by reducing the current. However, high Virtual Bus voltage requires semiconductor devices with higher blocking voltage, which imposes extra costs and switching losses.

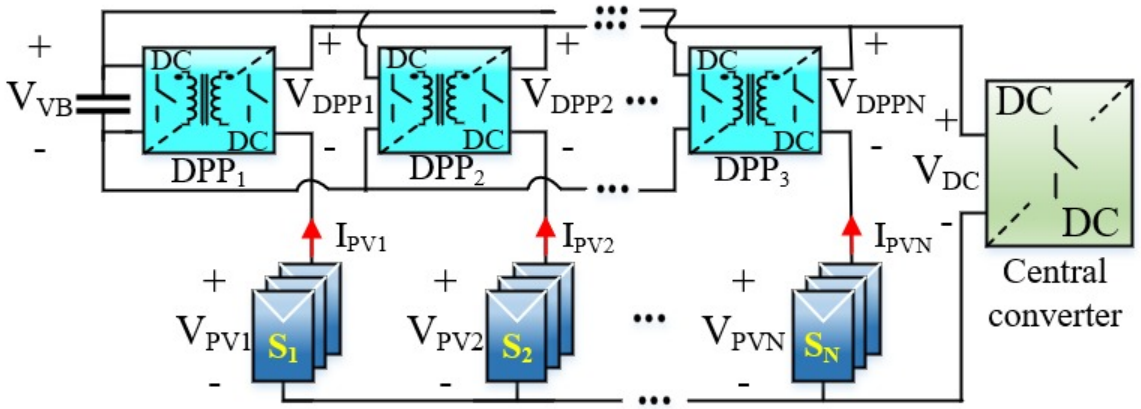


Figure 5: P-DPP PV2VB

The dynamic behavior of a power electronic system, including transient response, stability, reference tracking, load disturbance suppression, noise suppression, and tuning, is closely related to using a Proportional-Integral (PI) controller. The ability of the PI controller to adjust the control signals based on the error between the desired output and the actual output plays a critical role in achieving the desired performance of the power electronic system.

Moreover, A PI controller plays a crucial role in various control systems. Develop a PI controller algorithm tailored to the specific requirements of the PV2VB P-DPP configuration. The controller should incorporate proportional and integral components to manage errors and provide suitable control action effectively. Optimized tuning of the PI controller gain is critical to achieving the desired system performance. The proportional gain determines the controller's response to immediate errors, while the integral gain addresses the problem of long-term error accumulation.

The main objective of this project is to analyze the dynamic behavior of the PV2VB P-DPP configuration comprehensively. This encompasses investigating system stability and designing suitable controllers. Four steps need to be completed to achieve the main objective.
(i) We model PV2VB P-DPP configuration with a state space approach, then linearize it if necessary. In other words, we obtain the configuration's large and small signal models.
(ii) We obtain the state space equations into the Laplace form, then derive the transfer function for DPP converters and the central converter. With the transfer function, we design a robust PI controller for a central converter and DPP converters.
(iii) Analysis of the transient behavior. The analysis of transient behavior involves the simulation of how the systems respond to the shaded PV module.
(iv) Select the proper value of the capacitor in the virtual bus.

1.2 Key research question

The subject of this thesis is the modeling and design of PV2VB P-DPP. Some key research questions used as milestones throughout the project were formed based on the objective. Those questions are:

1- Which methodology must be applied to model the configuration?
2- In P-DPP PV2VB Architecture, Which parameter will affect the dynamic behavior?
3- How to apply the mathematical equation to design robust controllers?
4- Is there a range for the Virtual bus capacitance, or the more (or less), the better?
5- How to fine-tune the PI controller parameters in the controller design?

1.3 Thesis structure

The following chapter constitutes the report of this thesis. First, Chapter2 comprehensively reviews the different DMPPT techniques such as Micro inverters, MMCI, parallel, series, and TCT, series DPP, parallel DPP, and series-parallel DPP configurations. In chapter3, a model of PV2VB P-DPP Architecture details steady-state; then, it elaborates the methodology used to achieve dynamic modeling of the configuration. In the next step, the elaborated analysis's findings are provided in chapter4,. Chapter5 provides summarizes the thesis. Finally, chapter6 offers suggestions for further research.

2 Literature review

This chapter comprehensively reviews the state-of-the-art DMPPTs. subsection 2.1 discusses the MPPT algorithm and how it makes PV elements work at their MPP to maximize energy harvesting. subsection 2.2 shows the details of DMPPT at different levels of granularity. An introduction and comparison of the DPP and FPP configurations are provided in subsection 2.3. In particular, the P-DPP PV2VB architecture is introduced, and this architecture will be implemented in Chpater3 and Chapter4.

2.1 MPPT algorithm

As shown in Figure 6, a generic I-V curve and the associated P-V curve of PV has a maximum power point, and this maximum power point corresponds to a specific voltage and current called V_{MPP} and I_{MPP} respectively. Due to the irradiance or temperature change, the I-V and the P-V characteristics and the position of the MPP will change[7]. Figure 7 shows the effect of temperature change from 0 to 75 degrees. As the temperature rises, the short circuit current slightly increases, but the open circuit voltage drops significantly. Also, the maximum power decreases when the temperature rises. The irradiance will affect even more than the temperature of the I-V and P-V curves, as shown in Figure 8. Therefore, changes in the I-V curve have to be tracked continuously such that the operating point can be adjusted to be at the MPP after ambient conditions change[7]. The MPPT algorithm does this process.

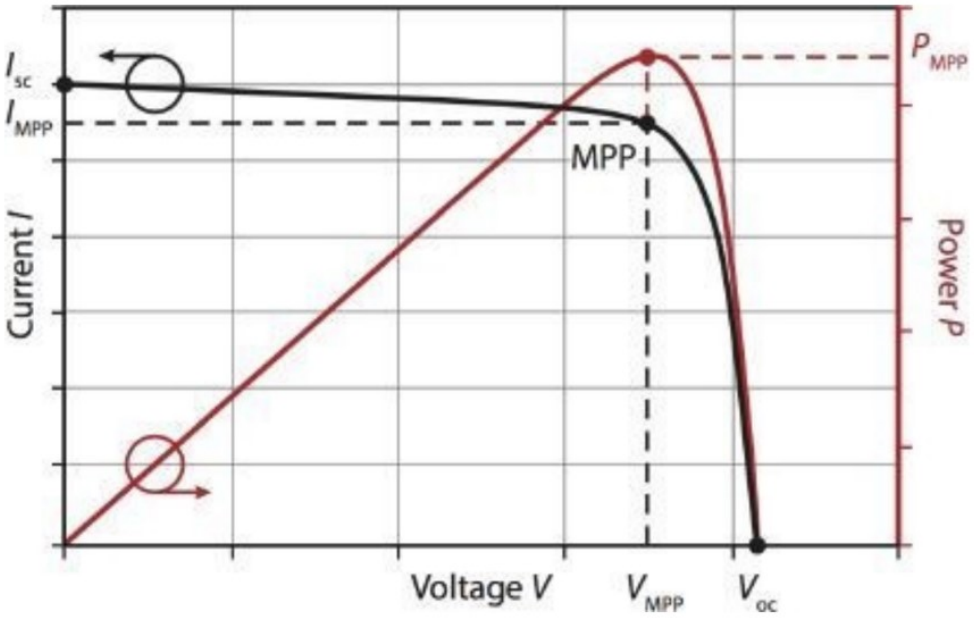


Figure 6: A generic I-V curve and the associated P-V curve. The maximum power point (MPPT) is indicated [7]

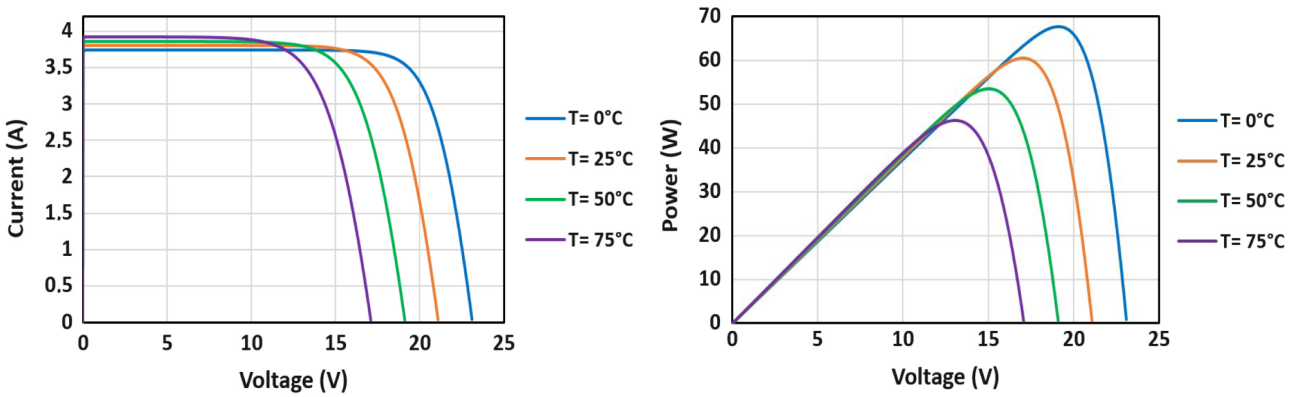


Figure 7: I–V and P–V characteristics for different values of temperature [8]

MPPT algorithms can be distinguished into two types: direct and indirect. Figure 9 shows some Direct and Indirect methods. The main difference between these two is that Direct MPPT requires IV characteristics, whereas indirect

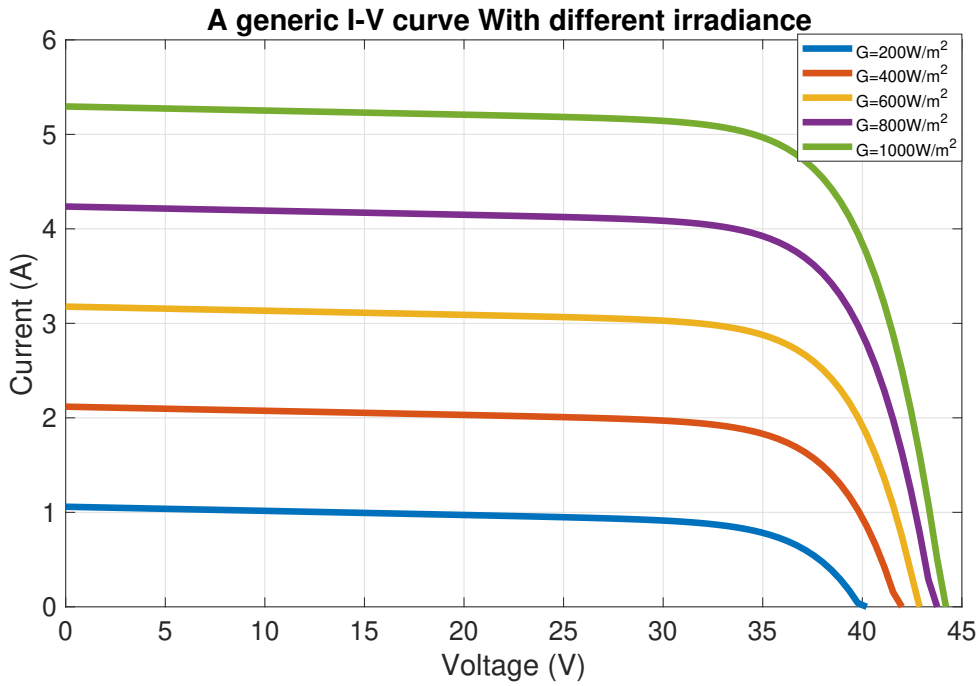


Figure 8: A generic I-V curve of a solar cell With irradiance

does not. Indirect MPPT located the position of the MPP is estimated via a hard-coded algorithm[7]. On the other hand, Direct MPPT is based on the IV curve to determine the MPP. Perutb and Observe and Incremental Conduction methods belong to the direct method, while Constant voltage, open circuit voltage, the short current method, and temperature method belong to the Indirect Method. More information can be found in the [9].

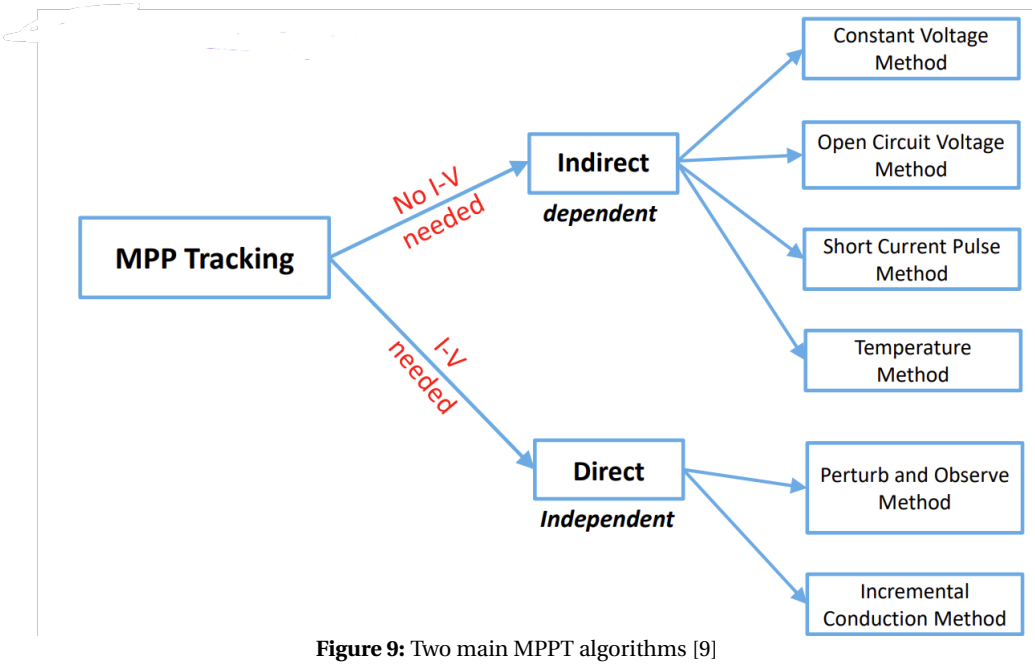


Figure 9: Two main MPPT algorithms [9]

2.2 DMPPT at different levels of granularity

In general, DMPPT solutions have been proposed at all different levels of granularity[10]. DMPPT PV architectures include four granularity levels – string level, module level, submodule level, and cell level[10]. Figure 10 shows DMPPT PV system architecture.

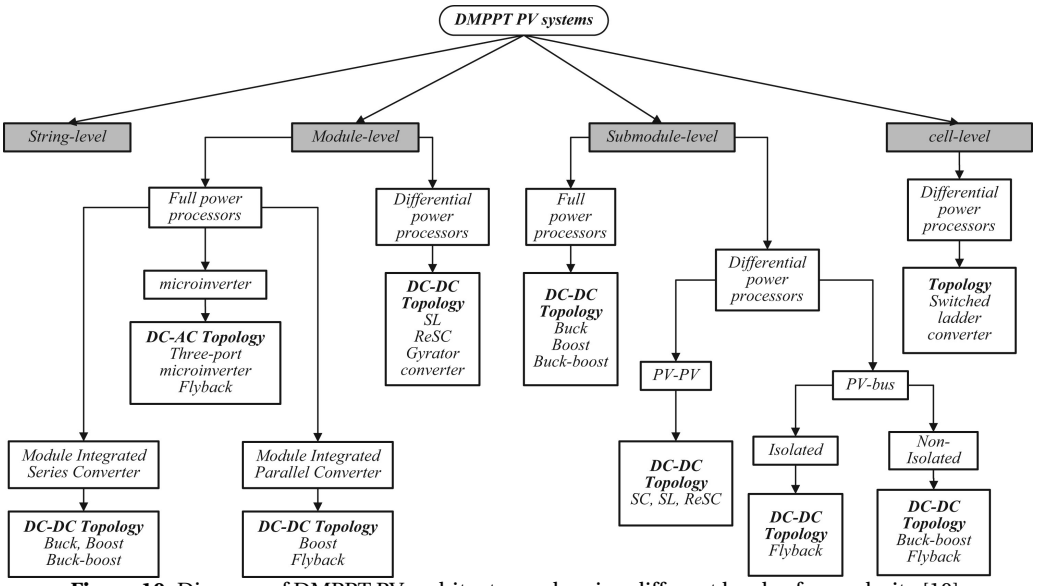
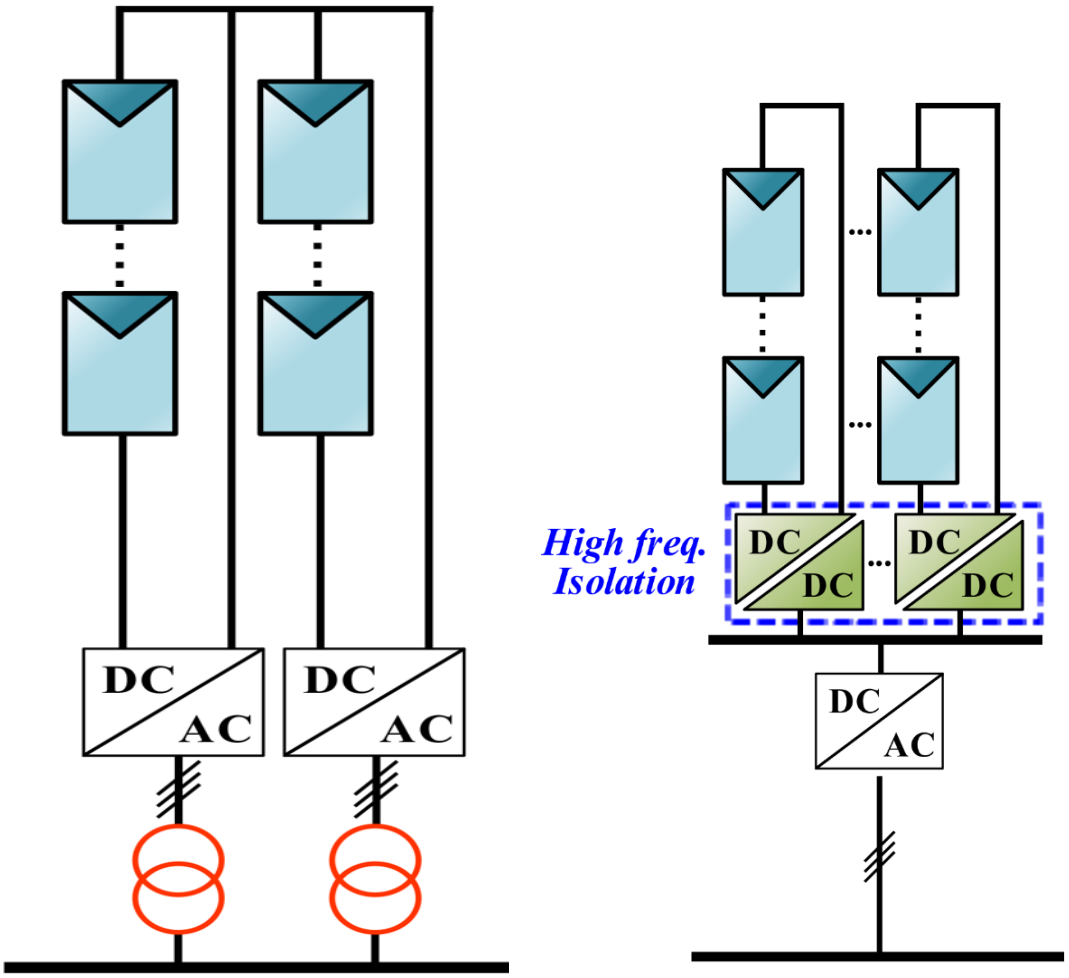


Figure 10: Diagram of DMPPT PV architectures showing different levels of granularity [10].

String level DPMMT

String level DMPPT is the lowest level of granularity in DMPPT PV architectures. The string level DMPPT has two main architectures: single and multi-string inverters. In the former, an inverter is connected to each PV string, and the voltage converts from DC to AC in a single inverter. That's why it's called single-string inverters (shown in Figure 11a). Another structure is called a multi-string inverter[11]. The PV string first connects to a common DC link via string level converters[12]. Then, The DC link directly connects the central inverter to the grid, transforming the voltage from DC to AC (shown in Figure 11b).

In general, in an MPPT at a string level, when a PV string experiences mismatch conditions, resulting in the PV modules not working on their MPP because the converter tracks the PV string's MPP instead of the PV module's MPP. In other words, the current generated by the PV string is determined by the most shaded solar module. As a result, string and multi-string DMPPT architectures can only mitigate mismatches among PV strings but not among PV modules[13].



(a) Single String structure [14] **(b)** Multi-string structure with isolated DC-DC converters [14]

Figure 11: String level DPMMT configuration

Cell level DPMMT

In contrast to string-level DMPPT, cell-level DMPPT allows for the highest granularity. Figure 12 shows an example of a PV cell integrated with an MPPT controller and a boost converter because the PV cell generates a relatively small amount of voltage.[15] To connect the grid directly, the voltage needs to step up. The main advantage of cell-level DMPPT is that MPPT can track the maximum solar cell power for every cell, so there are no mismatch losses. However, three main challenges exist: 1- having one converter per cell would require many power conversion units, increasing the system's complexity and cost; 2- With current technology, it is difficult to scale down the power rating of converters to the level of PV cells; and 3- the wire connection for every cell is complex.

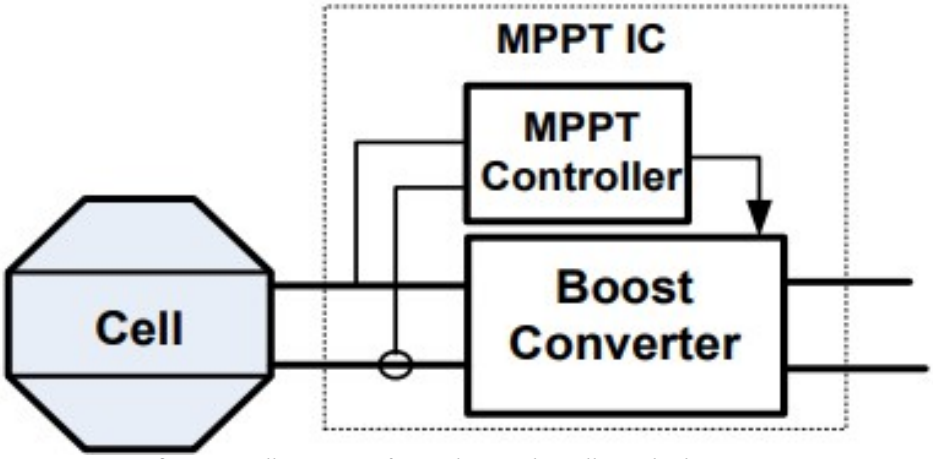


Figure 12: Configuration illustration of a single PV solar cell attached to MPPT IC [16].

The most common applications in DMPPT PV systems are at module and sub-module level. As the previous paragraph describes, Cell-level DPMMT is challenging to achieve in practice. Compared with string level DMPPT, if one PV module is partially shaded while other PV modules receive full sunlight, string level inverter tracking may force the entire string to operate at the MPP of the shaded module, resulting in energy loss. Module-level tracking allows each PV module to be adjusted independently, minimizing the effects of shading and maximizing overall energy output. Moreover, since the voltage of the PV submodule and module are higher than the PV Cell, higher efficiency for power converters will be accessible. As a result, module and submodule-level power converters have got the researcher's and industry's attention. The SMA company states that depending on the severity of the mismatch condition, a Micro inverter that performs module-level MPPT offers higher efficiency (1 – 4%) compared to the String level inverter [17]. Besides, compared with string-level conversion, module-level monitoring and data gathering help to diagnose faults quickly, and small-size packed module-level converters help technicians readily replace them, so repair time and availability will be improved[18].

2.3 DMPPT techniques at string, module, and sub-module level

There are two types of power processors for the various levels of DMPPT; one is called FPP, and another is called DPP. FPP converter must be able to handle 100% of the power generated by a PV module or a PV sub-module. Conversely, The DPP only needs to process a fraction of the power generated by the PV module or sub-module. In section subsubsection 2.3.1, the details of FPP will be discussed. Information about DPP can be found in Section subsubsection 2.3.2.

2.3.1 FPP

FPP converters can be divided into two major classes: AC-FPP and DC-FPP. Figure 13 shows the branch of DC-FPP and AC-DPP.

AC-FPP
As the name implies, AC-FPP converts DC to AC; in other words, The AC-FPP inverter 100% of the power is processed of the DC power generated by photovoltaic power generation into AC power. From Figure 13, AC-FPP is split into two categories: Micro inverters and MMCI. Micro inverters are generally applied to low voltage applications, such as the type of electricity used in most household and commercial applications.[20] Conversely, MMCI is mainly applied to high-voltage applications. Because MMCIs are used by high voltage applications, MMCIs are used in several typical practical applications: high-voltage direct current (HVDC) transmission grid integration of offshore wind farms and substations and grid connection, etc[21].

(i) **Micro inverters**
Since the name mentions 'micro', the size of the Micro inverter is small relative to MMCI. This leads to one of the advantages: the Micro inverters are easy to install at the back of the PV module and connect in parallel. [20]. These features increase flexibility, modularity, scalability, and lower installation costs.[22] Figure 14 displays a typical con-

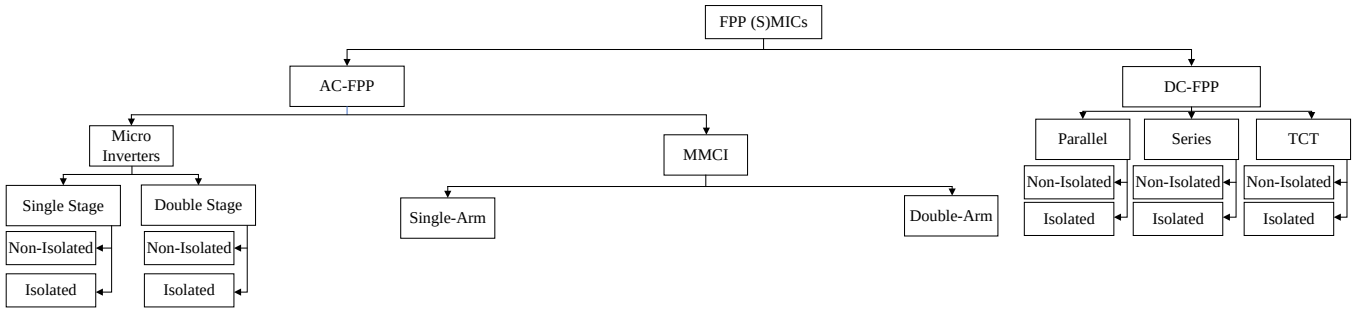


Figure 13: FPP-DMPPT classification [19].

figuration of Microinverters attached to the PV module. It shows that each inverter connected corresponds to the PV module, and there is no connection adjacent to the PV module. Since each PV module is independent, Micro inverters reduce the impact of a single point of failure. If one Micro inverter fails, the rest of the system can continue functioning. Moreover, adding or replacing panels is more accessible because each panel operates independently. This facilitates system expansion or modification.

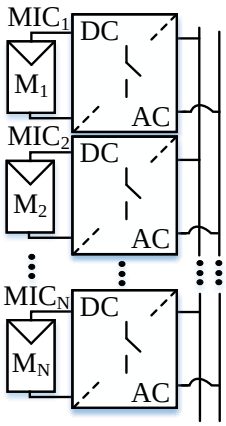


Figure 14: Micro inverters configuration, M_i indicates the i^{th} PV module and MIC_i indicates the i^{th} micro inverter in a PV system [19].

To continue distinguishing the Micro inverters, four main branches can be broken out (shown in Figure 13 left-hand part): Single-stage non-isolated, single-stage isolated, double-stage non-isolated, and double-stage isolated designs, respectively. To distinguish the single stage or double stage, The single-stage inverter combines the MPPT algorithm with DC-AC power conversion from the PV module to the grid. On the other hand, the inverter for the double stage, first the DC-DC converter stage, employs an MPPT algorithm. Moreover, The DC-DC converter adjusts the voltage level to match the optimal input voltage of the subsequent DC-AC inverter stage. This ensures that the inverter operates efficiently and produces high-quality AC power. Figure 15 shows the typical double stage in the Mirco inverter configuration. However, Implementing a two-stage conversion system requires additional components, circuits, and control systems for both the DC-DC and DC-AC stages. This complexity leads to higher manufacturing and maintenance costs. The main difference between a non-isolated converter and an isolated converter is the presence or absence of galvanic isolation between the inputs and outputs. Non-isolated converters regulate voltage levels directly without isolation, while isolated converters provide both voltage conversion and electrical isolation between input and output[23].

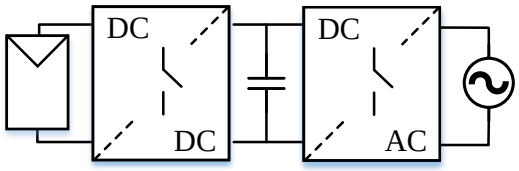


Figure 15: DC-AC double stage [24]

On the other hand, Micro inverters have some drawbacks. Each PV module generates a low voltage (less than 50 V), but the household grid requirement is 220/240 V. Consequently, the Micro inverter requires substantial voltage gain. For single-stage Mirco inverters, the major vulnerability is the grid power ripple flows in the DC Link, resulting in a double line frequency ripple in the DC Link voltage[25]. If the ripple phenomenon penetrates PV modules, the Micro inverter can hardly track the maximum power. As a result, using electrolyte high-capacitance capacitors for power decoupling is inevitable. These capacitors shorten Micro inverters' lifetime, increase cost, and reduce power density[26].

(ii) **MMCI**
MMCI is mainly applied to medium or high-voltage applications. Figure 16 displays an example of an MMCI configuration; One of the phases shows the detail of the inverter cluster, which consists of a PV sub-converter and bridge cells; these components can easily cope with electromagnetic interference (EMI)[27]. Since the size of the MMCI is greater than the micro inverter, it requires a smaller AC filter. Besides, micro inverters can only connect in a single phase, while MMCI can connect in single or three phases[28].

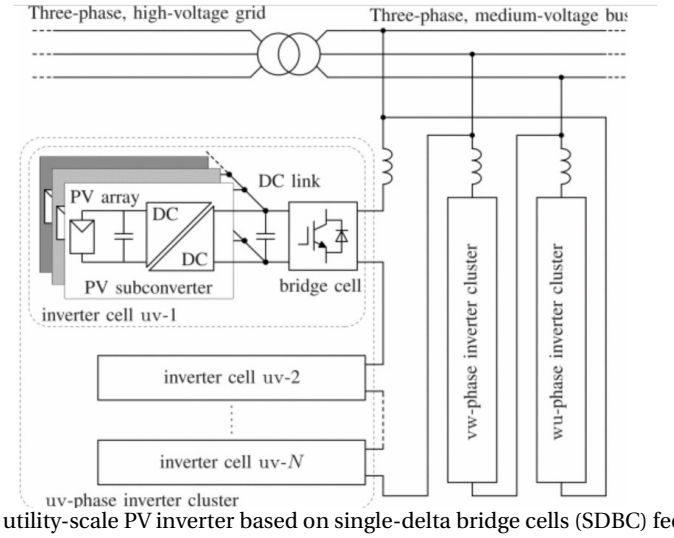
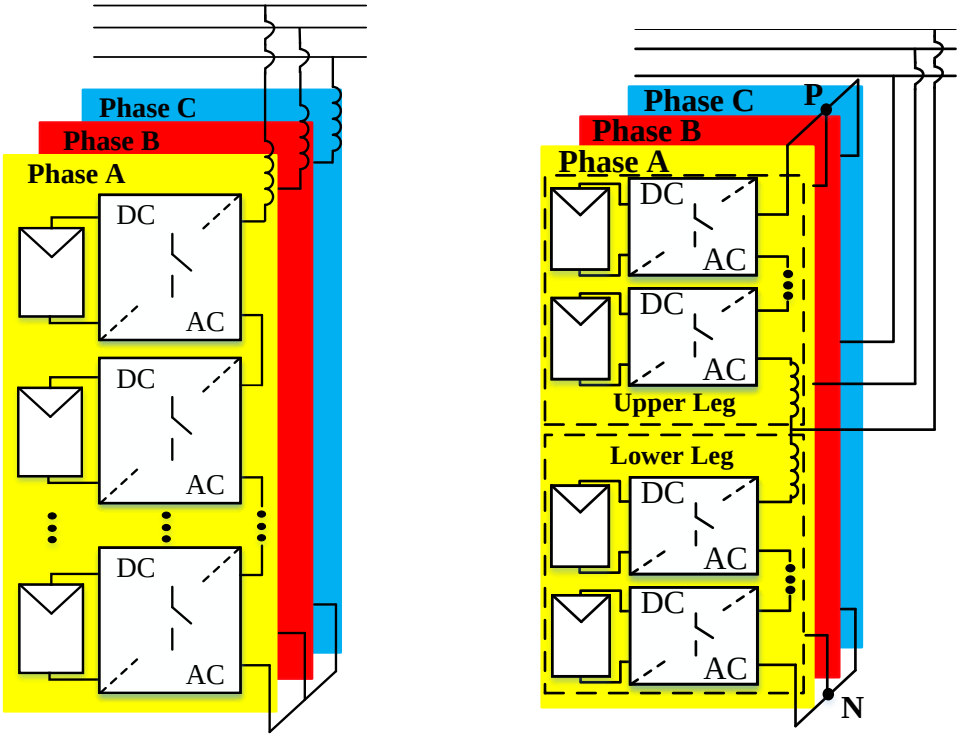


Figure 16: An MMCI utility-scale PV inverter based on single-delta bridge cells (SDBC) feeding an MV bus[29]

Generally, MMCI can be divided based on the number of leg inductors, single or double legs, namely single-arm or double-arm per phase. Figure 17a and Figure 17b show the single-arm and double-arm MMCI configuration respectively. In the single-arm configuration, the voltage can only be generated in zero or positive voltage. Undesirable DC voltage components are on the AC voltage side, resulting in harmonic distortion. On the other hand, the double-arm configuration does not have this issue because the AC voltage side is connected between two leg inductors. Therefore any DC voltage will be canceled out in the upper and lower inductors[30].

MMCI has one distinct disadvantage in terms of reliability. If a single device in an MMCI configuration fails, it can cause the entire system to fail. This susceptibility to a single point of failure raises concerns about the overall reliability of MMCI-based systems. In contrast, Micro inverters offer greater reliability by isolating a single point of failure and ensuring that the rest of the system remains operational despite a slight drop in power generation. In Table 1 displays the comparison between Micro inverters and MMCI.



(a) Single-Arm MMCI **(b)** Double-Arm MMCI

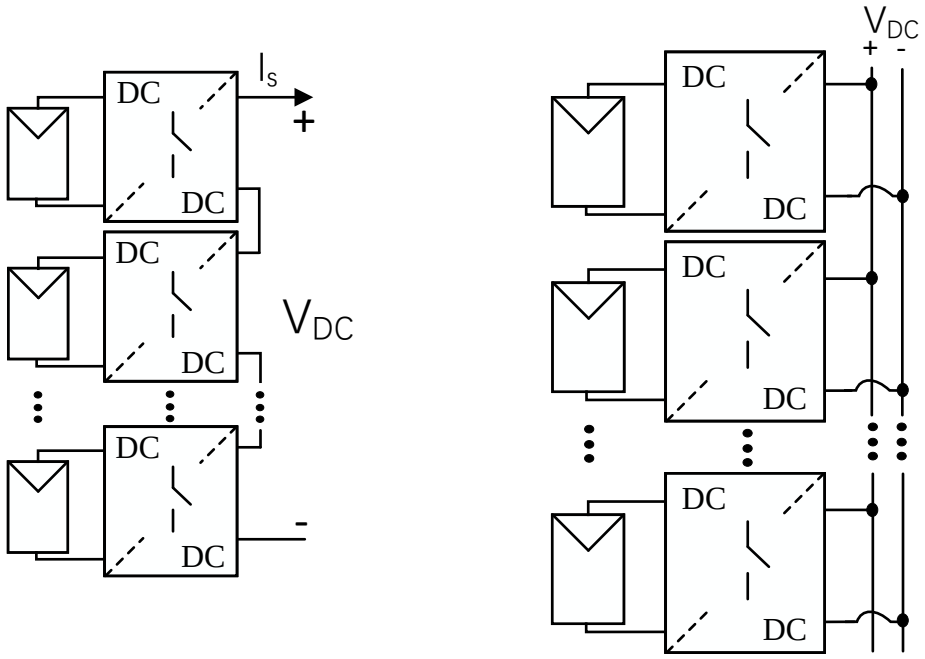
Figure 17: MMCI configurations

Table 1: Comparison between Micro inverters and MMCI

	Micro inverters	MMCI
Phase connection	single phase	single phase or three phase
EMI	High	Low
Voltage gain requirement	Required	Not Required
Flexibility	High	Low

DC-FPP

DC-FPP is similar to AC-FPP, except the output is in DC form. The power process is not as complex as AC-FPP because it is not the inverter that is connected but the converter. The DC-FPP can be divided into three branches: Series, Parallel, and TCT. In terms of the converter, it can be grouped into isolated and non-isolated. For isolated converters, flyback and forward are the typical options, while boost and buck-boost converters are common choices for non-isolated DC-FPP parts. Figure 18a, Figure 18b and Figure 19 show series, parallel and TCT layout in DC-FPP respectively.



(a) DC-FPP series layout **(b)** DC-FPP parallel layout

Figure 18: Series and Parallel DC FPP Configuration

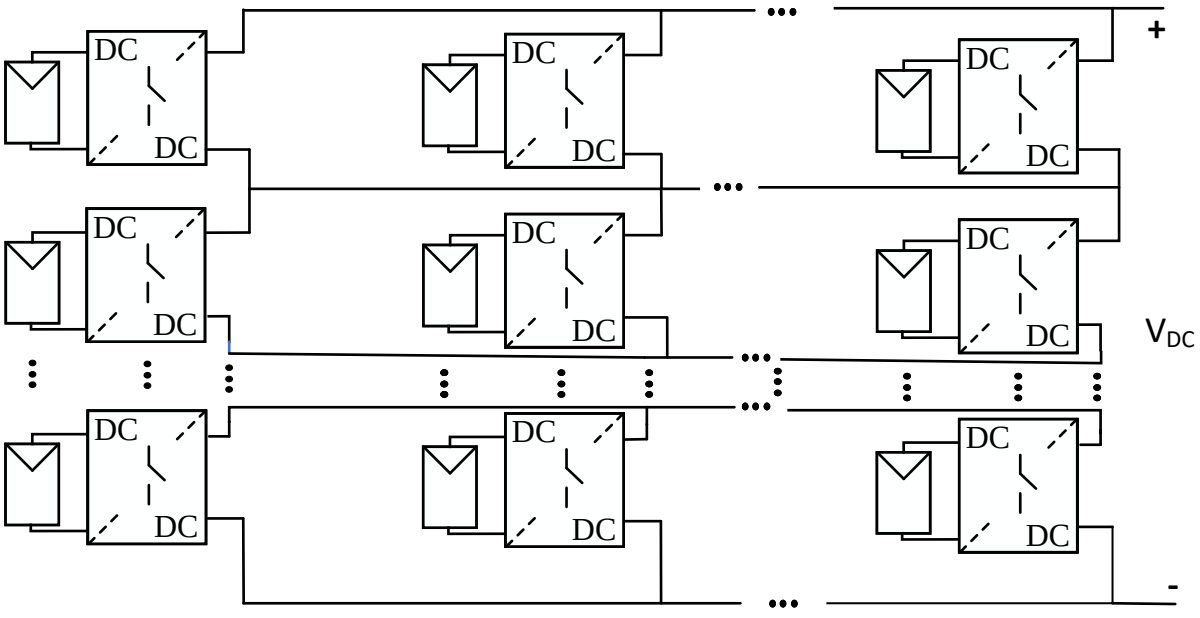


Figure 19: TCT DC-FPP layout

(i) **Series DC-FPP**

In the Series DC-FPP configuration, the lowest current PV module determines the string current (I_s). To maximize the string current, the converter compensates current from the unshaded PV module to the shaded PV module. In Figure 18a, each converter tracks the MPP of a single PV module, and the value of V_{DC} depends on the actual conversion ratio of the converters and can be different from the sum of the MPP voltages of the modules. V_{DC} represents a central converter voltage that sums all the PV module voltage and forms a DC bus. Thus, the central converter required less voltage step-up when connected to the grid. Moreover, suppose the string has enough PV modules due to the high voltage generated in V_{DC}. In that case, V_{DC} voltage is higher than the grid voltage connection requirement; the central converter no longer requires voltage set up instead of voltage step down. Therefore, the central converter can apply

buck and buck-boost converters to step down the voltage for the grid requirement. While few solar panels connected in series boost and buck-boost converters are an option[31].

(ii) **Parallel DC-FPP**
The Parallel DC-FPP configuration is similar to Micro inverters in AC-FPP, and parallel DC-FPP shares the same characteristics. For example, lower installation costs, high flexibility, modularity, scalability, and reliability. On the other hand, both configurations struggle with high voltage gain. The main difference is that the power form of the Parallel DC-FPP is the DC form, resulting in the component's cost being cheaper than Mirco inverters[32].

(iii) **TCT DC-FPP**
The TCT configuration is a hybrid structure of series and parallel connections. The TCT configuration is created to diminish the downside of series or parallel configuration. For instance, in a parallel connection, high voltage gain is required. A cross-couple effect may affect the PV module for a series connection, resulting in the maximum power that can not be delivered[33]. Hence, the TCT configuration inherits both series and parallel features. Nevertheless, The main challenge for TCT design is that the cable connection between series and parallel is complex and challenging to scale[34].

2.3.2 DPP

In the FPP power conversion, no matter whether the PV modules experience unbalanced irradiance, the power generated by the PV modules must pass through the FPP converter because there is no direct connection to the grid. In other words, despite no irradiance mismatch in the PV string, the PV string power delivered to the grid must pass through the FPP converter. Therefore, the PV string experienced losses from FPP converter conversion. In addition, the power rating of the FPP converter must be greater or equal to the maximum power of the PV module. A DPP configuration has been proposed to eliminate unnecessary losses when there is no irradiance mismatch; when there are no irradiance mismatches, DPP will not take intervention on the PV string[31]. Moreover, the DPP's power rating is only a fraction of the maximum power of the PV module. DPP categories have three main architectures: SP-DPP, S-DDP, and P-DPP (shown in Figure 20). In series DPP (S-DDP), the converter compensates for current mismatch between PV modules. On the other hand, between parallel DPP (P-DDP), the converter compensates for the mismatched voltage between PV string and DC bus to deliver maximum power to the output. Series and Parallel DPP (SP-DPP) combines S-DPP and P-DPP to eliminate mismatches among PV groups connected in series or parallel[19].

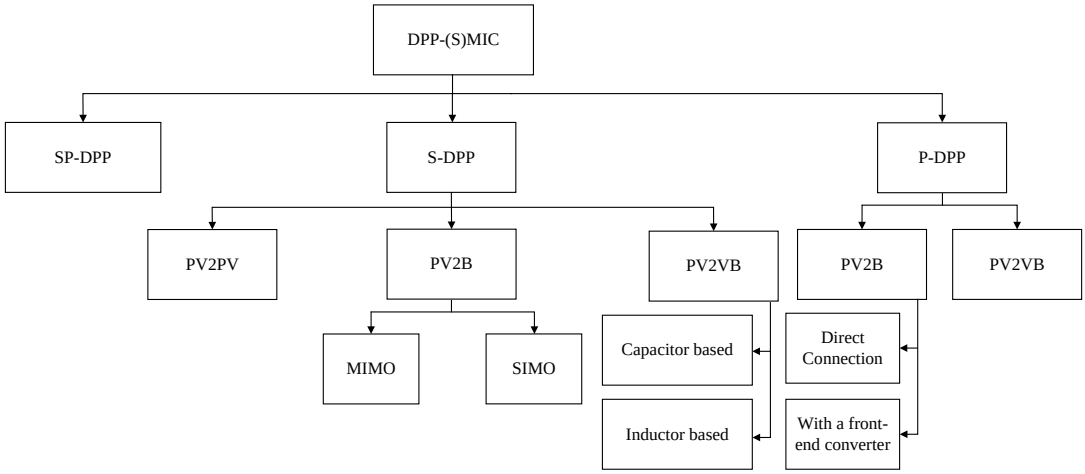


Figure 20: DPP-DMPPT classification [19]

S-DPP
S-DPP can be divided into three types of structure, PV2PV, PV2B, and PV2VB. Classification criteria are based on the converter output connection.

PV2PV
In the PV2PV configuration, the converter output is connected to the adjacent PV module as shown in Figure 21. The Module integrated converters (MICs) are located between two adjacent PV modules. To compensate for the current

mismatch in PV modules, the MICs require bidirectionality due to the converter enabling either withdrawing current from unshaded PV modules or delivering current to the shaded PV modules so that all the PV modules can work on their MPP. In the PV2PV structure, N number of PV modules required N-1 number of MIC. Figure 21 presents N PV modules and N-1 MIC in PV2PV configuration.

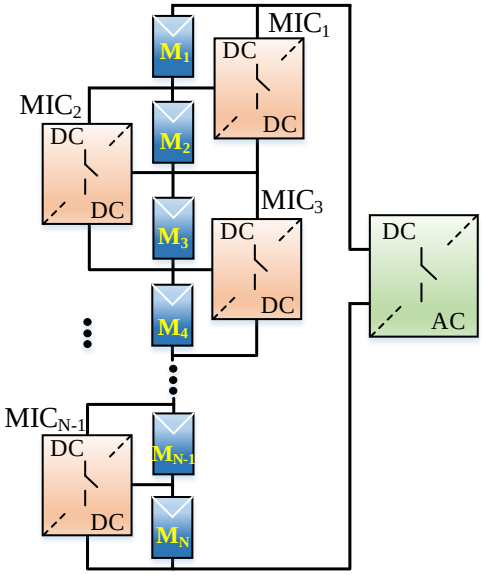


Figure 21: PV2PV configuration [19]

Using PV2PV structure has two benefits: first, the voltage rating of MIC's components is determined by the voltage characteristics of the PV modules. Second, the type of converter can select either a non-isolated or isolated converter, which leads to more options for the non-isolated converter, which provides higher efficiency and a simpler design with fewer components, leading to lower costs and reduced complexity. On the other hand, there are two drawbacks to the PV2PV structure. The cross-coupling effect exists in the PV2PV configuration, which means when some of the PV modules are shaded while PV modules are exposed to sunlight, the shaded PV modules can act as loads on the unshaded PV modules. This can lead to imbalances in current flow and voltage levels, reducing the overall power output of the system[35]. Another downside is the accumulation effect; in PV2PV configuration, the converter function compensates the current from the unshaded PV module to the shaded PV module; On the unshaded side, the power sum will be transferred to the shaded side, and the converter requires a high power rating to withstand the accumulation power[36].

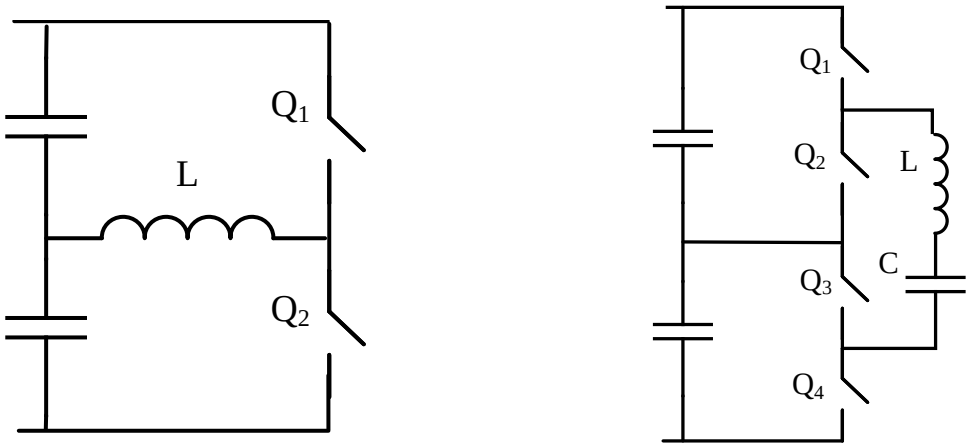
Suppose in a PV string, one-half of the PV string is shaded, and the other half is not shaded. The highest converter power rating required is located in the middle between the shaded module and unshaded module[36].

$$P_{C_{max}} = \frac{N}{4} P_{mpp} \times (1 - k) \tag{1}$$

In Equation 1, the converter maximum power rating depends on three factors: N (number of PV modules), k (shading factor), and P_{MPP} (PV module maximum power point). All three factors are in positive proportion. Usually, the converter power rating is smaller than the PV module's maximum power rating. In the PV string, the number of PV modules and power rating is fixed, and the only variable is the shading factor, Equation 2 demonstrates that when the shading factor exceeds the threshold, the PV system will not lose power.

$$k \geq 1 - \frac{4 \times r_p}{N} \tag{2}$$

Where the r_p is the ratio between the maximum power rating converter and PV module rating. There are two main types of converters in DPP PV2PV: Switched-Inductor and Switched-capacitor. Figure 22a and Figure 22b shows switched-inductor and switched-capacitor circuit respectively.



(a) Switched-inductor **(b)** fig:Switched-capacitor

Figure 22: PV2PV type of switches[19]

Regarding Figure 23, the process for obtaining the PV string current is as follows: assume the V_{mpp} is fixed when changing the irradiance and each PV module is identical. First, the string current (I_{tot}) is obtained by averaging the sum of the PV module current as shown in Equation 3; since the V_{mpp} is fixed, P_{mpp_i} is proportional to the current of PV modules, the string current can also be expressed as Equation 4. Then apply Equation 5 and compute the first converter process current ($I_{c,1}$) by using the string current minus the first PV module current ($I_{s,1}$). In Equation 6, apply KCL to determine the node between the first and second PV modules to determine the current to inject or extract into the second converter. Looping through each node (the node is defined on Figure 23 solid dot point). In Equation 7) can calculate each converter's current injection or withdrawal.

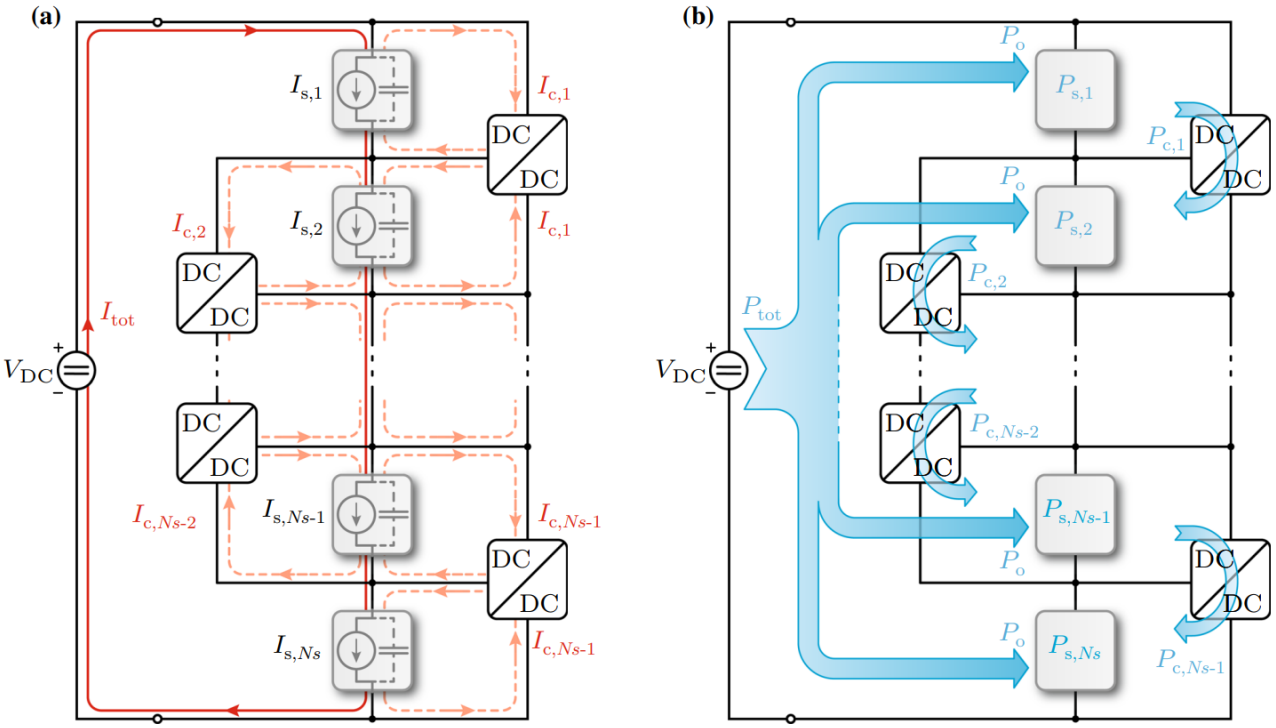


Figure 23: Detailed steady-state analysis of **a** the current flow and **b** the power flow in the generalized current diverter system balancing a string of cells. In (**a**), the cells are modeled as current sources $I_{s,i}$. The current I_{tot} from the DC-link flows through all current sources, while the difference between I_{tot} and the currents of the individual sources is compensated by the diverter modules with currents $I_{c,i}$. Since the voltages of all cells are equalized, the power flow analysis of **b** can be based on the derived currents, which shows that finally, each cell receives the power P_0 from the DC-link (or delivers it to the DC-link depending on the sign of P_0). Accordingly, the current diverters are compensating the mismatch between the individual cell power levels $P_{s,i}$ and P_0 [36]

$$I_{tot} = \frac{\sum_1^{N_s} P_{mpp_i}}{\sum_1^{N_s} V_{mpp_i}} \tag{3}$$

$$I_{tot} = \frac{\sum_1^{N_s} I_{mpp_i}}{N_s} \tag{4}$$

$$i_{c,1} = i_{tot} - i_{s,1} \tag{5}$$

$$I_{s,2} + I_{c,2} = I_{s,1} + 2 \times I_{c,1} \tag{6}$$

$$I_{s,Ns} + I_{c,Ns-1} = I_{s,N-1} + 2 \times I_{c,N-2} \tag{7}$$

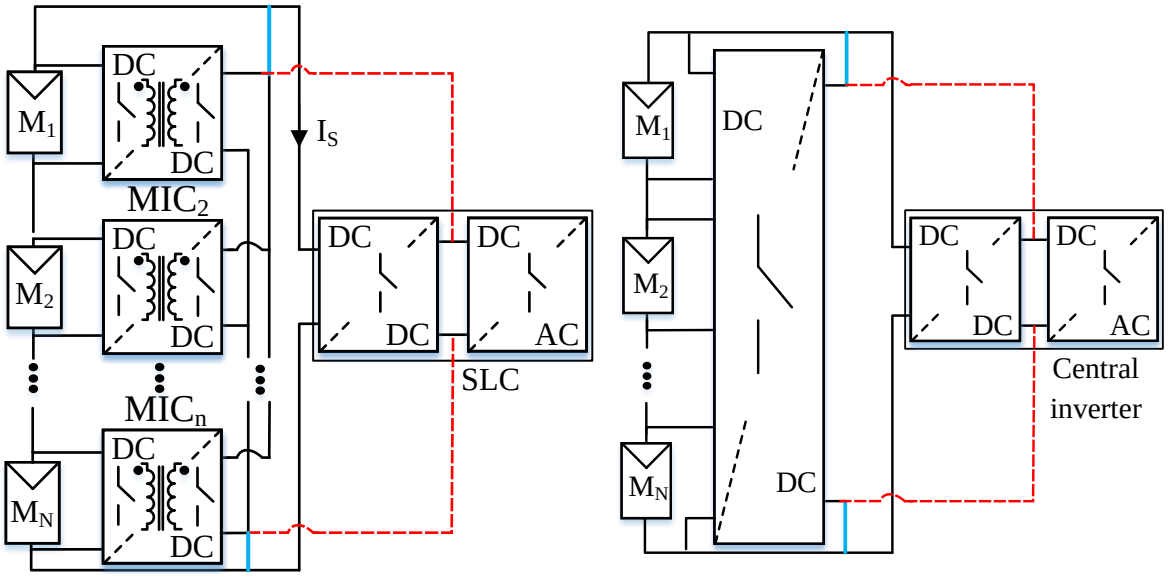
PV2B

In PV2B configurations, the converter output is connected to the DC bus. When the string contains N number of PV modules, the system requires N number of converters and a central inverter. Compared with the PV2PV structure, the main advantage is no accumulation effect[19]. In other words, the maximum power capacity requirements of the converter do not continue to increase as the string is expanded. Another advantage is that the current from the converter to the bus is low, leading to low-power processing because only part of the PV modules' current is processed on the converter[37].

On the other hand, PV2B has several disadvantages such as the isolation converter usually requires a high voltage setup, and the efficiency of the isolation converter is relatively low compared to the non-isolated converter[38]. Moreover, despite eliminating the accumulation effect, the cross-couple effect still exists. Consider the worst-case; the maximum power required for the converter is shown in Equation 8.

$$P_C = \frac{N_M - 1}{N_M} \times P_{MPP} \tag{8}$$

Where P_C, P_{MPP}, and N_M are converter power ratings, PV module maximum power, and the number of PV modules, respectively. PV2B topology can be divided into two branches: multiple-input–multi-output(MIMO) and multi-input–single-output (MISO). Figure 24a and Figure 24b displays the configuration of MIMO and MISO respectively.



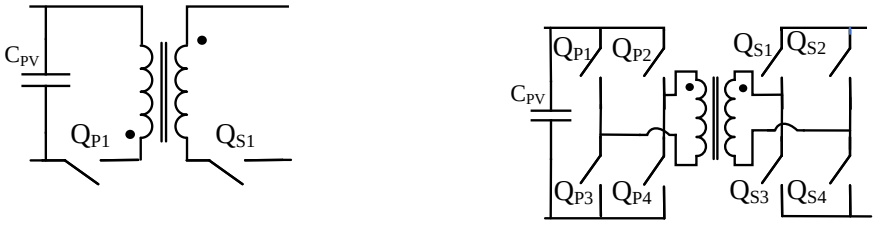
(a) MIMO **(b)** :MISO

Figure 24: PV2B configuration[19]

In the MIMO structure, the converter must be isolated to avoid the short circuit in the PV module. Typically, flyback and dual active bridge (DAB) converters can achieve isolation; the configuration is presented in Figure 25a and Figure 25b. The flyback converter is a relatively simple circuitry and control compared to DAB. In contrast, the DAB

converter offers higher efficiency but comes with increased complexity and is more expensive to implement.

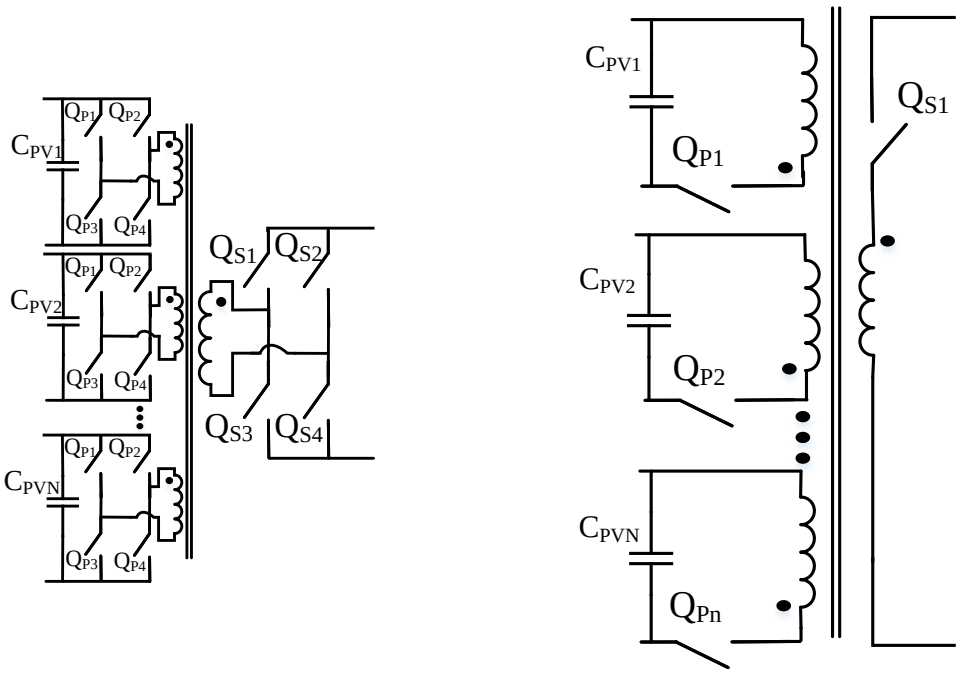
In MIMO, there are two different types of controls. The first type of control is for the DPP converters; the objective is to seek each PV module MPP and deliver power to the central converter. The second type of control is to optimize the string current. One of the common methods to optimize the string current is called least power point tracking (LPPT) [39]. For the least power point tracking method, after each PV module located its own MPP, the central controller decide how much current flow into the central inverter. The goal of the second type of controller is to maximize the current amplitude for the PV string as much as possible because a higher current means higher power delivery. On the other hand, because the power entering the converter will generate conversion losses, the converter should process the least current to achieve the highest current of the string[40].



(a) Flyback **(b)** Dual active bridge

Figure 25: MIMO type of converter[19]

The MISO configuration is similar to MIMO, but in the MISO configuration, there are fewer switches if both configurations have the same number of PV modules. Figure 26a and Figure 26b show the Multi-winding transformer active full-bridge and Multi-winding transformer flyback configuration, respectively. In the MIMO configuration, one MIC corresponds to one PV module. but in MISO configuration, it combines power generated by multiple PV modules into a single output, which is then injected into the bus via a shared inverter. There are fewer switches on the DC bus side; however, the switches on the DC bus side need to withstand higher voltage.



(a) Multi-winding transformer active full-bridge **(b)** Multi-winding transformer flyback

Figure 26: MISO MIC[19]

PV2VB

In the PV2VB structure, the converter output is connected to a virtual bus. Usually, the virtual bus is either made

by a capacitor or an inductor. In terms of the number of converters attached to the PV module, Pv2VB has a similar configuration to PV2B; both have N number of converters when N number of PV modules is applied. The main difference between PV2VB and PV2B is the converter output connection. In PV2B, the converter output is connected to the central inverter, while in the PV2VB configuration, the converter output is connected to the passive electronic component that stores electrical energy; typically, the passive elements are inductors and capacitors. The converter function is the same as other configurations. If the PV modules are shaded and generate less current, the converter injects current into the PV module. On the contrary, if the PV module is unshaded and generates a higher current, the converter withdraws the current from the virtual bus. The virtual bus is composed of a capacitor or inductor. Therefore, the average power of the virtual bus must be equal to 0. In other words, the average current of the virtual bus capacitor or the average voltage of the virtual bus inductor is equal to zero [**Skvarenina200**].

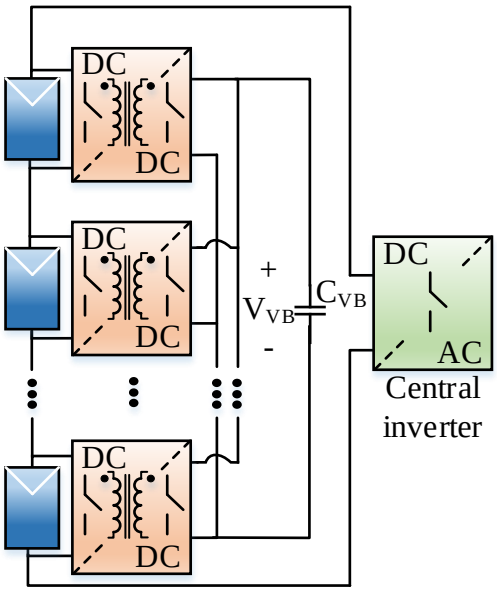


Figure 27: S-DPP PV2VB configuration [19]

Generally, converters used in a PV2VB S-DPP architecture must have two main features: to prevent a short circuit between two adjacent PV modules, such as the PV2B configuration, and to compensate for shading on a PV module, the converter must support bidirectional current flow.

The differences in charging and discharging rates between capacitors and inductors are primarily due to the nature of energy storage (electric field for capacitors, magnetic field for inductors). Current flows through an inductor, creating a magnetic field. However, due to the properties of the inductor, changes in current cause a reverse electromotive force (EMF), opposite to the change in current. This results in a slower rate of charging and discharge. Therefore in this project, the passive element in the virtual bus only considers the capacitor.

Designing virtual bus capacitors for PV2VB configuration requires careful consideration. Here are some of the critical factors designers should consider:

(i) Voltage rating: The voltage rating of the capacitor should be selected to handle the maximum expected voltage in the system, taking into account any voltage spikes, transients, and safety margins.

(ii) Capacitance value: The capacitance value determines the amount of energy the capacitor can store and release. It is important to select an appropriate capacitance value to meet the energy storage requirements of the application. Too low a capacitance value can lead to voltage ripple and instability, while too high a capacitance value can increase physical size and cost.

(iii) Ripple Current Ratings: Power electronics applications involve continuous charging and discharging cycles of capacitors. The ripple current rating specifies the maximum current ripple that a capacitor can withstand without overheating or degrading performance over time. Selecting a capacitor with an adequate ripple current rating ensures

reliable, long-lasting performance.

In Table 2 shows the comparison among PV2PV, PV2B, and PV2VB. Moreover, actuators enable the precise control and manipulation of electrical power, helping to regulate parameters like voltage, current, and power flow.

Table 2: Comparison among PV2PV, PV2B and PV2VB

	PV2PV	PV2B	PV2VB
Actuator	N-1	N	N+1
Number of converters	N-1	N	N
Accumulation effect	Yes	No	No
Isolated MIC	Not required	Required	Required
Scalability	High	Low	Low
Cross-couple effect	Yes	Yes	Yes

P-DPP

In S-DPP, the DPP converters compensate for the current difference between PV modules and maximize the string current based on the KCL. On the other hand, in the P-DPP configuration, the converter compensates for the voltage difference between the PV modules or PV strings. In PV characterization, shading has a more significant impact on current than on voltage. Figure 28 shows the IV curve of PV module at different irradiance; the dashed line represents V_{mpp} and I_{mpp} at different irradiance levels. When the irradiance decreases, the V_{mpp} is slightly decreased, whereas I_{mpp} has dramatically dropped; the I_{sc} decrease rate is proportional to the irradiance change. Therefore, the I_{mpp} is more sensitive to irradiance change. Under severe mismatched irradiance conditions, the PV strings connected in parallel experience voltage magnitude mismatches that are relatively tiny compared with the current mismatches in PV modules connected in series. Therefore, the P-DPP power rating required for converters is lower than S-DPP. However, there is little research on P-DPP. There are two different types of P-DPP configurations: PV2B and PV2VB.

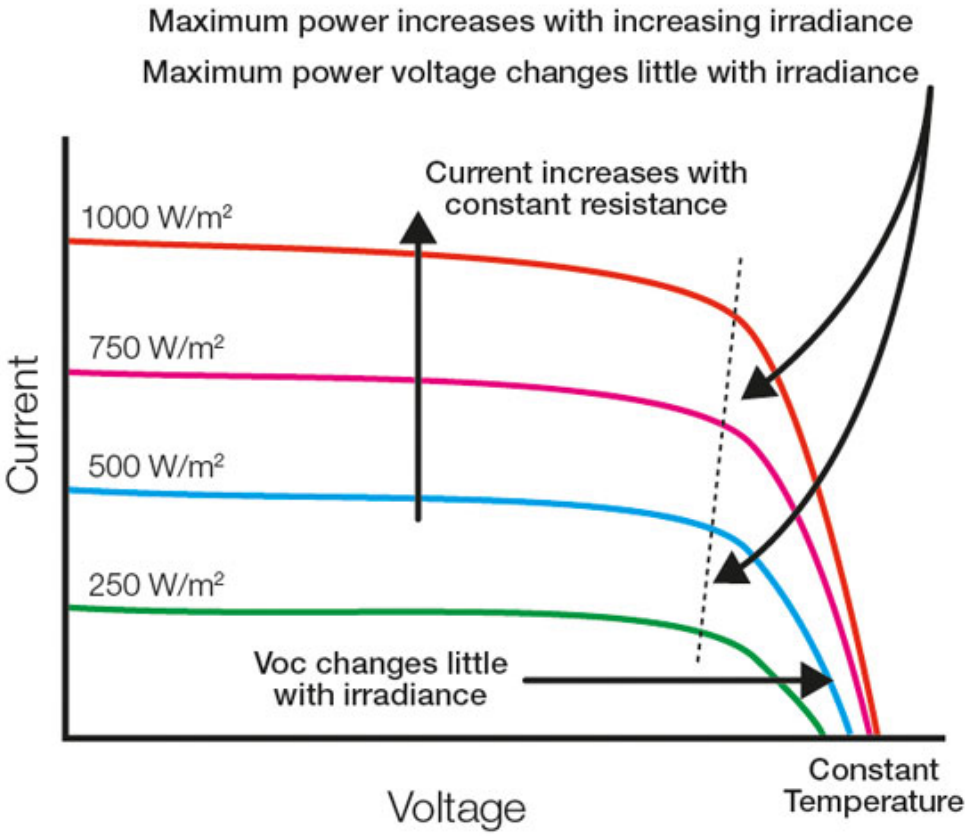


Figure 28: A generic I-V curve With different irradiance [41]

PV2B

In P-DPP PV2B, according to the definition, the converter's output is connected to a bus. Figure 29 displays the configuration for PV2B P-DPP. Similar to the S-DPP PV2B configuration, the type of converter needs to be isolated.

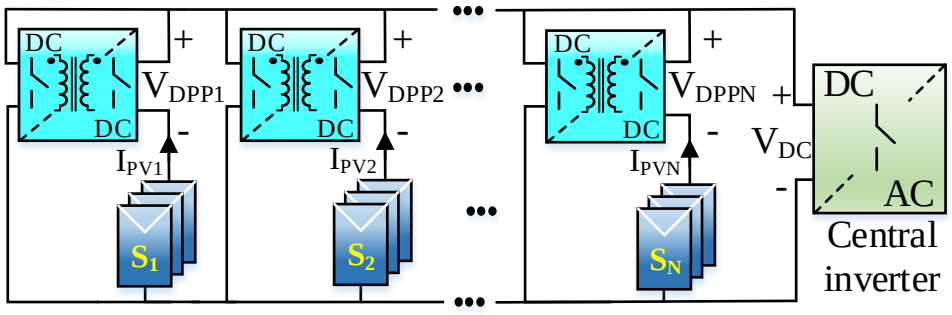


Figure 29: PV2B DPP configuration, S_i indicates the i^{th} PV siring and I_{PV_i} indicates the current of i^{th} PV string that generates, and V_{DC} indicates the voltage of central inverter in a PV system[19]

In each PV string, the DPP converters track the PV string's local MPP, then the central inverter optimizes the power obtained from each string. The central inverter reduces energy losses through fine-tuning. Notably, based on the previous research, in PV2B P-DPP configuration, DPP converters can only generate positive voltage because the typical selection for a DPP converter is a flyback converter no matter how the duty cycle changes from the range of 0-1, the output voltage remind positive [39]. This scenario leads to one significant constraint: the DC bus voltage must always exceed the maximum voltage in the PV string. Ideally, the DC bus voltage should match the highest achievable MPP string voltage. This setting leads to some DPP converters working at an extremely low duty ratio[39]. One of the solutions is to set a higher voltage at the bus. However, it requires high-voltage switches on the primary side of the central inverter resulting in high cost and higher voltage stress. In addition, the DPP converter power process is higher, which leads to more conversion losses occurring in the DPP converter.

PV2VB

Figure 30 shows the PV2VB P-DPP configuration. Note that S_i indicates the i^{th} PV siring and I_{PV_i} indicates the current of i^{th} PV string that generates,V_{PV_i} indicates the voltage of i^{th} PV string that generates, V_{DPPi} indicates the i^{th} PV string voltage injects to the correspond DPP or withdraws from the correspond DPP,V_{VB} indicates the voltage of virtual bus in a PV system, and V_{DC} indicates the voltage of central inverter in a PV system. On the other hand, PV2VB offers advantages that PV2B does not. Firstly, the string converter no longer needs to withstand high voltage due to the converter output having no direct connection to the central inverter. Thus, the converter is not required to boost the voltage up to the central converter voltage level, resulting in less power processed by the DPP converter. In addition, it is possible to reduce the rated voltage of the virtual bus voltage (V_{VB} below the DC bus voltage. Lastly, the DPP converter switches design can enable designers to use MOSFETs instead of IGBTs. MOSFETs operate at higher frequencies than IGBTs, reducing the size and cost of passive components. The next chapter will discuss the Dynamic modeling of P-DPP PV2VB.

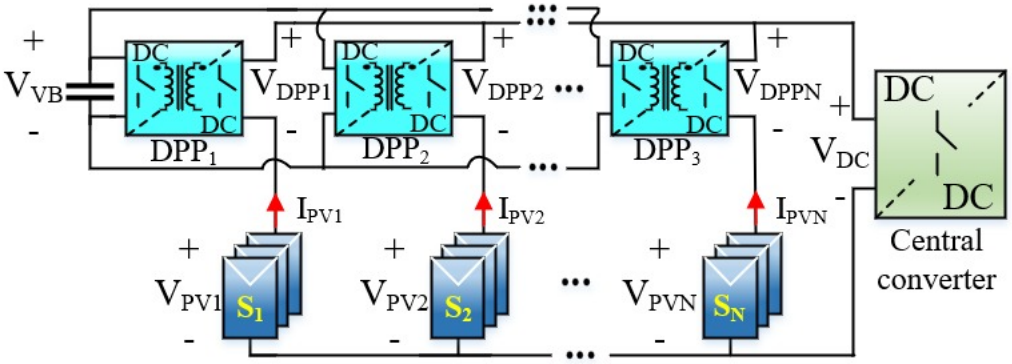


Figure 30: P-DPP PV2VB configuration [19]

3 Dynamic Model of PV2VB P-DPP Architecture

In [6], a PV2VB architecture is introduced (mention in Figure 2.3.2). The paper concerns the nominal operation condition in which the architecture is designed to perform in a steady state. In other words, the paper focused on situations in which its behavior is the same from cycle to cycle. However, Dealing with the consequences of unavoidable disturbances or errors that cause circuits to operate outside of their ratings is critical to maintaining the reliability, stability, and performance of electronic systems. These disturbances include variations and uncertainties in source, load, and circuit parameters, perturbations in switching times, and events such as startup and shutdown. The resulting evolution of the deviations from nominal behavior is called the dynamic behavior of the circuit.

Usually, properly designed controllers or compensators counteract the deviation from nominal conditions. controllers or compensators are crucial for ensuring that a system operates at its desired nominal conditions, and they must do so quickly and automatically to regulate the system effectively. This regulation is made by delaying, advancing, increasing, or decreasing the times when switches are turned on and off. Therefore, in this chapter, we begin to build the basis for analyzing the dynamic behavior of PV2VB P-DPP architecture; the next chapter focuses on analysis and control design using the dynamic model obtained in this chapter. This approach has many advantages, such as: (I) Anticipating the behavior of the circuit under diverse operating conditions, (II) generating candidate controller structures and parameters, (III) planning simulation studies, (IV) understanding experimental results, (V) recognizing which regimes of operation call for further investigation.

In subsection 3.1, first, we explain what a dynamic model is and why linearization plays an essential role in the study of dynamic behavior. In subsection 3.2,subsection 3.3 and subsection 3.4 PV string, central converter, and P-DPP modeling are provided in detail, respectively. After modeling each part of the system, in subsection 3.5 the steady state analysis for PV2VB P-DPP was constructed. The visualization PV2VB P-DPP model for large and small signals is displayed in subsection 3.7. Lastly, subsection 3.8 shows the state space equation for PV2VB P-DPP architecture.

3.1 Dynamic Model with Circuit Averaging and Linearization

3.1.1 Dynamic Model

As shown in Figure 30, a PV2VB P-DPP architecture consists of N PV strings, N P-DPP converters, and a central converter. Appropriate models for each part are central to analyzing the dynamic model of the architecture and designing the control. Like most power electronic converters, a PV2VB P-DPP architecture has Linear time-invariant (LTI) components, and to simplify the model, switches are ideal in other words, . Analyzing such a circuit in each switch configuration (or topological state) is as simple as analyzing an LTI circuit. The problem arises in piecing together the solutions from successive configurations. Here, the dynamic behavior of P-DPP converters is being analyzed through both circuit-level and state-space averaging techniques., which allows us to stay close to the circuit techniques that electrical engineers use so well.

3.1.2 Linearization

Since State-space equations of the whole architecture contain nonlinear terms, nonlinear dynamic models can be complex and challenging to analyze. Linearization simplifies these models by approximating them as linear around a specific operating point. Linear models are often easier to work with mathematically, making analysis and calculations more manageable. Linearization makes assessing stability and designing or evaluating controllers much more straightforward. Moreover, it allows us to obtain linear models that approximately govern slight deviations from the nominal solution. The linearized model called the small-signal model, is far more tractable than nonlinear models. Notably, the instability of the linearized model implies that the nominal operating condition cannot be maintained without further control action. Still, the stability of the linearized model does not, of course, tell us about recovery from significant disturbances.
In Equation 9 shows the typical state space mathematical model.

$$\begin{aligned} \frac{\partial x}{\partial t} &= f(x(t), u(t)) \\ y(t) &= g(x(t), u(t)) \end{aligned} \tag{9}$$

where: x is the state vector, u is the input vector, y is the output vector, y represents the vector of nonlinear differential equations that describe the system dynamics, and g represents the vector of output equations that define the relationship between the state and the output.

To linearize the dynamics equation, first, expand the terms x, y, and u in the DC signal and small AC signal. Equation 10 shows the term expansion.

$$\begin{aligned} x(t) &= \tilde{\boldsymbol{x}}(t) + X \\ u(t) &= \tilde{\boldsymbol{u}}(t) + U \\ y(t) &= \tilde{\boldsymbol{y}}(t) + Y \end{aligned} \tag{10}$$

Where X represents the DC signal and $\tilde{\boldsymbol{x}}$(t) represents the small AC signal and is similar to the terms u and y. Note that the magnitude of the DC signal is much greater than the AC signal.

$$\begin{aligned} \left|\tilde{\boldsymbol{x}}(t)\right| &<< |X| \\ \left|\tilde{\boldsymbol{u}}(t)\right| &<< |U| \\ \left|\tilde{\boldsymbol{y}}(t)\right| &<< |Y| \end{aligned} \tag{11}$$

Substituting Equation 9 back to Equation 9, the expansion is shown in Equation 12.

$$\begin{aligned} \frac{dX}{dt} + \frac{d\tilde{x}}{dt} &= f(X(t), U(t)) + \frac{\partial f}{\partial x}\tilde{x}(t) + \frac{\partial f}{\partial u}\tilde{u}(t) \\ Y(t) + \tilde{y}(t) &= g(X(t), U(t)) + \frac{\partial g}{\partial x}\tilde{x}(t) + \frac{\partial g}{\partial u}\tilde{u}(t) \end{aligned} \tag{12}$$

By eliminating the DC term, the linearized state space equation is expressed in Equation 13 :

$$\begin{aligned} \frac{\partial \tilde{\boldsymbol{x}}(t)}{\partial t} &= \frac{\partial f}{\partial x}\tilde{\boldsymbol{x}}(t) + \frac{\partial f}{\partial u}\tilde{\boldsymbol{u}}(t) \\ \tilde{y}(t) &= \frac{\partial g}{\partial x}\tilde{x}(t) + \frac{\partial f}{\partial g}\tilde{u}(t) \end{aligned} \tag{13}$$

3.2 PV Modelling

One of the methods for modeling PV is to apply the equivalent circuit for the PV module shown in Figure 31, a PV equivalent contain 4 main elements: I_{ph}, D, R_{sh} ,and R_s. I_{ph} represented as a current source, which represents the generated current when under illumination. This current value is proportional to the solar irradiance. D represents a diode; it reflects the PV module's voltage-dependent properties. R_{sh} and R_s represents the series and shunt resistance respectively. Equation 14 shows the PV module current output with respect to the parameters in the equivalent PV module circuit.

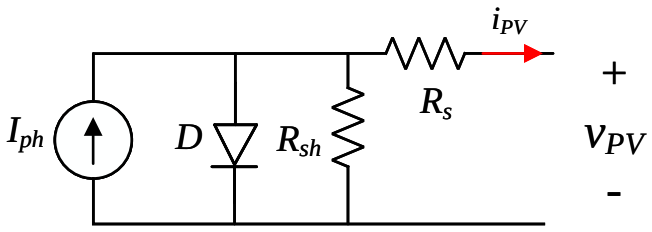


Figure 31: PV equivalent circuit

$$i_{PV} = I_{sc} - I_o\left(\exp\left(\frac{V_{PV} + I_{PV}R_s}{\eta \cdot N_s \cdot V_{th}}\right) - 1\right) - \frac{V_{PV} + I_{PV}R_s}{R_{sh}} \tag{14}$$

Where I_{sc} is short circuit current, I_o is the saturation current, N_s represents the number of cells connected in series, η is the ideality factor, and V_{th} is the thermal voltage. At STC (standard test condition) V_{th} is equal to 0.0259. When the temperature changes, the thermal voltage can be calculated in Equation 15, where k_B is Boltzmann constant q is elementary electric charge, and T is the PV module operation temperature.

$$V_{th} = \frac{k_B T}{q} \tag{15}$$

From the PV Manufacturer datasheet, I_{sc}, I_{mpp}, V_{mpp}, and V_{oc} can be found in the standard testing conditions, V_{PV} and I_{PV} can be measured by voltmeter and ammeter respectively. Refer to the Equation 14, the saturation current can be calculated in Equation 16, only the saturation current and two resistor R_{sh} and R_s values are unknown.
.

$$I_o = I_{sc} e^{-\frac{V_{oc}}{\eta N_s V_{th}}} \tag{16}$$

To find resistor R_s and R_{sh}, two scenarios for the PV module are applied: short circuit and open circuit.

$$\begin{aligned} 0 &= I_{ph} - I_o \left(\exp\left(\frac{V_{oc}}{\eta \cdot N_s \cdot V_{th}} \right) - 1 \right) - \frac{V_{oc}}{R_{sh}} \\ I_{sc} &= I_{ph} - I_o \left(\exp\left(\frac{I_{sc} R_s}{\eta \cdot N_s \cdot V_{th}} \right) - 1 \right) - \frac{I_{sc} R_s}{R_{sh}} \end{aligned} \tag{17}$$

Base on [42], apply the Lambert W-function, Rs can be calculated in Equation 18:

$$R_s = A\left(W_{-1}(B \exp(C)) - (D + C) \right) \tag{18}$$

where the coefficients of A to D are repressed below:

$$\begin{aligned} A &= \frac{\eta N_s V_T}{I_{mpp}} \\ B &= -\frac{V_{mpp}\left(2I_{mpp} - I_{sc}\right)}{\left(V_{mpp} I_{sc} + V_{oc}\left(I_{mpp} - I_{sc}\right)\right)} \\ C &= -\frac{2V_{mpp} - V_{oc}}{\eta N_s V_T} + \frac{\left(V_{mpp} I_{sc} - V_{oc} I_{mpp}\right)}{\left(V_{mpp} I_{sc} + V_{oc}\left(I_{mpp} - I_{sc}\right)\right)} \\ D &= \frac{V_{mpp} - V_{oc}}{\eta N_s V_T} \end{aligned} \tag{19}$$

After obtaining the R_s, substitute R_s back to Equation 17 to compute R_{sh}.

Diode Dynamic Resistance (R_d)
Dynamic resistance is diode dynamic resistance, which refers to the incremental change in voltage across a solar cell or PV module for a slight change in current through the diode under forward bias conditions. [43]. The diode dynamic resistance can be calculated in Equation 20[44].

$$R_d = \frac{\eta V_{th}}{I_o} \times e^{-\frac{V_{PV}}{\eta V_{th}}} \tag{20}$$

Combine series, shunt, and diode dynamic resistance into equivalent resistance; equivalent resistance refers to the single resistance value that represents the combined effect of all the resistive elements within the PV module, including the internal resistance of the PV cells, interconnects, and other components. This simplifies circuit analysis by allowing the PV module to be treated as only one equivalent resistor with this equivalent resistance. the equivalent resistance calculation is shown in Equation 21.

$$R_{eq} = \frac{R_d R_{sh}}{R_d + R_{sh}} + R_s \tag{21}$$

Since the converter tracks the PV module MPP, if the PV module operates at MPP, the dynamic resistance coincides with the static resistance, which is determined by the ratio of the MPP voltage (V_{mpp}) to the MPP current (I_{mpp}). The R_{eq} can approximative expressed as in Equation 22

$$R_{eq} = \frac{V_{mpp}}{I_{mpp}} \tag{22}$$

This approximation simplifies the calculation of dynamic resistance and is often used in theoretical and practical analyses of PV modules. However, it's important to note that this is an approximation, and the actual dynamic resistance can vary depending on factors like temperature, irradiance, and the specific characteristics of the PV module. R_{eq} can

represent a single PV module in the Dynamic analysis, Figure 32(a) represents the PV module large signal model, and Figure 32(b) represents PV module small signal model.
According to Figure 30, the string voltage is the sum of the PV module' voltage plus the converter voltage. The PV module voltage expression is shown in Equation 23 by rearranging the position.

$$V_{PV_i} = V_s - V_{DPP_i} \tag{23}$$

Therefore, based on the ohm law, the current of PV modules can be expressed in Equation 24. To linearize the large signal circuit of the PV module, first convert i_{PV} into the function of $f(V_{PV})$, differentiate respect to state variable v_s and v_{DPP_i}. Equation 25 and Equation 26 show the partial derivate respect to v_{DPP_i} and v_s.

$$i_{Pv} = f(V_{PV}) = -\frac{V_{PV}}{R_{eq}} = -\frac{v_s - v_{DPP_i}}{R_{eq}} \tag{24}$$

$$\frac{\partial f_{PV}}{\partial v_{DPP_i}} = \frac{1}{R_{eq}} \tag{25}$$

$$\frac{\partial f_{PV}}{\partial v_s} = -\frac{1}{R_{eq}} \tag{26}$$

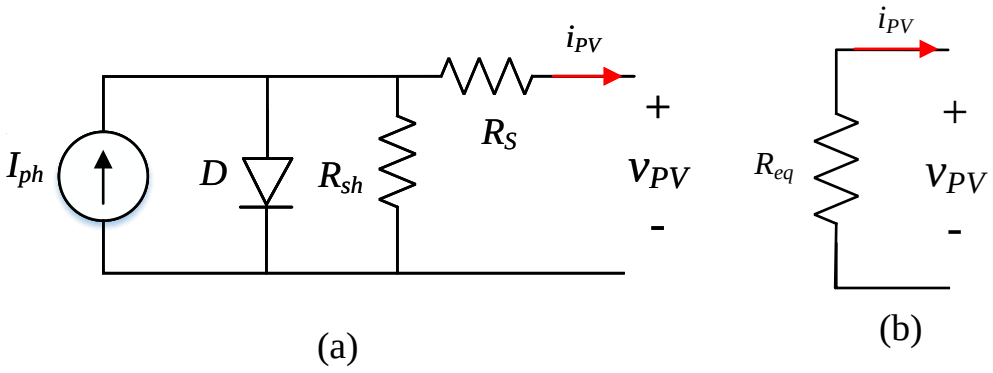


Figure 32: large signal model of PV module (a), (b) small signal model of PV module

To distinguish different string scenarios, R_i represents the equivalent resistance in $i^{th} PVstring$. Since the PV modules connect in series to form a PV string,

$$R_i = R_{eq(i)} = \frac{V_{mpp(i)} \times N_{modules(i)}}{I_{mpp(i)}} \tag{27}$$

3.3 Central converter modelling

Refer to Figure 30; the central converter represents the green block. For central converter modeling, one of the common options for a PV system to connect to a DC bus is a boost converter. There reasons to choose a boost converter as a central converter. The first reason is a boost converter is a DC-DC converter that can increase the voltage from input to output so that the output fulfills the bus voltage level requirement. The second reason is that a boost converter is easy to implement and cost-effective compared to an isolated converter. Figure 33 shows the boost converter schematic; the input (left-hand side of the diagram) is connected from all the PV strings in parallel, and the output (right-hand side of the diagram) is connected to a DC bus to deliver power. A boost converter's fundamental principle is storing energy in an inductor when the transistor is on and releasing energy to the output when the transistor is off. A capacitor in the boost converter is required to smooth the input voltage from the PV string (C_s).

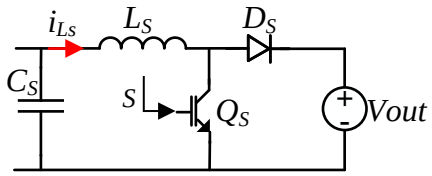


Figure 33: Boost converter schematic

Figure 34 shows a simplified circuit of a boost converter when the transistor is on, and Equation 29 and Equation 28 represent the voltage across the capacitor C_s and current through the inductor i_{Ls} respectively. and for the n^{th} represents how many PV strings are in the system, the current i_{PV_i} indicates i^{th} PV string current flow to the central converter input side. Based on KCL, the central converter input current is equal to the sum of each string current. When the transistor is on, the diode (D_s) is in reverse-biased mode, blocking the current toward the output. The input energy is transferred to the inductor and stored it.

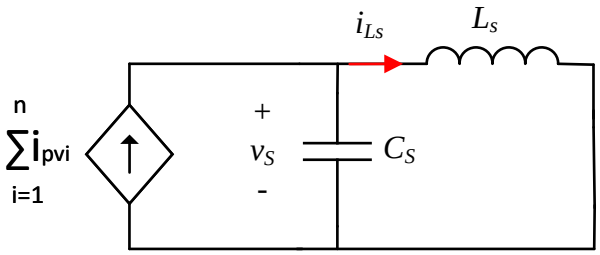


Figure 34: Boost converter transistor on

$$L_s \frac{\partial i_{Ls}}{\partial t} = v_s \tag{28}$$

$$C_s \frac{\partial v_s}{\partial t} = \sum_{i=1}^{n} i_{PV} - i_{Ls} \tag{29}$$

Figure 35 shows a simplified circuit when the transistor is off and Equation 31 and Equation 30 demonstrate the voltage across the capacitor C_s and current through the inductor i_{Ls} respectively. When the transistor is off, the diode is in forward-biased mode, and the energy stored in the inductor is released to the output.

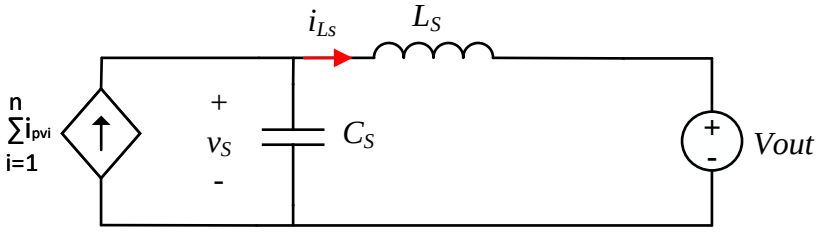


Figure 35: Boost converter transistor off

$$L_s \frac{\partial i_{Ls}}{\partial t} = v_s - V_{out} \times (1 - d_s) \tag{30}$$

$$C_s \frac{\partial v_s}{\partial t} = \sum_{i=1}^{n} i_{PV} - i_{Ls} \tag{31}$$

Combine the ON and OFF stages into a single period. Equation 29, Equation 28,Equation 30 and Equation 31 simplify to Equation 33 for voltage across capacitor and Equation 32 for current across inductor in transient stage. Where d_s

stands for the ratio of the on-time of the switch to the total switching period , also known as duty cycle.

$$\frac{\partial i_{Ls}(t)}{\partial t} = \frac{v_s(t) - V_{out}(t) \times (1 - d_s)}{L_s} = g_1(v_s, d_s) \tag{32}$$

$$\frac{\partial v_s(t)}{\partial t} = \frac{-i_{Ls} + \sum_{i=1}^{n} f_{PVi}(v_s - v_{DPP_i})}{C_s} = g_2(i_{L_s}, v_s, v_{DPP_i}) \tag{33}$$

Based on Equation 32 and Equation 33, The large-signal average model of the central converter is shown in Figure 36

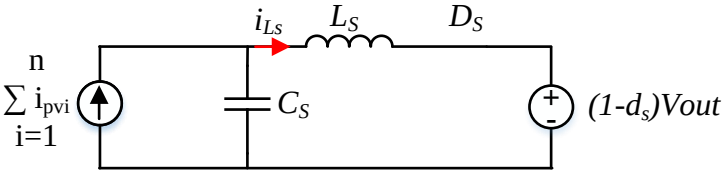


Figure 36: large-signal average model of the central converter

To find the model of a small signal with respect to the boost converter, apply the partial derivative method into Equation 33 and Equation 32. Consider V_{out} as constant. This assumption is based on the converter output connected to the DC grid. In a DC grid, the voltage remains relatively constant from the power source to the load; the dynamic behavior is relatively slow. Hence, the dynamic behavior of the DC grid can be neglected; therefore, the V_{out} considered constant voltage sources. So the state variable are included: v_s, i_{Ls}, and n v_{DPP_i}, for the input variable is d_s.

In Equation 33, there are 2+n variables: i_{Ls}, v_s and n v_{DPP_i}. Linearize to obtain a small signal model concerning the voltage across capacitance and current across the inductor, the deviation is shown in Equation 35 and Equation 34:

$$\frac{\partial \tilde{\boldsymbol{i_{L_s}}}(t)}{\partial t} = \frac{\partial g_1}{\partial v_s} \tilde{\boldsymbol{v_s}}(t) + \frac{\partial g_1}{\partial d_s} \tilde{\boldsymbol{d_s}}(t) \tag{34}$$

$$\frac{\partial \tilde{\boldsymbol{v_s}}(t)}{\partial t} = \frac{\partial g_2}{\partial i_{Ls}} \tilde{\boldsymbol{i_{Ls}}}(t) + \frac{\partial g_2}{\partial v_s} \tilde{\boldsymbol{v_s}}(t) + \sum_{i=1}^{n} \frac{\partial g_{2_i}}{\partial v_{DPP_i}} \tilde{\boldsymbol{v_{DPP_i}}}(t) \tag{35}$$

Substitute Equation 32, partial derivative of i_{Ls} is shown below
g1 denotes the small signal group on the inductor (L_s):

$$\frac{\partial g_1(t)}{\partial v_s} = \frac{1}{L_s} \tilde{\boldsymbol{v_s}}(t) \tag{36}$$

$$\frac{\partial g_1(t)}{\partial d_s} = \frac{V_{out}}{L_s} \tilde{\boldsymbol{d_s}}(t) \tag{37}$$

Substitute Equation 33, partial derivative of V_s is shown below
g1 denotes the small signal group on the capacitor (C_s):

$$\frac{\partial g_2(t)}{\partial i_{Ls}} = \frac{-1}{C_s} \tilde{\boldsymbol{i_{Ls}}}(t) \tag{38}$$

$$\frac{\partial g_2(t)}{\partial v_s} = -\frac{1}{C_s \sum_{i=1}^{n} R_i} \tilde{\boldsymbol{v_s}}(t) \tag{39}$$

$$\frac{\partial g_{2_i}(t)}{\partial v_{DPP_i}} = \frac{1}{C_s \sum_{i=1}^{n} R_i} \tilde{\boldsymbol{v_{DPP_i}}}(t) \tag{40}$$

After completing the partial derivative concerning i_{Ls} and v_s, Figure 37 shows the small signal diagram of the central converter.

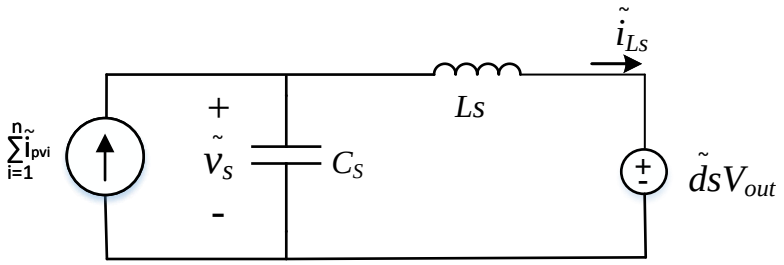


Figure 37: Small signal model of central converter

3.4 P-DPP Modelling

The P-DPP converter can be split into two parts: a DAB (dual active bridge) converter and a BLC (Bridgeless converter). In Figure 38, DAB is on the left-hand side of the diagram, while the BLC is on the right-hand side of the diagram. The primary side of the DAB converter is connected to the virtual bus, and the secondary side is connected to the Bridgeless converter via the DC link called v_B. On the other hand, the output of the Bridgeless converter is between the PV string and the central converter. In subsubsection 3.4.1, the modeling of DAB will be constructed. The modeling of BLC will be constructed in the subsubsection 3.4.2.

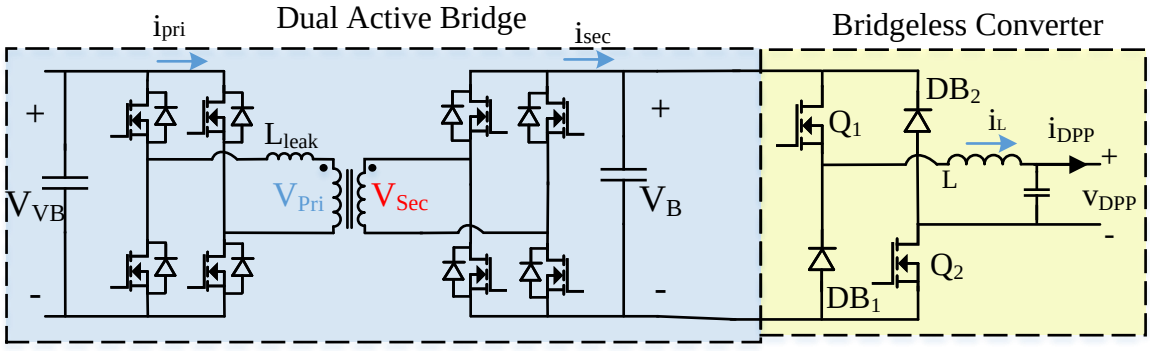


Figure 38: DPP converter consists of a DAB and BLC, Blue block represents DAB converter, DAB converter includes 8 transistors and a transformer. In the transformer, L_{leak} represents the leakage inductor. V_{pri} and V_{sec} indicate the voltage at the primary side and secondary side, respectively. On the BLC, there are 2 switches, namely Q_1 and Q_2. Also, 2 diodes exist in the BLC (DB_1 and DB_2). i_{DPP} and V_{DPP} represent the current and voltage in the P-DPP configuration. In other words, the product of i_{DPP} and V_{DPP} represents how much power is injected or withdrawn from the PV string. [6]

3.4.1 DAB

The power pass-through of a DAB converter can be expressed as [45]:

$$P = \frac{v_{VB} v_B \phi (1 - 2\phi)}{N_{trans} f_{sw} L_{leak}} \tag{41}$$

The current is the secondary side shown in Equation 42.

$$i_{sec} = \frac{v_{VB} \phi (1 - 2\phi)}{N_{trans} f_{sw} L_{leak}} \tag{42}$$

Where ϕ represents the phase angle difference between the primary side and secondary side, N_{trans} is the transformer turns ratio between the secondary side and primary side, f_{sw} is the switching frequency, and L_{leak} is the leakage inductance.

Controlling the phase angle (ϕ) in the DAB can help regulate the direction of power flow and magnitude of power transfer. There are two scenarios: one is ϕ greater than 0 another one is ϕ smaller than 0. Assume all the parameter

is fixed except the phase shift angle ϕ. To find the maximum value of P with respect to the variable ϕ in the Equation 41, one can analyze the function's derivative with respect to ϕ and locate the point where the derivative equals zero, indicating a potential maximum point—the expression in Equation 43.

$$\frac{\partial P}{\partial \phi} = \frac{v_{VB} v_B (1 - 4\phi)}{N_{trans} f_{sw} L_{leak}} \tag{43}$$

When maximum power transfers through DAB, in Equation 43, $\frac{\partial P}{\partial \phi} = 0$, therefore ϕ is equal to 0.25, in other words, when phase shift angle is 0.25, the DAB is transferred maximum power from the primary side to the secondary side. On the other hand, when the DAB is transferred maximum power in the opposite direction, the phase shift angle is equal to -0.25. Hence, the ϕ operation range is within absolute value 0.25, and the angle is between -90 and 90 degrees for degree conversion.

When the primary side voltage is leading the secondary side voltage (ϕ is greater than 0), the power flow is from the primary side to the secondary side. Figure 39 shows the primary side voltage leading to the secondary side voltage and power flow direction from the virtual bus side to the PV string.

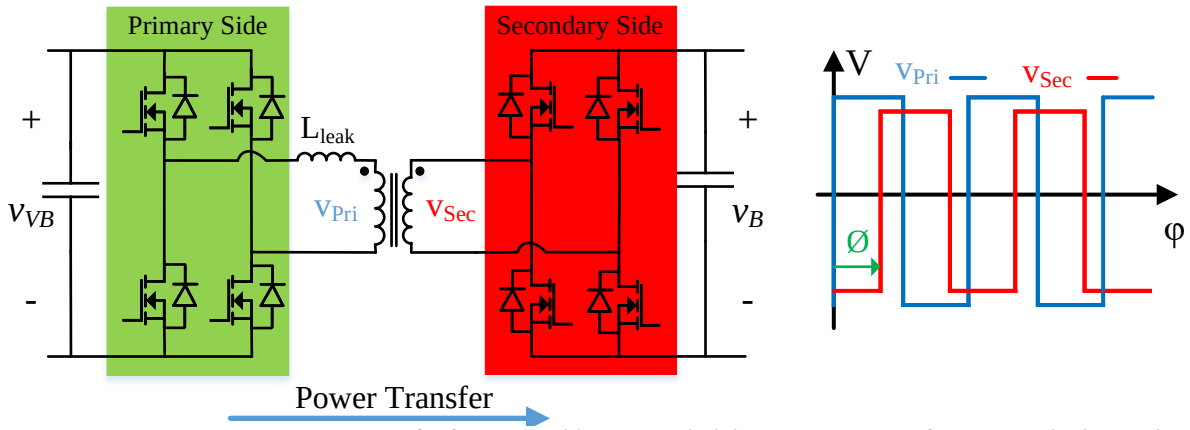


Figure 39: scenario $\phi > 0$, power transfer from virtual bus to DC link bus. First, a pair of primary side diagonal switches is on to create a path between the virtual bus voltage on the transformer's primary side and the transformer's primary side. This creates a voltage and stores energy on the transformer's primary windings. After that, the switch is off and isolates the primary side voltage source from the transformer. This helps prevent short circuits and allows energy to be transferred. In the intermediate state, all all switches are off. This intermediate state allows the energy stored in the transformer to be transferred to the secondary side without a direct connection. Following a pair of secondary side diagonal switches creates a path between the DC link bus voltage on the secondary side of the transformer and the secondary side.

On the other hand, when ϕ is smaller than 0, the primary side voltage lags the secondary side voltage, and the power flow is from the secondary to the primary side. Figure 42 shows the primary side voltage lagging concerning the secondary side voltage and power flow direction from the PV string to the virtual bus.

According to [45], a DAB large-signal diagram of the DAB can be expressed as Figure 44.

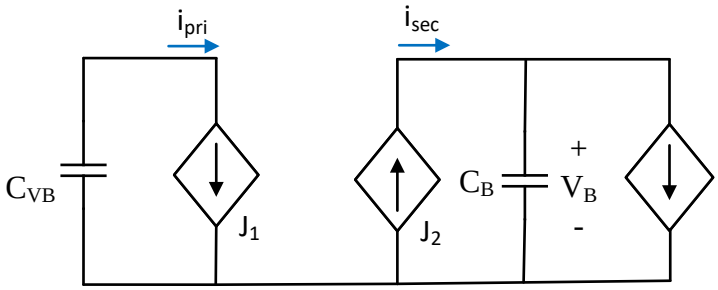


Figure 40: large-signal average mode of DAB

Refer to Figure 44, where J_1 and J_2 expression are show in Equation 44 and Equation 45

$$J_1 = \frac{v_{VB}\phi(1-2\phi)}{f_{sw}L_{leak}} \tag{44}$$

$$J_2 = \frac{v_{VB}\phi(1-2\phi)}{N_{trans}f_{sw}L_{leak}} \tag{45}$$

As shown in [46], the small signal of DAB can be expressed in Figure 47

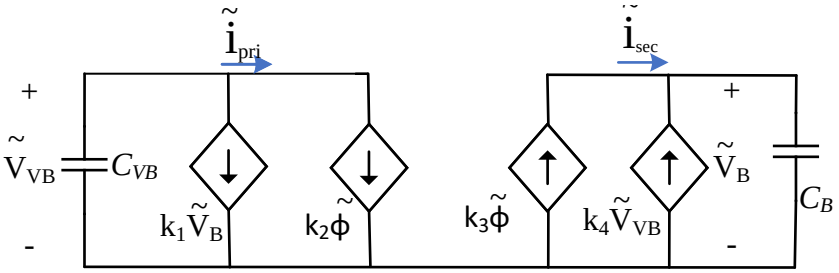


Figure 41: small signal model of the DPP

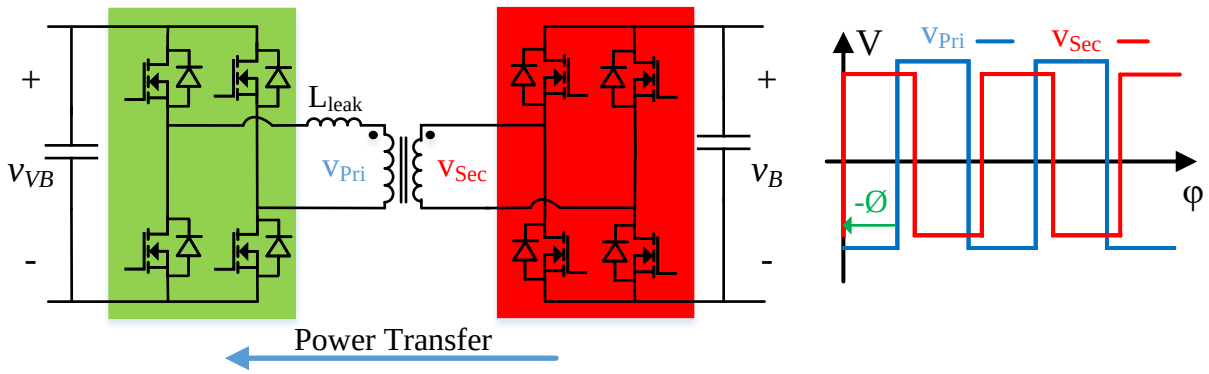


Figure 42: scenario $\phi < 0$, power transfer from DC link bus to virtual bus. First, a pair of secondary side diagonal switches is on to create a path between the DC link bus voltage on the transformer's secondary side and the transformer's secondary side. This creates a voltage and stores energy on the transformer's secondary windings. After that, the switch is off and isolates the secondary side voltage source from the transformer. This helps prevent short circuits and allows energy to be transferred. In the intermediate state, all all switches are off. This intermediate state allows the energy stored in the transformer to be transferred to the primary side without a direct connection. Following a pair of primary side diagonal switches creates a path between the DC link bus voltage on the primary side of the transformer and the primary side.

Refer to Figure 47, where k_1, k_2, k_3 and k_4 expression are show in Equation 46, Equation 47, Equation 48 and Equation 49 respectively.

$$k_1 = \frac{\phi_i(1-2\phi_i)}{f_{sw}L_{leak}C_{B_i}} \tag{46}$$

$$k_2 = \frac{v_{Bi}(1-4\phi_i)}{f_{sw}L_{leak}C_{B_i}} \tag{47}$$

$$k_3 = \frac{v_{VB}(1-4\phi_i)}{N_{trans}f_{sw}L_{leak}C_{B_i}} \tag{48}$$

$$k_4 = \frac{\phi_i(1-2\phi_i)}{N_{trans}f_{sw}L_{leak}C_{B_i}} \tag{49}$$

3.4.2 Bridgeless converter

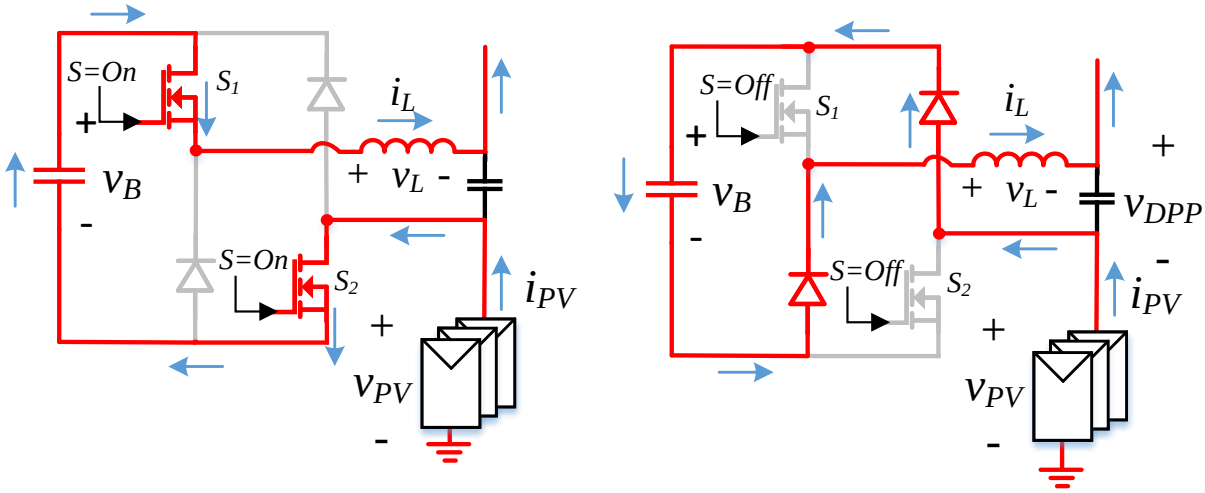
A bridgeless converter contains two active switches and two diodes in a non-isolated topology and typically employs pulse width modulation (PWM) to regulate the output voltage. In Figure 38, the v_{DPP} voltage are express in Equation 50:

$$v_{dpp} = (2d-1) \times v_B \tag{50}$$

Where d represents the switches S_1 and S_2 duty cycle. The duty cycle can be controlled using pulse width modulation (PWM) or other techniques. In PWM, the duty cycle is varied by adjusting the pulse width applied to the gate of the high-side and low-side switches. By varying the pulse width, the on-time of the switches can be adjusted, which in turn adjusts the converter's duty cycle.

Overall, controlling the duty cycle in a bridgeless converter is critical for achieving the desired output voltage and maintaining the converter's stability and efficiency. Proper control system design and implementation are essential for optimal converter performance[47].

As shown Figure 43a, while the switches are on, the polarity of the voltage before the LC output filter is the same as the input voltage, and the BLC input capacitor is discharged. On the other hand, when the switches are off, the BLC inverts the input voltage, and its capacitor is charged. To transfer the average power from the input to the output, the BLC duty cycle must be bigger than 0.5(D_{BLC}>0.5); otherwise, the average power direction is from the output. to the input.



(a) Switches on **(b)** Switches off

Figure 43: scenario for transistor stage On and OFF

The bridgeless converter's electrical properties are similar to the buck converter. Therefore, the large signal of the bridgeless converter can be referred to buck converter large signal model. Based on Equation 50, the large signal of the BLC schematic is shown in Figure 44.

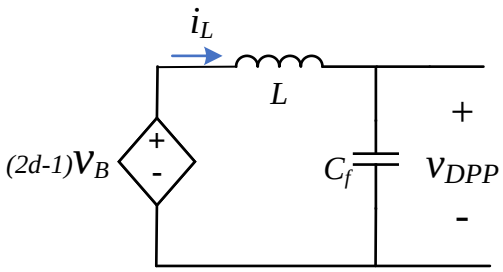


Figure 44: BLC large-signal average model

By differentiating the state variable and input, the small signal of the DPP schematic is shown in Figure 45.

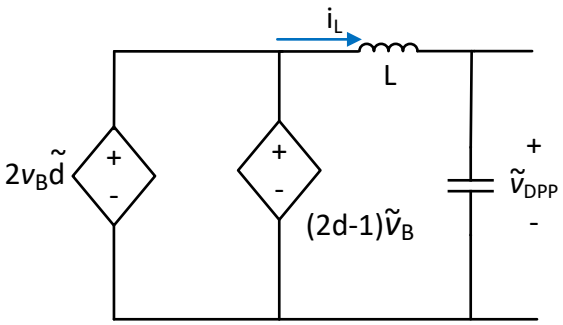


Figure 45: Small signal model of BLC

3.5 PV2VB P-DPP steady state analysis

In this section, mathematical models of the steady state for PV2VB P-DPP architecture will be constructed. The steady-state model is needed for analyzing dynamic behavior because it provides initial conditions for transient analysis and offers insights into stability and system performance.

To start with, the arbitrary PV module datasheet is selected, and the values of V_{mpp} and I_{mpp} are extracted. In the string, count how many PV modules connect in series, then the per string voltage is calculated as V_{mpp} time $N_{modules}$, the expression is shown in Equation 51.

$$V_{string}(i) = V_{mpp(i)} \times N_{modules(i)} \tag{51}$$

where $V_{string(i)}$ represents the i^{th} string voltage. Due to the series connection, the string current is equal to $I_{mpp}(i)$ assumed in the same string, the PV modules receive the same irradiance, and the expression is shown in Equation 52.

$$I_{string}(i) = I_{mpp}(i) \tag{52}$$

Where $I_{string}(i)$ represents the i^{th} string current, then the string power can be calculated, and the string power expression is shown in Equation 53.

$$P_{string(i)} = I_{string}(i) \times V_{string}(i) \tag{53}$$

Where $P_{string}(i)$ represents the i^{th} string power generated by the PV string, following the power delivered to the central converter is the sum of all string power; the expression is shown in Equation 54.

$$P_{CC} = \sum_{i=1}^{n} P_{string(i)} \tag{54}$$

Where P_{CC} represents the received central converter power. Refer to Figure 30, the current at the central converter is equal to the sum of each string current, Equation 55 shows the current pass through the central converter inductor.

$$i_{Ls} = \sum_{i=1}^{n} I_{mpp(i)} \tag{55}$$

Where i_{Ls} represents the average current pass through the central converter's inductor. following the central converter input voltage v_s can be calculated, the expression is shown in Equation 56.

$$v_s = \sum_{i=1}^{n} \frac{P_{CC}}{i_{Ls}} \tag{56}$$

Meanwhile, the voltage across the bridgeless converter (v_{DPP_i}) can be calculated based on Equation 57. Besides the central converter duty cycle can be calculated, the expression is shown in Equation 58.

$$v_{DPP_i} = v_s - V_{string}(i) \tag{57}$$

$$d_s = -\frac{v_s - V_{out}}{V_{out}} \tag{58}$$

Where d_s represents the duty of the central converter. After obtaining v_{DPP_i} and d_s, the duty cycle of the bridgeless converter (d_i) can be calculated, $v_{b(i)}$ value. The expression is shown in Equation 59.

$$d_i = \frac{v_b + v_{dpp_i}}{2 \times v_{B_i}} \tag{59}$$

Where v_{b_i} represents the i^{th} DC link voltage and the value of v_{B_i} is preset.
According to Equation 41, the last input ϕ_i can be calculated. by rearranging the Equation 41 into quadratic form $ax^2 + bx + c = 0$, Equation 60 shown the quadratic form for unknown ϕ_i.

$$\frac{v_{Vb} \times v_{B_i} \times (-2 \times \phi_i^2 + \phi_i)}{N_{trans} \times f_{sw} \times L_{leak}} - P_{string(i)} = 0 \tag{60}$$

In Equation 60 v_{Vb}, v_{B_i}, N_{trans}, f_{sw} and L_{leak} are pre-set value, $P_{string(i)}$ is calculated in Equation 53. ϕ_i can be calculated in Matlab software, applying the function called, *root*, ϕ_i unknown is solved based on the absolute value of ϕ_i being lower than 0.25; the excess solution can be eliminated. Based on the mathematical models of the steady state, Figure 46 shows the large signal model of a DPP connected to a PV string.

3.6 PV2VB P-DPP Dynamics

Now, combine the DAB and bridgeless converter into a single circuit. There are 3n+1 state variables in P-DPP v_{DPP_i}, v_{B_i},v_{VB}, and i_{DPP_i}. Note that in mathematical notation, the symbol "i" represents the PV string number, where "i" belongs to the range of 1 to n.

The transient voltage across inductor L_i can be found using the Equation 61 and group the state variable in function g_3.

$$\frac{\partial i_{L_i}(t)}{\partial t} = \frac{v_{B_i}(2d_i - 1) - v_{DPP_i}}{L_i} = g_{3_i}(v_{B_i}, d_i, v_{DPP_i}) \tag{61}$$

The transient current across capacitor C_{f_i} can be found using the Equation 62 and group the sate variable in function g_4.

$$\frac{\partial v_{DPP_i}(t))}{\partial t} = \frac{i_{DPP_i} - i_{PV_i}}{C_{fi}} = \frac{i_{DPP_i} - f_{PV_i}(v_s - v_{DPP_i})}{C_{fi}} = g_{4_i}(i_{DPP_i} v_s, v_{DPP_i}) \tag{62}$$

The instantaneous power across the virtual bus capacitor (C_{VB}) can be found using the Equation 63 base on instantaneous input power subtracted from instantaneous output power.

$$v_{VB} C_{VB} \frac{\partial v_{VB}(t)}{\partial t} = v_s \sum_{i=1}^{n} i_{Pv_i} - \sum_{i=1}^{n} v_{PV_i} i_{PV_i} \tag{63}$$

Rearrange it and group the state variable in function g_5.

$$\frac{\partial v_{VB}(t)}{\partial t} = -\frac{v_s \sum_{i=1}^{n} f(v_s - v_{DPP_i}) - \sum_{i=1}^{n} (v_s - v_{DPP_i}) f_{PV_i}(v_s - v_{DPP_i})}{C_{VB} v_{VB}} = g_5(v_{VB}, v_s, v_{DPP_i},) \tag{64}$$

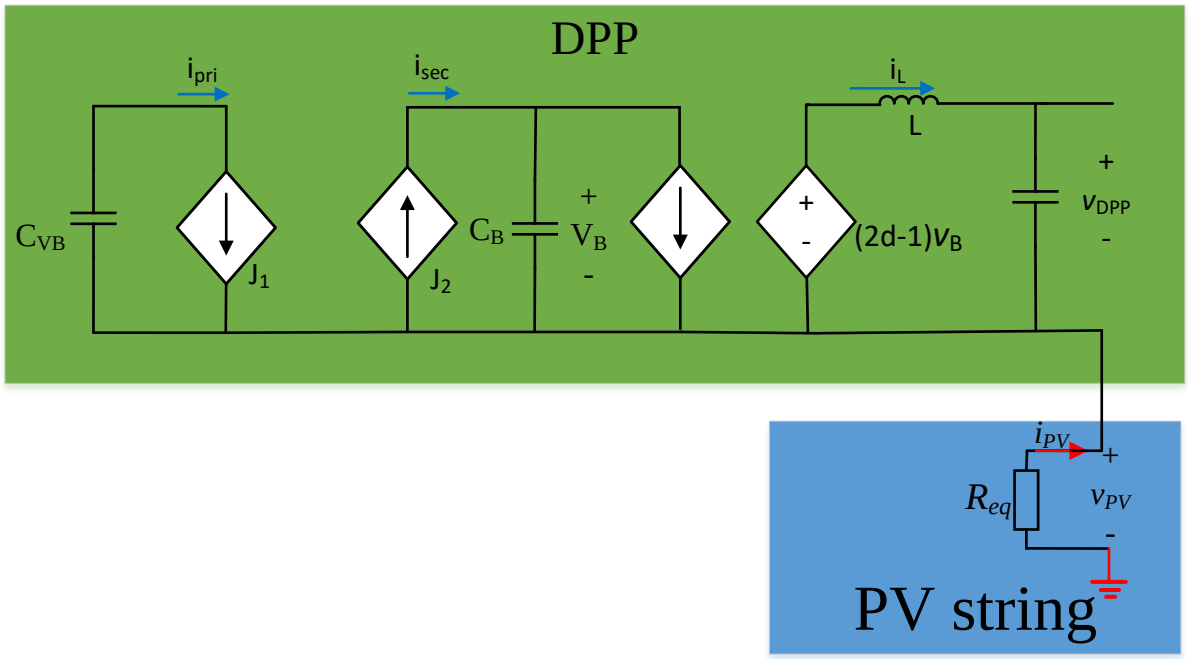


Figure 46: Large signal model of the DPP connected to the PV string

The transient current across capacitor C_B can be found using the Equation 65 and group the state variable in function g_6.

$$\frac{\partial v_{B_i}(t)}{\partial t} = \frac{v_{VB}\phi_i(1-2\phi_i)}{N_{trans}f_{sw}L_{leak}C_{B_i}} - \frac{(2d_i-1)i_{DPP_i}}{C_{B_i}} = g_{6_i}(i_{DPP_i}, d_i, v_{VB}, \phi_i) \tag{65}$$

To find the small signal model of the state variable, apply the partial derivative method. Equation 67, Equation 66, Equation 68, and Equation 69 present the partial differentiation of the small signal. v_{DPP_i},i_{DPP_i}, v_{VB} and v_{B_i} respectively.

$$\frac{\partial \tilde{\boldsymbol{v}_{\boldsymbol{DPP_i}}}(t)}{\partial t} = \frac{\partial g_{4_i}}{\partial i_{DPP_i}}\tilde{\boldsymbol{i}_{\boldsymbol{DPP_i}}}(t) + \frac{\partial g_4}{\partial v_s}\tilde{\boldsymbol{v}_{\boldsymbol{s}}}(t) + \frac{\partial g_{4_i}}{\partial v_{DPP_i}}\tilde{\boldsymbol{v}_{\boldsymbol{DPP_i}}}(t) \tag{66}$$

$$\frac{\partial \tilde{\boldsymbol{i}_{\boldsymbol{DPP_i}}}(t)}{\partial t} = \frac{\partial g_{3_i}}{\partial v_{B_i}}\tilde{\boldsymbol{v}_{\boldsymbol{B_i}}}(t) + \frac{\partial g_{3_i}}{\partial d_i}\tilde{\boldsymbol{d}_{\boldsymbol{i}}}(t) + \frac{\partial g_{3_i}}{\partial v_{DPP_i}}\tilde{\boldsymbol{v}_{\boldsymbol{DPP_i}}}(t) \tag{67}$$

$$\frac{\partial \tilde{\boldsymbol{v}_{\boldsymbol{VB}}}(t)}{\partial t} = \frac{\partial g_5}{\partial v_{VB}}\tilde{\boldsymbol{v}_{\boldsymbol{VB}}}(t) + \frac{\partial g_5}{\partial v_s}\tilde{\boldsymbol{v}_{\boldsymbol{s}}}(t) + \frac{\partial g_{5_i}}{\partial v_{DPP_i}}\tilde{\boldsymbol{v}_{\boldsymbol{DPP_i}}}(t) \tag{68}$$

$$\frac{\partial \tilde{\boldsymbol{v}_{\boldsymbol{B_i}}}(t)}{\partial t} = \frac{\partial g_{6_i}}{\partial i_{DPP_i}}\tilde{\boldsymbol{i}_{\boldsymbol{DPP_i}}}(t) + \frac{\partial g_{6_i}}{\partial d_i}\tilde{\boldsymbol{d}_{\boldsymbol{i}}}(t) + \frac{\partial g_6}{\partial v_{VB}}\tilde{\boldsymbol{v}_{\boldsymbol{VB}}}(t) + \frac{\partial g_6}{\partial \phi_i}\tilde{\boldsymbol{\phi}_{\boldsymbol{i}}}(t) \tag{69}$$

Each detailed partial derivative term is shown below.
g3:

$$\frac{\partial g_{3_i}}{\partial v_{B_i}} = \frac{(2d_i-1)}{L_i}\tilde{\boldsymbol{v}_{\boldsymbol{B_i}}}(t) \tag{70}$$

$$\frac{\partial g_{3_i}}{\partial d_i} = \frac{2v_{B_i}}{L_i}\tilde{\boldsymbol{d}_{\boldsymbol{i}}}(t) \tag{71}$$

$$\frac{\partial g_{3_i}}{\partial v_{Dpp_i}} = -\frac{1}{L_i}\tilde{\boldsymbol{v}_{\boldsymbol{Dpp_i}}}(t) \tag{72}$$

g4:

$$\frac{\partial g_{4_i}(t)}{\partial i_{DPP_i}} = \frac{1}{C_{f_i}}\tilde{\boldsymbol{i}_{\boldsymbol{DPP_i}}}(t) \tag{73}$$

$$\frac{\partial g_4(t)}{\partial v_s} = \frac{1}{C_{f_i}R_i}\tilde{\boldsymbol{v}_{\boldsymbol{s}}}(t) \tag{74}$$

$$\frac{\partial g_{4_i}(t)}{\partial v_{DPP_i}} = \frac{-1}{C_{fi}R_i} \tilde{v_{DPP_i}}(t) \tag{75}$$

g5:

$$\frac{\partial g_5(t)}{\partial v_{VB}} = \frac{v_s \sum_{i=1}^{n} f(v_s - v_{DPP_i}) - \sum_{i=1}^{n}(v_s - v_{DPP_i}) f_{PVi}(v_s - V_{DPP_i})}{C_{VB} v_{VB}^2} \tilde{\boldsymbol{v_{VB}}}(t) \tag{76}$$

$$\frac{\partial g_5(t)}{\partial v_s} = \frac{\sum_{i=1}^{n} f(v_s - v_{dpp_i})}{C_{VB} v_{VB}} \tilde{\boldsymbol{v_S}}(t) - \frac{\sum_{i=1}^{n} f(v_s - v_{dpp_i})}{C_{VB} v_{VB}} \tilde{\boldsymbol{v_S}}(t) + \frac{v_s \sum_{i=1}^{n} R_i}{C_{VB} v_{VB}} \tilde{\boldsymbol{v_S}} - \frac{\sum_{i=1}^{n}(v_s - v_{DPP_i}) R_i}{C_{VB} v_{VB}} \tilde{\boldsymbol{v_S}} \tag{77}$$

In Equation 77, the first two-term cancel each other, and the simplified coefficient of differential g5 with respect to v_s is shown in Equation 78.

$$\frac{\partial g_5(t)}{\partial v_s} = \frac{\sum_{i=1}^{n} v_{DPP_i}}{C_{VB} v_{VB} R_i} \tilde{\boldsymbol{v_S}}(t) \tag{78}$$

$$\frac{\partial g_{5_i}(t)}{\partial v_{DPP_i}} = \frac{-v_s \sum_{i=1}^{n} R_i + \sum_{i=1}^{n} f(v_s - v_{DPP_i}) + \sum_{i=1}^{n}(V_s - V_{DPP_i}) R_i}{C_{VB} v_{VB}} \tilde{\boldsymbol{v_{DPP_I}}}(t) \tag{79}$$

Similarly in Equation 79, after some term cancels each other, the simplified coefficient of differential g5 with respect to V_{DPP_i} coefficient is shown in Equation 80.

$$\frac{\partial g_{5_i}(t)}{\partial v_{PDP_i}} = \frac{-(\sum_{i=1}^{n} R_i v_{DPP_i} + \sum_{i=1}^{n} f(v_s - v_{DPP_i}))}{C_B v_{VB}} \tilde{\boldsymbol{v_{DPP_i}}}(t) \tag{80}$$

g6:

$$\frac{\partial g_{6_i}(t)}{\partial i_{L_i}} = -\frac{(2d_i - 1)}{C_{B_i}} \tilde{\boldsymbol{i_{L_i}}}(t) \tag{81}$$

$$\frac{\partial g_{6_i}(t)}{\partial d_i} = -\frac{2 i_{L_i}}{C_{B_i}} \tilde{\boldsymbol{d_i}}(t) \tag{82}$$

$$\frac{\partial g_{6_i}(t)}{\partial v_{VB}} = \frac{\phi_i(1 - 2\phi_i)}{N_{trans} f_{sw} L_{leak} C_{B_i}} \tilde{\boldsymbol{v_{VB}}}(t) \tag{83}$$

$$\frac{\partial g_{6_i}(t)}{\partial \phi_i} = \frac{v_{VB}(1 - 4\phi_i)}{N_{trans} f_{sw} L_{leak} C_{B_i}} \tilde{\boldsymbol{\phi_i}}(t) \tag{84}$$

Figure 47 shows the small signal model of a DPP connected to a PV string.

3.7 Figure for large average and small signal model in PV2VB P-DPP

After modeling the central converter, PV modules, and DPP (DAB BLC), PV2VB P-DPP can be modeled, Figure 48 shows the large signal model of PV2VB P-DPP which consists of components of the central converter, PV modules, and DPP (DAB BLC). Large signal analysis, commonly referred to as nonlinear analysis, examines how a circuit will behave under demanding operating conditions or input signals that could materially alter component performance.

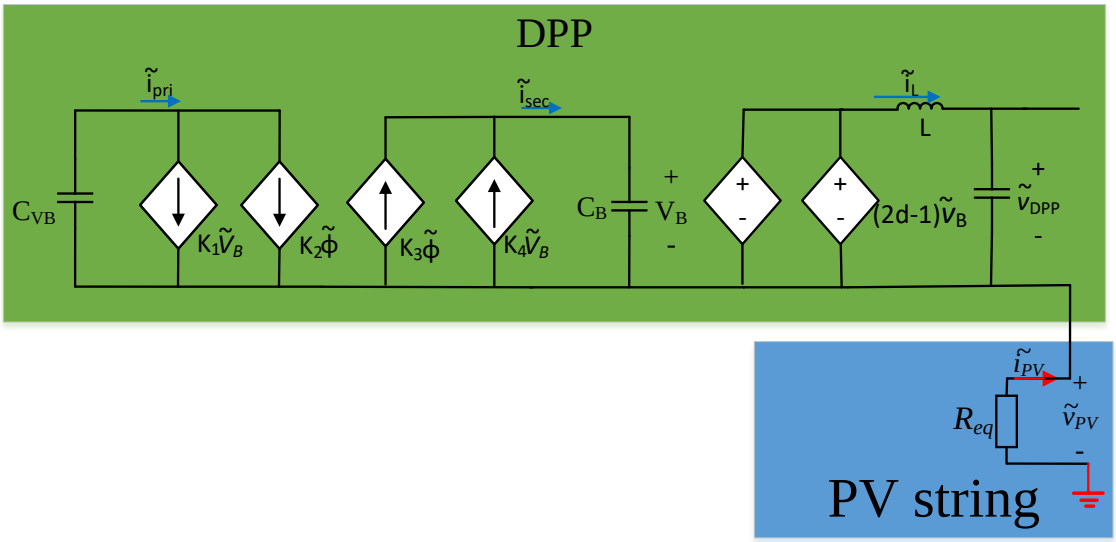


Figure 47: Small signal model of the DPP

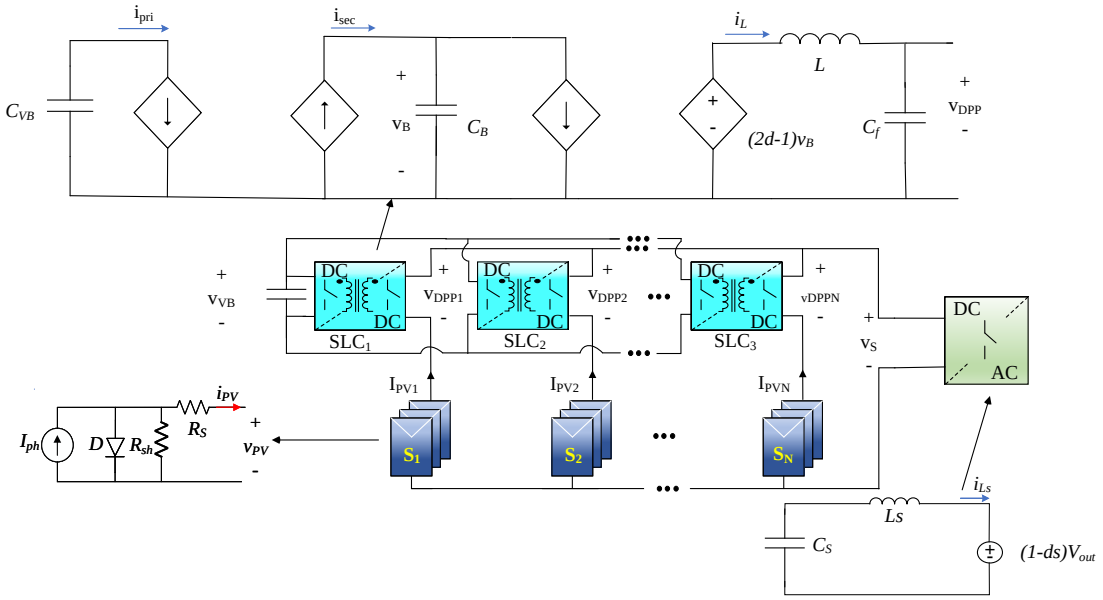


Figure 48: Large signal model of PV2VB P-DPP

On the other hand, small signal analysis examines the linear performance of a circuit around an operational point. Figure 49 shows the small signal model of PV2VB P-DPP dirgram.

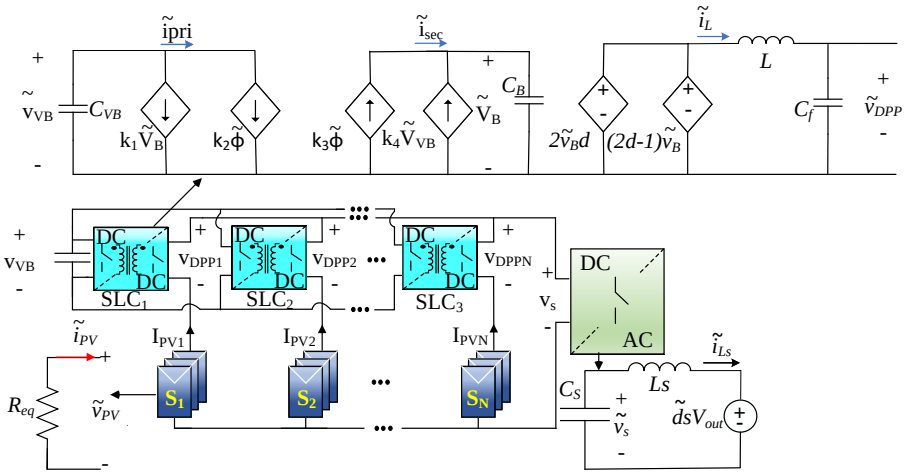


Figure 49: Small signal of model PV2VB P-DPP

3.8 State Space equation for PV2VB P-DPP

A typical state space equation is expressed in Equation 85.

$$\dot{\tilde{\boldsymbol{x}}}(t) = A\tilde{\boldsymbol{x}}(t) + B\boldsymbol{u}(t) \tag{85}$$

Where $\tilde{\boldsymbol{x}}$(t) represents the small signal state vector:

$$\tilde{\boldsymbol{x}}(t) = \begin{pmatrix} \tilde{v}_{DPP_1}(t) \\ \tilde{v}_{DPP_2}(t) \\ \vdots \\ \tilde{v}_{DPP_n}(t) \\ \tilde{i}_{DPP_1}(t) \\ \tilde{i}_{DPP_2}(t) \\ \vdots \\ \tilde{i}_{DPP_n}(t) \\ \tilde{v}_{B1}(t) \\ \tilde{v}_{B2}(t) \\ \vdots \\ \tilde{v}_{Bn}(t) \\ \tilde{v}_s(t) \\ \tilde{i}_{Ls}(t) \\ \tilde{v}_{VB}(t) \end{pmatrix} \tag{86}$$

And u(t) represents the input vector:

$$\boldsymbol{u}(t) = \begin{pmatrix} \tilde{\phi}_1(t) \\ \tilde{\phi}_2(t) \\ \vdots \\ \tilde{\phi}_n(t) \\ \tilde{d}_1(t) \\ \tilde{d}_2(t) \\ \vdots \\ \tilde{d}_n(t) \\ \tilde{d}_S(t) \end{pmatrix} \tag{87}$$

There are 3n+3 state variables. because each P-DPP has 3 state variables, and the central converter contains 3 state variables. The dimension of $\tilde{\boldsymbol{X}}$ (t) is $(3n+3)$. Therefore, matrix A size is $(3n+3\times 3n+3)$. For the input/control variable,

there are 2 input variables in a single P-DPP and 1 input/control variable in the central converter.
Because matrices A and B are extremely large, to simplify the matrix expression, the terms of block matrices were introduced, and each block matrix will be defined in terms of the coefficients from the dynamic equations of the preceding subsections. To match the matrix size, From A_{11} to A_{33}, A_{14} to A_{36}, A_{41} to A_{63} ,and A_{44} to A_{66} the matrix size are $(n \times n)$, $(n \times 1)$, $(1 \times n)$, and (1×1) respectively.

$$A = \begin{pmatrix} A_{11} & A_{12} & A_{13} & A_{14} & A_{15} & A_{16} \\ A_{21} & A_{22} & A_{23} & A_{24} & A_{25} & A_{26} \\ A_{31} & A_{32} & A_{33} & A_{34} & A_{35} & A_{36} \\ A_{41} & A_{42} & A_{43} & A_{44} & A_{45} & A_{46} \\ A_{51} & A_{52} & A_{53} & A_{54} & A_{55} & A_{56} \\ A_{61} & A_{62} & A_{63} & A_{64} & A_{65} & A_{66} \end{pmatrix} \tag{88}$$

In A_{11} to A_{16} and B_{11} to B_{13} represent Equation 66 in state-space form, in A_{11} represents the partial derivative respect to i_{DPP_i}, A_{12} represents the partial derivative respect to v_{DPP_i}, and A_{14} represents the partial derivative respect to v_s. Based on Equation 66, the rest of the matrix in A_{11} to A_{16} and B_{11} to B_{13} are filled with zeros, indicating that the small signal of v_{DPP_i} only involves these three state variables.

$$A_{11} = \begin{pmatrix} \frac{-1}{Cf_1R_1} & 0 & \cdots & 0 \\ 0 & \frac{-1}{Cf_2R_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{-1}{Cf_nR_n} \end{pmatrix} \tag{89}$$

$$A_{12} = \begin{pmatrix} \frac{1}{Cf_1} & 0 & \cdots & 0 \\ 0 & \frac{1}{Cf_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{1}{Cf_n} \end{pmatrix} \tag{90}$$

$$A_{13} = \begin{pmatrix} 0 \end{pmatrix}^{n \times n} \tag{91}$$

$$A_{14} = \begin{pmatrix} \frac{1}{Cf_1R_1} \\ \frac{1}{Cf_2R_2} \\ \vdots \\ \frac{1}{Cf_nR_n} \end{pmatrix} \tag{92}$$

$$A_{15} = \begin{pmatrix} 0 \end{pmatrix}^{n \times 1} \tag{93}$$

$$A_{16} = \begin{pmatrix} 0 \end{pmatrix}^{n \times 1} \tag{94}$$

In A_{21} to A_{26} and B_{21} to B_{23} represent Equation 67 in state-space form, in A_{21} represents the partial derivative respect to i_{DPP_i}, A_{23} represents the partial derivative respect to v_{B_i}. Moreover, B_{22} represents the partial derivative respect to d_i. Based on Equation 67, the rest of the matrix is zero in A_{21} to A_{26} and B_{21} to B_{23} are filled with zeros, indicating that the small signal of i_{DPP_i} only involves these two state variables and one input variable.

$$A_{21} = \begin{pmatrix} -\frac{1}{L_1} & 0 & \cdots & 0 \\ 0 & -\frac{1}{L_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -\frac{1}{L_n} \end{pmatrix} \tag{95}$$

$$A_{22} = \begin{pmatrix} 0 \end{pmatrix}^{n \times n} \tag{96}$$

$$A_{23} = \begin{pmatrix} \frac{2d_1-1}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{2d_2-1}{L_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{2d_n-1}{L_n} \end{pmatrix} \tag{97}$$

$$A_{24} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{98}$$

$$A_{25} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{99}$$

$$A_{26} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{100}$$

In A_{31} to A_{36} and B_{31} to B_{33} represent Equation 69 in state-space form, in A_{32} represents the partial derivative respect to v_{DPP_i}, A_{36} represents the partial derivative respect to v_{VB}. Moreover, B_{31} represents the partial derivative respect to ϕ_i, and B_{32} represents the partial derivative respect to d_i. Based on Equation 69, the rest of the matrix in A_{31} to A_{36} and B_{31} to B_{33} are filled with zeros, indicating that the small signal of v_{B_i} only involve these two state variables and two input variables.

$$A_{31} = \begin{pmatrix} 0 \end{pmatrix}^{n\times n} \tag{101}$$

$$A_{32} = \begin{pmatrix} -\frac{2d_1-1}{CB_1} & 0 & \cdots & 0 \\ 0 & -\frac{2d_2-1}{CB_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -\frac{2d_1-1}{CB_1} \end{pmatrix} \tag{102}$$

$$A_{33} = \begin{pmatrix} 0 \end{pmatrix}^{n\times n} \tag{103}$$

$$A_{34} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{104}$$

$$A_{26} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{105}$$

$$A_{36} = \begin{pmatrix} \frac{\phi_1\times(1-2\times\phi_1)}{N_{trans}\times f_{sw}\times L_{leak}\times CB_1} \\ \frac{\phi_2\times(1-2\times\phi_2)}{N_{trans}\times f_{sw}\times L_{leak}\times CB_2} \\ \vdots \\ \frac{\phi_n\times(1-2\times\phi_n)}{N_{trans}\times f_{sw}\times L_{leak}\times CB_n} \end{pmatrix} \tag{106}$$

In A_{41} to A_{46} and B_{41} to B_{43} represent Equation 33 in state-space form, in A_{41} represents the partial derivative respect to v_{DPP_i}, A_{44} represents the partial derivative respect to V_s, and A_{45} represents the partial derivative respect to V_s. Based on Equation 33, the rest of the matrix in A_{41} to A_{46} and B_{41} to B_{43} are filled with zeros, indicating that the small signal of v_s only involves these three state variables and one input variable.

$$A_{41} = \begin{pmatrix} \frac{1}{CsR_1} & \frac{1}{C_sR_2} & \cdots \frac{1}{C_sR_n} \end{pmatrix} \tag{107}$$

$$A_{42} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{108}$$

$$A_{43} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{109}$$

$$A_{44} = \begin{pmatrix} \frac{-1}{\sum_{i=1}^{n} R_i C_s} \end{pmatrix} \tag{110}$$

$$A_{45} = \begin{pmatrix} \frac{-1}{C_s} \end{pmatrix} \tag{111}$$

$$A_{46} = \begin{pmatrix} 0 \end{pmatrix}^{1\times 1} \tag{112}$$

In A_{51} to A_{56} and B_{51} to B_{53} represent Equation 32 in state space equation, in A_{54} represents the partial derivative respect to v_S,and B_{53} represents the partial derivative respect to D_s. Based on Equation 32, the rest of the matrix in

A_{51} to A_{56} and B_{51} to B_{53} are filled with zeros, indicating that the small signal of i_{Ls} only involves these one state variables and one input variable.

$$A_{51} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{113}$$

$$A_{52} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{114}$$

$$A_{53} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{115}$$

$$A_{54} = \begin{pmatrix} \frac{1}{L_s} \end{pmatrix} \tag{116}$$

$$A_{55} = \begin{pmatrix} 0 \end{pmatrix}^{1\times 1} \tag{117}$$

$$A_{56} = \begin{pmatrix} 0 \end{pmatrix}^{1\times 1} \tag{118}$$

In A_{61} to A_{66} and B_{61} to B_{63} represent Equation 68 in state space equation, in A_{61} represents the partial derivative respect to V_{DPP_i}, A_{64} represents the partial derivative respect to v_s, and A_{66} represents the partial derivative respect to v_{VB}. Based on Equation 68, the rest of the matrix in A_{61} to A_{66} and B_{61} to B_{63} are filled with zeros, indicating that the small signal of v_{VB} only involve these three state variables.

$$A_{61} = \begin{pmatrix} \frac{-(R_1 v_{DPP_1} + f(v_s - v_{DPP_i}))}{CVB v_{VB}} & \frac{-(R_2 v_{DPP_2} + f(v_s - v_{DPP_i}))}{C_{VB} v_{VB}} & \cdots \frac{-(R_n v_{DPP_n} + f(v_s - v_{DPP_n}))}{C_{VB} v_{VB}} \end{pmatrix} \tag{119}$$

$$A_{62} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{120}$$

$$A_{63} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{121}$$

$$A_{64} = \begin{pmatrix} \frac{\sum_{i=1}^{n} R_i v_{DPP_i}}{C_{VB} v_{VB}} \end{pmatrix} \tag{122}$$

$$A_{65} = \begin{pmatrix} 0 \end{pmatrix}^{1\times 1} \tag{123}$$

$$A_{66} = \begin{pmatrix} \frac{v_s \sum_{i=1}^{n} f(v_s - v_{DPP_i}) - \sum_{i=1}^{n} (v_s - v_{DPP_i}) f(v_s - v_{DPP_i})}{C_{VB} v_{VB}^2} \end{pmatrix} \tag{124}$$

Similarly, in Matrix B the sum of the sub-matrix block has to match. From B_{11} to B_{32}, B_{13} to B_{33}, B_{41} to B_{62} ,and B_{43} to B_{63} the matrix size are $(n \times n)$, $(n \times 1)$, $(1 \times n)$,and (1×1) respectively. Hence, the total input variable is $(2n+1)$, the matrix size of matrix B is $(3n + 3 \times 2n + 1)$.

$$B = \begin{pmatrix} B_{11} & B_{12} & B_{13} \\ B_{21} & B_{22} & B_{23} \\ B_{31} & B_{32} & B_{33} \\ B_{41} & B_{42} & B_{43} \\ B_{51} & B_{52} & B_{53} \\ B_{61} & B_{62} & B_{63} \end{pmatrix} \tag{125}$$

$$B_{11} = \begin{pmatrix} 0 \end{pmatrix}^{n\times n} \tag{126}$$

$$B_{12} = \begin{pmatrix} 0 \end{pmatrix}^{n\times n} \tag{127}$$

$$B_{13} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{128}$$

$$B_{21} = \begin{pmatrix} 0 \end{pmatrix}^{n\times n} \tag{129}$$

$$B_{22} = \begin{pmatrix} \frac{2v_{B1}}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{2v_{B2}}{L_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{2v_{Bn}}{L_n} \end{pmatrix} \tag{130}$$

$$B_{23} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{131}$$

$$B_{31} = \begin{pmatrix} \frac{v_{VB}\times(1-4\times\phi_1)}{N_{trans}\times f_{sw}\times L_{leak}\times CB_1} & 0 & \cdots & 0 \\ 0 & \frac{v_{VB}\times(1-4\times\phi_2)}{N_{trans}\times f_{sw}\times L_{leak}\times CB_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{v_{VB}\times(1-4\times\phi_n)}{N_{trans}\times f_{sw}\times L_{leak}\times CB_n} \end{pmatrix} \tag{132}$$

$$B_{32} = \begin{pmatrix} -\frac{2i_{DPP_1}}{CB_1} & 0 & \cdots & 0 \\ 0 & -\frac{2i_{DPP_2}}{CB_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -\frac{2i_{DPP_n}}{CB_n} \end{pmatrix} \tag{133}$$

$$B_{33} = \begin{pmatrix} 0 \end{pmatrix}^{n\times 1} \tag{134}$$

$$B_{41} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{135}$$

$$B_{42} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{136}$$

$$B_{43} = \begin{pmatrix} 0 \end{pmatrix}^{1\times 1} \tag{137}$$

$$B_{51} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{138}$$

$$B_{52} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{139}$$

$$B_{53} = \frac{V_{out}}{L_s} \tag{140}$$

$$B_{61} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{141}$$

$$B_{62} = \begin{pmatrix} 0 \end{pmatrix}^{1\times n} \tag{142}$$

$$B_{63} = \begin{pmatrix} 0 \end{pmatrix}^{1\times 1} \tag{143}$$

4 Simulations testing result

In the previous chapter, the general model of PV2VB P-DPP was established in a state space form. In this chapter, a PV2VB P-DPP system made of 2 PV strings is implemented in Matlab. Firstly, in subsection 4.1, the state space equation for the two string model is established. Following in subsection 4.2, by changing the number of bypassed PV modules in string two, an analysis of the minimum capacitor requirement in the virtual bus is performed. In subsection 4.3, sensitivity analysis of passive components in central converters and DPPs is performed. subsection 4.4 provide stability margin analysis. subsection 4.5 provide how the PI controller is implemented on the 2-string PV2VB P-DPP system. Finally, subsection 4.6 provides proper design for the central converter and DPP converter.

4.1 Two string model introduction

To simplify the model, the DPP of both strings is designed identically; in other words, two DAB converters and two BLC converters have the same specifications. In addition, it is assumed that both strings are equal, consisting of the same number of PV modules, and all PV modules are identical. All the parameters, like the inductor and capacitor value in BLC, are the same. Figure 50 shows the schematic of two string P-DPP PV2VB and Equation 144 and Equation 145 show the state matrix and Input-to-state matrix respectively. Note that, in Figure 50, the I_{PV1} and I_{PV2} respectively represent the currents generated by PV String 1 and PV String 2. SLC_1 and SLC_2 respectively represent the DPP corresponding to PV String 1 and PV String 2, V_{DPP_1} and V_{DPP_2} respectively represent the voltage either injected or extracted to the SLC_1 and SLC_2. Last but not least, V_s represents the input voltage at the central converter. Besides, Figure 51 shows the details of two string P-DPP PV2VB with details of every component, including the DPP converter split into two parts DAB and BLC, a single resistor represents the PV string module, and the central converter composes by diode, inductor, capacitor, and transistor.

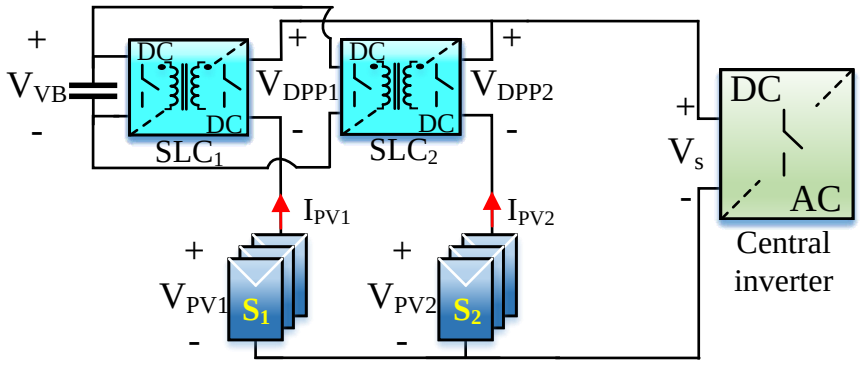


Figure 50: 2 string PV2VB P-DPP schematic

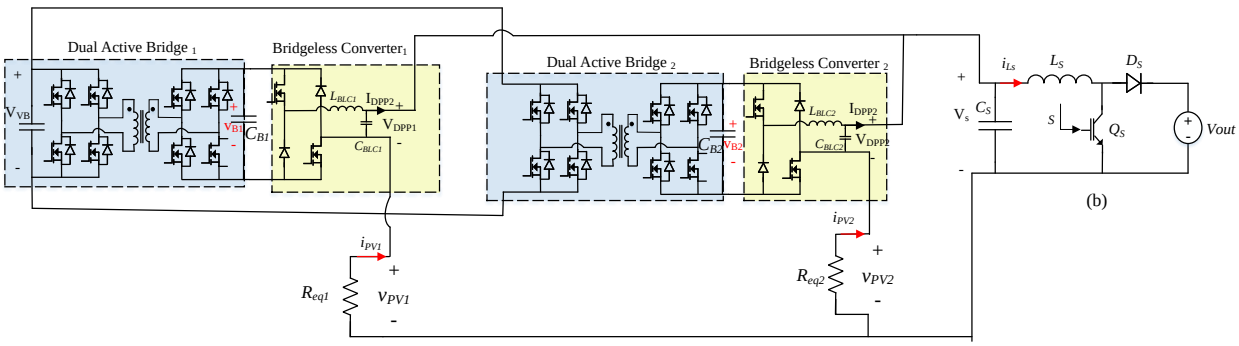


Figure 51: 2 string PV2VB P-DPP schematic with detail of how DPP connects to the virtual bus, PV string, and central converter.

$$A=\begin{pmatrix} \frac{-1}{R_1Cf} & 0 & \frac{1}{Cf} & 0 & 0 & 0 & \frac{1}{R_1C_f} & 0 & 0 \\ 0 & \frac{-1}{R_2Cf} & 0 & \frac{1}{Cf} & 0 & 0 & \frac{1}{R_2C_f} & 0 & 0 \\ \frac{-1}{Cf} & 0 & 0 & 0 & \frac{2d_1-1}{L_f} & 0 & 0 & 0 & \frac{\phi_1\times(1-2\times\phi_1)}{N_{trans}\times f_{sw}\times L_{leak}\times CB} \\ 0 & \frac{-1}{Cf} & 0 & 0 & 0 & \frac{2d_2-1}{L_f} & 0 & 0 & \frac{\phi_2\times(1-2\times\phi_2)}{N_{trans}\times f_{sw}\times L_{leak}\times CB} \\ 0 & 0 & -\frac{2d_1-1}{C_B} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{2d_1-1}{C_B} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{R_1C_s} & \frac{1}{R_2C_s} & 0 & 0 & 0 & 0 & \frac{-1}{(R1+R2)C_s} & \frac{-1}{C_s} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_s} & 0 & 0 \\ \frac{-I_{pv1}-\frac{v_{dpp1}}{R_1}}{C_{VB}v_{VB}} & \frac{-I_{pv2}-\frac{v_{dpp2}}{R_2}}{C_{VB}v_{VB}} & 0 & 0 & 0 & 0 & \frac{\frac{v_{dpp1}}{R1}+\frac{v_{dpp2}}{R2}}{C_{VB}v_{VB}} & 0 & \frac{v_{dpp1}i_{pv_1}+v_{dpp2}i_{pv_2}}{C_{VB}v_{VB}^2} \end{pmatrix} \tag{144}$$

$$B=\begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{2v_{B1}}{L_f} & 0 & 0 \\ 0 & 0 & 0 & \frac{2v_{B2}}{L_f} & 0 \\ \frac{v_{VB}\times(1-4\times\phi_1)}{N_{trans}\times f_{sw}\times L_{leak}\times CB} & 0 & -\frac{2i_{DPP_1}}{CB} & 0 & 0 \\ 0 & \frac{v_{VB}\times(1-4\times\phi_2)}{N_{trans}\times f_{sw}\times L_{leak}\times CB} & 0 & -\frac{2i_{DPP_2}}{CB} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{V_{out}}{L_s} \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \tag{145}$$

Refer to Equation 86, in 2 string model there are nine state variables; the order is shown in Equation 146 :

$$\tilde{\boldsymbol{x}}(t)=\begin{pmatrix} \tilde{v}_{DPP_1}(t) \\ \tilde{v}_{DPP_2}(t) \\ \tilde{i}_{DPP_1}(t) \\ \tilde{i}_{DPP_2}(t) \\ \tilde{v}_{B1}(t) \\ \tilde{v}_{B2}(t) \\ \tilde{v}_s(t) \\ \tilde{i}_{Ls}(t) \\ \tilde{v}_{VB}(t) \end{pmatrix} \tag{146}$$

Refer to Equation 87, in two string model there are five small signal input ; the order is shown in Equation 147 :

$$\boldsymbol{u}(t)=\begin{pmatrix} \tilde{\phi}_1(t) \\ \tilde{\phi}_2(t) \\ \tilde{d}_1(t) \\ \tilde{d}_2(t) \\ \tilde{d}_S(t) \end{pmatrix} \tag{147}$$

By the definition of the state space equation, the output expression is shown in Equation 148:

$$\boldsymbol{Y}=\boldsymbol{C}\boldsymbol{x}+\boldsymbol{D}\boldsymbol{u} \tag{148}$$

where $\boldsymbol{Y}$ represents the output of the system. $\boldsymbol{C}$ is the output matrix. It defines how the state variables $\boldsymbol{x}$ contribute to the system's output $\boldsymbol{Y}$. $\boldsymbol{D}$ is the input matrix. It describes how the control input $\boldsymbol{u}$ affects the state variables $\boldsymbol{x}$ [48]. When converting a state-space representation to a transfer function, it's common to assume that there are no direct feedforward inputs from the control input $\boldsymbol{u}$ to the output $\boldsymbol{Y}$. In other words, $\boldsymbol{B}$ is often assumed to be zero for this purpose. The output matrix for virtual bus voltage (v_{VB}) output is given in Equation 149.

$$C=\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \tag{149}$$

Moreover, the transfer function required a single output, although multiple transfer functions are possible for a system with multiple outputs. Select a single output in Matlab, and there is a function called ss2tf(A,B,C,D,ni), where the ni represents which input of a system with multiple inputs is excited by a unit impulse. For instance, if the user

wants to select $\tilde{d_S}(t)$, then the state space to transfer function must expressed in ss2tf(A,B,C,D,5). Convert state-space representation to transfer function is shown in Equation 150:

$$\boldsymbol{H}(s) = \frac{\boldsymbol{Y}(s)}{\boldsymbol{u}(s)} = \boldsymbol{C}(sI - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D} \tag{150}$$

Refer to subsection 3.5, the preset data of solar module are shown in Table 3; the state variable data are shown in Table 4, the input variable data are shown in Table 5, and the DPP converter and central converter passive element value is shown in Table 6.

Table 3: SolarTech MonoSi TS60-6M3-270S data sheet [49]

Maximum power	P_{max}	270	W
Open circuit	V_{oc}	38.79	V
Maximum power point voltage	V_{mpp}	31.19	V
Short circuit current	I_{sc}	9.37	A
Maximum power point current	I_{mpp}	8.69	A

Table 4: State variable data

v_{DPP_i}	Equation 57	V
i_{DPP_i}	i_{PV_i}	A
v_{B_i}	200	V
v_s	Equation 56	V
i_{Ls}	Equation 55	A
v_{VB}	200	V

Table 5: input variable data

ϕ_i	Equation 60	degree/ radian
d_i	Equation 59	N.A
d_s	Equation 58	N.A

Table 6: Passive element and transformer parameter

C_{BLC}	1×10^{-6}	F
L_{BLC}	500×10^{-6}	H
f_{sw}	1×10^{5}	Hz
N_{trans}	1	turns
L_{leak}	22×10^{-6}	H
C_B	100×10^{-6}	F
C_s	7×10^{-6}	F
L_s	2.5×10^{-3}	H

4.2 Analysis transfer function between v_{VB} and d_s

The transfer function between v_{VB} and d_s will be investigated because the central converter duty cycle directly controls the virtual bus voltage. In other words, d_s represents the transfer function input, and v_{VB} represents the transfer function output. Based on the transfer function of v_{VB} to d_s, stability and minimum capacitor for the virtual bus is determined. Each string contains 10 PV modules. To test the P-DDP PV2VB dynamic behavior, the following case is simulated: all the PV modules belonging to string 1 are uniformly illuminated, whereas string 2 is partially shaded. Illuminated PV modules are supposed to be subject to standard test conditions (irradiance equal to 1000 W/m^2 and operating temperature of 25 C), whereas shaded PV modules are bypassed by their own bypass diodes. Therefore, the operating voltage of string 1 is always equal to 10 times the MPP voltage of a single module (see Table 3). Whereas the operating voltage of string 2 depends on the number of modules that are bypassed. For instance, when 1 module is bypassed - that is 9 PV modules are producing power in the string, $V_{string2}$ is equal to 9 times the MPP voltage of a single PV module (see Table 3). Different cases are simulated, where the number of shaded/bypassed PV modules in string 2 varies from one to nine. Therefore, the DPP converter can either inject or withdraw power from the PV strings so PV strings are able to operate at their respective MPP, and the virtual bus capacitor starts to exchange power from string 1 to string 2.

The reason to restrict 10 PV modules per PV string is that the string voltage should be lower than the output voltage (400 V). Suppose the string voltage is higher than the output voltage due to the central converter being a boost converter. In that case, the input voltage (v_s) is higher than the output voltage (V_{out}), so the duty cycle becomes negative. The duty cycle operation range must be between 0-1. Hence, the boost converter is no longer functioning. The conducting experiment is to ensure that PV modules in string 1 are always working. And change the number of working PV modules from 9 to 1 in string 2. In other words, the number of bypassed PV modules is increased from 1 to 9. Meanwhile, when the number of bypassed PV modules is 1 to 9, record the minimum requirement capacitor for the virtual bus to maintain stability.

Figure 52 shows the flow chart of how to determine the minimum capacitor on the virtual bus. First, select the value of C_{vb} at the μF range capacitors because most of the microfarad range is commonly used in power supply filtering and energy storage. So the initial value of C_{VB} is 1μF. To determine whether the transfer function is stable or not, check the transfer function poles. If the system is stable, all the poles of its transfer function lie in the left half plane (LHP) of the complex plane. The complex plane, also known as the s-plane, is a fundamental tool for analyzing and designing linear time-invariant (LTI) systems. It is a graphical representation of complex numbers used to study the behavior of systems in the frequency domain. If the system is unstable, it has at least one pole located in the right-half plane (RHP) of the complex plane. The right-half plane is the region where the real parts of complex numbers are positive. To determine the minimum virtual bus capacitor, if the system response is stable, gradually reduce the value of C_{vb} 0.1 μF each time until the response becomes unstable. Then, select the smallest capacitance value ensuring system stability as the minimum value for C_{vb}. On the other hand, if the random value of C_{vb} reacts unstable, then increases the value of C_{VB} 1 μF each time until the system is stable, then selects the first value ensuring stability.

Figure 53 shows the simulation of minimum virtual bus capacitor requirements against the number of bypassed PV module changes at string two. The number of bypassed PV modules changes from 1-9. In other words, the number of fully functional PV modules reduced from 9-1.

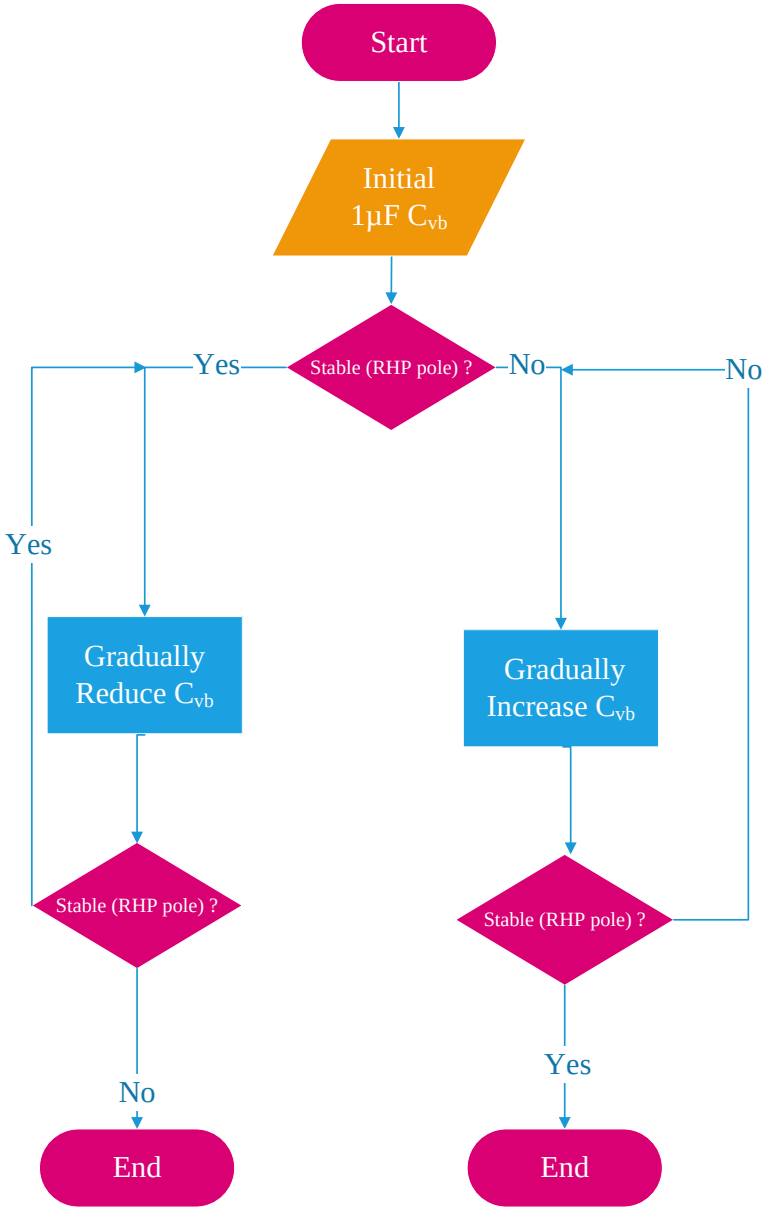


Figure 52: Determine the minimum C_{vb} flow chart based on the system stability

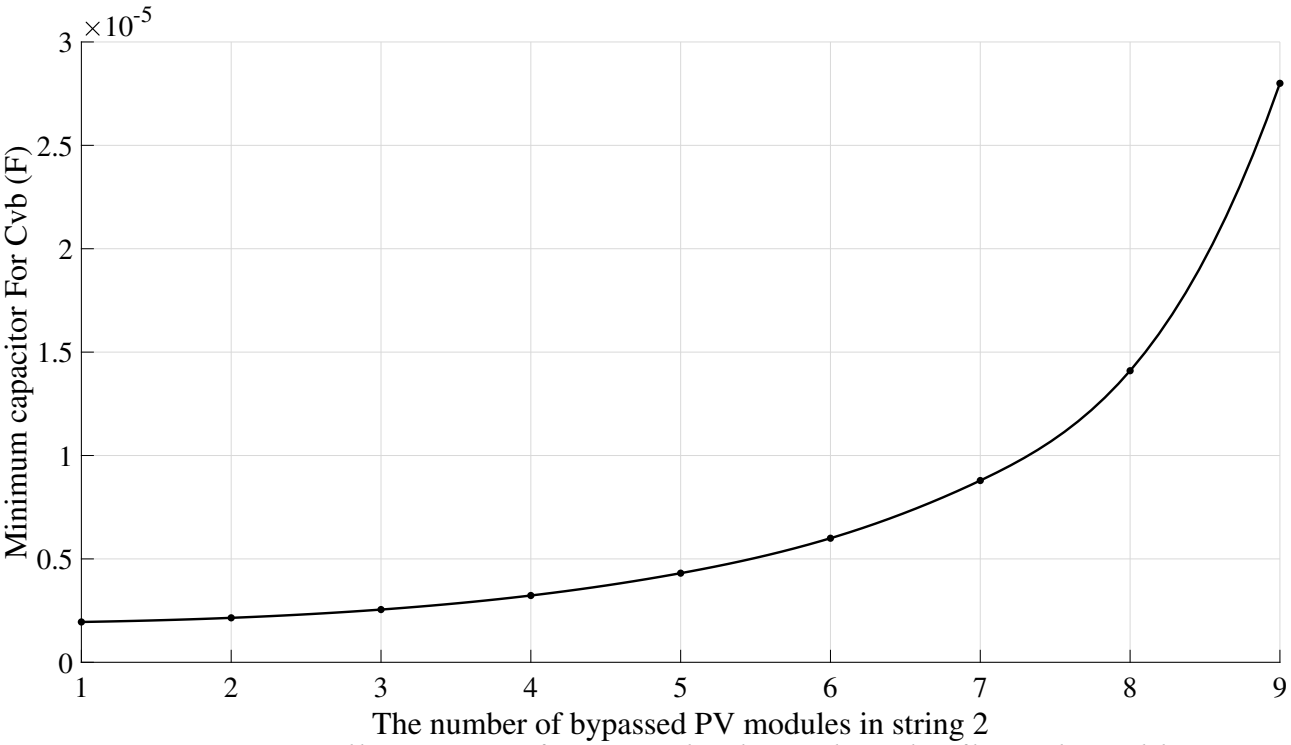


Figure 53: Minimum virtual bus requirements for capacitor when changing the number of bypassed PV modules in string 2. The virtual bus capacitor value increases as the number of bypassed PV modules in string 2 increases.

As the number of bypassed PV modules increases in string 2, the minimum capacitor for the virtual bus increases exponentially to maintain stability. The main reason is that the energy injected into the virtual bus is proportional to the square of the voltage injected into the DPP. Hence, the curve exhibits a parabolic-like behavior. When the number of bypassed PV modules increases, the voltage difference between $V_{string1}$ and $V_{string2}$ increases because the $V_{string1}$ provides constant voltage. Still, in string 2, as the number of fully functional PV modules decreases, the $V_{string2}$ continues dropping. Thus, the voltage difference is increasing. Figure 54 shows the v_{DPP_1} voltage against the number of bypassed PV mdoules change. The v_{DPP_1} represents the voltage injected into DPP from string 1; v_{DPP_1} is directly proportional to the number of bypassed modules in string 2. Based on Figure 53 and Figure 54, the minimum requirement of C_{VB} is proportional to the v_{DPP_1} square, in other words, the size of C_{VB} depends on the square of the voltage injected into the DPP.

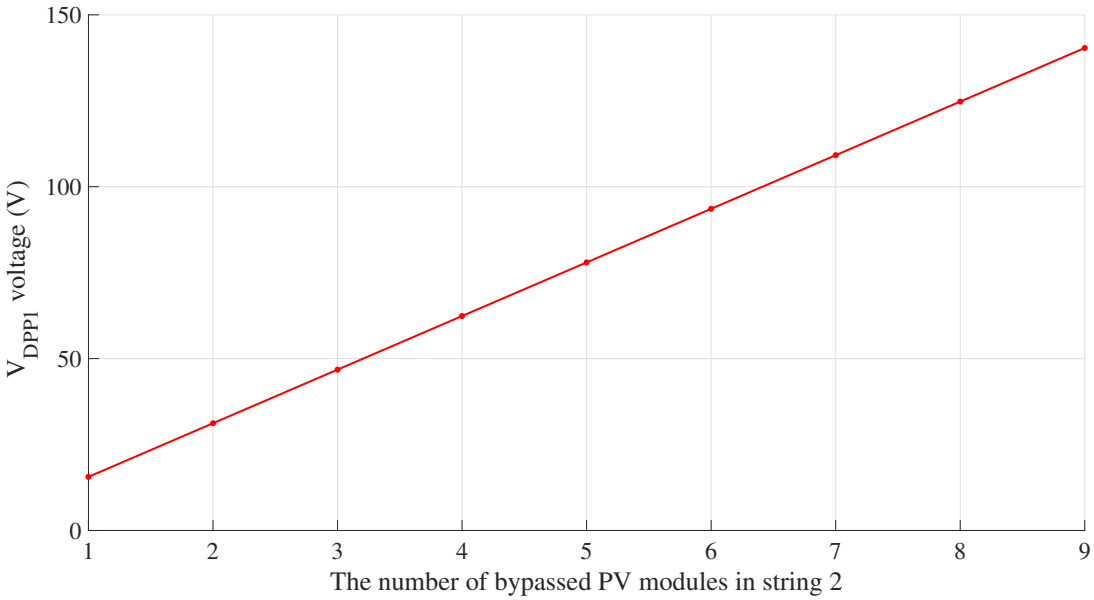


Figure 54: Voltage magnitude inject into SLC 1 converter from PV string 1

4.3 Testing passive elements in the system affect the minimum capacitor for the virtual bus

The previous section describes when the number of bypassed PV modules changes in string 2, the minimum requirement of the virtual bus capacitor also changes. However, In the 2-string PV2VB D-DPP configuration, not only the number of bypassed PV modules in string two can affect the system stability and the minimum requirement of the virtual bus capacitor, but also the passive components listed in Table 6 can affect the minimum requirement of the virtual bus capacitor.

The following simulation is the test of which passive element affects the virtual bus capacitor, and to figure out which parameter affects the minimum capacitor at the virtual bus, five elements will be investigated, which include from DPP: C_B, L_{BLC} and C_{BLC}, and from central converter: C_s and L_s.

To analyze five passive components that affect the minimum requirement of C_{VB}, the technique is to keep all the parameters the same, only changing one of the five components mentioned before, changing the value up to 10 times, or even more multiples (such as C_s component). On the other hand, the value can also be scaled down. For example, for the component B_{BLC}, the original value is 1×10^{-6}. For the sensitivity analysis, the value of B_{BLC} can be changed to 1×10^{-5} and 1×10^{-7}.

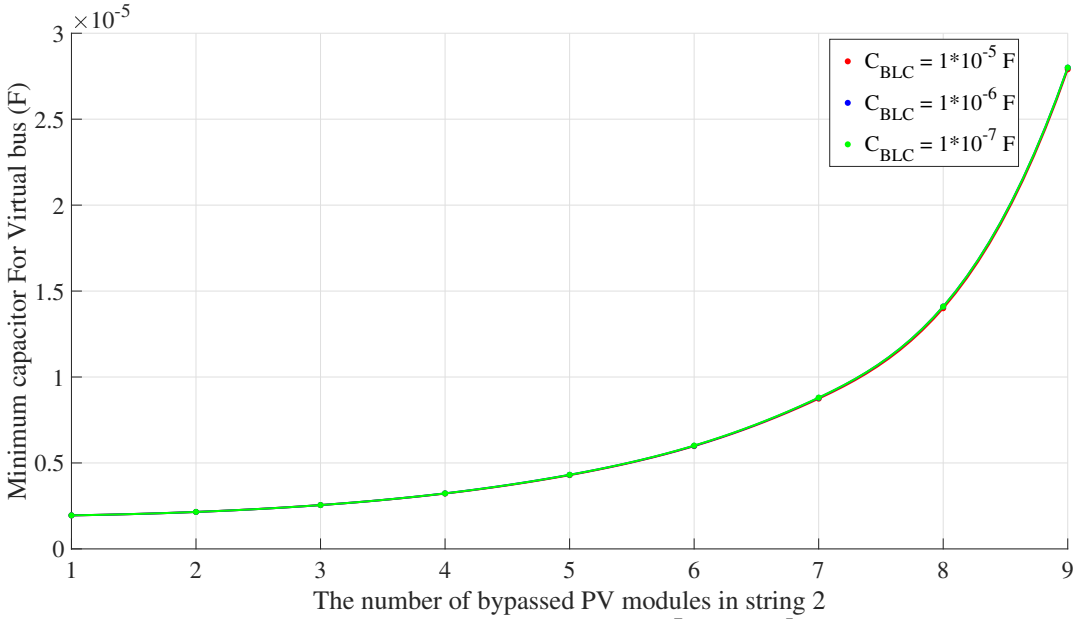


Figure 55: Effect of changing the parameterC_{BLC} change from 1×10^{-7} to 1×10^{-5} on C_{VB} minimum requirement

Figure 55 and Figure 56 show that when C_{BLC} and C_B vary up to a factor 100 times, the minimum capacitor at the virtual bus almost remains constant. The stability depends on the power compensation. The excess power first drops into SLC_1 and then passes through the virtual bus, following the power transfer to string two via SLC_2. The size of the virtual bus capacitor determines how much energy can transfer from string 1 to string 2; in other words, the bottlenecks of energy delivery are at the virtual bus. The stability of the transfer function of v_{VB} to d_s depends on the value of the virtual bus capacitor. C_{BLC} and C_B can not function for power transfer from string 1 to string 2. Therefore, there is no effect when changing the size of C_{BLC} and C_B does not affect the minimum value of C_{VB}.

However, for the inductor elements, no matter is L_s or L_{BLC}, when the size increase, the minimum capacitor for the virtual bus increase (shown in Figure 58 and Figure 59). The inductor instantaneous voltage is expressed in Equation 151; the larger the size of the inductor, the higher the instantaneous voltage, and the DPP is a voltage compensator at transient state; when the inductance is large, a slower response leads to a slower stabilization time; the inductor behavior delays the voltage compensation transition. Besides, due to the inherent characteristics of inductors, the current rate of change (rise or fall) is relatively slow compared to other components, such as capacitors. The virtual bus requires higher capacitance to remain stable when the inductance value increases.

$$v_L(t) = L\frac{di}{dt} \tag{151}$$

To study the effect of the last elements, C_s, consider the worst-case scenario (the number of bypassed PV modules in string two is equal to 9, the most considerable voltage difference between string 1 and string 2). Figure 57 shows that

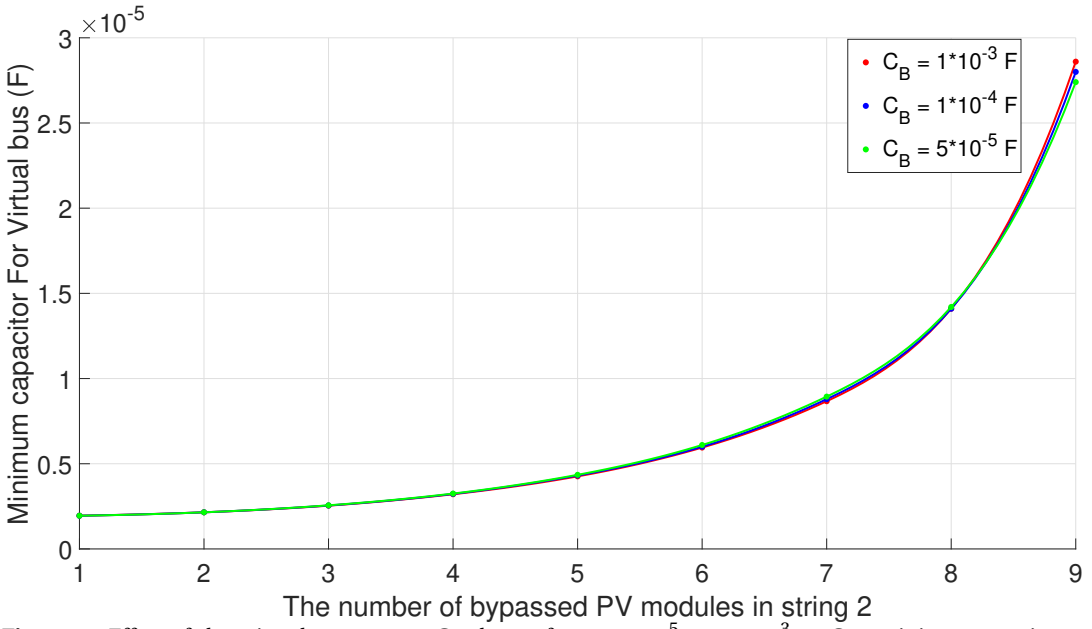


Figure 56: Effect of changing the parameterC_B change from 5×10^{-5} to 1×10^{-3} on C_{VB} minimum requirement

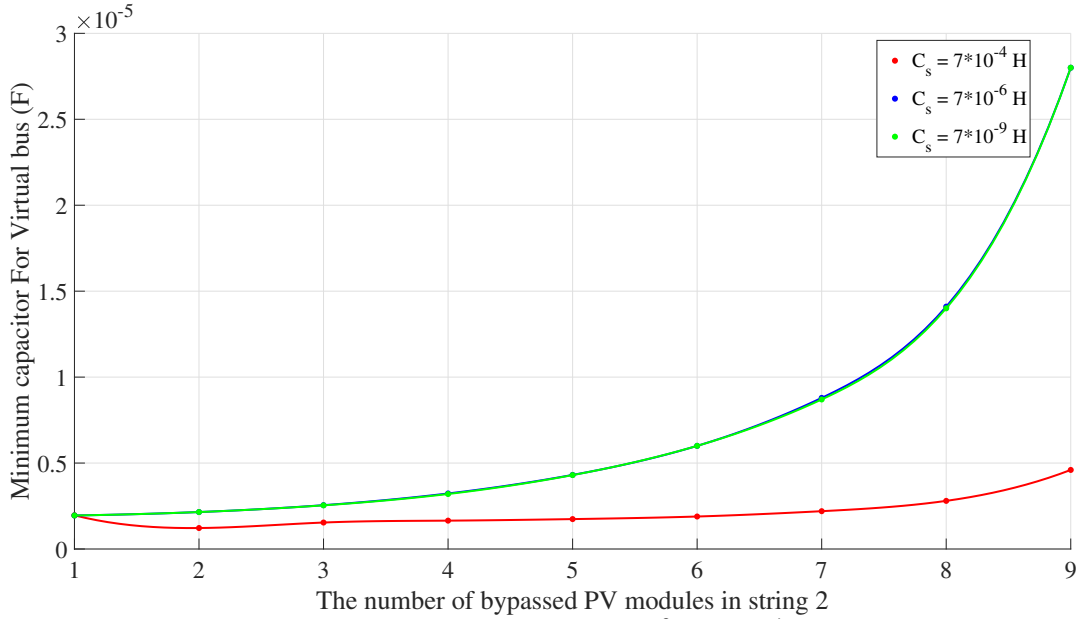


Figure 57: Effect of changing the parameterC_s change from 7×10^{-9} to 7×10^{-4} on C_{VB} minimum requirement

when C_s increases from 7×10^{-9} to 7×10^{-6}, the minimum requirement for virtual bus capacitor at worst scenario keeps constant, this is because the size of C_{VB} is much greater than C_s (10 times bigger), therefore under this condition, C_s has no effect on the stability of the transfer function. However, when C_s is bigger than C_{Vb}, it reduces the minimum requirement for a virtual bus capacitor in the worst scenario because the central converter provides an alternative path to compensate power flow from String 1 to String 2. In other words, the compensated power not only can flow via a virtual bus but also through the central converter. Still, the energy transfer via a central converter has two main disadvantages: first is a longer response time to deliver the power. The central converter is at a different hierarchy control, considering the DPP control as an inner loop and the central converter as an outer loop. In other words, the DPP control is the primary control, and the central converter is the secondary control. Therefore, when the power passes through the central converter, it takes a longer response time. Second, it leads to more complicated control for the power flow because central converters typically require complex control algorithms to manage power flow and voltage regulation. So, when unexpected or additional power flows through the central converter, the control algorithms become more complex.

In summary, changing the capacitor in C_{BLC} and C_B has no effect on the stability of the transfer function between v_{VB}

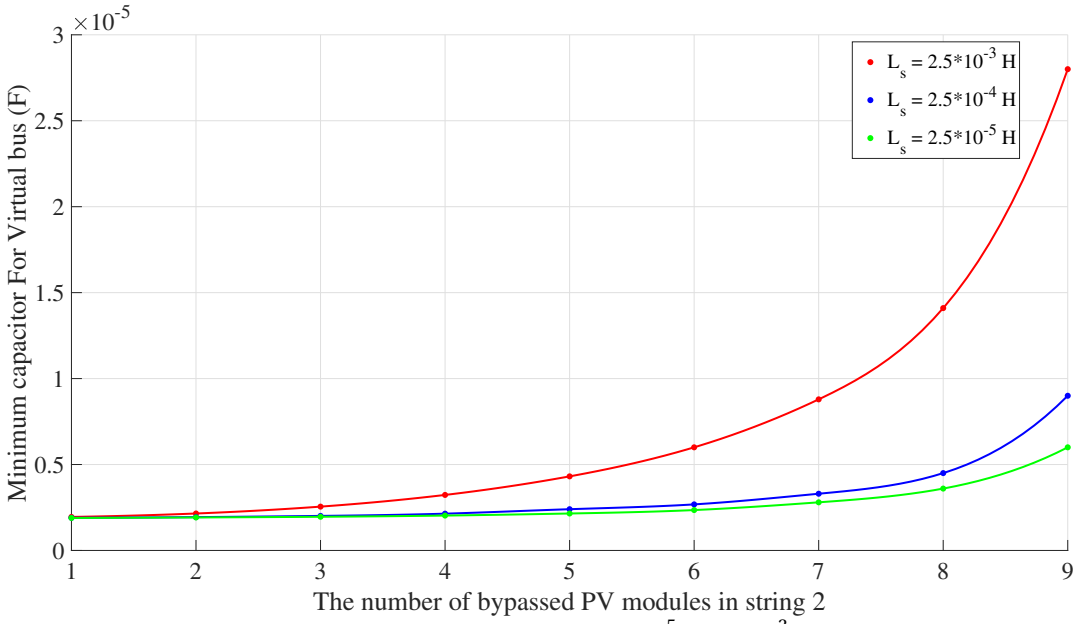


Figure 58: Effect of changing the parameterL_s change from 2.5×10^{-5} to 7×10^{-3} on C_{VB} minimum requirement

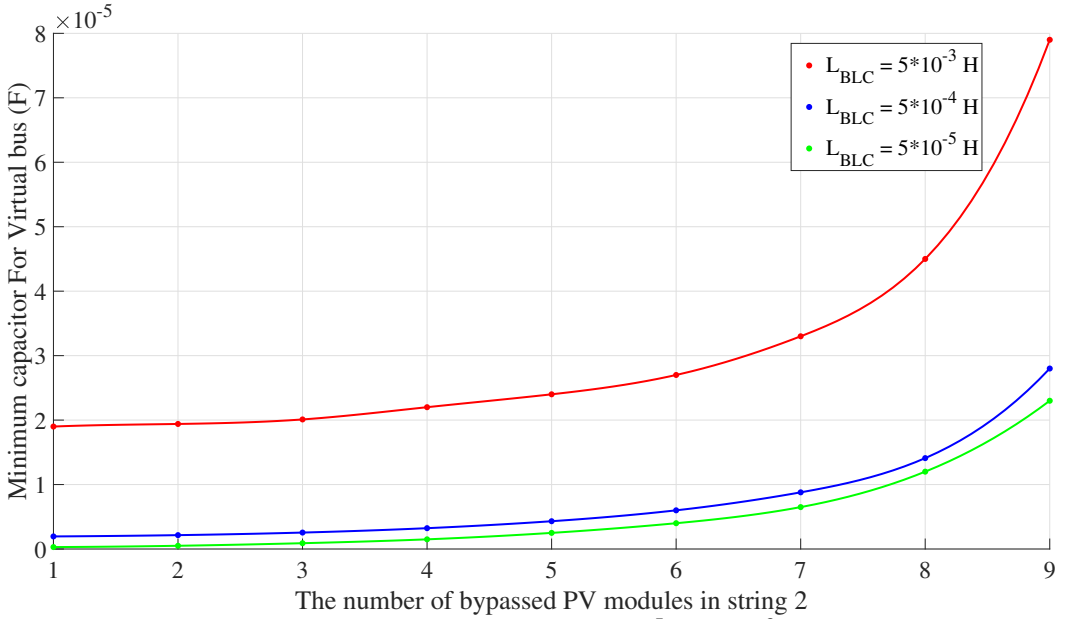


Figure 59: Effect of changing the parameterL_{BLC} change from 5×10^{-5} to 5×10^{-3} on C_{VB} minimum requirement

and d_s. Still, the inductor does affect the stability of the transfer function between v_{VB} and d_s. Lastly, changing the central capacitor may affect the stability of the transfer function.

In another simulation, the number of PV modules per string is doubled. Specifically, PV modules are put in parallel. So, for string 1, the total number of PV modules is up to 20, and the string voltage is still the same, but the string current is doubled. Figure 60 shows the minimum capacitor for the virtual bus against the 10-module string (series) and 20-module (series/parallel).
When a PV string contains 20 PV modules, the minimum capacitor for the virtual bus is four times higher than a PV string containing 10 PV modules because the power exchange in the virtual bus is proportional to the current. Therefore, the minimum capacitor for the virtual bus is four times higher than the original one. In addition, the DPP can not handle the worst-case scenario (9 bypassed PV modules in string two) due to the power rating of the DAB not being able to handle the power when it is two times bigger. As a recommendation, it is not worth installing double the PV modules in parallel in the string rather than expanding for another string by attaching a new DPP.

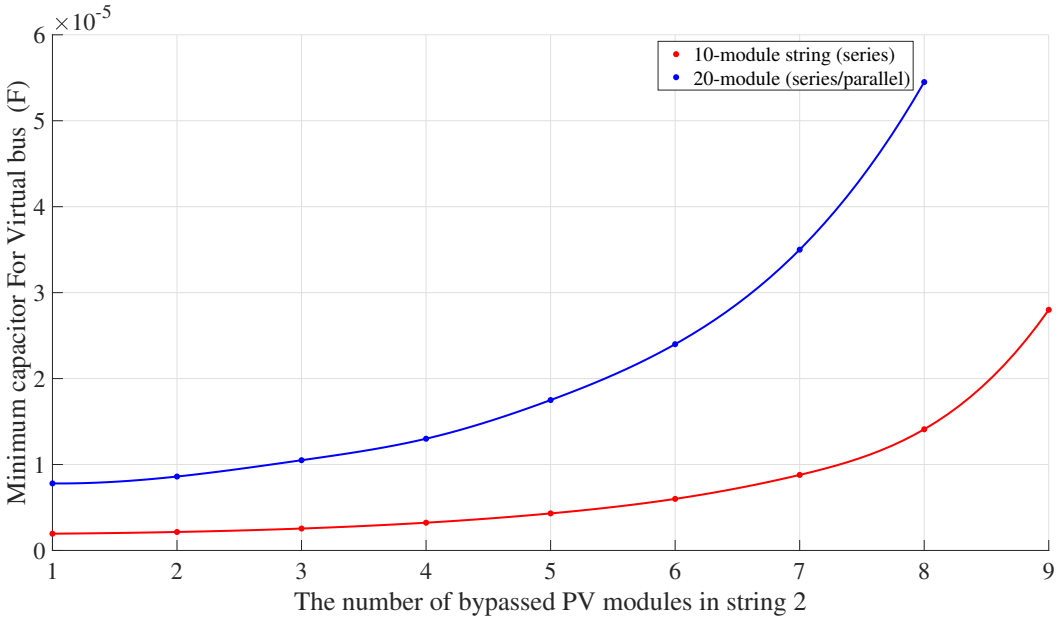


Figure 60: Minimum C_{VB} against the number of bypassed PV modules in string 2 in two scenarios: 10-module string (series) and 20-module (series/parallel)

4.4 Stability margin analysis

One of the methods to find optimal virtual bus capacitance is to analyze the stability margin of the transfer function to determine which pole is close to the right-hand side of the complex plane graph. In other words, In a stable system, all the poles should have negative real parts, which means they should be located on the left-hand side of the complex plane; to determine which pole is closer to the imaginary axis, the pole with the real part closest to zero (but still negative) is closer to the imaginary axis. that pole will determine the whole transfer function stability margin; these poles determine the primary dynamics of the system and play a crucial role in the formation of the overall response of the system. The pole closest to the imaginary axis is called the dominant pole. These poles typically control the stabilization time, overshoot, and overall system stability. Figure 61 shows how the dominant pole changes when the virtual bus capacitance varies from $28\mu F$ to $1mF$. Besides, Figure 62 shows the extension value of the virtual bus capacitor from $1mF$ to $0.1F$ corresponding to the pole that is closest to the imaginary axis; and in Table 7 shows the exact point how far the dominant pole is away the imaginary axis from the value from $28\mu F$ to $100F$.

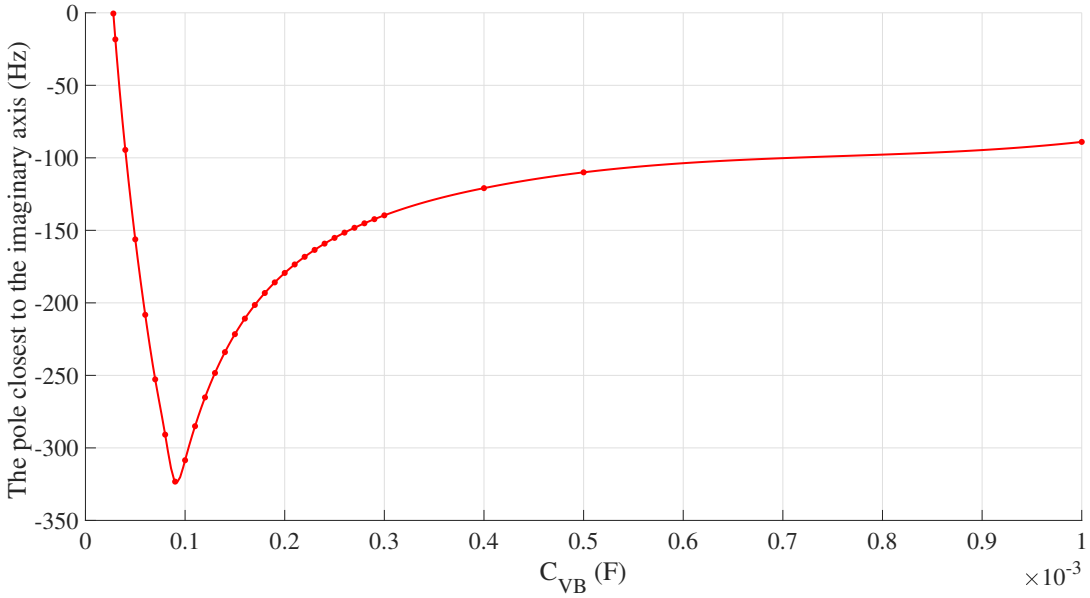


Figure 61: The dominant pole position against C_{VB} changes from $28\mu F$ to $1mF$. Note that when C_{VB} is $28\mu F$, the pole closest to the imaginary axis (-0.5002)

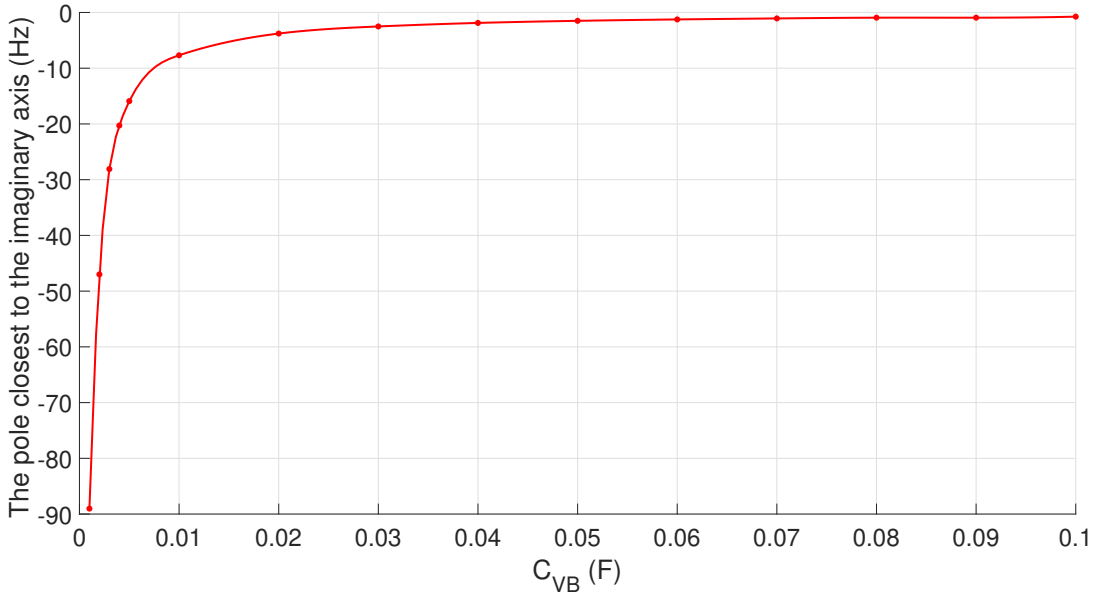


Figure 62: The dominant pole position against C_{VB} changes from $1mF$ to $100mF$

Table 7: Dominant pole position (real part) changes when the virtual bus capacitor changes from 1×10^{-3} to 100 F

C_{VB} value (F)	Real part of the dominant pole (Hz)
30×10^{-5}	-18.3066
50×10^{-5}	-156.2067
70×10^{-5}	-252.745
90×10^{-5}	-323.2576
1×10^{-4}	-308.51
1×10^{-3}	-89.0206
1×10^{-2}	-7.6814
1×10^{-1}	-0.7475
1×10^{0}	-0.0746
1×10^{1}	-0.0075
1×10^{2}	-0.0007

Based on Figure 61 and Table 7, As the virtual bus capacitor increases from 28μ F to 90μF, the dominant pole is moving farther away from the imaginary axis, in other words, it has a higher stability margin which increases the stability of the system. Because the stability margin of a system is a measure of how close the system is to becoming unstable. A higher stability margin means that the system is less likely to become unstable. The distance between a pole and the imaginary axis is a measure of the system's stability margin. The further away a pole is from the imaginary axis, the higher the system's stability margin [50]. However, when the virtual bus capacitor is increased from 90 μF, The dominant pole is shifted back toward the imaginary axis. To explain this dominant pole-shifting behavior, two aspects need to be taken into account. The first aspect is called robustness against noise and fluctuations. As the value of a capacitor increases, so does its ability to store charge. Larger capacitors are better at smoothing out voltage fluctuations and filtering out noise than smaller capacitors[51]. This is because a capacitor can act as an energy storage, helping the circuit maintain a more stable voltage level.

The second aspect is called performance stability. It deals with the effect of capacitors on the time constant and frequency response of a circuit. As the capacitance value increases, the time constant of the circuit changes. In some cases, a significant increase in capacitance value can result in a longer time constant, which affects the response time of the circuit and can lead to performance problems[51]. A power supply with too much capacitance can become unstable and start to oscillate. This can cause damage to the power supply and other components in the circuit [52]. From the virtual bus capacitor range from 28μF to 90 μF, the stability is determined by robustness against noise and fluctuations factors; after 90 μF, excessively large capacitors may cause unwanted delays in the output signal. This may reduce the overall stability of the circuit and affect its intended operation. Therefore, it reduces the stability margin. while larger capacitance improves robustness and noise filtering, there is a limit to the increase in capacitance beyond which the performance and stability of the circuit can be adversely affected.

In practice, the situation becomes more complicated because it has some internal resistance called equivalent series resistance (ESR). Using large capacitors leads to increased power losses due to high power processing. Based on Table 7, 90 μF value of the capacitor is the optimal choice for the simulated system. In the context of the specific system we are simulating, it's important to address the issue of ripple current in the PV string. In this case, consider the current ripple from the PV string; 8.69A of ripple current for the capacitor is required. In the electronic market, aluminum electrolytic capacitors provide high-quality capacitors in terms of the number of charging cycles. Table 8 provide the detail of capacitor parameter. A single capacitor can handle 0.87A ripple current. Therefore 12 capacitors connected in parallel are required to deal with the current ripple. The total capacitor in the virtual bus is 1.2 mF. Based on Table 8, 1.2 mF is the optimal choice because it fulfills two conditions: one handles ripple current, and second, the dominant pole to the imaginary axis is furthest.

Table 8: Aluminium Electrolytic Capacitors data sheet [53]

Voltage	value Cap (µF)	Catalog Part Number	Ripple (A)
450 Vdc @ 105°C	100	MAL225957101E3	0.87

4.5 Root locus and PI controller introduction

4.5.1 PI conrtoller

The PI controller is one of the classic feedback controls. The full name is proportional-integral controller, which can be split into two parts: proportional control and integral control. Equation 152 and Equation 153 show the PI con-

troller in the time domain and frequency domain form, respectively. The proportional term of the controller produces an output proportional to the current error, and in both equations, e stands for the current error. It applies a control strength proportional to the deviation between the set and actual values. The proportional gain determines the strength of this control action[54].

On the other hand, the controller's integration term accounts for the accumulated error over a period of time. It integrates the error signal and continuously sums up past errors. The integral action helps to eliminate steady-state errors and improves the system's ability to track the reference point. The integration gain determines the speed of response and the ability to eliminate steady-state errors[54].

Figure 63 shows the block diagram of the PI controller implemented on the P-DPP PV2VB system in a closed loop system, Where G(s) represents the transfer function and C(s) represent the controller. Since there are two different types of converters that need to be controlled, G(s) can represent the transfer function of the central converter or the transfer function of the DPP. In a two-string system, based on Equation 147 and Equation 148, there are nine outputs and 5 inputs. By the combination of the input and output, there are up to 54 possible transfer functions that can be set up. However, the transfer function between v_{VB} and d_s represents the transfer function of the central converter, and the transfer function between v_{dpp_1} and d_1 represents the transfer function of DPP. Both of these two transfer functions were investigated to design the PI controller for the central converter and DPP, respectively. Table 3 provide the PV modules parameter, in Table 4 and Table 5 provide how to determine the state variables and input variables base on Passive element, transformer parameter, and voltage output provides in Table 6.

$$u(t) = K_{\mathrm{p}} e(t) + K_{\mathrm{i}} \int_0^t e(\tau)\mathrm{d}\tau \tag{152}$$

$$u(s) = K_p e(s) + \frac{K_i}{s} e(s) \tag{153}$$

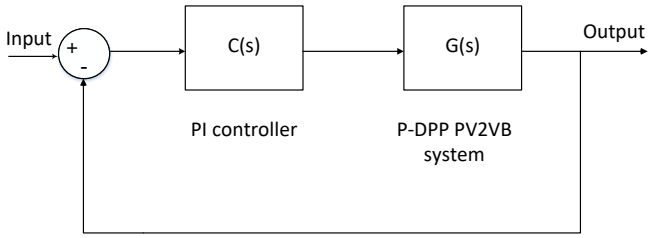


Figure 63: Block diagram of PI, G(s) can represent the transfer function of the central converter or the transfer function of the DPP. C(s) represents the PI controller implemented on the central converter or DPP.

4.5.2 Root locus

The root locus is a graphical method used to analyze and understand the behavior of closed-loop control systems in control systems engineering. It provides insight into how the poles of a system vary with a particular parameter (usually the system gain). The term "root" refers to the root of the system's characteristic equation, which corresponds to the pole of the transfer function.

In control systems, the goal is to design a closed-loop system with desired stability and performance characteristics. Root points help engineers determine how the closed-loop poles move in the complex plane as the system gains changes. This, in turn, allows them to evaluate and tune the stability, transient response, and steady-state response of the system. The following paragraph shows how the root locus diagram is constructed:
Refer to Figure 63, the transfer function of the close loop equation is expressed in Equation 154; the denominator is determined as the stability and transient response of the closed-loop transfer function, so set the denominator of the closed-loop transfer function equal to zero, the equation is expressed in Equation 155. The roots of the equation are called poles. If any of the poles of the system have a real part greater than 0, then the system is unstable. On the other hand, the nominator affects system dynamics, but they do not directly influence stability. The roots of the equation of nominator is called zero.

$$T(s) = \frac{C(s)G(s)}{1 + C(s)G(s)} \tag{154}$$

$$1 + K \times C(s)G(s) = 0 \tag{155}$$

The root locus diagram is constructed by tracing the path of the closed-loop poles as the gain (K) is varied from 0 to infinity, where K refers to the coefficient factor in Equation 155. In general, as the gain increases, the poles move towards the right-hand side of the complex plane (less negative real value). When the poles cross the imaginary axis and enter the right-half plane (RHP), the system becomes unstable. The reason behind this is that higher gains can introduce more positive feedback, making the system oscillate or diverge instead of converging to the desired reference point. Therefore, proper PI controller parameters need careful tuning based on the system's characteristics and desired performance. Proper tuning ensures that the system is stable, responds well to disturbances, and meets the design requirements.

To understand the root locus plot, it is better to understand the mechanics of how to draw the root locus. By the six following steps, a root locus plot can be obtained.
1- Find the number of poles, zeroes, number of branches, etc., from the combined PI compensator and original transfer functions, which is T(s) in Equation 154. Then, draw the plot that shows the poles and zeroes marked on it [55].
2- Calculate the angle of asymptotes and draw a separate sketch.
3- Find the centroid and draw a separate sketch.
4- Find the breakaway points. These points can also be in the form of complex numbers. We can use the angle condition to verify such points in the complex form. Calculate the intersection points of the root locus with the imaginary axis (or y-axis).
5-Calculate the angle of arrival and departure if applicable.
6-Draw the final sketch of the root locus by combining all the above sketches.
Here is an example of how to draw a root locus plot. Assume the transfer function T(s) is expressed in Equation 156. The poles can be found on the denominator. In this case, the denominator is the order of the third formula. Hence, there are three poles that exist: 0, -5, and -10. There are no zeros in the equation because, on the nominator, there is just a constant number one. After finding all the poles and zeros, the branches can be calculated on the number of poles minus the number of zeros. In this case, there are three branches that exist, then draw three poles on the diagram. The next step is to find the angle of asymptotes; the general calculations are shown in Equation 157. By calculation, the angles of asymptotes are 60, 180, and 300 degrees. The following step is to find the centroid based on Equation 158. Thus, in this example, the centroid of the root locus is at -5 on the real axis. For the breakaway point, more information can be found on [55]. After combining all the steps above, The root locus diagram is shown inFigure 64.

$$T(s) = \frac{K \times 1}{s(s+5)(s+10)} \tag{156}$$

$$\measuredangle = (2q+1)\frac{180}{P-Z} \tag{157}$$

Where q indicates branches sequence, in this example, branches sequence count from 0-2. P and Z represent the number of poles and zeros, respectively.

$$\sigma = \frac{\sum RP - \sum RZ}{P-Z} \tag{158}$$

Where RP represents the real part of poles position, and RP represents the real part of zeros position.

4.6 Design PI controller for central converter and DPP with C_{VB} 1.2 mF

4.6.1 transfer function between v_{VB} and d_s

In this simulation, the value of C_{Vb} is equal to $1.2mF$. Figure 65 show the root locus of G(s); as the proportional gain increases (K_p), the entire root position shifts from the open loop pole to the open loop zero. The region that needs to be investigated is close to the imaginary axis area. If the gain increases to a certain point, the pole real parts will be close to zero, and the gain margin becomes zero. If the gain continues to increase, the pole will enter the right-hand side plane, indicating that the system is unstable. In Figure 66 shows the gain that can be achieved at the Imaginary axis. In addition, Table 9 and Table 10 show the precise pole and zero position. The proportional gain is approximately 3.07. Knowing such a gain value, a proper PI controller can be designed.
Introduce Sisotool tool
Sisotool tool is a graphic user interface (GUI) tool in MATLAB's Control System Toolbox. It is used for the analysis and design of single-input, single-output (SISO) control systems. It is a powerful tool that allows engineers and researchers to interactively design and tune control systems using various graphical techniques and simplify the control system design.

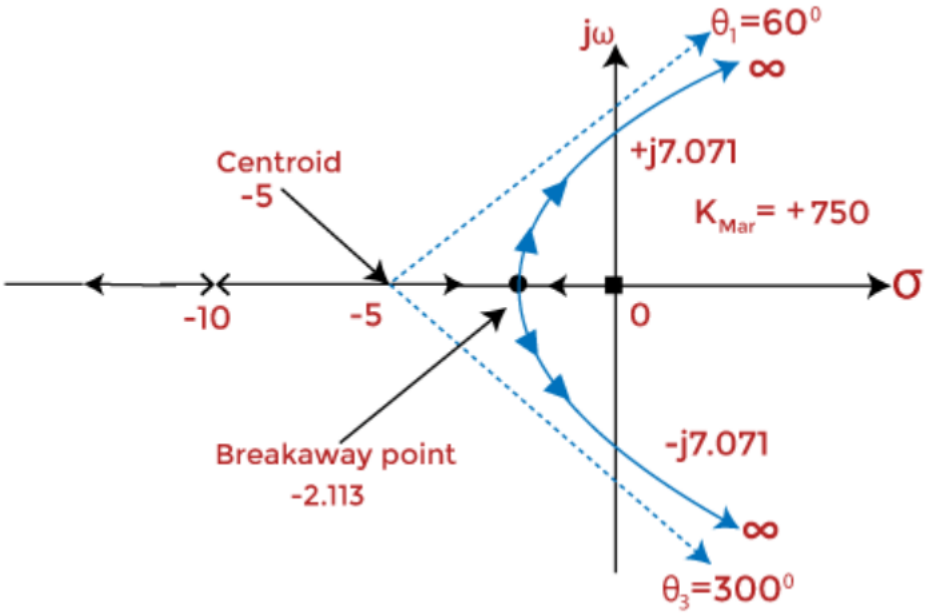


Figure 64: Example of root locus diagram[55]

Real	Imaginary
-3.1340×10^5	0.0000
-1.3903×10^4	4.123×10^4
-1.3903×10^4	-4.123×10^4
-3.8730×10^3	1.8229×10^4
-3.8730×10^3	-1.8229×10^4
-5.7016×10^2	1.0757×10^3
-5.7016×10^2	-1.0757×10^3
-85.62397	37.66224
-85.623970	-37.66224

Table 9: 10 poles exact position located on Figure 65

Real	Imaginary
8.7593×10^4	0.0000
-1.7277×10^4	4.1297×10^4
-1.7277×10^4	-4.1297×10^4
2.2245×10^4	0.0000
0.0558×10^4	0.0000
-0.0171×10^4	0.0000

Table 10: 6 zeros exact position located on Figure 65

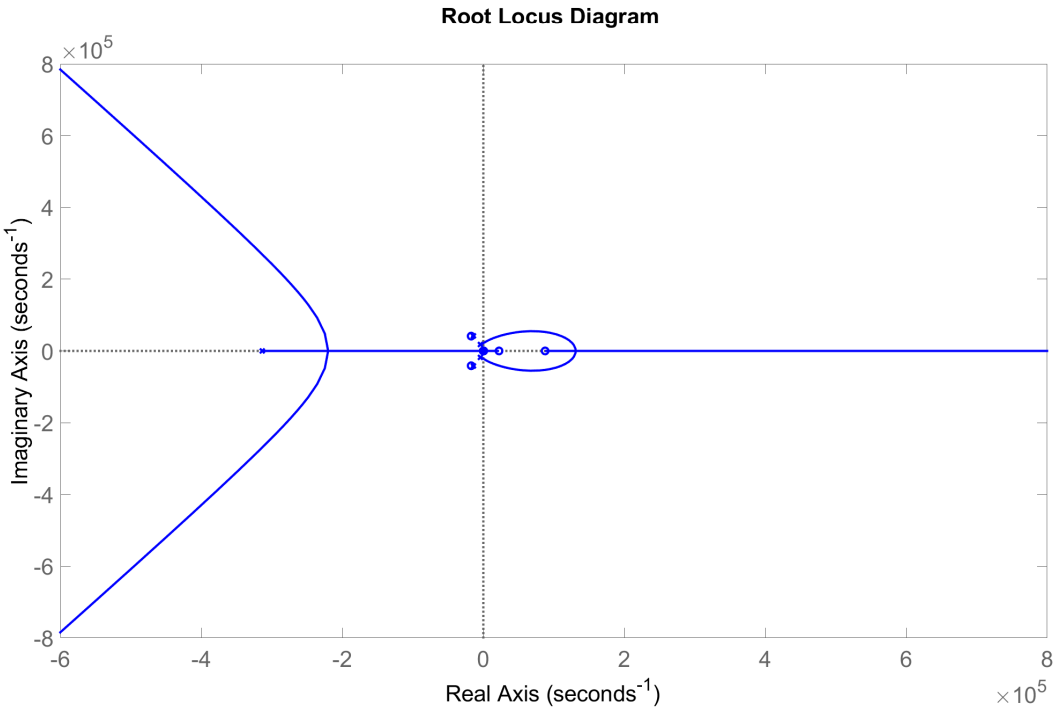


Figure 65: Root locus diagram of transfer function v_{VB} and d_s with 1.2 mF C_{Vb}. Note that the "x" and "o" symbols represent poles and zeros in function v_{VB} and d_s, respectively.

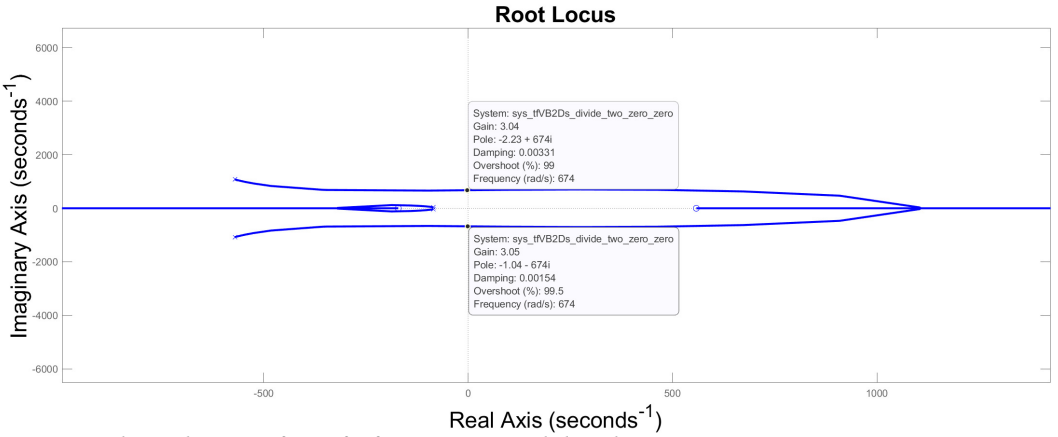


Figure 66: Root locus diagram of transfer function v_{VB} and d_s with 1.2 mF C_{Vb} (zoom in version in imaginary axis region)

The procedures using Sistool to design the PI controller first insert the system transfer function into the Sisotool tool interface. The code is called sisotool (x), and x represents the system transfer function. The transfer function between v_{VB} and d_s is applied on sisotool. Then open the PID tuning interface, Figure 67 shows the PID tuning interface, select controller type to PI, the next step is to fine-tune the PI controller value (K_P and K_i) via the interface based on response time (fast or slow) and transient behavior (aggressive and robustness). To determine the PI controller parameter, there are three main factors that need to be considered: phase margin, gain margin, and settling time. In general, a suitable PI controller will have a gain margin of at least 10 dB and a phase margin of at least 45 degrees. For the settling time of less than 5 seconds because the transfer function between v_{VB} and d_s is the outer loop loop control. Thus, compared with the inner loop control, the transient response speed of the outer loop control is slower. Besides, the settling time is the time it takes for the system's output to stabilize within a desired tolerance (10%error to the reference point) after a disturbance or setpoint change.Equation 159 shows the PI controller parameter, and Figure 68, Figure 69 and Figure 70 show the bode plot with gain margin and bode of a plot of phase margin and transient response respectively.

Note that in the Sisotool toolbox bode plot, here is the symbol meaning.

x: Frequency at which the magnitude of the open-loop transfer function (C(s)×G(s)) equals 1 (0 dB).
Blue circle: Frequency at which the phase margin is 0 degrees.
Red circle: Point where the open-loop gain crosses the -180 degrees phase line.
Orange circle: Gain crossover frequency.

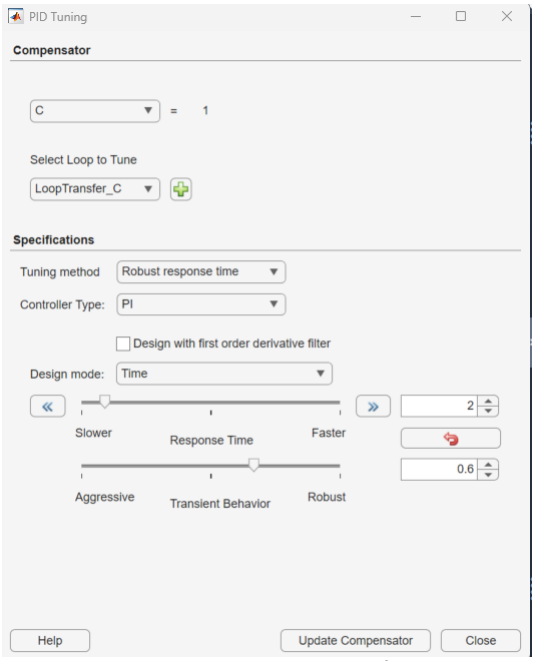


Figure 67: PID tuning interface

$$C(s) = 5 \times \frac{1 + 0.1 \times s}{s} \tag{159}$$

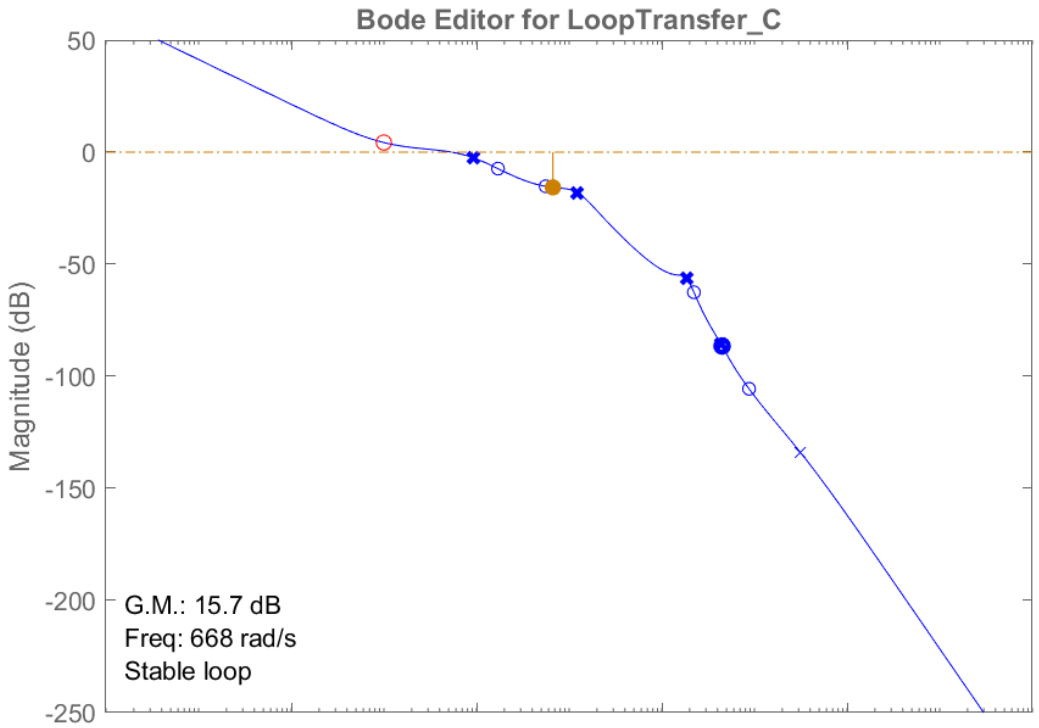


Figure 68: Bode plot of gain margin with combined PI controller(Equation 159) and the transfer function of v_{VB} and d_s.

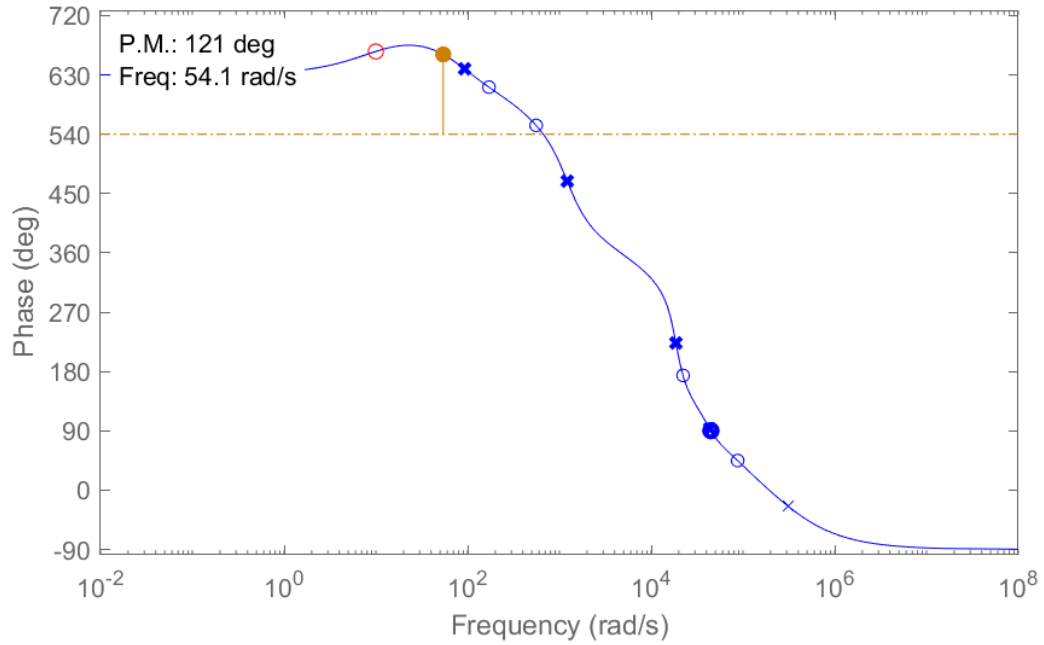


Figure 69: Bode plot of phase margin with combined PI controller(Equation 159) and the transfer function of v_{VB} and d_s

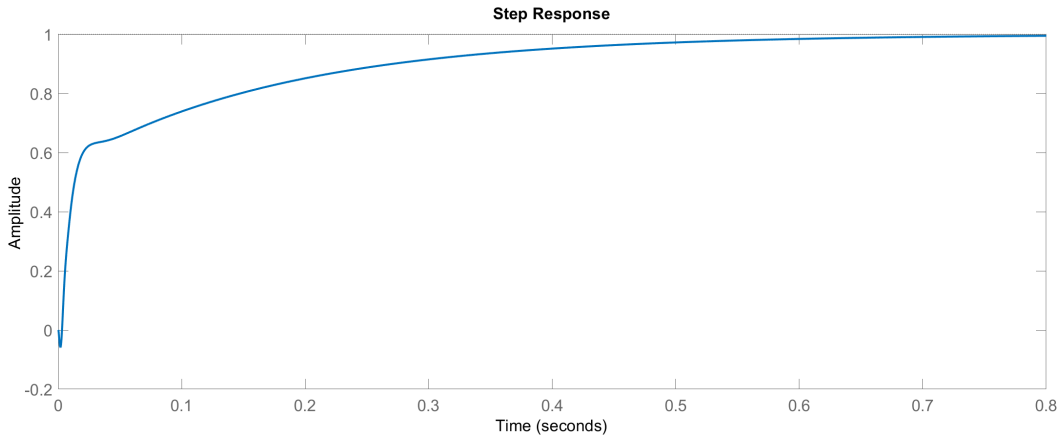


Figure 70: Step response graph for central converter

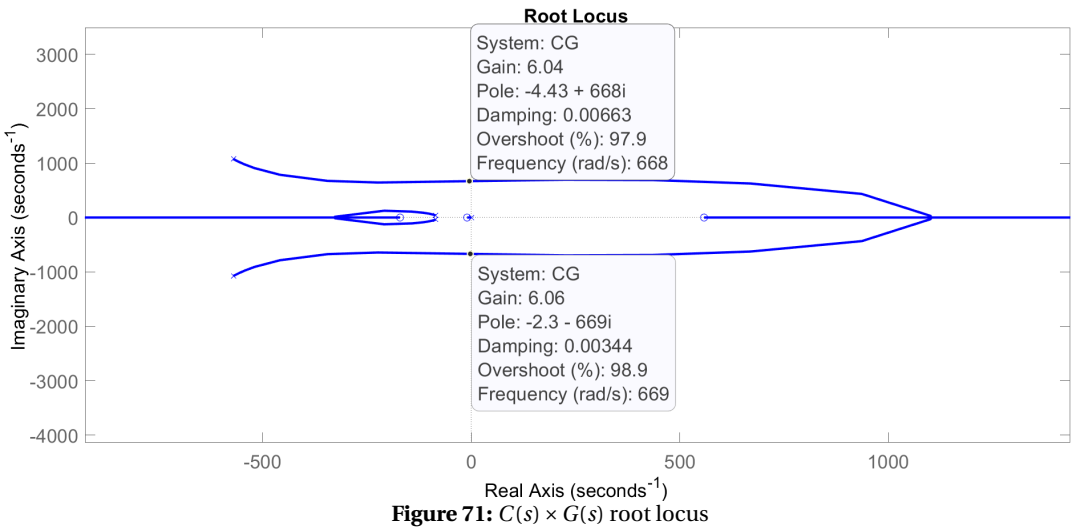


Figure 71: $C(s) \times G(s)$ root locus

4.6.2 Investigative how changes of K_i and K_p affect PM, GM, and settling time.

Table 11: PI controller performance when we keep K_p constant and change K_i

K_p	K_i	GM	PM	Settling time (s)
0.5	1	15.7	131	3
0.5	5	15.7	121	0.8
0.5	10	15.7	109	0.4
0.5	20	15.6	89.2	0.2
0.5	40	15.4	64.7	0.1
0.5	80	14.8	38.6	0.1

The first simulation is to keep K_p constant and vary the K_i parameter, Table 11 shows the simulation result when K_i is changing and K_p remains constant. The red data represents Equation 159 control parameter setting.

When the value of K_i decreases from 5 to 1, the phase margin increases from 121 to 131 because, with lower K_i values, the -90 degree phase shift due to integral action is reduced, leading to a slightly higher phase margin. For the gain margin, as the value of K_i decreases, the gain margin is slightly increasing. The smaller the value of K_i, the smaller the effect of the integration pole on the root position, and the larger the gain margin. The robustness of the system to gain variations and disturbances is also increased. And last, the time to reach steady-state increases from 0.8s to 3s. Decreasing K_i decreases the integrating action, resulting in a slower response to steady-state errors. The system takes longer to reach the reference point, resulting in a longer settling time.

On the other hand, an increase in K_i has several effects in terms of phase margin and settling time. In this simulation, the value of K_i increases up to 80 (20 times higher than the original value). For the phase margin, when the value of K_i increases to 80, the phase margin decreases significantly to 38.6 degrees, which does not satisfy the design requirement. Hence, increasing K_i will decrease the phase margin. The integral action introduces a -90-degree phase shift at low frequencies, which can reduce the gain margin slightly. As the value of K_i increases, the gain margin is decreasing. As K_i increases, the role of the integration pole becomes more prominent, causing the dominant pole to move closer to the imaginary axis. This movement decreases the gain margin, making the system more sensitive to gain changes and decreasing the stability margin. Lastly, when the K_i increases, the settling time reduces to 0.1s. The main reason is that increasing K_i will enhance the controller's integral action, resulting in a more positive response to steady-state errors. The integral action will cause the system to reach the reference point faster. However, refer to Table 11, when K_i changes from 40 to 80, the settling time remains constant. The reason behind this is there may be practical limits to how much the integral action can affect the system; further increases in K_i won't have much impact on the transient response because the controller is already working at its limits.

Table 12: PI controller performance when we keep K_i constant and change K_p

K_p	K_i	GM	PM	Settling time (s)
0.1	5	29.6	92.3	0.5
0.25	5	21.7	112	0.78
0.5	5	15.7	121	0.8
1	5	9.69	80.1	1
1.25	5	7.75	70.3	1.1
1.65	5	5.25	57.6	1.2
2.5	5	1.73	32.6	0.09 (can not cancel the error)

The second simulation is to let K_i remain constant and vary the K_p, Table 12 shows the result when K_p is changing, the PM and K_i remain constant. The red data represents Equation 159 control parameter setting.

The first conducting simulation is the decreased value of K_p down to 0.1. When decreasing K_p slightly decreases the phase margin, the smaller K_p is, the smaller the phase lag is at higher frequencies, resulting in a slight decrease in phase margin. An increase in phase margin enhances the stability of the system against phase shifts. For the gain margin, as K_p reduces, the gain margin increases. when K_p is reduced, K_p is a multiplier that determines the strength of the controller's response to an error signal. A lower K_p means that the controller will respond less aggressively to errors. Thus, with the same K_i parameter, it has a higher gain margin. Lastly, decreasing K_p reduces the control effort, resulting in a faster system response to the error. The smaller K_p is, the less sensitive the control action is to the error, resulting in a slower response. As a result, the settling time increases, and the system takes longer to reach the set

point.

On the other hand, increasing K_p to 2.5 (5 times higher than the original one; Note that if the increase is more than 6 times, the system is unstable) will lead to the following results: First, it can reduce phase margin (reduce up to 32.6 degrees), A larger K_p may introduce more phase lag at higher frequencies, thus reducing the phase margin. A reduced phase margin can make the system more sensitive to phase shifts, leading to potential instability. Second, It can reduce the gain margin (reduce up to 1.73). The larger K_p is, the more sensitive the system is to gain changes, which may cause the dominant pole to move closer to the imaginary axis. A decrease in the gain margin reduces the stability margin and brings the system closer to an unstable state. Lastly, Increasing K_p will result in more aggressive control action, causing the system to respond faster to the error. The greater K_p, the greater the control effort, proportional to the error, resulting in a faster response. As a result, the settling time will be shorter, and the system will reach the set point faster. however, The larger the K_p value, the more responsive the control system will be to any errors. If the system encounters sudden changes or disturbances, larger corrections will be made, which may result in the output exceeding the expected value. This phenomenon is called overshoot, which results in a large oscillation and takes a longer time to reach steady state. Thus, in the system under analysis, a higher value of K_p takes a longer time to reach a steady state.

In general. When tuning a PI controller, it is critical to find the proper balance between proportional and integral action to achieve the desired closed-loop performance while maintaining stability and robustness. Careful consideration should be given to the control system requirements and performance objectives during the tuning process. By investigating the K_p and K_i relationship with PM, GM, and settling time, consider the criteria mentioned before, in Equation 159 shows one of the optimal PI control parameters, it fulfills all the requirements, and it has sustained high PM and relatively low settling time.

4.6.3 Transfer function between v_{B1} and ϕ_1 analysis

The next investigation is v_{B1} to ϕ_1 transfer function, Figure 72 shows the root locus of v_{B1} to ϕ_1 transfer function. It is clear that there is no line across the imaginary axis, which is proven in Figure 73 the zoom-in area of the imaginary axis region. In other words, the gain can increase to infinite, and the system still remains stable. However, the PI controller still needs to fine-tune the parameter, the reason being that PM and settling time are the key factors that need to be considered. Compared with the previous PI controller operating at the central converter, this PI controller operates at string 1 DPP converter, and it has different criteria for the settling time it requires in the millisecond range but the phase margin criteria is the same (above 45 degrees). There are two main reasons why the settling time is required in the millisecond range. First, the PI control operated at the DPP converter is considered the inner loop control, and the PI control operated at the central converter is considered the outer loop control. It's common for the inner loop to require a quicker response compared to the outer loop. This concept is known as "nested control loops." The second reason is the operation frequency of DAB operates at hundreds of kHz. Thus, fast correction of disturbances and deviations helps prevent issues like overshoot and oscillations, which can be detrimental to the system's performance and stability. By using the PI controller interface, tuning response time, and transient behavior, reasonable PM and settling time can be achieved. To satisfy the PM above 45 degrees and settling time in the millisecond range, in Equation 160 shows the PI controller parameter for v_{B1} to ϕ_1 transfer function. In addition, Table 13 shows the data of GM, PM, and settling time, meanwhile Figure 74, Figure 75 and Figure 76 shows bode diagrams with GM and PM and settling time for Transfer function v_{B1} to ϕ_1 with PI controller in close loop.

$$C(s) = 10 \times \frac{1 + 0.01 \times s}{s} \tag{160}$$

Table 13: PI controller integral with transfer function, data of GM, PM, and settling time

GM	PM	settling time
inf	93.9	1ms

In summary, in this chapter, a string model of PV2VB P-DPP was established. Then, use the model to simulate the scenario when the string voltage difference between two strings is the minimum capacitor requirement for the virtual bus. In addition, using the method holds all other variables constant and only changes a single variable to figure out which passive elements are the implications on the minimum capacitor requirement. The final step is the PI controller implementation on the central converter and DPP converter. Note that the central converter control is more important than the DPP converter control because it controls the overall system performance. The DPP converter control is used to control the performance of a single PV string, but it is not directly responsible for the overall system performance.

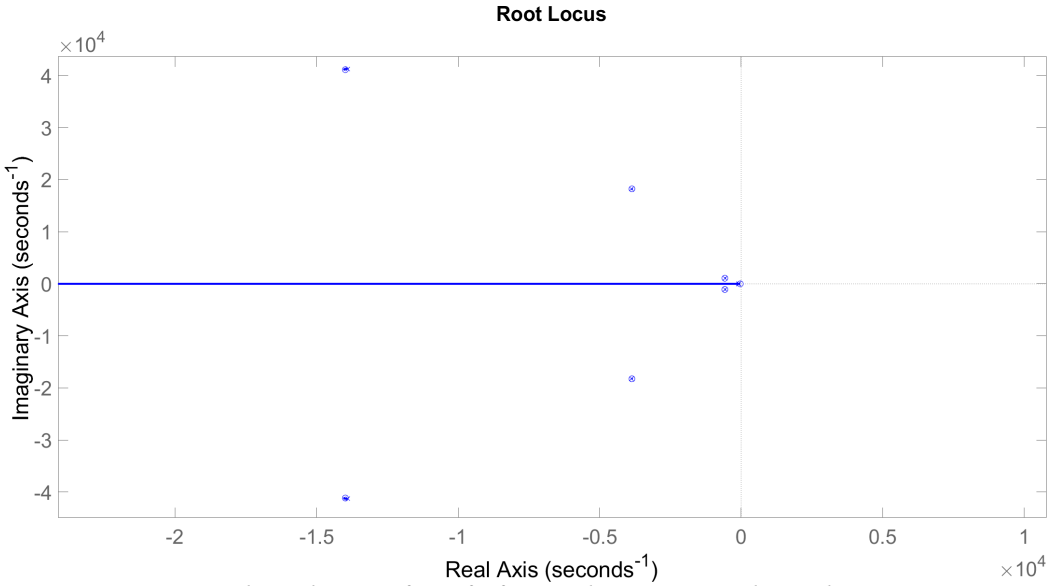


Figure 72: Root locus diagram of transfer function between v_{B1} and ϕ_1 with 1.2 mF C_{Vb}

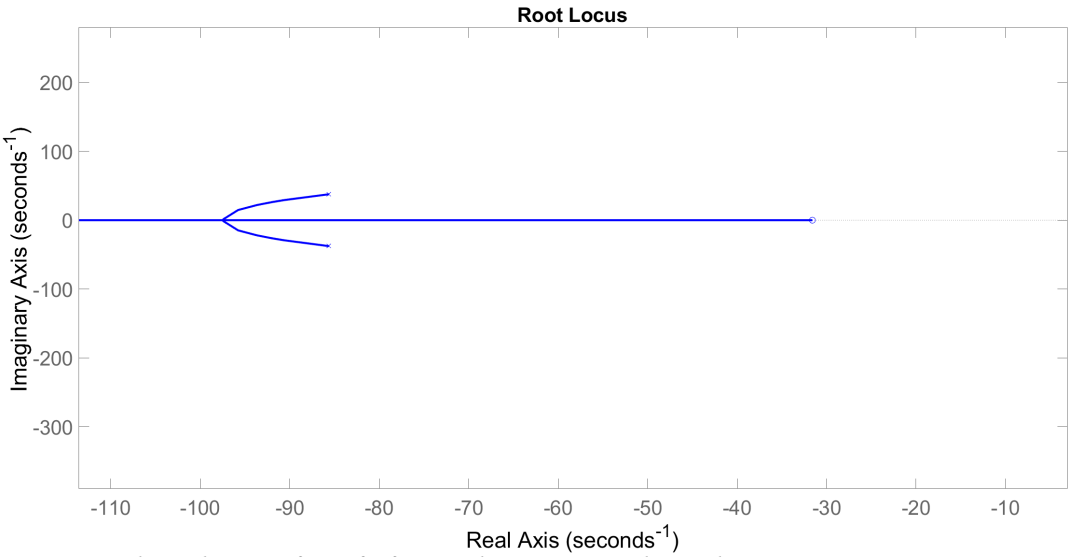


Figure 73: Root locus diagram of transfer function between v_{B1} and ϕ_1 with 1.2 mF C_{Vb} (zoom in version in imaginary axis region)

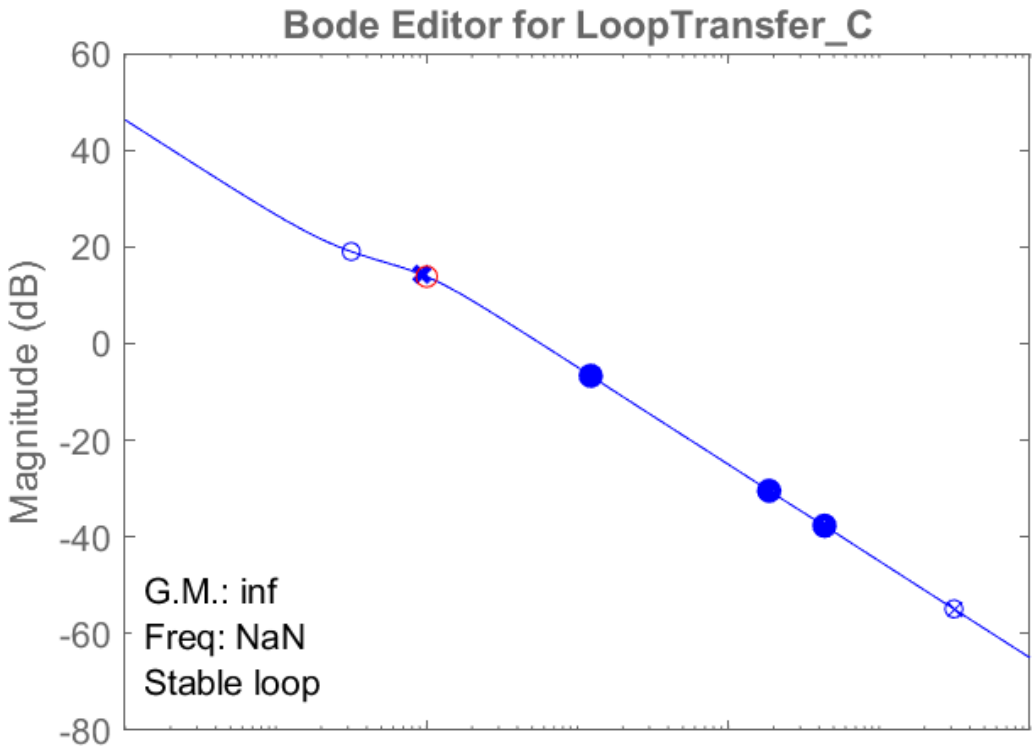


Figure 74: Bode plot of gain margin with combined PI controller(Equation 160) and the transfer function of v_{B1} to ϕ_1.

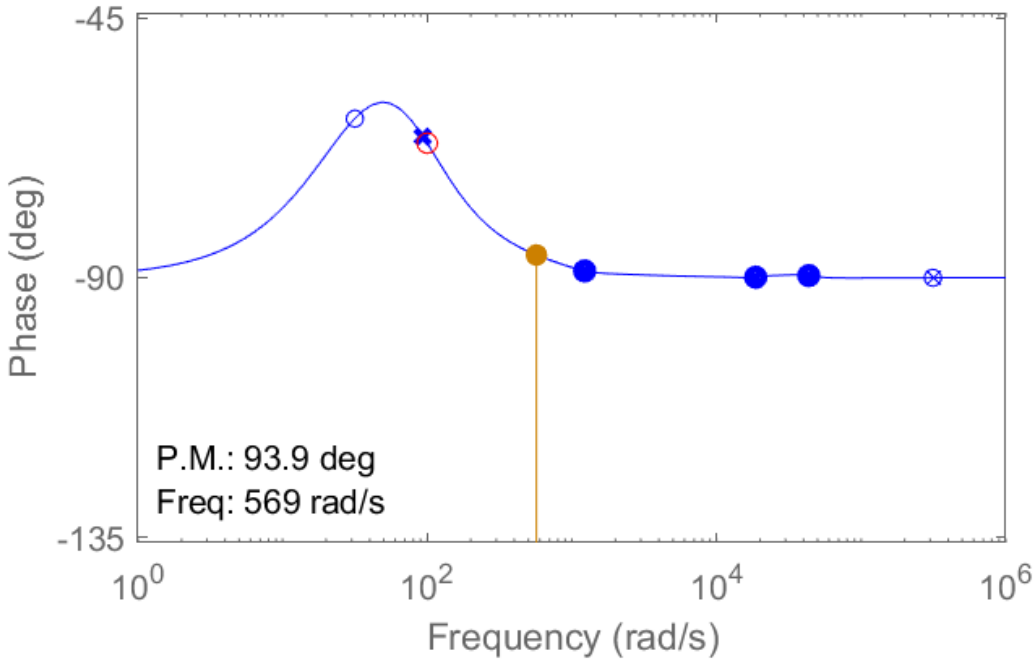


Figure 75: Bode plot of phase margin with combined PI controller(Equation 160) and the transfer function of v_{B1} to ϕ_1.

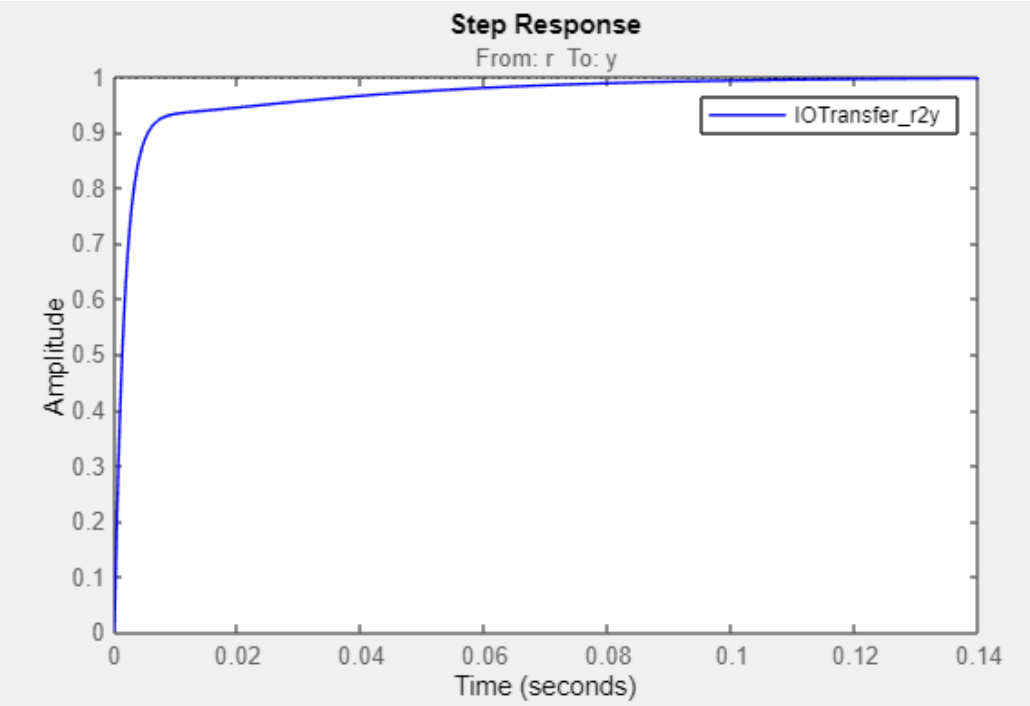


Figure 76: Step response graph for DPP_1 converter

5 Conclusion

The objective of modelling and studying the dynamic behavior of the PV2VB P-DPP configuration in order to analyze the system stability and design appropriate controllers was achieved. The following chapter is to answer the research question.

1- Which methodology can be applied to model the configuration?
Linearisation and state space analysis can be applied. State space equation representation is a mathematical framework for describing the behavior of linear time-varying systems concisely and systematically. It provides a convenient method for modeling and analyzing system dynamics, designing controllers, and studying system responses to various inputs and initial conditions. However, power converters contain nonlinear elements. Therefore, the state space equations describing its behavior will contain non-linear terms. Nonlinear systems are often more complex to analyze and control. To simplify the model, as well as its analysis and design, the linearization technique can be applied. Here's how linearization around an operating point is typically performed: first, define State Variables and Inputs, then write the equilibrium equations and linearize it. Then, To analyze the linearized system, we first define the input and output, then convert the equilibrium equations into state space equations, and finally convert the state space equations into transfer functions.

2- In P-DPP PV2VB Architecture, how do the different parameters affect the dynamic behavior of a PV2VB P-DPP architecture?
P-DPP PV2VB Architecture compensates the voltage between PV strings so each PV string can operate at operate at their own MPP. The duty cycle of the central converter can control the virtual bus voltage. Therefore, the transfer function between v_{VB} and d_s can represent the dynamic behavior of P-DPP PV2VB Architecture. As shown in Chapter4, a PV2VB P-DPP system made of 2 PV strings is implemented and analyzed. As the voltage difference generated between two PV strings increases, to maintain stability, the minimum requirement value of the virtual bus capacitor needs to increase. Furthermore, for the passive components, the value of the inductor at the DPP and central converter increases, and the minimum requirement value of the virtual bus capacitor must increase to maintain stability. Changing the value of the capacitor in the DPP has almost no effect on the minimum requirement value of the virtual bus capacitor. However, when the value of the capacitor in the central converter is much greater than the virtual bus capacitor, it reduces the minimum requirement value of the virtual bus capacitor.

3- How to apply the mathematical equation to design robust controllers?
In this project, the central converter control is determined by v_{VB} to d_s After obtaining the transfer function and implementing it in MATLAB, consider the worst-case scenario, which is that one string is fully operational, whereas in the other string, only one PV module is fully functioning while the other 9 modules are bypassed. Extract the transfer function into the SISOtool toolbox. Based on the criteria on GM (greater than 10 dB), PM (greater than 45 degrees), and transient response time (lower than 5 seconds), a robust controller can be obtained. A robust controller performs its intended function even when there are unexpected in the environment (such as partial shading occurring on the PV module). The system remains stable.

4- What is the optimal value (or range) of virtual bus capacitance, and how can it be evaluated?
The stability margin determines the dominant pole, Based on Figure 61, at 90μF, the dominant pole is furthest from the imaginary axis with the highest stability margin. So is the optimal choice in the worst-case scenario. However, in reality, capacitor selection needs to consider voltage rating and ripple current. The optimal range for virtual bus capacitance range is between 100μF to 1 mF.

5- In the controller design, how to fine-tune the PI controller parameters?
After setting the PI controller, the proportional gain determines the strength of this control action. The integral action helps to eliminate steady-state errors and improves the system's ability to track the reference point. The sensitivity test can be applied to fine-tune the PI controller parameters. In other words, keep K_p constant and vary the value of K_i, or keep K_i constant and vary the value of K_p based on the GM, PM, and transient response time. The optimal PI controller parameters can be obtained. A gain margin of 15.7 dB, a phase margin of 121 degrees, and a settling time of 0.8 s have been achieved for the outer control loop (central converter) by setting K_i and K_p to $5s^{-1}$ and 0.5, respectively.

6 Recommendation for further work

In this section, some suggestions are made as it was impossible to explore these options more within the timeframe of this thesis project. This section can be divided into two parts, the first relating to further simulations and the second to experiments.

6.1 Simulation Suggestion

6.1.1 Multiple String simulate

In Chapter 4, two strings are fully modeled and analyzed. Using the simulation framework developed during this project, the model can be scaled up to N string. For example, to model a four-string system, we can import different shading level parameters into the model, the shading detail in terms of I_{MPP} and V_{MPP} are shown in Table 14). We can then analyze the transient behavior of the system. Similarly, we can model a three-string system. By comparing different shading level combinations, we can determine the minimum size of the capacitor needed for the virtual bus.

Table 14: Shading effect on maximum power point [56]

Shading	I_{sc} (A)	V_{oc} (V)	P_{MPP} (W)	I_{MPP} (A)	V_{MPP} (V)
0%	3.31	21.1	51	3.15	16.2
25%	3.24	17.49	36.5	2.68	13.6
50%	2.85	17.1	30.5	2.35	13
75%	0.7	15.01	7.5	0.625	12

6.1.2 Central inverter implementation

In this project, a central converter was used. However, if the central converter is replaced with an inverter, a solar inverter is no longer necessary. This is because the central inverter performs the same function as a solar inverter, which is to convert the direct current (DC) electricity generated by solar panels into alternating current (AC) electricity that can be used by household appliances. When designing or selecting an inverter, some key factors to consider are power rating and load requirements, voltage and frequency, protection and safety features, electromagnetic interference (EMI), and noise and harmonics.
When designing or selecting an inverter, some key factors to consider are power rating and load requirements, voltage and frequency, protection and safety features, electromagnetic interference (EMI), and noise and harmonics.

6.1.3 Implement PID control

For the controller, refer to Figure 63, replace PI controller with PID controller; in the SISOtool toolbox, the tuning interface refers to Figure 67, change the change type from PI to PID. In PID control, the derivative term can predict future errors and thus react faster to changes and helps dampen oscillations, thereby reducing overshoot. However, PID control is more complex to implement than PI control because PID control can be more sensitive to changes in the system parameters[57]. Finding the optimal balance of proportional, integral, and derivative terms for the best performance is a challenging and time-consuming process.

6.1.4 Improve User-friendly interface in Matlab

In the current Matlab code, if a new user wants to test a new model for dynamic behavior, it is difficult for new users to insert input data. So, the suggestion is to use Graphical User Interface (GUI) in MATLAB. GUI is an interactive interface that allows users to interact with your MATLAB programs visually. For the P-DPP PV2VB code, here is the assumption to make it user-friendly. First, ask the user how much string want to simulate, then let the user enter each string information like the number of PV modules and the parameter of V_{mpp} and I_{mpp}, after entering the PV string information the value of the parameter in Table 6 can be set. In addition, the voltage of the DC link and virtual bus can be set. The last figure that needs to be entered is the value of the virtual bus capacitor. After the pre-conditions setting, select which transfer function you want to process. Then, the program will determine whether the system is stable or not. If the user wants to know the minimum value of the virtual bus capacitor to maintain stability, click the min button. The minimum value of the virtual bus capacitor can be obtained by using a loop to test the system's stability.

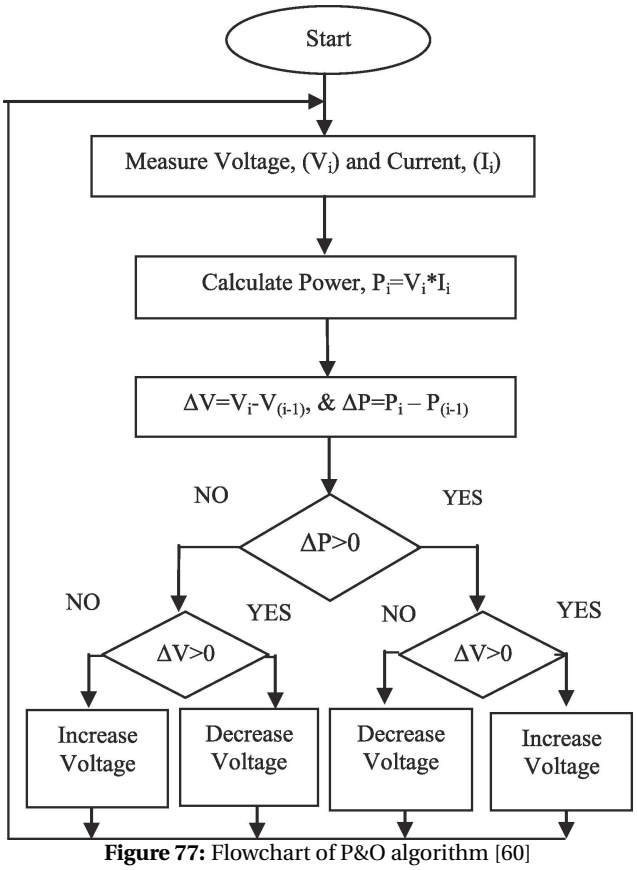


Figure 77: Flowchart of P&O algorithm [60]

6.1.5 Adding more PV module parameters for better modeling and performance

The current PV model assumes that the PV module is operating at its (MPP) based on the irradiance. However, the temperature, degradation, and dust on the PV panel can affect the MPP performance. To account for the temperature effect, one method is to implement the Sandia equation[58]. This equation takes into account the temperature of the PV module and the ambient temperature to calculate the MPP voltage and current. While there are other factors that can affect the degradation of a PV module, such as manufacturing defects and UV radiation, two of the most important factors are its age and climate. Age can be quantified by the number of years that the module has been in operation, while climate can be quantified by factors such as temperature, humidity, and wind speed. The rate of degradation will vary depending on the module's design and the conditions it is exposed to. Historical data can be used to predict how the performance of a PV module will degrade over time. PV modules are more likely to degrade in hot and humid climates because the heat and humidity can accelerate the degradation of the materials in the modules [59]. The dust effect on PV modules can be taken into account by considering two scenarios: sunny days and rainy days. On a sunny day, dust will accumulate on the PV module, which can reduce the module's output power. On a rainy day, some of the dust will be washed away, depending on the intensity of the rain.

6.1.6 P&O algorithm implementation on PV module to track MPP

In this project, the PV module is assumed to operate at MPP condition. However, the PV module may operate in non-MPP regions to track the PV module operation at MPP; the P&O method is implemented on the PV module. Figure 77 shows the flow chart of P&O algorithm. To begin, measure the initial PV voltage and current and calculate the corresponding power. Then, considering a small perturbation in voltage (ΔV) or duty cycle (ΔD) of the DC-DC converter in one direction, the corresponding power is calculated and compared with the previous value of power[60]. If the change in power (ΔP) is positive, then the perturbation is in the correct direction; otherwise, the direction should be reversed (i.e., decrementing ΔV) [60].

6.2 Practical Suggestion

6.2.1 Optimization of the power process

In reality, not only is tracking maximum power points important, but the loss is another factor that needs to be considered. In both cases, the objective is to extract the maximum power for the PV array and deliver it to the grid/load. However, there is more constraint; in reality, the DPP is not 100% efficient due to switching loss, components power dissipation, transformer leakage loss, etc. Although DPP can still eliminate the voltage mismatch between the strings, the power output after implementing P-DPP PV2VB can be lower compared with a system without P-DPP PV2VB. Therefore, optimizing how much power flows to the DPP can enhance power delivery to the grid/load. Another limitation is temperature since most losses cause heat from the power electronics. High temperatures can lead to thermal stress and decomposition of the materials inside the device, affecting the overall reliability and service life [61]. Installing a heat sink is one way to avoid overheating the power electronics. Heat sinks help transfer heat from the power electronic to the surrounding air by conduction and convection. Another way is to place a sensor to monitor the temperature and develop control algorithms to ensure the components operate below the temperature limit.

6.2.2 Micro controller design

For the control of the DPP and central converter, one of the options is to use a microcontroller to implement control algorithms. Microcontrollers provide the computational power, flexibility, and integration necessary to implement PID and PWM controllers effectively in various control applications. Their real-time capabilities, ease of algorithm implementation, and adaptability make them a versatile platform for designing and deploying control systems.

References

[1] H. Li, H. Mu, and M. Zhang, "Analysis of china's energy consumption impact factors," *Procedia Environmental Sciences*, vol. 11, pp. 824–830, 2011, 2011 2nd International Conference on Challenges in Environmental Science and Computer Engineering (CESCE 2011), ISSN: 1878-0296. DOI: https://doi.org/10.1016/j.proenv.2011.12.126. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1878029611009492.

[2] A. Energy. "Renewable Energy vs Fossil Fuels: 5 Essential Facts." (2022), [Online]. Available: https://amigoenergy.com/blog/renewable-energy-vs-fossil-fuels/.

[3] H. Ritchie, M. Roser, and P. Rosado, "Energy," *Our World in Data*, 2022, https://ourworldindata.org/energy.

[4] ucdavis. "What is Solar Power?" (2022), [Online]. Available: https://www.ucdavis.edu/climate/definitions/how-is-solar-power-generated/.

[5] P. Manganiello, M. Balato, and M. Vitelli, "A survey on mismatching and aging of pv modules: The closed loop," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7276–7286, 2015.

[6] A. Nazer, P. Manganiello, and O. Isabella, "A virtual bus parallel differential power processing configuration for photovoltaic applications," *Mathematics and Computers in Simulation*, 2023, ISSN: 0378-4754. DOI: https://doi.org/10.1016/j.matcom.2023.06.001. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378475423002446.

[7] A. Smets, K. Jäger, O. Isabella, R. van Swaaij, and M. Zeman, *Solar Energy: The physics and engineering of photovoltaic conversion, technologies and systems*, English. UIT Cambridge Limited, 2016, ISBN: 978-1-906860-32-5.

[8] S. Motahhir, A. El Hammoumi, and A. El Ghzizal, "Photovoltaic system with quantitative comparative between an improved mppt and existing inc and po methods under fast varying of solar irradiation," *Energy Reports*, vol. 4, pp. 341–350, 2018, ISSN: 2352-4847. DOI: https://doi.org/10.1016/j.egyr.2018.04.003. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352484717302998.

[9] T. delft PVMD. "PV Systems Components - Maximum Power Point Tracking." (2022), [Online]. Available: https://brightspace.tudelft.nl/d2l/le/content/491381/viewContent/2635862/View.

[10] O. Khan and W. Xiao, "Review and qualitative analysis of submodule-level distributed power electronic solutions in pv power systems," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 516–528, 2017, ISSN: 1364-0321. DOI: https://doi.org/10.1016/j.rser.2017.03.073. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032117304094.

[11] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel pwm control scheme for pv application," *IEEE transactions on industrial electronics*, vol. 57, no. 6, pp. 2111–2123, 2009.

[12] S. Rivera, S. Kouro, B. Wu, J. I. Leon, J. Rodríguez, and L. G. Franquelo, "Cascaded h-bridge multilevel converter multistring topology for large scale photovoltaic systems," in *2011 IEEE International Symposium on Industrial Electronics*, 2011, pp. 1837–1844. DOI: 10.1109/ISIE.2011.5984437.

[13] D. Kolantla, S. Mikkili, S. R. Pendem, and A. A. Desai, "Critical review on various inverter topologies for pv system architectures," *IET Renewable Power Generation*, vol. 14, no. 17, pp. 3418–3438, 2020.

[14] H. Kim, G. Yu, J. Kim, and S. Choi, "Pv string-level isolated dc–dc power optimizer with wide voltage range," *Energies*, vol. 14, no. 7, 2021, ISSN: 1996-1073. DOI: 10.3390/en14071889. [Online]. Available: https://www.mdpi.com/1996-1073/14/7/1889.

[15] A. Shawky, F. Helmy, M. Orabi, J. A. Qahouq, and Z. Dang, "On-chip integrated cell-level power management architecture with mppt for pv solar system," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 572–579. DOI: 10.1109/APEC.2014.6803366.

[16] A. Shawky, F. E. Helmy, M. Orabi, J. A. A. Qahouq, and Z. Dang, "On-chip integrated cell-level power management architecture with mppt for pv solar system," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 572–579, 2014.

[17] C. Olalla, C. Deline, D. Clement, Y. Levron, M. Rodriguez, and D. Maksimovic, "Performance of power-limited differential power processing architectures in mismatched pv systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 618–631, 2015. DOI: 10.1109/TPEL.2014.2312980.

[18] Z. Moradi-Shahrbabak, A. Tabesh, and G. R. Yousefi, "Economical design of utility-scale photovoltaic power plants with optimum availability," *IEEE Transactions on Industrial Electronics*, vol. 61, pp. 3399–3406, 2014.

[19] O. I. Afshin Nazer Patrizio Manganiello, "A comprehensive classification of state-of-the-art distributed maximum power point tracking techniques in photovoltaic systems," *IEEE*, vol. Submitted to Proceedings of the IEEE. 2022.

[20] K. Alluhaybi, I. Batarseh, and H. Hu, "Comprehensive review and comparison of single-phase grid-tied photovoltaic microinverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1310–1329, 2020. DOI: 10.1109/JESTPE.2019.2900413.

[21] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002. DOI: 10.1109/TIE.2002.801052.

[22] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in pv systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2711–2726, 2013. DOI: 10.1109/TPEL.2012.2221482.

[23] K. Mansfield, "Comparison of single stage and two stage stage grid-tie inverters," University of Central Florida, 2007.

[24] A. Bineshaq, M. I. Hossain, H. Binqadhi, A. Salem, and M. A. Abido, "Design and control of two-stage dc-ac solid-state transformer for remote area and microgrid applications," *Sustainability*, vol. 15, no. 9, 2023, ISSN: 2071-1050. DOI: 10.3390/su15097345. [Online]. Available: https://www.mdpi.com/2071-1050/15/9/7345.

[25] N. E. Zakzouk, A. K. Abdelsalam, A. A. Helal, and B. W. Williams, "Pv single-phase grid-connected converter: Dc-link voltage sensorless prospective," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 526–546, 2016.

[26] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: An overview," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1305–1314, 2004. DOI: 10.1109/TPEL.2004.833460.

[27] A. Lashab, D. Sera, F. Hahn, *et al.*, "Cascaded multilevel pv inverter with improved harmonic performance during power imbalance between power cells," *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2788–2798, 2020. DOI: 10.1109/TIA.2020.2978164.

[28] S. Barcellona, M. Barresi, and L. Piegari, "Mmc-based pv single-phase system with distributed mppt," *Energies*, vol. 13, no. 15, 2020, ISSN: 1996-1073. DOI: 10.3390/en13153964. [Online]. Available: https://www.mdpi.com/1996-1073/13/15/3964.

[29] P. Sochor and H. Akagi, "Energy-balancing control of a delta-configured modular multilevel cascade inverter for utility-scale photovoltaic systems," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 4706–4713. DOI: 10.1109/ECCE.2015.7310325.

[30] M. Bahrami-Fard, N. Moeini, M. Shahabadini, H. Iman-Eini, and M. Liserre, "A new topology and modulation strategy to suppress the leakage current in transformerless cascaded h-bridge inverters in pv application," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 1219–1229, 2023. DOI: 10.1109/JESTPE.2022.3158424.

[31] Z. Liang, R. Guo, J. Li, and A. Q. Huang, "A high-efficiency pv module-integrated dc/dc converter for pv energy harvest in freedm systems," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 897–909, 2011. DOI: 10.1109/TPEL.2011.2107581.

[32] S. Ravyts, M. Dalla Vecchia, G. Van den Broeck, and J. Driesen, "Review on building-integrated photovoltaics electrical system requirements and module-integrated converter recommendations," *Energies*, vol. 12, no. 8, 2019, ISSN: 1996-1073. DOI: 10.3390/en12081532. [Online]. Available: https://www.mdpi.com/1996-1073/12/8/1532.

[33] J. Huusari and T. Suntio, "Origin of cross-coupling effects in distributed dc–dc converters in photovoltaic applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4625–4635, 2013. DOI: 10.1109/TPEL.2012.2235860.

[34] S. R. Pendem and S. Mikkili, "Assessment of cross-coupling effects in pv string-integrated-converters with pamp;o mppt algorithm under various partial shading patterns," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 4, pp. 1013–1028, 2022. DOI: 10.17775/CSEEJPES.2019.03330. [Online]. Available: https://www.sciopen.com/article/10.17775/CSEEJPES.2019.03330.

[35] S. R. Pendem and S. Mikkili, "Assessment of cross-coupling effects in pv string-integrated-converters with po mppt algorithm under various partial shading patterns," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 4, pp. 1013–1028, 2022. DOI: 10.17775/CSEEJPES.2019.03330.

[36] M. J. Kasper, D. Bortis, and J. W. Kolar, "Unified power flow analysis of string current diverters," *Electrical Engineering*, vol. 100, pp. 2085–2094, 2018. [Online]. Available: https://api.semanticscholar.org/CorpusID:116358994.

[37] G. Chu, H. Wen, Y. Hu, L. Jiang, Y. Yang, and Y. Wang, "Low-complexity power balancing point-based optimization for photovoltaic differential power processing," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 306–10 322, 2020. DOI: 10.1109/TPEL.2020.2977329.

[38] T. Zhang and J. Jiang, "A review on differential power processing for pv submodule dmppt," in *2020 IEEE 3rd Student Conference on Electrical Machines and Systems (SCEMS)*, 2020, pp. 1012–1017. DOI: 10.1109/SCEMS48876.2020.9352300.

[39] H. Lee and K. A. Kim, "Design considerations for parallel differential power processing converters in a photovoltaic-powered wearable application," *Energies*, vol. 11, no. 12, 2018, ISSN: 1996-1073. DOI: 10.3390/en11123329. [Online]. Available: https://www.mdpi.com/1996-1073/11/12/3329.

[40] Y.-T. Jeon, H. Lee, K. A. Kim, and J.-H. Park, "Least power point tracking method for photovoltaic differential power processing systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1941–1951, 2017. DOI: 10.1109/TPEL.2016.2556746.

[41] Seaward. "How does temperature and irradiance affect I-V curves?" (2022), [Online]. Available: https://www.seaward.com/gb/support/solar/faqs/00797-how-does-temperature-and-irradiance-affect-i-v-curves//.

[42] J. Cubas, S. Pindado, and C. De Manuel, "Explicit expressions for solar panel equivalent circuit parameters based on analytical formulation and the lambert w-function," *Energies*, vol. 7, no. 7, pp. 4098–4115, 2014, ISSN: 1996-1073. DOI: 10.3390/en7074098. [Online]. Available: https://www.mdpi.com/1996-1073/7/7/4098.

[43] J. Charles, M. Abdelkrim, Y. Muoy, and P. Mialhe, "A practical method of analysis of the current-voltage characteristics of solar cells," *Solar cells*, vol. 4, no. 2, pp. 169–178, 1981.

[44] N. Dani, "Modelling and control of mppt converters for dc microgrids," Delft University of Technology, 2022.

[45] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, 1991. DOI: 10.1109/28.67533.

[46] A. R. Rodríguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional dc/dc conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 1129–1135. DOI: 10.1109/ECCE.2010.5617847.

[47] Y. Cho and J.-S. Lai, "Digital plug-in repetitive controller for single-phase bridgeless pfc converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 165–175, 2013. DOI: 10.1109/TPEL.2012.2196288.

[48] M. I. of Technology. "State-space representation of lti systems." (2023), [Online]. Available: http://web.mit.edu/2.14/www/Handouts/StateSpace.pdf.

[49] TSEC. "V-series 270 - 280 w mono solar panel." (2023), [Online]. Available: https://www.solartechpower.com/images/TSEC%206x10%20Mono%20270-280W%20with%20PTC%20Value.pdf (visited on 08/08/2023).

[50] K. Ogata. "Modern control engineering." (2010), [Online]. Available: http://docs.znu.ac.ir/members/pirmohamadi_ali/Control/Katsuhiko%20Ogata%20_%20Modern%20Control%20Engineering%205th%20Edition.pdf.

[51] A. Namvar, *Robust Control Systems*. 2019. [Online]. Available: https://sharif.edu/~namvar/index_files/robust.pdf.

[52] T. Skvarenina, *The Power Electronics Handbook*. CRC Press, 2002. [Online]. Available: https://library.uoh.edu.iq/admin/ebooks/62729-crc-press---the-power-electronics-handbook---t.-skvarenia-(2002)-ww.pdf.

[53] M. Electronics. "Aluminum electrolytic capacitors power high ripple current miniaturized snap-in." (2023), [Online]. Available: https://nl.mouser.com/ProductDetail/Vishay-BC-Components/MAL225957101E3?qs=r5DSvlrkXmKYqS%2FXiJVE%2Fg%3D%3D (visited on 08/12/2023).

[54] A. O'Dwyer, "A summary of pi and pid controller tuning rules for processes with time delay. part 1: Pi controller tuning rules," *IFAC Proceedings Volumes*, vol. 33, no. 4, pp. 159–164, 2000, IFAC Workshop on Digital Control: Past, Present and Future of PID Control, Terrassa, Spain, 5-7 April 2000, ISSN: 1474-6670. DOI: https://doi.org/10.1016/S1474-6670(17)38237-X. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S147466701738237X.

[55] Javatpoint, *Example of root locus*, 2023. [Online]. Available: https://www.javatpoint.com/example-of-root-locus.

[56] A. A. Elgendy, M. M. Eltamaly, and M. A. El-Sherif, *Performance analysis of photovoltaic modules under shading effect*, 2019. [Online]. Available: https://www.researchgate.net/publication/268485690_Performance_Analysis_of_Photovoltaic_Modules_Under_Shading_Effect#pf2.

[57] Author(s), "Comparative study of p, pi, and pid controller for speed control of vsi-fed induction motor," *International Journal of Engineering Development and Research*, vol. 2, no. 2, p. 2740, 2014, ISSN: 2321-9939. [Online]. Available: http://www.ijedr.org.

[58] S. N. Laboratories, *Sandia pv array performance model*, 2023. [Online]. Available: https://pvpmc.sandia.gov/modeling-steps/2-dc-module-iv/point-value-models/sandia-pv-array-performance-model/.

[59] D. C. Jordan, J. H. Wohlgemuth, and S. R. Kurtz, "Technology and climate trends in pv module degradation: Preprint," Oct. 2012. [Online]. Available: https://www.osti.gov/biblio/1053315.

[60] D. Pilakkat and S. Kanthalakshmi, "An improved P&O algorithm integrated with artificial bee colony for photovoltaic systems under partial shading conditions," *Solar Energy*, vol. 178, pp. 37–47, 2019, ISSN: 0038-092X. DOI: 10.1016/j.solener.2018.12.008. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038092X18311836.

[61] J. Huang, W. Sun, Z. Zhang, Z. Ling, and X. Fang, "Thermal protection of electronic devices based on thermochemical energy storage," *Applied Thermal Engineering*, vol. 186, p. 116507, 2021, ISSN: 1359-4311. DOI: https://doi.org/10.1016/j.applthermaleng.2020.116507. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1359431120339818.