Monolithic Integration of Rectifiers and Drivers for low power SSL applications on a Rigid to Flex Substrate

Delft University of Technology

Monolithic Integration of Rectifiers and Drivers for low power SSL applications on a Rigid to flex substrate

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Abstract

Solid State Lighting (SSL) is one of the prominent light sources for future lighting applications with benefits such as high energy savings, long lifetimes and high efficiency. The main drawback in solid state lighting system is that the total initial cost of the system is high for large scale production. Packaging and electronics components in the system account to about 60% of the total cost. Silicon based wafer level packaging offers great advantages for large scale cheap production. Furthermore it also helps to create to create miniaturized and multifunctional system with integrated electronics with LEDs. In this thesis, a novel schottky diode in BiCMOS having high current conduction and high breakdown is designed and fabricated. A monolithically integrated rectifiers composed with four schottky diodes is presented. The rectifiers designed using schottky diodes are fabricated in a simple and low cost DIMES BiCMOS7 process. A detailed modeling and simulation of schottky diodes in a standard BiCMOS process is done to derive design parameters to achieve high current and high breakdown voltage. It has been found that with guard rings and a n well doping concentration determined by a phosphor dose of 6e12, schottky diodes with a breakdown voltage of 27V and forward current of 1A at 0.68V are fabricated in this process. A complete design, fabrication, characterization and spice modeling of the schottky diodes are presented. NMOS and NPN bipolar transistor fabricated in the BiCMOS process are characterized and modeled. A basic linear and switch mode driver using the devices fabricated in the BiCMOS process is analyzed. A design proposal for integrating the rectifiers and drivers on a Rigid to flex substrate is presented. The developed concept offers great advantage for wafer level integration of SSL system to reduce cost and create smart multifunctional miniaturized products.

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Chapter 1

Introduction

With the invention of semiconductor devices and integrated circuit, this era has been defined as the electronics era. The semiconductor industry is a key driver for the development of many industries such as education, transportation, biomedical, communication and entertainment to name a few. Electronics systems have influenced every aspect of our lives and play a vital role in day to day activities. The next big development in the semiconductor industry over the last decade has been with the advent of Solid State Lighting (SSL) for general lighting application.

Technology for the lighting industry began with the invention of the incandescent bulb by Thomas Alva Edison in 1879. Later in the year 1906, General Electric patented the first tungsten light bulb. Though incandescent lamps are very cheap to manufacture, they were inefficient as they convert only about 1% to 5% of the consumed electricity into usable light. The next generation of lighting technology followed with the introduction of fluorescent lamp in 1930's. These lamps have improved efficiency than incandescent bulbs but contain small amount toxic gases like mercury which is harmful for the atmosphere. Due to the above drawbacks of incandescent and fluorescent lamps, there is a need for the lighting industry to create lighting systems that are efficient, have lower manufacturing cost and reduced atmospheric pollution [1].For this development, there here has been a lot of interest in the field of Solid State Lighting as it provides good potential for energy efficient, safe and affordable lighting solutions. In the recent survey, the lighting market, including light sources(LED's), electronics and luminaries is estimated to increase from €50 billion in 2010 to €70 billion by the year 2020 [2].

Solid State Lighting refers to light obtained from semiconductor devices. The first report on electroluminescence was published by Henry J Round in 1907 when he found that current passed through carborundum diode emitted light. But the invention of Light Emitting Diode is credited to Russian scientist Losev who correctly explained the phenomena of light emission in

silicon carbide diodes used in his work on radio receivers [3]. LED's mainly red, blue, green was used as indicators, displays in electronic systems due to their low lumen/watt till the early 90's. The development of white LED's in mid-90's provided interest to use LED's as an alternative to general lighting and it has accelerated the growth of LED's. The design of LED lighting system is complex and different from conventional lighting .It provides a lot of design and reliability challenges in the area of electrical, packaging, optical and luminaries.

LED's are constant voltage load with a low equivalent series resistance. Most of the LED's are powered by DC source. For general lighting it becomes essential to convert AC main supply voltage to regulated DC voltage using rectifiers and filters. Based on the topology of the connected LED's i.e. series or parallel, a constant voltage regulated driver or current regulated driver is used [4]. The electronics components in the SSL system that account to cost and PCB space include rectifying diodes, driver IC and passive components. The process integration of the electronics and passive components by monolithically or wafer level integration can significantly bring down the initial cost of the SSL system. Since SSL is based on semiconductor technology, it can be integrated with standard CMOS process to create a complete multifunctional miniaturized module.

In the introductory chapter, the design of an SSL system is first discussed. Then the concepts of wafer level integration for SSL are presented. Finally, the research focus and a systematic approach followed in the thesis for monolithic integration of rectifiers and driver for low power solid state lighting system on rigid to flexible platform is presented.

1.1 Solid State Lighting System

The design of SSL system is similar to a microelectronics system design. It is different from the conventional lighting system design. The fundamental part of the SSL system is the LED (Light emitting diode). Light Emitting Diodes are p-n junction diodes when forward biased emit light by spontaneous recombination of electron-hole pairs and simultaneous emission of photons. The energy of the photons emitted determines the wavelength of light emitted. LED's are made from silicon carbide material or III–IV semiconductor like gallium arsenide, gallium nitride. The light emitted from LED occupies a narrow spectrum and the specific wavelength or color depends on the band gap of the material. Most white light LED's use an LED emitting at shorter wavelength (e.g. blue) and a wavelength converter (e.g. phosphor). The light emitted by the blue LED is absorbed by the phosphor material and converted as white light with longer wavelength [5] . The quality measurement of LED's are defined using the table of white light from blue LED is achieved by wavelength converters. The LED die is mounted in a on a silicon carrier and installed in a package for electrical connection. This LED module is the fundamental component of the solid state lighting system.

A brief summary of SSL system components and its functions is presented in Table 1.1[6]

Table 1.1 Levels of SSL System

Level	System Component	Example	Function
0	**LED Die**		**To achieve high luminous efficiency**
1	**LED Package**		**For electrical connection, heat dissipation and mechanical stability.**
2	**Multi LED Board**		**Increasing the number of LED's for higher lumen output.**
3	**LED Power Control and Drivers**		**To convert AC to DC and provide constant current and control of the LED.**
4	**Luminaire Designs**		**To enable usage of LED bulb as conventional bulb by using retrofit design.**
5	**Lighting System Designs**		**Multiple interconnected luminaries for lighting system on large scale.**

As described in Table 1.1, it can be seen that the electronics components comprise more than 50% of a complete SSL system. The main semiconductor IC components of this system are power converters and driver circuitry. A composition of the cost analysis of driver for SSL

system for a LED lighting system is shown in Figure 1.1[2]. The major cost component of the LED system is due to the LED package which contributes to about 30% of the total LED bulb. The other component that drives the cost is the thermal/ mechanical housing and electrical components in the system.

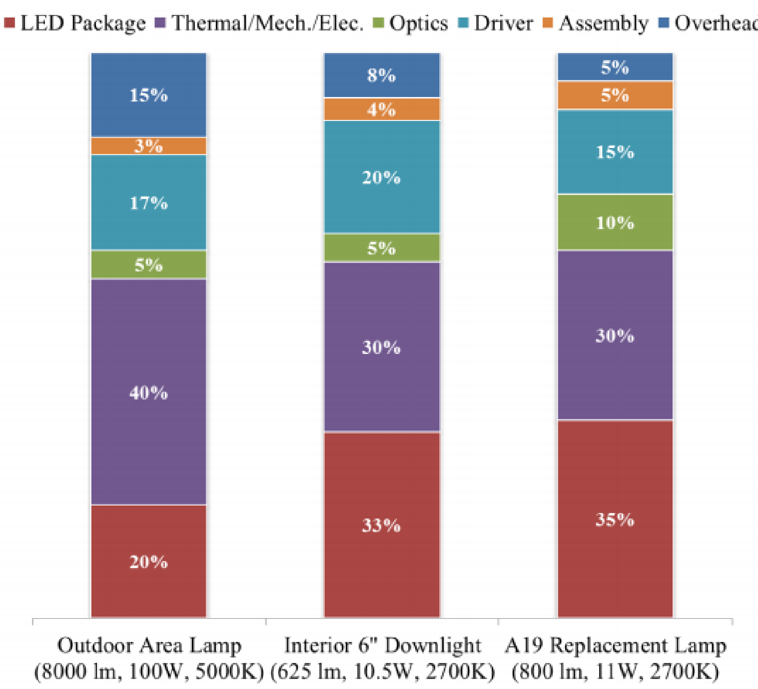

Figure 1.1 Cost breakdown of SSL System

Since LED packaging and electronics are the critical components that drive the total system cost, the integration of both packaging and electronics for the SSL system can result in the reduction of total system cost. Some of the concepts of wafer level integration are discussed in the next section.

1.2 Wafer Level Integration for SSL system

Heterogeneous wafer level system integration and packaging is a key driving technology for multifunctional system in a package (SiP) microelectronic systems for reducing cost, size and improving performance. The main aspect of system in a package technology is to combine semiconductor technology with other technologies in an electronic packaging dimension. This includes integration of heterogeneous functions like electrical, optical, mechanical to create high value single miniaturized system package at low cost [7].

For a SSL system in a package, the main challenges include integration of power converters, drivers and passives along with LED module. Since LED's are manufactured on

silicon carbide or gallium nitride substrate and semiconductor IC technology is on silicon substrate, it is not possible to integrate both lighting functions and IC functionalities on a single substrate. One of the methods for integrating LED module with integrated circuits is shown in Figure 1.2 [6]. In the first design the LED is mounted on a silicon sub mount and wire bonded to the PCB for electrical connection. The IC chip for LED driver and power controller are packaged components connected to the LED through PCB interconnections.

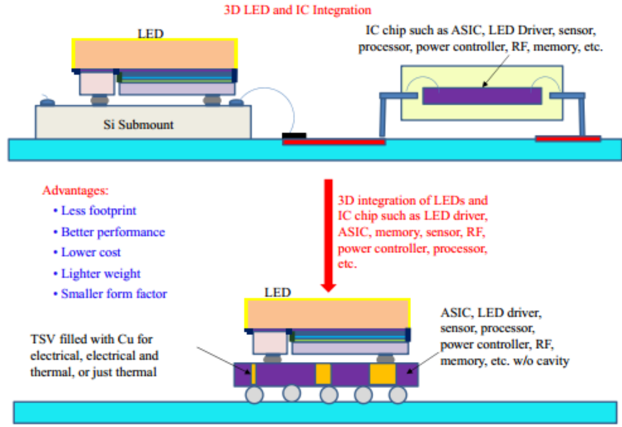

Figure 1.2 3D LED and IC integration

With 3D integration the passive Si sub mount in the LED module will be replaced by the ASIC, LED drivers, power controller and processors in a 3D method. The electrical connection for this module is achieved by through silicon vias (TSV) of copper. The main advantages of this system in a package is less footprint , low cost and small form factor [6] [8].

Conventional LED packaging consists of LED module with interconnect leads housed in a ceramic packaging. A better LED packaging technology that is suitable for wafer level integration is using silicon based packaging. Silicon is used as carrier wafer and interconnection with LED is made using through silicon vias (TSV). The LED chips are then encapsulated in a silicone lens. An example of silicon based packaging is shown in Figure 1.3 [9].

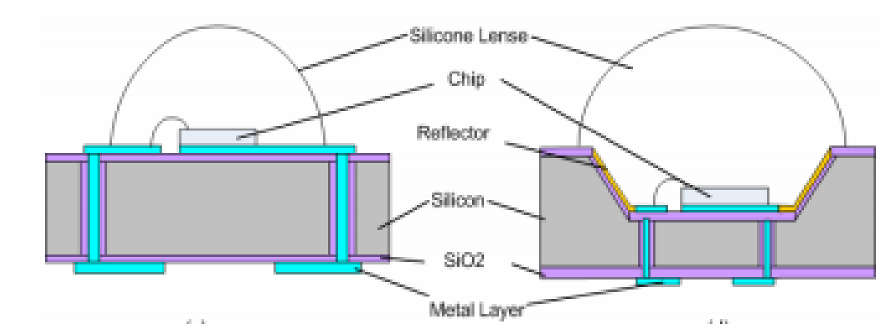

Figure 1.3 LED packaging on Silicon platform

Since, SSL system is essentially a microelectronic system with semiconductor components like diodes, driver IC's required of powering the LED chip; a silicon platform for LED chip packaging allows a great possibility of integration of semiconductor devices along with the LED chip for a complete wafer level integration of SSL system. The wafer level packaging on silicon discussed in Fig 1.2 is rigid and two-dimensional. A 3D form factor for wafer level packaging of LED can be achieved by using flexible interconnect technology as discussed in [10] .The flexible interconnect technology consists of aluminum layer sandwiched between two spin layers of polyimide material. An example of aluminum interconnect embedded in polyimide substrate is shown in Figure 1.4 [10]

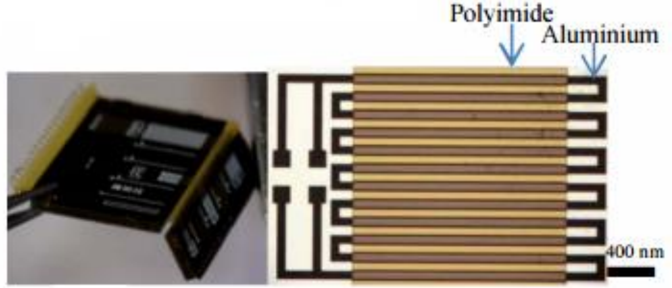

Figure 1.4 Rigid to Flex interconnect technology

A combination of silicon wafer level packaging using flexible interconnect and integration of power converters ,drivers and sensors on chip to form a single system in a package offers great potential for smart miniaturized SSL system.

The main challenge using silicon as the substrate material for integration is that the breakdown voltage for silicon is less than 100V [11]. Hence, silicon as substrate material cannot be used for high power lighting application. The power converters and driver electrical circuit for the LED require large storage capacitors. These are used as discrete components on PCB. The electrolytic capacitors are mainly used as the storage capacitors. They are bulky and occupy a lot of space. Another challenge with silicon as the substrate is the integration of capacitors in silicon to match the storage capacity of electrolytic capacitor.

By considering the above drawbacks of silicon, the design considerations have to be made to know about the components that can be integrated on chip and off chip. For low voltage applications, silicon as substrate material offers a great potential for monolithic integration of rectifiers and drivers. But passive components such as capacitors, inductors and high watt resistors provide huge challenges to be integrated on-chip. These components have to be off chip components.

In order to study the feasibility of integration of power converters and drivers using silicon as the substrate material, we consider a low power LED module – for example a G4 retrofit LED capsule. A breakout of the G4 capsule is shown in Figure 1.5 [12]. The PCB consists of discrete components such as diodes, electrolytic capacitor and driver IC. The research

focus of the thesis project is to build a integrated rectifier and driver on chip to reduce system cost and PCB space.

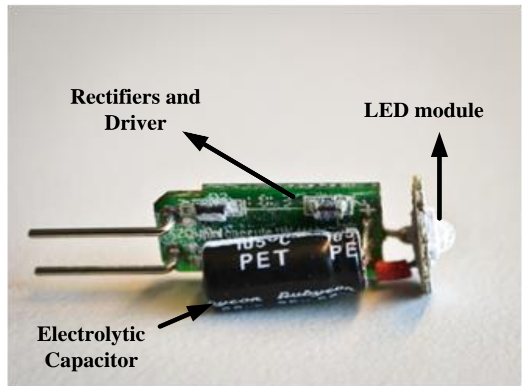

Figure 1.5 G4 LED Capsule

1.3 Design and Thesis focus

In this thesis, a proof of concept for monolithic integration of rectifiers and drivers in a standard BiCMOS7 for low power LED system is investigated. In this section, the electrical requirements of G4 retrofit LED capsule and design proposal for integration of the rectifiers and drivers on a rigid to flex substrate is presented.

1.3.1 Electrical specifications for G4 retrofit LED capsule

The G4 LED capsule is a 2.5W that can provide a lumen output of 100lumen. The input voltage requirement of G4 LED capsule is 12V AC. The G4 module uses a single LED for light output. Considering these specification for a low power LED system, the basic block diagram of this system is shown in Figure 1.6. The input 12V AC is first converted into DC by a bridge rectifier. The bridge rectifier uses schottky diodes due to their low forward voltage drop and high current conduction.

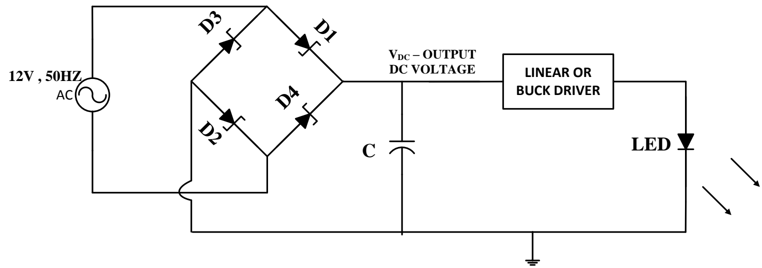

Figure 1.6 Schematic of a low power 12V LED system

During the positive half cycle of ac input voltage diodes D1 and D2 are forward biased. The current flows from diode D1, the capacitor C and LED load. During the negative half cycle the diodes D3 and D4 are forward biased and current flows through D3, D4, capacitor C and the LED load. Since two diodes are in series when forward biased, the output voltage V_{dc} will be lower than the input voltage by two voltage drops of the diode. If we consider ideal schottky diodes with forward voltage drop of 0.4V, then for a 12V input ac voltage the output dc voltage will have a maximum voltage of 11.2V. The important parameter for the bridge rectifier is the peak inverse voltage (PIV) rating. The peak inverse voltage is the maximum voltage across the diode during the reverse bias condition. It is given by [13],

$$PIV = V_m \tag{1.1}$$

Where,

V_m – Peak AC input voltage

For an AC input voltage of 12V, Vm = 16.97 volts. Hence the peak inverse voltage of the bridge rectifier in Fig 1.6 is PIV = 16.97V. The schottky diodes must have a breakdown voltage that is greater than 16.97V to block the AC voltage during negative half cycle. A breakdown voltage of 40V is desired for schottky diodes in this configuration. The commercial available schottky diodes used for rectifier circuit have vertical device structure with a top anode contact and bottom cathode contact as shown in Figure 1.7[11] . With the vertical structure it is difficult to integrate in a planar standard BiCMOS process. An example of planar structure of schottky diodes is shown in Figure 1.8[14]. The current flow laterally in this device is from schottky contact to the ohmic contact. This structure provides a great potential for integrating the rectifiers using schottky diodes in a planar standard BiCMOS. In this thesis, a detailed study on the design and fabrication of high current and high breakdown schottky diodes in standard BiCMOS process suitable for low voltage integrated rectifiers is presented.

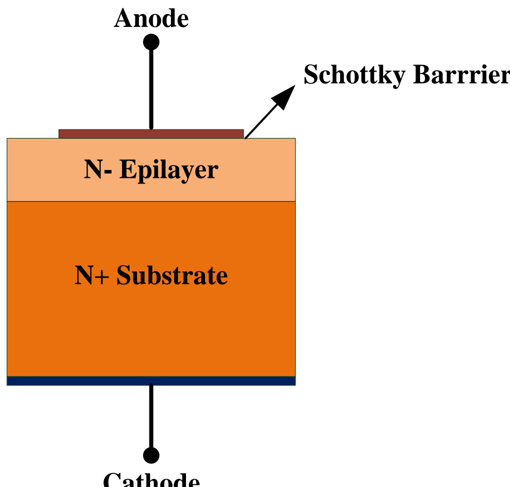

Figure 1.7 Vertical power schottky diode

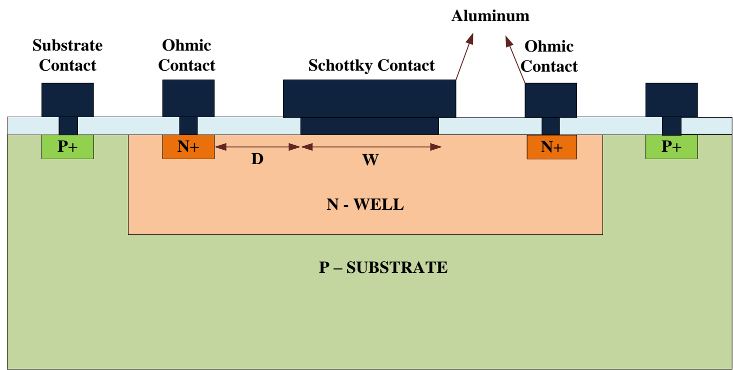

Figure 1.8 Schottky diode structure in Standard CMOS process

The two methods to maintain constant current in a LED are by using a linear driver or a switch mode driver. The linear current driver is cost effective but it has poor efficiency. A basic circuit for linear constant current driver for LED is shown in Figure 1.9 and Figure 1.10[15].

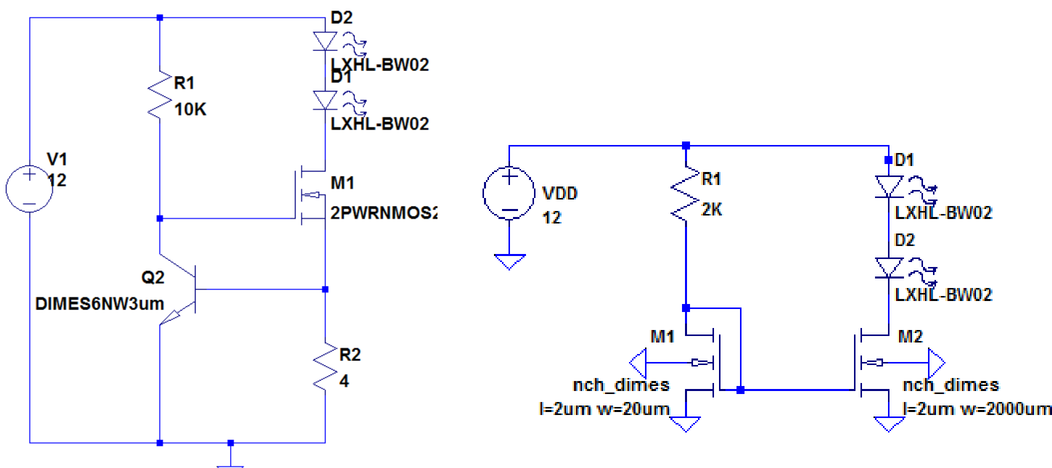

Figure 1.9 Linear driver circuit example **Figure 1.10 Current mirror linear driver**

The current in the circuit in Figure 1.9 is set by the resistor R2.The NMOS is on when the voltage at R1 is greater than the threshold voltage of the NMOS. The transistor Q2 turns on with base emitter voltage Vbe of the transistor set by voltage drop across R2 that should be less than 600mV. The transistor Q2 turns on it pulls down the voltage at the gate of the NMOS causing the MOSFET to go into linear region and limits the current in the circuit. In the Figure 1.10 ,the circuit for the linear driver is a constant current mirror of nmos devices. The current through the LED's is set by the resistor R1. The current in the LED branch is set by the ratios of the width of the NMOS M1 and M2.

In a switch mode regulator configuration, the switch basically mosfets takes a small portion of energy for a given time from the input voltage source and transfers it to the driven load [16].

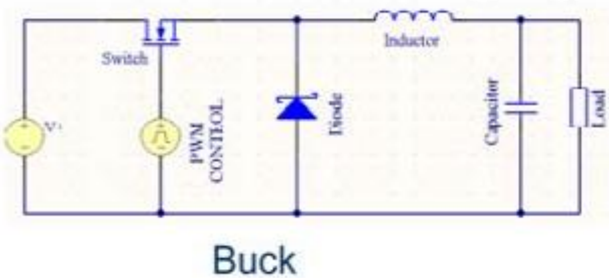

Figure 1.11 Schematic of Buck driver topology

The switch mode driver is more efficient in power conversion than linear drivers. A simple circuit of a buck driver is shown in Figure 1.11.In the switch mode driver the main components that controls the switching function is the PWM controller. When the switch is closed the mosfets is on and the current flows through the inductor and the load while the diode is reverse biased. When the switch is open, the energy stored in the inductor provides the current path through the diode which is forward biased. At the output of the load instead of square voltage only a ripple voltage will be seen[16]. The integration of switch mode driver on chip is difficult due to the presence of inductor and capacitor components in the circuit. A basic explanation of the rectifiers and drivers are discussed in this section. The on chip components that can be integrated will include power mosfets, schottky diodes and PWM control IC. The output voltage of a buck driver is given by,

$$V_{out} = V_{in} \frac{T_{ON}}{T} \tag{1.2}$$

where,

V_{in} – input DC voltage

T_{on} – Duty cycle of the PWM control

One of the basic topology of the PWM control for the buck driver is discussed in paper [17]. The circuit is shown in Figure 1.12. This circuit consists of an error amplifier and a PWM generator for controlling the power mosfets. This circuit uses the sense resistor to apply feedback for the PWM control. If the value of the sense resistor voltage is greater than the reference voltage, the output of the error amplifier is negative and the PWM control is adjusted so that the voltage across the sense resistor increases and the error amplifier output attains a positive value.
The PWM amplifier uses a saw tooth waveform to generate a pulse output based on the output of the error amplifier and the compensation network of R and C.

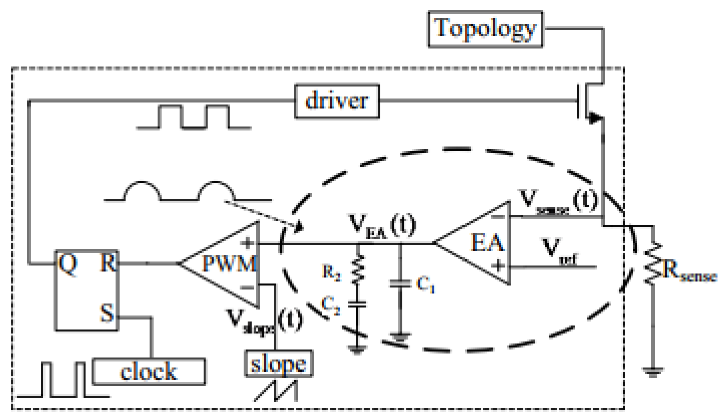

Figure 1.12 Schematic of average current control buck driver

This thesis does not focus on the implementation of PWM control but provides a basic design of buck driver circuit in which a ring oscillator controller is used for switching the power mosfets.. The ring oscillator has a duty cycle of 50% which provides an output voltage which is equal to half the input DC voltage.

1.3.2 Design proposal

In this thesis, monolithic integrated of bridge rectifiers using schottky diodes are designed, fabricated in BiCMOS7 process. BiCMOS7 is a semiconductor fabrication process in which diodes, transistors and mosfets are fabricated in a planar process on a single substrate. The DIMES BiCMOS7 process is simple, low cost 7 mask process to fabricate the devices. The schottky diodes fabricated in standard planar process have a breakdown of about 27V .The fabricated chip in this process with rectifiers using schottky diode are shown in Figure 1.13.

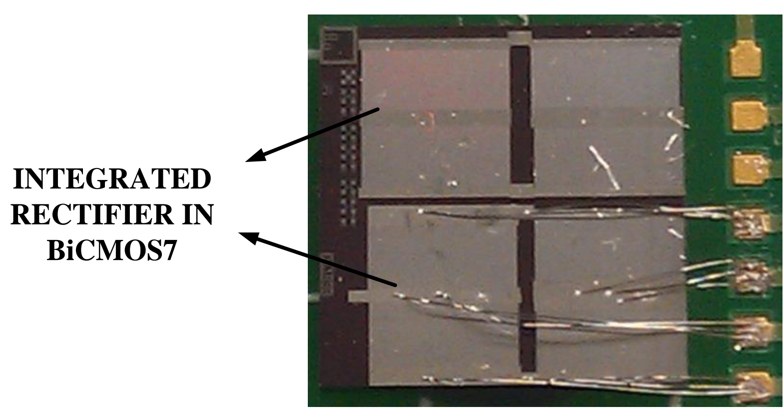

Figure 1.13 Fabricated Integrated rectifiers chip in BiCMOS7

The integrated rectifier has a dimension of 3mm by 3mm. The schottky diodes are optimized for high breakdown and high current conduction as discussed in detail in chapter 2 of the thesis. Using the same BiCMOS7 process in which the schottky diodes and rectifiers are fabricated, a design proposal for integrating both rectifiers and driver on a rigid to flex substrate is proposed. A 3D illustration of retrofit G4 module is shown in Figure 1.14. In this module, the on chip components include monolithic integrated rectifiers and drivers and the off-chip components include capacitors and inductors. The flexible interconnect allows a 3D form factor design and integration of more than one LED chip. This offers advantage of both monolithic integration of devices and 3D wafer level packaging of LED module using silicon as the substrate.

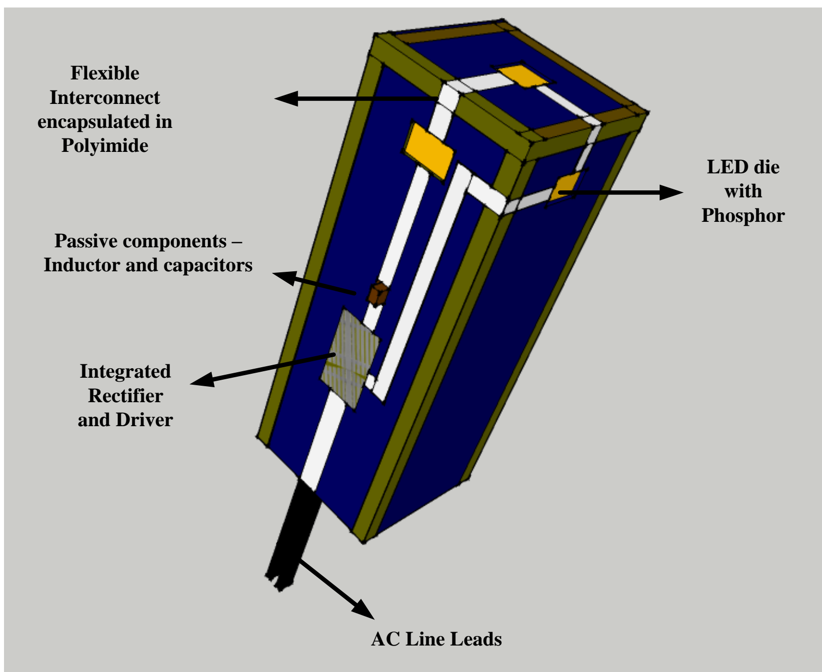

Figure 1.14 3D model of monolithically integrated rectifiers and drivers on to Flex-to-rigid substrate.

For the integration of schottky diodes, rectifiers a systematic design flow is followed in the thesis. The design flow and the related tools used in the process is shown in Figure 1.15. An analytical model of schottky diode in standard BiCMOS process is done and compared with the model of a conventional schottky diode in this step. This study gives us an understanding of the process and layout design required for achieving the specification of high current conduction and high breakdown voltage schottky diode. In the next step this analytical model is verified by simulations using TCAD software TSUPREM4 and MEDICI. This provides guidance for simulating the process and device models that allow us to predict the process parameters that would be required during fabrication of the devices. The next step is the electrical characterization of the schottky diodes. The measurements are done using cascade probe station with ICCAP software. A spice model is extracted from the measurement data for circuit analysis.

In the same measurement procedure, characterization of BJT and NMOS devices of the various wafers are done to extract the spice parameters.

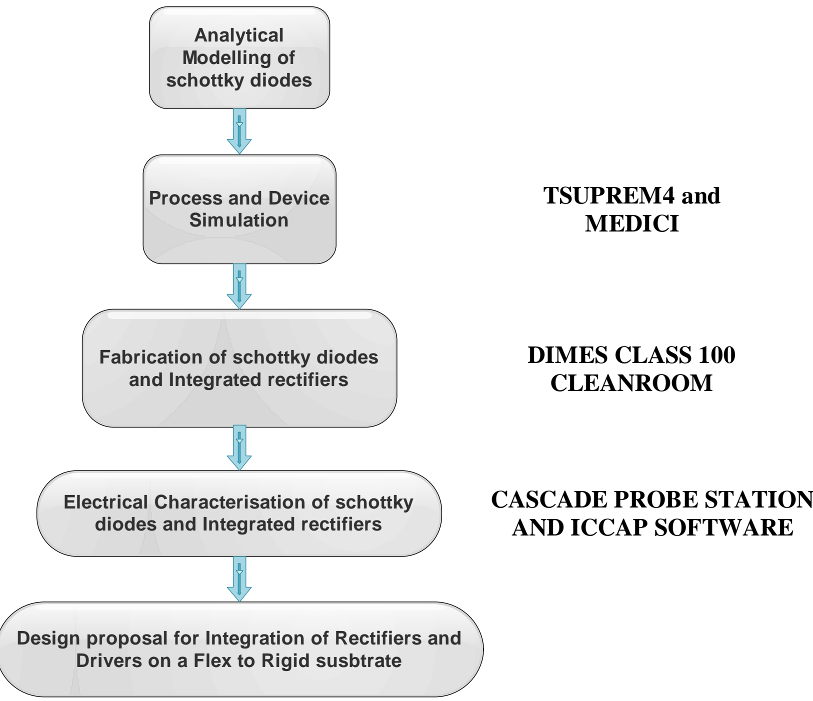

Figure 1.15 Design Flow

Using the spice models extracted from the software, electrical circuit analysis is done for the basic linear and buck driver circuits. A design proposal is presented for integration of rectifiers and drivers on a Flex to Rigid substrate. This design steps allows us to check and iterate at each step to optimize the design for future process.

The key research goals of this thesis topic are,

- Develop an analytical model for designing schottky diodes in standard BiCMOS process for achieving high current conduction and high breakdown
- Process and Device Modeling of schottky diode in BiCMOS process to deduce a set of design parameters.
- To provide a complete methodology for electrical characterization and modeling of schottky diodes, NPN bipolar transistors and MOS devices.
- Analyze the driver circuits that can be integrated in this process.
- To provide a design proposal for integrating rectifiers and drivers on rigid to flex substrate

Since designing an SSL system is similar to designing a microelectronic system, for an in- depth design analysis it becomes essential to know the concepts from device processing to circuit analysis and packaging and integration for the system development. A design cycle for building a wafer level integrated SSL system with G4 capsule as an example is illustrated shown in Figure 1.16.

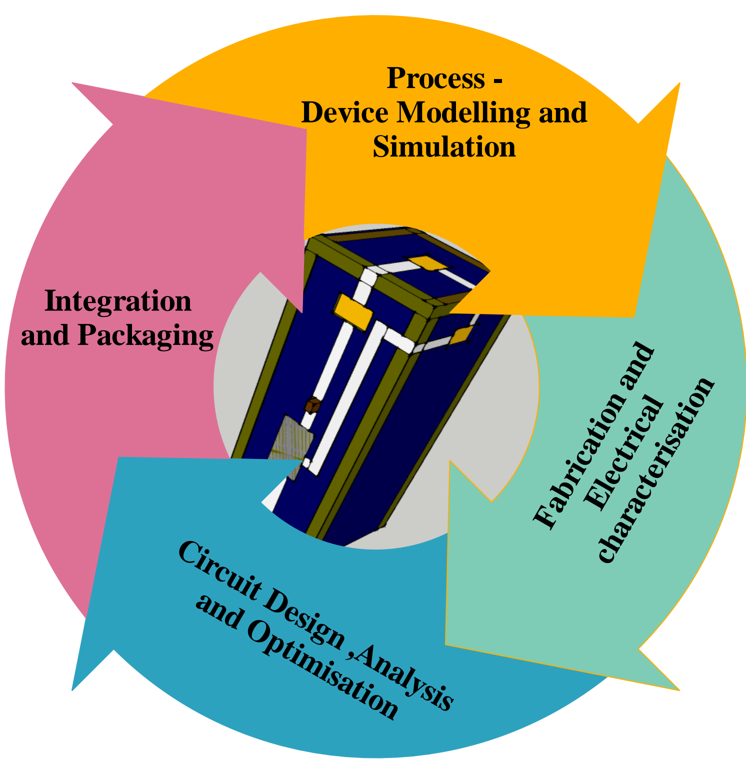

Figure 1.16 Design cycle for Wafer level integration of G4 module

A robust process and device modeling of the devices intended for integration on chip must be done. The devices are then fabricated and characterized. With the device models extracted from the measurement data, circuit analysis is done for integrating higher level circuits. Silicon wafer level packaging for LED dies and flexible interconnects for electrical connection is designed. The design concepts are tested for reliability and optimized in the next development cycle.

1.4 Thesis Outline

In this thesis, monolithically integrated rectifiers is designed, fabricated in BiCMOS7 process and characterized. The thesis organization is discussed below,

In Chapter 2 a detailed analytical modeling for schottky diode in standard BiCMOS process is presented. Process and device modeling is done using TCAD simulation software like TSUPREM4 and MEDICI.

In Chapter 3 the fabrication process steps of schottky diodes and rectifiers in BiCMOS is presented. The schottky diodes are characterized and a spice model is extracted from the measurement data. A spice model is also extracted for NPN Bipolar transistor and NMOS devices fabricated in the same process.

In Chapter 4 the characterization of integrated rectifiers is discussed. A circuit analysis basic linear and buck driver from the spice model extracted is analyzed. A design proposal for integration of rectifiers and drivers on flex to rigid substrate is presented.

In Chapter 5, the conclusions of the thesis and future work recommendations are provided.

Chapter 2

Process and Device Modeling

This chapter deals with process and device modeling of schottky diodes used in the design of integrated full wave bridge rectifiers. First conventional schottky diode characteristics and working is discussed. The factors affecting forward current conduction and breakdown of the schottky diodes are explained. The working principle of vertical and planar schottky diode structure is discussed. The process and device simulation for schottky diode in BiCMOS7 process is done in Tsuprem4 and device simulation in Medici. Finally, the design parameters for schottky diodes in DIMES standard BiCMOS7 are derived based on these modeling results.

2.1 Schottky diodes

The current transfer to external components from a semiconductor device can be achieved by two ways namely ohmic contact and schottky contact. Ohmic contacts are non-rectifying metal semiconductor junction with low-resistance providing current conduction in both directions. Ohmic contacts are made by sputtering or evaporating metal on highly doped p+ or n+ region. Schottky junction or schottky barrier diode contain a metal semiconductor junction with rectifying characteristics i.e. they allow current to flow only in forward biasing condition [18]. Schottky contacts are mostly made by sputtering or evaporating metal directly on low doped n– type semiconductor. Schottky diodes are unipolar semiconductor devices.

In order to understand the working principle of schottky barrier diode, let us consider the band diagram of metal and the semiconductor before and after contact. The energy band diagram of the metal and semiconductor before contact as discussed in [18] is shown in Figure 2.1. The vacuum energy level given by E_v is the energy level where the electron is essentially free from the metal. ϕ_m is the metal work function defined as energy required in removing an electron from metal to vacuum level and ϕ_n is the n-type semiconductor work function defined as the

energy required in removing an electron from semiconductor to the vacuum level. In the Figure 2.1, the situation of $\phi_n > \phi_s$ is considered and Fermi level of semiconductor is above the Fermi level of the metal. When metal is brought in contact with semiconductor electrons will flow from semiconductor to lower energy states in the metal. At the interface of the metal-semiconductor the positively charged donor atoms create a space charge region and Fermi level become constant through the system as shown in Figure 2.2

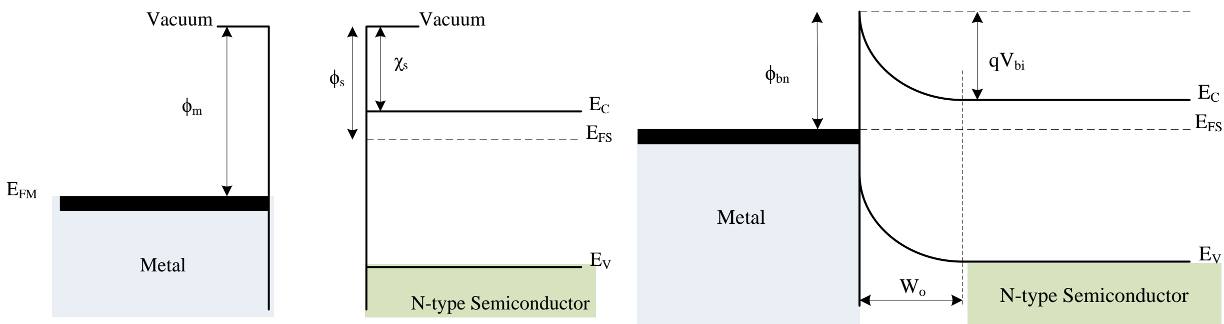

Figure 2.1 Energy Band Diagram before metal contact

Figure 2.2 Energy Band Diagram after metal contact

At the interface, the electrons moving from the metal to the semiconductor see a potential barrier of ϕ_{bn}. This barrier is called the schottky barrier [18] and it is given by,

$$\phi_{bn} = (\phi_m - \chi) \tag{1}$$

where :

ϕ_m = metal work function of the metal,

χ = electron affinity of the semiconductor

Next the electrons from the conduction band of the semiconductor moving into the metal see a barrier given as built-in potential barrier V_{bi}. This is given by,

$$V_{bi} = (\phi_{bn} - \phi_n) \tag{2}$$

where :

ϕ_n = work function of n-type semiconductor

ϕ_n is given as,

$$\phi_n = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right) \tag{3}$$

where :

N_c = effective density of states in conduction band,

N_d = donor impurity concentration

From Eq (1), it can be seen that the schottky barrier height ϕ_{bn} is dominantly dependent on the metal work function and the semiconductor in contact.

The current mechanism in schottky diodes is different from that of p-n junction diodes. The current in p-n junction diodes is mostly determined by the diffusion of majority and minority carriers across the depletion region in forward bias. In schottky diodes the current mechanism is by thermionic emission of the majority carriers over the potential barrier. In p-n junction diode the turn on voltage is dependent on the doping concentrations. In comparison, turn-on voltage of schottky diode is a function of barrier height of the metal semiconductor contacts. It is always less than the turn on voltage of p-n junction diode [18]. Since schottky diode is a majority carrier device, there is no minority stored carrier charge in the reverse bias condition. Schottky diodes are used in high frequency applications as it is able to switch between the on and off states very fast. They are used in rectifiers in low power systems due to their low forward voltage drop and high forward currents. The disadvantage of schottky diodes is that they have lower breakdown and higher reverse leakage current than p-n junction diode.

A cross section of vertical power schottky diode is shown in Figure 2.3. The main difference between conventional schottky diode and power schottky diode is the presence of a thick layer of lightly doped N-type drift region. This drift region supports the reverse blocking voltage of schottky diode. The wafers used for fabricating are heavily doped N+ substrate. The lightly doped N-type drift region is grown on top of the N+ substrate handle by epitaxial process [11]. The doping concentration of this drift region determines the blocking voltage of the schottky diode which is discussed later. A layer of silicon-di-oxide with thickness of about 300nm is thermally grown on the semiconductor. The contact openings are patterned and the silicon surface is cleaned to remove the native SiO_2 on the surface. Al /1% Si or other contact metal like tungsten, platinum is sputtered and patterned. This forms the schottky contact to the semiconductor and it is the anode terminal of the schottky diode. The bottom of the semiconductor is highly doped with n+ to obtain ohmic contact. This is the cathode terminal of the diode. The equivalent circuit of the device can be represented as diode and series resistance or on-resistance (Ron). This resistance is the sum contribution of the drift region resistance, substrate resistance and ohmic contact resistance.

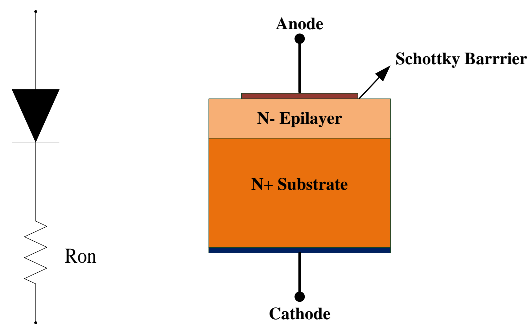

Figure 2.3 Cross section of Power Schottky Diode

2.1.1 Forward I-V Characteristics of Schottky Diodes

In this section the factors the forward voltage drop and current conduction is discussed. Under forward bias condition for schottky junctions on n-type semiconductor, the basic conduction mechanism as discussed in [18] is shown in Figure 2.4. They are described below,

1. Thermionic emission (A): Transport of electrons from the conduction band over the schottky barrier into the metal.
2. Electrons close to the barrier tunnel through the barrier (B).
3. Generation and Recombination of electrons and holes in the depletion region (C).
4. Hole injection into the neutral region of the semiconductor (D).

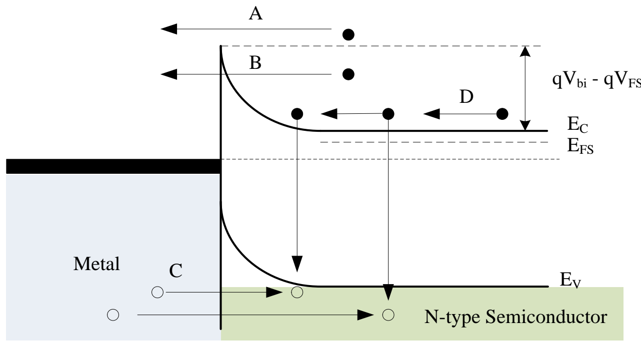

Figure 2.4 Schottky diode current transport mechanism in Forward Bias

The schottky diode forward I-V characteristics are mostly determined by thermionic emission (A) described in Figure 2.4. The forward current equation for schottky diode is given by [18],

$$
\begin{aligned}
I &= AJ_F \\
&= AJ_S[\mathrm{e}^{(qV_a/kT)} - 1] \\
&= AA^*T^2\mathrm{e}^{-(q\phi_{bn}/kT)}[\mathrm{e}^{(qV_a/kT)} - 1]
\end{aligned}
\tag{4}
$$

where :

A = active area of schottky contact,

J_F = forward current density [A/cm^2],

J_S = $A^*T^2\mathrm{e}^{-(q\phi_{bn}/kT)}$ = reverse saturation current density [A/cm^2],

A^* = effective Richardson constant for thermionic emission,

V_a = forward voltage drop across schottky contact.

The on-state voltage drop V_F of the power schottky diode depends on voltage drop across the schottky junction, ohmic voltage drop in the drift region, substrate and ohmic contact. For a given forward current density J_F it is given by [11],

$$V_F = V_{SCHOTTKY} + V_R = \frac{kT}{q}\ln\left(\frac{J_F}{A^*T^2}\right) + \phi_{bn} + R_{ON}J_F \tag{5}$$

where :

R_{ON} = total series-specific on resistance

From Eq (5), the main components that affect on-state voltage drop of the schottky diode are the schottky barrier height ϕ_{bn} and specific on-resistance.

The total series specific on resistance R_{ON} of the schottky diode is the resistance of the schottky diode under saturated forward bias condition. It is the sum of epitaxial drift layer, the substrate resistance and the contact resistance of anode and cathode. It is given by [11],

$$R_{ON} = R_{DRIFT} + R_{SUB} + R_{CNT} \tag{6}$$

Since the drift region is lightly doped N-type semiconductor, it is the dominant factor of the total specific on resistance when compared to the highly doped N+ substrate and contact resistance. The resistance of the drift region is determined by epitaxial layer thickness (t_{epi}), doping concentration (N_d) and electron mobility (μ_n) [19] given by,

$$R_{ON} \cong R_{DRIFT} = \frac{t_{epi}}{q\mu_n N_d} \qquad [\ \Omega\text{cm}^2\ ] \tag{7}$$

From Eq (7), the total on-resistance approximated to drift region resistance is inversely proportional to the doping concentration in the drift region for a given epitaxial layer thickness. The dependency of doping concentration and the drift resistance is shown below in Figure 2.5.

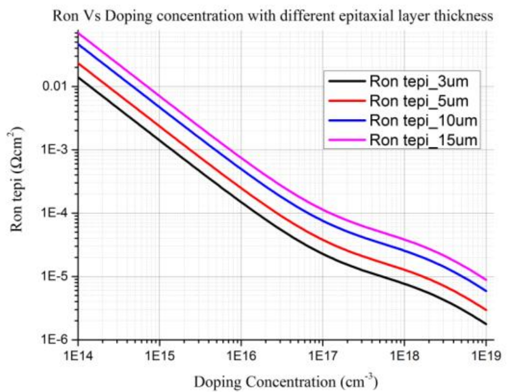

Figure 2.5 RON v/s Doping concentrations for different epitaxial layer thickness

The thickness of the epitaxial layer and the doping concentration is an important design parameter for the forward voltage drop. As seen from Figure 2.5 a higher doping concentration reduces the on resistance of the drift region and thus the on-state voltage drop of the diode.

The next significant design parameter as per Eq (5) affecting the forward voltage drop is schottky barrier height. The schottky barrier height is a function of the metal work function as seen in Eq(1) earlier. A lower barrier height is needed to reduce the on-state voltage drop across the diode. The experimental determined value of schottky barrier height of various metals [11] is shown in Table 2.1 the effective Richardson's constant A^* for schottky contact with n-type semiconductor is given as 110 $Acm^{-2}K^{-2}$ [20] .Using Eq (4) and Eq (5), the forward voltage drop V_F for forward current $I_F =$ 1A is determined for different areas and schottky barrier heights in and illustrated in Figure 2.6. For lower on-resistance R_{ON} , consider a doping density of 10^{18} with epitaxial layer thickness of 3um which is calculated as $7.65 x 10^{-6} \Omega cm^2$.

Table 2.1 On-state forward voltage drop V_F for different metal contact and schottky area

Metal	Barrier Height (eV)	Schottky Contact Area (cm^2)	Current Density J_F at I_F = 1A (A/cm^2)	On state forward voltage drop V_F (V)
Al/1%Si	0.7	0.05 x 0.05	400	0.450
		0.1 x 0.1	100	0.413
		0.25 x 0.25	16	0.367
		0.5 x 0.5	4	0.331
WSi_2	0.65	0.05 x 0.05	400	0.403
		0.1 x 0.1	100	0.370
		0.25 x 0.25	16	0.320
		0.5 x 0.5	4	0.282
$MoSi_2$	0.55	0.05 x 0.05	400	0.303
		0.1 x 0.1	100	0.270
		0.25 x 0.25	16	0.225
		0.5 x 0.5	4	0.182
$PtSi_2$	0.78	0.05 x 0.05	400	0.533
		0.1 x 0.1	100	0.500
		0.25 x 0.25	16	0.450
		0.5 x 0.5	4	0.412

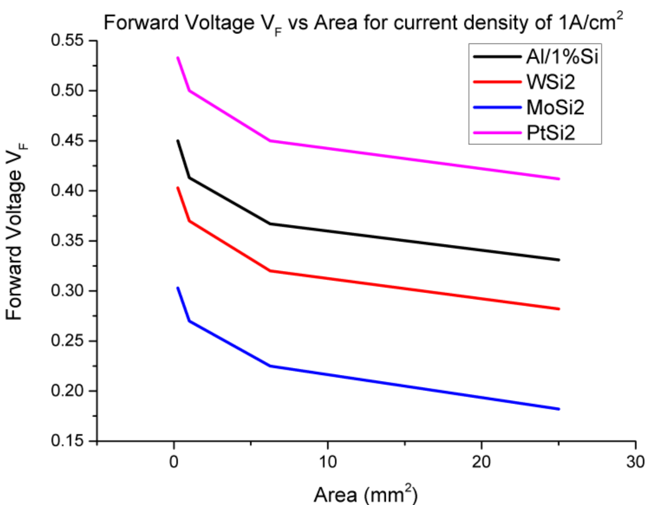

Figure 2.6 Forward Voltage V_F for various barrier height and area at J_F = 1A/cm^2

From the above analysis, the schottky metal contact with lower barrier provides a lower on state voltage drop. Increasing the area of the diode has a significant impact on the current conduction and the on state voltage drop. With large the area, the forward current density decreases and the on-state voltage drop decreases significantly. Considering a standard packaged schottky device dimension taken as $A = 2.5\text{mm} \times 2.5\text{mm} = 6.25\text{mm}^2$, schottky contacts using $MoSi_2$ or WSi_2 provides higher current conduction at lower on-state voltage drop.

In this section, the factors affecting the on-state voltage drop and current conduction was discussed. It can be seen that a higher doping of the drift region and lower schottky barrier metal provides a good design choice for the fabrication of low voltage high current schottky diodes. But using a highly doped drift region affects the breakdown performance of the schottky diode. This is discussed in the next section.

2.1.2 Analysis of Breakdown Voltage in Schottky Diodes

In schottky diodes, under reverse bias condition there is high electric field created in the interface of the metal contact and at the edges of the semiconductor metal contact. The large current flow with increasing reverse voltage is caused due to avalanche breakdown phenomena. In reverse bias, the electrons or holes that enter the depletion region due to diffusion or recombination are swept out by the electric field. With increasing reverse voltage, the depletion region electric field increases and the mobility of carriers is increased. These carriers collide with the lattice atoms and generate electron-hole pairs. This is referred as impact ionization which is a multiplicative process that generates more electron-hole pairs with increasing reverse voltage. The reverse current increases rapidly and the device breakdown at this condition. The critical electric field is dependent on the material and the doping concentration of the drift region. For

silicon the maximum critical electric field before breakdown is calculated to be $2.5 \text{ x } 10^5$ V/cm [11]. The dependency of critical electric field with doping concentration is it is given by,

$$E_{C,Si} = 4010 N_D^{1/8} \qquad (8)$$

where :
N_D = drift region doping concentration

The relation of breakdown voltage with doping concentration in the drift region is given by Eq (9). The breakdown voltage at the schottky junction is inversely proportional to the doping concentration of the drift region [11] N_D .

$$BV_{Si} = 5.34\text{x}10^{12} N_D^{-3/4} \qquad (9)$$

In the conventional schottky diode with increased reverse bias the depletion region at the schottky metal contact will expand both vertically and along the lateral direction. The electric field converges at the edge of the contact and it is maximum at the edge. The breakdown is mostly due to edge effect [21]. The high concentration of the electric field will give rise to increased reverse leakage current. This causes premature breakdown of the schottky diodes. The electric field distribution under large reverse bias modeled in COMSOL is shown in Figure 2.7 (Electric field range $0.5\text{x}10^5$ V/cm [blue] to $3.8\text{x}10^5$ V/cm [red]). The substrate is highly doped N+ layer with a doping concentration of 10^{19}cm^{-3} . The epitaxial drift layer has a doping concentration of 10^{16}cm^{-3} .At the edges the electric field is about $3.8\text{x}10^5$V/cm whereas at the metal interface it is around $0.5\text{x}10^5$V/cm. The electric field at the metal interface is still less than critical breakdown for Si ($2.5\text{x}10^5$ V/cm) but at the metal edges it has crossed this critical field value. This causes soft breakdown at the edges of the schottky diodes.

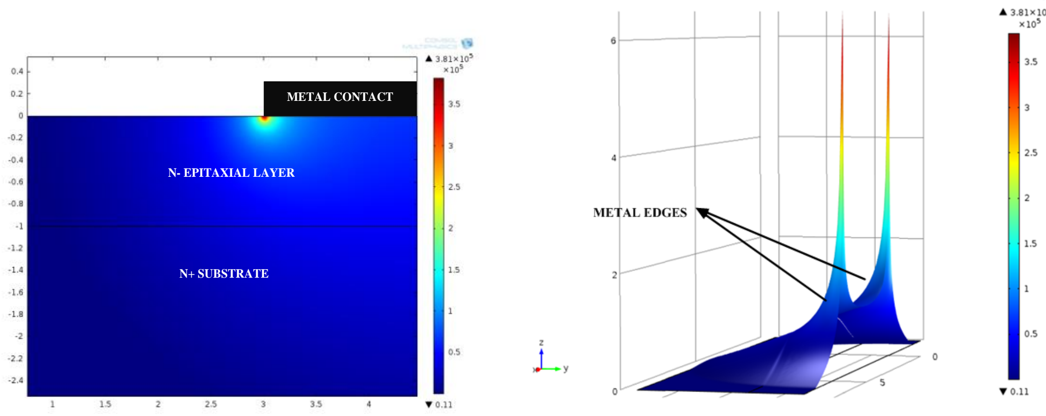

Figure 2.7 Electric Field at reverse bias voltage of 100V

From the analysis of forward conduction and breakdown voltage in schottky diodes it can be seen that for design the schottky diode the following cases is considered,

1. A lower doping concentration and thicker epitaxial drift layer is important for high breakdown voltage.
2. A higher doping concentration, thinner epitaxial drift layer, schottky metal with lower barrier height and large area device is important for lower on resistance, lower turn-on voltage and higher current conduction.

The above choice of design parameters of doping concentration, breakdown voltage and thickness of epitaxial layer is dependent on the application of the schottky diodes.

To improve the reverse breakdown voltage of the schottky diode many edge termination techniques are used. These are employed in Junction Barrier Schottky (JBS) diode which is explained in the next section.

2.1.3 Junction Barrier Schottky Diodes

One of the main disadvantages of Schottky diodes are high reverse leakage current and lower breakdown. From the analysis of electric field and breakdown voltage in the previous section it can be seen that the breakdown voltage is predominantly determined by high electric field at the edges of the schottky metal contact. There are many methods employed to reduce the electric field at the edges of the schottky contact. In Junction barrier Schottky diode, a p+ guard ring is incorporated at the edges of the schottky metal contact junction in the n-type epitaxial drift layer [22, 23]. The cross-section of a Junction barrier schottky diode is shown in Figure 2.8. The equivalent circuit of this structure has schottky diode in parallel with a p-n junction. In forward bias, the forward voltage drop is defined by the voltage drop of the schottky diode.

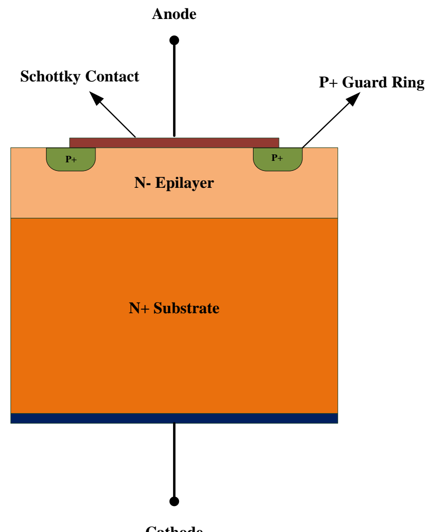

Figure 2.8 Cross section of Junction Barrier Schottky diode

In reverse bias condition, the p+ junction depletion layer expands and a potential barrier is created at the schottky metal edge. This prevents the schottky barrier lowering and increase of reverse saturation current. The reverse blocking voltage of the schottky diode can be increased by this method. The p+ guarding is fabricated by argon or boron implantation

The forward conduction of the JBS diode is modified by the addition of the p+ guard ring. The series resistance is affected by the presence of the junction grid. The JBS show higher on state forward voltage drop when compared to conventional schottky diodes. But the reverse blocking voltage is increased by this structure.

The concepts of forward conduction and reverse conduction of conventional schottky diodes are discussed in this section. In the next section we discuss implementing the schottky diode in DIMES BiCMOS process.

2.2 Schottky diodes in BiCMOS process

Conventional schottky diodes and junction barrier power schottky diode are fabricated as vertical structure with top anode contact and bottom cathode contact. These are the general packaged diodes available as commercial off the shelf components. The disadvantage of these power schottky diodes having vertical structure is that it cannot be integrated monolithically with other integrated circuit components in a standard BiCMOS process. In this thesis project the requirement of a schottky diode with a breakdown voltage of 40V is desired. The schottky diodes fabricated in standard CMOS process forms the basic component of integrated low voltage full wave bridge rectifier circuit for powering the driver and LED. In this section we discuss the factors affecting the current conduction and breakdown voltage of schottky diodes in standard BiCMOS process. The current and breakdown mechanism in the planar schottky diode follow similar behavior as the vertical structure of the schottky diode discussed in the previous section.

2.2.1 Forward characteristics of Schottky diodes in BiCMOS process

In the vertical structure of power schottky diodes there is a wide choice of metal like aluminum, platinum, tungsten that can be used in the fabrication process. But in the fabrication of planar schottky diodes in a standard BiCMOS process, the choice of metal for the schottky contact is limited. In this process, aluminum is the metal used for the schottky contact. The next difference between the vertical schottky diode and the planar schottky diode is the n-type region of schottky contact. In vertical schottky diode the schottky metal is in contact with a lightly doped n-type drift layer. In the planar process, the schottky metal is in contact with moderately doped n-type layer obtained by N-Well diffusion process. The anode contact of the schottky diode is made with the n-well region and the cathode ohmic contact is with a heavily doped n+ layer [14, 24]. A cross-section of planar schottky diode is shown in Figure 2.9 .

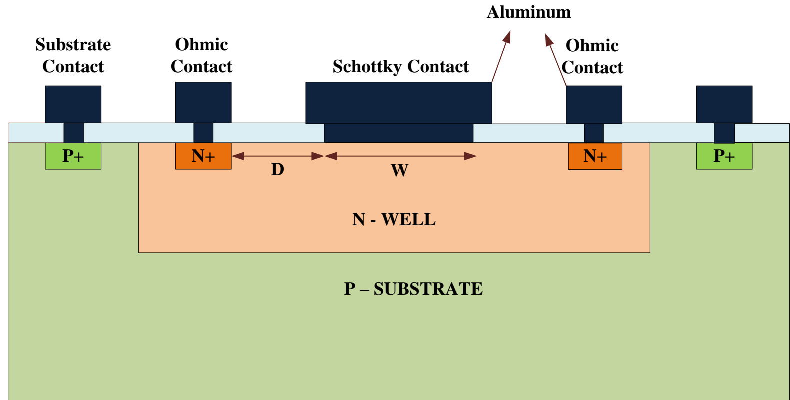

Figure 2.9 Cross section of Planar Schottky Diode device

The schottky contact area shown in Figure 2.10 is given as (W x L) where width W is the width of the schottky diode and L is the length of the schottky diode. The distance between the schottky contact and ohmic contact is defined with D. The drift region in this case is the lightly doped N-Well region. The current conduction in planar schottky diode is in the lateral direction from anode schottky contact to the cathode ohmic contact .When the anode terminal of the schottky diode is forward biased by applying a negative bias voltage, the electrons cross over the schottky barrier by thermionic emission move towards the cathode ohmic contact though the n-well region .The current under forward bias is given by the general schottky diode current equation as [24],

$$I = AA^{*}T^{2}e^{-(q\phi_{bn}/kT)}[e^{(qV_a/kT)} - 1] \tag{10}$$

where :
A = schottky contact area defined by (W x L)

The current conduction of schottky diode described in Eq (10) follows similar mechanism of vertical schottky diode as explained before in section 2.1 of this chapter. The main factors for the consideration of current conduction are discussed below,

1. Schottky barrier height ϕ_{bn} – In this process the schottky barrier height is defined by the aluminum metal in contact and hence it is a constrained value.
2. Area of the schottky diode A – The area parameter of the schottky diode is directly proportional to the current as seen in Eq (10).
3. Specific series on resistance R_{ON} – This is the sum of resistance in the current path from schottky contact to ohmic contact. This component plays a significant role to determine the on-state voltage drop of the schottky diode.

The total specific series on-resistance R_{ON} modeled by resistor components for the planar schottky diode is shown in Figure 2.10[25]. It is given as,

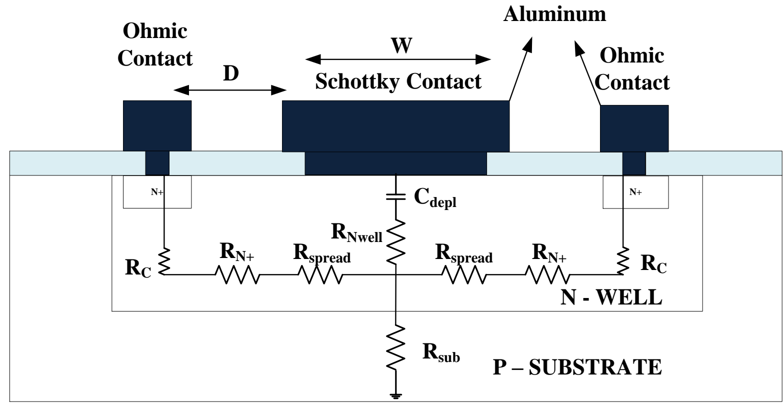

Figure 2.10 Components of series resistance in Planar Schottky Diode

$$R_{ON}=R_{nwell}+R_{Spread}+R_{N+}+R_{C} \qquad (11)$$

The resistance components in Eq (11) is discussed and analyzed. The first component R_{nwell} is the n-well resistance. This resistance is taken at 0V bias since the n-well will be un-depleted and the resistance at this bias maximum. It is given as [25],

$$R_{nwell}=\frac{1}{WL}\rho_{nwell}T_{nwell} \qquad (12)$$

where :

W = Width of the schottky contact,

L = Length of the schottky contact,

ρ_{nwell} = resistivity of n-well layer,

T_{nwell} = Thickness of un-depleted N-well layer,

The second component R_{Spread} is the spreading resistance defined as the resistance due to the current spreading under and around the anode metal contact of the schottky diode. It is given as [25],

$$R_{Spread}=\frac{1}{3}\frac{W}{4}\frac{1}{L}\rho_{nwell}T_{nwell} \qquad (13)$$

where :

W = Width of the schottky contact,

L = Length of the schottky contact,

ρ_{nwell} = resistivity of n-well layer,

T_{nwell} = Thickness of un-depleted N-well layer,

From Eq (12) and Eq (13), the n-well resistance and the spreading resistance is inversely proportional to length L of the schottky diode. These resistances can be minimized by increasing the length L of the schottky diode and keeping the width W as small as possible. The resistivity of n-well is inversely proportional to doping concentration. A higher doping concentration and a thinner n-well layer defined in the process can also contribute to reduce these resistances.

The third component is R_{N+} which is defined as the resistance in the current path due to the distance between the ohmic contact and the schottky contact. This distance is defined as D in the .Figure 2.10 R_{N+} is given by,

$$R_{N+} = \frac{1}{2}\frac{D}{L}\frac{\rho_{n+}}{T_{n+}} \quad (14)$$

where :

D = Separation between schottky contact and ohmic contact,

L = Length of the schottky contact,

ρ_{n+} = resistivity of n+ layer,

T_{n+} = Thickness of n+ layer

The reduction of R_{N+} can be achieved by decreasing the separation between the schottky contact D to as minimum as possible. This is layout dependent parameter limited by the lithography limit of the process. The last component R_C is the contact resistance due to the ohmic contact. It is given by,

$$R_C = \frac{1}{2L}\sqrt{\rho_C \frac{\rho_{n+}}{T_{n+}}} \quad (15)$$

where :

ρ_C = specific contact resistivity,

ρ_{n+} = resistivity of n+ layer,

T_{n+} = Thickness of n+ layer

The specific contact resistivity of Al /Si ohmic contacts[26] is in the range of 10^{-6} Ωcm^2 . Hence, the R_C can be reduced by increasing L.

Consider two diodes with same area with different perimeter. Diode A (square device) with L = 70µm, W = 70µm and Diode B (long device) with L = 245µm, W = 20µm. The n-well thickness is taken to be 3µm. Since the area is same the n-well resistance R_{nwell} is same. Let us

analyze the effect of doping concentration on the spread resistance R_{Spread} shown in Figure 2.11. Next the separation between the ohmic contact and the schottky contact is kept as close as possible from value of 2µm to 20µm. The effect on the total series resistance with respect to the separation between ohmic and schottky contact is shown in Figure 2.12 .

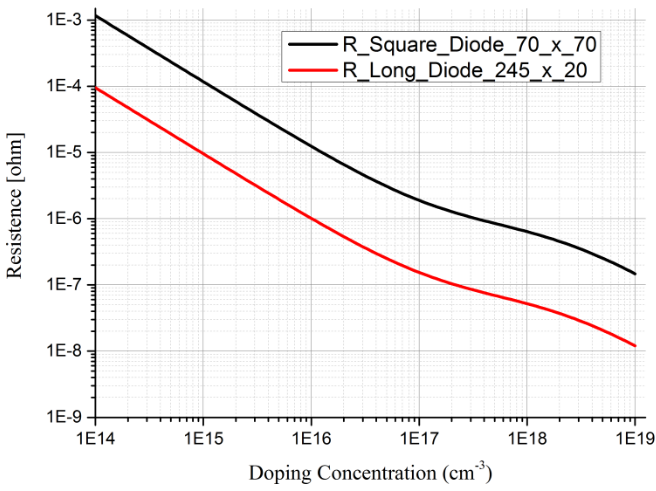

Figure 2.11 Spread Resistance RSPREAD vs. Doping concentration

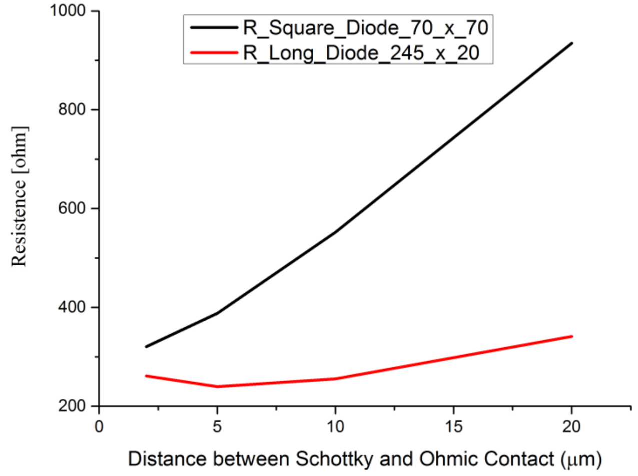

Figure 2.12 Resistance RN+ vs. distance between schottky and ohmic contact

From the above analysis of series resistance components, it can be seen that by increasing the length of the schottky contact L and decreasing the schottky width W with same diode area (long diode instead of a square diode) the total series specific on resistance R_{ON} can be reduced. This would provide us a lower on state voltage drop V_F for the schottky diode under forward bias condition.

In the schottky diode current equation Eq (10), the forward current conduction of schottky diode is directly proportional to the schottky contact area A. For higher current

conduction, the schottky contact area must be increased without increasing the series resistance. From the analysis of series resistance, it is evident that if we increase the area we need to design schottky diodes having long contacts and shorter width. The method for increasing schottky contact area keeping series resistance minimum is by designing the layout of the schottky and ohmic contacts in a finger structure [24] . The finger structure of schottky and ohmic contacts are placed alternate to each other as shown in Figure 2.14. A cross section comparison of square schottky diode and finger schottky diode is shown in Figure 2.13 and Figure 2.14.

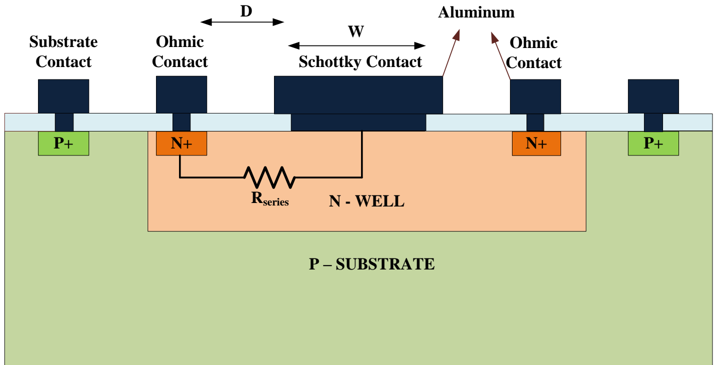

Figure 2.13 Planar Square Schottky diode device cross section

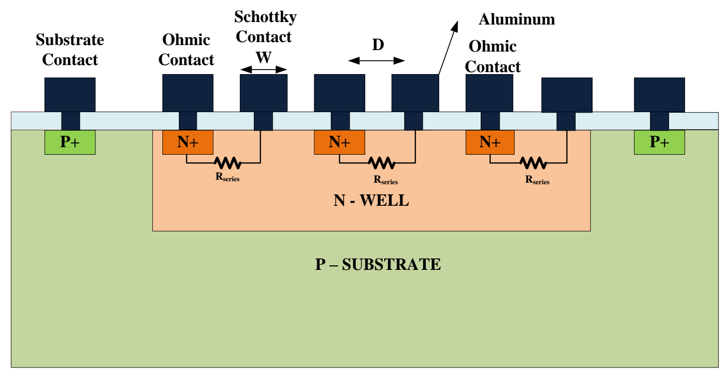

Figure 2.14 Planar finger structure schottky diode device cross section

By increasing diode size, the distance between the schottky contact and the ohmic contact increases. The resistance between the ohmic contact and schottky contact is high and hence lower current conduction. Another disadvantage of square schottky diode configuration is that the electrons under forward bias can be swept down to the substrate thereby reducing the current of the diode. With finger configuration of the layout the minimum distance between the schottky and ohmic contact will be the same. The schottky contact area can be increased by increasing the length of the schottky contact and the number of fingers. The total resistance in the finger design structure is the parallel combination of the total specific on resistance R_{ON} . This further reduces the series resistance of the device and increases the diode current conduction.

Although the schottky diode finger layout design having minimum distance between schottky contacts and ohmic contacts provide good benefits for high current conduction, it has adverse effects on the breakdown voltage of the schottky diode. It is analyzed in the next section.

2.2.2 Breakdown voltage analysis of Schottky diodes in BiCMOS process

In planar schottky diodes, under high reverse bias condition there is a large electric field build up at the edges of the schottky metal contact. This causes increase in reverse saturation current and premature breakdown of the schottky diodes. Figure 2.15 represents the critical electric field for silicon for different doping concentrations obtained from matlab using Eq (8). The critical electric field varies by a small factor with maximum electric field in the range of $2.5 \sim 3\text{x}10^5\ \text{V/cm}$.

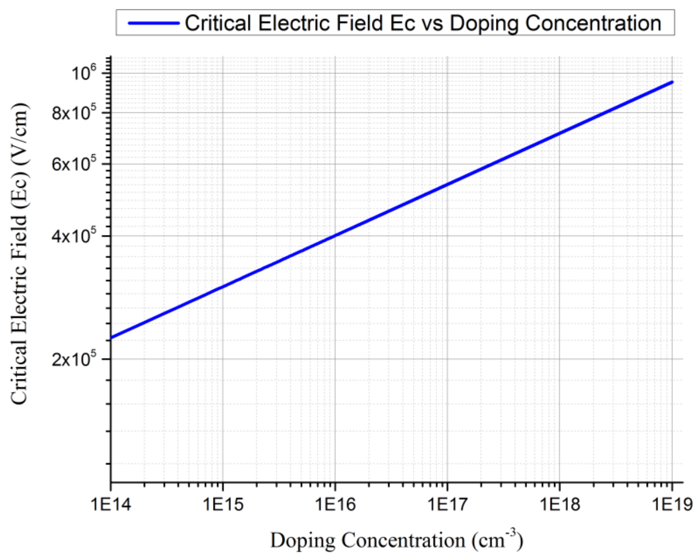

Figure 2.15 Critical Electric Field v/s Doping concentrations for Si Schottky diode

The increase of electric field at the schottky contact edges for planar schottky diodes at various increasing reverse bias condition for a planar schottky diode model built in COMSOL Multiphysics tool is shown below in Figure 2.16 with a reverse bias voltage of -10V and Figure 2.17 for the reverse bias voltage of -50V. The n-well concentration doping concentration used for the simulation is 10^{16} cm $^{-3}$. The electric field at the schottky interface and at the edge of the schottky contact increases with increasing reverse bias as shown in the two figures. The maximum electric field is obtained at the edge of the schottky contacts. It is about $0.6 \text{ x } 10^5$ V/cm for the reverse bias voltage of -10V and $2.23 \text{ x } 10^5$ V/cm for a reverse bias voltage of -50V. The theoretical maximum for a reverse bias voltage of 50V and a doping concentration of 10^{16} cm $^{-3}$is specified to be 4 x 10^5 V/cm. The schottky diode under this condition is at the edge of critical electric field and it occurs at the edges first than the metal

interface as shown in the two figures. The schottky diode must always be operated below the critical electric field values.

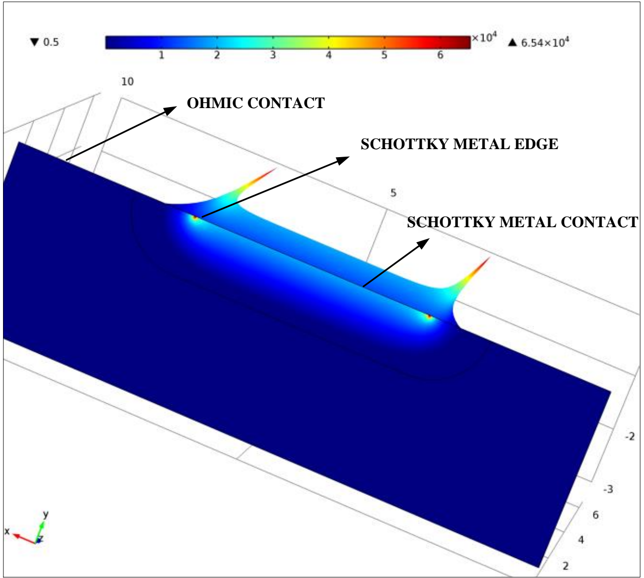

Figure 2.16 Field of Planar Schottky Diode at Reverse Bias of -10V

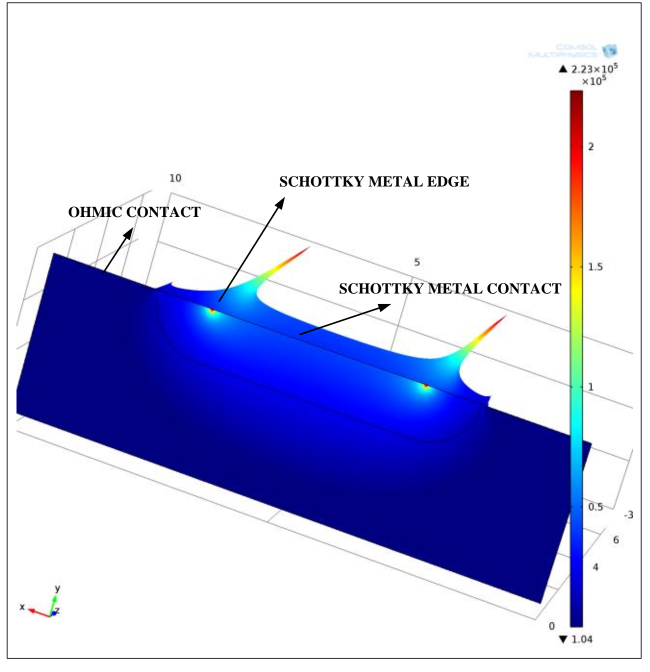

Figure 2.17 Electric Field of Planar Schottky Diode at Reverse Bias of -50V

The factor that also affects the breakdown voltage of planar schottky diode is the doping concentration of the n-well. In planar schottky diodes the drift layer is described by the n-well layer. It is governed by the same equation as described before for the vertical schottky diodes. It is given by [11],

$$BV_{Si} = 5.34x10^{12} N_D^{-3/4} \qquad (16)$$

where :

N_D = Doping concentration of n-well layer

A graph of the above relation obtained using matlab is shown in Figure 2.18. From this graph it is evident that for Si schottky diodes the n-well doping concentration of about 5 x 10^{15} - 10^{17} cm^{-3}, the breakdown obtained will be in the range of 10 – 100V.

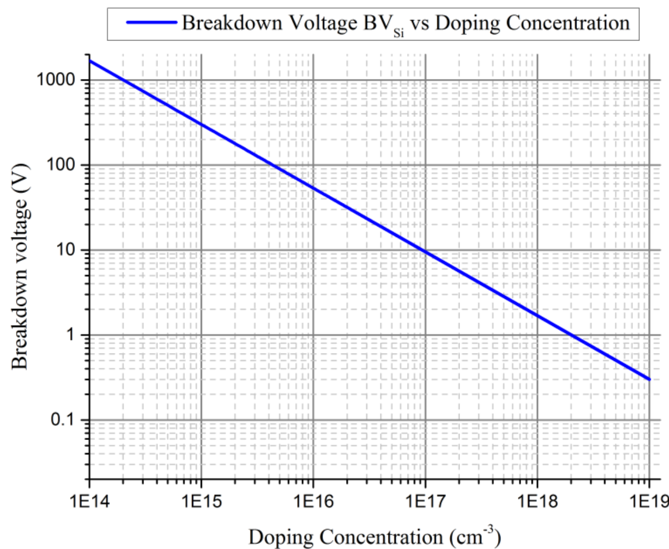

Figure 2.18 Breakdown voltage v/s Doping concentrations for Si Schottky diode

The n-well layer provides the foundation for the PMOS transistor and bipolar NPN transistor in BiCMOS fabrication process. For bipolar NPN transistor, a thinner and heavily doped n-well region offers lower collector resistance and higher current handling capability whereas a thicker and lightly doped collector region offers a higher collector-base breakdown voltage. In CMOS device, the n-well profile must be optimized for the PMOS. The lower n-well concentration provides lower source/drain capacitances [27]. Hence, the important process trade-off in integrating schottky diodes, bipolar transistor and CMOS in the same fabrication process involves the N-well profile dictated by the doping concentration and depth. In schottky diode, a n-well concentration of $10^{17} - 10^{18} cm^{-3}$ has the breakdown voltage in the range of 10V – 100V. So a lower bulk n-well doping concentration is preferred to achieve a higher breakdown.

From the electric field analysis it can be seen that the planar schottky diodes also have a similar problem of high electric filed at the edges as the vertical structure schottky diodes. Two commonly used methods for enhancing breakdown voltage are discussed below,

1. Layout modification :

The schottky junctions are usually made by using rectangular window in the contact opening mask. Metal is then deposited and patterned on these openings to form the schottky junction. The depletion region formed expands laterally under the oxide in the reverse bias condition. In the rectangular finger mask layout design shown in Figure 2.19. In this layout, a cylindrical junction is formed at the finger edges and a spherical junction formed at the corner of these fingers. There is a large increase in the electric field due to the presence of sharp corners and formation of spherical junction in the layout. The breakdown voltage at these junctions is lower than the edges of the finger. The analysis of both the cylindrical and spherical junction has shown that the cylindrical junction has lower breakdown voltage than spherical junction [28]. The decrease of breakdown due to the edges can be eliminated by using curved mask layout at the contact openings without edges. This design will reduce the large electric field build up at the spherical junction formed at the edges of the finger layout design [11]. An example design is shown in Figure 2.20.

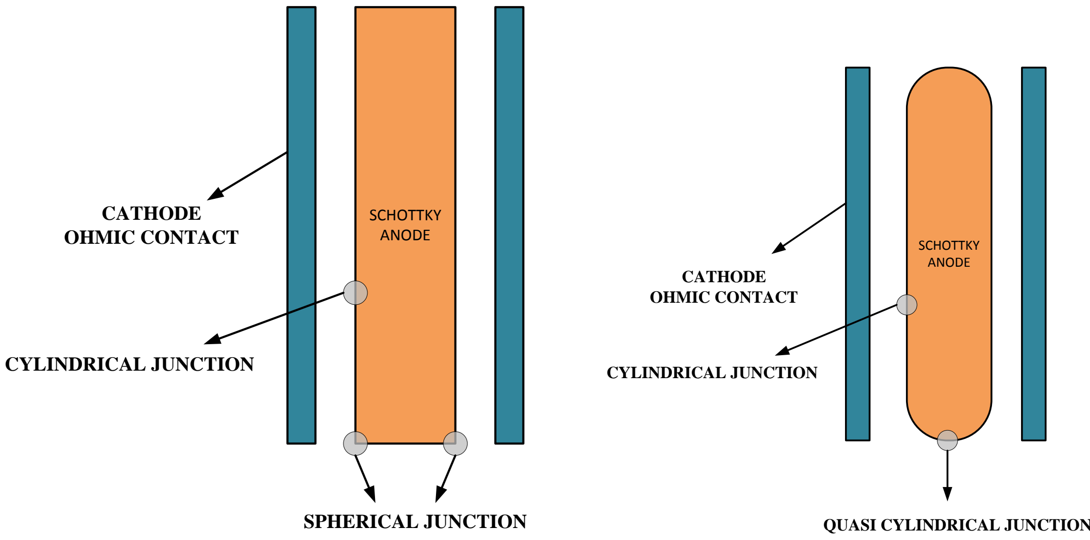

Figure 2.19 Layout rectangular masks **Figure 2.20 Layout cylindrical masks**

2. P+ Guard rings :

The most commonly used method for increasing the breakdown voltage is the incorporation of p+ guard rings in the schottky edge interface. The guard rings will overlap the edges of the schottky anode contact and reduces the large build-up of the electric fields. This is a similar technique that is discussed earlier in vertical Junction Barrier Schottky diodes. The guard rings creates a p-n junction in parallel with the schottky diode. The on state voltage drop is determined by the schottky contact and the breakdown is determined by the presence of pn junction as the schottky junction breakdown at a lower voltage [11]. The P+ guard ring for the

schottky diodes can be made using the same process mask as that of the PMOS and pnp bipolar transistor so there is no additional mask cost. The design of a p+ guard rings around the schottky junction is shown in Figure 2.21. A combination of cylindrical mask termination and guard ring is used to design a schottky diode in this process to reduce the electric field and enhance the breakdown voltage.

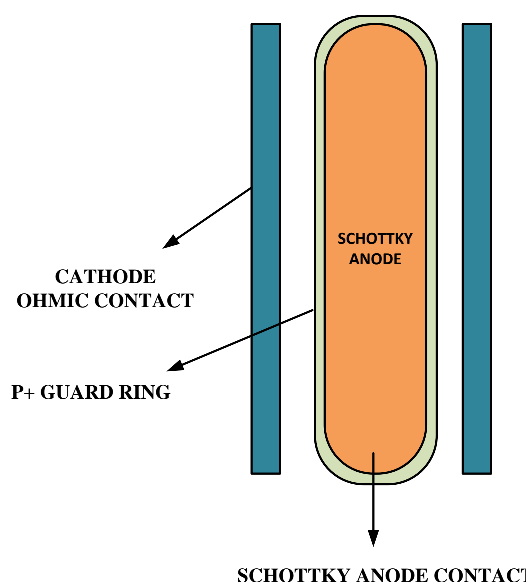

Figure 2.21 Schottky diode layout with P+ guard rings

2.2.3 Design parameters for schottky diodes in BiCMOS process

In the previous section we discussed the factors affecting forward conduction and breakdown of schottky diodes in standard BiCMOS process. Based on these we can deduce the design parameters required for the fabrication of schottky diodes related to process technology and layout considerations.

1. Process technology design parameters :
    a) The main process technology parameter that affects both the forward voltage drop and breakdown voltage is the doping concentration and thickness of the n-well region. From the analytical analysis a breakdown voltage in the range of 10-100V n-well doping concentration needs to be in the range of 10^{16} cm^{-3} - 10^{17} cm^{-3}.
    b) The next consideration is barrier metal used for the schottky junction. The barrier metal in the DIMES BiCMOS process used is aluminum.
    c) The schottky diodes and the schottky barrier height are very sensitive to silicon surface in contact. This quality of the schottky contact depends on the pre-metallization process step. The native oxide residues on the surface of the schottky contact before the deposition of Al/1%Si can increase the schottky

barrier height. In standard IC step, an HF dip is done before the metallization process to remove the native oxide and surface passivation. A good control on this step can result in a good metal-silicon interface before the deposition of Al/1%Si [29].

2. Layout design parameters :
   a) A finger design structure of cathode and anode layout is preferred than a square cathode layout design as this reduces the series resistance. The distance between schottky contact and ohmic contact must be placed as close as possible. A good variation in theses distances must be chosen keeping mine that the schottky contact which are too close to the ohmic contact will have a lower breakdown due to high electric field at the edges. To have a large area diode alternate finger structure layout of schottky (anode) and ohmic (contacts) can be made instead of a large width of the schottky contact.
   b) A curved layout at the edges of the schottky metal contact should be used to eliminate the effects of spherical junction formation and high electric field at the edges.
   c) A p+ guard ring surrounding the schottky metal contacts must be defined to reduce the reverse saturation current and increase the breakdown voltage.

Using the above guidelines for designing the schottky diodes a variety of schottky diodes structure can be made and measured. In this section analytical analysis of the schottky diode in standard BiCMOS process is done. These concepts are used for process and device simulation to study the behavior of the schottky diodes in BiCMOS fabrication process.

2.3 Process and Device simulation of Schottky diodes in DIMES BiCMOS7 process

Process and device simulation using simulators like Tsuprem4 or COMSOL provides evaluation and optimization of the various BiCMOS fabrication steps without the need of a lot of a time consuming fabrication and measurement procedures. These simulators are used in the technology development phase to simulate process steps like thermal oxidation, ion implantation of dopants, diffusion etc. The simulators are based on semiconductor physics models to predict and simulate the behavior of the various fabrication steps [30]. DIMES BiCMOS7 fabrication process utilizes 7 masks for fabricating diodes, bipolar transistor and MOS devices using a simple layout design and process steps developed at DIMES technology centre. The TSUPREM4 models built is based on these process steps. The process simulation of n-well doping profile is first done to determine the doping concentration and depth. As discussed before the doping profile of n-well is a key parameter in the fabrication of schottky diodes in standard BiCMOS process. Next the

complete process and device simulation of schottky diode using the DIMES BiCMOS7 process steps is done to study the forward and reverse characteristics of various design parameters discussed in the previous section. The process simulation is done in TSupreme4 and device simulation is done in Medici. COMSOL semiconductor analysis tool is also used to do some basic modeling of the schottky diodes to analyze electric field and current density.

2.3.1 Modeling and simulation of N-Well Doping profile

The process of n-well formation is done by ion implantation followed by limited source diffusion. The doping concentration and depth of the n-well is determined by dose of phosphorus implant and the drive in time after implantation. From the previous analysis of design parameters for schottky diode a lower n-well doping concentration is desired for higher breakdown voltage and higher n-well doping concentration for lower on-resistance. The n-well surface concentration we need to achieve must be between 10^{16}-$10^{17}cm^{-3}$ with a depth of 2-3 μm. A p-type boron substrate having resistivity 2-5 Ωcm with doping concentration of about $5e15\ cm^{-3}$ is used for n-well formation and the doping profile is illustrated in Figure 2.22. The surface concentration is given by N_s and junction concentration of N_o .

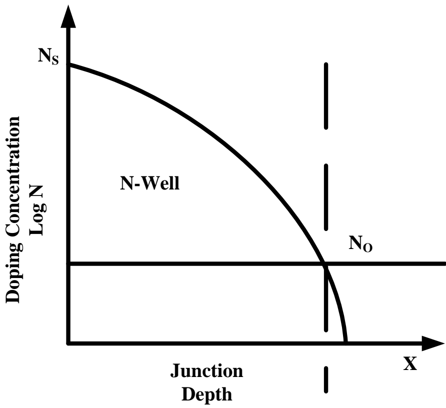

Figure 2.22 N-Well Doping profile

A Gaussian profile is formed after implantation and n-well drive-in. It is given by [31],

$$N(x,t) = \frac{Q}{\sqrt{\pi D t}} e^{-\left(\frac{x}{2\sqrt{Dt}}\right)^2} \tag{17}$$

where :

Q = Implantation dose of phosphorus [cm^2],

D = Diffusion co-efficient of phosphorus [$cm^2 sec^{-1}$],

x = junction depth [μm],

t = Diffusion time [s]

The doping concentration at the surface is given by,

$$N(0,t) = \frac{Q}{\sqrt{\pi D t}} \tag{18}$$

A theoretical calculation can be made by using the Eq (17) and Eq (18) to find the dose and diffusion time. The diffusion temperature defined in the process for drive-in is 1150˚C.

Table 2.2 Implantation Dose and drive-in time for different surface concentration

Surface concentration (cm^{-3})	Junction Depth (μm)	Implantation dose of phosphorus (cm^{-2})	Drive-in time (hr)
10^{16}	2 μm	2E12	4.5
	3 μm	3E12	10
10^{17}	2 μm	10E12	1
	3 μm	15E12	2

From the theoretical analysis, a n-well of junction depth of 3 μm having surface doping concentration of 10^{16}-$10^{17}$$cm^{-3}$ can have phosphorus implantation dose in the range of 3E12 to 15E12 with drive –in time of 2-10 hrs. A deeper n-well with lower doping concentration requires more drive-in time. For measurement and analysis of schottky diodes in a compatible BiCMOS process a deeper n-well with drive-in time of 8 hrs was chosen. The implantation dose was varied as 3E12, 6E12 and 9E12 cm^2.. A 2-D simulation formation of the n-well processed using DIMES BiCMOS fabrication steps is shown in Figure 2.23. A 1-D doping profile of n-well for the different implant dose is shown in Figure 2.23 to Figure 2.26.

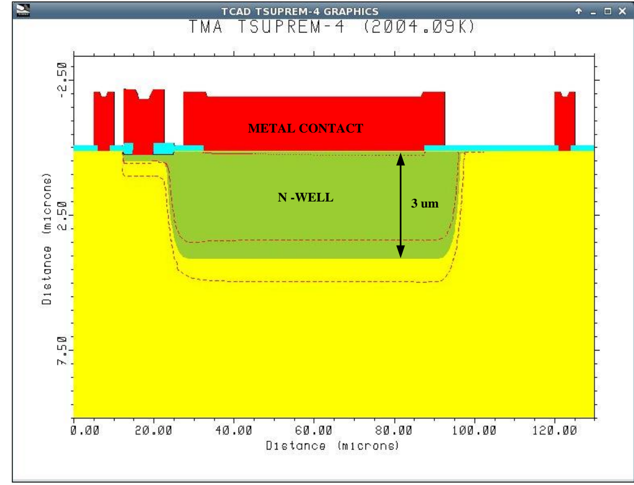

Figure 2.23 2-D simulation of N-Well for Dose 6e12 and drive-in time 8Hrs

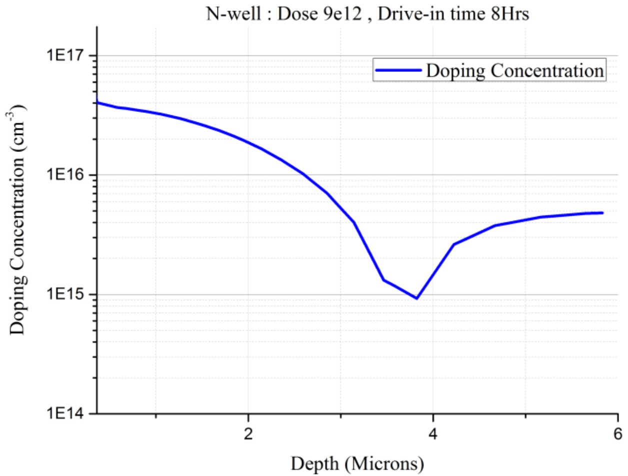

Figure 2.24 N-Well Doping profile for Dose 9e12 and drive-in time 8Hrs

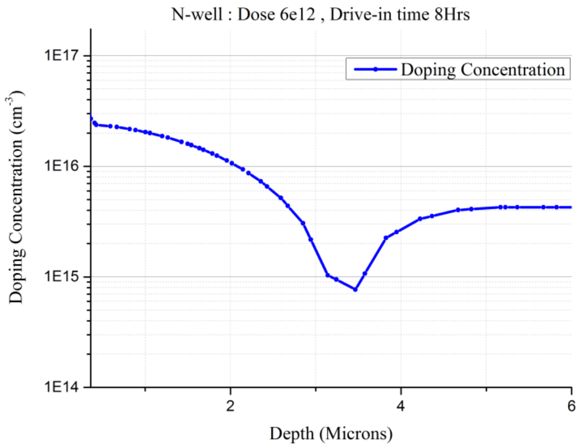

Figure 2.25 N-Well Doping profile for Dose 6e12 and drive-in time 6Hrs

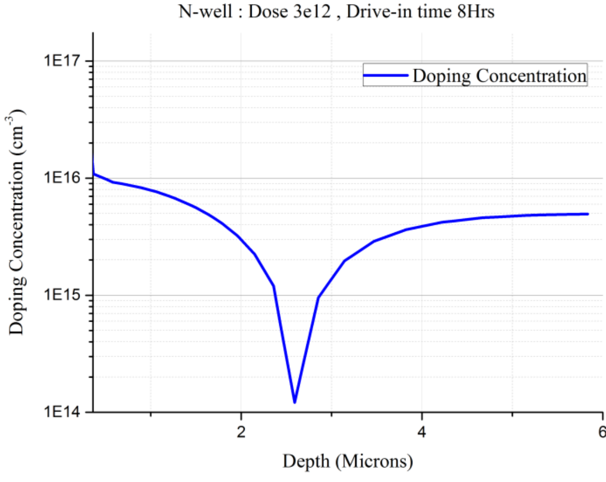

Figure 2.26 N-Well Doping profile for Dose 6e12 and drive-in time 6Hrs

Table 2.3 Surface concentration theoretical and practical comparison

Implantation dose of phosphorus (cm^{-2})	Surface Concentration Theoretical (cm^{-3})	Surface Concentration Simulated (cm^{-3})
3e12	1.82×10^{16}	1.08×10^{16}
6e12	3.04×10^{16}	2.69×10^{16}
9e12	5.04×10^{16}	4.03×10^{16}

A comparison of theoretical and simulated n-well surface concentration is shown in Table 2.3. The simulated values closely match with calculated values. This shows that the simulated n-well doping profile obtained from TSUPREM4 is a robust model for predicting the doping profile in the BiCMOS fabrication process steps. Using this n well model the schottky diodes are simulated and explained in the next section.

2.3.2 Modeling and simulation of Schottky Diodes

The information derived in the design parameters for schottky diodes in BiCMOS process is utilized in simulating and studying the forward current conduction in TSUPREM4 and MEDICI. The main layout parameters for forward conduction that is modified in the below simulation is the anode schottky metal width (W) and the distance between schottky contact and ohmic contact (D) as shown in Figure 2.27 and Figure 2.28 below. The simulation is limited to usage of rectangular mask in TSUPREM4 software. The forward characteristics of a square diode (70μm x 70μm) and a long schottky diode (245μm x 20μm) with the same area are first studied.

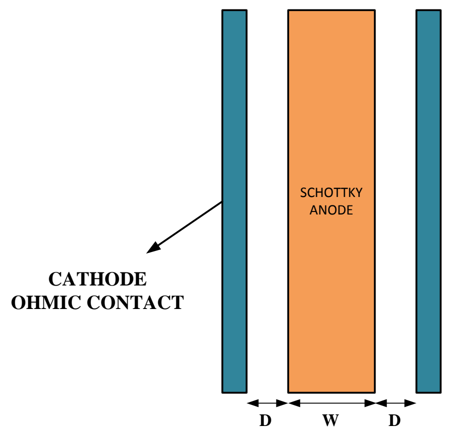

Figure 2.27 Layout of Long diode

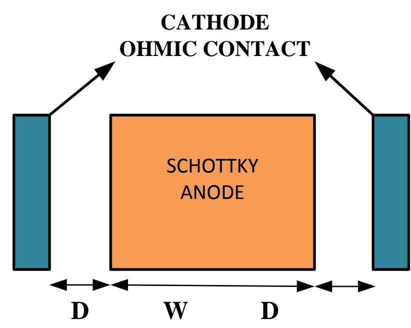

Figure 2.28 Layout of square diode

The standard DIMES BiCMOS7 fabrication uses 7 masks. The following are the fabrication process steps used for simulation,

1. P-type substrate with concentration of 5E12 is implanted with Phosphorus with dose and energy as calculated before.
2. Drive in step for phosphorus diffusion.
3. Arsenic implantation step for Shallow N layer.
4. Boron implantation step for Shallow P layer.
5. VT adjustment step for NMOS and PMOS threshold voltage adjustment
6. Oxidation and anneal
7. Contact opening and first metallization of Aluminum
8. Oxide deposition
9. Second metallization of Aluminum.

A 2-D simulation with current flow of the schottky diode using the above process steps is shown in Figure 2.29.

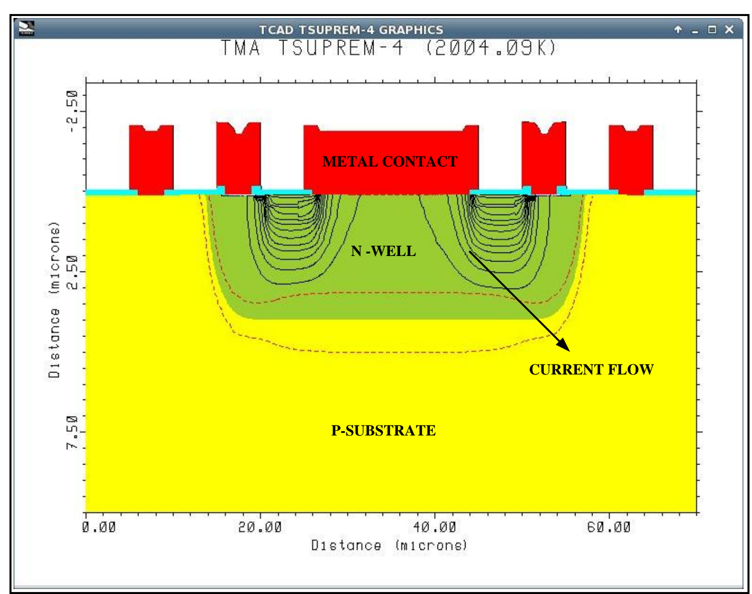

Figure 2.29 2-D current simulations of schottky diode - 245µm x 20µm

From the Figure 2.29, it can be seen that the current density is highest at the edges of the anode schottky metal contact and n+ cathode ohmic contact. The current flow in the bulk of the n-well is limited. A plot of IV characteristics is simulated using MEDICI to study the forward current of the schottky diode for both the diode configuration long diode and square diode. A comparison plot of the IV characteristics is shown in Figure 2.30. The long diode (A) and square diode(B) show similar characteristics in the low bias region but during the high forward bias the

series resistance of the square diode is greater than the series resistance and the current conducted is lesser than the long diode.

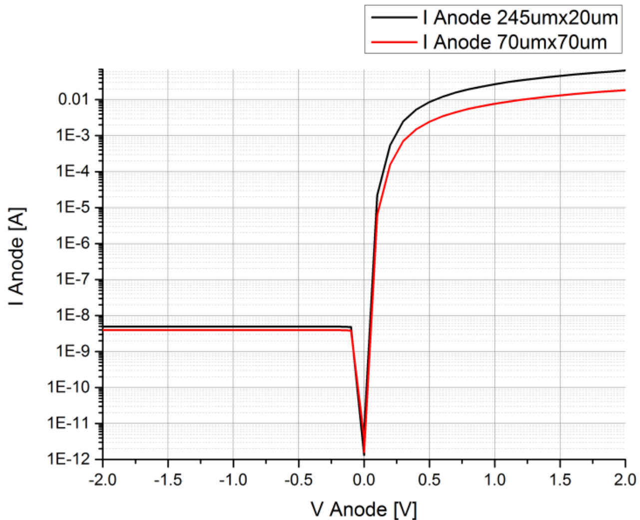

Figure 2.30 Forward IV characteristics of– Long and Square Schottky diode

For the long diode A the forward voltage $V_F = 0.4$ at $I_F = 5mA$ and for the short diode B the forward voltage $V_F = 0.4$ at $I_F = 1.5mA$. In this analysis we know that schottky diode with same areas but having different perimeter, the perimeter factor of the schottky diode dominates for higher current conduction. A similar model is used in COMSOL to study the effect of current conduction in the schottky diode. Based on the fabrication steps of the schottky diode, the 3D model in COMSOL is designed. The doping profile of n-well with a depth of 3um is modeled. The metal is in contact with the n-well layer and the ohmic contact is with highly doped. The distribution of electron concentration in the schottky diode in the entire semiconductor block is shown in Figure 2.31.

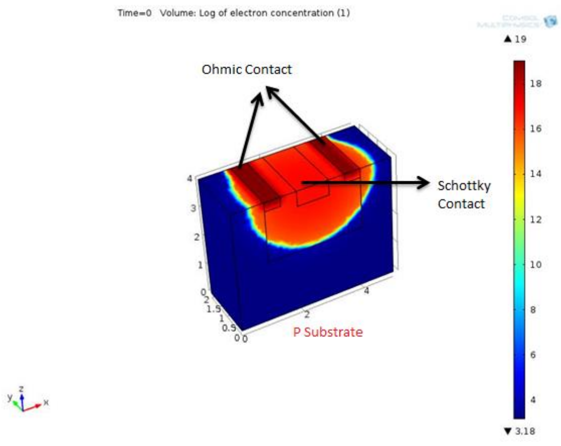

Figure 2.31 Electron concentration profile in Schottky diode 3D Model

The profile shows N+ region (dark red) with electron concentration of 10^{19} cm^{-3} and n-well concentration (red) with electron concentration of $10^{17}cm^{-3}$.For the long diode configuration a similar forward IV characteristics was performed for the COMSOL model. The current density in the planar schottky diode is shown Figure 2.32. The current at the schottky metal contact edge and ohmic contact is maximum.

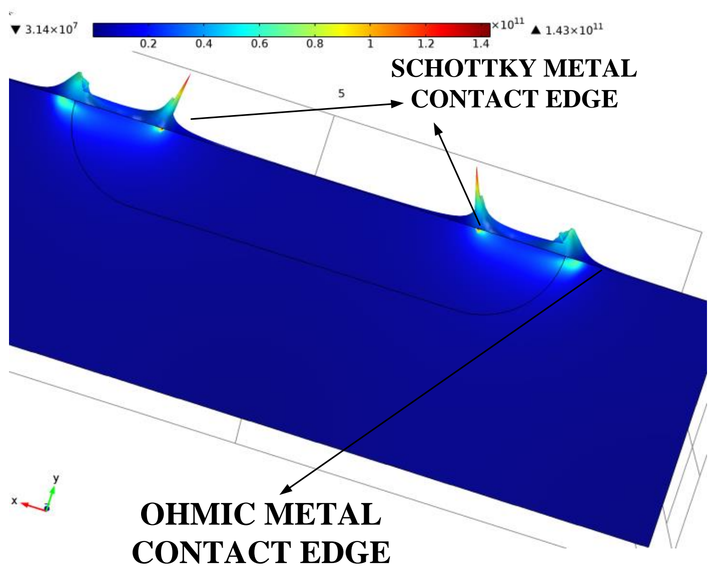

Figure 2.32 Current Density profile for Schottky diode in forward bias

With analytical and simulation models, it is clear that a schottky diode with small width and large length should be used for higher current conduction. A finger design is preferred over a square design. In the next section simulation and analysis of for high current schottky diode is done.

2.3.3 Modeling and simulation of high current Schottky Diodes in BiCMOS process

In this section various layout design of the finger structure is analyzed. The main layout parameter to vary is the distance between schottky metal contact and the ohmic contact (D) as shown in Figure 2.27. The simulations are done for different n-well dose which ranges from 3E12, 6E12 and 9E12 for a drive-in of 8hrs. The aim is to keep the distance between the schottky contact and ohmic contact 'D' as minimum as possible. The distance D is varied from 5µm to 2µm and the schottky contact width is varied from 20µm to 5µm. The results are tabulated in Table 2.4. The analysis is done with area of schottky diodes 250µm x (W). For a forward voltage drop of V_F = 0.4V the forward current I_F for the different layout configuration is noted. A comparison is made for all the layout structures and the forward IV characteristics are shown from Figure 2.33 to Figure 2.35. The aim is to achieve a target of 1A at a forward voltage drop of 0.4V. The barrier metal in this simulation is restricted to the process material of Al/1% Si.

Table 2.4 Schottky diode with different W and distance D

Implantation dose of phosphorus (cm^{-2})	Width (W) µm	Distance (D) µm	Forward current I_F at $V_F = 0.4V$
3e12	20 µm	5 µm	1.7 mA
		2 µm	2.39 mA
	10 µm	5 µm	1.25mA
		2 µm	1.79mA
	5 µm	5 µm	1.1 mA
		2 µm	2.15 mA
	3 µm	5 µm	0.9 mA
		2 µm	1.24 mA
6e12	20 µm	5 µm	5.23 mA
		2 µm	7.17 mA
	10 µm	5 µm	3.8 mA
		2 µm	5.39 mA
	5 µm	5 µm	4.28 mA
		2 µm	6.4 mA
	3 µm	5 µm	2.75 mA
		2 µm	3.7 mA
9e12	20 µm	5 µm	7.98 mA
		2 µm	10.75 mA
	10 µm	5 µm	5.66 mA
		2 µm	8.08 mA
	5 µm	5 µm	7.1 mA
		2 µm	9.6 mA
	3 µm	5 µm	8.24 mA
		2 µm	4.84 mA

The data analysis in shows that for increasing n-well dose the forward current at given forward voltage increases .The shorter the distance between schottky contact and ohmic contact ‘D’ the current is higher. The higher the width of the schottky contact ‘W’ of the schottky contact the current density is higher. Hence a schottky diode with larger width ‘W’ shorter distance ‘D’ and higher N-well dose is preferred for high current conduction. The forward IV curve follows a similar behavior for all layout configurations with main difference is in the amount of current conduction at the given forward voltage.

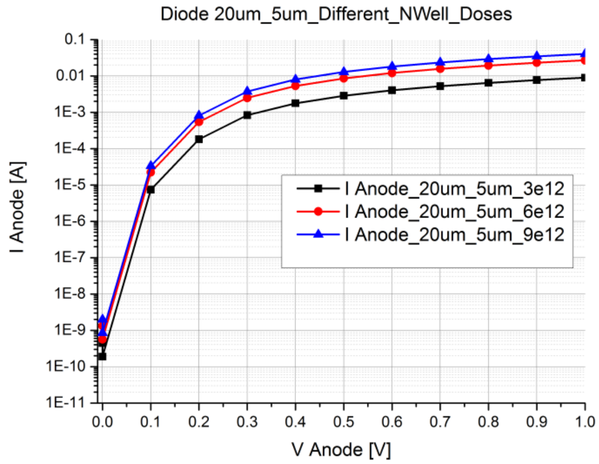

Figure 2.33 Schottky diode W=20um D = 5um for different n-well dose

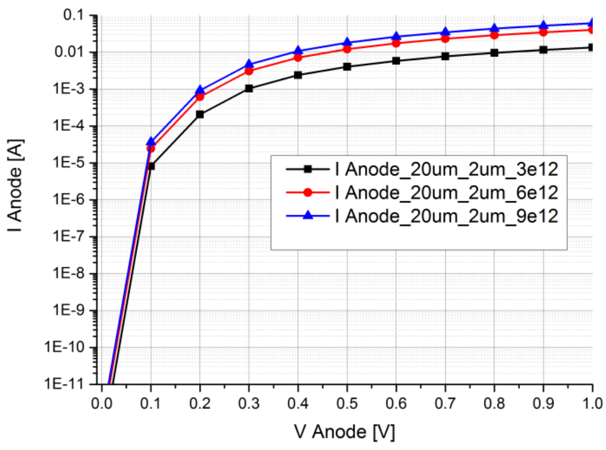

Figure 2.34 Schottky diode W=20um D = 2um for different n-well dose

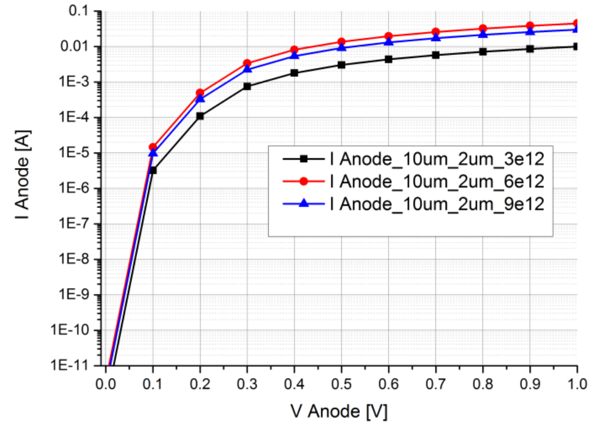

Figure 2.35 Schottky diode W=10um D = 2um for different n-well dose

As discussed in the previous section of this chapter, two ways to increase the current conduction at low bias is by using metal or metal silicides with lower barrier height or increasing the area of the device. Since we are limited to aluminum the option is to increase the area. The effect of finger structure in large current schottky diodes is studied by a 2-D simulation of the current conduction of finger structure of schottky diode in TSUPREM4. It is shown in Figure 2.36. Due to the limitation of TSUPREM tool to simulate large structure, schottky diode with a schottky area of 250µm x 20µm and 5 fingers is done.

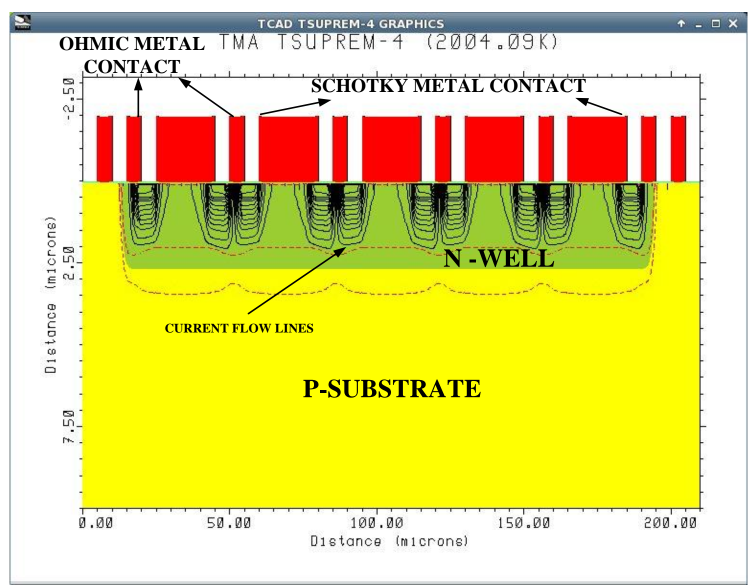

Figure 2.36 2-D current simulations of schottky diode 5 fingers- 250µm x 20µm

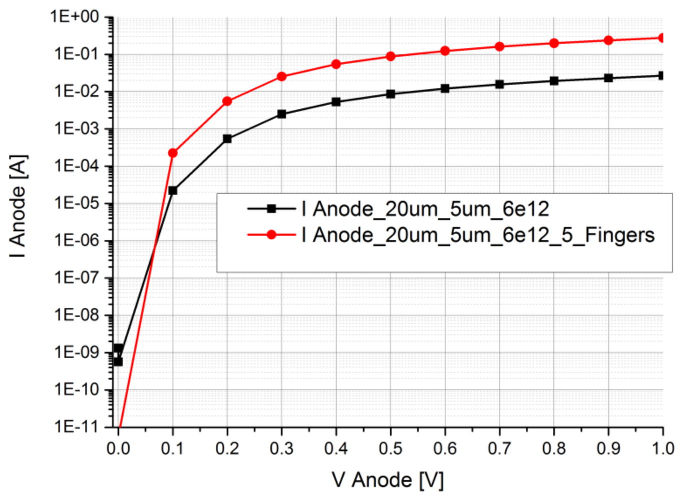

Figure 2.37 Schottky diode finger design vs. single schottky diode W = 20, D = 5

The current flow in the finger structure is mostly on the edges from schottky anode to the ohmic cathode. The schottky contacts are connected together to the anode terminal. The total current is the sum of the currents through each finger. A comparison of IV characteristics with the finger schottky structure and a single schottky diode is shown in Figure 2.37. With a 5 fingers design the forward current I_F = 21 mA at V_F = 0.4 when compared to single finger schottky diode I_F = 5 mA at V_F = 0.4. The current is increased to about 4-5 times. From this analysis, if we consider a finger of 250µm x 20µm can achieve average current 1mA, then for 1A we need a parallel configuration of 1000 fingers each having schottky contact are area of 250µm x 20µm with a total area of $5mm^2$. But since we need to keep in the limits of space of packaged diodes which is in the range of 2~ $2.5mm^2$, the length and the number of fingers can be altered. The area of each finger can be 1000µm x 20µm for a total of 70 fingers to achieve a current of 1A assuming per finger can conduct about 20mA of current. So the total schottky contact area of this device would be about $1.4mm^2$. In order to make use of the large area, with the calculated device area a multiplication factor of 2~3 is used to achieve the configuration of schottky diode conducting a forward current of 1A at a V_F of 0.4V. Using this analogy the mask layout is made by using parallel finger design of schottky contact and ohmic contacts inside the n-well layer.

The above simulations in TSUPREM and COMSOL were used to study the behavior of the schottky diode in forward bias and ways to increase the forward current. But the limitation and problems were found during the breakdown analysis. COMSOL had many convergence issues while TSUPREM4 had problems in loading the correct models to study the breakdown of the schottky diodes. Hence, in modeling and simulation of schottky diodes, the various breakdown techniques were not studied with simulations. The breakdown techniques of guard ring and junction curvature derived analytically is used to design the mask layout. In the high current design of schottky diodes, each finger of the schottky contact are used with cylindrical corners with guard rings attached at the edges of the schottky contacts as discussed before. By this process we try to achieve a high current and high breakdown schottky diode design in standard BiCMOS process.

2.4 Chapter Summary

In this chapter a detailed analytical analysis of schottky diode in BiCMOS process is studied. The design parameters were derived analytically and verified with TCAD simulations for high current schottky diodes. These parameters serve as the platform for layout design and fabrication in BiCMOS process. It was deduced that the main factors that affect the forward and reverse characteristics are doping concentration of the n-well region. Higher doping concentration gives higher forward current conduction and lower doping gives higher breakdown voltage. Hence there is a trade-off between these characteristics. It becomes essentially to tune this doping concentration to suit both the needs.

Chapter 3

Fabrication and Characterization

In this chapter the fabrication steps and characterization of schottky diodes in DIMES BiCMOS7 process is discussed. Measurements of the devices are done using cascade probe station and semiconductor analyzer tool using ICCAP measurement software. A spice level 3 model is extracted from the measurement data for circuit analysis. NPN bipolar transistor, NMOS and PMOS devices fabricated in this process is also characterized and spice model is extracted.

3.1 Fabrication of Schottky diodes in DIMES BiCMOS7 process

The BiCMOS process technology is a combination of Bipolar and CMOS transistors combined in a single integrated process [27]. The BiCMOS7 process developed in DIMES provides a low complexity, low cost 7 mask process for the fabrication of bipolar transistors, MOSFETs and integrated circuits. The schottky diode designed in this thesis for rectifier applications is fabricated in this process in such a way that it can also satisfy the process technology requirement of bipolar transistors and mosfets. This process also offers a benefit of flexible and simple mask layout design of the devices. In this section, the procedure for designing and fabricating schottky diode for high current and high breakdown done as part of the thesis work is discussed. The design rules for mask layout used are first discussed. Next the complete fabrication steps involved in this process for schottky diodes are explained.

3.1.1 Design rules for mask layout

The mask design is done in L-Edit software. In DIMES BiCMOS7 process 7 masks are used to fabricate diodes, transistors and mos devices. It is important to have a set of design rules that defines the minimum spacing between mask layers of the devices. This prevents shorting of

the layers (for example in metal 1 layer if the design of two lines to close to each other), tolerance during photolithography process and mask layers misalignment [31]. The 7 mask layers used in the design is shown below,

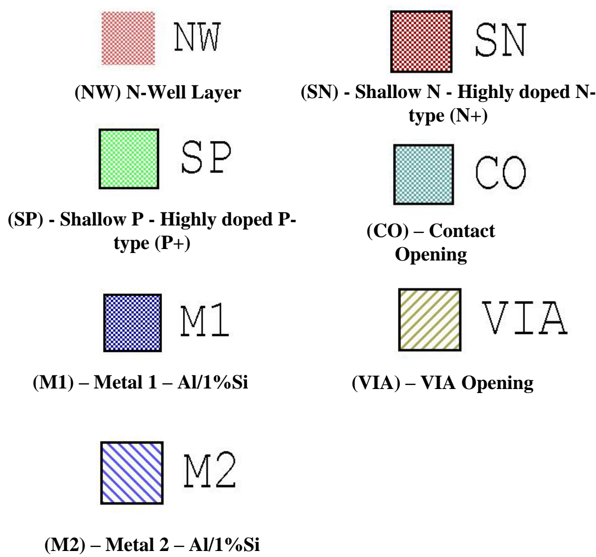

Figure 3.1 Layers for BiCMOS mask design

A brief discussion of the functionalities of each layer in the mask design is described below,

5. N-Well Layer (NW) – A low doped n-type layer. This layer forms the substrate of PMOS transistor, the collector of NPN bipolar transistor and the n-type region for the schottky metal contact.
6. Shallow N (SN) Layer – A highly doped n+ layer to provide ohmic contact. This layer also forms the source and drain of NMOS, emitter for the NPN transistor.
7. Shallow P (SP) Layer – A highly doped p+ layer forms the source and drain of PMOS, emitter for the PNP transistor. This layer is also used as guard rings in the schottky diode and mosfets.
8. Contact Opening (CO) Layer –This mask layer provides the contact openings for ohmic metal contacts for all the devices. For schottky devices this mask provides the opening for the schottky contact.
9. Metal 1 (M1) Layer – The metal layer mask is a dark field mask that is used to pattern the aluminum metal formed by sputtering.
10. VIA (VIA) Layer –This mask layer provide the openings for metal 2 layers. This layer exposed after deposition of 500nm oxide.
11. Metal 2 (M2) Layer – This is the second aluminum metal layer.

An example mask layout and device cross-section of schottky diode in BiCMOS process using the layers defined above is shown in Figure 3.2. The mask layout of schottky diodes is

designed by first considering the schottky contact width of the device (W). The distance (D) between the schottky metal contact and the SN layer edge defines the main separation of the anode and cathode contact. The designs of schottky diodes are made by varying the distance (D) and width (W) of the schottky contacts. The substrate contact is done through the SP layer.

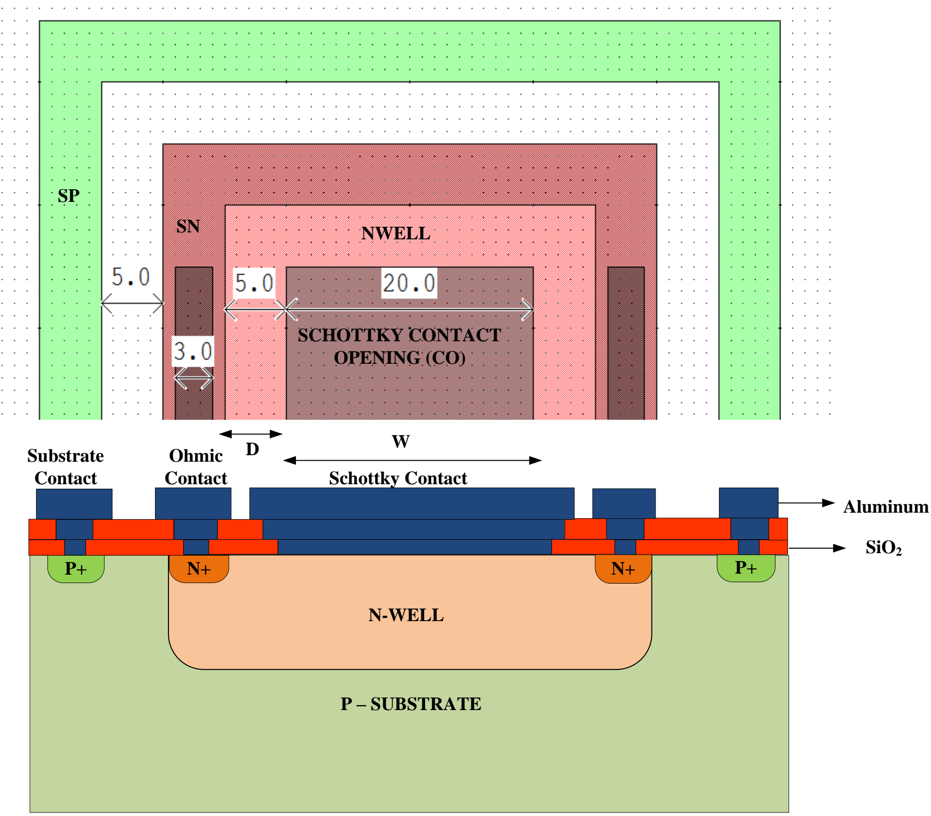

Figure 3.2 Mask Layout and device cross section – scale in µm

The SP layer is also used as the guard ring at the schottky junctions. The design rules are defined by minimum feature size that can be transferred on the wafer using the lithography equipment. In DIMES BiCMOS7 process the minimum feature size is set at 0.5µm (λ). For designing the schottky and ohmic contact a minimum size of 2µm is used to have a safety factor due to misalignment tolerance. The spacing between the contact opening and shallow N layer is kept at a distance of 2µm to prevent overlap of ohmic contact diffusion layer with the schottky junction. The minimum distance between Metal1 and contact opening (CO) is kept as 1µm. The distance between two metal 1 layout structures is a minimum of 2 µm. An example layout of spacing between metal1 layouts is shown in Figure 3.3. This minimum spacing prevents shorting of the metal layers. The metal 2 is deposited on via openings. A similar rule as used by the Metal1 and contact opening is used. The minimum spacing between two metal 2 layout structures is 2µm .The spacing between VIA mask and Metal2 is kept at a distance of 1µm. An example layout design of VIA, Metal2 mask layout is shown in Figure 3.4. These design rules

are kept in consideration for the complete design of low current and high current schottky diodes fabricated in BiCMOS7 process.

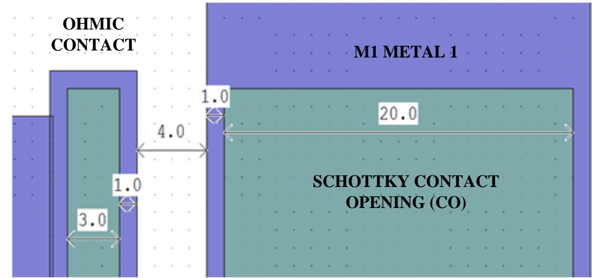

Figure 3.3 Example layout design for spacing between metal 1 (M1)

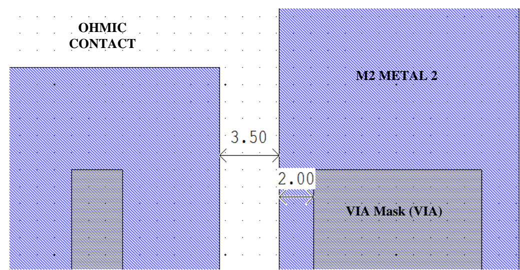

Figure 3.4 Example layout design for spacing between metal 2 (M2)

The two main schottky diode designs that were made are schottky diodes with small area and schottky diodes with large area having finger structure. The small area schottky diodes are with dimensions 250µm x (W), where W is the factor varying from 20 µm to 3µm. For high current schottky diode design is made with finger structures with schottky area calculated to be a current conduction of up to 1A for a forward bias voltage V_F = 0.4V. The different layout structure used includes rectangular schottky contact, cylindrical schottky contact and cylindrical schottky contact with guard ring and an example these schottky contacts are shown in the Figure 3.5 to Figure 3.6.

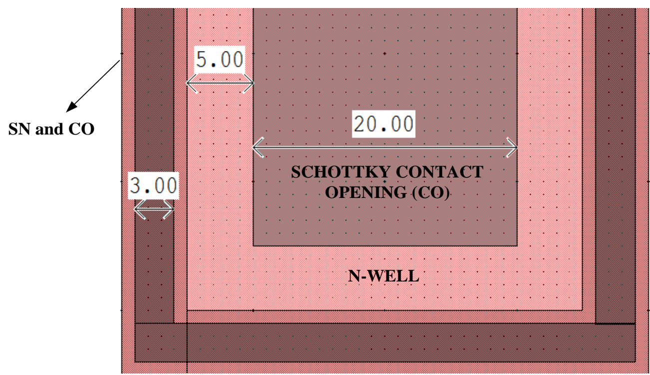

Figure 3.5 Rectangular schottky diode layout designs

The design for high current schottky diode is made by using alternate fingers of schottky contacts and ohmic contact. An example design with cylindrical schottky contact having p+ guard rings and ohmic contact is shown in Fig 3.6.

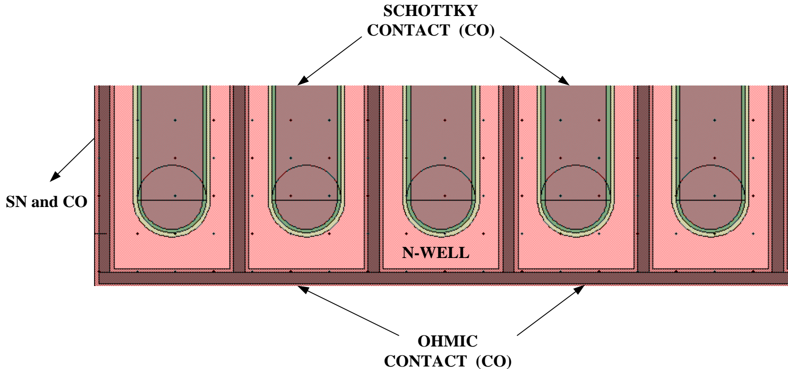

Figure 3.6 Cylindrical schottky diode finger designs for schottky and ohmic contacts

Using the design rules and layout structure described above, the various test structures for low current and high current schottky diodes are designed as shown in Figure 3.7 and Figure 3.8. The mask fabricated is a stepper mask that allows all the layers placed in a single mask frame.

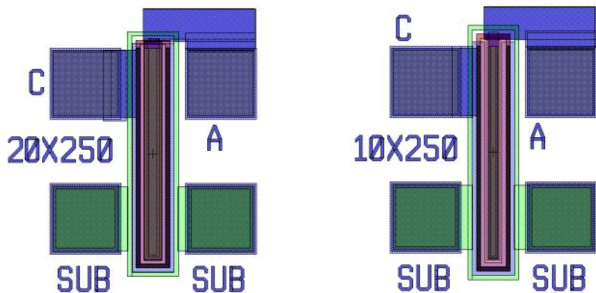

Figure 3.7 Test structures of low current schottky diode W = (20µm, 10µm), L =250µm

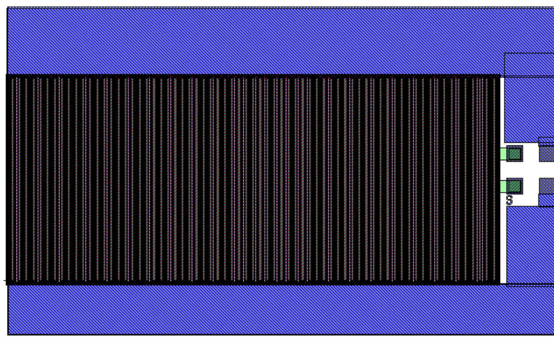

Figure 3.8 Test structures of high current schottky diode W = 20µm, L =1000µm 70 fingers with schottky contact area = 1.4 mm2

3.1.2 DIMES BiCMOS7 fabrication process

The BiCMOS7 fabrication process steps incorporating schottky diodes using the layout designs described earlier is explained in this section. The substrate wafer is a p-type wafer with resistivity 2-5Ω-cm with orientation 1-0-0. This corresponds to a substrate doping concentration of 3×10^{15}- 5×10^{15} cm^{-3}. The alignment markers are patterned and etched in the wafer to align each new mask to the previous mask level [31]. For the fabrication 10 wafers are used to study process parameter variations. The main process steps are described below,

1) N-Well formation:

The N-well layer is the first layer that is fabricated in the process using NW mask. The process step is illustrated in Figure 3.9. The wafers are cleaned in the wet bench with 10 mins in fuming nitric acid, 10 mins in concentrated nitric acid and rinsed in demi-water.

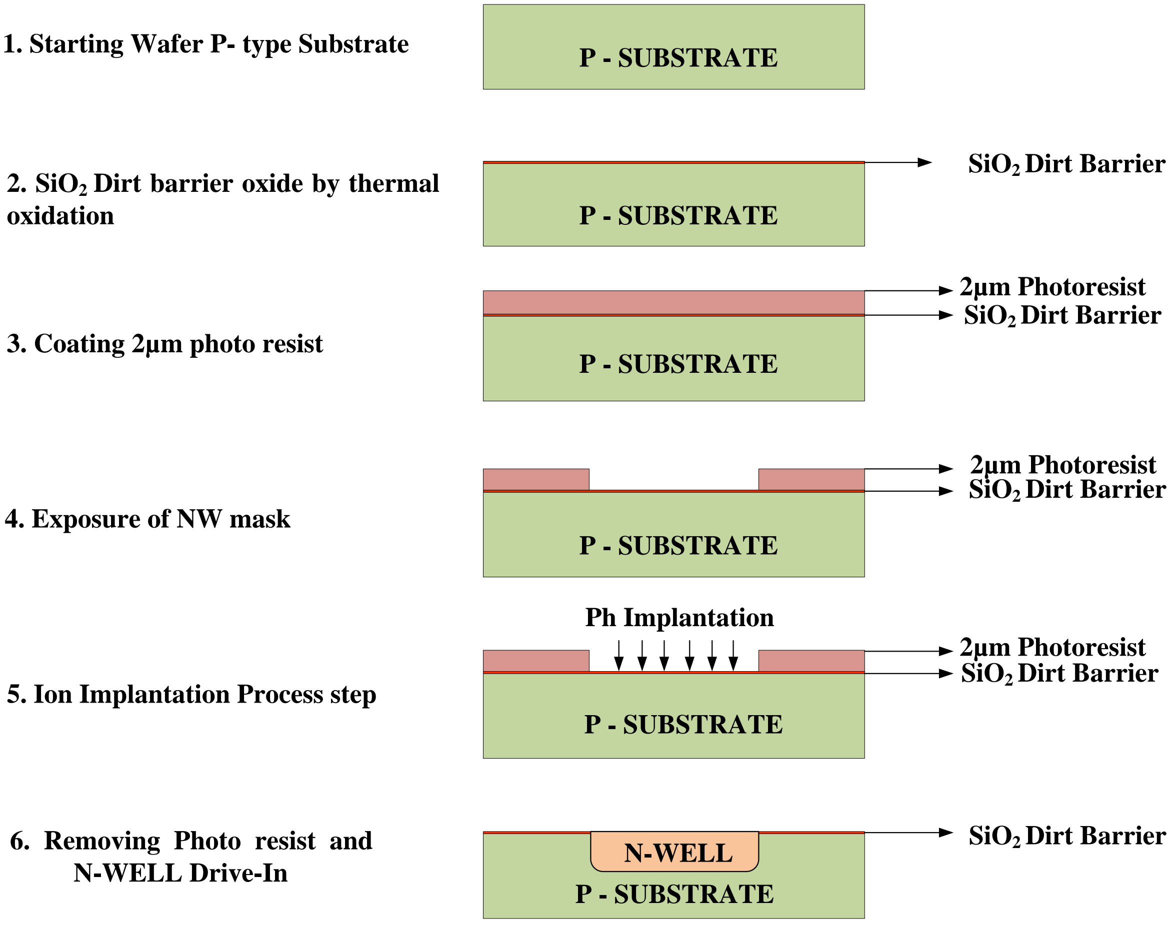

Figure 3.9 N well formation process steps

A 20nm thick silicon oxide is first grown by thermal oxidation. This process is done in TEMPRESS Diffusion furnace at 950˚C for 35 mins. This layer forms the dirt barrier layer. It is used as a masking layer during implantation and to prevent impurities in silicon in unexposed regions. A 2μm thick photo resist is coated using EVG wafer coater and developer. Next the NW mask in the stepper mask is exposed on the photo resist with ASML – ASM PAS 5500 stepper. Since a thicker photo resist is used the exposure energy is set to 280mJ / cm^2. The wafers are developed using a standard double puddle procedure for post exposure bake and development in EVG wafer coater and developer.

The wafers are subdivided into batch of three containing three wafers each. This distribution is done to vary the dose of the phosphorus implantation. The energy of the implantation is 150 keV. The dose for the three batches is varied as 3×10^{12} cm^{-3}, 6×10^{12} cm^{-3} and 9×10^{12} cm^{-3} respectively. After the implantation, the photo resist is removed. The n-well drive in is performed at a temperature of 1150 ˚C with drive-in time of 8hrs for a deeper n-well as discussed in the previous chapter.

2) Shallow N (SN) layer:

In the drive-in diffusion process, a thickness of 335nm of SiO_2 is formed. This thermal oxide is removed by wet etching in buffered HF solution. The etch rate was calculated to be 1.3nm/s. The wafers were placed in this solution for about 5 minutes and checked until the backside of the wafers are hydrophobic. The wafers are cleaned and prepared for Shallow N implantation. A dirt barrier thermal SiO_2 is first formed on the wafer by dry oxidation. The wafers are coated with 1.4μm thick photo resist and SN mask is exposed on the photo resist. The wafers are developed by standard single puddle recipe in the EVG developer. A standard Arsenic implantation at a energy of 40 keV and dose of 5×10^{15} cm^{-2} is done.

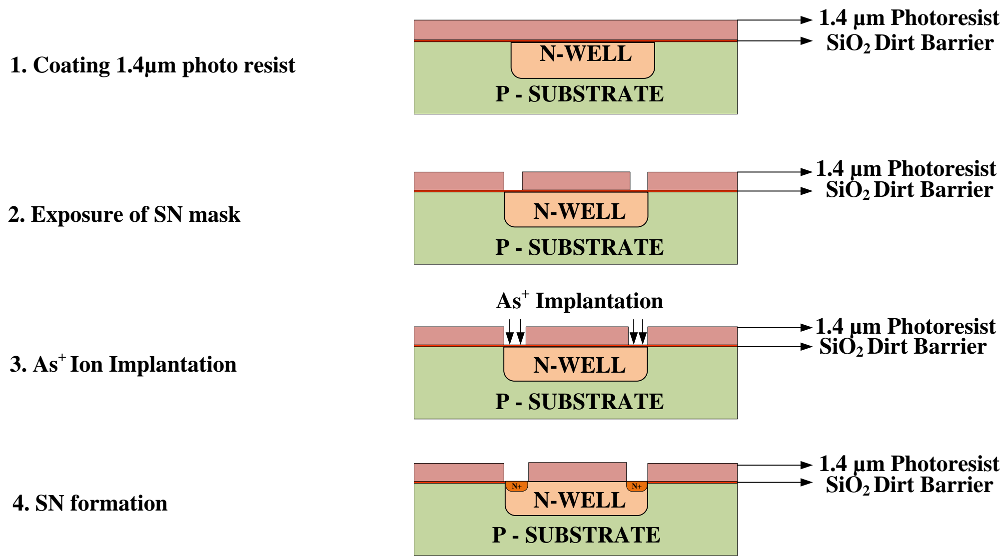

Figure 3.10 Shallow N process steps

The shallow N layer forms the emitter of NPN transistor, source and drain for NMOS and cathode ohmic contact for schottky diode. The process flow is illustrated in the Figure 3.10. An optical microscope image of the SN layer patterned from the mask transferred to the wafer after development is shown in Figure 3.11. Arsenic implantation is done in this exposed area of the photo resist.

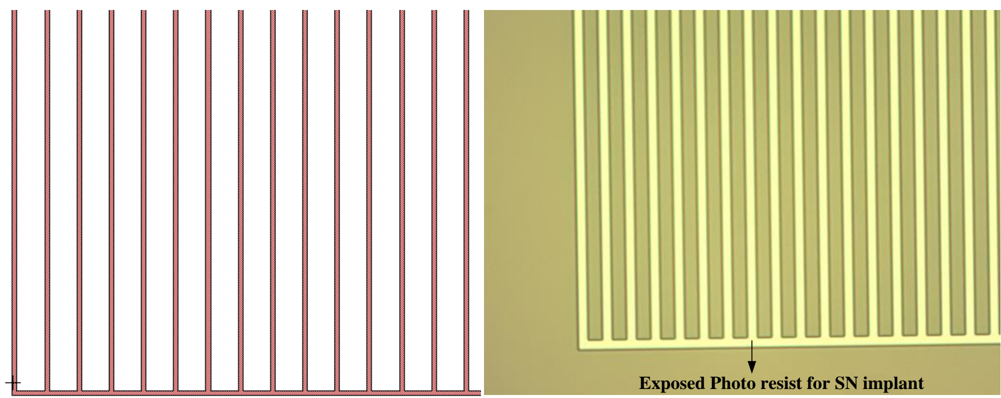

Figure 3.11 Shallow N patterns on wafer after development compared with SN mask

3) Shallow P (SP) layer:

The shallow P layer forms the base of NPN transistor, source and drain of PMOS devices, guard ring and substrate contact for schottky diodes. The process steps are shown in Figure 3.12. The wafers are coated 1.4µm thick photo resist with standard procedure. The SP layer in the mask is exposed .The wafers are then developed. The exposed SP layer patterns in the wafer after development along with previously implanted SN layer is shown in Figure 3.13. For SP layer, boron implantation is done at energy of 40 keV and dose of 5 x 10^{15} cm^{-2}.

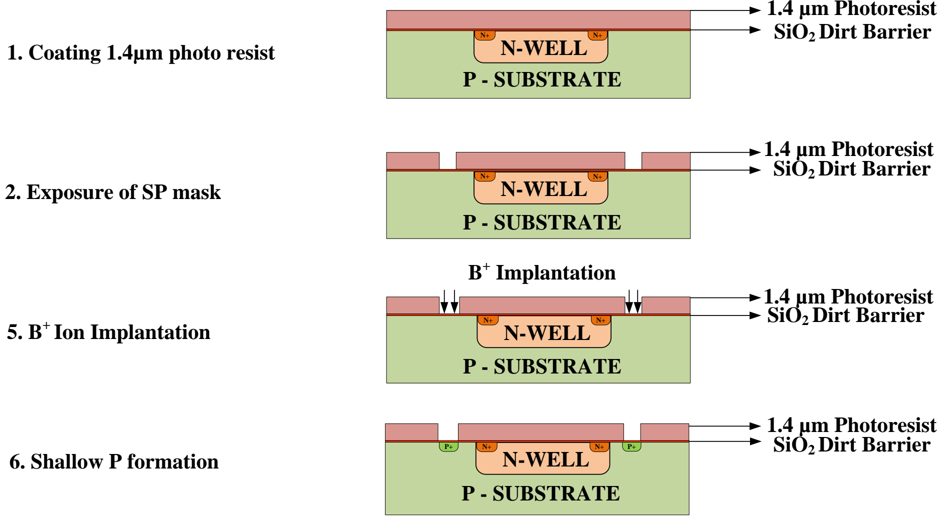

Figure 3.12 Shallow P process steps

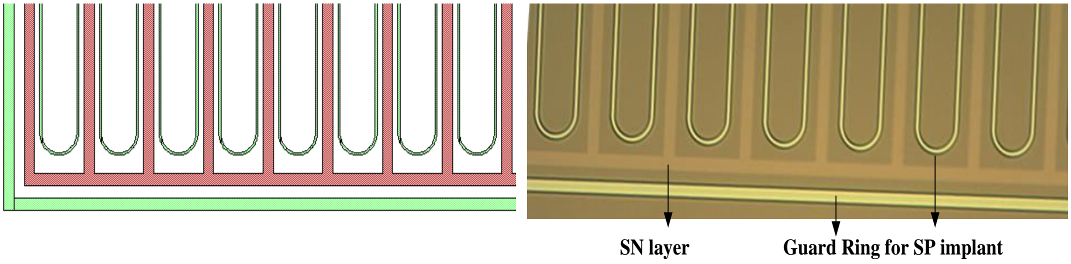

Figure 3.13 Shallow P pattern on wafer after development and SN Layer

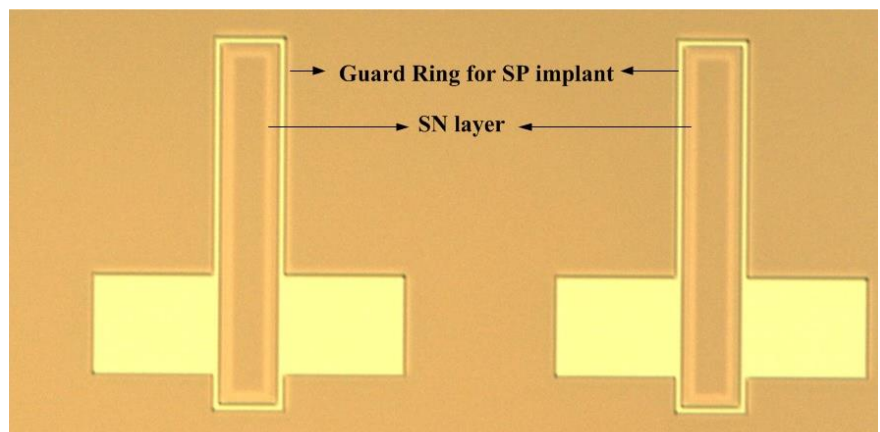

Figure 3.14 Shallow P pattern on wafer after development and SN Layer

4) V_T adjust for threshold voltage modification:

The threshold voltage of the NMOS and PMOS device are adjusted by implanting boron into the channel regions of NMOS and PMOS devices. In case of NMOS device the boron implant increases the threshold voltage of the as it increases the p-type channel concentration. In PMOS device the threshold voltage becomes less negative with boron implantation [27]. In order to study the variation in the threshold voltage and the effect on schottky diode forward and reverse characteristics, the batch of wafers was divided into 3 groups having same NW dose with different dose of boron implant. The boron implantation was done at energy of 25keV with dose ranging from 3 x 10^{12} cm^{-2} to 8 x $10^{12}cm^{-2}$ for three groups of the wafers as shown in Figure 3.15.

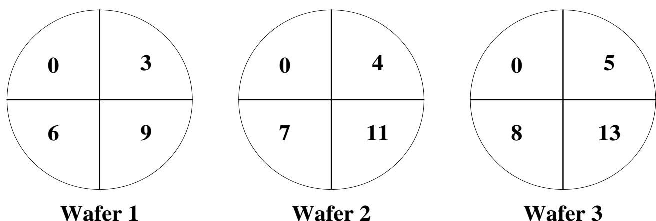

Figure 3.15 VT adjust B+ implant (in 1012 cm-2) for 3 wafers of same N-Well dose.

5) Contact Opening (CO) and Surface passivation

Before the contact opening step, the gate oxide is formed by thermal oxidation and anneal step. The wafers are placed in the TEMPRESS furnace and the oxidation duration is set for 2 hrs and 30 minutes. After the oxidation, the measured mean oxide thickness on undoped areas was 110 nm. The mean oxide thickness on SN was 220nm and on SP was 118nm. The process flow until contact opening steps is shown in Figure 3.16. The wafers are coated with 1.4 µm photo resist and patterned with contact opening (CO) mask. The wafers are developed and the contact opening patterns obtained for different structures is shown in Figure 3.17.

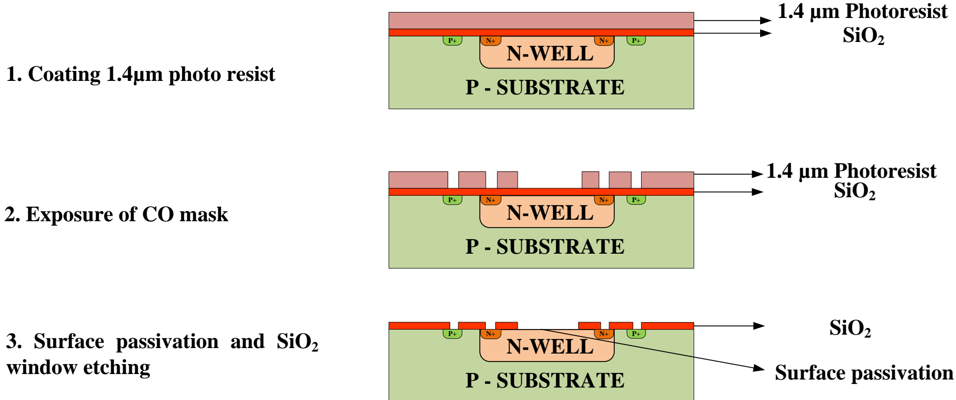

Figure 3.16 Contact opening (CO) process steps

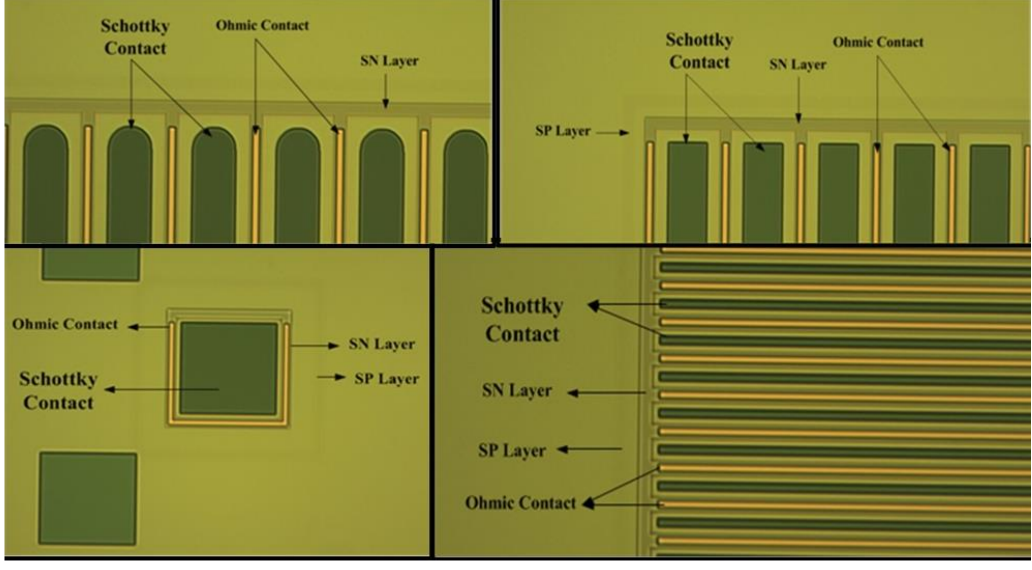

Figure 3.17 Contact opening (CO) pattern on wafer after development – rectangular and cylindrical schottky contacts – single and finger structures

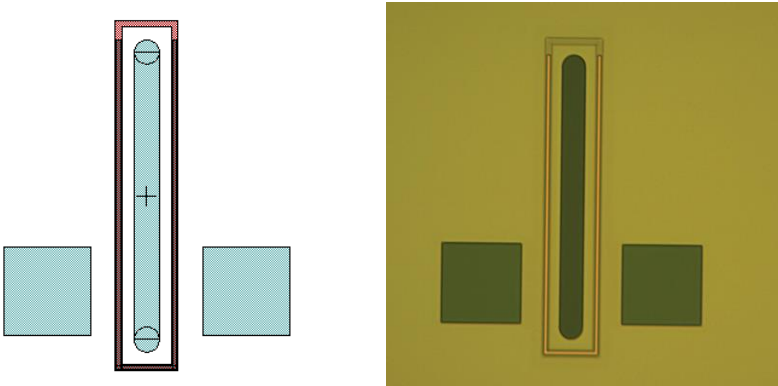

Figure 3.18 Contact opening (CO) pattern on wafer after development with CO mask

After the contact openings are patterned on the wafer, the next important step in the fabrication of schottky diodes is the silicon oxide window etching and surface passivation. The schottky barrier height is sensitive to the surface to which the metal is in contact. The schottky barrier height is increased due to the presence of native oxide residues. Hence, a good surface at the metal semiconductor junction before the metal deposition is essential for a good schottky junction [29]. The oxide window etching is done by wet etching using buffered HF solution. The wafers are cleaned and a pre-metallization step is performed. In this step, the wafers are placed in 0.55 % HF solution and an extended HF dip is performed for 10 mins. The metallization step is immediately performed after drying the wafer to reduce the formation of oxide at the surface of the contact openings.

6) Metallization Metal1, VIA and Metal2

The deposition of first metal layer using Aluminum and 1% silicon with thickness 200nm is done using TRIKON SIGMA sputter machine at 350 ˚C. The wafers are coated, patterned and developed using the M1 mask. Aluminum is etched using plasma etcher. The next step is to deposit oxide between metal 1 and metal 2. A layer of 500nm of silicon-di-oxide is deposited using Novellus PECVD. The openings for the deposition of metal 2 layer is done through VIA openings from the VIA mask layer. The second metallization process is done in the similar way with 99% Al and 1% Si deposited with a thickness of 2µm at 350˚C. The process step for the metallization is described in Figure 3.19. The optical images after patterning and etching of metal1 is shown in Figure 3.20. The final metallization process steps of M2 are shown in Figure 3.21and the images after complete patterning and etching is shown in Figure 3.22. The final step in the fabrication process is alloying done in nitrogen and hydrogen environment at a temperature of 400 ˚C. This step provides passivation of the silicon/silicon di-oxide and also improves the contact between metal and the semiconductor.

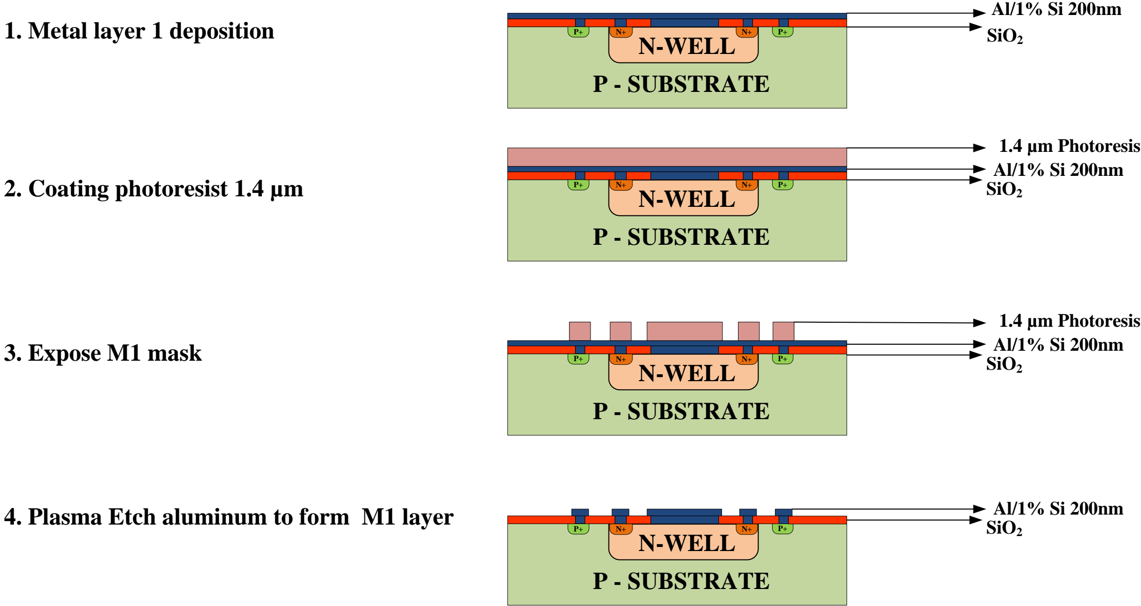

Figure 3.19 Metal 1 layer process steps

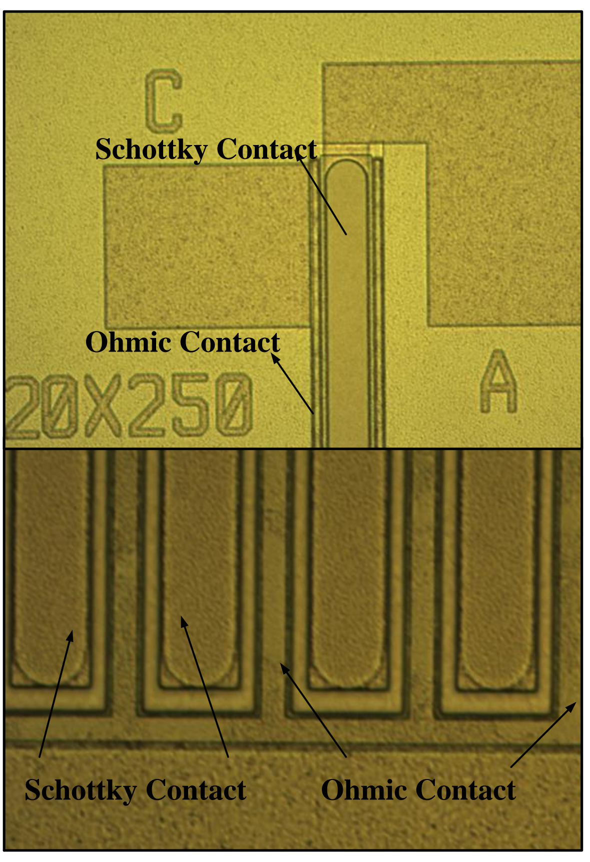

Figure 3.20 Metal 1 after patterning and etching

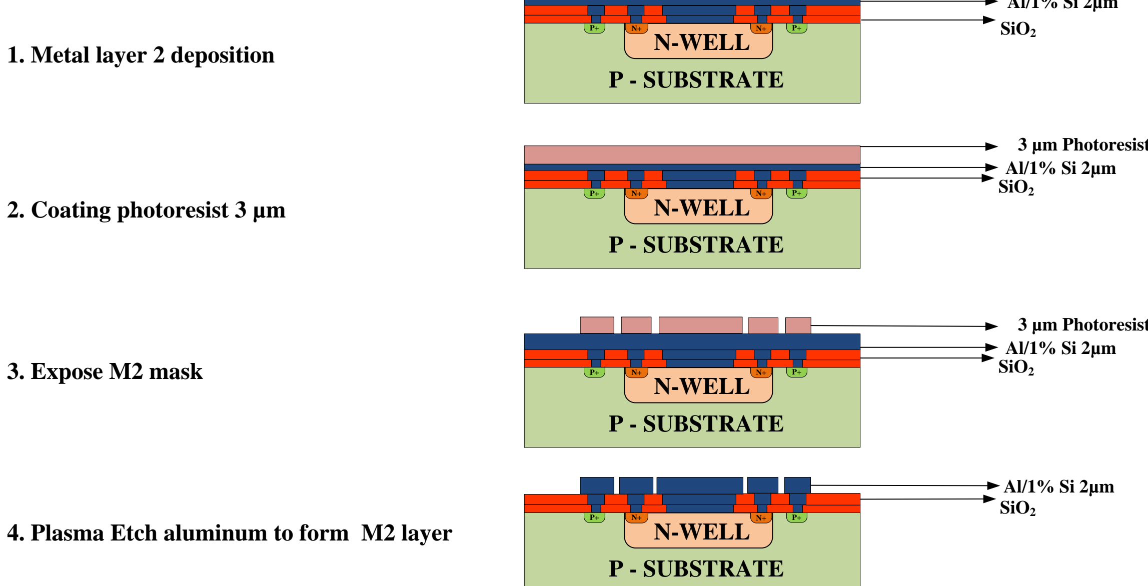

Figure 3.21 Metal 2 layer process steps

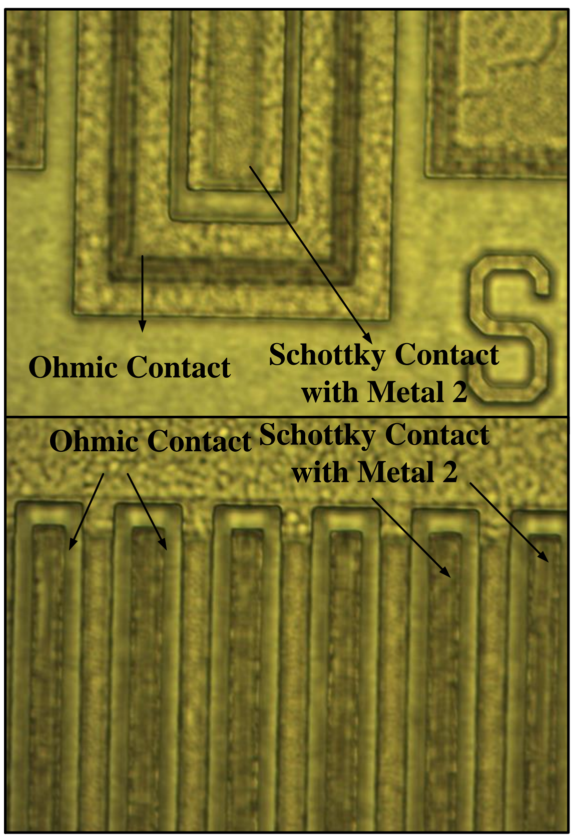

Figure 3.22 Metal 2 after patterning and etching

The final fabricated devices on wafer after metallization process is shown in Figure 3.23. The wafer consists of 3 dies with different schottky mask design. One die with integrated rectifiers. A generic DIMES BiCMOS design chip and designs of the student projects in BiCMOS process. Each design is fabricated on a 6mm x 6mm die in a 4 inch wafer

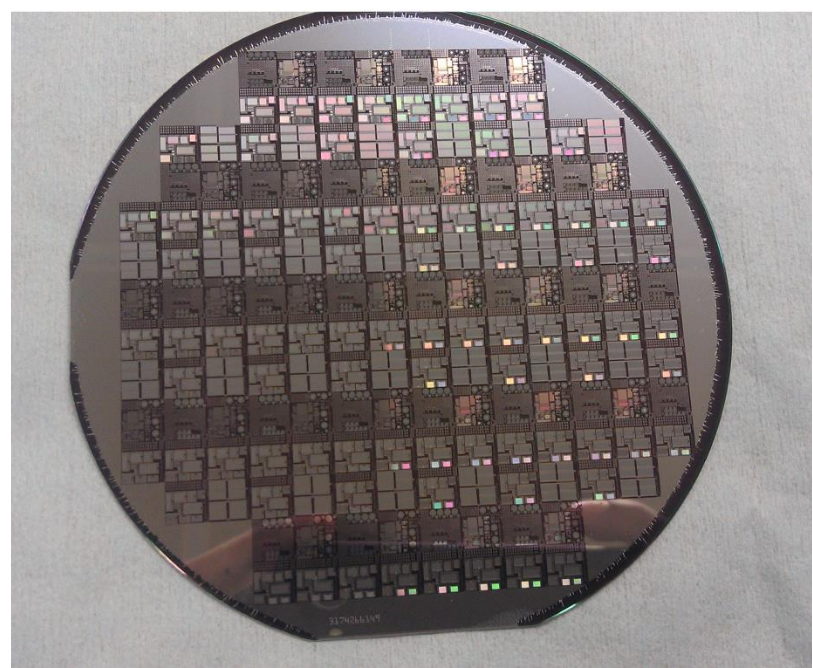

Figure 3.23 Wafer after metallization and alloying step

3.2 Measurement and Characterization of Schottky diodes

As described in the previous section, the two main schottky diode configurations that were designed are low current schottky diodes and high current schottky diodes. The electrical measurements are done using cascade probe station with Agilent ICCAP software. The important measurements performed for schottky diodes are forward IV measurements, reverse IV measurements, capacitance measurements and temperature measurements. A spice model is extracted from the measurement data for circuit analysis.

3.2.1 Measurements of low current Schottky diodes in BiCMOS7 process

The measurement for the low current schottky diodes is done by choosing three wafers having different NW dose. The wafers chosen are with phosphorus implant dose of 3 x 10^{12} cm^{-3}, 6 x 10^{12} $cm^{-3}$and 9 x 10^{12} cm^{-3}. In each wafer the schottky length is fixed as L = 250 µm. In the structures, the width (W) of the schottky contact and the distance (D) between the schottky and ohmic contact are varied. The different layout structure fabricated in the process are schottky

contacts with rectangular mask, schottky contact with cylindrical mask and schottky contact with cylindrical mask and guard rings. An example mask layout is shown in Figure 3.24.

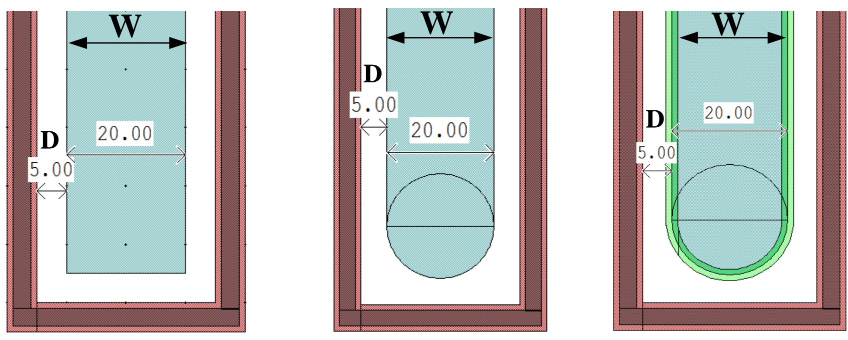

Figure 3.24 Schottky diode structures for measurements rectangular, cylindrical and cylindrical with guard rings (from left to right)

For the low current schottky diodes, 5 samples in each wafer for the various structures are measured. In this measurement the part of the wafers without V_T adjusts are taken into consideration as described in Figure 3.15 The complete wafer measurement with V_T adjusts are done for high current schottky diodes described in the next section. The complete measurement results for low current schottky diodes are tabulated in Table 3.1. The schottky diode is biased from -2V to 2V and the IV characteristics is noted. The semiconductor parameter analyzer used for measurement has a compliance value of 100mA. The forward voltage required to achieve a current of 100mA is noted for each of the structures on different wafers and the average values are tabulated. An example test structure of schottky diode on the wafer is shown in Figure 3.25.

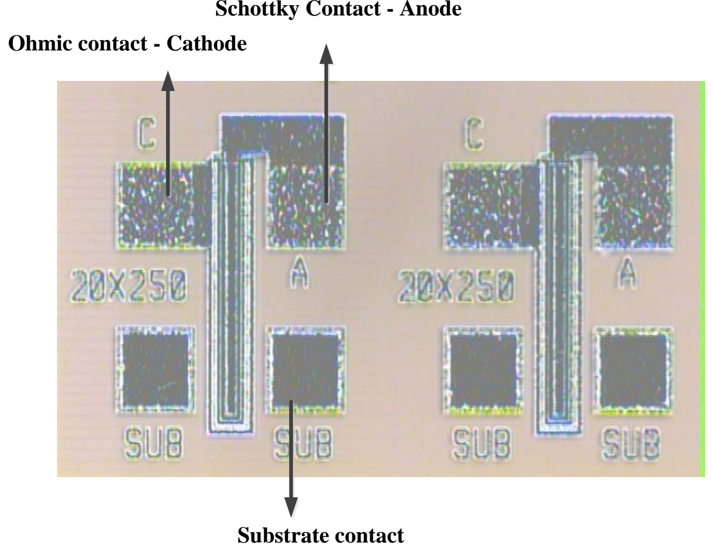

Figure 3.25 Test structure for measurement of schottky diode W=20μm D=5μm

Table 3.1 Measurements of Schottky diodes (L = 250μm) with different W and distance D to determine V_F for I_F = 100mA and breakdown voltage

Implantation dose of phosphorus cm^{-2}	Width (W) μm	Distance (D) μm	Rectangular		Cylindrical		Guard ring	
			V_F	BV	V_F	BV	V_F	BV
3e12	70	10	1.2	21	1.21	23	1.6	17.5
		5	1.18	21.4	1.3	22	1.4	16
		2	1.15	21	1.3	22.5	1.45	15
	20	10	1	20.9	1.1	21.3	1.5	15
		5	1.1	20.9	1.2	21.3	1.5	15.5
		2	1.1	19.8	1.16	20.2	1.32	17
	10	10	1.01	20.8	1.1	21.8	1.2	14.8
		5	1.13	20.9	1.14	22.3	1.4	14.5
		2	1.13	1	1.13	3.2	1.4	15.4
	5	10	1.03	21.9	1.03	22.6	1.3	17.5
		5	0.99	22.4	1.35	23.4	1.45	17.9
		2	1.06	0.2	1.07	1	1.1	17.6
	3	5	1.09	24.08	1.19	24.6	1.19	16
		2	1.09	0.2	1.09	0.2	0.99	16.2
6e12	70	10	1.19	20.4	1.21	21.4	1.6	29.8
		5	1.13	20	1.4	20.6	1.62	28.4
		2	1.1	20.3	1.4	20.4	1.65	28.4
	20	10	1.01	14.5	1.05	14.8	1.3	27.2
		5	0.98	14.2	1	14.4	1.7	26.8
		2	0.92	14.1	1.15	14.3	1.2	26.6
	10	10	1.02	14.6	1.05	14.9	1.25	27.8
		5	0.99	14.8	1.1	14.9	1.46	26.4
		2	0.96	13.9	1.2	14	1.24	26.2
	5	10	1	14.8	1.02	15.3	1.2	26.8
		5	0.99	15.4	1.14	15.6	1.3	26.6
		2	0.95	14	1.18	14.9	1.2	26.2
	3	5	1.01	15.8	1.2	16	1.3	26.4
		2	0.9	14	1.02	14.2	1.1	15.6

Implantation dose of phosphorus cm^{-2}	Width (W) µm	Distance (D) µm	Rectangular		Cylindrical		Guard ring	
			V_F	BV	V_F	BV	V_F	BV
9e12	70	10	1.2	15.3	1.21	15.9	1.4	25
		5	1.15	15.5	1.23	16	1.5	23.2
		2	1.15	13.5	1.25	14	1.4	23.2
	20	10	1.03	12	1.05	12.23	1.3	24.4
		5	0.99	12.07	1.1	12.5	1.2	22.8
		2	0.93	11.8	0.95	12	1.1	22.2
	10	10	1	12.4	1.03	12.8	1.15	22.4
		5	0.99	12.2	1.1	12.5	1.3	22.2
		2	0.95	11.4	1.03	12	1.2	22
	5	10	1	12.6	1.03	12.8	1.2	22.5
		5	0.96	12.2	1.01	12.6	1.3	22
		2	0.95	12	1	12.2	1.3	22
	3	5	0.97	12	1.1	12.2	1.3	22.4
		2	0.95	11.5	1	11.9	1.2	16.2

The following points can be deduced from the measurement data of IV characteristics,

1. The parameters that mainly influence the forward current are the N-Well doping concentration, the schottky contact width (W) and the distance between schottky contact and ohmic contact D.

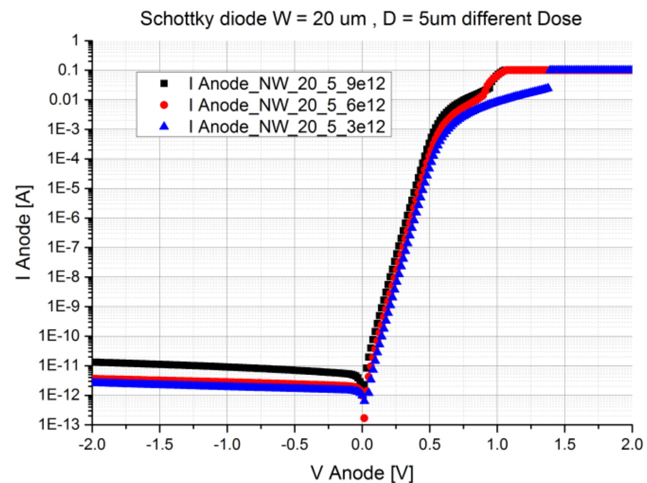

Figure 3.26 Schottky diodes W = 20µm, D = 5µm for different NW dose

With higher doping concentration, the current conduction is high at low forward bias as shown in Figure 3.26 considering the example of schottky diode with W = 20µm and D = 5µm. The average V_F at I_F = 100mA for n-well 3e12 is 1.1V, for 6e12 it is 1V and for 9e12 it is 0.96V.

2. The schottky contact mask with guard ring structure has lower reverse current than schottky contact mask with rectangular or cylindrical structure as shown in Figure 3.27. But the current at low bias for schottky diode with guard ring is lower than the schottky diodes without guard ring due to the influence of the p+ junction as discussed before.

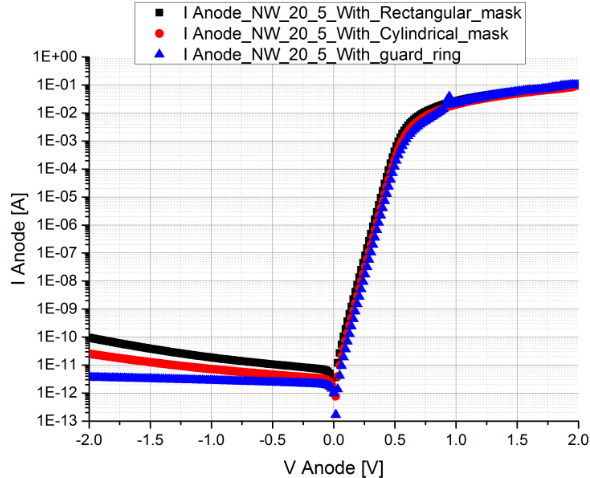

Figure 3.27 Schottky diodes W = 20µm, D = 5µm for different layout design

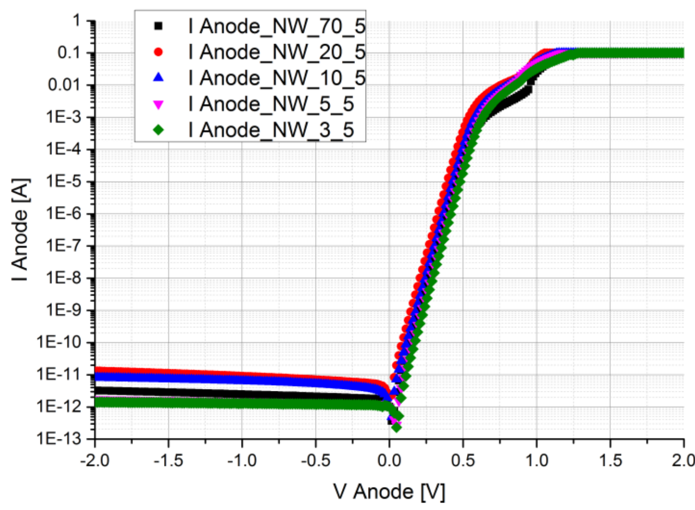

Figure 3.28 Schottky diodes with different schottky contact width W

3. The influence of the schottky contact width (W) on the forward current is shown in Figure 3.28. The larger the width W the lower the current at low bias voltage. With increasing schottky contact width W the resistance in the n well region plays a role to reduce the current conduction. As seen the current at same bias for schottky contact width W = 70μm is less than the current for the schottky diode with W = 5μm.

4. The influence of the distance between ohmic contact and schottky contact (D) is shown in Figure 3.29. The smaller the distance the current conduction is higher. The spread resistance in the region between ohmic contact and schottky contact reduces with smaller D. This characteristic follows the analytical and simulation analysis done in chapter 2.

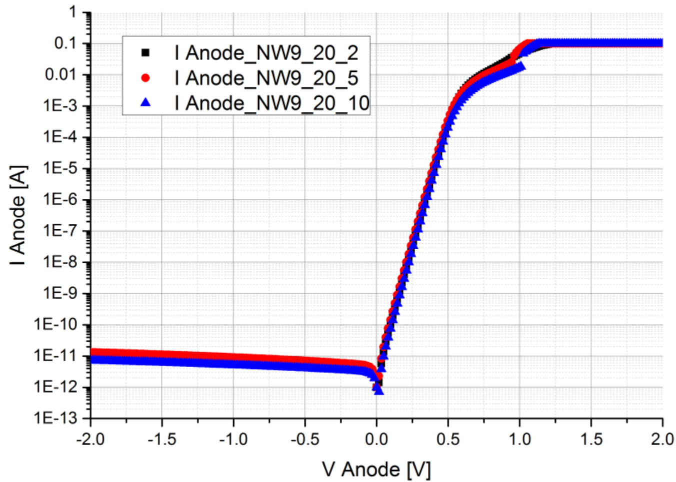

Figure 3.29 Schottky diodes with different distance D

In summary from the above points, the forward conduction of the schottky diode is highly dependent on doping concentration of the n-well, schottky contact width (W) and distance (D). Using higher doping of n-well, with reduced distance between schottky and ohmic contact (D) yields higher current.

Next the analysis of breakdown voltage of the schottky diode from the data in table is discussed in the following points below,

1. In the previous chapter the analytical analysis yields that the breakdown voltage is highly dependent on the doping concentration of the n-well. Lower the doping concentration, lower the reverse current and higher the breakdown voltage. By controlling the dose of the n-well we can achieve lower doping in the n-well region as verified previously. From measurement data of Table 3.1and Figure 3.30 to Figure 3.33 it can be seen that with lower n-well dose the breakdown voltage is higher. The average breakdown voltage for n-well dose of 3e12 is about 21V, for 6e12 it was 20V and for 9e12 it is around 15V for rectangular schottky contact mask. The schottky layout with

cylindrical contacts showed a slightly higher breakdown about 5%. This is not too large when compared to the rectangular layout. The average value is 21V for 3e12, 22V for 6e12 and 16V for 9e12. For schottky diode with guard ring there is large increase in breakdown voltage and large decrease in the reverse saturation current for n well dose of 6e12 and 9e12. The average value of the breakdown voltage is 29V for 6e12 and 24V for 9e12. For 3e12 the breakdown voltage with guard ring did not show significant improvement. This could be due to the fact that punch through might occur due to lower thickness of n-well.

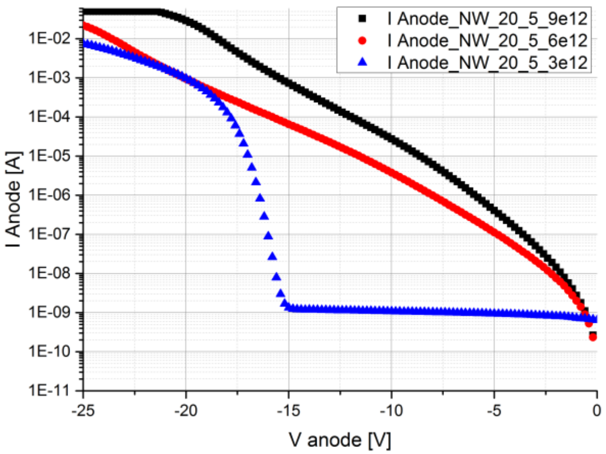

Figure 3.30 Breakdown Voltage for W = 20µm, D = 5µm for different NW dose – Rectangular schottky contact mask

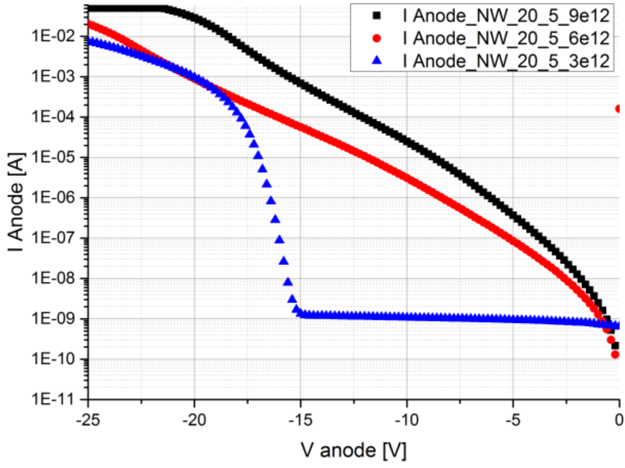

Figure 3.31 Breakdown Voltage for W = 20µm, D = 5µm for different NW dose – Cylindrical schottky contact mask

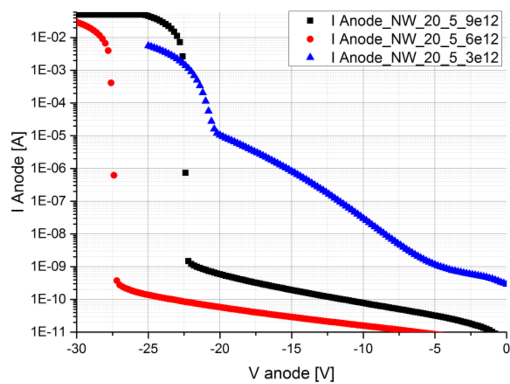

Figure 3.32 Breakdown Voltage for W = 20µm, D = 5µm for different NW dose – Cylindrical schottky contact mask with guard ring

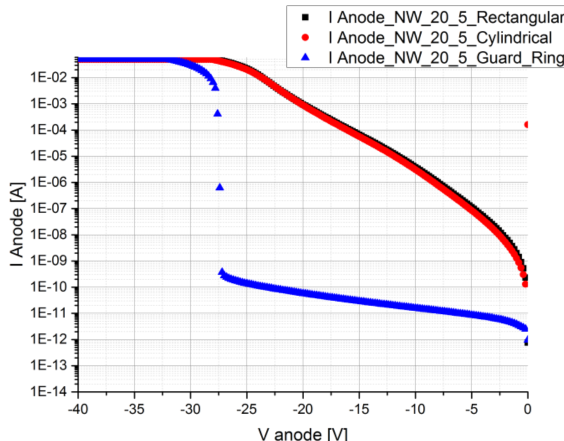

Figure 3.33 Breakdown Voltage for W = 20µm, D = 5µm for different layouts

2. The influence of the layout dependency on breakdown voltage is shown in Figure 3.35. The cylindrical layout structure for the schottky contact did have a small effect on the breakdown voltage. The breakdown voltage increase to about 5%. But the predominant effect on the breakdown voltage can be seen with the addition of guard ring structure. The breakdown voltage increase to about 30% when compared to breakdown voltage without guard ring structure.

3. The variation of breakdown voltage for guard ring structure with different width of the schottky contact is shown in Figure 3.34for n-well of 9e12 and Figure 3.35 for n-well of 6e12. It can be seen that the increase in width of the schottky contact does not have a much effect on the breakdown voltage. The reverse current is lower but for lower width W of the schottky contact.

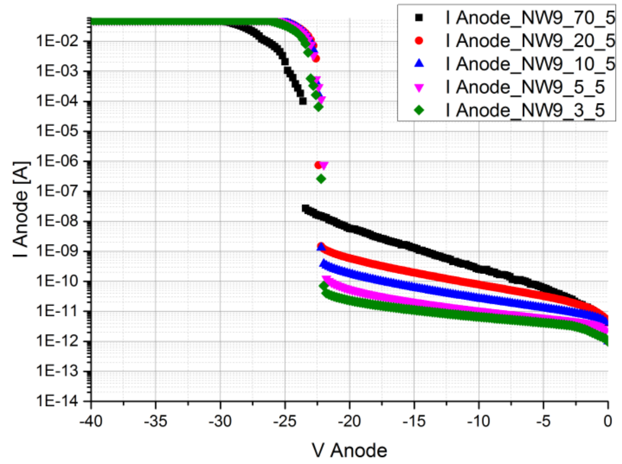

Figure 3.34 Breakdown Voltage for different schottky contact width W - NW9e12

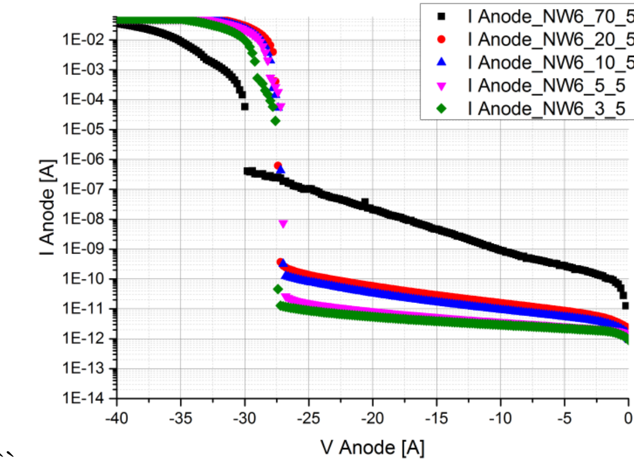

Figure 3.35 Breakdown Voltage for different schottky contact width W - NW6e12

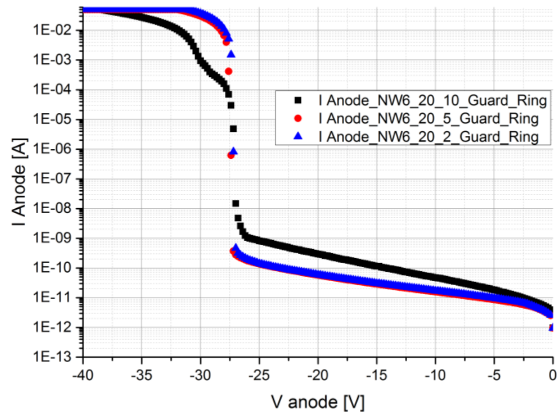

Figure 3.36 Breakdown Voltage for different distance D - NW6e12

4. The influence of the separation between schottky contact and ohmic contact (D) is shown in Figure 3.36 From the Table 3.1, the variation in the breakdown voltage with decreasing D is large for schottky diodes without guard ring structure. The breakdown voltage is similar for the range of D between 5µm and 10µm. But with lowering of D to about 2µm, the diodes breakdown as low as 1V. But with the addition of guard ring structure a higher breakdown is achieved similar to the structure with D = 5µm.

In summary of breakdown analysis from the measurement data, it can be seen that the breakdown voltage is increased to about 30% by the addition of p+ guard ring to the edge of the schottky contact. The distance 'D' between the schottky contact and ohmic contact should be kept at a minimum of 5 µm to achieve higher breakdown of the devices. Highest breakdown was achieved for n well dose of 6e12 with p+ guard ring in the range of 26-29V.

From the measurement of forward and reverse characteristics, in order achieve high current and high breakdown in this process the following are the main points deduced,

1. Schottky diode must have a p+ guard ring structure having doping with n-well dose of 6e12-9e12 (with depth of 3µm from drive-in time of 8hrs).
2. The minimum separation D between the schottky contact and ohmic contact should be 5µm to achieve reliable breakdown with p+ guard rings.
3. The width of the schottky contact (W) should be in the range of 5µm -20µm.

3.2.2 Measurements of high current Schottky diodes in BiCMOS7 process

The structures used for the measurement for high current schottky diodes are done by choosing wafers having different NW dose. From the previous analysis, for high current measurements the schottky diodes having width W = 5µm to 20µm with distance D = 5µm are chosen. The wafers are with phosphorus implant dose of 3 x 10^{12} cm^{-3}, 6 x 10^{12} $cm^{-3}$and 9 x 10^{12} cm^{-3}. In each wafer the forward and reverse characteristics of schottky diodes having guard rings with 50 fingers is used. The forward voltage is determined for a forward current I_F of 1A. In each wafer 24 dies having schottky diode with guard ring structures are tested. To study the effect of V_T adjust on the forward current and breakdown voltage, 6 dies in each quadrant of the wafers are measured. The average forward voltage drop for a forward current of 1A and the breakdown voltage is tabulated in Table 3.2. An example test structure of high current schottky diode with W = 20 µm and D = 5µm with 50 fingers on the wafer is shown in Figure 3.37.

Table 3.2 Measurements of Schottky diodes with guard ring - V_F for I_F = 1A

Implantation dose of phosphorus cm^{-2}	Schottky Diode Layout (W,D)	Schottky contact area mm^2	V_F	BV
3e12	20, 5 – 50 Fingers	1	0.8	14.5
	10, 5 – 50 Fingers	0.5	0.76	14.4
	5, 5 – 50 Fingers	0.25	0.77	13.2
6e12	20, 5 – 50 Fingers	1	0.73	27
	10, 5 – 50 Fingers	0.5	0.7	26.8
	5, 5 – 50 Fingers	0.25	0.68	27
9e12	20, 5 – 50 Fingers	1	0.68	22.5
	10, 5 – 50 Fingers	0.5	0.67	22.4
	5, 5 – 50 Fingers	0.25	0.66	22

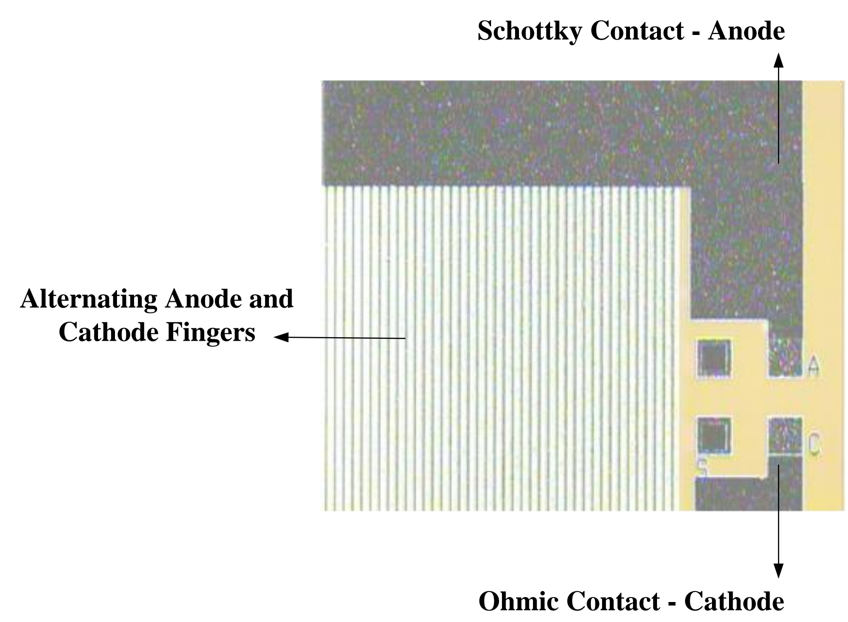

Figure 3.37 Test structure of high current schottky diode W=20μm D=5μm 50 fingers

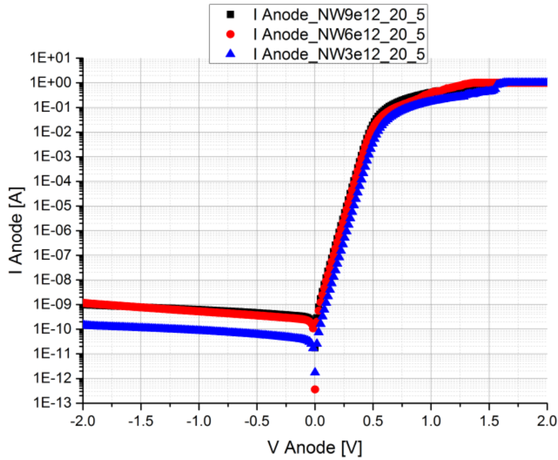

Figure 3.38 Schottky diodes W = 20µm, D = 5µm, 50 fingers for different NW dose

The data provided in the Figure 3.38 is the IV characteristics with single probe measurements to analyze the different data structures equally. The data tabulated in Table 3.2 is the IV characteristics by using two probe measurements at anode terminal. This type of measurement reduces the effect of contact resistance of the probe and it can be seen that the there is about 200mV to 300mV voltage drop due to the resistance of the probe. From the Figure 3.39, it can be seen that as doping increases the current conduction of the schottky diode at low bias increases. The current is highest for schottky diode with NW dose of 9e12. Hence a high doping ensures higher current for the same area of the schottky diode.. The forward voltage at I_F = 1A is the least for N-Well 9e12 which is 0.65V.

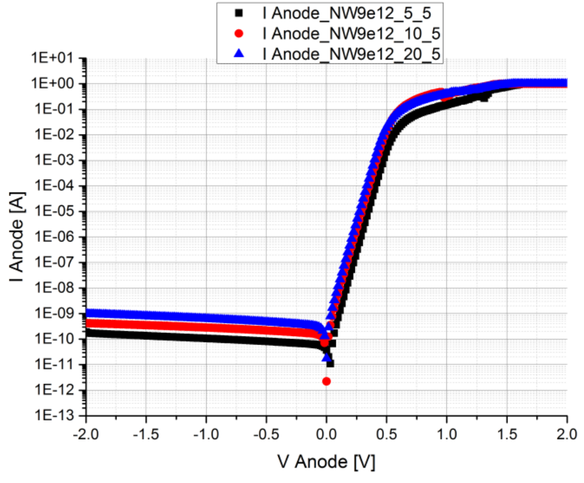

Figure 3.39 High current Schottky diodes with different width W for NW = 9e12

The highest current at low forward bias is obtained for schottky diode with W = 20µm and W = 10µm as shown in Figure 3.39. Hence a higher width W provides a better current conduction at low bias. A similar observation is made in Figure 3.40to Figure 3.41for schottky diodes with n-well dose of 3e12 and 6e12.

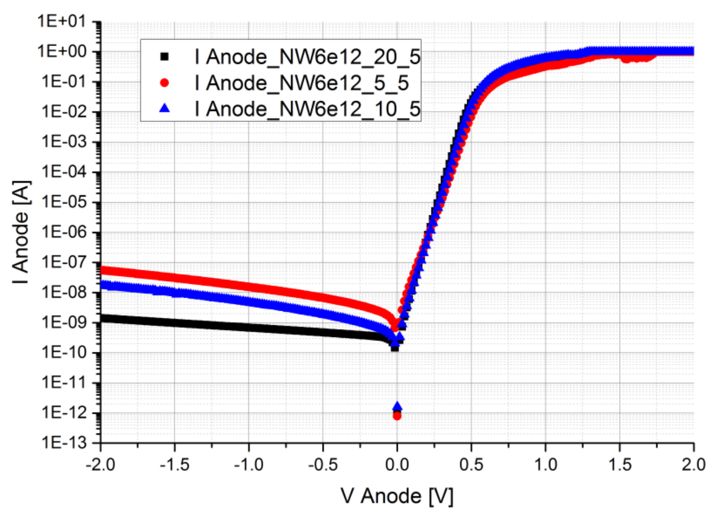

Figure 3.40 High current Schottky diodes with different width NW dose = 6e12

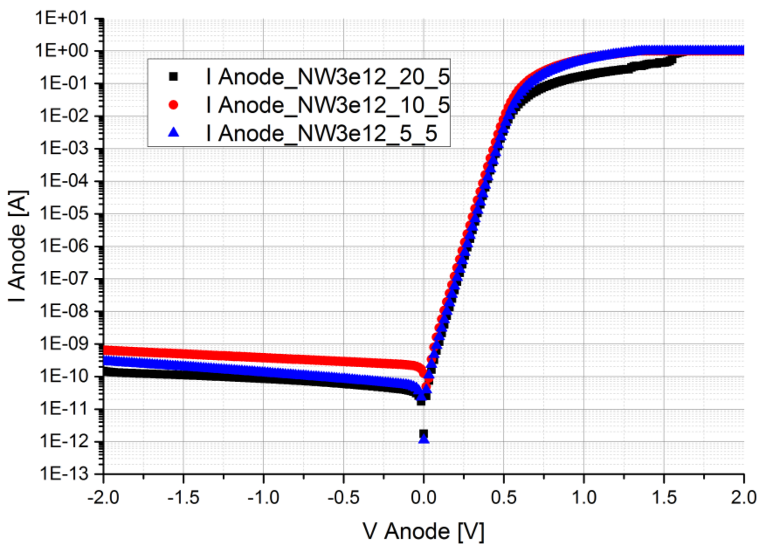

Figure 3.41 High current Schottky diodes with different width NW dose = 3e12

From the above forward characteristics measurement it can be seen that the schottky diodes having W = 20µm and D = 5µm with 50 fingers and schottky contact area 1.4mm^2 provide the lowest forward voltage drop of 0.65V at a forward current of 1A.

Next we perform breakdown analysis in these structures. The DC voltage is biased from 0 to -40V to study the breakdown behavior of the high current schottky diodes. The reverse characteristics for same structure with different doping concentration are shown in Figure 3.42. From the figure it can be seen that the doping concentration has a significant effect on the breakdown voltage of the schottky diode. For NW dose of 9e12, 6e12 and 3e12 the average breakdown voltage is 22.5V, 26.8, 15.8 respectively. The breakdown voltage for dose of N well 3e12 shows a similar behavior as that of the low current schottky diodes. This could be the fact

that the lower n-well doping concentration has lower n-well depth for the same drive-in time as discussed in chapter 2.There is a possibility of punch through with high reverse bias voltage at the n-well and substrate junction.

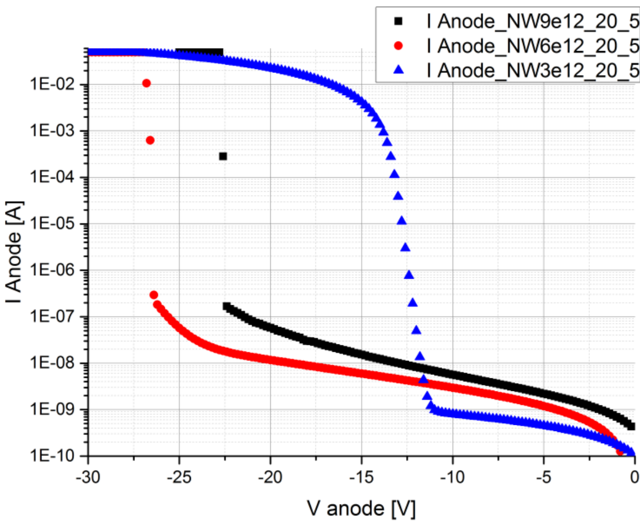

Figure 3.42 Schottky diodes W = 20µm, D = 5µm, 50 fingers for different NW dose

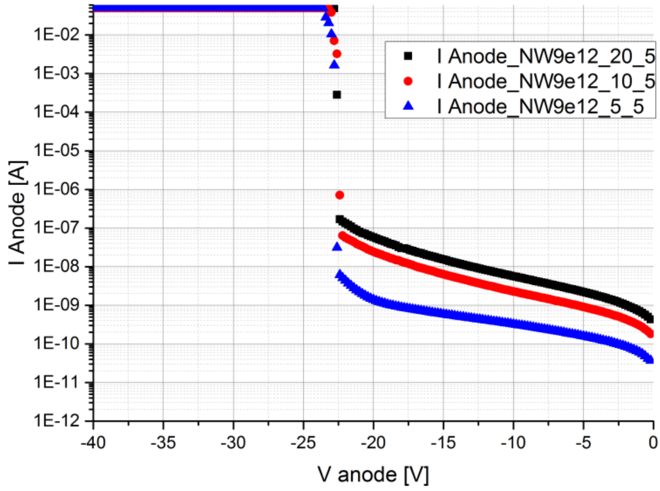

Figure 3.43 High current Schottky diodes with different width NW dose = 9e12

From the Figure 3.43, it can be seen that the as schottky contact width decreases the breakdown voltage also decreases. The device structure with width W = 20µm and distance D =5µm provides the highest breakdown voltage. Thus a higher width of the schottky contact W is preferred for higher breakdown voltage. A similar behavior is observed for the breakdown voltage behavior of the devices with n-well doping of 3e12 and 6e12 shown in Figure 3.44 and Figure 3.45.

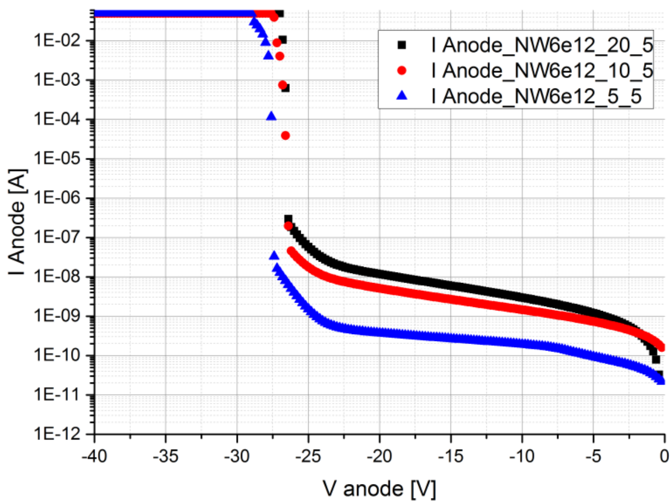

Figure 3.44 High current Schottky diodes with different width NW dose = 6e12

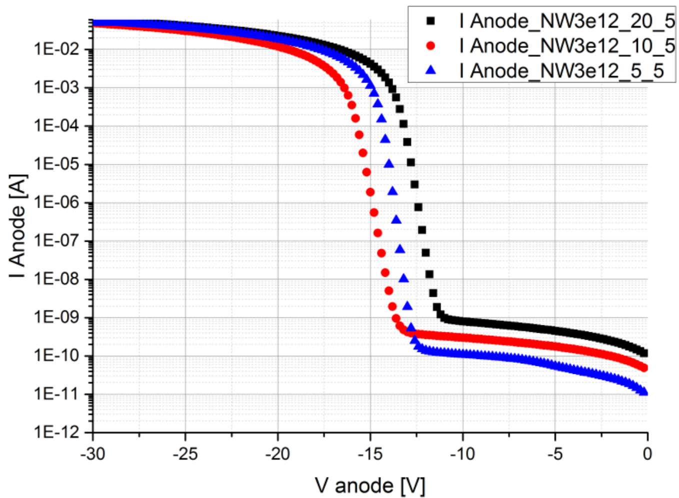

Figure 3.45 High current Schottky diodes with different width NW dose = 3e12

From the breakdown analysis of the fingers structure schottky diode it can be seen that the best device with the highest breakdown with large number of devices exhibiting similar behavior is achieved for a doping concentration of 6e12 and width W = 20µm and D = 5µm. The diodes with less W had large number of devices that breakdown with repeated reverse voltage bias. Thus the schottky diode with width W = 20µm and D = 5µm used in the design of integrated rectifiers will show better performance.

One of the factors to consider the behavior of the schottky diodes due to the processing steps of extended HF dip etch. The wafers with schottky diode were dipped in 0.55 % HF solution for 10 mins to remove the native silicon di-oxide residues at the schottky metal interface. All the wafers followed this procedure except a test wafer which did not have the

extended HF dip etch. The HF dip was done only for 4 mins. The variation of the current characteristics of the schottky diodes with and without HF dip is shown in Figure 3.46

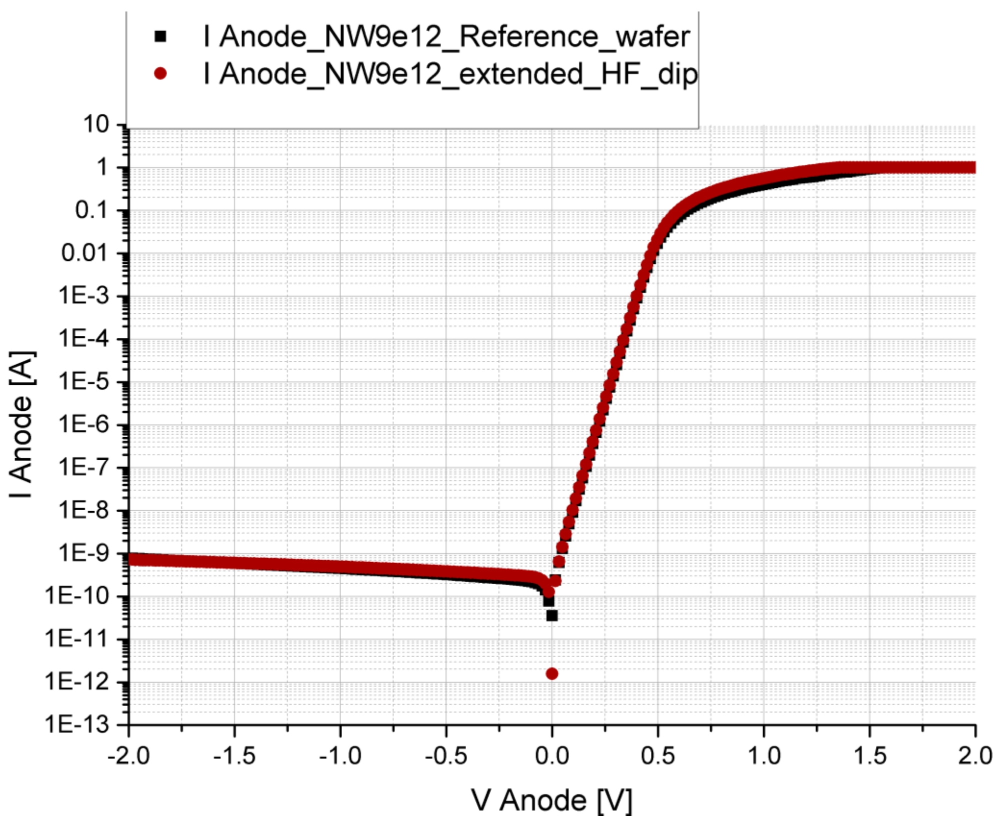

Figure 3.46 High current Schottky diodes comparison with extended HF dip

The current at low bias for schottky diodes with extended HF dip showed a slight improvement of about 5% in current but a significant increase was not seen. This could be the fact that the native oxide particles are still present on the schottky contact openings. One method to have a better surface passivation of the schottky contact is to increase the time of HF dip more than 10mins.

3.2.3 Temperature measurements of high current Schottky diodes

The next measurement setup was done to study the effect of temperature on the forward and reverse characteristics of the schottky diodes. The temperature was varied from room temperature to 150 degrees. The effect on the forward bias characteristics for different temperature is shown in Figure 3.47. The corresponding reverse bias characteristics are shown in Figure 3.48.

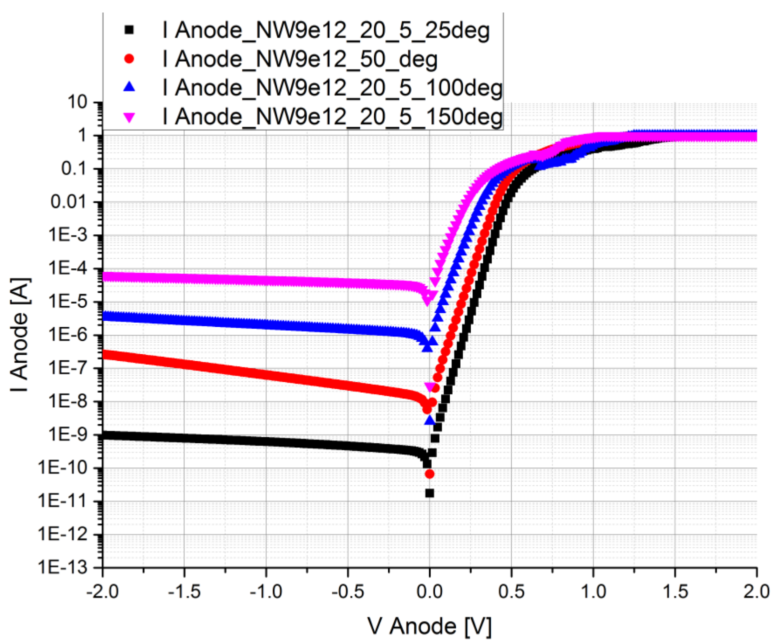

Figure 3.47 High current Schottky diodes temperature characteristics forward IV

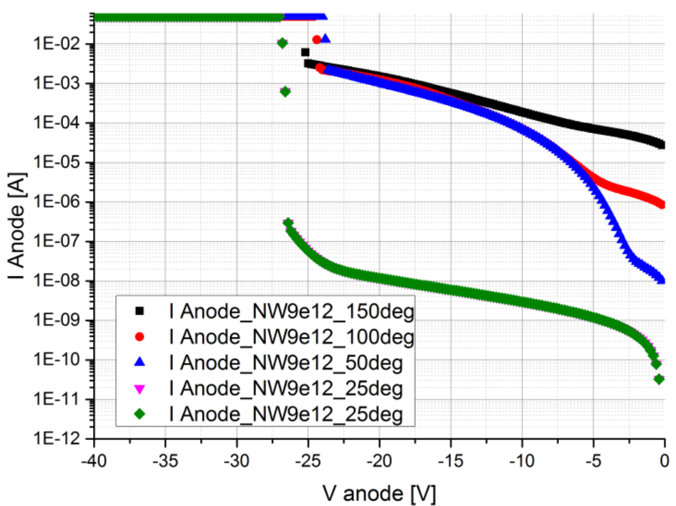

Figure 3.48 High current Schottky diodes temperature characteristics reverse IV

From the temperature measurements it can be seen that the reverse current increases as temperature increases. The breakdown occurs at a lower voltage value than at room temperature. Although silicon provides good thermal conductor for heat dissipation, a better method for thermal management needs to be investigated. At high temperatures, the schottky diodes breakdown much faster. This thesis does not focus much on the temperature characteristics.

3.2.4 Spice Model of Schottky diodes

The spice model of schottky diodes consists of mathematical equations, parameters, and all the variables which are derived in such a way that they can simulate the complete device as accurately as possible in a simulator supporting spice models of semiconductor devices. The accuracy in which the parameters are extracted depends on the extraction methodology. The large signal equivalent circuit of a schottky diode is shown in Figure 3.49. The circuit consists of an ideal diode with a forward voltage drop of V_F in series with a resistor R_S. This is the resistance of the diode is in saturated forward bias condition. G_{MIN} is the shunt conductance across the junction.

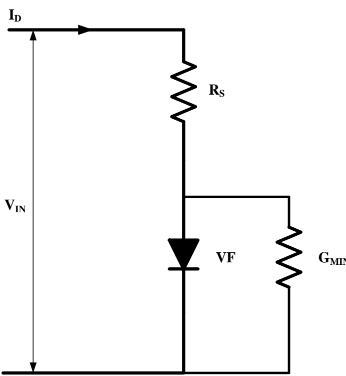

Figure 3.49 Large signal equivalent circuit of Schottky diode

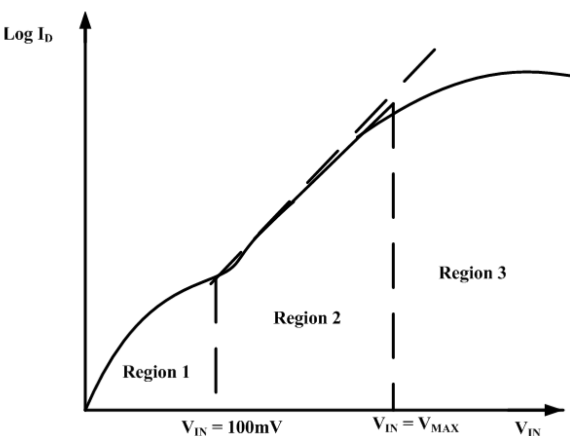

Figure 3.50 Regions in forward IV characteristics

In Figure 3.50 Region 1 is the region at low forward voltage bias under 100mV caused due to extreme low level injection of carriers across the junction. Region 2 operated in low level injection and the diode is almost ideal. The current increases rapidly for low changes in voltage. This happens until the maximum value of V_{IN} is reached where the series resistance of the diode

comes into effect and it is the Region 3. The slope of the line in Region 2 gives the ideality factor of the diode. The main measurements that are made to extract the dc parameters for the spice model of the diode are forward IV measurements, reverse IV measurements and Capacitance-Voltage measurements. The main parameters extracted for each measurement data is shown in Table 3.3.

Table 3.3 Measurements of Schottky diodes and extracted model parameter

Measurement	Extracted Model parameter
Forward IV measurements	IS,RS,N
CV measurements	CJO,VJ,M
Breakdown	BV, IBV

1. **Forward IV Measurements :**

The measurements were done on cascade probe station and ICCAP software. The forward bias was increased from -2V to 2V. For extraction of ideality factor N, the region 2 of the IV curve in Figure 3.50 is used for parameter extraction. The slope of this line gives the ideality factor N. The extractions of N for schottky diode W = 20μm and D = 5μm having 50 fingers is shown in Figure 3.51. The parameter Rs is extracted from the high bias region using the method in as shown in Figure 3.52

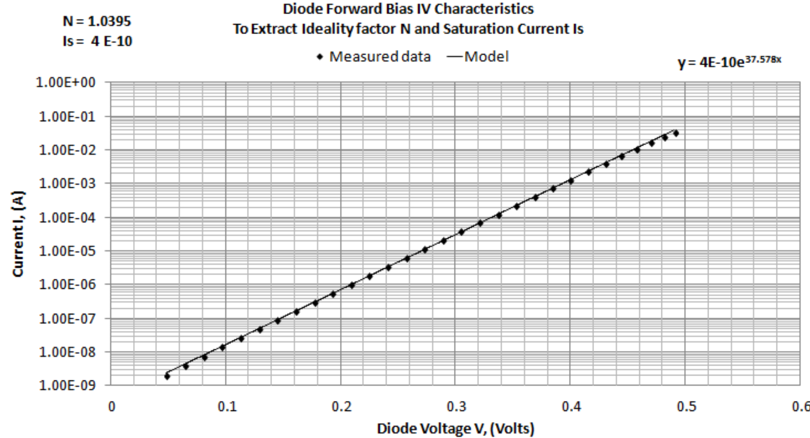

Figure 3.51 Extracting Ideality factor N for N-well dose = 9e12

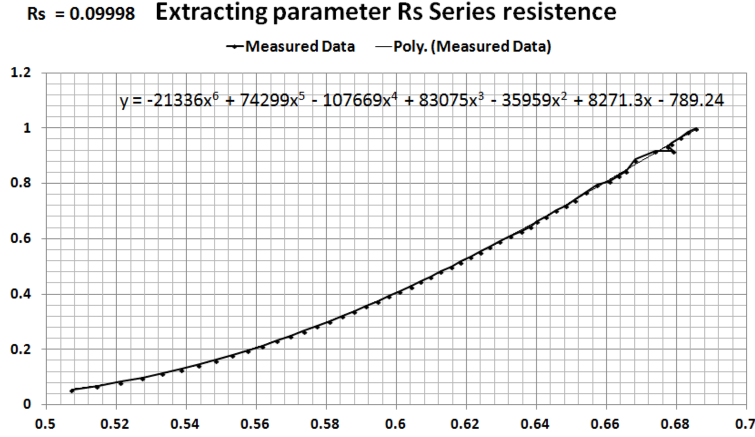

Figure 3.52 Extracting factor Rs for N-well dose = 9e12

2. Capacitance Measurement :

The capacitance measurements were by reverse biasing the schottky diode from 0 to -3V. The CV characteristics obtained is shown in Figure 3.53. The capacitance for large area schottky diode is in the range of 600pF to 800pF

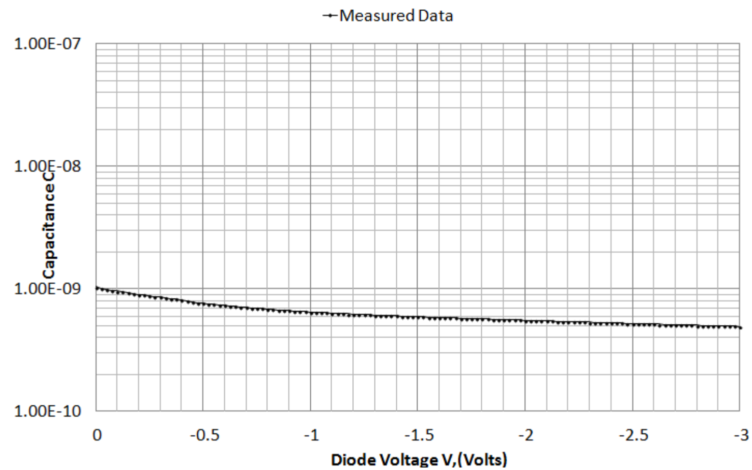

Figure 3.53 Capacitance – Voltage characteristics of schottky diode

The capacitance parameters have a strong dependency on the area of the schottky diode. As the area increases the capacitance also increase. Hence, one of the disadvantages of large area schottky diode is the increase in capacitance of the device. A comparison of schottky diodes with area 1.23 sq mm and 0.23 sq.mm is shown in Figure 3.54. The capacitance of large diode is in the order of 800pF whereas the capacitance of the small diode is in the range of 200pF.

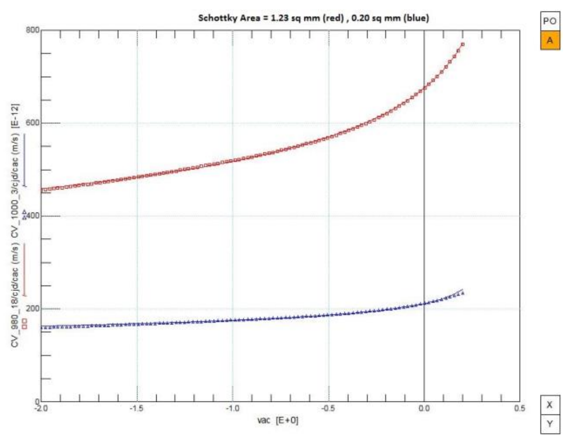

Figure 3.54 Capacitance – Voltage characteristics different area

3. **Breakdown characteristics :**

The reverse characteristics are done using the same approach as previously in the measurement of high current schottky diodes. From the Table 3.2 discussed before, the breakdown voltage and the current at breakdown IBV is derived.

Table 3.4 Spice model extracted parameters of high current schottky diode

Parameter	Name	NW9e12	NW6e12	NW3e12
IS	Saturation current	4E-10	2E-10	IS
RS	Ohmic resistance	0.09968	0.101	0.09
N	Ideality factor	1.03	1.02	1.0395
CJO	Zero bias junction capacitance	890pF	733pF	633pF
VJ	Contact potential	0.4298	0.26	0.13
M	Junction capacitance grading	0.277	**0.23**	0.2278
BV	Reverse breakdown	22.5	26.4	11.2
IBV	Current at reverse breakdown	1.35E-06	2.9E-07	1.85E-9

In order to extract the transit time and the reverse recovery time is parameter special setup is needed. The reverse recovery time of the diode is defined as the time that the current becomes negative and recovers to a value to about 10% of the peak reverse saturation current during the switching from forward bias to reverse bias. A JEDEC test circuit is required for the extraction of this parameter. The final parameters that are derived for high current schottky diodes using the spice model approach is shown in Table 3.4. The parameters EG – energy gap, XTI – Is temperature co-efficient are considered as default values. The above spice model is used for the LT spice circuit analysis.

3.3 Measurement and characterization of NPN BJT and NMOS in BiCMOS process

In the introductory part of the thesis a description for design proposal of simple linear driver and a buck driver is proposed. The driver for the LED module is a constant current driver. The linear driver and buck driver consist of components such as power MOSFETS, NPN bipolar transistor and resistors. The design proposal intends to integrate all these circuits and components in the standard BiCMOS process along with schottky diodes and rectifiers. For this purpose, first the electrical characterization is done to extract parameters for the spice model of basic NPN transistors, MOSFETS and sheet resistance structures fabricated along with the schottky diode wafers. The spice model is used for circuit analysis. In this section, a basic measurement procedure for extracting spice model using cascade probe station and ICCAP tool is described for NPN bipolar transistor, NMOS, PMOS fabricated in BiCMOS process.

3.3.1 Modeling and characterization of NPN Bipolar Transistors

Modeling and parameter extraction of an NPN bipolar junction transistor in steady state condition give a set of parameters that simulate the device characteristics in electrical circuit simulators. A UCB bipolar transistor model supported in simulators like LTspice is extracted from the measurement data using ICCAP. The UCB bipolar model is a combination of Eber's-Moll model and Gummel- Poon model [32]. From the schottky diode measurement analysis it is seen that the wafers with NW dose of 3 x 10^{12} cm^{-3} have poor performance in terms of both forward conduction and breakdown voltage. Thus, in the measurement and spice model extraction for BJT the wafers with NW dose of 6 x 10^{12} cm^{-3} and 9 x 10^{12} cm^{-3} are considered for measurements. The procedure for extracting the spice model parameters for npn transistor as described in [32] is followed to extract the DC parameters and CV parameters for the spice model of the transistor. A large signal schematic of Gummel-Poon model of bipolar junction transistor is shown in Figure 3.55[33]. This model describes the various resistors and capacitors that are formed in the BJT.

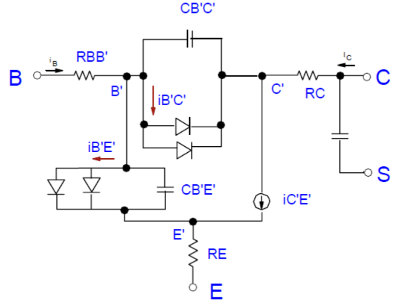

Figure 3.55 Large signal Gummel Poon model of BJT

In the measurement procedure first the data is measured with the set of bias voltages to the terminals of the transistors. The spice model parameter is extracted. Next this data is used to simulate to match with measurement data and the parameters are optimized. The structure used for the measurement of NPN BJT to build the spice model are with different emitter area varying from L_E = 10μ, 15μm, 20 μm and 40μm. An example test structure of NPN BJT used in the measurement is shown in Figure 3.56. For measurements, The procedure to determine the parameters of UCB model is discussed as follows [32],

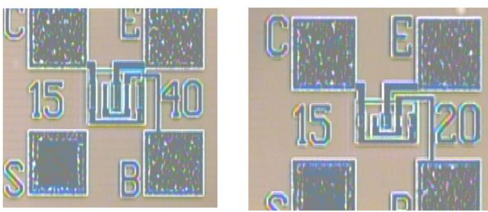

Figure 3.56 Test structure for BJT modeling

1. **Capacitance-Voltage Measurements :**

In a bipolar transistor, the main capacitances are due to the p-n junctions at the emitter-base junction (Cbe) and collector-base junction (Cbc). To determine this capacitance, the p-n junction is biased from a small forward bias to a large reverse bias voltage.

Table 3.5 CV measuremet procedure and extracted parameter

Measurement	Measurement data	Extracted Model parameter
Base-Emitter Capacitance Cbe	Vbe –- -0.6 to 0.6	CJE,MJE,VJE
Base-Collector Capacitance Cbc	Vbe –- -0.6 to 0.6	CJC,MJC,VJC

The plot of capacitance voltage measurement data for different emitter structure is shown in Figure 3.57.

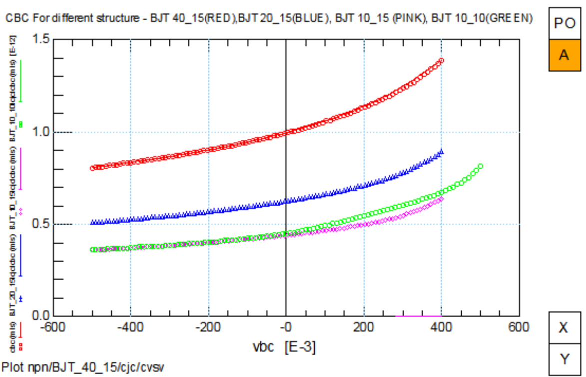

Figure 3.57 CV measurement (CBE) for different BJT structure

NPN transistor with width 40um and L = 15um (red) has a higher capacitance than the other configurations.

2. DC- Measurements :

The dc measurements are done in a bipolar transistor to extract large signal parameters of the transistor. The forward Gummel measurements and reverse Gummel measurements provide model data for forward gain β of the transistor and saturation currents I_S. Next the forward early and reverse early measurements are done to provide the parameters of forward early voltage and reverse early voltage. Some of the important parameters extracted are shown in Table 3.6

Table 3.6 DC Measurements

Measurement	Measurement data	Extracted Model parameter
Forward Gummel	Vbe – 0 to 700mV, I_C and I_B	β_F, I_{KF}, I_{SE}, N_E
Reverse Gummel	Vcb – 0 to 700mV, I_C and I_B	β_R, IKR, I_{SC}, N_C
Forward Early	Vcb vs I_C	V_{AF}
Output characteristics	V_{CE} vs I_C	R_B, R_E , R_C

Using the standard procedures in the ICCAP manual, the parameters are extracted, simulated and optimized from the measurement data. A plot of β_F vs V_{BE} is shown in Figure 3.58. The measured and simulated value of β_F agree closely. The output characteristics of the transistor are shown in Figure 3.59.

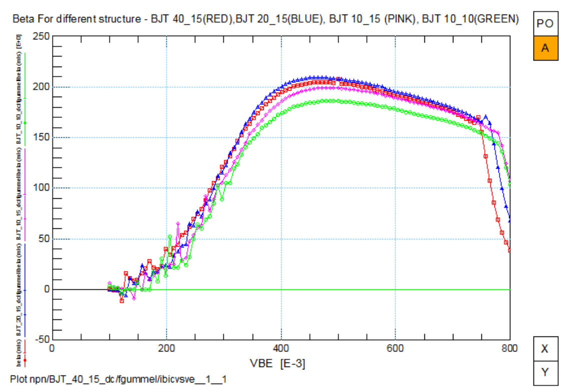

Figure 3.58 Large signal Gummel Poon model of BJT

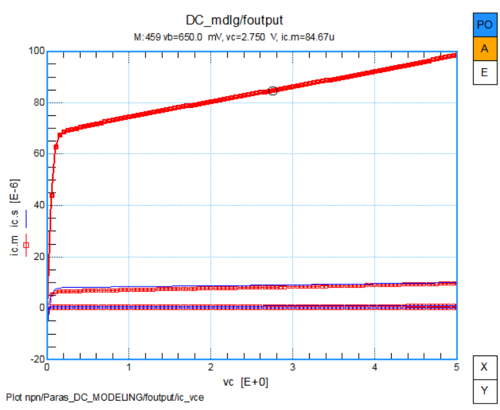

Figure 3.59 Large signal Gummel Poon model of BJT

The extracted parameter of NPN BJT is shown below

Table 3.7 NPN SPICE MODEL Parameters

Parameter	Name	NW6e12
BF	Forward Gain	186.6
IS	Transport Saturation Current	7.05731E-016
IKF	Knee Current	0.00278388
ISC	Base Collector Leakage Saturation Current	1E-017
NC	B-C leakage co-eeficient	1.7079

ISE	Base Emitter Leakage Saturation Current	3.03E-15
VAF	Forward Early Voltage	12
RE	Emitter Resistance	9
RC	Collector resistance	6
CJC	Base Collector capacitance	988E-15
CJE	Base emitter capacitance	1E-12
RB	Base Resistance	17

3.3.2 Modeling and characterization of NMOS Transistors

The MOSFET model obtained from the ICCAP tool and nmos measurement data of the BiCMOS chip is a spice level 3 model. This is developed by UCB group and it is fully compatible with spice simulators. In the modeling of mosfets first we need to have basic devices in the chip with different length and width. The mosfets parameters are specified for short channel and large channel devices. In this measurement procedure, the capacitance parameters we not extracted due to unavailability of specific capacitance structures having different area and perimeter factor of the source and drain regions [32]. The test structure used for the development of the model is shown in Figure 3.60. For short channel parameter extraction the device with length = 2μm is used. In case of long channel, the devices with 10μm are used.

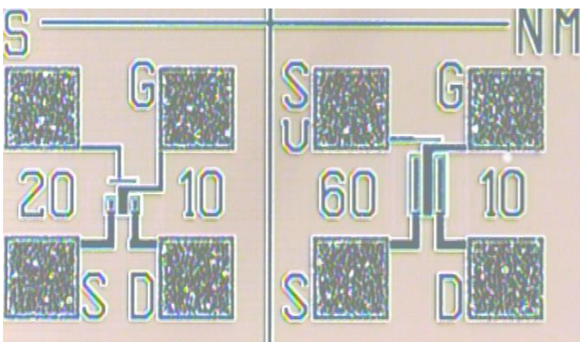

Figure 3.60 Test structure for NMOS modeling

Modeling and parameter extraction of an NPN bipolar junction transistor in steady state condition give a set of parameters that simulate the device characteristics in electrical circuit

simulators. A UCB bipolar transistor model supported in simulators like LTspice is extracted from the measurement data using ICCAP.

Table 3.8 DC measuremet procedure and extracted parameter

Measurement	Measurement data	Extracted Model parameter
Large nmos Id vs vg	I_D vs V_{GS} (0 , 1V)	NSUB, UO, UEXP, VTO
Narrow nmos Id vs vg	I_D vs V_{GS} (0 , 1V)	DELTA, WD
Short Id vs vg	I_D vs V_{GS} (0 , 1V)	LD, RD, RS, XJ
Short Id vs Vd	V_{CE} vs I_C	ETA, KAPPA

The main dc measurements are of two types. Drain current versus gate voltage I_D vs V_{GS} for different substrate bias and Output characteristics given by a plot of drain current versus V_{DS} for different Vgs. A plot of simulated and measured drain current versus gate voltage is shown in Figure 3.61

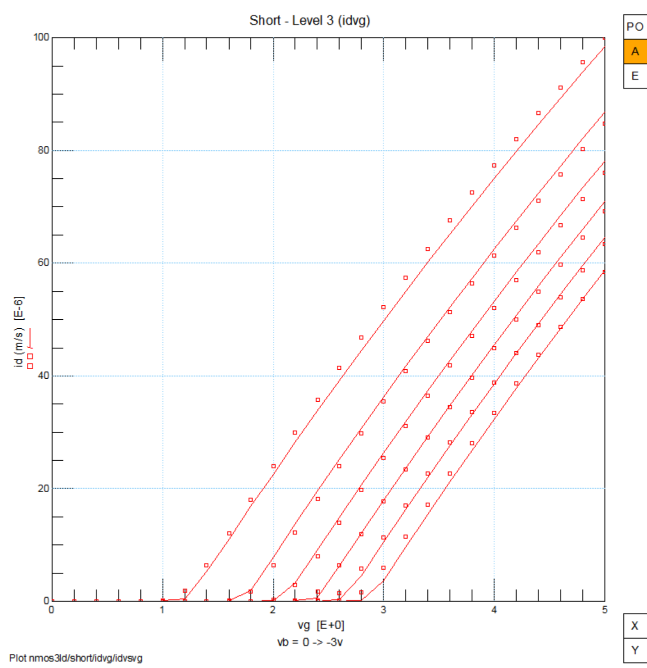

Figure 3.61 ID versus VGS to extract threshold voltage

From Id versus Vgs graph we can extract the threshold voltage parameter. The threshold voltage in the N-well 6e12 process was found to be between 1.2-1.5V. The simulated plot for the

extracted values follows closely with the measurement data. The output characteristics plot for Id versus Vds is shown in Figure 3.62.

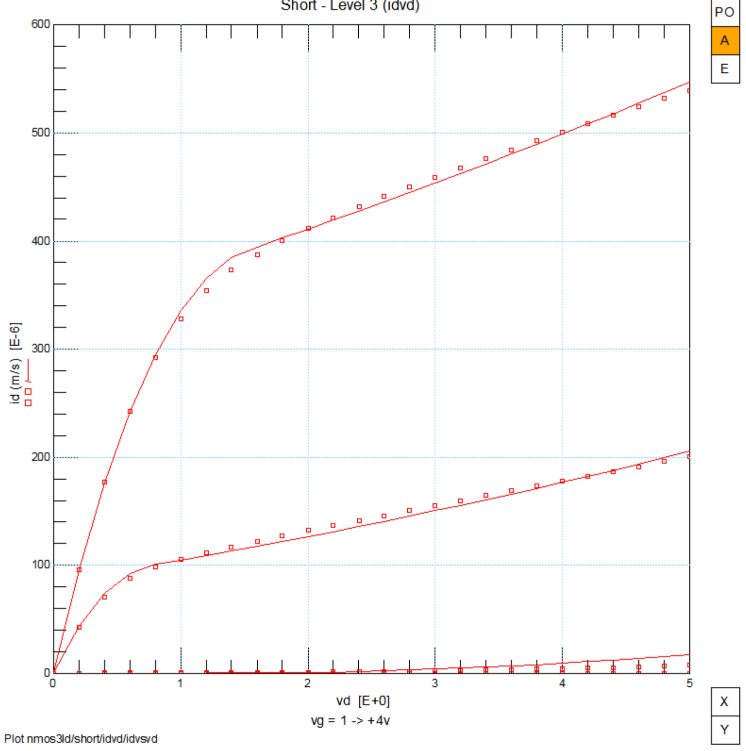

Figure 3.62 ID versus VDS

The nmos devices measured are small area devices. In the BiCMOS process there was also a power mos device that was fabricated. The power mos device serves as a key component in the linear and buck driver for LED. The test structure of power mos device is shown in the Figure 3.63.

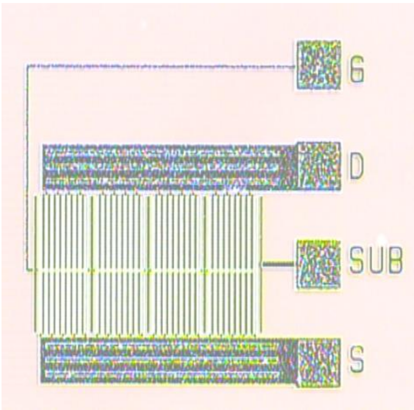

Figure 3.63 Power MOSFET Test structure

The area of this power mos device is 2mm. The output characteristics of the power mos device is shown in Figure 3.64

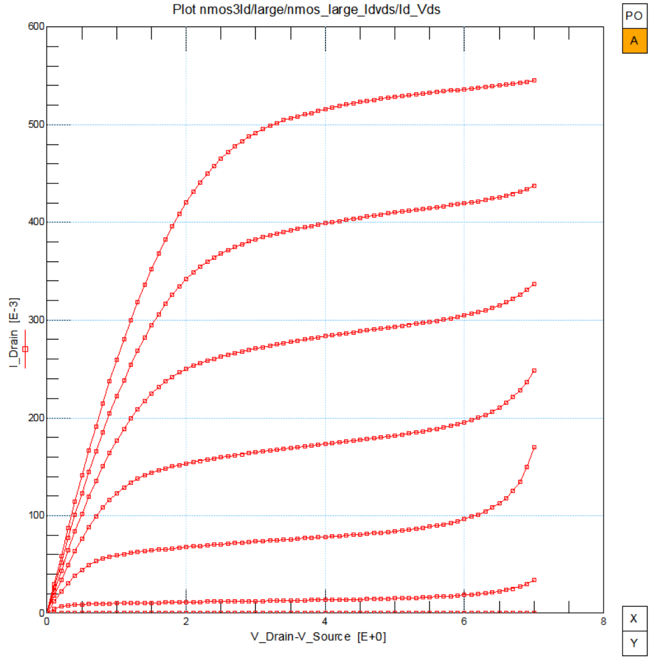

Figure 3.64 ID versus VDS for Power Mosfet

The output characteristics show that when the drain source voltage is 7V with Vgs at 4V, the mosfet can conduct up to 500mA current. Using the measurement data, the spice parameters of the mosfets is derived. NMOS device fabricated with a n-well doping of 6e12 and depth of 3um has the below spice parameter.

Table 3.9 NMOS SPICE Parameter extracted

Parameter	Name	NW6e12
VTO	Threshold Voltage	1.213
XJ	Metallurgical Junction Depth.	8.95118E-08
DELTA	Width Effect on Threshold Voltage	0.00278388
LD	Lateral Diffusion Coefficient	2.6670E-07
U0	Surface Mobility at Low Gate Levels	649.442
THETA	Mobility Reduction	1.650E-06

RSH	Sheet resistance	6.7955E+01
NSUB	Substrate Doping Concentration	5.00360E+15
NFS	Effective Fast Surface State Density	2.8500E+12
VMAX	Maximum Drift Velocity of Carriers	2.31329E+05
ETA	Static Feedback.	13.7153E-02
KAPPA	Saturation Field Factor	3.158E-01

Using the above spice model of the mosfet, circuit analysis is done for the implantation of drivers in BiCMOS process. The spice model extracted give good matching with the measurement data with the simulated data. A better model can be obtained with more well defined nmos and pmos structures.

3.4 Chapter Summary

In this chapter a detailed fabrication process steps for schottky diodes are presented. The electrical characterization is performed to derive the best schottky diodes applicable for high current and high breakdown voltage. It was derived that schottky diode with width W = 20 µm and L = 250 µm provided high current and higher breakdown. The n-well doping concentration formed with a dose of 6e12 was the optimized data in terms of both forward conduction and reverse breakdown voltage . The spice model parameters are extracted for schottky diodes, transistors and mos devices. The spice model extracted was simulated with the measurement data and it showed close matching with the measurement data.

Chapter 4

Integrated Rectifiers and Drivers on Rigid to Flex Substrate

In this chapter the electrical characterization of integrated rectifiers in BiCMOS7 process is presented. The rectifier circuit is simulated using LTspice with schottky diode spice diode model extracted in previous chapter. A basic linear driver and a buck driver circuit are analyzed with the NPN bipolar transistor and NMOS spice model derived in the previous chapter. Finally a design proposal for integration of rectifiers and drivers on flex to rigid substrate is presented.

4.1 Integrated rectifiers in BiCMOS7 process

In the previous chapter the fabrication of schottky diodes in DIMES BiCMOS7 process was presented. The schottky diodes in this thesis are the main component of the rectifier circuit for ac to dc conversion. A spice level 3 model was obtained in the previous chapter. This model is used for electric circuit analysis to simulate the behavior of the rectifier built using the schottky diodes. In this section, the circuit analysis is done using LT Spice and the electrical measurement results of the integrated bridge rectifier in BiCMOS7 process are discussed.

4.1.1 Simulation of Rectifiers using DIMES BiCMOS7 schottky diode model

The rectifier configuration used in the conversion of AC to DC is a bridge rectifier circuit. The bridge rectifier consists of four schottky diodes connected as shown in Figure 4.1.The diodes are connected in such a way that during the positive half cycle of the ac input signal diodes D1 and D2 are in forward bias and conduct. During the negative half cycle, the diodes D3 and D4 will be conducting and D1 and D2 are reverse biased. In both the cases the

current flowing through the storage capacitor C and load is in the same direction. The output DC voltage obtained will be equal to the peak AC input minus the twice the forward voltage drop across the schottky diode. The input AC voltage is 12V with frequency 50 Hz. The output DC voltage is in the range of 11V with the voltage drop across the schottky diodes are around 0.4V.

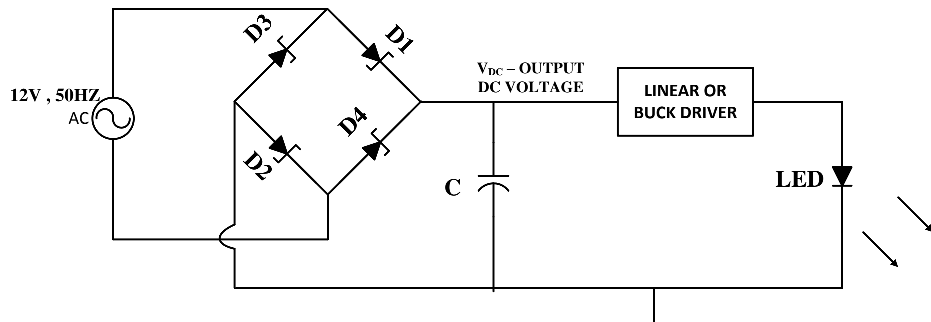

Figure 4.1 Schematic of Rectifier circuit with schottky diodes

A schematic of full wave bridge rectifier in LTspice considering a small load of 100 Ω is shown in Figure 4.2 . The circuit is simulated for AC input voltage of 12V, 50Hz. The spice models used are the schottky diode models derived from the previous chapter. The Output voltage waveforms obtained are shown in Figure 4.3 to Figure 4.5

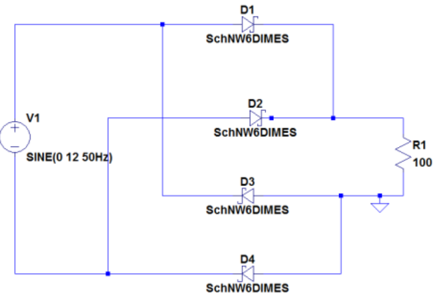

Figure 4.2 Schematic of Rectifier circuit with schottky diodes

Figure 4.3 Output voltage at diode D1

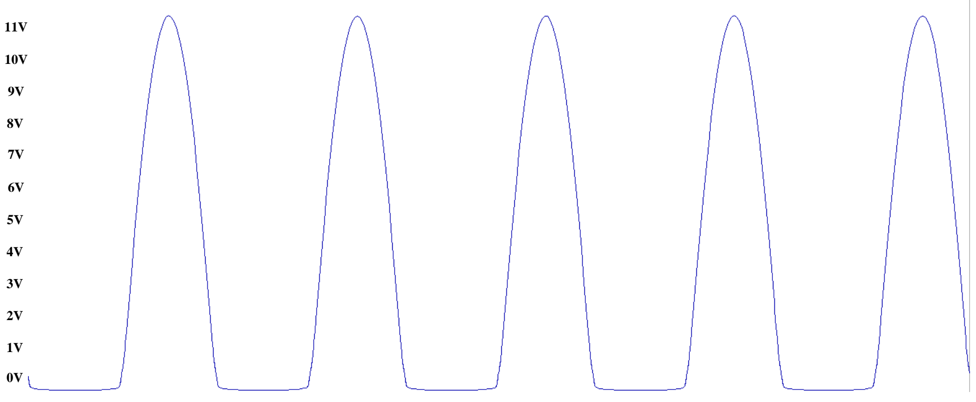

Figure 4.4 Output voltage at diode D4

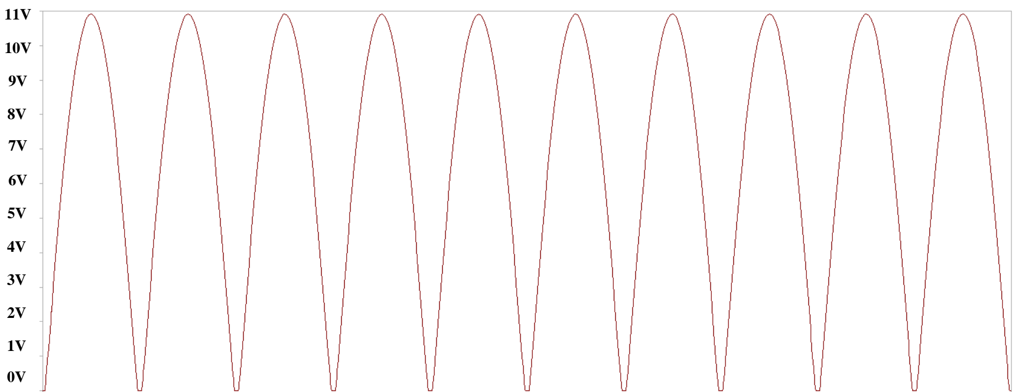

Figure 4.5 Output voltage at resistor

From the above simulations, it can be seen that the output voltage at the individual diode terminals is about 11.4 to 11.5V. This means the forward voltage drop across the schottky diode is about 0.5-0.6V. The output voltage from Figure 4.5 is about 11V. The output ripple is due to the absence of storage elements in the schematic. To minimize the ripple, a storage capacitor is used to filter the output voltage and provide a constant dc voltage. The storage capacitor C charges during the positive cycle of the output DC voltage. As the diode voltage drop goes low due to the AC input signal, the capacitor discharges slowly across the resistor, thus providing a lesser ripple than a circuit without capacitor. The capacitor charges again during the next positive cycle of the output DC voltage thus trying to maintain a constant output DC voltage across the load. The discharge time of the capacitor is dependent the RC time constant of the filter circuit. A schematic of LTSpice simulation with storage capacitor and LED as load is shown in Figure 4.6and the output voltage and current obtained in the circuit is shown in Figure 4.7 to Figure 4.8.

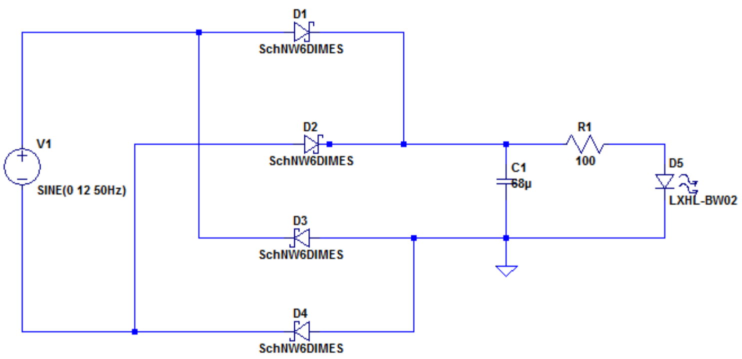

Figure 4.6 LTspice schematic of Rectifier circuit with resistor as linear driver

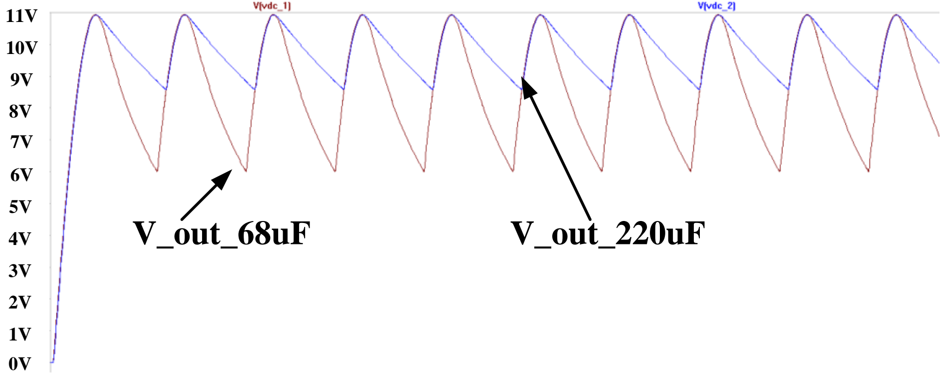

Figure 4.7 Output voltage simulation of the integrated rectifier circuit with schottky diodes fabricated in DIMES BiCMOS7 process

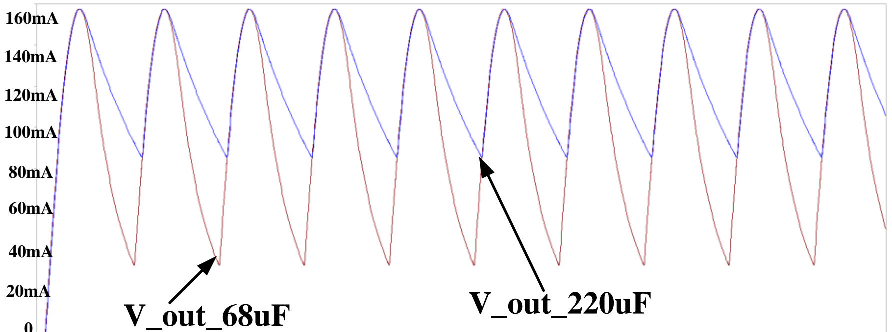

Figure 4.8 Output current simulation of the integrated rectifier circuit with schottky diodes fabricated in DIMES BiCMOS7 process

The output current ripple is about 35% for capacitor with 220µF with maximum current at 160mA and it is about 70% for capacitor with 68µF. Hence a resistor based LED driver is highly inefficient as a constant current driver. In the next section, the characterization of the fabricated integrated rectifier chip is discussed.

4.1.2 Characterization of Rectifiers fabricated in DIMES BiCMOS7 process

A characterization setup for testing the rectifier as shown in Figure 4.9 is used. The terminals of the rectifier chip are probed using the cascade probe station. The terminals of the cascade station are then connected to an oscilloscope and a function generator to study the electrical characteristics of the rectifier chip.

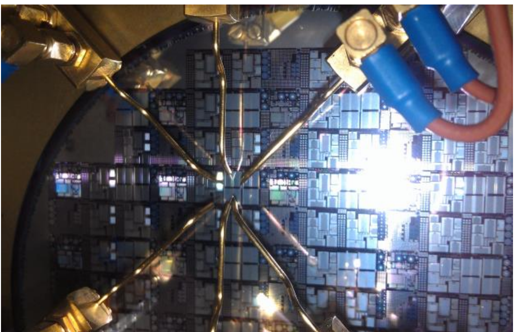

Figure 4.9 On wafer testing of the rectifiers using cascade probe station

Similar measurements are made as the simulation of the rectifier in LTspice. The input voltage was set at 11V due to the limitation of the frequency generator. The frequency is set as 50Hz. The output at the diode D1 in the rectifier circuit in Figure 4.10 obtained is shown below,

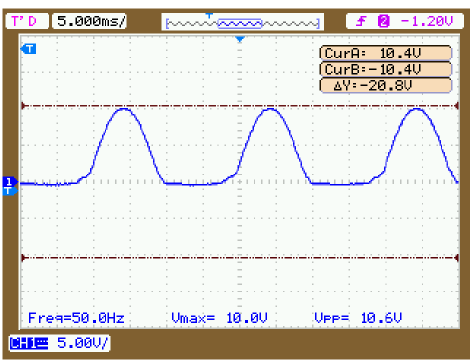

Figure 4.10 Output voltage at diode D1 of the integrated rectifier

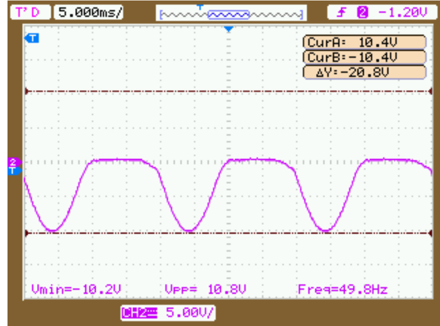

Figure 4.11 Output voltage at diode D4 of the integrated rectifier

The diode D1 conducts only in the positive half of the cycle whereas the diode D4 conducts only during the negative half of the cycle. The maximum DC voltage obtained for an input of 11V is 10.4V. The drop across the schottky diode and the probe connector resistor is about 0.6V. The output at the load of the bridge rectifier is shown in Figure 4.12. The output across the load resistor is about 9.8V. There is a drop of 1.2V across the rectifiers and the probes.

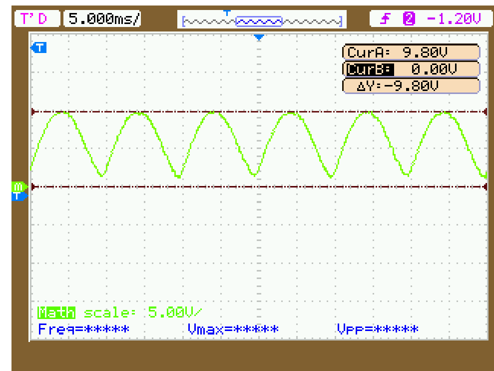

Figure 4.12 Output voltage at the load of the integrated rectifier

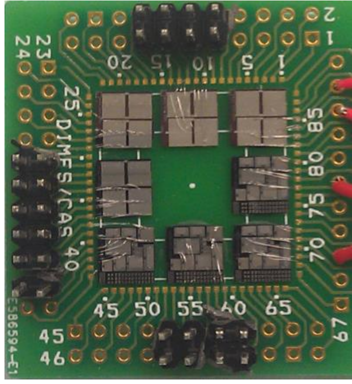

Figure 4.13 Integrated rectifier wirebonded to PCB

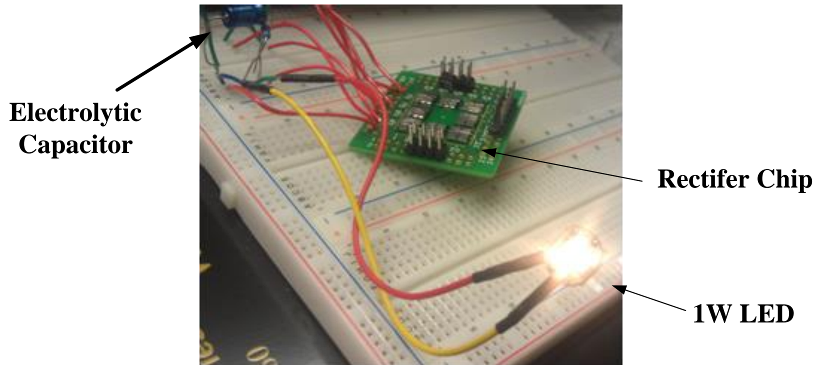

Figure 4.14 Integrated rectifiers and linear driver for the G4 LED

Next a circuit was built up for rectifier chip with a filter capacitor of 220 μF. The capacitor along with a load resistor of 100 Ω forms the circuit of a linear driver for powering the LED. The setup is shown in Figure 4.14. The storage capacitor provides a constant dc voltage and the resistor limits the current to 100mA in the LED.

A fully integrated rectifiers using schottky diode in BiCMOS7 process was modeled and experimentally verified. The measured output closely matches with the simulated output in LTspice. In the next section, a basic linear driver and buck driver with integrated rectifiers is analyzed.

4.2 Integrated drivers in BiCMOS7 process

In the previous chapter the spice model was extracted for the NPN BJT and NMOS devices in DIMES BiCMOS7 process. Using this spice model, analysis of two configurations of linear driver is done. The circuit in Figure 4.15 shows a linear driver based on mosfets and NPN bipolar transistor. In this circuit, the current in the LED is determined by the resistor R2. The base emitter voltage is kept below 0.7V. For a resistor value of 4 ohms, the current across the two LED is obtained as 174mA. The circuit can be optimized for the desired value of current across the LED. The NMOS is turned on when the voltage at the gate of the mosfets is greater than the threshold voltage of the mosfets. The transistor Q2 turns on with Vbe of the transistor set by voltage drop across R2 that should be less than 700mV. The MOSFET is operating at the linear region when the transistor turns on and it pulls down the voltage the gate of the mosfets and maintains a constant current across the LEDs [4, 34].

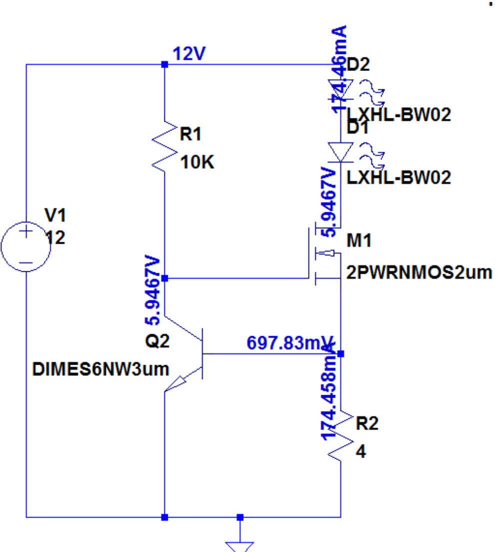

Figure 4.15 Linear driver circuit example

The next circuit that is analyzed is linear driver based on current mirror. The current mirror is based on two NMOS devices. The circuit is shown in Figure 4.16.

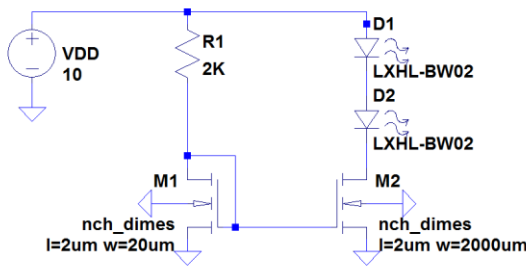

Figure 4.16 Current Mirror driver circuit example

In the current mirror the drain current across the transistor M1 is mirrored to the drain of M2. The current across the M2 is set by the width ratio of M1 and M2. In this example the current across R1 is 2mA. The ratio of widths of M2 and M1 is 200. The current is multiplied by this factor and the current across the LED is about 200mA. The circuit simulation of this current mirror is shown in Figure 4.17. The current is about 170mA.

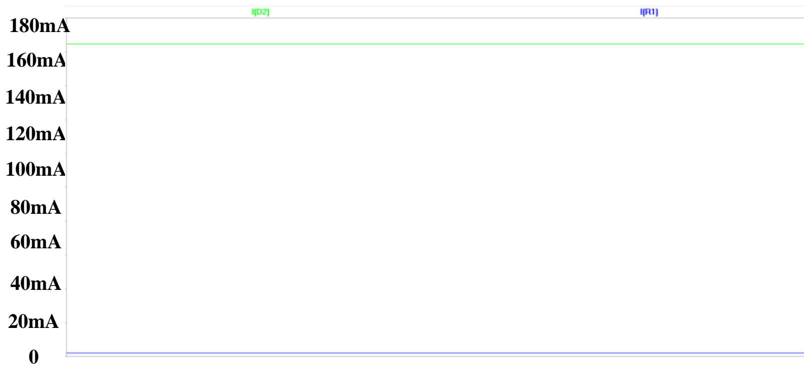

Figure 4.17 Current mirror output

This current mirror driver is integrated with the rectifier circuit as shown in Figure 4.18

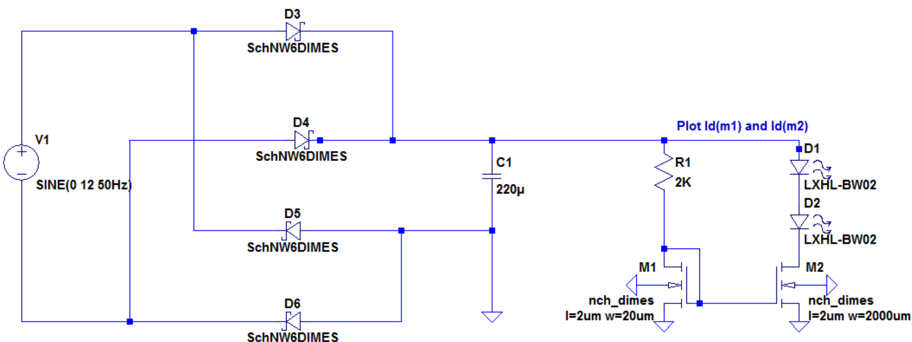

Figure 4.18 Current mirror with rectifiers using schottky diodes

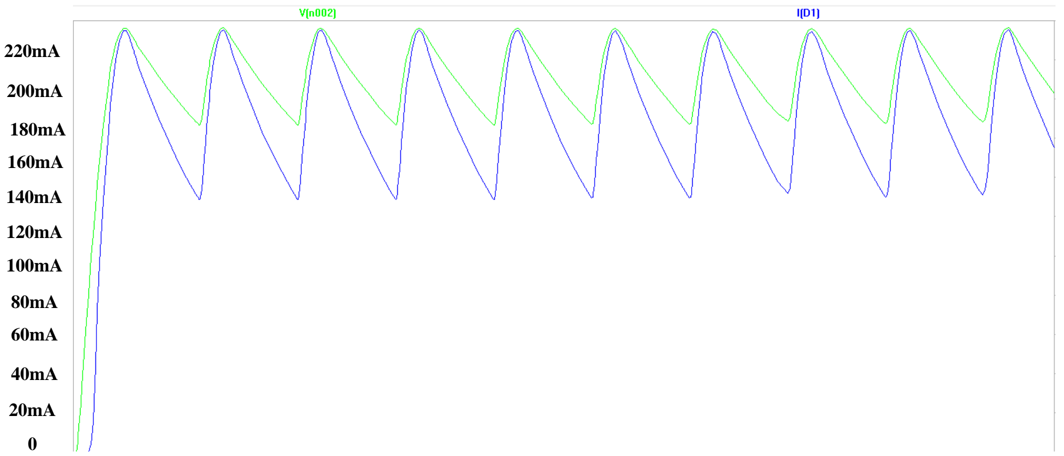

Figure 4.19 Output of Current mirror with rectifier

The output current is about 200mA. The circuit provided uses all the components that can be fabricated in BiCMOS process to achieve a fully integrated rectifier and driver.

The disadvantage of linear driver is that they are inefficient and consume more power and dissipate a lot of heat. The switch mode driver can achieve higher efficiency when compared to linear driver. A buck driver is a step down DC converter. This driver configuration is used if the output load voltage is less than the input voltage. The buck driver requires inductor and capacitor components for energy storage. A simple buck driver using ring oscillator for switching the mosfets is shown in Figure 4.20. The ring oscillator is designed using NMOS and PMOS devices. The output of the ring oscillator has a buffer so that it can drive the power MOSFET. The switching frequency of the ring oscillator is about 200 kHz. When the MOSFET is turned on the inductor stores energy. This energy is then used to provide current in the LED when the MOSFET is turned off. A schottky diode provides a return path for the current during the MOSFET off time across the LED and inductor circuit.

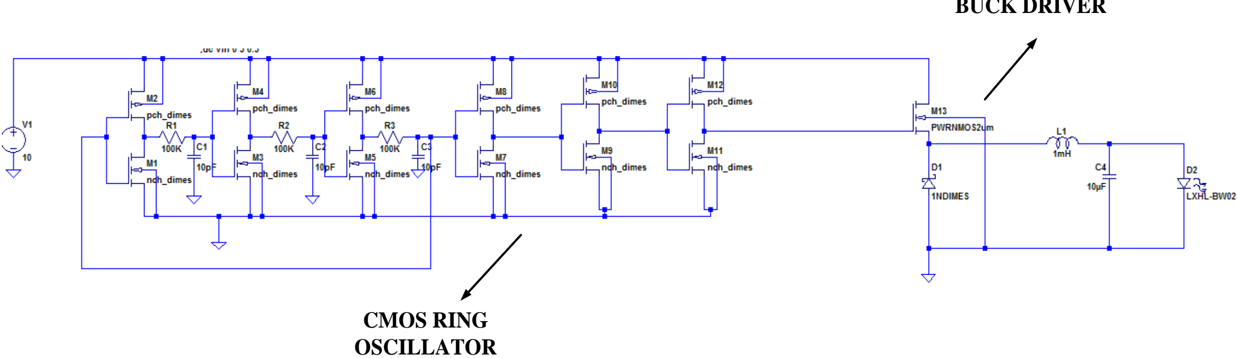

Figure 4.20 Buck driver with ring oscillator used for switching the mosfet

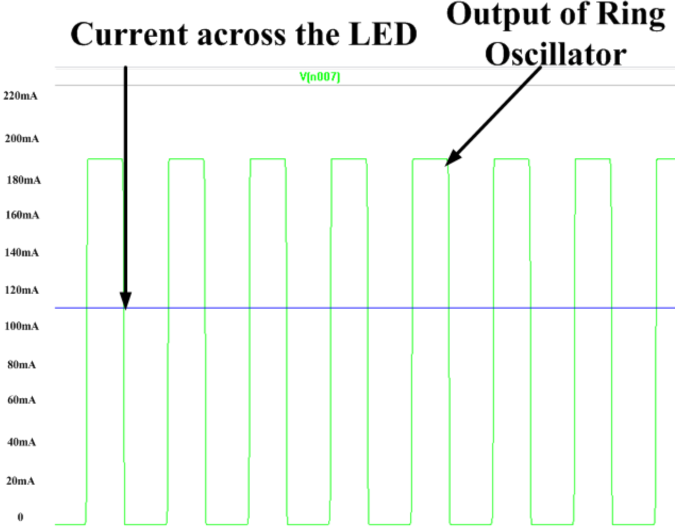

Figure 4.21 Output of Buck driver with ring oscillator

The output waveforms obtained is shown in Figure 4.21. The output current is constant current of 110mA. The ring oscillator has a switching frequency of 220 KHz.

In this section a circuit analysis of the npn transistor and nmos devices fabricated in BiCMOS process for linear and buck driver applications was studied. It can be seen that the BiCMOS technology offers a great potential for on chip integrated driver solutions. In combination with integrated rectifiers a complete ac dc conversion and constant current driver can be integrated on a single substrate in a planar process technology.

4.3 Design of Integrated rectifiers and drivers on Rigid to flex substrate

Wafer level packaging offers the advantage of reduction in the total cost of the LED system. By incorporating flexible interconnects a 3D form factor of the SSL module can be achieved. The flexible interconnects consists of aluminum encapsulated in polyimide. The proposed integrated and rectifier a flex to rigid substrate is shown in Figure 4.22. In the integration with flex to rigid substrate, the BiCMOS7 fabrication process step as discussed in previous chapter is done to integrate the rectifiers and drive using schottky diodes , npn transistors and mos devices. The process steps for Rigid to flex substrate are shown in Figure 4.23[10].

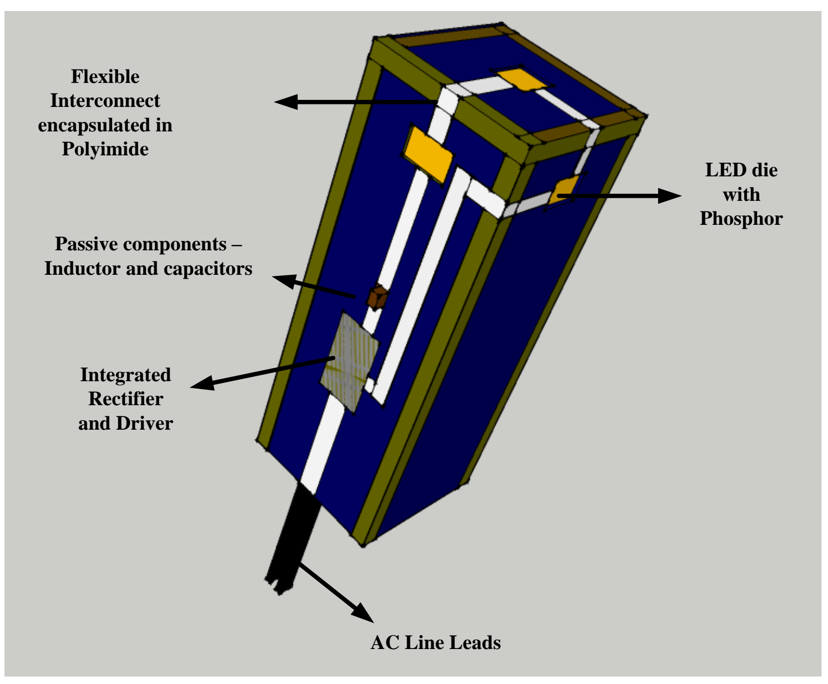

Figure 4.22 3D illustrationsof proposed integrated rectifier and driver in a Rigid to Flex substrate

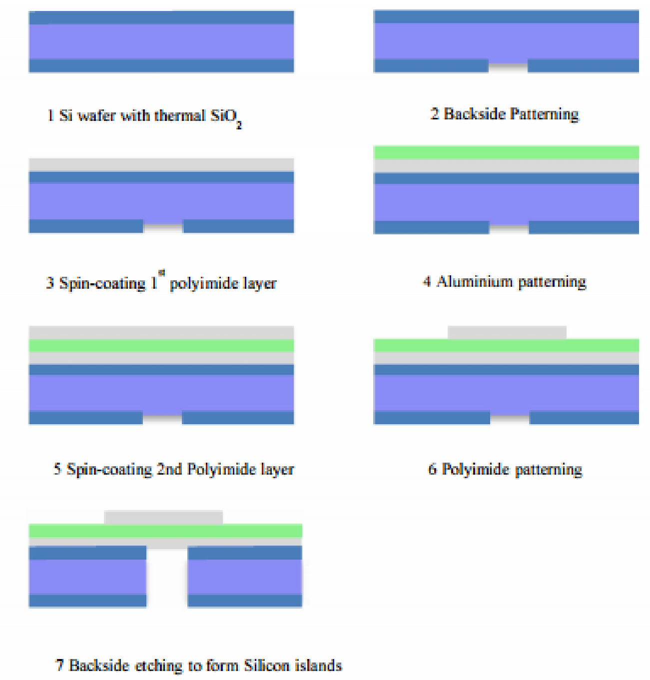

Figure 4.23 Process step of Rigid to flex substrate

The proposed process steps for the integrated rectifiers and drivers on silicon is stated below,

1. The schottky diodes, rectifiers, NPN, MOS devices and driver circuit can be first processed in the BICMOS7 process up to the metal 2 - M2 layer. This layer of aluminum can be combined with the aluminum layer of the flexible interconnect.
2. The thermal oxide is grown on the processed wafer. First the backside patterning of the oxide is done at the regions required for bending of interconnect.
3. Next the first polyimide is spin coated. This is cured. Aluminum is then sputtered and patterned
4. The second layer of polyimide is spin coated on top of the aluminum.
5. The polyimide is patterned and a back etch of the silicon is done to release the polyimide hinges.

An example mask design file for integration of rectifiers and driver in the G4 module on Rigid to Flexible substrate is shown in Figure 4.24.The design is done to drive two LED modules. The driver consists of either linear driver or simple buck driver as discussed earlier in this chapter.

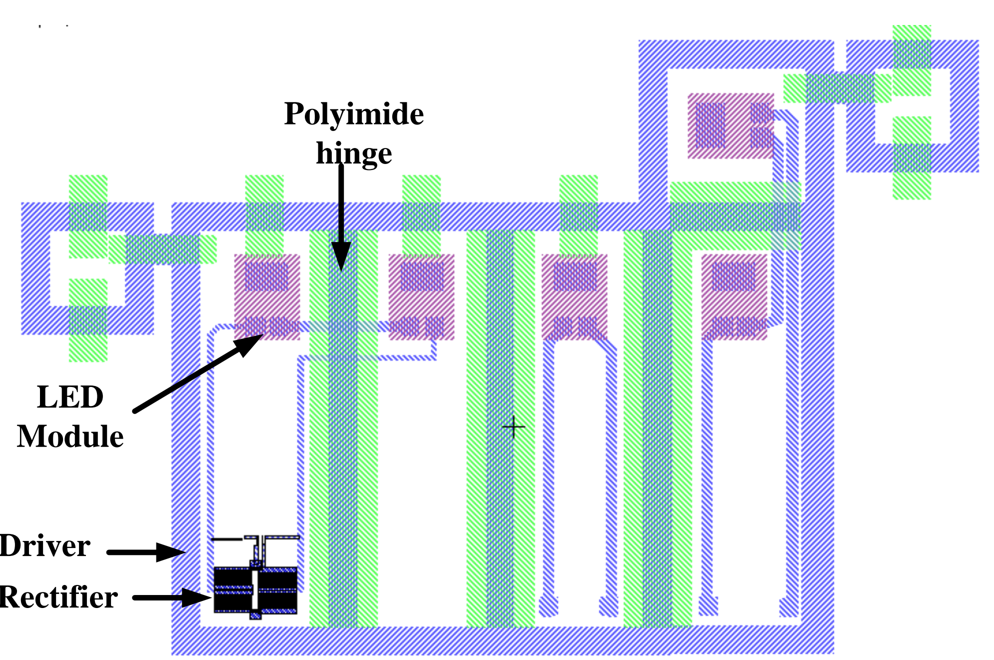

Figure 4.24 Proposed Mask design for integrated rectifier and driver usin Rigid to Flex substrate

A detailed analysis and fabrication process is not included in this thesis. Only a design proposal is made. It is intended for future processing. Using flexible interconnect gives the advantage of integrating more LED dies on a single package.

4.4 Chapter Summary

In this chapter the electrical characterization of the integrated rectifiers in standard BiCMOS process is presented. A circuit driving a 1W LED was built and tested. A simple linear driver and a buck driver are analyzed with the devices models fabricated in the BiCMOS process. A basic fabrication steps for integrating the rectifiers and drivers on rigid to flex substrate is proposed.

Chapter 5

Conclusion and Future Recommendations

In this chapter a complete summary of the work done as part of this thesis is presented. With the detailed design and development of schottky diodes in DIMES BiCMOS7 process, future recommendations are presented.

5.1 Conclusions

The main goal of this thesis is to design and fabricate schottky diodes for rectifier application in standard DIMES BiCMOS7 process that can be integrated with foldable wafer level LED package developed in DIMES. The steps followed in the thesis to achieve this goal is discussed below,

1. The design specification of the schottky diode needed for rectifier applications was first derived. It was seen that silicon as a substrate is suitable for low power conversion application.
2. The next task was to study the fabrication process of conventional silicon power schottky diode and it was deduced that the conventional power schottky diode is not suitable for integrating in a planar fabrication process due to it vertical structure.
3. A detailed analytical calculation was done to study the factors affecting the forward characteristics and the breakdown voltage of the schottky diodes in BiCMOS process. The analytical analysis was verified with process and device simulation tools like TSUPREM4, MEDICI and COMSOL In this analysis it was found that forward and reverse characteristics had a great dependency on the doping concentration of the n-well, the layout of the schottky contact and ohmic contact and resistance of the n-well region. It was found that for high current conduction a higher doping and closer structures is

required and for high breakdown lower doping and schottky contacts with p+ guard ring is required. The process and layout design parameters were optimized to achieve high current and high breakdown.

4. The devices are fabricated in DIMES BiCMOS7 process. The forward and reverse measurement was done to study the behavior of the different structures of the schottky diodes. The optimized structure obtained for high current and high breakdown was with schottky contact width of W = 20 µm and D = 5 µm. The optimized doping for high breakdown was found to be the n-well layer with nwell dose of 6e12. Schottky diodes with a breakdown of 27V and a forward current of 1A at forward voltage V_F = 0.68V was achieved in this process.
5. Integrated rectifier with the above schottky diode structure was fabricated in the BICMOS7 process
6. A complete characterization of the schottky diodes, NPN transistor and NMOS devices were done to extract the spice model data for circuit analysis.
7. Using the spice model, the rectifiers, linear and a simple buck driver was analyzed.
8. The monolithically integrated rectifier circuit was successfully tested and show good results for low voltage power conversion application.
9. From this result, a design proposal and the process for integrating both rectifiers and drivers on a rigid to flex substrate is presented.

A novel schottky structure for high current conduction and high breakdown was designed, fabricated and characterized in this thesis. The schottky diodes forms the core component of the rectifier.

A novel schottky diode structure in BiCMOS process for providing high current and high breakdown at the desired BiCMOS doping concentration of n-well was designed fabricated and characterized.

Silicon wafer level packaging for LED offers great advantages for integrating both optical function and electrical function on the same substrate. This offers space and cost reduction. By monolithically integrating rectifiers, drivers along with wafer level packaging of LED on silicon offers better reliability at reduced cost. In this thesis, low power rectifiers in DIMES BiCMOS7 process was successfully designed, fabricated and characterized. The large area schottky diodes fabricated in this process achieved an average breakdown of 26V with forward current conduction of 1A at a forward voltage drop of 0.65-0.7V. The schottky diodes, NPN transistor and MOS devices were successfully characterized and a robust spice model was extracted from the measurement data using ICCAP tool. DIMES BiCMOS7 process offers an exciting platform for integrating functionalities like drivers, sensors for SSL applications.

5.2 Future Recommendations

The following points would be interesting for future applications,

1. A more robust process and device models can be built for the DIMES BiCMOS7 process by using recent TCAD software packages like Silvaco. This gives a better understanding of the device and process behavior. This will help in optimizing the process and device parameters for many applications like sensor integration.
2. For low power applications, the schottky diode developed in this process using silicon substrate and planar process can be investigated.
3. A robust device characterization for the DIMES BiCMOS7 process can be made by using the standard set of mask layout structures defined by ICCAP manuals. The models extracted from this measurement data can be very helpful for circuit analysis.
4. More complex driver circuits with integrated opamp and pwm controller can be investigated for monolithically integrated driver solutions using DIMES BiCMOS7 process.

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List of Publications

M. R. Venkatesh, P. Liu, H. W. van Zeijl, and G. Q. Zhang, "Modeling and simulation of monolithic integration of rectifiers for solid state lighting applications," in *Thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems (eurosime), 2014 15th international conference on*, 2014, pp. 1-6.

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