

# **Characterization of pure boron depositions integrated in silicon diodes for nanometer-deep junction applications**

Francesco Sarubbi



**Characterization of pure boron depositions  
integrated in silicon diodes  
for nanometer-deep junction applications**

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# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Boron doping by chemical vapor deposition . . . . .	2
1.2	Innovative nanometer-deep <i>pn</i> -junction applications . . . . .	4
1.2.1	Silicon-on-glass varactors for RF applications . . . . .	6
1.2.2	Photodiodes for detection of ultraviolet (UV) radiation . . . . .	8
1.3	Outline of the thesis . . . . .	11
<b>2</b>	<b>Chemical vapor deposition of boron layers</b>	<b>13</b>
2.1	Processing conditions . . . . .	13
2.2	Transmission electron microscopy analysis . . . . .	14
2.2.1	B-layer morphology and growth rate . . . . .	14
2.2.2	Topography dependence: selectivity, uniformity, and isotropy .	15
2.2.3	Low-temperature deposition . . . . .	16
2.3	Secondary ion mass spectrometry analysis . . . . .	18
2.3.1	Boron content in as-deposited layers . . . . .	18
2.3.2	B-layer removal . . . . .	19
2.3.3	Boron diffusion during the deposition . . . . .	20
2.4	Electrical characterization of surface boron doping . . . . .	23
2.4.1	Sheet-resistance measurements . . . . .	23
2.4.2	Depletion-type MOS-capacitors . . . . .	24
2.4.3	Capacitance-voltage profiling . . . . .	27
2.5	Conclusions . . . . .	30
<b>3</b>	<b>B-layers studied in <i>p</i><sup>+</sup><i>n</i> diode configurations</b>	<b>31</b>
3.1	Device fabrication . . . . .	31
3.2	Ohmic contacts . . . . .	32
3.3	<i>p</i> <sup>+</sup> <i>n</i> junction diodes . . . . .	34
3.3.1	Exposure time dependence . . . . .	34
3.3.2	Temperature dependence . . . . .	36
3.3.3	Flow rate and pressure dependence . . . . .	37
3.3.4	Masking . . . . .	39
3.3.5	Non-planar Si surfaces . . . . .	40
3.3.6	Pure aluminum metallization . . . . .	40

3.3.7	Comparison of B-deposition and B-doped Si epitaxy . . . . .	42
3.4	Emitters in <i>pnp</i> bipolar transistors . . . . .	42
3.5	Conclusions . . . . .	45
<b>4</b>	<b>B-layers as source for dopant diffusion</b>	<b>47</b>
4.1	Thermal annealing . . . . .	47
4.1.1	Thermal annealing of $\leq 1$ ML boron coverage . . . . .	48
4.1.2	Thermal annealing of B-layers . . . . .	49
4.2	Thermally annealed B-layers in <i>pnp</i> transistors . . . . .	53
4.3	Conclusions . . . . .	56
<b>5</b>	<b>B-layers applied to silicon-on-glass varactor technology</b>	<b>57</b>
5.1	Reverse I-V characteristics of as-deposited B-diodes . . . . .	57
5.2	Strategies for improving reverse I-V characteristics . . . . .	60
5.3	Silicon-on-glass varactor technology . . . . .	62
5.3.1	Device fabrication . . . . .	64
5.3.2	Electrical characterization . . . . .	65
5.4	Conclusions . . . . .	68
<b>6</b>	<b>Deep-/extreme-ultraviolet radiation photodiodes</b>	<b>69</b>
6.1	Formation of photodiode $p^+$ front-area . . . . .	69
6.1.1	B-deposition . . . . .	70
6.1.2	<i>In-situ</i> thermal annealing . . . . .	70
6.1.3	Selective B-doped silicon epitaxial growth . . . . .	72
6.2	Device fabrication . . . . .	73
6.3	Electrical characterization . . . . .	74
6.3.1	Dark current . . . . .	74
6.3.2	Series resistance and response time . . . . .	75
6.4	Optical characterization . . . . .	77
6.4.1	Responsivity in DUV spectral range . . . . .	77
6.4.2	Responsivity in EUV spectral range . . . . .	78
6.5	Performance stability . . . . .	80
6.5.1	Dark current degradation . . . . .	80
6.5.2	Responsivity degradation . . . . .	82
6.6	Conclusions . . . . .	82
<b>7</b>	<b>Conclusions and recommendations</b>	<b>85</b>
7.1	Conclusions . . . . .	85
7.2	Recommendations . . . . .	86
<b>Bibliography</b>		<b>89</b>
<b>List of symbols and abbreviations</b>		<b>95</b>
<b>Summary</b>		<b>99</b>

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<b>Samenvatting</b>	<b>103</b>
<b>List of publications</b>	<b>107</b>
<b>Acknowledgments</b>	<b>111</b>
<b>About the author</b>	<b>113</b>



# Chapter 1

## Introduction

This thesis presents the formation of nanometer-thick boron (B) layers on (100)-oriented Si surfaces during exposure to diborane ( $B_2H_6$ ) in a chemical vapor deposition (CVD) system either at atmospheric or reduced pressures. At the applied temperatures from 500 °C to 700 °C, the deposition forms a layer stack of amorphous boron ( $\alpha$ -B) and boron-silicon compound ( $B_xSi_y$ ) from which the crystalline Si substrate (c-Si) is *p*-doped to depths below 10 nm up to the solid solubility by thermal diffusion. This process exhibits high selectivity to Si, isotropy, spatial homogeneity, and compatibility with standard semiconductor device fabrication. The dependence of the growth mechanism and boron doping on processing parameters is investigated by analytical techniques in conjunction with an extensive electrical characterization. The B-layer is also demonstrated to be a stable and controllable supply of B for the formation of deep  $p^+$ -regions by using thermal drive-in.

The pure B CVD process is applied to fabricate high-quality, extremely ultra-shallow  $p^+n$ -junction diodes, where the saturation current can be tuned from high Schottky-like values to low deep-*pn*-junction-like values by increasing the deposited B-layer thickness. In particular, the study of *pnp* structures with  $p^+$  B-deposited emitters shows that the presence of an  $\alpha$ -B layer significantly increases the effective Gummel number of the as-diffused emitter. Such unique properties are exploited with great advantages in  $p^+n$  diodes fabricated at 700 °C for the integration of two distinct device technologies: varactor diodes for adaptive functions in radio frequency (RF) applications and photodiodes for detection of ultraviolet (UV) radiation.

In the former case, B-deposition offers a low-temperature process module within the silicon-on-glass (SOG) substrate-transfer technology to secure hyper-abrupt arsenic (As) profiles needed for highly-linear tunable varactors. Similarly, outstanding electrical and optical performance is achieved for  $p^+n$  photodiodes implemented by forming the radiation-exposed  $p^+$  area with B-layers. In particular, this technology enables the maximum silicon spectral responsivity over the complete UV photon spectral range.

The following two sections of this introductory chapter illustrate the motivation of the research activity, which was focused on two areas: process/characterization of

a new material and integration in Si-based devices. First, on the materials level, the B-deposition is set within the general context of novel CVD doping technologies proposed to face the difficult challenges in the front-end processing that have emerged due to the aggressive downscaling of vertical dimensions for future semiconductor devices. However, the process substantially differs from other techniques that use  $\text{B}_2\text{H}_6$  exposure for surface doping, both with respect reaction kinetics and the low temperatures used. The latter is generally very attractive for versatile use of a doping technology. Thus, the deposition of a B-layer on Si is demonstrated to offer unprecedented advantages that have not been explored so far for formation of ultrashallow and more efficient *pn*-junctions in the nanometer-regime. On the device level, the integration of B-layers mainly aims to boost the performance of dedicated device technologies that are developed at DIMES of the Delft University of Technology.

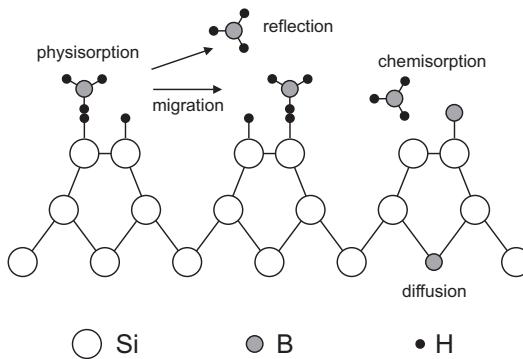
## 1.1 Boron doping by chemical vapor deposition

Low-energy  $\text{B}^+$  and  $\text{BF}_2^+$  ion implantations conventionally combined with high-temperature, very short-time thermal anneals are the main techniques used by the semiconductor device industry to form  $p^+$  ultrashallow contacts and junctions. However, a drawback of this method is the undesirable broadening of the associated doping profiles due to implantation damage induced transient-enhanced diffusion (TED) effects that are particularly severe for B dopants. In addition, the presence of any lattice damage can be detrimental when the doping profiles in the vicinity of the junction are decisive for the device operation.

As an alternative to implantations, *in-situ* doping during Si or SiGe chemical vapor deposition (CVD) has been increasingly used, for instance in raised or re-filled source/drain CMOS regions or intrinsic bases of HBT devices. TED effects are effectively avoided since no lattice defects are created during the process. The advantages of CVD methods for device manufacturing reside also in low cost, high throughput, compatibility with standard semiconductor processing, and capability of well-controlled epitaxial growth even at low temperatures. In particular, diborane ( $\text{B}_2\text{H}_6$ ) gas is widely used as *p*-type dopant gas, while arsine ( $\text{AsH}_3$ ) and phosphine ( $\text{PH}_3$ ) are added for *n*-type doping.

However, a few studies have demonstrated *p*-like doping behavior of *n*-type (100) Si surfaces after exposure solely to  $\text{B}_2\text{H}_6$  in an oxygen-free atmosphere without any extra addition of silane-based sources, either using ultrahigh vacuum and low-pressure apparatus [1–5] or CVD systems operating at atmospheric pressure [6, 7]. This technique differs from other conventionally used *p*-type doping methods based on dopant diffusion from a gas source, where B drive-in is implemented in an oxidizing ambient. Moreover, in the latter case the doping efficiency, i.e. the maximum doping concentration, is governed by the solid solubility at the processing temperature. On the other hand, pure  $\text{B}_2\text{H}_6$  gas injection in the reactor chamber can lead the boron density at the Si surface to significantly increase beyond the solid solubility by appropriately varying the source gas parameters and the exposure time.

A model of the surface reaction doping for boron atoms on silicon during exposure



**Figure 1.1:** Doping reaction model for Si surface exposure to  $\text{B}_2\text{H}_6$  dopant gas (after [8]).

to diborane in a CVD reactor was proposed by [8], as schematically shown in Fig. 1.1. Assuming that  $\text{BH}_3$  is the dopant species generated by thermal dissociation of  $\text{B}_2\text{H}_6$  gas,  $\text{Si}-\text{H}$  are silicon atoms at the surface whose dangling bonds are terminated by hydrogen, and  $\text{Si}^\circ$  are silicon atoms with dangling bonds, the sequence of the mechanisms is:

1. Physisorption:  $\text{Si}-\text{H} + \text{BH}_3 \rightarrow \text{Si}-\text{HBH}_3$
2. Reflection:  $\text{Si}-\text{HBH}_3 \rightarrow \text{Si}-\text{H} + \text{BH}_3$
3. Migration:  $\text{Si}-\text{HBH}_3 + \text{Si}-\text{H} \rightarrow \text{Si}-\text{H} + \text{Si}-\text{HBH}_3$
4. Recombination:  $\text{Si}-\text{HBH}_3 + \text{Si}-\text{HBH}_3 \rightarrow 2\text{Si}-\text{H} + \text{B}_2\text{H}_6$
5. Chemisorption:  $\text{Si}^\circ + \text{BH}_3 \rightarrow \text{SiB} + 3\text{H}$
6. Diffusion:  $\text{SiB} \rightarrow \text{Si}^\circ + \text{B}(\text{diffused})$

Therefore, the  $\text{B}_2\text{H}_6$  surface reaction doping relies on the thermal decomposition of the source gas, so that the available boron atoms may stick to the surface, chemically react with silicon atoms, and diffuse into the substrate. However, the reactivity with the silicon surface is reduced by the presence of hydrogen-terminated silicon dangling bonds, since the physisorption and migration of  $\text{BH}_3$  precursor is enhanced. In fact, chemisorption and  $\text{Si}-\text{B}$  bonds formation, which is a prior step for the in-diffusion, can only occur when  $\text{Si}^\circ$  are available.

However, when all Si surface sites are occupied by B, the model should also take into account a chemisorption mechanism at B-occupied surface sites to describe the well-known non-self-limiting adsorption. Thus, the boron coverage can exceed one monolayer (1 ML), which is equivalent to the surface density of  $6.78 \times 10^{14} \text{ cm}^{-2}$  for (100)-oriented Si, and lead to the formation of a distinct boron layer [9, 10]. This behavior differentiates boron from other doping impurities, such as phosphorus and arsenic, [1, 4, 11, 12].

In this respect, the exposure conditions in terms of dopant gas flow rate and carrier gas play the most significant role. Indeed, termination of Si dangling bonds is maintained during dopant injection when hydrogen is used as carrier gas and the

diborane concentration is low ( $\leq 4$  ppm). This is valid even at high deposition temperatures, where hydrogen thermal desorption might be a dominant mechanism [11]. Thus boron segregation is suppressed, but actual doping of the substrate can be still achieved. On the other hand, either different inert ambient, such as in nitrogen gas, or high flow rate of diborane ( $\geq 6$  ppm) can significantly reduce the probability of hydrogen-terminated Si dangling bonds, and large amount of boron atoms can be deposited on the silicon surface proportionally to the exposure duration [8, 11]. At the same time, the growing B-layer will act as a source for boron diffusion into the silicon substrate during the CVD process itself [13].

While gas parameters can determine the transition from surface Si doping to B-deposition, the temperature mainly influences the actual boron doping of the silicon substrate and the final composition of the deposited film. In fact, high temperatures certainly increase boron diffusion at any gas flow conditions. On the other hand, boron-silicon compounds can be formed when B segregation occurs at high temperatures. In fact, as reported in [9, 10], boron silicide is the predominant phase in deposited film prepared at temperatures  $\geq 800$  °C. On the other hand, amorphous boron will be formed on the silicon surface if the deposition temperature is lower.

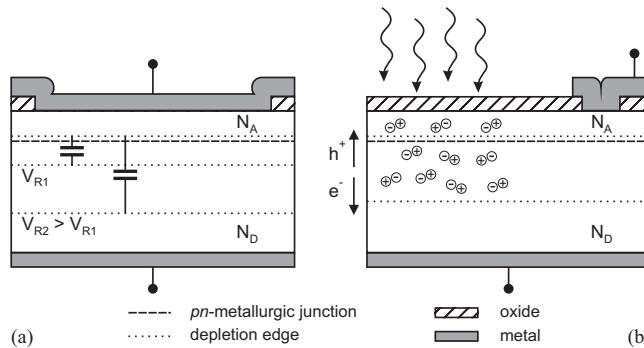
For device applications, the bulk of these earlier works focused on deposition temperatures around 800–900 °C, where substantial B-doping of the Si substrate is expected. Even though few experiments were performed at lower temperatures, such as 400–600 °C [5, 7], the exposure conditions were mainly chosen to prevent boron adsorption to less than a monolayer. In fact, either pure boron segregation or formation of boron-silicon compounds were often addressed as drawbacks of the  $\text{B}_2\text{H}_6$  reaction kinetics. In contrast to such propositions, in this work excessive B adsorption is intentionally promoted during  $\text{B}_2\text{H}_6$  exposure at temperatures down to 500 °C. The material and electrical properties of the deposited layer are studied as function of processing parameters and subsequently exploited in the formation of extremely ultrashallow junctions for silicon-based  $p^+n$  diodes.

## 1.2 Innovative nanometer-deep *pn*-junction applications

For several years now source/drain formation for CMOS devices has been the main driving force behind the development of novel doping technologies targeting nm-shallow, ultra-abrupt, and highly-doped junctions with damage-free properties. Likewise, for advancing the speed of SiGe heterojunction bipolar transistors (HBTs), downscaling and precise engineering of doping profiles has also become a crucial line of development.

There are also many other *pn*-junction-based devices beyond the Bipolar/CMOS scenario that also can profit from advances in doping technology. Here the focus has been on two Si devices that have become the first, very successful, applications of the B-deposition:

1. varactor diodes for tunable circuits in RF applications,



**Figure 1.2:** Schematic cross-section of: (a) a varactor diode and (b) a photodiode.

## 2. photodiodes for radiation detection in UV/soft X-ray spectral range.

Although both device concepts are well-known [14], their performance has been so far limited by manufacturability and design trade-offs. Schematic cross-sections of the devices are shown in Fig. 1.2 for a  $p^+n$  diode implementation, but similar conclusions can be drawn for  $n^+p$  structures. More details will be given in the following paragraphs, while here the general operating principles are briefly considered. This discussion, in fact, will essentially highlight the benefits on the device design and performance resulting from a doping technology that can provide ultrashallow junctions and high doping efficiency. The latter feature, rather than being associated with a low sheet-resistance of the doped region, is here mainly of importance due to the fact that an ‘effective’ one-sided abrupt junction can be formed ( $N_A \gg N_D$ ) in a manner that the diode current is only determined by the minority carrier injection into the substrate.

A varactor is a device whose reactance can be varied in a controlled manner with a bias voltage. In particular, the capacitance per unit area associated with the depletion region can be expressed as

$$C = \frac{\epsilon_0 \epsilon_{Si}}{W(N_D(x), V_R)} \quad (1.1)$$

where  $\epsilon_0$  is the permittivity in vacuum,  $\epsilon_{Si}$  the Si permittivity,  $W$  the depletion width,  $N_D(x)$  the n-type doping profile, and  $V_R$  the reverse bias voltage. Therefore, by properly varying the distribution of the bulk doping profile, many capacitance-voltage relationships can be achieved and thus different tunable capabilities. However, all the physics-based designs of  $N_D(x)$  are derived under the assumption of a one-sided abrupt junction, i.e. the depletion does not extend into the  $p^+$ -doped region due to the high dopant concentration and abruptness.

Photodiodes also count on the depletion region of a *pn*-junction and on the resulting electric field in order to separate electron-hole pairs generated by the incident radiation and to collect holes and electrons at the anode and cathode, respectively.

Nevertheless, photogenerated carriers are also formed in the quasi-neutral top diffused junction. In fact, the intensity of the radiation and thus the carrier generation rate inside the device decreases exponentially from the surface with a characteristic length, i.e. the penetration depth, defined as the reciprocal of the absorption coefficient at the incident radiation wavelength. Therefore, an extremely ultrashallow junction will be instrumental for minimizing the carrier loss in the quasi-neutral region, since electron-hole pairs can recombine before being collected at the electrodes, while most of the photogeneration could occur in the space-charge-region.

Based on these considerations, a Schottky diode would appear the most efficient solution for both devices, since it gives an ideal abrupt junction and the depletion starts already from the surface. On the other hand, since such devices generally operate in reverse bias conditions, *pn*-junction configurations are preferred to Schottky contacts because the I-V characteristics of the former have lower current levels. Therefore, the choice of a *pn*-based device structure will translate for the varactors into a more ideal capacitive behavior, since the equivalent parallel resistance would be higher. On the other hand, photodiodes with low ‘dark’ current, i.e. the current without irradiation, can have a greater signal-to-noise ratio and be more sensitive to weak radiation intensities. The influence on optical performance will be discussed below.

Although ultrashallow and abrupt  $p^+$  doping profiles became available, the reduction of the junction depth should be also supplemented with higher doping efficiency, otherwise the I-V characteristics would be influenced in a less favorable way. In fact, the resulting junction will not suppress the injection of minority carriers from the substrate, and the diode current will be high. Doping techniques, such as implantation or CVD epitaxial growth, are not suitable. In the former case, in fact, beside the unavoidably broadening of either the  $p^+$  profile or the background *n*-type doping distribution, the depletion region might be affected by reduced carrier lifetime due to lattice damage. This will generally increase the generation-recombination leakage current and, in particular, the loss of photogenerated carriers in devices for radiation detection. CVD depositions can provide nm-thick Si layers with abrupt doping transitions, but low-temperature processing, which are required for instance in varactor implementations, cannot provide high efficiency for boron doping due to limited solid solubility.

In this thesis, the boron CVD deposition is demonstrated to be a reliable solution for the formation of the  $p^+$ -junction needed in these devices. Outstanding performance has been achieved and the fabricated devices represent to our knowledge the state-of-the-art among academic and industrial communities both for varactor-based and UV detector technologies.

### 1.2.1 Silicon-on-glass varactors for RF applications

Future wireless systems increasingly demand circuit techniques that facilitate RF adaptivity. Some examples of adaptive circuits include tunable filters, tunable matching networks for low-noise and power amplifiers, and multiband voltage controlled oscillators. However, these applications rely on a tunable capacitive element that

should particularly ensure high linearity, wide tuning range, extremely low loss, i.e. high quality-factor (Q), and ruggedness to high voltage and high current.

Such requirements have generally disqualified the use of varactor diodes for RF tuning techniques due to the inherently non-linear behavior at the microwave frequency of interest for use with modern communication standards. In addition, conventional bulk-silicon device implementations suffered from high losses in terms of parasitic resistive and capacitive components, which strongly inhibit high frequency performance, due to the need for buried layers or finger structures for contacting the device regions.

Nevertheless, in the last years a number of record-breaking circuits with excellent linearity and high Q-factors were fabricated with varactor-based circuit topologies in the DIMES silicon-on-glass (SOG) substrate-transfer technology [15–19]. This excellent performance has been possible as a result of two design/process strategies:

- a) *Tuning range and linearity constraints are concomitantly fulfilled by proper choice of the varactor doping profile and circuit topology.*

Assuming that the *pn*-junction is one-sided and the doping distribution  $N_D$  of the substrate is  $N_D = Kx^m$ , the C-V relationship of Eq. 1.1 can be expressed as  $\propto (V_R + V_{bi})^{-s}$ , where  $V_{bi}$  is the built-in potential of the *pn*-junction and  $s = \frac{1}{m+2}$  is the varactor sensitivity, which thus strictly depends on the doping profile. The larger the  $s$ , the larger the capacitance variation will be, i.e. the tuning range, with the biasing voltage. For  $m = 0$  the profile corresponds to a uniformly doped one-sided abrupt junction. For  $m \leq -1$  the so-called hyper-abrupt junctions are formed, and they have higher sensitivity [14, 20].

A theoretical analysis has demonstrated that cancellation of distortion arising from the non-linear C-V varactor characteristics can occur for circuit topologies when the doping is such that  $s$  is  $\geq 0.5$  [21]. For instance, a theoretical ‘Distortion-Free Varactor Stack’ (DFVS) configuration can be achieved with an anti-series connection of two identical uniformly doped varactors ( $s = 0.5$ ), while a ‘High Tuning Range Varactor Stack’ (HTRVS) topology based on an anti-series/anti-parallel configuration of four hyper-abrupt varactor diodes ( $s > 0.5$ ) can facilitate linear operation with higher  $C_{max}/C_{min}$  ratio [22]. In particular, novel configurations have been recently presented, namely the ‘Narrow/Wide Tone-Spacing Varactor Stack’ (NTSVS-WTSVS) to solve even further linearity constraints with narrow and wide tone-spacing in a single technology [17, 19], while also providing an increased tuning range. These circuit topologies are based on varactors with an exponential C-V relationship. The required *n*-doping profile is composed of a lightly-doped top layer, which is fully depleted at zero bias voltage, with an abrupt transition to a  $1/x^2$ -like profile. From a technological point of view, fabrication of these hyper-abrupt  $p^+n$  junction profiles is now possible owing to the recent developments of As-doped epitaxial growth techniques [23]. Moreover, the optimized circuit topologies are also less sensitive to process deviations [15, 17].

- b) *High Q-factors translate into efficient elimination of losses from parasitic resistances and capacitances.*

While the silicon-on-insulator (SOI) technology has the merit of having enhanced significantly the RF circuit characteristics due to substrate-loss reduction, the back-wafer contacted silicon-on-glass technology developed at DIMES has ultimately pushed even further the capability to enable the fabrication of high performance low-power RF integrated circuits with on-chip integration of active devices and high quality passive components [24]. First, the high-precision lithography for patterning of the back-wafer-aligned contacts in the substrate-transfer technology improves the access to the active device areas for the electrical terminals. This unique property is particularly attractive from the device design point of view, since very compact layouts are possible and device structures approach theoretical one-dimensional behavior. The process has been further enhanced with low-ohmic and low-defect contacts, which are formed by excimer laser annealing of implanted arsenic, and low metal-track resistance by using thick copper electroplating.

Based on these two approaches, implemented varactor configurations have shown output third-order intercept point ( $OIP_3$ ) of  $\sim 60$  dBm and average Q-factor of 80–100 at 2 GHz [19]. These excellent results, however, strongly rely on the technique used for formation of the front  $p^+$  anode region. For linearity requirements, the challenges are to guarantee one-sided junctions and, at the same time, that the  $p^+$  process should not involve temperatures or defect creation that cause any significant arsenic diffusion by thermal or transient-enhanced effects. Moreover, an ultra-low-loss tunable element can be targeted if the  $pn$ -junction is not affected by excessive diode leakage current at reverse biasing. Finally, theoretical breakdown voltages should be achieved in order to effectively profit from the wider tuning range. Therefore, in this thesis the B-deposition is also considered as a solution to such specific technology demands.

### 1.2.2 Photodiodes for detection of ultraviolet (UV) radiation

Recent years have witnessed a significant growing interest for development and fabrication of highly sensitive and stable detectors for radiation in the ultraviolet (UV) spectral range ( $\lambda = 400\text{--}10$  nm), particularly at vacuum UV (VUV) wavelengths ( $\lambda = 200\text{--}10$  nm), down to soft X-rays ( $\lambda = 10\text{--}0.1$  nm). This has been mainly driven by advances in lithography equipment, since several sensors are used to evaluate and optimize the imaging performance as position sensing and beam intensity monitoring. In fact, for future high-volume nanoelectronics manufacturing, after ArF ( $\lambda = 193$  nm) and F<sub>2</sub> ( $\lambda = 157$  nm) excimer-laser lithography systems, the semiconductor industry has chosen to develop extreme-ultraviolet (EUV) lithography tools with 13.5 nm radiation wavelength, and commercialization is planned for application at the 22 nm device node by 2014 [25]. Furthermore, remote sensing instrumentation needed for next solar metrology missions have also triggered an intense research of high-performance devices for radiation detection at visible, EUV, and X-ray wavelengths [26].

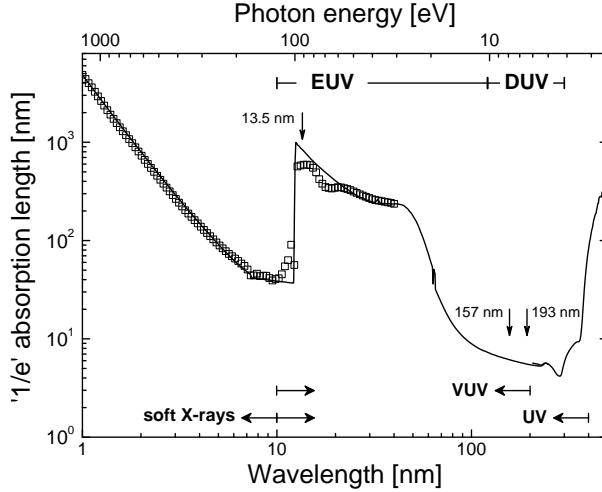
For many such applications, the radiation-sensitive area is exposed to high photon

flux doses and is generally affected by either surface or bulk contamination. These harsh conditions readily deteriorate the optical performance and limit the lifetime of the device itself. Therefore, ruggedness and long-term stability to high radiant exposure and aggressive environments is one of the key features demanded for detector applications in the VUV spectral range, along side extreme requirements for excellent reliability, high and spatially uniform sensitivity, wide dynamic range, high linearity, and low noise, i.e. low dark current.

Solutions for UV radiation detection are generally offered by silicon-based devices, which are inherently responsive to a broadband radiation extending from the near infrared region wavelengths ( $\leq 1 \mu\text{m}$ ) down to soft X-rays ( $\lambda \sim 1 \text{ nm}$ ). Moreover, they have attractive characteristics in terms of accuracy and prediction of optical efficiency [27]. Although III-N wide-bandgap semiconductors, like gallium nitride (GaN), aluminum nitride (AlN), aluminum-gallium nitride (AlGaN), have been recently considered as promising candidates mainly due to their radiation hardness [28–30], they still face lower sensitivity and many processing issues compared to more mature and cost-effective Si technologies. Even their intrinsic solar-blindness, i.e. a good UV/visible response ratio, can be feasibly achieved for silicon devices. In fact, it has been demonstrated that integration of a thin film of a suitable filtering material directly on the exposed surface is fully compatible and makes possible selective response to a much narrower band [31].

Regarding the device structure, documented methods of producing reliable UV detectors involve mainly planar diffused silicon *pn*-junctions, either  $p^+n$  [32] or  $n^+p$  [33], and Schottky diodes [34]. Instead, natural-inversion-layer photodiodes result in low yield due to poor process control of the indirect method of forming the surface depletion and conductive top-layer. As stated above, diffusion-type photodiodes have lower dark current. In addition, they are much more sensitive than Schottky-type photodiodes either on Si or III-N compounds, especially at deep-ultraviolet (DUV) wavelengths (120–200 nm). The limited radiation sensitivity for Schottky diodes might be due to a combination of several factors, mainly dependent on the specific photodiode technology, such as high reflection and absorption losses in the front metal contact, lower surface electric field, and higher surface recombination. On the other hand, the presence of a metallic front-layer has been demonstrated to provide more stable performance under heavy radiation exposure [35]. Similar ruggedness has been reported for metal-silicide windows on  $n^+p$  junction diodes [36, 37].

Moreover, for planar diffused diodes, the spectral sensitivity to UV radiation is also dependent on the Si absorption coefficient, since the ‘ $1/e$ ’ penetration depth of UV photons into silicon approaches values lower than 10 nm in the wavelength range of 100–350 nm, as shown in Fig. 1.3. In particular, a minimum of  $\sim 5 \text{ nm}$  is reached at the DUV wavelengths of applicative interest, such as  $\lambda = 157 \text{ nm}$  and  $\lambda = 193 \text{ nm}$ . Therefore, to optimize the optical conversion efficiency the uppermost edge of the depletion region should be within this distance. However, commercial *np*-junction diodes more simply rely on both the built-in electric field induced by the gradient of the  $n^+$  diffused doping profile and the formation of junctions shallower than the diffusion length of the minority carriers. The latter requirement is quite straightforward to realize, since the diffusion length of holes is about  $0.4 \mu\text{m}$  or higher for



**Figure 1.3:** ‘1/e’ absorption length in Si as a function of the radiation wavelength in the UV/soft X-rays spectral range: — after Ref. [38], □ after Ref. [39].

the reported  $n^+$  doping levels of about  $10^{18}$ – $10^{19}$  cm $^{-3}$ . Most of the built-in electric field is also induced by steep dopant pile-ups that are intentionally formed during thermal growth of SiO<sub>2</sub> coating layers. In fact,  $n$ -type species, such as arsenic and phosphorus, segregate at the Si/SiO<sub>2</sub> interface [33]. In contrast, for boron profiles an opposite segregation mechanism does not allow to tailor the electric field in this manner, and thus the carrier collection efficiency is poorer than the  $n^+p$  implementation. Furthermore, the presence of positive charges in the anti-reflection oxide coating can induce further carrier losses in the  $p^+$  front region, since the resulting electric field will hinder the carrier collection. For these reasons,  $n^+p$  photodiodes have been generally preferred over  $p^+n$  junctions and claimed to be inherently more stable than boron-diffused devices in UV spectral range [40]. However, one could easily argue that the  $n^+$  surface peak would be too strictly dependent on the presence of the SiO<sub>2</sub> front-layer, which can be either a cause of radiation absorption at short wavelengths or radiation-induced degradation.

On the other hand, the ability to form extremely ultrashallow and highly-doped junctions can maximize the optical performance up to the theoretical limits even for  $p^+n$  photodiodes, as in the case of B-deposition. In fact, the reduced junction depth would significantly increase the percentage of carriers generated in the depletion region. At the same time, the electric field induced by the high-concentration doping profile would efficiently separate any further electron-hole pairs created in the shallow diffused area, since it will not be confined within the space-charge region, but it would extend until the surface [14]. The high doping concentration can have the additional advantage of being able to screen any influence of oxide charges when anti-reflection coating layers are needed. Moreover, the enhancement of carrier collection by such doping-induced electric fields strongly prevents any recombination of photogenerated

carriers at the Si surface or Si/SiO<sub>2</sub> interface, since minority carriers will be in the presence of recombination traps for a negligible time.

### 1.3 Outline of the thesis

The thesis is organized as follows. The following Chapter illustrates the experimental procedures for the formation of CVD boron layers on Si surfaces. Transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) are used to study the morphology and the boron content in the deposited layers, respectively. The analytical characterization is then coupled to electrical measurements of test structures incorporating the layers in order to study the boron surface doping and junction depth. In Chapter 3, the previous results are assessed with respect to reliable implementation of B-deposition in Si devices. The electrical properties of the B-layers are extensively investigated as a function of the processing conditions by fabricating contacts, diodes, and *pnp* bipolar structures. The thermal stability and doping efficiency of B-layers during the subsequent drive-in process are examined in Chapter 4. Both *in-situ* and *ex-situ* thermal anneals are considered. Chapter 5 reports on the B-deposition applied to the silicon-on-glass varactor technology. Particular accent is set on the reverse-biased I-V characteristics of as-deposited B-diodes. Processing and design solutions are also discussed which aim to increase the maximum operating voltage up to theoretical breakdown limits. Fabrication of planar *p<sup>+</sup>n* photodiodes for UV radiation detection is illustrated in Chapter 6, where B<sub>2</sub>H<sub>6</sub> exposure conditions are properly tuned to optimize the optical conversion efficiency. In addition, the technology is demonstrated to be tailored for further improvement of photodiodes parameters, such as series resistance, by also combining the pure B-deposition with optional extra-processing steps. The electrical and optical performance of the fabricated photodiodes are shown, also with respect to their stability after high dose irradiation. Finally, Chapter 7 gives the main conclusions and provides recommendations for the future work.



## Chapter 2

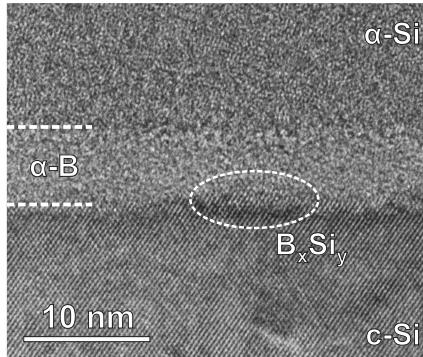
# Chemical vapor deposition of boron layers

The experimental conditions for the deposition of boron layers on Si surfaces are described here. Analytical characterization techniques have been applied to investigate the film morphology and the boron content as function of processing parameters. The Chapter also reports on the study of the surface boron doping to determine the diffused active boron doses and the resulting  $p^+$ -junction depths by means of electrical test structures. The experimental results have been also validated by process and device simulations, which have been carried out with the Taurus TSUPREM-4<sup>TM</sup> and MEDICI<sup>TM</sup> softwares, respectively, [41, 42].

### 2.1 Processing conditions

The B-layer formation is performed in an ASM Epsilon One reactor by chemical vapor deposition (CVD) at either atmospheric pressure (AP), i.e. 760 Torr, or reduced pressures (RP), such as 60 Torr or 36 Torr. The depositions themselves have been monitored for processing temperatures ranging from 500 °C to 800 °C. Diborane (B<sub>2</sub>H<sub>6</sub>) is injected into the reactor chamber as the dopant gas with a typical flow rate of 490 sccm, while hydrogen (H<sub>2</sub>) is used as the carrier gas and for dilution of the doping source. Rotation of the sample can provide homogeneous exposure preventing gas depletion phenomena. Nevertheless, the influence of the doping gas flow on the deposition process has been also investigated for various diborane partial pressures (10<sup>-8</sup>–10<sup>-3</sup> Torr). For a given temperature, ambient pressure and diborane concentration, the boron coverage of the Si surface and the doping of the crystalline silicon substrate can be controlled by varying the deposition time. The results presented here correspond to exposures in the range of 1 s to 30 min.

It is known that the boron atoms will not be adsorbed as a distinct layer on SiO<sub>2</sub> [2, 9, 10], so it is crucial to provide an oxide-free Si surface for the deposition. This is achieved by first treating the substrates by conventional wet cleaning and HF dipping.



**Figure 2.1:** High-resolution TEM image of a B-layer formed after 10 min  $\text{B}_2\text{H}_6$  exposure at 700 °C. The sample has been covered with PVD  $\alpha$ -Si as contrasting layer.

In the reactor itself, any remaining native  $\text{SiO}_2$  is removed before  $\text{B}_2\text{H}_6$  exposure by an *in-situ* thermal cleaning step in  $\text{H}_2$  ambient at 900 °C for 30 min. In the case of a patterned  $\text{SiO}_2$  layer being used as hard-mask for selective B-deposition, the pre-bake step should be carried out at atmospheric pressure to avoid high-temperature silicon-dioxide decomposition [43, 44]. However, lower temperatures, such as 700 °C, have also been demonstrated to be appropriate for *in-situ* surface cleaning.

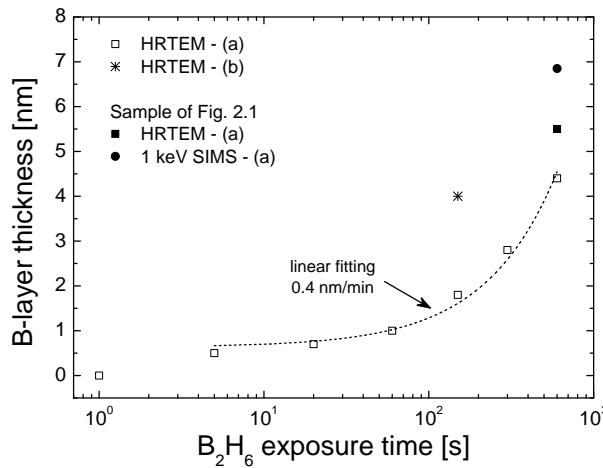
Finally, in our experiments only (100) Si wafers have been exposed to the gas mixture, due to their wide use in device fabrication. However, while the deposition rate of pure boron layers is independent of the crystallographic orientation [9], Saitoh's work demonstrated (100) silicon surfaces to induce faster growth for boron-silicide films as compared to (111) substrates.

## 2.2 Transmission electron microscopy analysis

### 2.2.1 B-layer morphology and growth rate

A high-resolution TEM image of a B-layer formed after 10 min  $\text{B}_2\text{H}_6$  exposure at 700 °C in a 760 Torr ambient is shown in Fig. 2.1. During the thermal decomposition of diborane, the high gas-source injection (490 sccm) causes boron atoms to readily segregate on the bare silicon surface in amorphous phase, thus forming an  $\alpha$ -B layer. In addition, at such temperature the very high and uniform B content at the Si interface induces boron atoms to initiate a reaction with the silicon in a boron-silicon phase [9]. Thus a boron silicide  $\text{B}_x\text{Si}_y$  layer is also formed, which is here seen as a roughening of the c-Si surface.

The film is uniform, and the corresponding average thickness determined from HRTEM images is shown in Fig. 2.2 as a function of the  $\text{B}_2\text{H}_6$  exposure time at 700 °C. Apart from the 5 s exposure point, the time dependence of the B-layer thickness for the CVD on blanket Si surfaces is quite linear with a calculated growth rate of 0.4 nm/min. At the early stage of the deposition, such as at 5 s, HRTEM



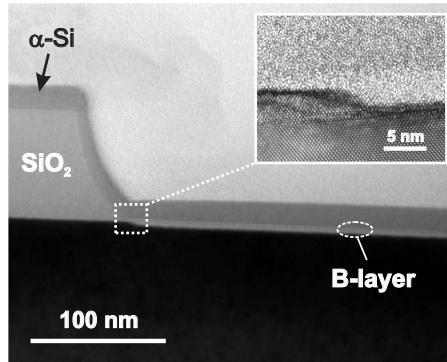
**Figure 2.2:** The average B-layer thickness as a function of  $B_2H_6$  exposure time at 700 °C determined from HRTEM images. For the 10 min as-deposited sample shown in Fig. 2.1, the physical thickness is also compared to the full-width-at-half-maximum (FWHM) of the corresponding SIMS (1-keV- $O_2^+$ ) boron profile. The analytical characterization was performed on samples where B-layers were deposited either (a) on blanket (100) Si surfaces or (b) in contact windows.

images revealed adsorbed boron to either approximately form an atomic plane on silicon or interact non-homogeneously with the first atomic Si plane, the distance between {100} Si planes being equal to the lattice constant of 5.4 Å. Finally, the deviation between the 10 min B-doped samples is probably due to the temperature calibration of the reactor chamber, which has been performed in different time frames.

### 2.2.2 Topography dependence: selectivity, uniformity, and isotropy

TEM imaging has been used to investigate the growth of B-layers performed directly into contact windows of various sizes ranging from  $1 \times 1 \mu\text{m}^2$  to  $450 \times 450 \mu\text{m}^2$ . The windows have been wet-etched into a 100 nm thermal silicon oxide. The pattern dependence has been studied for samples with 4 min *in-situ* pre-bake step at 700 °C followed by a 2.5 min  $B_2H_6$  exposure at the same temperature.

The TEM image of Fig. 2.3 shows that the pure diborane exposure provides selective deposition on Si: no boron can be observed on the flat or beveled  $\text{SiO}_2$  surfaces. In the window, the boron layer is seen to be continuous and uniform across the Si with an average thickness of 4 nm independent of the window sizes investigated. The film is, however, thicker than the layers deposited on the bare Si surface, as shown in Fig. 2.2. An inspection of the window periphery reveals a  $\sim 3$  nm recession of the Si with respect to the Si/ $\text{SiO}_2$  interface, which, at least in part, is due to the cleaning steps performed before and after loading the sample into the reactor. Some



**Figure 2.3:** TEM image of a B-layer directly formed in a contact window during a 2.5 min  $\text{B}_2\text{H}_6$  exposure at  $700^\circ\text{C}$ . The inset shows an enlarged view of the edge periphery that reveals a  $\sim 3$  nm recession of the Si with respect to the  $\text{Si}/\text{SiO}_2$  interface.

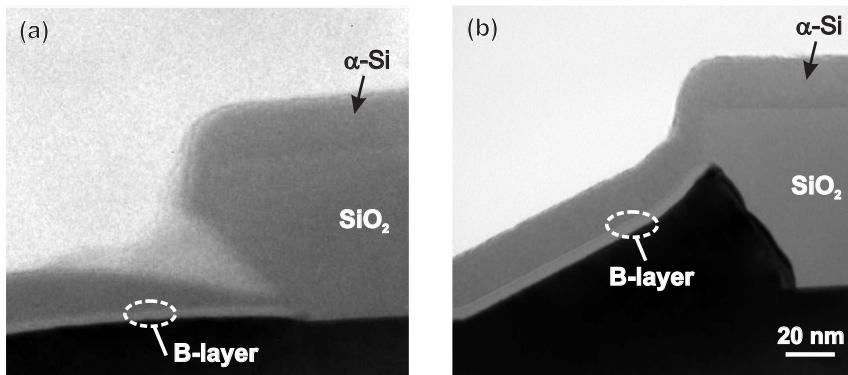
Si consumption may also be due to the reaction with B atoms during formation of the boron-silicide layer [9].

Figs. 2.3 and 2.4 can be used to compare three different types of contact window perimeters after 2.5 min B-deposition. The non-conventional topographies of the window edges seen in Fig. 2.4 have been formed after *in-situ* thermal cleaning at low pressure and at a temperature of  $900^\circ\text{C}$ . Under these conditions, the oxide sidewalls are steadily undercut as a result of  $\text{SiO}_2$  decomposition at the perimeter of the contact opening. This is due to the reaction  $\text{Si} + \text{SiO}_2 \longrightarrow 2\text{SiO}$ , where the SiO is a volatile product [43, 44]. In addition to this, on a clean Si surface, as obtained here by *in-situ* H-baking, the Si atoms will be mobile and can accumulate at the perimeter of patterned areas. In all cases, the CVD process ensures excellent boron coverage of the silicon surface up to the oxide edge, whether a cavity, e.g. Fig. 2.4(a), or a Si mount, e.g. Fig. 2.4(b), was formed. The latter case evidences that the growth mechanism is isotropic, since the B-layer thickness appears to be independent of the c-Si surface orientation, as expected for temperatures  $\leq 700^\circ\text{C}$  [9].

### 2.2.3 Low-temperature deposition

The growth rate of the B-layers, as well as the resulting layer-stack composition, is dependent on the deposition temperature [9]. At temperatures below  $600^\circ\text{C}$ , the decomposition of diborane, although not completely dissociative, has been found to result in the formation of pure boron layers, while at  $700^\circ\text{C}$  some reactivity with the silicon atoms is initiated, and the consequent silicidation of the B-layer increases with temperature.

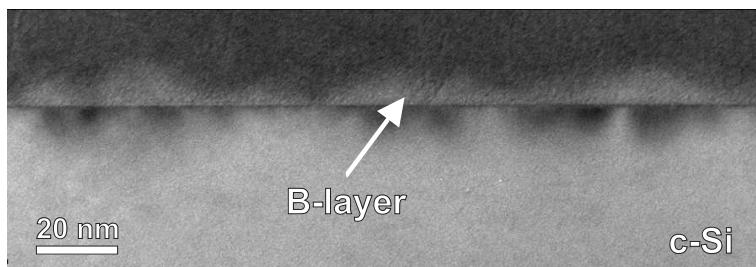
In Fig. 2.5, a TEM image is shown for a substrate treated with 10 min  $\text{B}_2\text{H}_6$  exposure at  $500^\circ\text{C}$ . A B-layer was formed with an average thickness of  $\sim 6$  nm, although the uniformity along the Si surface is poor in comparison to deposition at  $700^\circ\text{C}$ . In fact, at low temperatures, boron forms preferably B-rich grains separated by regions



**Figure 2.4:** TEM images of contact windows after 2.5 min B-deposition at 700 °C. The SiO<sub>2</sub> etch geometry was generated by low pressure *in-situ* thermal cleaning at 900 °C before diborane exposure.

of clean silicon, while larger and rough islands are formed by coalescence of several grains after longer exposures [10, 45]. On the other hand, depositions performed at higher temperatures, even for shorter times, exhibited better spatial homogeneity. Therefore, it is probable that high temperatures enhance the migration of species along the Si surface, besides promoting the reactivity of boron with Si atoms.

Furthermore, the bending contours of the TEM diffraction contrast image reveal the presence of local stress between the B-layer and the c-Si substrate. The stress might be induced by an altered lattice parameter at the Si surface due to the deposited B atoms. Variation in lattice plane distances could not really be discerned, although a tendency towards a lower {110} lattice plane distance, i.e. horizontal compression, was observed. As reported in [3], such structural effect would be in agreement with the fact that boron substitution at the (100) Si surface will distort the Si lattice to achieve a Si—B bond length of 2.0–2.1 Å, substantially shorter than the 2.35 Å bond length in bulk silicon.



**Figure 2.5:** TEM image of a B-layer formed after a 10 min B<sub>2</sub>H<sub>6</sub> exposure at 500 °C. The analysis has been performed with the electron beam direction a few degrees away from [110] so that the 220 reflection is in the Bragg's condition.

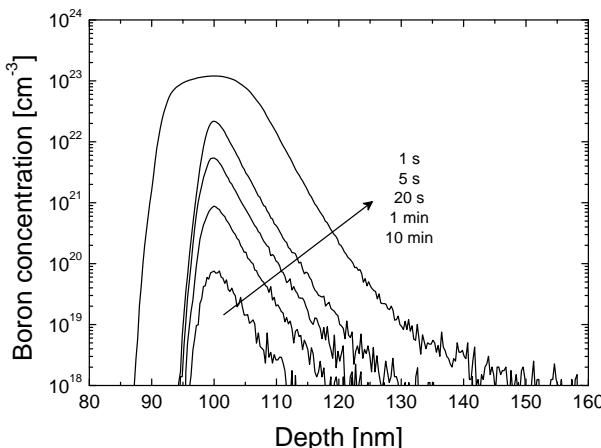
## 2.3 Secondary ion mass spectrometry analysis

### 2.3.1 Boron content in as-deposited layers

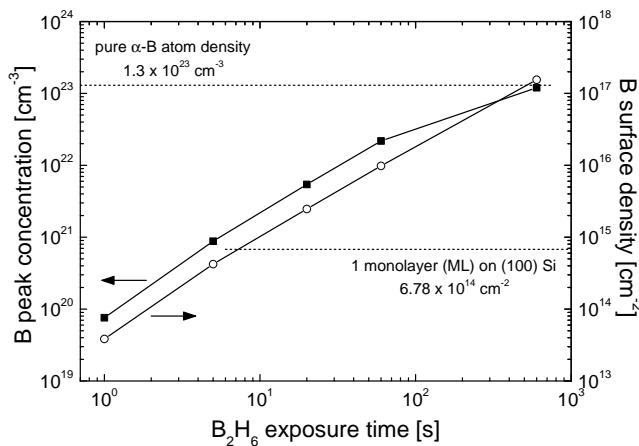
The number of boron atoms in as-deposited layers has been monitored by using secondary ion mass spectrometry (SIMS) with  $O_2^+$  primary ion beam either at 2 keV or 1 keV. On the other hand, oxygen levels were monitored by using  $Cs^+$  primary ions at 3 keV. In order to get an accurate SIMS signal from the surface, a layer of 100 nm amorphous silicon ( $\alpha$ -Si) has been sputtered on the samples at room temperature after the boron deposition.

In Fig. 2.6 SIMS profiles are shown of B-layers formed at 700 °C for various deposition times. The  $B_2H_6$  exposure was performed at atmospheric pressure with a flow rate of 490 sccm. Both the B peak concentrations and the integrated surface densities have been extracted, and the corresponding values are presented in Fig. 2.7 as a function of the deposition time.

The SIMS analysis of these ultrashallow and highly-doped layers will be influenced by the knock-on effect, which gives errors in determining the absolute value of boron concentration and limits the depth resolution. Nevertheless, the B-content increase seen in these measurements is similar for both surface density and peak concentration, and the time dependence has a grading coefficient of 1.2. The concentration peak of the SIMS profiles seems to saturate at the equivalent atom density of amorphous B for very long exposures, the latter being determined by the atomic weight (10.81 g/mole) and density (2.34 g/cm<sup>3</sup>) of boron [46]. On the other hand, the time dependence of the surface density has shown that the saturation coverage occurs within the first 20 s followed by a transition to the non-self-limiting segregation of boron. As is also visible from TEM images and indicated in Fig. 2.2, after 5 s the boron coverage starts



**Figure 2.6:** SIMS profiles (2-keV- $O_2^+$ ) of B-layers formed for 1 s to 10 min deposition at 700 °C. For comparison, the point of boron peak concentration has been moved to 100 nm in all cases.



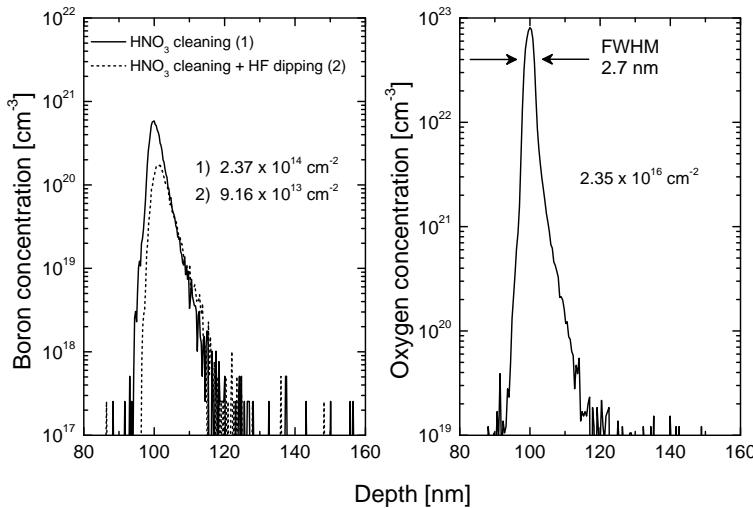
**Figure 2.7:**  $\text{B}_2\text{H}_6$  exposure time dependence at  $700\text{ }^\circ\text{C}$  of boron peak concentration (left y-axis) and surface density (right y-axis) as determined from SIMS profiles shown in Fig. 2.6.

to exceed the surface atomic density of one monolayer (ML), which corresponds to  $6.78 \times 10^{14} \text{ cm}^{-2}$  on (100) Si. High-resolution SIMS profiling was performed on the sample with a 10 min B-deposition and the full-width-at-half-maximum (FWHM) value, also included in Fig. 2.2, is in good agreement with the other data.

### 2.3.2 B-layer removal

The chemical reactivity of boron with  $\text{HNO}_3$ -based acid solutions [9, 46] can facilitate the removal of the  $\alpha$ -B layer in a standard cleaning process. After a 10 min B-deposition at  $700\text{ }^\circ\text{C}$ , a substrate has been soaked for 10 minutes in a boiling concentrated nitric acid solution (65%) at  $110\text{ }^\circ\text{C}$ . The resulting boron and oxygen profiles are shown in Fig. 2.8. The cleaning step completely dissolves the high-boron peak region ( $> 10^{23} \text{ cm}^{-3}$ ), which supports the assumption that it is a metal-like boron layer. The oxygen delta-profile, which has a FWHM of only  $\sim 3$  nm, is most likely due to cleaning-induced oxidation of about 1.3 nm of silicon, assuming that the Si thickness is 0.455 times the oxide thickness. A 4 min dipetch in an HF solution (0.55%) removes the oxide.

After the  $\text{HNO}_3$  treatment, the boron SIMS profile reveals a concentration peak of  $6 \times 10^{20} \text{ cm}^{-3}$  that is slightly reduced upon HF dipping, showing that some boron atoms are also incorporated in the cleaning-induced oxide. A similar high boron concentration ( $8 \times 10^{20} \text{ cm}^{-3}$ ) was also obtained by using a 750-eV-SIMS analysis, as shown in the following section. Since these levels considerably exceed the B solid solubility of  $1.7 \times 10^{19} \text{ cm}^{-3}$  at  $700\text{ }^\circ\text{C}$  in bulk Si [47], the surface peak is attributed to the high boron content in the  $\text{B}_x\text{Si}_y$  layer, which is only partly oxidized and removed during the  $\text{HNO}_3 + \text{HF}$  cleaning sequence [13].

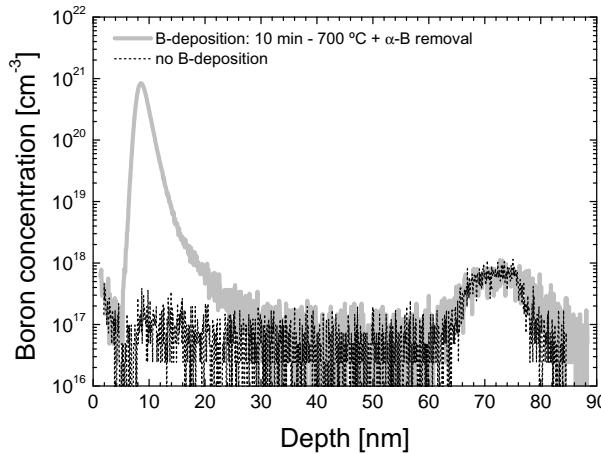


**Figure 2.8:** Boron and oxygen SIMS profiles of an as-deposited 10 min B-doped layer formed at 700 °C after standard cleaning in boiling  $\text{HNO}_3$ . The boron profile resulting from the removal of the cleaning-induced oxide with an HF dip is also shown.

### 2.3.3 Boron diffusion during the deposition

Along with the surface reactions that induce formation of a B-layer, diffusion of boron atoms into the Si substrate is also accomplished during the  $\text{B}_2\text{H}_6$  exposure [8,13]. However, the doping of the c-Si is too light to be distinguished in the HRTEM or in the corresponding B-profile determined by SIMS. For the application in devices it is important to know if this doping and the background doping are affected by any deposition-associated defect formation that causes transient-enhanced (TED) or boron-enhanced diffusion (BED). In particular, the latter effect has been observed during annealing at 950 °C either for B-implanted samples when the dopant dose exceeds  $1 \times 10^{15} \text{ cm}^{-2}$  or for an evaporated B-layer containing  $3.2 \times 10^{16} \text{ cm}^{-2}$  boron atoms on the Si surface [48]. The influence is, however, more pronounced in the former case. In both situations, the formation of a silicon-boride phase due to the high B content is assumed to be a source of excess interstitials.

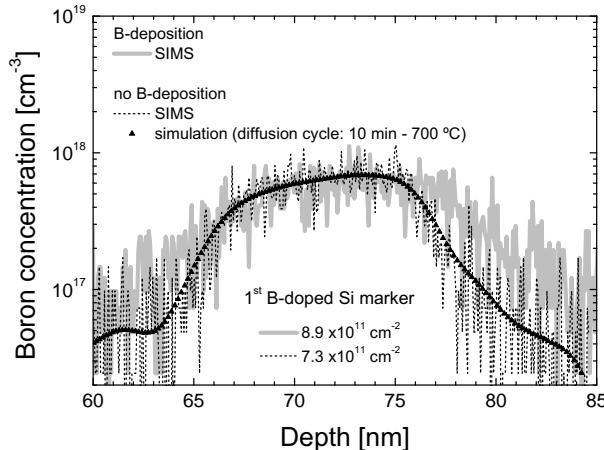
Enhanced diffusion effects have been evaluated, here, by examining the out-diffusion of epitaxially grown B-doped Si markers after a 10 min B-deposition at 700 °C. This layer contains  $1.55 \times 10^{17} \text{ cm}^{-2}$  boron atoms, which is much higher than in the above mentioned evaporated layer, but the process/anneal temperature is much lower, i.e. 700 °C, instead of 950 °C. Two samples were fabricated with 20-nm-wide B-markers located approximately at a depth of 70 nm, 350 nm, and 700 nm. The resulting B-layer has been removed to minimize the SIMS knock-on effect, and then a capping layer of 10 nm amorphous silicon has been deposited at room temperature on both samples. A SIMS with primary  $\text{O}_2^+$  beam energy of either 2 keV or 750 eV was used to study the diffusion in respectively all the markers or, with improved



**Figure 2.9:** SIMS profiles ( $\text{O}_2^+$  primary ion beam at 750 eV) of samples with and without a 10 min B-deposition at 700 °C on a Si wafer containing epitaxially-grown B-doped Si markers. The  $\alpha$ -B layer was removed with  $\text{HNO}_3$  cleaning and HF dip etching before covering the sample with 10 nm PVD  $\alpha$ -Si.

resolution, the region within 100 nm of the surface. The boron profiles obtained from the latter analysis condition are shown in Figs. 2.9–2.10.

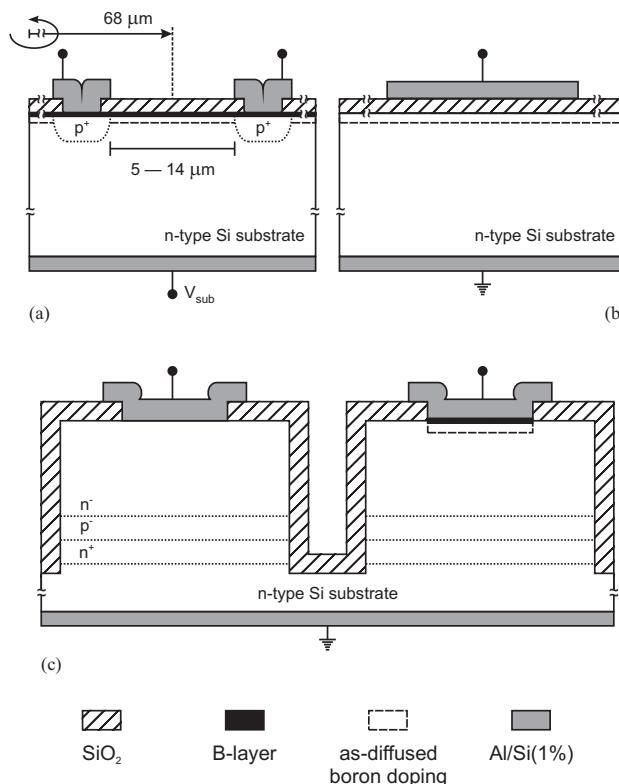
Firstly, although the doping profile might still be influenced by the SIMS energy and the high B concentration peak at the surface, the junction depth for an *n*-type background doping level of  $10^{17} \text{ cm}^{-3}$  is expected to be within 20 nm of the sur-



**Figure 2.10:** Enlarged view of the SIMS profiles shown in Fig. 2.9 for the first B-marker. The result of a simulation of a 10 min thermal anneal at 700 °C of the original B-marker is also included.

face. Thus the drive-in of boron atoms during the CVD process itself is very limited. However, more accurate profiling has been achieved with capacitance-voltage measurement technique, as described in Section 2.4.3 on page 27.

Secondly, within the resolution of the high-energy SIMS, no broadening of the B-markers could be discerned. However, the B-profiles obtained with a 750-eV-analysis did show very slight deviations at the first marker of the different samples, as can be seen in Fig. 2.10. To evaluate the possible effect of the 10 min thermal processing cycle at 700 °C in itself, a diffusion simulation was performed on the as-grown B-doped Si marker. This did not reveal any diffusion effects. This result along with the spread in the calculated B-doses is a clear indication that the differences should be accorded to variations in the original B-doped epitaxial growth rather than enhanced-diffusion effects. Thus, the high B-concentration and gradient at the surface is only instrumental in doping of the c-Si up to the solid solubility by thermal diffusion.



**Figure 2.11:** Schematic cross-sections of the fabricated test structures used to determine: (a) sheet-resistance, (b) as-diffused boron doping density, and (c) junction depth.

## 2.4 Electrical characterization of surface boron doping

This section illustrates the electrical measurements of sheet-resistances and depletion-type MOS-capacitors that have been used to determine the active boron concentration in the silicon substrate. In addition, the corresponding junction depth has been extracted from capacitance-voltage profiling.

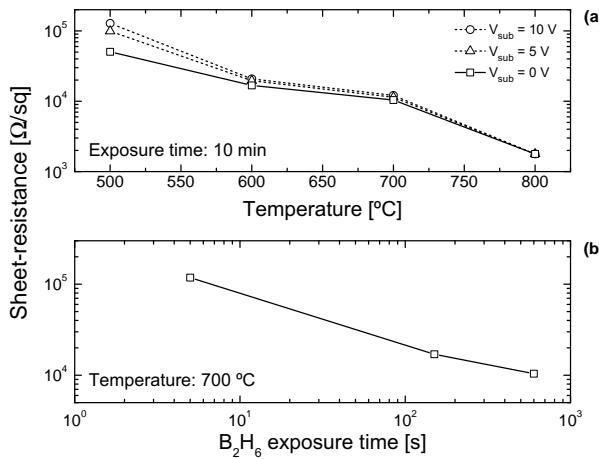
Schematic cross-sections of fabricated test structures are shown in Fig. 2.11. The devices were fabricated on  $n$ -type 2–5  $\Omega\text{cm}$  substrates. For the sheet-resistance and MOS capacitance-voltage measurements, the B-layer was prepared uniformly over the wafer and covered with 300 nm PECVD TEOS oxide. The B-layer itself was contacted via contact windows to pre-fabricated implanted  $p^+$  plugs, and PVD Al/Si(1%) metallization of both the front and backside of the wafer provided electrodes to the  $n$ -wafer as well as the  $p$ -type regions and gates on the front side. For the C-V profiling technique, an epitaxial  $n^-$ - $p^-$ - $n^+$  layer stack was grown on  $n$ -type substrates. Shallow trenches were made to isolate the devices. Then LPCVD TEOS oxide was deposited in which contact windows were etched for B-deposition and subsequently metalized. Schottky diodes were also formed on the same sample by contact opening to the neighboring structure and Al/Si(1%) deposition. For all devices, the boron layer was formed at atmospheric pressure with a  $\text{B}_2\text{H}_6$  flow rate of 490 sccm.

### 2.4.1 Sheet-resistance measurements

The sheet-resistance of as-deposited B-layers has been determined by using differential electrical measurements on ring-shaped structures similar to those described in [49]. In Fig. 2.12(a) the extracted sheet-resistance  $\rho_s$  is shown for samples with 10 min deposition at temperatures ranging from 500 °C to 800 °C. In addition, the time dependence of  $\rho_s$  is reported in Fig. 2.12(b) for  $\text{B}_2\text{H}_6$  exposures performed at 700 °C. The reduction of the sheet-resistance with either the deposition temperature or time is reasonably consistent with the expected diffusion rate of boron into the silicon, where the B concentration peak is limited by the solid solubility. Therefore, higher dopant activation is obtained with increasing temperatures and this in turn reduces the influence of the substrate bias voltage on  $\rho_s$ , as also seen in Fig. 2.12(a).

Above 700 °C a boron-silicide film is formed [9,10], but of relatively thin layers of a few nm. Thus, the lateral conductivity should still be dominated by impurity diffusion, if the reported resistivity values for B-Si phases of 0.2–20  $\Omega\text{cm}$  apply [50]. On the other hand, based on experimental results reported by [51], formation of  $\text{B}_{12}$  icosahedron could influence the electrical properties of the B-layer, and the corresponding sheet-resistance would be comparable to that of the boron-doped c-Si region. Such boron phase was demonstrated to be induced by heavy doping implantations ( $\geq 3 \times 10^{16} \text{ cm}^{-2}$ ) into silicon substrates, and concomitantly a high hole concentration (about  $10^{21} \text{ cm}^{-3}$ ) was generated without any post-annealing. Thus,  $\text{B}_{12}$  was proposed to be responsible for the measured low resistivity (2  $\text{m}\Omega\text{cm}$ ) by acting as a double acceptor.

Sheet-resistance measurements of B-exposed areas have been also performed after  $\text{HNO}_3$  cleaning and HF dipping until a hydrophobic surface was achieved. This



**Figure 2.12:** Sheet-resistance of B-layers as a function of (a) deposition temperature, and (b) B<sub>2</sub>H<sub>6</sub> exposure time.

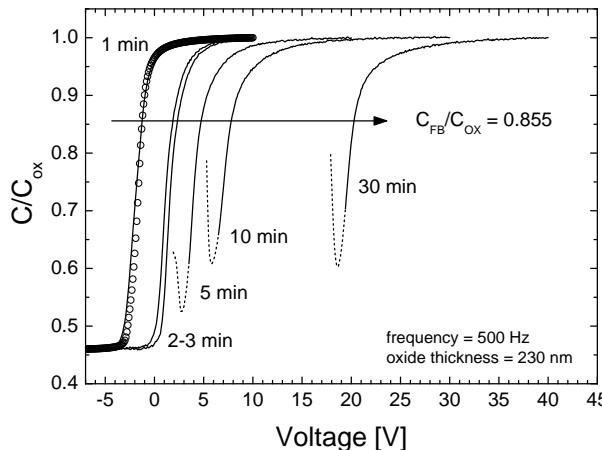
removal of the B-layer significantly increases the sheet-resistance. In particular, for exposure times shorter than 5 min, the *p*<sup>+</sup> boron-doped region is either largely removed or depleted by charges in the field isolation oxide. The latter observation is confirmed by capacitance-voltage measurements described in the following section. A summary of sheet-resistance for B-layers formed at 700 °C without and with the HNO<sub>3</sub> + HF cleaning process is given in Table 2.1.

#### 2.4.2 Depletion-type MOS-capacitors

A quantitative analysis of the active boron dose diffused in the c-Si substrate during the deposition process is enabled by capacitance-voltage measurements of depletion-type *p*-channel MOS devices, since variation of the doping underneath the gate oxide can readily affect the C-V characteristics in terms of either threshold or

**Table 2.1:** Sheet-resistance of B-layers deposited at 700 °C before and after the HNO<sub>3</sub> cleaning + HF dipping sequence.

Sample description		Sheet-resistance	
B <sub>2</sub> H <sub>6</sub> exposure time	α-B removal	[Ω/sq]	
2.5 min	no	1.8 × 10 <sup>4</sup>	
10 min	no	1.0 × 10 <sup>4</sup>	
≤ 5 min	yes	-	
10 min	yes	2.5 × 10 <sup>5</sup>	
30 min	yes	5.9 × 10 <sup>4</sup>	



**Figure 2.13:** Normalized C-V characteristics of depletion-type *p*-MOS structures fabricated for various min-long  $\text{B}_2\text{H}_6$  exposures at  $700^\circ\text{C}$  followed by an  $\text{HNO}_3 + \text{HF}$  cleaning sequence. The shift of the flatband voltage due to boron doping of the c-Si substrate is also indicated. The 1 min B-doped sample has been assumed as reference. The simulated  $C/C_{\text{OX}}$  curve (open-circles) is of an equivalent enhancement-type MOS structure with  $D_B = 0$  and  $D_{\text{OX}} = 9.25 \times 10^{10} \text{ cm}^{-2}$ .

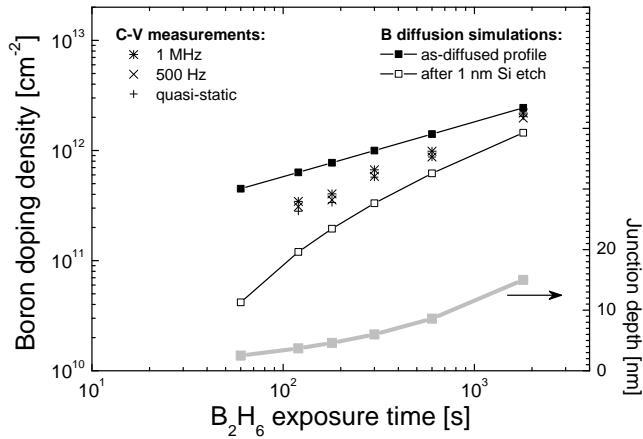
flatband voltages [14].

However, since the presence of the B-layer has been found to screen any influence of the metal/ $\text{SiO}_2/\text{Si}$  system up to  $\pm 100$  V, the  $\alpha$ -B layer was removed before performing gate oxide deposition. For the latter, the actual thickness was 230 nm. Normalized C-V characteristics are shown in Fig. 2.13 at a measurement frequency of 500 Hz. Similar results have also been achieved at higher frequencies, such as 1 MHz, and during quasi-static measurements. Nevertheless, in all cases a shift of the C-V curve is constantly observed for increasing deposition times.

This result indicates the presence of higher boron content at the surface of the *n*-type c-Si substrate. Therefore, the boron doping density  $D_B$  [ $\text{cm}^{-2}$ ] can be derived from the flatband voltage  $V_{FB}$  shift according to the following expression:

$$\Delta V_{FB} = V_{FB}(D_B) - V_{FB}(D_B = 0) = \frac{qD_B}{C_{\text{OX}}} \quad (2.1)$$

where  $C_{\text{OX}}$  is the oxide capacitance per unit area. However, the presence of a positive oxide charge density  $D_{\text{OX}}$  can shift the  $V_{FB}$  in the opposite direction. This effect is particularly visible in the C-V curve of a 1 min B-doped sample where the flatband voltage has been found to be  $-1.2$  V. In fact, by neglecting the influence on  $V_{FB}$  of the boron doping, the measured curve could be interpreted as an enhancement-type *p*-MOS structure ( $D_B = 0$ ) with  $D_{\text{OX}} = 9.25 \times 10^{10} \text{ cm}^{-2}$ , as shown in Fig. 2.13. Therefore, this device has been used as flatband voltage reference, i.e.  $V_{FB}(D_B = 0)$ . Under the assumption of similar  $D_{\text{OX}}$  in all other samples, the relative boron doping densities have been calculated as a function of the exposure time according to Eq. 2.1,

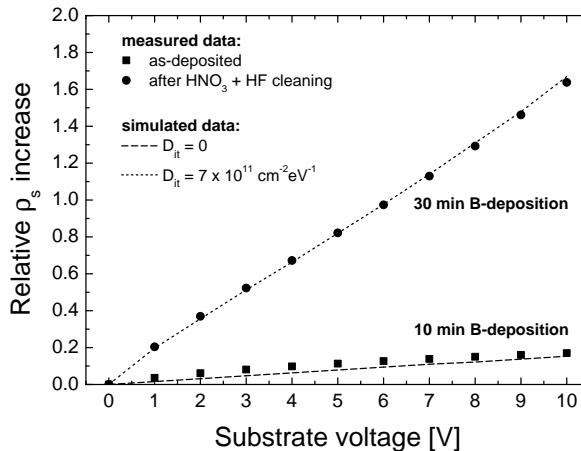


**Figure 2.14:** (Left y-axis) Boron doping density as a function of  $\text{B}_2\text{H}_6$  exposure time at  $700^\circ\text{C}$  determined from the flatband voltage shift at  $C_{FB}/C_{OX} = 0.855$  of the C-V characteristics for three different measurement frequency conditions. For comparison, the simulation results of boron diffusion at  $700^\circ\text{C}$  with a surface source are also displayed for either as-diffused profiles or after removal of a 1 nm surface Si layer. (Right y-axis) The simulated time dependence of the as-diffused B-doped junction depths for an  $n$ -type substrate doping level of  $10^{15} \text{ cm}^{-3}$ .

and they are plotted in Fig. 2.14 for various measurement frequencies. In comparison, simulation results of boron diffusion at  $700^\circ\text{C}$  are also reported for either as-diffused profiles or after removal of a 1 nm Si surface layer, which would be a plausible effect of the cleaning sequence.

Both diffusion and Si etching simulations were performed with Taurus TSUPREM-4<sup>TM</sup> [41]. In particular, a diffusion process can be modeled when the concentration of one or more impurities in the ambient gas is specified at the surface of the structure. In our case, the growing B-layer acts as the source of boron for the adjacent bulk silicon [13]. Therefore, the dopant surface concentration was varied during the simulated diffusion cycle according to the time dependence of the B-layer peak concentration as determined by the SIMS results shown in Fig. 2.7. Diffusion temperature and time were then defined as the experimental  $\text{B}_2\text{H}_6$  exposure conditions. The diffusion equations and the activation of boron impurities were solved by using the most comprehensive models available with the default material parameters. Besides information on the diffused profile, such as boron dose and junction depth (see Fig. 2.14), the software is also able to extract electrical characteristics, as demonstrated by the simulated high-frequency capacitance-voltage curve in Fig. 2.13 for the enhancement-type MOS structure.

The time dependence of the measured boron densities is in good agreement with the 0.5 grading coefficient of the simulated doping process, although for short exposures the B-layer removal might also slightly reduce the amount of active boron atoms incorporated at the c-Si surface. The C-V method thus overcomes the limitation of



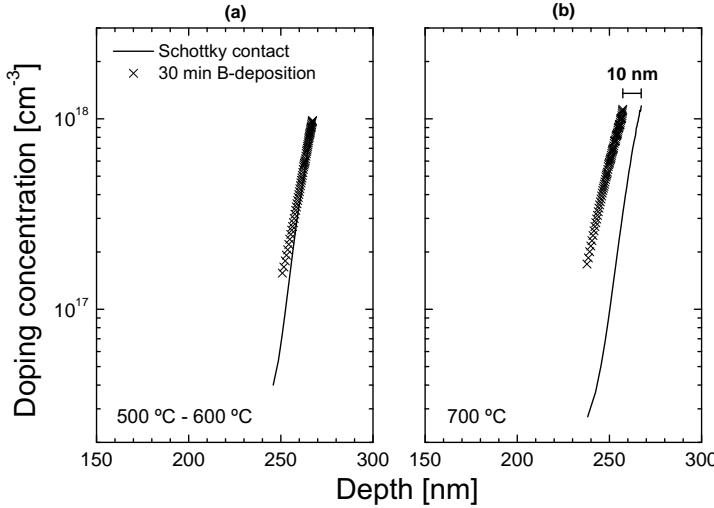
**Figure 2.15:** Relative increase of the sheet-resistance with respect to the sheet-resistance at 0 V reverse biasing as a function of the substrate bias for either a 10 min as-deposited B-layer or a 30 min B-doped sample after standard cleaning and HF dipping. Simulation results are also reported for a boron doping profile formed during boron diffusion at 700 °C for equivalent exposure times. The influence of oxide charges has been taken into account for the latter sample.

sheet-resistance measurements, since boron doping is also revealed to be present for deposition times less than 5 min. In fact, oxide charges in combination with interface trapped charges can readily deplete or even invert such ultrashallow  $p^+$ -doped region.

An attempt to extract the interface trapped charge density  $D_{it}$  has also been made by using a conventional method proposed in [52] based on the comparison of C-V measurements at 1 MHz and in quasi-static conditions. The calculated  $D_{it}$  show a similar 0.5 grading coefficient in the  $B_2H_6$  exposure dependence. In particular, an interface trapped charge density of  $7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  has been determined for a 30 min B-doped sample. Although the  $D_{it}$  level would also introduce a slight correction in the B doses, as seen for oxide charges, their effect is more evident on the sheet-resistance measurements shown in Fig. 2.15 as a function of the substrate voltage. In fact, the presence of the  $\alpha$ -B layer formed after 10 min deposition can screen any influence of the oxide charge, and thus the relative increase is in agreement with simulated  $p^+n$  junction depletion spreading in an equivalent boron-diffused region. On the other hand, after the removal of the  $\alpha$ -B film, the sheet-resistance of a 30 min B-doped sample will experience a more rapid increase due to charge-induced depletion at the Si surface. The latter effect is even more severe for samples with shorter exposures treated with the cleaning sequence.

### 2.4.3 Capacitance-voltage profiling

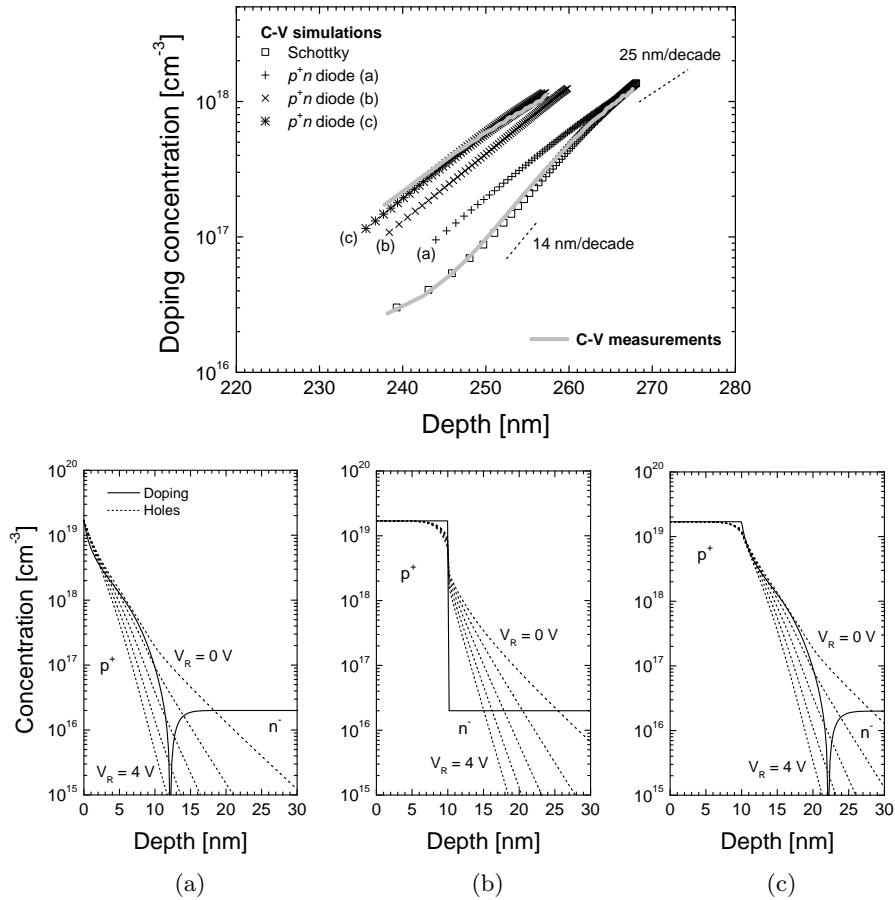
In order to confirm that the B-deposition process is suitable for fabrication of nm-deep junctions, the diffusion of boron atoms into the c-Si substrate has been deter-



**Figure 2.16:** C-V doping profiles of the abrupt  $n^+$  buried layer measured by using at the surface either a Schottky contact or a B-layer. The boron deposition has been performed for 30 min at temperatures of (a) 500 °C and 600 °C, (b) 700 °C.

mined with an in-house capacitance-voltage profiling technique that uses the abrupt  $n^+$  buried layer of the  $n^-$ - $p^-$ - $n^+$  epi-stack to profile the tail of B-doped junctions at the wafer surface [53]. The  $B_2H_6$  exposure has been carried out at temperatures ranging from 500 °C to 700 °C. In Fig. 2.16 the profile of the  $n^+$  buried layer obtained from a Schottky contact is compared to that of the  $p^+$ - $n^-$ - $p^-$ - $n^+$  structure with a 30 min B-deposition at the surface. For both 500 °C and 600 °C exposures, the two curves essentially coincide, which suggests that a  $p^+$ -like layer is formed without any significant diffusion of dopant atoms. For the 700 °C deposition, the 10 nm difference in the position of the two curves verifies that the junction depth remains limited even after prolonged deposition times. In comparison, a similar 700 °C thermal treatment for a 5 keV  $BF_2^+$  implantation of  $1 \times 10^{15} \text{ cm}^{-2}$  will result in a diffused junction profile approximately six times deeper and much less steep [53, 54].

Device simulations of the C-V profiling technique have been also performed, and the results are shown in Fig. 2.17. The profile of the  $n^+$  buried layer from the  $n^-$ - $p^-$ - $n^+$  structure with a Schottky contact is coincident with the experimental curve. On the other hand, for the  $p^+$ - $n^-$ - $p^-$ - $n^+$  device, the influence of the boron deposition has been first investigated by assuming the  $p^+$ -doped junction to be formed only from a 30 min boron diffusion at 700 °C. The B surface source has been varied accordingly with the SIMS data. The resulting B profile is shown in Fig. 2.17(a) along with the majority carrier distribution for different reverse biasing voltages. Thus, the hole distribution rather than the actual doping affects the extraction of the  $n^+$ -profile mainly for impurity concentrations as low as  $10^{17} \text{ cm}^{-3}$ , where the characteristic length of the majority carriers (6–9 nm/decade) is comparable to the slope of the buried layer



**Figure 2.17:** (Top) Simulation and measurement results of the C-V profiling technique. (Bottom) The influence of a 30 min  $\text{B}_2\text{H}_6$  CVD process at  $700^\circ\text{C}$  has been simulated by assuming the  $p^+$ -doped region to be formed by: (a) thermal diffusion of boron with surface source in accordance with SIMS data, (b) 10 nm deep uniform B-doped layer, and (c) combination of profile (a) and (b).

(14 nm/decade). Instead, at higher reverse biasing voltages the abruptness of the hole profile will be determined by the Debye length of 1 nm corresponding to the boron peak concentration of  $1.7 \times 10^{19} \text{ cm}^{-3}$ , i.e. the solid solubility limit, and thus the C-V technique will reconstruct the less steep buried layer gradient ( $\sim 25 \text{ nm/decade}$ ). On the other hand, the experimental profile can be reconstructed by combining the effect of the as-diffused B profile with a 10 nm-deep uniform B-doped region (see Fig. 2.17(c)). The latter could be attributed to both silicon consumption during *in-situ* pre-bake cleaning and growth of a boron-silicide layer, since only use of the profile in Fig. 2.17(b) would still not completely describe the measured curve.

## 2.5 Conclusions

It has been demonstrated that the growth of boron layers on (100) Si substrates during diborane ( $B_2H_6$ ) exposure in a chemical vapor deposition reactor can be performed such that high selectivity, excellent isotropy and uniform coverage can be achieved for any surface topography and patterning. The thermal dissociation of  $B_2H_6$  at high gas flow rates forms a reproducible and high-quality electrically active  $p^+$ -like layer, the composition of which varies from a pure boron doping phase to a boron-silicon compound for increasing temperatures. Either the deposited or diffused B atoms can be quantitatively controlled by varying the exposure time, while temperatures below 700 °C can ensure an extremely limited junction depth even after prolonged deposition times.

# Chapter 3

## B-layers studied in $p^+n$ diode configurations

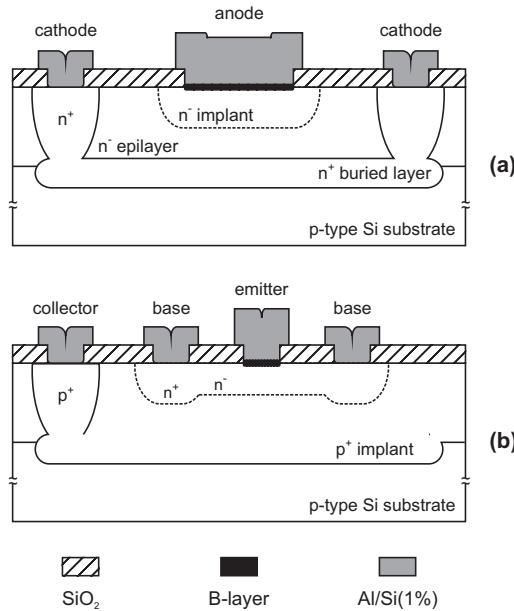
The  $p^+$ -like behavior of the B-layers can be further exploited in Si-based devices. Thus, the electrical properties have been studied here by fabricating and characterizing ohmic contacts, diodes, and bipolar  $pnp$  structures under different  $B_2H_6$  exposure conditions. In addition, the compatibility of the doping technique with the standard Si device manufacturing is also discussed with respect to the use of hard-mask materials to selectively form B-layers in contact openings, the integration of the CVD process in non-planar device schemes, and the use of pure aluminum metallization.

### 3.1 Device fabrication

Schematic cross-sections of a diode and a bipolar  $pnp$  structure are shown in Fig. 3.1. The substrates were 2–5  $\Omega\text{cm}$   $p$ -type (100) Si wafers. The diodes were placed in an  $n$ -type region consisting of a 0.9  $\mu\text{m}$  epitaxial layer, doped to  $10^{16} \text{ cm}^{-3}$ , grown on an  $n^+$  buried layer that was contacted by implanted  $n^+$  plugs. Kelvin test structures for measurement of the contact resistance of the Al/Si(1%) on the as-deposited B-layers were implemented by creating a  $p^+$  diffusion tap in the low-doped  $n$ -type epilayer with both a deep and shallow  $B^+$  implantation of  $5 \times 10^{15} \text{ cm}^{-2}$  at 180 keV and 15 keV, respectively, [55].

For the integration of  $pnp$  bipolar structures, a deep  $B^+$  implantation of  $10^{13} \text{ cm}^{-2}$  at 400 keV was used to increase the  $p$ -type doping of the substrate that functions as collector. Then,  $P^+$  implantations of  $10^{12} \text{ cm}^{-2}$  and  $1.5 \times 10^{12} \text{ cm}^{-2}$  at 40 keV and 180 keV, respectively, were performed with the goal of both increasing the epilayer doping of the diodes and creating a region comparable to that of the base of conventional fully-implanted  $pnp$  bipolar transistors. To achieve a non-critical, i.e. large, width of this base region, the peak concentration of about  $10^{17} \text{ cm}^{-3}$  was chosen. The base and collector implants were activated by a 1 min anneal at 1050 °C.

Thereafter, a 300 nm LPCVD TEOS oxide isolation layer was deposited onto 30



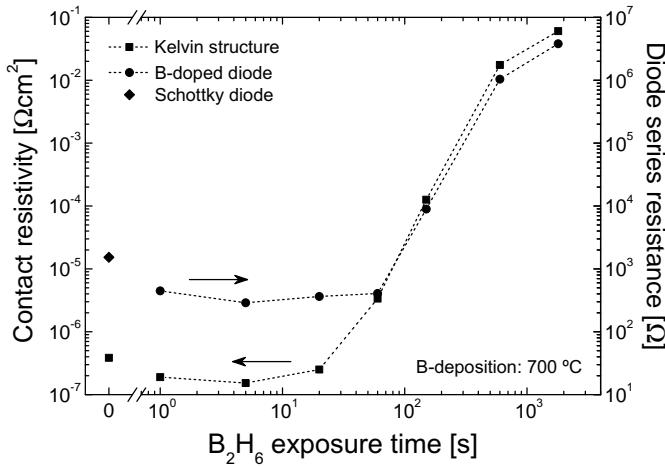
**Figure 3.1:** Schematic cross-sections of fabricated devices: (a)  $p^+n$  diode, and (b) vertical  $pnp$  bipolar transistor.

nm thermal  $\text{SiO}_2$ . Contact openings to be treated with B-deposition were plasma etched with soft landing on the Si. The B-layers were deposited at either 500 °C or 700 °C for various exposure times and metallized by an Al/Si(1%) physical vapor deposited (PVD) layer. Contacts to other device regions were then also opened and metallized by a second layer of PVD Al/Si(1%). After metal patterning, a 400 °C alloy step in forming gas was performed.

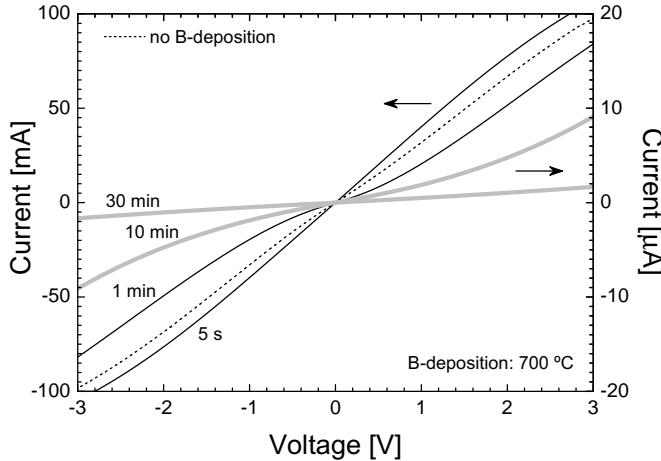
To further examine the dependence of the B-layer growth on processing parameters, such as temperature, ambient pressure, and diborane flow rate for min-long exposures, i.e. when significant boron segregation occurs, as well as the IC processing compatibility of the doping technique, the electrical characterization has been performed on more simple device structures. Thus, for the experiments reported in Sections 3.3.2–3.3.6, B-depositions were carried out directly into contact windows that were wet-etched through 750 nm  $\text{SiO}_2$  thermally grown on  $n$ -type 2–5 Ωcm Si substrates.

## 3.2 Ohmic contacts

The measured contact resistivity, defined at zero biasing voltage, is shown in Fig. 3.2 as a function of  $\text{B}_2\text{H}_6$  exposure time at 700 °C along with that of a contact processed without B-deposition, i.e. zero exposure time. For finite exposure times, the contact resistivity first drops when going from 1 s to 5 s and then increases to reach

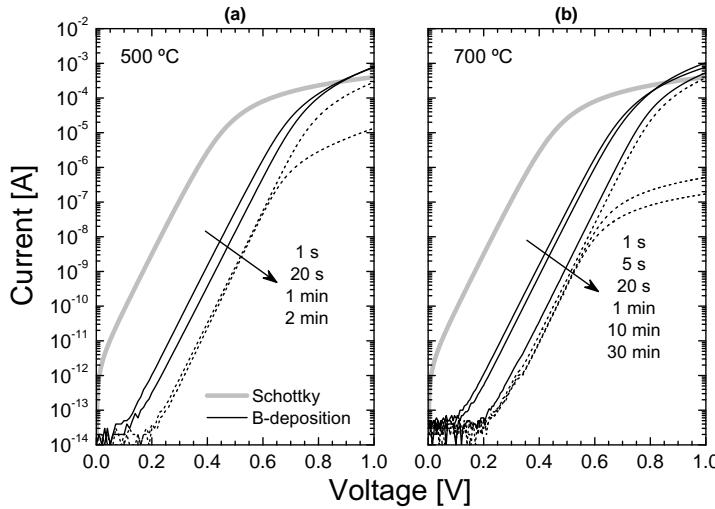


**Figure 3.2:** (Left y-axis) Contact resistivity as a function of  $\text{B}_2\text{H}_6$  exposure time at  $700^\circ\text{C}$  measured by using Kelvin test structures with a contact size of  $2 \times 2 \mu\text{m}^2$ . For comparison, the contact resistance of the  $\text{Al}/\text{Si}(1\%)$  metallization directly on the diffusion  $p^+$  tap is shown, i.e. 0 s exposure time. (Right y-axis) The series resistance at high forward voltages of  $1 \times 1 \mu\text{m}^2$  diodes is shown for an  $\text{Al}/\text{Si}(1\%)$  Schottky-junction and B-deposited devices.



**Figure 3.3:** I-V characteristics of resistors formed by a  $p^+$  diffusion tap contacted through B-treated windows of  $2 \times 2 \mu\text{m}^2$  size. The x-axis refers to the actual applied voltage between the two terminals.

higher values for minute long depositions. This indicates that the short-time exposure can either change the surface conditions to reduce the Fermi level pinning [56] or actually increase the surface  $p^+$  doping in the contact window. On the other hand,



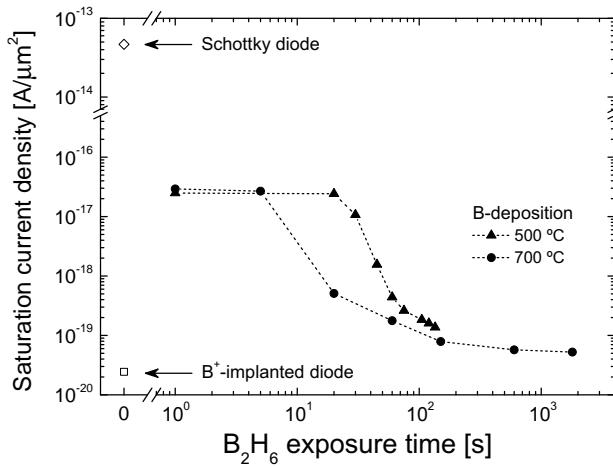
**Figure 3.4:** I-V characteristics of as-deposited B-diodes formed for various  $B_2H_6$  exposure times at (a)  $500\text{ }^\circ\text{C}$  and (b)  $700\text{ }^\circ\text{C}$ . The anode area is  $2 \times 1 \mu\text{m}^2$ . A structure is used with an  $n^+$  buried layer and a surface doping of  $\sim 10^{17} \text{ cm}^{-3}$ . For comparison, the I-V curve of an Al/Si(1%) Schottky diode is also included.

when B atoms start to significantly segregate in the amorphous phase, such as for a 10 min exposure time, the contact behaves as a high-ohmic tunneling layer, in accordance with the fact that the layer is only nanometers thin. From the measured contact resistivity and the thickness of the B-layer determined by HRTEM images, it can be concluded that the film has a resistivity in the order of  $10^4 \Omega\text{cm}$ . This value is in the resistivity range of  $10^3\text{--}10^5 \Omega\text{cm}$  reported in literature for various  $\alpha$ -B layers [57], while boron-silicon compounds would be characterized by higher conductivity [50]. For a 30 min deposition the contact resistance is increased by a factor of  $\sim 3$  as compared to that obtained with a 10 min  $B_2H_6$  exposure. This is in good agreement with the linear time dependence of the film growth. By exploiting this property, the B-layer filled contact windows could be used as very compact, small area, non-linear resistors, as demonstrated in Fig. 3.3.

### 3.3 $p^+n$ junction diodes

#### 3.3.1 Exposure time dependence

In References [1,3] it was found that even for a B coverage below one monolayer, the presence of boron atoms on an  $n$ -type (100) silicon surface will significantly affect the position of the corresponding Fermi level  $E_F$  at the interface. In particular, Yu *et al.* showed that, as the  $B_2H_6$  exposure is commenced, the Fermi level is rapidly shifted towards the valence band, as one would expect for electrically active  $p$ -type dopants.



**Figure 3.5:** Saturation current density as a function of  $B_2H_6$  exposure time extracted from I-V characteristics of diodes formed with B-deposition at either  $500\text{ }^\circ\text{C}$  or  $700\text{ }^\circ\text{C}$ . For comparison, data of  $\text{Al}/\text{Si}(1\%)$  Schottky and deep  $p^+$  $n$ -junction diodes are also shown.

This effect is confirmed by the I-V characteristics shown in Fig. 3.4 for B-deposited diodes processed at either  $500\text{ }^\circ\text{C}$  or  $700\text{ }^\circ\text{C}$  in comparison to an  $\text{Al}/\text{Si}(1\%)$  Schottky contact directly onto the substrate. First, it should be noted that all diodes exhibit near-ideal behavior with ideality factors lower than  $\sim 1.02$ , thus confirming that the B-layer fabrication does not introduce any defects that cause significant leakage currents. Secondly, already after 1 s  $B_2H_6$  exposure a noteworthy current reduction is observed with respect to the Schottky-diode situation. However, at such an early stage of the CVD process, the deposition temperature does not appear to be a critical parameter. This would be in agreement with the proposition made by [1] that the interaction between boron and low-density donor surface states is mainly responsible for the rapid band bending. In particular, the maximum  $E_F$  shift as determined by X-ray photoelectron spectroscopy (XPS) was observed for a surface boron density of  $2 \times 10^{14}\text{ cm}^{-2}$  at an exposure temperature of  $650\text{ }^\circ\text{C}$ , and any further influence could not be detected, although the boron adsorption was limited to less than a monolayer. Nevertheless, our experiments indicate that formation of a distinct  $\alpha$ -B layer, which occurs for min-long exposures, is an effective way to further the current lowering. In this respect, the higher deposition temperatures are more efficient, in that it promotes a faster and spatially more homogeneous film growth.

In Fig. 3.5 the extracted saturation current density is shown as a function of the  $B_2H_6$  exposure time at deposition temperatures of  $500\text{ }^\circ\text{C}$  and  $700\text{ }^\circ\text{C}$ . The doping gas conditions in the latter case induce a B coverage of  $4.22 \times 10^{14}\text{ cm}^{-2}$  within 5 s, and in this time span the current level hardly changes, which is in agreement with the results reported in [1]. However, after 20 s the segregation of B atoms starts, and the saturation current is significantly reduced. Then the continued increase of

the surface boron density progressively lowers the current level, which asymptotically approaches a value typical of deep  $p^+n$ -junction diodes. Similar behavior can be observed for diodes processed at 500 °C, although the lower temperature delays the boron coverage and the corresponding effect on the I-V characteristics. Therefore, we can assume that the saturation current will be mainly dominated by the hole injection from the  $p^+$  region into the  $n$ -substrate as governed by the Gummel number of this region. The high level of electron injection, which dominates the current in the Schottky diode counterpart, is suppressed even though the actual  $p^+$ -junction is only a few nanometers deep. This is confirmed by the comparison with the I-V performance of a 0.7  $\mu\text{m}$  deep junction that was fabricated with a 20 min thermal anneal at 950 °C of a B<sup>+</sup> implant at 15 keV to a dose of  $3 \times 10^{15} \text{ cm}^{-2}$ . The saturation current density of the 10 min deposition is only 2.3 times higher than that of the annealed B-implanted device.

The B-layer deposition, however, influences the I-V characteristics at high forward voltages in a less favorable way. In particular, Fig. 3.2 shows the extracted series resistance of a  $1 \times 1 \mu\text{m}^2$  diode as a function of B<sub>2</sub>H<sub>6</sub> exposure time at 700 °C. Similarly to the contact resistance, a beneficial effect on the high-current levels is seen during the first stage of the deposition that in conjunction with the saturation current lowering results in a reduction of the series resistance, and a minimum is reached for 5 s. Afterwards, the current at high forward biasing starts to be significantly attenuated, and the series resistance will be dominated by the high resistivity value of the growing  $\alpha$ -B layer.

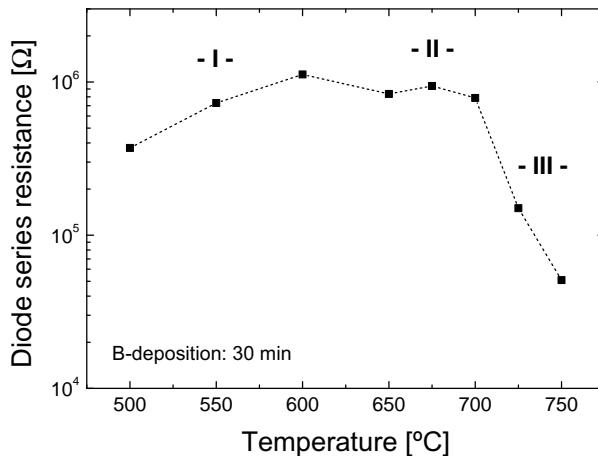
### 3.3.2 Temperature dependence

In Fig. 3.6 the diode series resistance is shown as a function of the CVD processing temperature for a  $1 \times 1 \mu\text{m}^2$  diode fabricated with a 30 min B-deposition. Three different regions can be distinguished, and they reveal a change in the growth mechanism and the layer composition, in agreement with results reported in [9].

In fact, at temperatures lower than 650 °C, a pure boron layer is expected to be formed by thermal decomposition of diborane, which is enhanced for increasing temperatures. Indeed, the measured series resistance confirms the presence of a high-ohmic B-film. In addition, the positive temperature coefficient suggests that the deposition of boron atoms on the silicon surface is more efficient as the temperature increases. This can be also explained by an increase of hydrogen desorption from the adsorbed layer, i.e. more sites are open for further boron adsorption, [1].

The second growth regime is from about 650 °C to 700 °C and characterized by a slightly lower series resistance with negligible temperature dependence. In this temperature regime, silicon begins to react with the segregated boron atoms on the surface. Therefore, the high-ohmic pure boron layer is partly converted into a more conductive boron-silicide region.

Finally, B<sub>2</sub>H<sub>6</sub> exposure at temperatures higher than 700 °C results in a rapid decrease of the series resistance, since the silicon-boron reaction is significantly promoted along with faster diffusion of boron atoms into the substrate, which reduces the probability of B segregating on the surface in a pure phase.



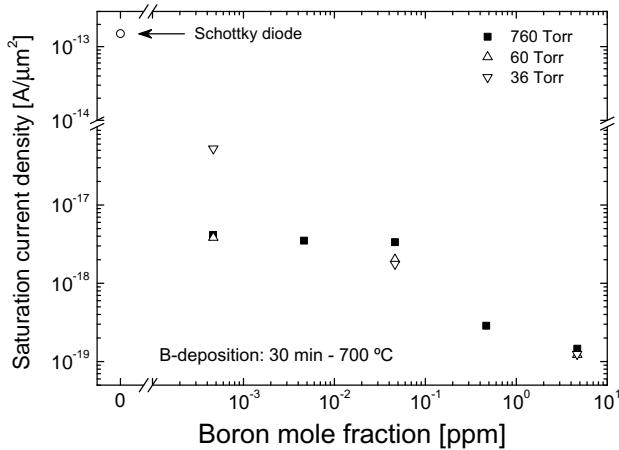
**Figure 3.6:** The diode series resistance as a function of the deposition temperature for a 30 min  $\text{B}_2\text{H}_6$  exposure. The anode size is  $1 \times 1 \mu\text{m}^2$ .

### 3.3.3 Flow rate and pressure dependence

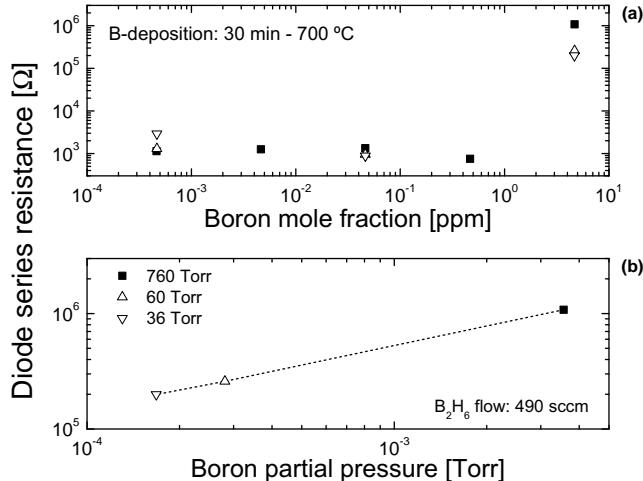
The influence of the diborane flow rate in the CVD process was investigated for three different reactor pressures, namely 760 Torr, 60 Torr, and 36 Torr, at the deposition temperature of 700 °C. For 30 min  $\text{B}_2\text{H}_6$  exposure time, diode I-V characteristics revealed that  $pn$ -junctions were formed for all the processing conditions. However, as shown in Fig. 3.7, the current levels decreased with increasing boron mole fraction, which for a given  $\text{B}_2\text{H}_6$  flow rate is defined here as the ratio between the resulting boron partial pressure and the total ambient pressure. Furthermore, the measured diode series resistance is plotted in Fig. 3.8 as a function of the dopant gas concentration. Thus, the typical high-ohmic behavior of the B-layer is achieved only for  $\text{B}_2\text{H}_6$  injection at levels as high as 490 sccm either at atmospheric or reduced pressures. On the other hand, lower gas-source flow rate does not induce any segregation of boron atoms in an amorphous phase even for long exposures such as 30 min, and the series resistance is limited by the substrate resistivity.

This dependence is similar to results reported in [11], where a change in the surface reaction kinetics was observed to occur for  $\text{B}_2\text{H}_6$  concentrations higher than 6 ppm. In fact, for lower gas-source flow the substrate was doped just as it would by conventional diffusion from a source with constant surface concentration. In contrast, for a higher gas flow an adsorbed boron layer was formed, and the surface boron concentration became dependent on the exposure time. Additionally, it is worth noting that the hydrogen carrier gas plays an important role in the sticking of boron atoms to the Si surface. Changing the carrier gas to, for example, nitrogen has been demonstrated to induce boron segregation even at lower diborane flow rate [8].

For a diborane flow rate of 490 sccm, the series resistance increases almost linearly with the boron partial pressure, as shown in Fig. 3.8(b). This is consistent with the theory of molecular gas dynamics, where the number of molecules impinging on a plane

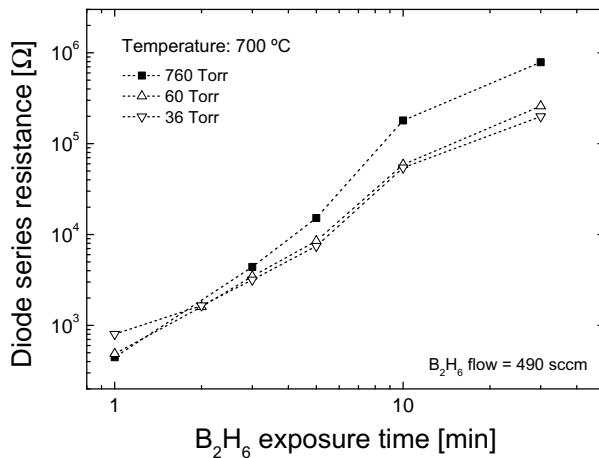


**Figure 3.7:** The diode saturation current density as a function of the boron mole fraction. The depositions have been performed at 700 °C for 30 min by varying the total pressure from 36 Torr to 760 Torr and the  $B_2H_6$  flow rate. The anode size is  $314 \times 760 \mu\text{m}^2$ .



**Figure 3.8:** The diode series resistance as a function of (a) the boron mole fraction and (b) the boron partial pressure. The anode size is  $1 \times 1 \mu\text{m}^2$ .

per unit area and time is proportional to the partial pressure of the precursor [11]. The difference between B-depositions at atmospheric and reduced pressures can be also distinguished in Fig. 3.9 for various exposure times, when the resistive component of the B-layer becomes greater than the bulk spreading resistance.



**Figure 3.9:** The diode series resistance as a function of  $B_2H_6$  exposure time at 700 °C for three ambient pressures. The anode size is  $1 \times 1 \mu\text{m}^2$ .

### 3.3.4 Masking

The most simple device structure that can be implemented relies on the selectivity of the B-deposition process by using thermal  $\text{SiO}_2$  as hard-mask material in which contact windows are formed. In addition, the relatively low CVD temperatures ( $\leq 700$  °C) prohibit any diffusion of dopant species through the field isolation layer. Nevertheless, the  $B_2H_6$  exposure has been also studied by using two different types of LPCVD materials that are generally used as isolation layers in standard IC processing, such as low-stress  $\text{SiN}$  and  $\text{TEOS}$  oxide, the latter being also used in the experiments reported above. Test structures with or without a thermal silicon oxide interface prior to deposition of such LPCVD films have been also fabricated.

The electrical characterization of diodes demonstrated the selectivity of the deposition to be still ensured regardless the type of isolation layer, despite the report of experiments indicating that a B-layer was formed on blanket  $\text{Si}_3\text{N}_4$  surfaces [9] under similar  $B_2H_6$  exposure conditions. This might be due to either different stoichiometric composition of the nitride or the metal patterning during device fabrication. The latter processing step, in fact, could have etched most likely any deposited boron film, since halogens-based chemistry for aluminum dry etching ( $\text{Br}_2$ ,  $\text{Cl}_2$ ) has a certain reactivity with boron. However, in presence of 300 nm  $\text{SiN}$  layer, either directly used as hard-mask or in stack with a 30 nm thermal  $\text{SiO}_2$ , the boron deposition appears to be significantly augmented. In fact, the diode series resistance is increased by a factor of 10, even for structures as large as  $40 \times 40 \mu\text{m}^2$ . Therefore, a thicker B-layer is expected to be formed when  $\text{SiN}$  is used as isolation material. Since the silicon nitride layers have larger hindering effect against boron diffusion [9], migration of the dopant species over the surface is presumably greater, and more boron atoms can segregate in contact openings.

### 3.3.5 Non-planar Si surfaces

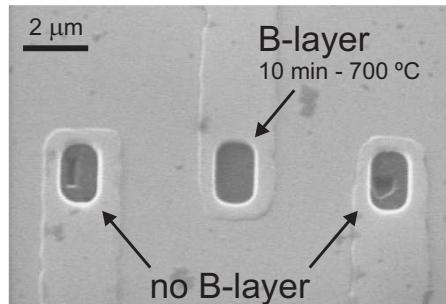
B-layers are generally deposited in contact windows formed through the field isolation layer by either anisotropic reactive ion etching (RIE) or wet HF-based etching, although the former is preferred due to better dimensional control of the resulting openings. The planar silicon surface morphology, however, is still preserved.

In order to explore the potential applications of the B-deposition in novel device schemes, the active area of the devices has been treated after oxide patterning with silicon-RIE or TMAOH etching. While the former leads Si vertical sidewalls to be also exposed to the doping gas source, tilted silicon faces are induced by the latter process. Ideal  $pn$ -junction behavior has been achieved for diodes fabricated during a 10 min B-deposition at 700 °C on surfaces either with 150 nm silicon recession or anisotropically etched in TMAOH. The absence of leakage current in the I-V characteristics confirms the results of TEM imaging, where the boron layer was found to be conformal and that perfect coverage of non-planar Si surfaces was achieved due to the isotropy of the film. Therefore, the CVD B-doping technique is also very attractive, for instance, for use in trenches and recessed-contact technologies.

### 3.3.6 Pure aluminum metallization

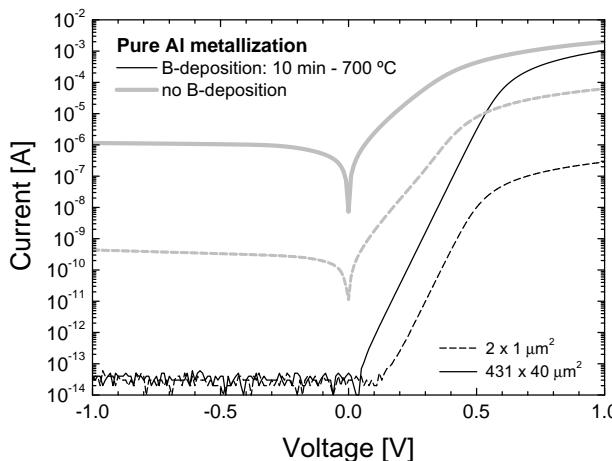
Although Al/Si(1%) is commonly used for metallization, the presence of the B-layer is here demonstrated to facilitate the integration of pure Al contacts without suffering from formation of spikes during an alloy step in forming gas at 400 °C for 20 min, which would otherwise cause the ultrashallow boron-doped junction to be shorted. This result can offer more flexibility in metal processing and device design. The B-doped diodes were fabricated by  $B_2H_6$  exposure at 700 °C for 10 min along with Schottky devices also contacted by PVD Al without standard (1%) Si pre-saturation.

First, the contact interface of Schottky and B-doped diodes has been investigated by scanning electron microscopy (SEM) after removal of the aluminum metallization with a wet-etching recipe ( $H_3PO_4:CH_3COOH:H_2O:HNO_3$ ). For those devices where



**Figure 3.10:** SEM image after Al wet-etching of  $2 \times 1 \mu m^2$  contact windows treated with and without a 10 min B-deposition at 700 °C. The contact Al metallization was followed by a 20 min alloy step in forming gas at 400 °C.

aluminum directly contacted the silicon substrate, the SEM image in Fig. 3.10 shows that the formation of spikes cannot be avoided during the thermal alloy, due to the tendency for the silicon to migrate into the aluminum. On the other hand, the surface of the contact opening treated with  $B_2H_6$  exposure prior to the Al metallization did not present any change in morphology. Therefore, the large amount of boron adsorbed on the surface forms a barrier to the silicon diffusion into the metal.



**Figure 3.11:** Typical I-V characteristics of Schottky and B-doped diodes contacted with pure Al and alloyed in forming gas at 400 °C.

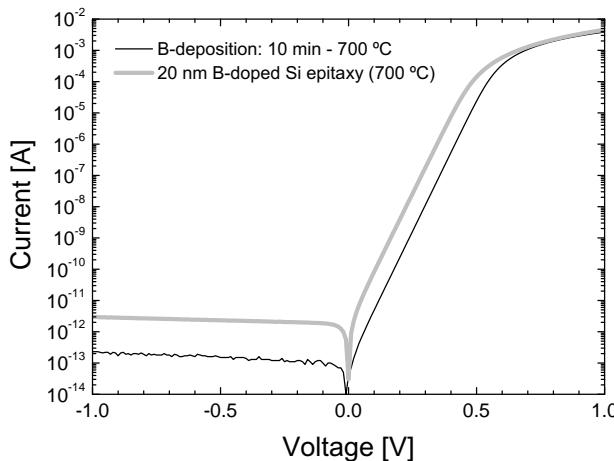
Furthermore, the absence of spikes in B-doped diodes has been confirmed by electrical measurements. In fact, the I-V characteristics reported in Fig. 3.11 present ideal behavior and current levels as in devices with conventional Al/Si(1%) metallization. This result has been also confirmed to be reproducible for either small or large area devices, where any reaction between the aluminum and the underlying silicon would have lead to higher leakage currents as measured for Schottky diodes.

However, it should be noted that the  $SiO_2$  etch geometry might play a role. In fact, higher current levels have been observed in B-doped diodes fabricated in wet-etched contact windows. Since the presence of the B-layer has been demonstrated to avoid formation of Al-induced spikes, the Schottky-like current behavior has been attributed to reduction of oxide along the  $Si/SiO_2$  interface of the contact window, which leads the metal to contact directly the Si substrate. In fact, due to the high selectivity, B cannot be deposited on the beveled  $SiO_2$  pedestal that can, however, be dissolved by Al during the 400 °C alloy step. Solutions to avoid such leakage current are offered by either peripheral  $p^+$  guard-ring diffusions or raised epitaxially grown Si regions.

### 3.3.7 Comparison of B-deposition and B-doped Si epitaxy

In order to demonstrate the superior doping efficiency respect to conventional *in-situ* boron doping during chemical vapor deposition of silicon, two sets of diodes have been fabricated at 700 °C with either a 10 min  $\text{B}_2\text{H}_6$  exposure or solely a 20 nm B-doped Si epitaxial growth. A high flow rate of the doping gas (490 sccm) has been used in both cases. The *n*-type substrate is formed by a 4  $\mu\text{m}$  thick epitaxial layer with a uniform As doping concentration of  $10^{16} \text{ cm}^{-3}$  grown on *p*-type Si wafers.

As shown in Fig. 3.12, the saturation current level for the as-deposited B-layer is one order of magnitude lower than B-doped Si film. This result confirms that I-V characteristics are determined by the segregated boron on the silicon surface, since the electrical activation of dopant atoms diffused in the c-Si substrate during the deposition process is governed by the solubility, similarly to the *in-situ* boron doping of the Si epitaxial growth.



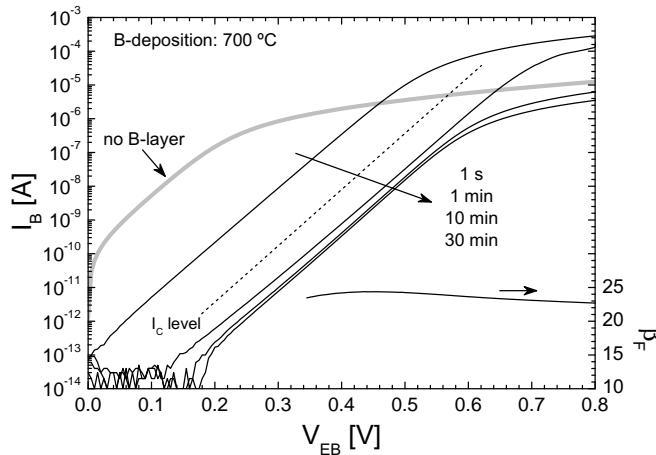
**Figure 3.12:** I-V characteristics of diodes fabricated at 700 °C with only either a 10 min B-deposition or 20 nm B-doped Si epitaxial growth. The anode area is  $760 \times 314 \mu\text{m}^2$ .

## 3.4 Emitters in $pnp$ bipolar transistors

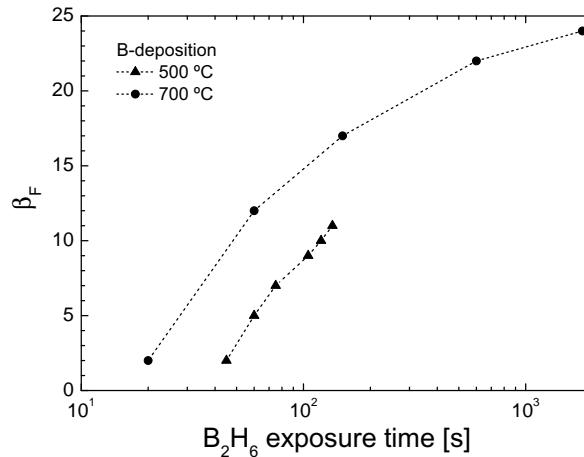
The unique feature of the B-layers being capable to tune the current level of the resulting *pn*-junction has been then further explored by incorporating the diodes discussed above in vertical *pnp* bipolar transistors, where the hole and electron currents can be measured separately. The Gummel plots of *pnp* structures fabricated at 700 °C for  $\text{B}_2\text{H}_6$  exposure times from 0 to 30 min are shown in Fig. 3.13. The indicated collector current only appears if a B-deposition has been performed, i.e. holes are then injected as minority carriers into the base. Thus the surface must be *p*-doped already

by the 1 s deposition. Moreover, the ideal behavior of the base current  $I_B$  also supports the earlier conclusion that the interactions of the deposited B with the Si do not introduce defects in the doped c-Si.

In Fig. 3.14 the maximum common-emitter current gain of *pnp*'s fabricated with emitters deposited at either 500 °C or 700 °C is shown as a function of the exposure



**Figure 3.13:** Base current of *pnp* bipolar transistors for different B-deposition times at 700 °C. The collector current level is also shown as a reference. The common-emitter current gain (right y-axis) is reported for a device formed with a 30 min  $\text{B}_2\text{H}_6$  exposure. The emitter area is  $40 \times 40 \mu\text{m}^2$ .



**Figure 3.14:** Maximum common-emitter current gain of *pnp* bipolar transistors as a function of  $\text{B}_2\text{H}_6$  exposure time for an emitter area of  $40 \times 10 \mu\text{m}^2$ . The emitter region has been fabricated with B-deposition at either 500 °C or 700 °C.

time. At 500 °C a current gain larger than unity is not obtained before 45 s of B<sub>2</sub>H<sub>6</sub> exposure. After this point,  $\beta_F$  follows the same growth rate as for the 700 °C deposited emitters, which is in accordance with the fact that the  $\alpha$ -B layer growth rate is essentially controlled by the exposure time in these experiments.

The ideal base current, i.e. the electrons injected into the emitter from the base, can be written as [58]

$$I_{n,B-E} = \frac{q n_{i0}^2}{G_E} \iint_{A_{BE,eff}} \left( e^{\frac{V_{EB}}{V_T}} - 1 \right) dx dy \quad (3.1)$$

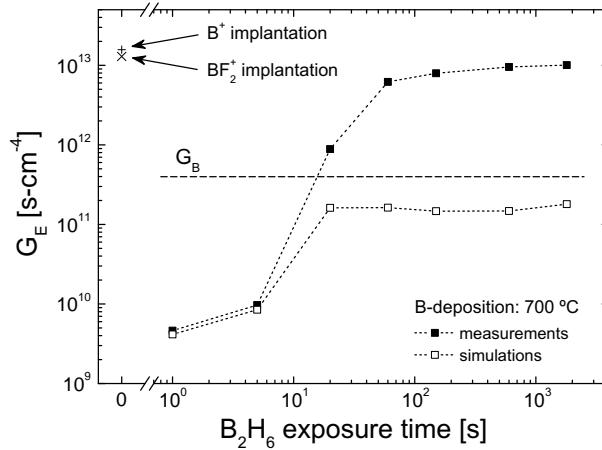
where  $V_T = kT/q$  is the thermal voltage,  $k$  the Boltzmann's constant,  $T$  the absolute temperature, and  $q$  the electron charge. The  $G_E$  is the emitter Gummel number defined as

$$G_E = \int_{W_{QNE}} \frac{N_E(z)}{D_n(z)} \frac{n_{ie}^2(z)}{n_{ie}^2(z)} dz + \left. \frac{N_E}{S_E} \frac{n_{i0}^2}{n_{ie}^2} \right|_{\text{contact}} \quad (3.2)$$

where  $W_{QNE} = W_{\alpha-B} + W_{B_xSi_y} + W_{c-Si}$  is the width of the quasi-neutral emitter region composed of the  $\alpha$ -B, B<sub>x</sub>Si<sub>y</sub>, and B-doped c-Si layer widths, namely  $W_{\alpha-B}$ ,  $W_{B_xSi_y}$ , and  $W_{c-Si}$ , respectively.  $n_{ie}(z) = n_{i0} \exp\left(\frac{\Delta E_G(z)}{2kT}\right)$  is the effective intrinsic carrier concentration,  $n_{i0}$  is the intrinsic concentration in Si,  $\Delta E_G$  is the bandgap difference with respect to Si,  $D_n$  is the electron diffusion coefficient,  $N_E$  is the active *p*-type dopant concentration, and  $S_E$  is the recombination velocity at the emitter contact.

Since the silicidation process is inhibited at temperatures as low as 500 °C [9], the similarity of the 500 °C and 700 °C curves means that the B<sub>x</sub>Si<sub>y</sub> layer cannot be contributing in any significant way to  $G_E$ . Also the contribution of the B-doped c-Si will be very low because the electron diffusion length is in the range of a micron, meaning that the  $W_{c-Si}$  of a few nm will essentially be transparent for electron injection. Therefore, the  $\alpha$ -B layer must be dominating the  $G_E$ , for example through a very low diffusion coefficient, a very low effective carrier concentration, or a very low recombination velocity at the Al contact. Since the  $\alpha$ -B is a semi-metal, it would not be expected to act as a wide bandgap material with correspondingly low  $n_{ie}$ . The fact that the  $G_E$  is increasing with  $\alpha$ -B layer thickness while  $S_E$  is constant, could therefore suggest that a very short electron diffusion length and low electron mobility are playing a role. Rudimentary calculations based on the simple two-regions model for polycrystalline emitters of [59] show that values less than 1 nm and 1 cm<sup>2</sup>/Vs, respectively, would have to be assumed to fit the results.

The importance of the  $\alpha$ -B layer thickness is underlined by the experimentally extracted  $G_E$  values that are compared to simulations of the c-Si  $G_E$  in Fig. 3.15. For the latter it is assumed that the emitter is formed only by the B-diffused junction achieved during the deposition at 700 °C. For a 30 min deposition this corresponds to a doping of  $2.4 \times 10^{12}$  cm<sup>-2</sup>, as discussed in Section 2.4.2 on page 24. While for



**Figure 3.15:** Measured Gummel number for the emitter region formed by B-deposition at 700 °C as a function of  $\text{B}_2\text{H}_6$  exposure time, in comparison to conventional  $\text{B}^+$  and  $\text{BF}_2^+$  implanted emitters. The Gummel number level for the base region is also shown. Simulated data refers to bipolar structures where the emitter region is only formed by a B-doped junction resulted from boron in-diffusion at 700 °C.

exposures below 20 s, measured and simulated data are in good agreement, the latter stagnates at very low values for prolonged B-depositions, almost 2 decades below the measured values.

It should be commented that the electron injection into the emitter might also be controlled by transport and recombination mechanisms across the B-layer/Si interface [60]. Preliminary simulations have shown that experimental results could be similarly modeled by assuming a reduction of the surface recombination velocity from  $5.0 \times 10^6 \text{ cm/s}$  to  $3.9 \times 10^5 \text{ cm/s}$  by increasing the  $\text{B}_2\text{H}_6$  exposure from 20 s to 30 min. Further investigations, however, are needed to address the physical mechanisms of this effective blocking action.

Finally, for comparison Fig. 3.15 also displays the extracted emitter Gummel number for conventional vertical *pnp* transistors, where the emitter was fabricated with either  $\text{B}^+$  or  $\text{BF}_2^+$  ion implantations at 15 keV to a dose of  $5 \times 10^{15} \text{ cm}^{-2}$  and thermally annealed at 900 °C for 20 min. The effective Gummel number for the implanted devices is only a factor 1.4–1.6 higher than a 10 min B-deposited emitter. This result is very remarkable, since a 10 min B-deposition creates a junction with a depth that is at least 50 times lower.

## 3.5 Conclusions

This Chapter reported on the electrical characterization of B-layers integrated in contacts, diodes, and bipolar structures. Deposition conditions can be chosen so as to form very low-ohmic contacts and/or ultrashallow  $p^+n$  junctions with excellent I-V

characteristics in terms of ideality and current levels. In fact, the most unique feature of these diodes is the very high effective Gummel number that can be obtained by tailoring the  $\alpha$ -B layer. This layer suppresses the electron minority carrier injection from the  $n$ -substrate so that saturation currents as low as in conventional deep  $p^+n$  junctions can be obtained. For increasing  $\alpha$ -B layer thickness the series resistance through this high-resistive layer will eventually dominate the I-V behavior. However, it is demonstrated here that conditions can be found where both an exceptionally low series resistance and saturation current can be achieved. Therefore, the B-layer can be seen as a new IC compatible material that can be both instrumental in the downscaling of bipolar heterojunction transistors (for emitters in  $pnp$ 's and TED-free base contacts) and CMOS devices (for source/drain fabrication in  $p$ -MOSFETs) and attractive for many novel Si device configurations.

# Chapter 4

## B-layers as source for dopant diffusion

Although the boron chemical concentration significantly exceeds the solid solubility at the silicon surface, for as-deposited B-layers the active dopants into the c-Si substrate have been found to be essentially limited by substitutional incorporation at the deposition temperature. However, in this Chapter the B-layer is demonstrated to act as abundant source of dopant for solid-phase diffusion during any subsequent annealing step. Previous works have also aimed to use  $\text{B}_2\text{H}_6$  exposure and thermal anneal as post-processing in order to obtain higher dopant activation and deeper junction depths. However, they generally experienced a boron desorption from the Si surface [61, 62]. In fact, their diborane exposure conditions mainly avoided or minimized the formation of a distinct layer of boron. To avoid B-desorption, an oxide capping layer was proposed to be deposited before high temperature annealing [5], but still the available B will be limited under the given deposition conditions.

In contrast, the presence of a relatively thick B-layer can offer the additional advantage of being able to minimize boron evaporation, thus reducing process complexity, while removal of the  $\alpha$ -B layer after anneal is still feasible when necessary. Amorphous boron layers, indeed, have been found to be thermally stable in the solid phase at least up to 1000 °C [1]. This has been attributed to the very low vapor-pressure, which in fact differentiates boron from other doping impurities, such as for example phosphorus [11, 63].

### 4.1 Thermal annealing

This section presents the doping efficiency that can be achieved by combining B-deposition with thermal annealing. In particular, either *in-situ* or *ex-situ* thermal processing can be performed on as-deposited B-layers. Rapid drive-in can also be carried out within the CVD reactor itself, since it provides fast ramping-up and cooling-down with rates of 20 °C/s and 4 °C/s, respectively. However, it is worth noth-

ing that for *in-situ* anneals, after  $\text{B}_2\text{H}_6$  injection is terminated, the drive-in process is still performed in a hydrogen atmosphere. This condition can favor out-diffusion of boron atoms compared to an anneal in an inert ambient. Although such an effect has been already mentioned in [62], reduction of native oxide on the surface was there addressed as responsible for the onset of B desorption. On the other hand, the study of Zhong *et al.* demonstrated that the dependence on the annealing atmosphere was not interfered by any oxide film. The occurrence of out-diffusion in hydrogen was related to the formation of boron compounds with high vapor pressures, such as boron hydrides  $\text{B}_n\text{H}_m$ , that can easily evaporate [63]. Boron hydrides, in fact, can be either adsorbed during the deposition process itself due to not complete dissociation of the dopant gas, as reported by [8], or formed subsequently by reaction with hydrogen during the annealing process.

#### 4.1.1 Thermal annealing of $\leq 1$ ML boron coverage

First, thermal anneals were applied to B-layers formed after very short  $\text{B}_2\text{H}_6$  exposures. Thus, the high temperature cycle was also limited to few seconds. Blanket (100) *n*-type Si substrates ( $2\text{--}5 \Omega\text{cm}$ ) were exposed to  $\text{B}_2\text{H}_6$  for 5 s at  $700^\circ\text{C}$ . As determined from SIMS profiles, such deposition time induces boron coverage of nearly one monolayer ( $4.22 \times 10^{14} \text{ cm}^{-2}$ ) with a concentration peak of about  $10^{21} \text{ cm}^{-3}$ . Then, an *in-situ* annealing was performed by raising the chamber temperature without injection of the dopant gas up to  $840^\circ\text{C}$  and  $1000^\circ\text{C}$  within 7 s and 15 s, respectively. Afterwards, the substrates were rapidly cooled, and test structures for either sheet-resistance or depletion-type MOS-capacitance measurements were fabricated as described in Section 2.4 on page 23. For the latter characterization technique, the devices were implemented with an actual PECVD TEOS gate oxide thickness of 530 nm.

In Table 4.1 the measured sheet-resistance of as-deposited and thermally annealed samples is shown as a function of the drive-in cycle. Furthermore, the active dopant doses have been determined from the flatband voltage shift in the C-V curves of *p*-MOS capacitors, and the values are also reported in Table 4.1. For the  $1000^\circ\text{C}$  anneal experiment a lower limit has been indicated, since the high boron doped region formed in the Si substrate prohibited the depletion/inversion regime to be observed in the MOS characteristics within the maximum measurement voltage range of  $\pm 200 \text{ V}$ .

From the extracted values we can confirm that the sheet-resistance reduction is mainly due to increase with the final annealing temperature of substitutional B doping of silicon substrate. Therefore, even for coverages of about one monolayer, the adsorbed B acts as a source of dopant. In order to study the stability of the  $\leq 1$  ML boron coverage at such high temperatures, simulations of both the B-deposition and subsequent thermal annealing process were performed by using a boron surface source extracted from SIMS data. The simulation results are also reported in Table 4.1. For the as-deposited sample, the measured value would be in agreement with a 5 Å thick B-doped Si layer with an active boron concentration peak of  $1.7 \times 10^{19} \text{ cm}^{-3}$ , i.e. the B solubility, while simulation of purely boron diffusion at  $700^\circ\text{C}$  will result in a negligible doping density ( $2 \times 10^{10} \text{ cm}^{-2}$ ). This assumption is plausible,

**Table 4.1:** Sheet-resistance and boron doping density for as-deposited and thermally annealed B-layers formed with 5 s  $\text{B}_2\text{H}_6$  exposure at 700 °C.

<i>In-situ</i> thermal anneal		Sheet-resistance [ $\Omega/\text{sq}$ ]	Active boron dose [ $\text{cm}^{-2}$ ]	
Ramp-up time [s]	Final temperature [°C]	measurement	measurement	simulation
-	-	$1.18 \times 10^5$	$8.65 \times 10^{11}$	$8.58 \times 10^{11}$
7	840	$6.79 \times 10^4$	$1.25 \times 10^{12}$	$6.46 \times 10^{12}$
15	1000	$1.12 \times 10^4$	$> 10^{13}$	$1.39 \times 10^{14}$

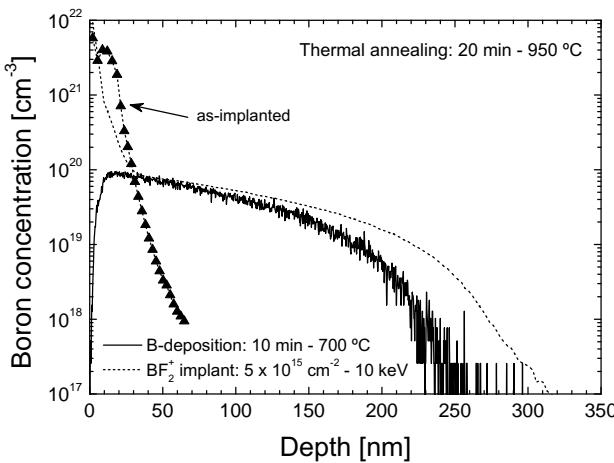
since at such an early stage of the deposition process the reaction with the first atomic Si plane play a significant role [3]. On the other hand, the deviation between simulation and measurement results for the high temperature annealing is indicative of a faster out-diffusion process. The model only accounts for the B impurity flux in the diffusion equations at the interface between ambient and exposed surface of the simulation structure. However, a boron evaporation coefficient in a hydrogen ambient was nevertheless used. This coefficient was determined in an early work on boron auto-doping during Si epitaxy [64].

#### 4.1.2 Thermal annealing of B-layers

Higher doping efficiency can be provided when nm-thick B-layers are formed prior to the thermal annealing. In particular, Fig. 4.1 shows the boron SIMS profile after a 20 min anneal at 950 °C for a 10 min B-deposited layer in comparison to a  $5 \times 10^{15} \text{ cm}^{-2}$   $\text{BF}_2^+$  implantation at 10 keV annealed under equivalent conditions. The latter shows a deeper junction, which corresponds to extra depth of the B-atoms achieved during the implantation itself. In Table 4.2 the total boron dose obtained by integrating the SIMS profile is compared to an as-deposited layer either without or with the removal of the  $\alpha$ -B phase. Thus, the 950 °C anneal has driven-in about  $8 \times 10^{14} \text{ cm}^{-2}$  boron atoms, which have been supplied by the  $\alpha$ -B layer and not only the  $\text{B}_x\text{Si}_y$  layer that contains less than  $10^{14} \text{ cm}^{-2}$  B-atoms. Nevertheless, the ample

**Table 4.2:** Boron dose of a 10 min B-layer formed at 700 °C before and after post-processing steps.

Post-processing		Dose [ $\text{cm}^{-2}$ ]
Annealing	B-layer removal	
-	-	$1.55 \times 10^{17}$
-	yes	$9.16 \times 10^{13}$
20 min - 950 °C	yes	$8.54 \times 10^{14}$



**Figure 4.1:** SIMS profile ( $O_2^+$  primary ion beam at 2 keV) of a 10 min B-layer deposited at 700 °C after a 20 min thermal annealing at 950 °C. Before the SIMS analysis, the sample has been treated with an  $HNO_3 + HF$  cleaning sequence. For comparison, the profile of a  $BF_2^+$  implantation before and after the thermal drive-in is also included.

supply of B still gives a good control of the resulting junction depth.

Furthermore, the thermal stability of a 4-nm-thick B-layer, formed after 2.5 min  $B_2H_6$  exposure at 700 °C and annealed in the CVD reactor at 850 °C for 1 min, has been confirmed by TEM analysis (see Fig. 6.3 on page 72). The film did not suffer from any change in morphology, while the sheet-resistance was already reduced by almost one order of magnitude with respect to the as-deposited sample. In Table 4.3 sheet-resistance values are listed for boron-doped junctions formed by either B-deposition or in conjunction with *in-situ* thermal annealing at 850 °C.

Thereafter, 100 min *ex-situ* thermal anneals at 1100 °C were performed on B-layers deposited at 700 °C uniformly over Si substrates for different deposition times.

**Table 4.3:** Sheet-resistance of as-deposited and thermally annealed B-layers.

B-deposition at 700 °C		Thermal annealing		Sheet-resistance
Time [min]	Temperature [°C]	Time [min]		[\mathbf{\Omega}/sq]
2.5	-	-		$1.85 \times 10^4$
2.5	850	1		$2.45 \times 10^3$
10	-	-		$1.04 \times 10^4$
10	850	1		$1.76 \times 10^3$

**Table 4.4:** Sheet-resistance of boron-doped junctions formed by *ex-situ* thermal annealing at 1100 °C of B-layers deposited at 700 °C for various B<sub>2</sub>H<sub>6</sub> exposure times.

100 min - 1100 °C	
B-deposition time [min]	Sheet-resistance [Ω/sq]
2.5	12.8
5	6.1
10	4.7
15	4.7
20	4.6
30	4.6

195 min - 1100 °C	
B-deposition time [min]	Sheet-resistance [Ω/sq]
20	3.3

A four-point probe technique was used to determine the corresponding sheet-resistance, and the measured values are reported in Table 4.4. Thus, the 1100 °C anneal experiments show that both the B-layer thickness and the corresponding boron concentration can be increased during deposition to values that make it feasible to drive-in the maximum possible doping even for long time, high temperature anneals. For example, a 5 min deposition does not supply a thick and dense enough α-B layer for reaching the minimum possible sheet-resistance, whereas the 10 min and longer depositions do. Furthermore, for a 20 min B<sub>2</sub>H<sub>6</sub> exposure, junction depth as deep as 4.9 μm were achieved after 195 min anneal at 1100 °C.

Finally, either 950 °C or 1000 °C *ex-situ* thermal anneals have been studied for B-layers formed under different deposition conditions, such as varying temperature, carrier gas, exposure time, and boron partial pressure. The samples, however, were capped with PECVD TEOS oxide to prevent desorption of boron. Here, in fact, the annealing process was primarily used as an indirect method to investigate the influence of processing parameters on the adsorption of boron on the Si surface. The measured sheet-resistances are summarized in Table 4.5.

First, in hydrogen atmosphere the B-deposition can be successfully achieved for temperatures as low as 400 °C, similarly to [7,9]. The sheet-resistance after a 950 °C thermal anneal is equivalent for all the samples, while further reduction of the deposition temperature limits the adsorption of boron and thus the available dopants for drive-in. An attempt was also made to deposit boron at 200 °C in H<sub>2</sub> atmosphere, but electrical measurements indicated that no p<sup>+</sup> region was formed.

B<sub>2</sub>H<sub>6</sub> exposure at very low temperatures was characterized in [1,4]. For instance,

**Table 4.5:** Sheet-resistance of boron-doped junctions formed by *ex-situ* thermal annealing at either 950 °C or 1000 °C of B-layers deposited at various B<sub>2</sub>H<sub>6</sub> exposure conditions.

***Ex-situ* thermal annealing: 20 min - 950 °C**

<i>B-deposition: 10 min in H<sub>2</sub> ambient</i>	
Temperature [°C]	Sheet-resistance [Ω/sq]
300	1–5 × 10 <sup>3</sup>
400	97
500	89
600	92
700	92

<i>B-deposition: 10 min in N<sub>2</sub> ambient</i>	
Temperature [°C]	Sheet-resistance [Ω/sq]
300	97
400	89
500	88
700	100

***Ex-situ* thermal annealing: 45 min - 1000 °C**

<i>B-deposition: 700 °C in H<sub>2</sub> ambient</i>	
Time [s]	Sheet-resistance [Ω/sq]
1	4–7 × 10 <sup>3</sup>
5	828
20	63
40 <sup>a</sup>	184
600	29

<sup>a</sup> For this sample the boron partial pressure was 1.65 × 10<sup>-3</sup> Torr, while all the other samples have been exposed to B<sub>2</sub>H<sub>6</sub> gas with a boron partial pressure of 3.3 × 10<sup>-3</sup> Torr.

exposure at room temperature was reported by Yu *et al.* to induce a boron coverage of  $< 5 \times 10^{13} \text{ cm}^{-2}$ . Moreover, Tillack studied B-adsorption during a 4 min  $\text{B}_2\text{H}_6$  exposure as a function of the temperature from 200 °C to 400 °C, both for low and high diborane partial pressures. In the former case, B coverage increased with temperature, although still limited to less than a monolayer. On the other hand, at high  $\text{B}_2\text{H}_6$  partial pressures, the B surface density increased from 0.2 ML to 2 ML only over the range 200–250 °C. Thereafter, B-adsorption was not dependent on temperature, and a maximum coverage of about 4–5 ML was achieved at 300–400 °C. This surface density, if capped to avoid boron desorption, would be still sufficient to form after a 20 min 950 °C anneal a B-diffused junction with a sheet-resistance of  $\leq 100 \Omega/\text{sq}$ .

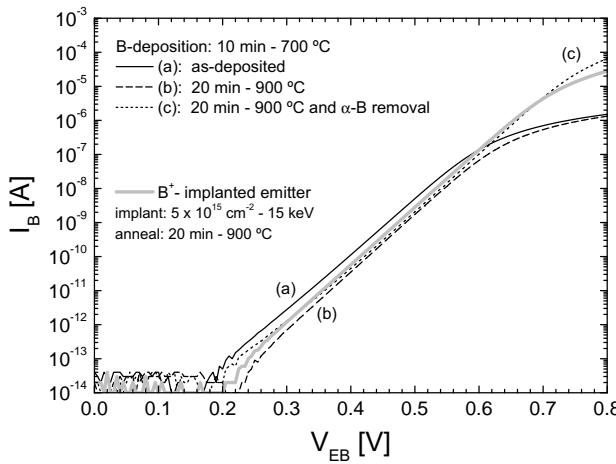
However, our experimental result for B-deposition at  $\leq 300$  °C could have been also influenced by the Si surface configuration. In fact, hydrogen termination of silicon dangling bonds obtained during the *ex-situ* and *in-situ* cleaning steps will be hardly changed at very low temperatures, since hydrogen desorption starts to occur at  $\geq 400$  °C. In addition, Kiyota *et al.* demonstrated that hydrogen termination is responsible for hindering the reactivity between B and Si atoms and thus the adsorption of boron on the surface [8]. On the other hand, as seen in Table 4.5, by using nitrogen as carrier gas during  $\text{B}_2\text{H}_6$  exposure, the B density deposited at 300 °C has the same doping efficiency of  $\text{B}_2\text{H}_6$  exposures carried out at higher temperatures. Thus, nitrogen effectively reduces the probability of hydrogen to terminate Si atoms at the surface and promotes B-adsorption.

Finally, the reduction of the sheet-resistance with the deposition time for the samples annealed at 1000 °C confirms the time dependence of the boron surface density deposited during  $\text{B}_2\text{H}_6$  exposure. However, a reduction of the boron partial pressure is not properly compensated by an increase of the exposure time by the same factor, as seen from the comparison of the 20 s and 40 s deposited samples. Therefore, although the number of molecules impinging on a plane per unit area and time is proportional to the partial pressure of the precursor, the probability for dopant species to be effectively adsorbed seems to increase at higher gas flow rates.

## 4.2 Thermally annealed B-layers in *pnp* transistors

The doping efficiency of thermal anneals has been studied also for B-layers that act as emitters in *pnp* bipolar transistors. The fabrication of the devices was identical to that reported in Section 3.1 on page 31. However, different combinations of  $\text{As}^+$  implants were used to achieve a suitable *n*-type base region for all the emitter designs, which were implemented by combining B-depositions at 700 °C with *in-situ* thermal annealing at various temperatures. A few samples with post-deposition anneals were cleaned in  $\text{HNO}_3 + \text{HF}$  prior to the metallization, so that the influence of the  $\alpha\text{-B}$  removal on the device performance could also be evaluated.

Fig. 4.2 shows the base current of a *pnp* transistor with a 10 min B-deposited emitter annealed at 900 °C for 20 min compared to either the non-annealed device or a conventional  $\text{B}^+$  implanted *pnp* structure. As discussed previously in Section 3.4 on page 42, the base current level for a 10 min as-deposited emitter is slightly higher than

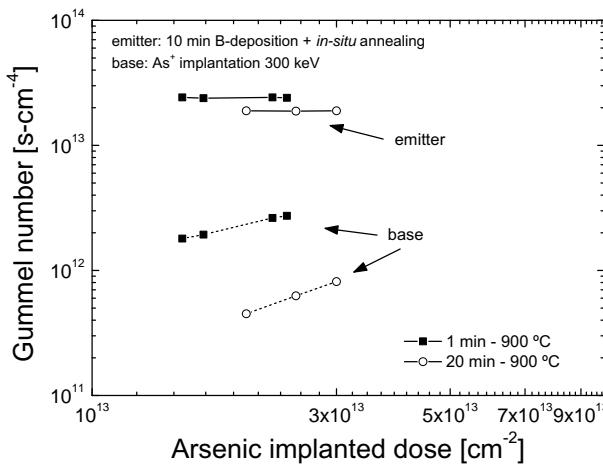


**Figure 4.2:** Base current of *pnp* bipolar transistors for different B-layer emitter designs: (a) as-deposited, (b) after 20 min thermal anneal at 900 °C, and (c) after B-layer removal on annealed samples. For comparison, the base current of a  $B^+$ -implanted emitter is also included. The emitter area is  $40 \times 10 \mu\text{m}^2$ .

for implanted emitters. However, the subsequent annealing of the B-deposited *pnp* can give an emitter that more effectively suppresses the  $I_B$  than the implanted one, even though the junction depth is lower. This may be a result of the defect-free nature of diffusion from the B-depositions. The  $\alpha$ -B layer is not playing a significant role in this respect, because removal of this layer mainly affects the high-current behavior and slightly increases the ideal  $I_B$  level. As seen in Fig. 4.2, after removal the  $I_B$  is still 25% below that of the implanted device, while the current drivability at high forward biasing is drastically improved.

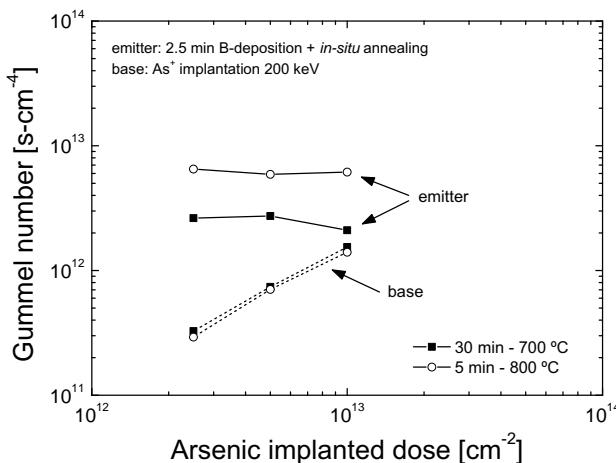
Gummel numbers for the emitter and base regions have been extracted from the measured base and collector currents, respectively, and the values are shown in Fig. 4.3 as a function of the 300 keV  $As^+$  implanted dose. Measured data for a 1 min anneal at 900 °C are also displayed. Therefore, the prolonged anneal results in lower  $G_B$ , i.e. deeper emitter junction depth, and the current gain is correspondingly increased. On the other hand, the emitter efficiency is almost equivalent between the samples, although a lower  $G_E$  for the 20 min anneal could mean a slight boron desorption even for a 10 min B-layer. Compared to as-deposited emitters (see Fig. 3.15 on page 45), the Gummel number is effectively increased by the high temperature anneal. This can be mainly ascribed to the enhanced doping activation in the quasi-neutral emitter region, i.e.  $N_E$  in the  $G_E$  expression (see Eq. 3.2 on page 44).

Thereafter, similar characterization has been applied to *pnp* structures fabricated with 2.5 min  $B_2H_6$  exposure and post-anneals either at the same deposition temperature or alternatively at 800 °C or 850 °C. The base regions were formed with  $As^+$  implants at 200 keV and 100 keV, and the measured Gummel numbers are reported in Fig. 4.4 and 4.5, respectively, as a function of the base implant dose. First, the

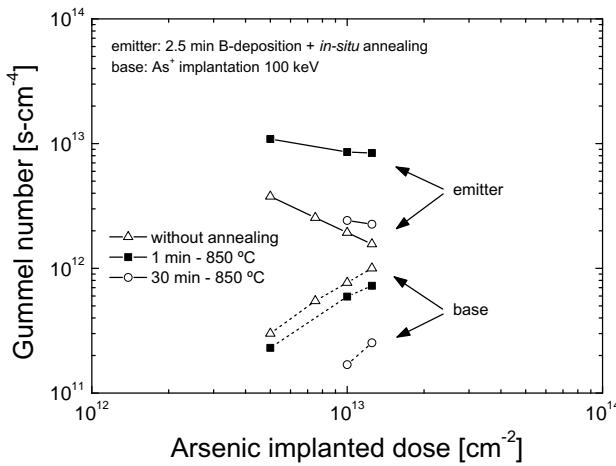


**Figure 4.3:** Gummel number of the emitter and base regions as a function of a 300 keV  $\text{As}^+$  base implantation dose. The emitters were implemented with 10 min B-layers formed at 700 °C and subsequently annealed at 900 °C.

thermal anneals performed either at 700 °C for 30 min or at 800 °C for 5 min induce similar emitter junction depths. However, the higher dopant activation at 800 °C is revealed by the increase of the emitter Gummel number by a factor of 2.5 on average with respect to the 700 °C annealed emitters. This is in good agreement with the 2.6 ratio between boron solubilities at the two annealing temperatures (after [47]:  $4.4 \times 10^{19} \text{ cm}^{-3}$  at 800 °C,  $1.7 \times 10^{19} \text{ cm}^{-3}$  at 700 °C).



**Figure 4.4:** Gummel number of the emitter and base regions as a function of a 200 keV  $\text{As}^+$  base implantation dose. The emitters were implemented with 2.5 min B-layers formed at 700 °C and subsequently annealed at either 700 °C or 800 °C.



**Figure 4.5:** Gummel number of the emitter and base regions as a function of a 100 keV  $\text{As}^+$  base implantation dose. The emitters were implemented with either only a 2.5 min as-deposited B-layers at  $700^\circ\text{C}$  or subsequently annealed at  $850^\circ\text{C}$ .

Furthermore, as shown in Fig. 4.5, during  $850^\circ\text{C}$  anneals both out-diffusion of boron atoms from the surface and drive-in of dopants into the c-Si substrate can occur for a B-layer formed during 2.5 min  $\text{B}_2\text{H}_6$  exposure, since both the emitter and base Gummel number decreases for very long annealing times, respectively. Therefore, the thermal stability of this layer is inferior to a 10 min B-layer annealed for 20 min at  $900^\circ\text{C}$ . However, a short drive-in, such as 1 min, can still provide higher emitter efficiency than in as-deposited emitters due to greater dopant activation, while desorption can be minimized. In fact, at  $850^\circ\text{C}$  the solubility is 3.8 times higher than at  $700^\circ\text{C}$  (after [47]:  $6.5 \times 10^{19} \text{ cm}^{-3}$ ), and this is in accordance with the measured  $G_E$  enhancement, which is in the range of 2.9–5.4.

### 4.3 Conclusions

This Chapter described the thermal annealing process that can be carried out after B-deposition in order to provide deeper junctions and reduced sheet-resistances. Both analytical and electrical characterization of the resulting B-doped junctions were presented. During thermal anneals the presence of the B-layer gives the advantage of acting as a capping layer that prevents B desorption and also gives an abundant supply of boron that can be diffused into the Si substrate. This approach is demonstrated to offer high doping efficiency and a good control of the resulting junction depth. In addition, thermal annealing experiments gave further insight into the B-adsorption dependence on  $\text{B}_2\text{H}_6$  exposure conditions.

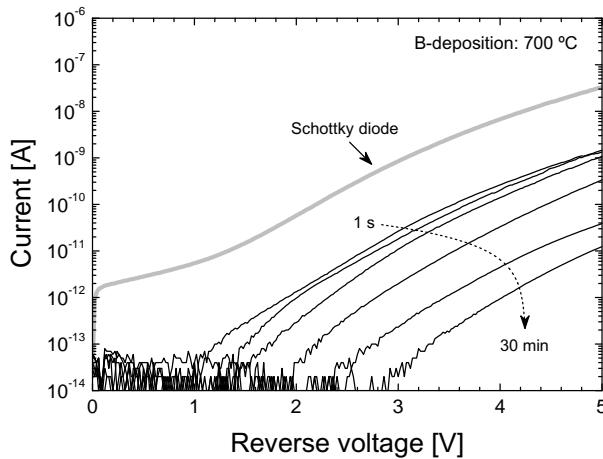
# Chapter 5

## B-layers applied to silicon-on-glass varactor technology

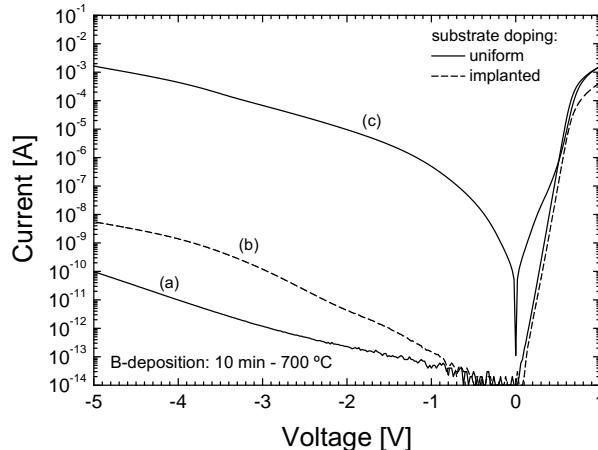
The electrical characterization presented in the previous Chapters has been focused on B-deposited diodes under operating conditions of forward biasing. Here, the performance of B-layers is investigated when reverse voltages are applied up to the expected diode breakdown limit. This is in fact important for a reliable integration of varactor and photodiode applications based on the pure B CVD process, since the devices mainly operate in the reverse biasing mode. Therefore, most of the considerations discussed below for suppressing leakage current and premature breakdown can similarly be applied to improve the I-V performance of the devices presented in Chapter 6.

### 5.1 Reverse I-V characteristics of as-deposited B-diodes

Fig. 5.1 shows the reverse I-V characteristics of as-deposited B-diodes, the forward I-V curves of which have been already reported in Chapter 3 (Fig. 3.4 on page 34). Compared to Schottky contact the current is lower, and prolonged  $\text{B}_2\text{H}_6$  exposures are instrumental in reducing the reverse current. However, a rapid increase is observed in all cases at relatively low voltages. This effect is even more accentuated when the doping level of the *n*-type substrate is increased, as shown in Fig. 5.2. In particular, non-ideal current under forward biasing is also visible for  $N_D \geq 10^{18} \text{ cm}^{-3}$ . At present, this reverse leakage current is the main issue in the electrical performance of SOG varactor devices implemented with as-deposited B-layers, since such a ‘premature breakdown’ reduces the actual operating voltage range and increases parasitic conductive components.



**Figure 5.1:** Reverse I-V characteristics of as-deposited B-diodes formed for various  $\text{B}_2\text{H}_6$  exposure times at  $700\text{ }^\circ\text{C}$ . The anode area is  $2 \times 1 \mu\text{m}^2$ . A structure is used with an  $n^+$  buried layer and a surface doping of  $\sim 10^{17} \text{ cm}^{-3}$ . For comparison, the I-V curve of an Al/Si(1%) Schottky diode is also included.

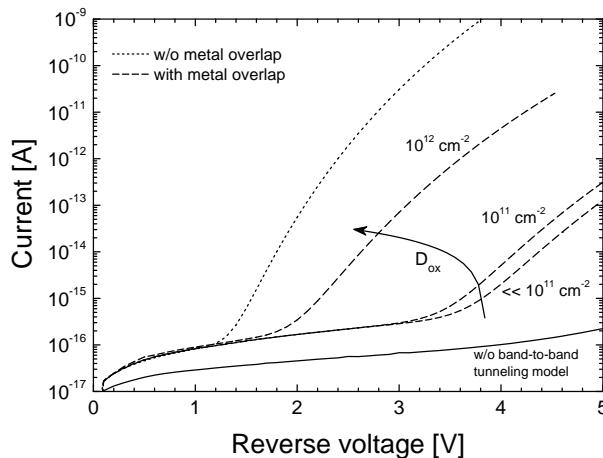


**Figure 5.2:** Reverse I-V characteristics of as-deposited B-diodes formed with 10 min B-deposition at  $700\text{ }^\circ\text{C}$  on different  $n$ -type substrates: (a) uniform profile with doping level of  $10^{16} \text{ cm}^{-3}$ , (b) implanted profile with surface doping peak of  $\sim 10^{17} \text{ cm}^{-3}$ , and (c) uniform profile with doping level of  $10^{18} \text{ cm}^{-3}$ . The anode has an annular geometry with a perimeter of  $862 \mu\text{m}$  and a width of  $10 \mu\text{m}$ .

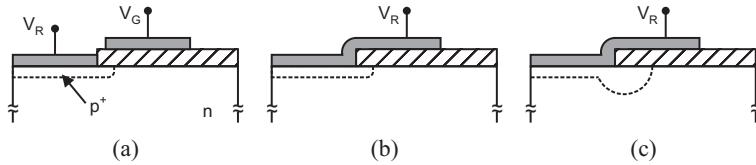
In order to determine the cause of the reverse I-V behavior, simulations were performed for a diode structure where the  $p^+$  anode region was assumed to be formed by a 10 min boron in-diffusion at  $700\text{ }^\circ\text{C}$ . The substrate doping was defined by  $\text{P}^+$

implants as for the fabricated devices of Fig. 5.1. Along with the impact ionization model, band-to-band tunneling was also included as proposed by [65]. Furthermore, the influence of the anode electrode structure and oxide charges was considered. The results are shown in Fig. 5.3. While for the applied reverse voltage range of 0–5 V only the impact ionization analysis, i.e. avalanche breakdown mechanism, would not be sufficient to describe the measured curves, the tunneling seems to be the current phenomena that governs the experimental results. This is in agreement with the criteria also mentioned in [14], where the band-to-band tunneling contribution is dominant for electric fields larger than  $7 \times 10^5$  V/cm or equivalently for breakdown voltages below  $\sim 5$  V. The extremely shallow junction curvature at the contact periphery is indeed responsible for such a high electric field. However, it should be pointed out that substrate doping above  $5 \times 10^{17}$  cm $^{-3}$  can concomitantly contribute to enhance the tunneling effect [65].

The fabricated devices are based on an ‘overlay’ anode structure, i.e. the metal electrode extends 1  $\mu$ m over the 300-nm-thick field isolation oxide. This design is known to reduce the electric field crowding at the contact rim [66]. However, simulations indicated that the onset of the band-to-band tunneling is only delayed with respect to an electrode metallization that is self-aligned to the contact openings without overlap. In fact, the curvature radius of the junction is still determining the critical electric field distribution. In addition, high density positive oxide charges can readily counteract any beneficial effect arising from the metal field plate.



**Figure 5.3:** Simulation results of reverse I-V characteristics for a diode with a  $p^+$  region formed by 10 min boron in-diffusion at 700 °C and  $n$ -type substrate formed by  $P^+$  implants as in the fabricated devices of Fig. 5.1. The anode has a circular geometry with a 1  $\mu$ m radius, and the anode metal structure is either without or with a 1  $\mu$ m overlap on the field isolation  $\text{SiO}_2$ . The influence of positive oxide charge density  $D_{\text{ox}}$  is also investigated. In all cases the impact ionization analysis is included. Dashed and dotted lines are obtained with trap-assisted and band-to-band tunneling models [65].



**Figure 5.4:** Cross-section of a  $p^+$  $n$  diode for three different implementations: (a) gate-controlled diode, (b) overlay electrode, and (c) overlay electrode with diffused  $p^+$  guard-ring.

## 5.2 Strategies for improving reverse I-V characteristics

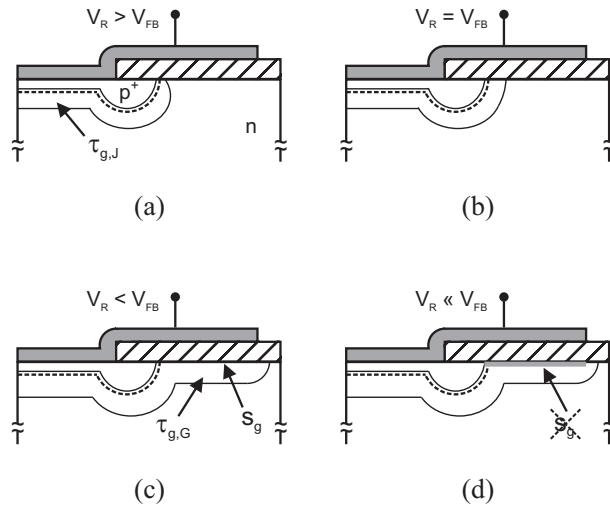
The transport mechanisms at the edge of reverse-biased B-deposited diodes have previously been demonstrated to play a significant role. In the past, many methods were developed to avoid similar edge effects on the diode I-V characteristics in terms of high leakage current and reduced breakdown voltages [66]. The proposed solutions aimed to modify the field distribution at the contact periphery of either Schottky or shallow  $pn$  diodes by using, for example, an additional gate electrode in proximity of the junction (Fig. 5.4(a)) or an ‘overlay’ electrode (Fig. 5.4(b)). A more efficient approach, however, is based on a diffused  $p^+$  guard-ring (Fig. 5.4(c)) at the contact edge. This method in conjunction with an overlay anode metallization can minimize the electric field peak by further extending the depletion region [67].

However, besides the fact that a guard-ring might be integrated in the device, the reverse current of a  $pn$ -junction is still determined by other factors. In fact, the biasing conditions of the diode change the volume of the depletion region in the edge area and under the MOS-like structure formed by the anode electrode and the  $\text{SiO}_2$  isolation layer, as shown in Fig. 5.5. Following the analysis reported in [52], four regions can be identified which contributes to the total  $pn$ -junction current: (1) the diode space-charge region (*scr*), (2) the quasi-neutral region, (3) the electrode-induced *scr*, and (4) the depleted surface under the electrode. The current components can be expressed by

$$\begin{aligned} I_1 &= \frac{qn_{i0}W_J A_J}{\tau_{g,J}} & I_2 &= \frac{qn_{i0}^2 A_J}{N_D} \sqrt{\frac{D_p}{\tau_r}} \\ I_3 &= \frac{qn_{i0}W_G A_G}{\tau_{g,G}} & I_4 &= qn_{i0}s_g A_G \end{aligned} \quad (5.1)$$

where  $W_J$  and  $A_J$  are the width and area of the depletion region corresponding to the  $pn$  diode, respectively,  $\tau_{g,J}$  the generation lifetime in the diode *scr*, and  $\tau_r$  the minority recombination lifetime in the quasi-neutral zone. Similar notation is used for the region under the ‘anode-gate’ (G) structure, which is characterized by the generation lifetime  $\tau_{g,G}$  and surface generation velocity  $s_g$ .

For an  $n$ -type substrate, reverse biasing greater than the MOS flatband voltage  $V_{FB}$  leads the surface under the gate in accumulation (Fig. 5.5(a)). This condition



**Figure 5.5:** Cross-section of a  $p^+$  $n$  diode with a guard-ring and an overlay anode structure at four different biasing conditions: (a) accumulation ( $V_R > V_{FB}$ ), (b) flat-band condition ( $V_R = V_{FB}$ ), (c) depletion ( $V_R < V_{FB}$ ), and (d) inversion ( $V_R \ll V_{FB}$ ). Solid and dashed lines indicate the depletion region edges and the junction depth, respectively.

mainly minimizes the contribution to the current arising from the surface generation. Nevertheless, persistence of this situation during reverse biasing can induce tunneling phenomena and ‘premature’ breakdown, since the field strength in the proximity of the  $p^+$ -junction edge is enhanced. In this respect, positive charges, which are always present in the oxide, can be detrimental. In fact, they shift the  $V_{FB}$  level in a less favorable way and inhibit the depletion from extending along the Si/SiO<sub>2</sub> interface. This will also cause an increase of the electric field near the  $p^+$ -junction. When the applied voltage is equal to  $V_{FB}$ , the *scr* width is the same at the surface as in the bulk (Fig. 5.5(b)), and the depletion starts to decrease the electric field distribution at the contact rim. A proper beveling of the field oxide can also contribute to spread the depletion more rapidly with the applied voltages [66]. For biasing  $< V_{FB}$ , the total reverse current is then determined by surface generation and electrode-induced *scr* currents (Fig. 5.5(c)), although the former contribution can disappear when the surface is inverted (Fig. 5.5(d)).

The generation-recombination parameters previously mentioned are also field-dependent. In fact, trap-assisted tunneling effects were reported to properly describe non-ideal diode I-V characteristics under forward and reverse biasing when the substrate doping concentration exceeded the critical value of a few times  $10^{18} \text{ cm}^{-3}$  [65]. These effects will basically govern the current level before band-to-band tunneling is initiated. A rudimentary example is given in Fig. 5.3. With respect to the conventional Shockley-Read-Hall recombination (solid line), the current at low reverse voltages is increased by including the trap-assisted tunneling model (dotted and dashed

lines) along with the band-to-band mechanism.

Based on these preliminary considerations, the reverse I-V characteristics of varactors and photodiodes will rely on the quality of the epitaxial *n*-type Si growth, i.e.  $\tau_{g,J}$  and  $\tau_r$ . This is strongly dependent on the surface defect density of the initial Si substrate. The Si/SiO<sub>2</sub> interface properties, i.e.  $s_g$ , are generally secured by thermal oxidation, and the 400 °C alloy step in forming gas can further provide hydrogen passivation of the remaining Si dangling bonds. The SiO<sub>2</sub> growth in conjunction with extra-processing, such as implantations, in the vicinity of the diode area can also alter the bulk generation lifetime underneath the electrode, i.e.  $\tau_{g,J} \longrightarrow \tau_{g,G}$ .

Moreover, for varactor diodes the ‘current generation’ volume can readily extend to the edge of the Si island, since the anode metallization completely covers the trenches (Fig. 5.6). Here, the crystal damage due to Si reactive ion etching can cause the leakage current to increase. On the other hand, photodiodes can experience a large extension of the total depletion region due to the very lightly doped substrates and surface oxide charge instabilities. Therefore, an *n*-type implantation is proposed to laterally confine the space-charge region.

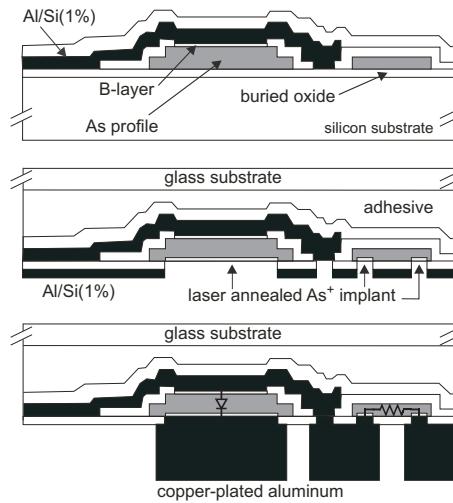
Finally, on the design level, varactor devices are generally of large squared geometry, and the edge effects can be intensified by the electric field distribution at the corners [14]. Therefore, future layouts could be either implemented with circular structures or square anode contacts with rounded corners. In the latter case, the lateral radius of the window curvature should be larger than the depletion-layer width at breakdown of an ideal parallel plane junction, in order to effectively profit from the higher cylindrical junction breakdown voltage [68].

### 5.3 Silicon-on-glass varactor technology

This section illustrates the silicon-on-glass technology for three varactor doping profile implementations, namely uniform and  $1/x^2$  arsenic profiles for either high or low control voltages [24, 69]. The cross-section of the device is shown in Fig. 5.6. Examples of the As epi-grown profiles are given in Fig. 5.7, as determined from capacitance-voltage measurements. The excellent agreement with the desired doping confirms the fine control of As incorporation attained during epitaxial growth and the formation of a one-sided abrupt  $p^+$ -junction by using B-layers.

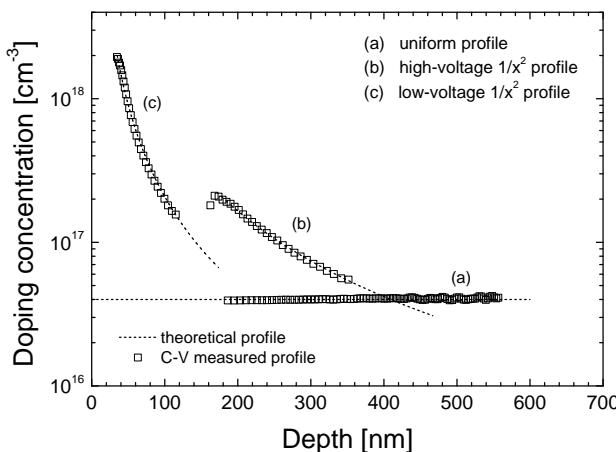
**Table 5.1:** Varactor doping profile implementations.

Profile	Sample description		Theoretical breakdown voltage [V]
	Thickness [nm]	Doping peak [cm <sup>-3</sup> ]	
Uniform	900	$4 \times 10^{16}$	23
$1/x^2$	180/820	intrinsic/ $2.1 \times 10^{17}$	20
$1/x^2$	30/200	intrinsic/ $2.1 \times 10^{18}$	7



**Figure 5.6:** Cross-section of the basic process flow for fabricating a silicon-on-glass varactor [69].

The doping distribution and the total epilayer thickness are determined by optimized designs based on a trade-off between tuning range, quality factors at zero bias, and the maximum operation reverse voltage [15, 17]. The latter is chosen to approach the breakdown value in order to benefit from the maximum feasible  $C_{max}/C_{min}$  ratio. The varactor parameters are listed in Table 5.1 along with the theoretical reverse



**Figure 5.7:** Arsenic doping profiles implemented in varactor diodes [70]: (a) uniform profile, (b)  $1/x^2$  profile for high control voltages, and (c)  $1/x^2$  profile for low control voltages. The desired As distribution is compared to the doping concentration extracted by using a capacitance-voltage profiling technique.

voltage limit of a planar *pn*-junction, as determined by device simulations with the corresponding As profile. It should be pointed out, however, that already in the ‘ideal’ case, i.e. planar junction, the low-voltage  $1/x^2$  profile is affected by band-to-band tunneling due to the high As concentration peak.

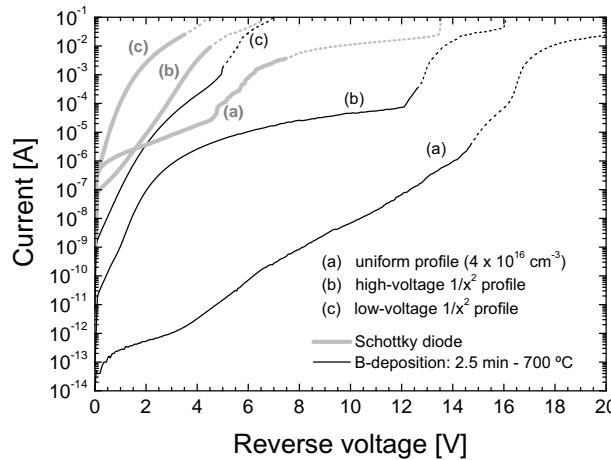
### 5.3.1 Device fabrication

SOI SOITEC wafers with  $0.34\ \mu\text{m}$  intrinsic silicon on  $0.4\ \mu\text{m}$  buried oxide (BOX) were used as starting material. The desired arsenic doping profiles were then epitaxially grown on the intrinsic silicon substrate by conventional CVD technique using the method described in [70]. Diode silicon islands were then defined by two or three shallow trenches to the BOX, depending on the total top silicon-layer thickness. Each silicon step after plasma etching is not larger than  $0.5\ \mu\text{m}$  to guarantee sufficient step coverage and a low stress level associated with the metallization layers on the front-wafer. The trench etching is also used to form high-ohmic resistors as determined by the sheet-resistance of the resulting Si region.

Guard-ring diffusions were implemented with a 5 keV  $\text{BF}_2^+$  implant to a dose of  $10^{15}\ \text{cm}^{-2}$ , while silicon trenches were treated with a 5 keV  $\text{P}^+$  implant to a dose of  $5 \times 10^{15}\ \text{cm}^{-2}$ . The activation of the dopants was carried out during a thermal oxidation at  $850\ ^\circ\text{C}$ . The resulting 30-nm-thick  $\text{SiO}_2$  can provide a high-quality Si/oxide interface and optimal electrical isolation prior to the deposition of a surface isolation layer of 600 nm LPCVD TEOS at  $700\ ^\circ\text{C}$ . It should be pointed out that the relatively low-temperature oxidation and deposition process are highly compatible with the hyper-abrupt  $1/x^2$  profiles, since the diffusivity of arsenic at temperatures  $\leq 850\ ^\circ\text{C}$  is still very low. It should also be commented that the influence on linearity due to profile deviations has shown a very reasonable fabrication window [17], namely the power law exponent can vary from  $-1.85$  to  $-2.15$ .

After anisotropic plasma etching for oxide planarization, B-layers were then formed at  $700\ ^\circ\text{C}$  directly in contact openings, which were plasma etched with soft landing on the Si, and covered by a  $0.6\ \mu\text{m}$   $\text{Al/Si}(1\%)$  PVD metallization. Schottky diodes were then also fabricated by first etching contact windows through the Al/oxide stack and subsequently sputtering a  $0.6\ \mu\text{m}$   $\text{Al/Si}(1\%)$  layer. After metal patterning, the wafer was covered with  $1\ \mu\text{m}$  PECVD oxide. Forming-gas alloying at  $400\ ^\circ\text{C}$  was performed prior to gluing the sample to a  $700\ \mu\text{m}$  glass wafer. Thereafter, the silicon substrate was removed by TMAOH etching selectively to the BOX. A 70 nm  $\text{Al/Si}(1\%)$  layer was sputtered on the back-wafer as reflective mask for laser annealing. The back-wafer contact windows were then etched through the  $\text{Al/Si}(1\%)$  and BOX. Si plasma etching was also performed in order to approach the interface between the epitaxial layer and the initial intrinsic silicon substrate. This is necessary to minimize the contribution to the series resistance from the latter.

The low-ohmic contacts to the back of the diodes and resistors were then implanted with 5 keV  $10^{15}\ \text{cm}^{-2}$   $\text{As}^+$  and laser annealed at energy of  $900\ \text{mJ}/\text{cm}^2$ . In fact, after substrate transfer to glass, only thermal processing temperatures below  $300\ ^\circ\text{C}$  are allowed to preserve the integrity of the adhesive. Therefore, excimer laser annealing is by now the only viable option for activation of the arsenic implanted con-



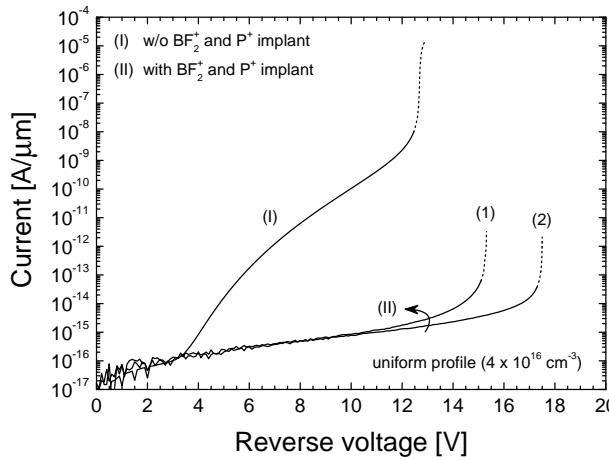
**Figure 5.8:** Reverse I-V characteristics of varactor diodes fabricated with either a 2.5 min B-deposition at 700 °C or an Al/Si(1%) Schottky contact. The corresponding As doping profiles are shown in Fig. 5.7. The anode area is  $340 \times 490 \mu\text{m}^2$ .

tacts. Next, the contact windows to the front-wafer metal were etched, and a  $1.4 \mu\text{m}$  Al/Si(1%) was sputtered and patterned on the back-wafer. Finally, a 3 h alloy step at 300 °C in forming gas was performed. Samples with a  $4 \mu\text{m}$  copper electro-plating on the Al/Si(1%) were also fabricated to further reduce the resistance of metal-tracks.

### 5.3.2 Electrical characterization

Fig. 5.8 displays the electrical results of the early SOG varactor implementations, i.e. without the use of guard-ring and channel-stop diffusions, for the three As doping profiles. Typical reverse I-V characteristics of  $340 \times 490 \mu\text{m}^2$  diodes fabricated with either a 2.5 min B-deposition or an Al/Si(1%) Schottky contact are shown. In both cases, a high electric field at the contact edges and possible low-lifetime Si regions significantly increases the losses of the varactors. The substrate doping peak in the profiles (b) and (c) might also contribute to the rapid current drift. The electrical behavior varies significantly among devices, and the dependence on the layout geometry, e.g. squared or circular anode structures, cannot be properly validated.

As one of the leakage sources, the high-current band-to-band tunneling behavior can already be predicted by simulations of the varactor structure where the anode region is assumed to be formed at 700 °C by a 2.5 min B-diffused junction. The results for a uniform  $4 \times 10^{16} \text{ cm}^{-3}$  doping profile are shown in Fig. 5.9. This graph gives also evidence of the noteworthy improvement in the reverse I-V characteristics that can be obtained by including in the varactor process the  $\text{BF}_2^+$  and  $\text{P}^+$  implants. In particular, a larger junction curvature of the diffused guard-ring is responsible for the higher breakdown voltage of the I-V curve (2) in comparison to (1). In the former case, in fact, the adopted dopant diffusion model was more accurate, and a deeper

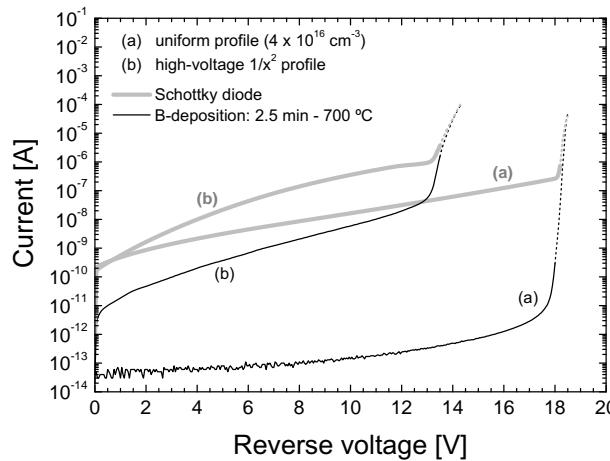


**Figure 5.9:** Simulated reverse I-V characteristics of a varactor diode with a uniform As doping profile of  $4 \times 10^{16} \text{ cm}^{-3}$ . The anode is assumed to be formed by a 2.5 min B in-diffusion at  $700^\circ\text{C}$ . The results have been obtained for different structure implementations: (I) without guard-ring and channel-stop regions, (II) with annealed  $\text{BF}_2^+$  and  $\text{P}^+$  implants, as determined by process simulations. For the latter case, curve (2) is obtained by using a more comprehensive model for dopant diffusion during the  $850^\circ\text{C}$  thermal oxidation.

junction resulted after the  $850^\circ\text{C}$  thermal oxidation.

The experimental results in Fig. 5.10 for diodes with an annular anode structure confirms that an extremely low reverse current can be restored. In addition, the actual breakdown voltage approaches the theoretical limit, which now is only reduced by the edge cylindrical geometry of the junction. Similarly, the guard-ring and channel-stop diffusions also enhance the electrical performance of the  $1/x^2$ -profile-based devices. However, the current level seems to be affected by trap-assisted tunneling, and lower breakdown voltage is achieved. In fact, simulation results predicted an I-V curve similar to the uniformly doped device up to  $\sim 16$  V.

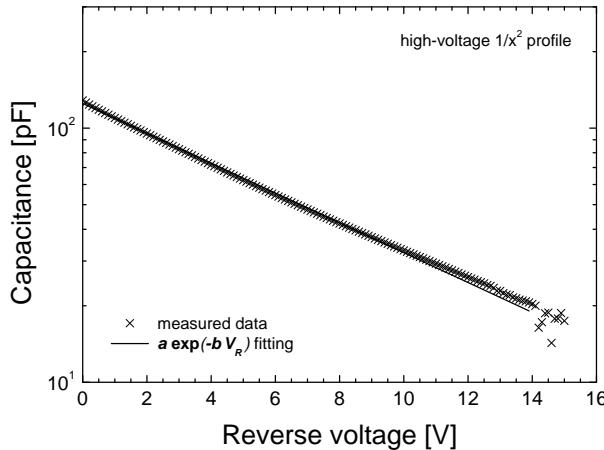
The I-V characteristics are quite reproducible over the wafer. Schottky and B-deposited diodes show the same breakdown voltage, although the  $p^+n$ -junction offers superior reverse current reduction. In these experiments, the geometry dependence is more evident. For diodes with the uniform profile, a square-shaped anode layout suffers from higher current, and the breakdown voltage is about 2 V lower than in devices with circular geometry. For the high-voltage  $1/x^2$  profile, the reduction of the maximum operating voltage is less pronounced ( $\sim 1$  V). The small guard-ring extension, which has been initially chosen to overlap the contact edge by  $0.5 \mu\text{m}$ , might also be responsible for some non-uniformities. The proximity of  $\text{BF}_2^+$  and  $\text{P}^+$  implants is also of practical importance to prevent breakdown reduction. Experimental results indicate that an acceptable situation is created for distances  $\geq 2 \mu\text{m}$ . Therefore, future varactor implementations should comply with these layout guidelines.



**Figure 5.10:** Reverse I-V characteristics of varactor diodes fabricated with either a 2.5 min B-deposition at 700 °C or an Al/Si(1%) Schottky contact. Guard-ring and channel-stop diffusions were also added to the process after the growth of the As profiles. The anode has an annular geometry with a perimeter of 862  $\mu\text{m}$  and a width of 10  $\mu\text{m}$ .

In addition, an increase of the current level and ‘premature’ breakdown have been measured for devices whose cathode contact is placed directly under the anode window. This behavior is found to be consistent over the wafer and can be plausibly attributed to: (1) the Si back-etch and (2) the  $\text{As}^+$  back-contact implantation. The sensitivity of the breakdown voltage to the latter process has been already reported in [69,71]. It was shown that residual defects in the form of interstitials injected during the implantation were detected up to 0.6  $\mu\text{m}$  away from the contact. Thus, high-tilt (60°) implants were adopted to direct the injected interstitials more away from the diode, and the tuning of the laser-anneal conditions could favor defect annealing as a consequence of the laser heating. However, the reverse current has now been reduced to such a level that further optimization of the back-wafer implantation and laser anneal is required. The Si reactive ion etching of the back-side contact prior to the  $\text{As}^+$  implant might also be responsible for higher defect density in the active device region along with the fact that it adds deep sidewalls into the Si substrate that could either reduce the actual vertical depletion extension or locally increase the electric field distribution. In this respect, a new implementation for the uniform profile will be investigated. The aim is to create a uniform doping level of  $4 \times 10^{16} \text{ cm}^{-3}$  already in the SOITEC Si substrate by successive  $\text{As}^+$  implants before the epitaxial growth. In this way, the epi-thickness to be grown can accordingly be reduced by  $\sim 300$  nm and no Si back-etch is needed.

Finally, Fig. 5.11 shows the C-V curve of a varactor with the high-voltage  $1/x^2$  profile when the  $\text{BF}_2^+$  implant is used to form the diffused guard-ring. The structure still exhibits the expected exponential capacitance variation, thus confirming the compatibility of the process modules with the hyper-abrupt As doping distribution.



**Figure 5.11:** C-V characteristic of a varactor diode implemented with the high-voltage  $1/x^2$  As profile. The anode is fabricated with a 2.5 min B-deposition at  $700\text{ }^\circ\text{C}$ , and diffused guard-rings are formed with thermally annealed  $\text{BF}_2^+$  implant. The anode area is  $340 \times 490\text{ }\mu\text{m}^2$ .

## 5.4 Conclusions

The reverse I-V characteristics of B-deposited diodes have been investigated with the aim of a reliable application of the pure boron CVD process to varactor devices in the DIMES silicon-on-glass substrate-transfer technology. In the initial implementations, although the B-deposition could ensure the theoretical tunable behavior by providing a one-sided abrupt junction, the devices suffered from high leakage current and premature breakdown. Simulations have demonstrated that the high electric field induced by the ultrashallow B-doped region at the anode contact edges is responsible for band-to-band tunneling current, while high-lifetime Si materials are also needed to minimize trap-assisted tunneling effects. Diffused guard-rings have been proposed as a solution to reduce the electric field crowding at the contact rim, while channel-stop implants can prevent the depletion region to approach the RIE-damaged Si trenches. A noteworthy improvement of the electrical performance has been achieved by the latest varactor implementations for a uniform profile and a hyper-abrupt  $1/x^2$  junction, both designed for high control voltages. The devices have unprecedented low reverse leakage current and an increased operating voltage range close to the theoretical breakdown limit. At the same time, the desired capacitance-voltage relationship is still preserved by the compatibility of the thermal processing steps with the As profiles. However, from these preliminary tests new challenges have emerged due to the sensitivity of the breakdown voltage to the backside ohmic contact formation. Therefore, further developments of the back-wafer process module, along with an optimization of the current device layout, could feasibly yield unique ruggedness and reliability.

# Chapter 6

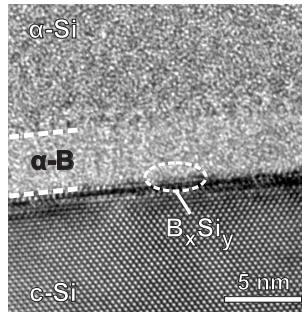
# Deep-/extreme-ultraviolet radiation photodiodes

The B-deposition has been successfully applied for the fabrication of planar  $p^+n$  photodiodes for radiation detection in deep-/extreme-ultraviolet (DUV/EUV) spectral range. In this Chapter, the  $\text{B}_2\text{H}_6$  exposure conditions for the formation of the front anode surface have been specifically optimized to increase the optical conversion efficiency, while the process module is also proven to be extended in a compatible manner for the series resistance reduction and optical coating.

The fundamental advantages of the B-layers for use as a novel  $p^+$  front-layer in UV detectors are illustrated by the electrical and optical performance, along with the stability to high radiation doses. The results are also supported by the comparison with commercial state-of-the-art photodiodes. The optical characterization was performed at the UV radiometry laboratories of the Physikalisch-Technische Bundesanstalt (PTB) located at the BESSY II electron storage ring in Berlin, Germany, [72].

## 6.1 Formation of photodiode $p^+$ front-area

Depending on the radiation wavelengths of interest, the  $p^+$  region of the diode can be formed in three subsequent steps: (a) pure boron deposition from diborane ( $\text{B}_2\text{H}_6$ ), (b) *in-situ* thermal annealing, and (c) selective B-doped Si epitaxial growth. In fact, the responsivity to nm-deep-absorbed DUV photons is certainly maximized by the extremely ultrashallow and ideal  $p^+n$  junction achieved by using solely the B-deposition. However, the basic process can be extended combining the B-layer with the last two optional steps to mainly achieve a reduced sheet-resistance of the top-semiconducting layer, i.e. a lower photodiode series resistance, and increased processing flexibility without compromising the optical efficiency for those applications where the silicon radiation absorption length is higher, such as in the EUV spectral range.



**Figure 6.1:** High-resolution TEM image of a B-layer formed after 2.5 min  $\text{B}_2\text{H}_6$  exposure at  $700^\circ\text{C}$ . The sample has been covered with PVD  $\alpha$ -Si for the TEM analysis.

### 6.1.1 B-deposition

As the central step in the diode formation process, the detection area is covered by B-layers formed at  $700^\circ\text{C}$  during  $\text{B}_2\text{H}_6$  exposure with gas flow rate of 490 sccm in a 760 Torr ambient. An example is shown in Fig. 6.1 for a 2.5 min B-deposition. In particular, the exposure time should be chosen in order to minimize any possible quantum efficiency loss due to absorption and reflection of radiation in the front  $\alpha$ -B layer. Thus, the film thickness determined from either HRTEM or SIMS analysis has been compared with the values extracted by modeling spectral responsivity data around the boron-K edge energy of about 188 eV, i.e. 6.6 nm wavelength, in the presence of an equivalent absorbing pure B-layer. Optical constants for elemental boron have been used as derived by [39]. The extracted B-layer thickness is listed in Table 6.1 for three min-long  $\text{B}_2\text{H}_6$  exposures.

Although segregation of boron atoms has been demonstrated to occur for depositions longer than 20 s, the optical characterization confirms the time dependence of the layer density, i.e. the boron concentration, which indeed turns out to affect the radiation absorption. The excess of boron atoms on the Si surface, due to either B-Si phase or  $\alpha$ -B, starts to be detected only for  $\text{B}_2\text{H}_6$  exposures  $\geq 5$  min. Although the thickness might vary between B-layers deposited on blanket and patterned Si surfaces, the actual thickness can be reconstructed from the spectral signal as long as the B concentration peak saturates at the equivalent atom density of pure boron, e.g. for a 10 min B-layer. Therefore, a 2.5 min deposition is preferably selected for the implementation of photodiodes, since a  $\sim 4$ -nm-thick B-layer provides still EUV radiation transparency and ensures excellent uniform boron coverage even for large area devices, thus securing the spatial homogeneity of the spectral responsivity.

### 6.1.2 *In-situ* thermal annealing

For very large active area photodiodes with a conventional peripheral electrode, the main contribution to the total series resistance will come from the sheet-resistance of the top-semiconducting layer [73]. The sheet-resistance of as-deposited B-layers

**Table 6.1:** B-layer thickness (in [nm]) determined from analytical and optical characterization techniques.

B-deposition time	Characterization technique			
	TEM <sup>a</sup>	TEM <sup>b</sup>	SIMS <sup>a, c</sup>	188 eV radiation <sup>b</sup>
2.5 min	1.8	4.0	-	0
5 min	2.8	-	-	2.5
10 min	4.4–5.5	-	6.8	6.5

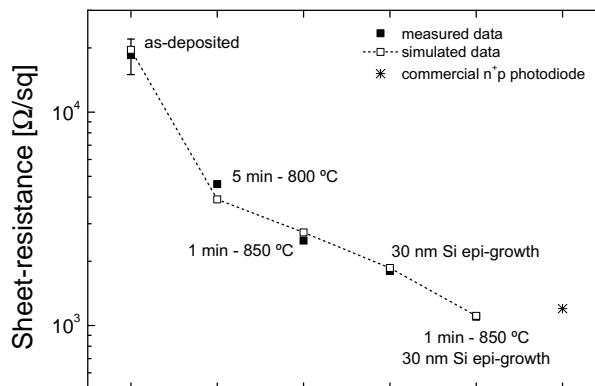
<sup>a</sup> B-deposition on blanket Si surfaces (see Fig. 2.2).

<sup>b</sup> B-deposition in contact windows.

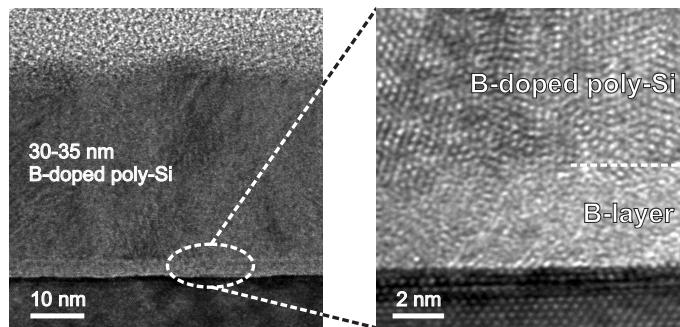
<sup>c</sup> Full-width-at-half-maximum.

applied for photodiode integration has been measured to increase from  $10 \text{ k}\Omega/\text{sq}$  to  $20 \text{ k}\Omega/\text{sq}$  as the deposition time is reduced from 10 min to 2.5 min. This may degrade performance in those applications where severe requirements are imposed on parameters such as linearity and response time.

However, as illustrated in Chapter 4, the conductivity of the B-layer stack can be substantially increased by an *in-situ* thermal annealing. In particular, short-time drive-ins are chosen in order to limit boron diffusion into the substrate. The results presented here correspond to anneals of 5 min at  $800^\circ\text{C}$  and 1 min at  $850^\circ\text{C}$  carried out on 2.5 min B-layers, and the corresponding sheet-resistance values are shown in Fig. 6.2. While both thermal treatments were selected in order to ensure a similar junction depth ( $\sim 40 \text{ nm}$ ), as determined by diffusion simulations, the reduction of the sheet-resistance in the boron-doped top-layer for increasing temperatures is due to greater dopant activation.



**Figure 6.2:** Measured and simulated sheet-resistance of a 2.5 min as-deposited B-layer without or with post-processing treatments. For comparison, the sheet-resistance of the  $n^+$ -junction of a commercial  $n^+p$  photodiode is also shown (after [73]).



**Figure 6.3:** TEM image of a B-doped Si film grown by CVD at 700 °C after a B-layer was formed with 2.5 min B<sub>2</sub>H<sub>6</sub> exposure at 700 °C and thermally annealed at 850 °C for 1 min.

### 6.1.3 Selective B-doped silicon epitaxial growth

The formation of the active  $p^+$  region can be optionally completed with a selective B-doped Si epitaxial growth at 700 °C both on the as-deposited and thermally annealed B-layers in the same CVD reactor at reduced pressure. A TEM image of the final layer stack is shown in Fig. 6.3 for a sample where a 2.5 min B-deposition was combined with 1 min *in-situ* thermal anneal at 850 °C and followed by a 30–35 nm thick CVD Si growth. A B<sub>2</sub>H<sub>6</sub> gas was also used for boron doping of the deposited Si film. The interface between each layer of the stack can be clearly distinguished. The image also confirms the B atoms segregated during B<sub>2</sub>H<sub>6</sub> exposure to be thermally stable when annealed at higher temperatures. The TEM analysis reveals the grown Si film to be polycrystalline with randomly oriented grains. In fact, the presence of a relatively thick  $\alpha$ -B layer prevented the film from taking the orientation of the (100) Si substrate, in a manner similar to results reported in [74].

This process was primarily intended to improve the current drivability of the active surface layer. The corresponding reduction on the sheet-resistance is also reported in Fig. 6.2. In addition, an ‘effective’ absorbing  $p^+$  depth was extracted by modeling the response of the photodiode at the Si-L edge energy of 100 eV, i.e. 12.4 nm wavelength. The radiation is seen to be absorbed by a  $\sim$  38 nm thick Si layer, which does in fact fit with the physical thickness of the poly-Si film. Therefore, adding such an extra Si layer would compromise the responsivity for DUV radiation, but for EUV wavelengths above Si-L edge, such as 13.5 nm, the penetration depth is much larger ( $\sim$  600 nm, after [39]), and the optical conversion efficiency would not be strongly influenced.

In addition, the raised epitaxially grown layer was found to be instrumental in suppressing the leakage current observed in those devices fabricated without peripheral  $p^+$  guard-ring diffusion and contacted with pure aluminum metallization. In fact, reduction of thermal oxide along the Si/SiO<sub>2</sub> interface of the contact window during the alloy in forming gas was identified as being responsible for the high current levels. The slight overgrowth of the poly-Si film on the beveled oxide surface not covered by the B-layer can avoid contacting of the Si substrate to the Al after the alloy process.

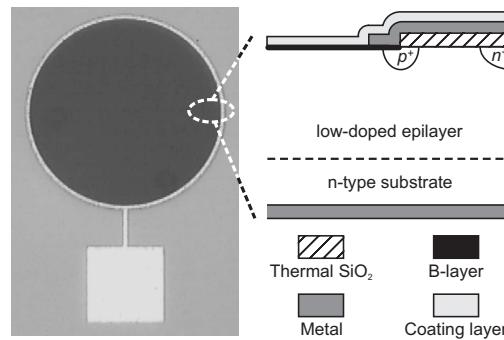


Figure 6.4: Micro-image and cross-section of fabricated photodiodes ( $\varnothing 200 \mu\text{m}$ ).

## 6.2 Device fabrication

A micro-image and a schematic cross-section of the fabricated photodiodes are shown in Fig. 6.4. A low-doped ( $< 10^{14} \text{ cm}^{-3}$ ) epitaxial layer was grown on a  $1-10 \Omega\text{cm}$   $n$ -type (100) Si substrate. The epilayer thickness is adjusted for specific applications requirements in terms of breakdown voltage and junction capacitance. After the growth of a 300 nm thermal SiO<sub>2</sub>,  $n^+$  channel-stop and  $p^+$  guard-ring diffusions were formed with P<sup>+</sup> ( $10^{13} \text{ cm}^{-2}$  at 300 keV) and B<sup>+</sup> ( $10^{13} \text{ cm}^{-2}$  at 180 keV) implantations, respectively, and thermally activated with a 1000 °C anneal. In addition, a P<sup>+</sup> implantation ( $3 \times 10^{15} \text{ cm}^{-2}$  at 40 keV) on the backside of the wafer was used to provide an ohmic contact to the substrate.

The  $p^+$  detection area was then selectively formed, as described above, directly in contact windows that were wet-etched into the SiO<sub>2</sub> field isolation. In particular, photodiodes for the DUV spectral range were fabricated using solely the pure B-deposition, while EUV devices were also implemented by combining *in-situ* thermal annealing and B-doped Si epitaxial growth. Thereafter, Al PVD metallization and patterning define both the outer ring anode contact on the front-side and the cathode electrode on the backside.

Typically, the anode structure is implemented by extending the metallization across the field oxide from the guard-ring to the channel-stop region. In fact, such an electrode has been demonstrated to provide higher reliability to high-energy photons exposure [32], besides the benefits of lower field at the junction edge and better immunity from degradation of reverse I-V characteristics in presence of charge at the silicon/oxide interface. Moreover, for photodiodes with a large active area, the anode contact can also be implemented on the detection surface with a metal mesh layout in order to eliminate the lateral current spreading effect in the as-deposited B-layers by promoting an intrinsic one-dimensional current flow that will reduce the photodiode series resistance.

The diode processing was then completed by an optical coating of the active area and a 400 °C alloy step in forming gas. For DUV radiation, a PECVD SiO<sub>2</sub> is deposited directly on the active B-doped surface as anti-reflection coating layer.

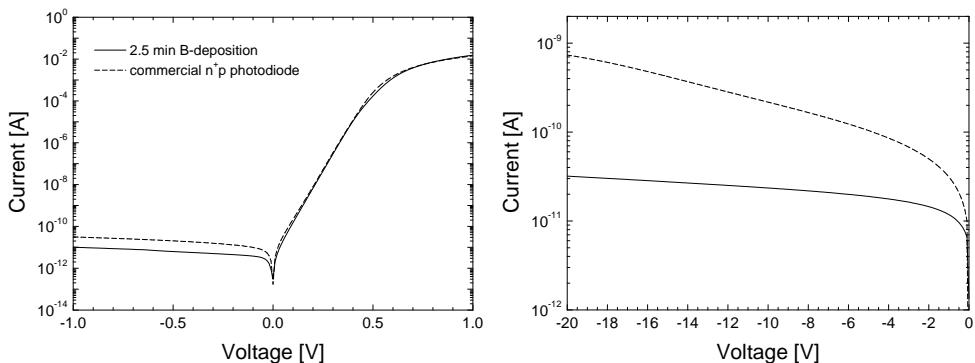
In contrast, for EUV radiation, insulating or conductive top-layers can be optionally deposited to, for example, protect the diode surface or facilitate the design and integration of thin film filters with radiation pass-bands optimized for specific applications. It is worth noting that conductive film filters can also contribute to reduce the series resistance in a manner similar to metal mesh anode layout. Experimental results are reported below for photodiodes with 15 nm PVD aluminum nitride (AlN), 100 nm low-stress PECVD silicon nitride (SiN) as protection layers, and a PVD layer stack of 100 nm zirconium (Zr) and 150 nm silicon as optical filter.

The electrical and optical performance of the fabricated devices are compared in the following sections to either commercially available  $n^+p$  photodiodes or referenced works representative of the current state-of-the-art UV silicon detector technology. In particular, the characterization could also be performed directly on a commercial  $n^+p$  diode with the same circular geometry ( $\varnothing 3.7$  mm). The tested diode was formed by a 9 nm TiSi window on the  $n^+$  active top layer, with a junction depth in the range of 100 nm and a sheet-resistance of  $\sim 1.2 \text{ k}\Omega/\text{sq}$ . Apart from this information, we did not have access to the fabrication details.

## 6.3 Electrical characterization

### 6.3.1 Dark current

Fig. 6.5 shows the I-V characteristics of a 2.5 min as-deposited B-diode in comparison to a commercial  $n^+p$  photodiode. Excellent electrical performance is achieved in terms of low dark current ( $< 50 \text{ pA}$  at a reverse bias voltage of 20 V) and ideal behavior. In fact, the voltage dependence of the dark current for the state-of-the-art device reveals that the generation effects dominate, while B-doped diodes benefit from high-lifetime semiconducting material in the depletion region and negligible surface generation-recombination over the entire active area.



**Figure 6.5:** (Left) Forward and (right) reverse I-V characteristics of a 2.5 min as-deposited B-diode compared to a state-of-the-art  $n^+p$  photodiode. The active area is  $10.75 \text{ mm}^2$  ( $\varnothing 3.7$  mm).

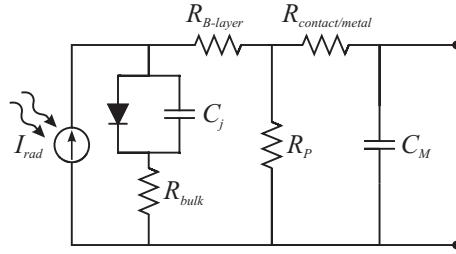


Figure 6.6: Equivalent circuit of a photodiode.

### 6.3.2 Series resistance and response time

As illustrated by the equivalent circuit in Fig. 6.6, the series resistance  $R_S$  of a photodiode consists of three components determined by the resistivity of the substrate, the sheet-resistance of the front-layer, and the contact/metallization resistances [75]. For the tested diodes with a diameter of 3.7 mm, both the large active area and the reverse bias voltage reduce the contribution from the low-doped epilayer. The contact resistances along with the metal interconnections have been measured to be within  $\sim 10\text{--}20\ \Omega$ . On the other hand, the ultrashallow B-doped junction can remarkably contribute to the total  $R_S$  when a peripheral ring electrode is used. In fact, by assuming uniform current generation over the active area, i.e. dark or fully-illumination conditions, the distributed resistive path of a layer with circular geometry and sheet-resistance  $\rho_s$  is characterized by the following lumped term [76]:

$$R_{B-layer} = \frac{\rho_s}{8\pi} \quad (6.1)$$

Therefore, for 2.5 min as-deposited B-layers, Eq. 6.1 predicts that the resistance of the photodiode would be  $740\ \Omega$  on average, while post-processing steps can reduce  $R_{B-layer}$  down to  $45\ \Omega$ .

A capacitance-voltage measurement has been applied to determine the series resistance of fabricated photodiodes. In fact, compared to many other methods reviewed in [52], the series resistance can be directly measured under the typical operating conditions of a detector, i.e. at reverse biasing voltages. An HP4284A LCR meter has been used, which however assumes the device to be represented by either a series  $C_{S,m}\text{--}R_{S,m}$  or parallel  $C_{P,m}\text{--}R_{P,m}$  equivalent circuit. These quantities differ from the actual device lumped components  $C_J$ ,  $R_P$ , and  $R_S$ . Nevertheless, the measured series resistance  $R_{S,m}$  can be in particular expressed as a function of the latter values by

$$R_{S,m} = R_S + \frac{R_P}{\left[1 + (\omega C_J R_P)^2\right]}. \quad (6.2)$$

At high frequency, such as 1 MHz, for typical junction capacitance  $C_J$  of  $\sim 100\ \text{pF}$  and shunt-resistance  $R_P$  of  $\gg 100\ \text{M}\Omega$ , the second term of the right-hand side of Eq. 6.2 can be neglected, and the actual series resistance is measured. However, it

**Table 6.2:** Series resistance of fabricated photodiodes.

Sample description			Total series resistance [ $\Omega$ ]	
B-deposition [min]	Anneal <sup>a</sup> [°C]	Si epitaxy [nm]	experimental <sup>b</sup>	theoretical <sup>c</sup>
2.5	-	-	581–837	600–885
2.5	800	-	215	193
2.5	850	-	112	109
2.5	-	30	95	82
2.5	850	30	70	55
<i>n<sup>+</sup>p</i> diode with 9 nm TiSi			57	48 <sup>d</sup>

<sup>a</sup> *In-situ* thermal anneals for 5 min at 800 °C or 1 min at 850 °C.

<sup>b</sup> The data correspond to  $R_S$  as determined from Eq. 6.3 by using the measured  $R_{S,m}$ ,  $C_J$ , and  $C_M$  values.

<sup>c</sup> A constant contact/metal resistance of 10  $\Omega$  has been added to  $R_{B-layer}$ . The latter is determined by using Eq. 6.1 with the experimental sheet-resistance data of Fig 6.2.

<sup>d</sup> The value only refers to the series resistance of the  $n^+$ -junction.

should be pointed out that the capacitance  $C_M$  of the MOS-like structure formed by the metal track on the field isolation oxide can still influence the measurement, particularly when the biasing conditions favor either accumulation or inversion regime ( $C_M = C_{OX} \approx 60\text{--}80$  pF, depending on the anode metal track area on the  $\text{SiO}_2$ ). The measured value  $R_{S,m}$  will be lower than the actual series resistance  $R_S$  as determined from

$$R_{S,m} = \frac{R_S / (\omega C_M)^2}{R_S^2 + \left( \frac{1}{\omega C_J} + \frac{1}{\omega C_M} \right)^2}. \quad (6.3)$$

Table 6.2 summarizes the total series resistance  $R_S$  of the fabricated photodiodes at a reverse bias voltage of 7.5 V, as extracted by using Eq. 6.3. Thus, the experimental data are in good agreement with the theoretical values. Some deviations are mainly due to uncertainties of  $C_M$  in the (deep)-depletion regime and variation of the metal/contact resistance among the samples.

The photodiode transient response to pulsed-light will be accordingly dominated by the time constant of the  $R_S\text{--}C_J$  equivalent circuit. The measurements were performed at the Electronic Instrumentation Laboratory of Delft University of Technology [77]. A green light-emitting diode (LED) was used as the light source. Radiation wavelengths in the range of 520–565 nm have a penetration depth in silicon of  $\sim 1$   $\mu\text{m}$ , which is comparable to the absorption of EUV radiation above the Si-L edge. Thus, the setup could offer a feasible and reliable measurement of the corresponding response time. The LED was driven by a pulsed signal with a frequency of 100 kHz and pulse duration of 100 ns. The time constant extracted from the exponential decay

**Table 6.3:** Responsivity at the radiation wavelength of 193 nm.

Sample description			Responsivity [A/W]
B-deposition [min]	Anode electrode structure	SiO <sub>2</sub> [nm]	
2.5	peripheral	270–280 <sup>a</sup>	0.115
2.5	mesh	270–280 <sup>a</sup>	0.106
2.5	peripheral	100	0.100
5	peripheral	270–280 <sup>a</sup>	0.088
5	mesh	270–280 <sup>a</sup>	0.072
5	mesh	-	0.077
10	mesh	-	0.042
PtSi- <i>n</i> -Si <sup>b,c</sup> (2–7 nm)			0.021–0.040
<i>n</i> <sup>+</sup> <i>p</i> diode with 4 nm PtSi <sup>c</sup>			0.004
<i>n</i> <sup>+</sup> <i>p</i> diode with 6 nm nitrided SiO <sub>2</sub> <sup>c</sup>			0.095
<i>n</i> <sup>+</sup> <i>p</i> diode with 160 nm nitrided SiO <sub>2</sub> <sup>c</sup>			0.105

<sup>a</sup> The actual oxide thickness is not known and might vary among the samples due to different coating process conditions. An indicative value has been determined from comparison between spectral responsivity data and optical simulations of SiO<sub>2</sub> transmittance.

<sup>b</sup> After [34].

<sup>c</sup> After [35].

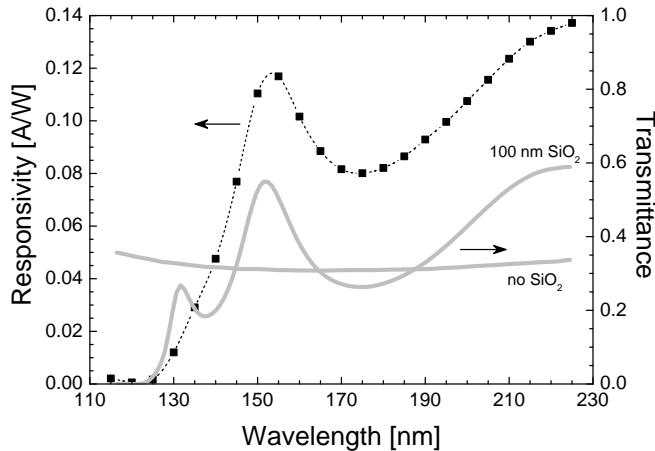
of the output signal was about 98 ns for a 2.5 min as-deposited B-diode at reverse biasing condition of 7.5 V. This value is found to be quite consistent with respect to the measured  $R_S$  and  $C_J$  components.

## 6.4 Optical characterization

### 6.4.1 Responsivity in DUV spectral range

As-deposited B-doped diodes with and without an anti-reflection SiO<sub>2</sub> coating layer have been characterized in the wavelength range from 115 nm to 225 nm for different B<sub>2</sub>H<sub>6</sub> exposure times. Samples fabricated with 20- $\mu$ m-pitch metal mesh anode structure on the active surface have also been included to investigate any significant responsivity attenuation traded-off with very low photodiode series resistance ( $\sim 10 \Omega$ ). A summary of measured responsivity is presented in Table 6.3 for the radiation wavelength of 193 nm. The DUV optical performance is also compared to that of both Schottky-junction and commercial *n*<sup>+</sup>*p* photodiodes, where the latter is covered with either 6–160 nm nitrided SiO<sub>2</sub> or a metal-silicide layer.

All B-doped photodiodes show high sensitivity in the DUV spectral range, al-



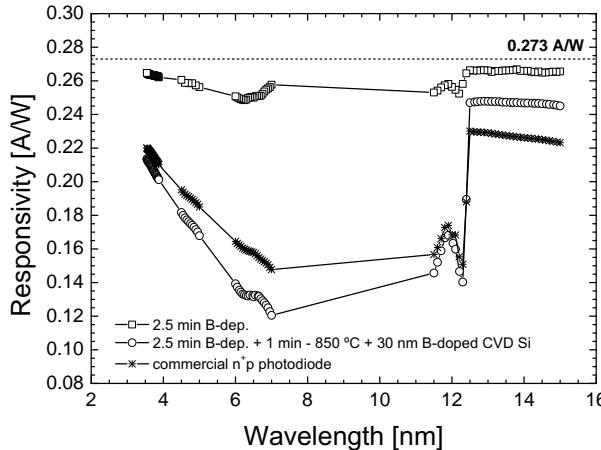
**Figure 6.7:** (Left y-axis) Measured spectral responsivity (symbols) of a 2.5 min B-doped diode with 100 nm  $\text{SiO}_2$  anti-reflection coating layer in the 115–225 nm wavelength range. (Right y-axis) The normal incidence transmittance into silicon with and without a 100 nm  $\text{SiO}_2$  coating layer as determined by optical simulations.

though longer deposition times result in lower responsivity due to a thicker and ‘optically’ more dense B-layer, which might at these wavelengths introduce not only absorption but also reflectance losses. Nevertheless, the responsivity of all types of detectors is higher than the Schottky-like diodes, which generally suffer from low optical response and poor reproducibility, despite their stability under prolonged irradiation [35]. On the other hand, for boron-doped junctions with a similar sheet-resistance of the as-deposited B-layers, doping methods proposed elsewhere resulted in rapid decrease in optical response [32], since photogenerated carriers are likely to experience a significant surface recombination.

Furthermore, the presence of a metal grid on the active surface seems to reduce slightly the responsivity. However, it was not possible to quantitatively determine the corresponding attenuation, since oxide thickness variations among the samples might concomitantly affect the optical response. Fig. 6.7 shows the typical responsivity of a 2.5 min B-doped photodiode with 100 nm PECVD  $\text{SiO}_2$  coating layer. The variations in the responsivity are caused by the spectral dependence of the  $\text{SiO}_2$  transmittance, as also confirmed by optical simulations of the interference effects in the stacked materials for normal incidence. Therefore, for wavelengths greater than 140 nm, the oxide thickness could be more responsible for non-uniformities of responsivity in large-area detectors. In contrast, at shorter wavelengths the thick oxide layer significantly absorbs the incident radiation.

#### 6.4.2 Responsivity in EUV spectral range

EUV spectral responsivity of 2.5 min B-deposited diodes without and with an 850 °C thermal anneal combined with boron doped epitaxial silicon growth is shown



**Figure 6.8:** Measured EUV spectral responsivity (symbols) of 2.5 min B-deposited diodes without and with a 1 min *in-situ* thermal anneal at 850 °C and 30 nm epitaxial B-doped Si growth, compared to a commercial state-of-the-art  $n^+p$  photodiode with 9 nm TiSi front window. The dashed line shows the theoretical limit for silicon responsivity 1/3.66 A/W (after [78]).

in Fig. 6.8. The diodes were characterized in three wavelength ranges, namely, from 11.5 nm to 15 nm, which includes also the Si-L edge at 12.4 nm (100 eV), a range around the boron edge at 6.6 nm (188 eV), and above and below the carbon edge at 4.4 nm (284 eV). The latter wavelength ranges gave more insight into the B-layer properties and could detect carbon contamination on the active surface.

At the radiation wavelength of 13.5 nm, the as-deposited B-diode has a responsivity that is practically that of an ideal lossless system, which is 0.273 A/W [78]. Thus, the superior optical performance with respect to the current commercial state-of-the-art photodiode displays the advantages of the ultrashallow and high-quality junction resulting from the B-deposition process, which minimizes any internal quantum efficiency loss due to either recombination of photogenerated carriers or absorption in the front window. Even after adding an extra Si layer to reduce the series resistance, the photodiode still performs with higher responsivity.

A summary of measured responsivity at the radiation wavelength of 13.5 nm is presented in Table 6.4 for samples with different  $p^+$  active-area formation-processes and top-layer coatings. First, the thermal annealing either at 800 °C or at 850 °C does not significantly change the responsivity with respect to as-deposited devices with an AlN coating, and thus can without trade-off be used to lower the series resistance. In fact, the electric field induced by the resulting doping distribution can counteract the junction depth increase.

Furthermore, the technology has been proven to be capable of coating the photosensitive surface without compromising the initial optical performance, since the measured responsivity has been found to be in good agreement with values deter-

**Table 6.4:** Responsivity at the radiation wavelength of 13.5 nm.

Sample description				Responsivity [A/W]
B-deposition [min]	Anneal <sup>a</sup> [°C]	Si epitaxy [nm]	Coating layer	
2.5	-	-	-	0.266
5	-	-	-	0.261
10	-	-	-	0.256
2.5	850	30	-	0.247
2.5	-	-	100 nm SiN	0.170
2.5	-	-	15 nm AlN	0.184 <sup>b</sup>
2.5	800	-	15 nm AlN	0.171
2.5	850	-	15 nm AlN	0.170–0.182 <sup>b</sup>
2.5	850	30	15 nm AlN	0.166
2.5	850	30	100/150 nm Zr/α-Si	0.107
<i>n<sup>+</sup> p diode with 9 nm TiSi</i>				0.227

<sup>a</sup> *In-situ* thermal anneals for 5 min at 800 °C or 1 min at 850 °C.

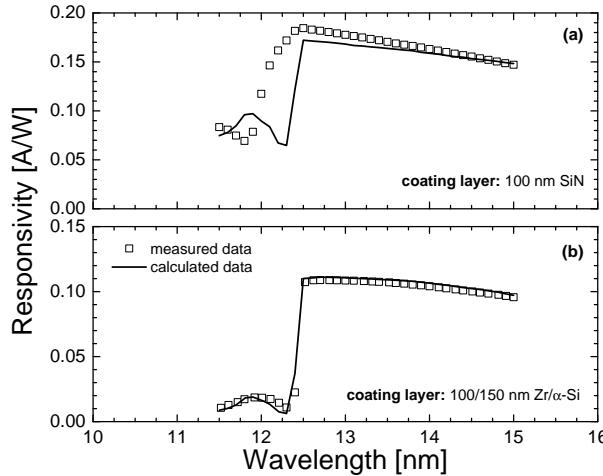
<sup>b</sup> The actual AlN thickness appeared to be thinner than the nominal value.

mined by modeling the absorption of the top-layers. In particular, Fig. 6.9(a) shows the measured and calculated spectral responsivity for a 2.5 min as-deposited B-diode covered with a 100 nm SiN protective layer, while Fig. 6.9(b) illustrates the radiation pass-band of conventional Zr/α-Si optical filter directly integrated by PVD deposition on the active front-window. While in the latter case the sharper cut-off at the Si-L edge is mainly dominated by the 150 nm α-Si top layer, the non-stoichiometric composition of the 100 nm SiN layer gives a more gradual transition in the measured optical response than the theoretical curve does. In all cases, however, the spectral responsivity at longer wavelengths is well described by the transmittance of the coating films and the initial optical efficiency of the B-layer. Thus, these results confirm both the reliability and reproducibility of the entire process.

## 6.5 Performance stability

### 6.5.1 Dark current degradation

In order to investigate radiation-induced degradation on the electrical performance, the stability of the dark current and photogenerated signal was first tested within a 10 min time interval with on/off radiation cycles at the wavelength of 11.5 nm. In fact, at this radiation the responsivity is particularly sensitive to changes of the charge collection efficiency of the active volume within ∼ 50 nm from the top



**Figure 6.9:** Measured (symbols) and calculated (solid line) EUV spectral responsivity of: (a) 2.5 min B-doped diode with a protective coating layer of 100 nm PECVD SiN; (b) optical filter layer stack of 100/150 nm PVD Zr/α-Si deposited on the  $p^+$  active area formed by combining a 2.5 min B-deposition with 1 min *in-situ* 850 °C thermal anneal and 30 nm epitaxial B-doped Si growth. Calculations have been made by using optical absorption coefficients from [39].

interface. The pulse response of a 2.5 min B-doped photodiode either without or with the optional post-processing steps was measured to be very stable during all the illumination cycles. Therefore, under normal radiation exposure conditions, the  $p^+$ -doped active layer formed in our process is very robust.

Thereafter, accelerated aging tests were performed on the photodiodes with prolonged exposure to high dose EUV radiation, as those described in the next section. A relatively high increase of the photodiode dark current in the range of  $10^{-7}$ – $10^{-6}$  A was particularly observed for those samples not properly designed with respect to prevention of surface generation and anode-induced space-charge region currents under the field isolation oxide. This degradation was generally found to be partially or completely annealed out by thermal treatment at relatively low temperatures, such as  $\sim 200$  °C, similarly to [32]. Recent implementations, however, demonstrated that the stability to radiation exposure was improved in a manner that the dark current increased only up to 10 nA after a 400 kJ/cm<sup>2</sup> irradiation. Reduction of minority carrier lifetime in the bulk Si can be excluded because the radiation spectrum used for the tests does not involve Si lattice damage. On the other hand, the charging of the field isolation oxide during UV irradiation [79] is most likely the mechanism that governs the dark current degradation, rather than B-layer or Si properties being altered. This oxide charging in conjunction with the chemical and electrical instability of the SiO<sub>2</sub> surface due to environment humidity conditions can adversely and heterogeneously influence the diode I-V characteristics [80].

**Table 6.5:** Degradation of the responsivity at the wavelength of 13.5 nm after prolonged exposure to EUV radiation.

Sample description			Exposure conditions	Responsivity degradation
B-deposition [min]	Anneal [°C]	Coating layer		
2.5	-	-	21 h - 190 kJ/cm <sup>2</sup>	1.3%
5	-	-		1.5%
10	-	-		1.0%
2.5	-	100 nm SiN	24.5 h - 219 kJ/cm <sup>2</sup>	0.9%
2.5	800	15 nm AlN		0.0%
2.5	850	15 nm AlN		0.4%
<i>n<sup>+</sup> p diode with 9 nm TiSi</i>			21 h - 190 kJ/cm <sup>2</sup>	3.0%

### 6.5.2 Responsivity degradation

The stability of the optical performance for photodiodes fabricated with different B-layer processing was characterized by prolonged exposure to intense EUV photon levels, by using the setup described in [37]. A summary of the responsivity degradation after high-dose irradiation is reported in Table 6.5. The effect of insulating coating layers, such as AlN and SiN, on the radiation hardness has been also investigated. All photodiodes exhibit negligible change in responsivity when exposed to EUV radiation with a power density of 2.5 W/cm<sup>2</sup>. This result confirms the excellent stability in the optical behavior of the B-layer compared to the state-of-the-art photodiodes, where, however, the measured responsivity degradation is mainly due to carbon contamination rather than change in the internal quantum charge collection efficiency. Furthermore, the ruggedness to EUV photons for photodiodes with front insulating layers, such as AlN and SiN, is a demonstration of the high quality of the interface with the B-doped region. In fact, although a common cause of instability of silicon photodiodes to photon irradiation is the degradation of the front window, no exposure-induced instability was observed. This can be mainly due to the high boron content in the surface layers that can secure the built-in electric field.

## 6.6 Conclusions

The B-layers have been successfully implemented in a silicon-based planar photodiode technology for radiation detection in the complete VUV spectral range down to soft X-ray wavelengths. Outstanding photodiode performance has been achieved using the as-deposited B-layers, since comparison with the state-of-the-art detector technology showed that B-deposited devices perform with superior electrical and op-

tical characteristics. In fact, they exhibit an ideal diode behavior with lower dark current. Furthermore, by properly tuning the  $\text{B}_2\text{H}_6$  exposure conditions to minimize any quantum efficiency loss, the extremely shallow front active  $p^+$  region offers higher sensitivity over a wider UV spectral region. In particular, they show near theoretical responsivity at short-wavelength radiation with excellent reproducibility.

The B-doped diodes proved to be robust to high-dose radiation exposure, since negligible degradation has been observed. Such a ruggedness and reliability are also demonstrated when an optical coating is integrated to either minimize reflection losses or determine a filtered radiation pass-band. Finally, the process offers high flexibility in optimizing further device parameters in relationship to application specific designs, such as the diode series resistance, by combining the B-deposition with *in-situ* thermal annealing and/or selective epitaxial Si growth, without compromising the optical efficiency for radiation wavelengths with lower Si absorption coefficient.

Therefore, these properties make the fabricated devices particularly suitable for photon detection in several applications ranging from next-generation EUV lithography tools to solar metrology in space mission, offering a very noteworthy contribution to the present status of Si-based UV detector technology.



# Chapter 7

## Conclusions and recommendations

### 7.1 Conclusions

The main conclusions of the work are summarized as follows:

- **Material and IC processing characteristics**
  - A boron-rich layer can be formed on (100)-oriented silicon in a chemical vapor deposition reactor either at atmospheric or reduced pressures by using  $\text{B}_2\text{H}_6$  gas at high concentrations. The boron surface density is predominantly determined by the exposure time, and constant film growth rate is observed. The composition of the layer is dependent on the processing temperature and can vary from amorphous boron ( $\alpha\text{-B}$ ) to a boron-silicon ( $\text{B}_x\text{Si}_y$ ) compound for increasing thermal budget,  $\sim 700^\circ\text{C}$  being the transition temperature.
  - The high-concentration B-layer acts as a source for dopant in-diffusion already from the first stage of the  $\text{B}_2\text{H}_6$  exposure itself. Owing to the relatively low temperatures ( $\leq 700^\circ\text{C}$ ) and the absence of any enhanced diffusion effects,  $p^+$  doping of the silicon substrate can be achieved within few nanometer of the surface even for prolonged depositions. The maximum doping concentration is limited by solid solubility, while the time dependence of the diffused dose is  $\propto \sqrt{time}$ .
  - The process is fully IC compatible and highly selective to Si. Either  $\text{SiO}_2$  or  $\text{SiN}$  can be used as hard-mask for direct deposition in contact openings. At  $700^\circ\text{C}$  the spatial uniformity is excellent and ensures isotropic coverage of non-planar Si surfaces. Thus, the B-layer can be reliably integrated in device structures that include trenches or recessed-contacts. The reactivity with some acid-based solutions allows removal of the B-layer, while the film is also proven to form a silicon diffusion barrier for integration of pure aluminum contacts.

- The B-layer can be used as a well-controlled source of boron during subsequent *in-situ* or *ex-situ* high-temperature drive-in. Additional capping layers can be avoided, since the thermal stability of nm-thick layers prevents boron desorption. However, anneals in hydrogen ambient can still favor evaporation of boron-hydrides. Thus for *in-situ* thermal processing, short-time drive-ins are preferable.

- ***pn*-junction formation**

- B-layers are successfully applied to form high-quality, extremely ultrashallow  $p^+n$ -junction diodes and emitters in *pnp* BJT's. The bipolar devices show excellent junction properties, which indicate the doping technology to be 'defect-free'. By increasing the exposure time, i.e. the thickness of the layer, the I-V characteristics can be tuned from Schottky-like behavior to deep  $p^+n$  diode current levels, despite the nm-deep junction depth. The high-effective Gummel number of the  $p^+$ -region that is necessary for this, is mainly accorded to the properties of the  $\alpha$ -B layer. Thus, doping efficiency superior to conventional B-doped Si epitaxy and comparable to  $B^+/BF_2^+$  ion implants is achieved. The high-resistivity property of the B-layer can be also used as a very compact means for inserting high-ohmic resistors.

- **Innovative applications**

- The B-deposition has proven to be attractive in varactor diodes for RF tuning applications. In fact, the CVD process enhances the capabilities of the silicon-on-glass substrate-transfer technology since the abruptness of the  $p^+$  anode region and the low thermal deposition can preserve the As doping profiles needed for linearity constraints. Although reverse I-V characteristics of as-deposited B-layers suffer from band-to-band tunneling at the contact edges, integration of a guard-ring diffusion enables ideally low reverse current and extends the maximum operating voltage up to the theoretical breakdown limit.
- B-layers applied to UV photodiode technology can provide electrical and optical performance as a state-of-the-art detector technology. Low dark current and near theoretical responsivity in the UV spectral range down to soft X-ray wavelengths are achieved. Surface optical coating is also fully compatible without compromising the intrinsic properties of the sensitive detection area. Rapid *in-situ* thermal annealing can be used to improve the current drivability of the  $p^+$  region without affecting the optical performance.

## 7.2 Recommendations

Future work can span over the following research areas:

- **Material characterization**

- A preliminary analytical characterization has been here presented by using TEM and SIMS techniques, but a more thorough investigation of the layer

composition could be performed to obtain additional information on the surface reaction kinetics. Techniques such as X-ray photoelectron spectroscopy (XPS), Fourier-transform infrared spectroscopy (FTIR), Raman spectroscopy, and scanning probe microscopy can be used in this respect.

- **Process and device integration**

- Compared to silicon, incorporation of boron in the SiGe lattice is higher for the same processing temperature. Thus, pure  $B_2H_6$  exposure could also be applied to SiGe system. The contact resistivity and sheet-resistance can significantly profit from concomitant Ge bandgap engineering and doping concentration enhancement.
- The B-deposition process can be combined with an excimer laser annealing to facilitate the incorporation of boron atoms into the silicon well above the solid solubility. Initial experiments already suggested very high doping efficiency. This can offer exciting possibilities to develop novel devices. For example, recently Bustarret *et al.* have successfully demonstrated superconductivity in heavily B-doped silicon [81].
- The  $B_2H_6$  exposure can be considered for implementation of the intrinsic base region of *npn* homojunction or heterojunction bipolar transistors.
- The thin epilayer stack of the  $1/x^2$  varactor profile for low control voltages prohibits the use of guard-ring diffusions. Edge effects might be eliminated by considering the moat-etched version of the overlay structure [82]. Profiting from the isotropy of the B-deposition, the convex contact created by controlled Si etching under the oxide layer can give the necessary junction curvature. This approach could also be applicable to profiles for higher control voltages.
- The process scheme for the formation of the varactor Si islands could be optimized to reduce the Si surface/bulk RIE-damage and provide better coverage and lower stress associated with the front-wafer isolation/metal stacks.
- Although the increase of the photodiode dark current after prolonged irradiation might not be due to degradation of the B-layer itself, this aspect should be further investigated in order to provide devices with improved ruggedness.



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# List of symbols and abbreviations

*List of symbols:*

$\beta_F$	common-emitter current gain
$\Delta E_G$	bandgap difference with respect to Si
$\Delta V_{FB}$	shift of the MOS flatband voltage
$\epsilon_0$	permittivity in vacuum
$\epsilon_{Si}$	silicon dielectric constant
$\lambda$	wavelength
$\rho_s$	sheet-resistance
$\tau_{g,G}$	generation lifetime in the MOS gate-induced space-charge region
$\tau_{g,J}$	generation lifetime in the diode space-charge region
$\tau_r$	minority recombination lifetime in the diode quasi-neutral region
$\omega$	angular frequency
$A_{BE,eff}$	effective base-emitter junction area
$A_G$	metal gate area
$A_J$	effective junction area
$C$	capacitance per unit area
$C_{max}/C_{min}$	ratio between the maximum and minimum varactor capacitance
$C_{FB}$	MOS capacitance per unit area at the flatband voltage
$C_J$	junction capacitance
$C_M$	capacitance of the MOS structure formed by the metal track on the isolation oxide
$C_{OX}$	oxide capacitance per unit area
$C_{P,m}$	capacitance as measured by an LCR meter in parallel equivalent circuit mode
$C_{S,m}$	capacitance as measured by an LCR meter in series equivalent circuit mode
$D_{it}$	interface trapped charge density
$D_n$	electron diffusion coefficient
$D_p$	hole diffusion coefficient
$D_B$	boron doping density
$D_{OX}$	positive oxide charge density
$E_F$	Fermi energy level
$G_B$	base Gummel number
$G_E$	emitter Gummel number
$I_{n,B-E}$	electron injection current into the emitter from the base
$I_B$	base current
$I_C$	collector current
$k$	Boltzmann's constant
$m$	power-law exponent of the varactor bulk doping distribution
$n_{i0}$	intrinsic carrier concentration in silicon
$n_{ie}$	effective intrinsic carrier concentration
$N_A$	acceptor doping concentration

$N_D$	donor doping concentration
$N_E$	doping concentration in the emitter
$OIP_3$	output third-order intercept point
$q$	electron charge
$Q$	quality-factor
$R_{B-layer}$	lateral series resistance of the B-layer
$R_P$	photodiode shunt resistance
$R_{P,m}$	resistance as measured by an LCR meter in parallel equivalent circuit mode
$R_S$	series resistance
$R_{S,m}$	resistance as measured by an LCR meter in series equivalent circuit mode
$s$	varactor sensitivity
$s_g$	surface generation velocity at the Si/SiO <sub>2</sub> interface
$S_E$	recombination velocity at the emitter contact
$T$	absolute temperature
$V_{bi}$	built-in voltage of a <i>pn</i> -junction
$V_{sub}$	substrate voltage
$V_{EB}$	voltage between the emitter and base terminals
$V_{FB}$	MOS flatband voltage
$V_G$	gate voltage
$V_R$	reverse bias voltage
$V_T$	thermal voltage
$W$	width of the depletion region
$W_{\alpha-B}$	thickness of the $\alpha$ -B layer
$W_{c-Si}$	depth of the as-diffused B-doped c-Si region
$W_{B_xSi_y}$	thickness of the $B_xSi_y$ layer
$W_G$	width of the depletion region in a MOS structure
$W_J$	width of the depletion region in a <i>pn</i> -junction
$W_{QNE}$	width of the quasi-neutral emitter region

*List of chemical symbols and abbreviations:*

$\alpha$ -	amorphous
Al	aluminum
Al/Si(1%)	aluminum pre-saturated with silicon (percentage of silicon)
AlGaN	aluminum-gallium nitride
AlN	aluminum nitride
ArF	argon fluoride
As	arsenic
As <sup>+</sup>	arsenic ions
AsH <sub>3</sub>	arsine
B	boron
B <sup>+</sup>	boron ions
B <sub>12</sub>	icosahedron boron cluster
BF <sub>2</sub> <sup>+</sup>	boron fluoride ions
B <sub>2</sub> H <sub>6</sub>	diborane
B <sub>n</sub> H <sub>m</sub>	boron hydride
B <sub>x</sub> Si <sub>y</sub>	boron-silicon compound (often referred to as boron-silicide)
Br <sub>2</sub>	bromine
c-	crystalline
Cl <sub>2</sub>	chlorine
Cs <sup>+</sup>	cesium ions
F <sub>2</sub>	fluorine
GaN	gallium nitride
Ge	germanium

<b>H<sub>2</sub></b>	hydrogen
<b>HF</b>	hydrofluoric acid
<b>HNO<sub>3</sub></b>	nitric acid
<b>N<sub>2</sub></b>	nitrogen
<b>O<sub>2</sub><sup>+</sup></b>	oxygen ions
<b>P<sub>2</sub><sup>+</sup></b>	phosphorus ions
<b>PH<sub>3</sub></b>	phosphine
<b>PtSi</b>	platinum silicide
<b>Si</b>	silicon
<b>SiGe</b>	silicon-germanium alloy
<b>Si<sub>3</sub>N<sub>4</sub></b>	silicon nitride
<b>SiN</b>	non-stoichiometric silicon nitride
<b>SiO<sub>2</sub></b>	silicon dioxide (often referred to simply as silicon oxide)
<b>TEOS</b>	tetraethylorthosilicate
<b>TMAOH</b>	tetramethylammonium hydroxide
<b>TiSi</b>	titanium silicide
<b>Zr</b>	zirconium

*List of abbreviations:*

<b>AP</b>	atmospheric pressure
<b>BED</b>	boron-enhanced diffusion
<b>BJT</b>	bipolar junction transistor
<b>BOX</b>	buried oxide
<b>C-V</b>	capacitance-voltage
<b>CMOS</b>	complementary metal-oxide-semiconductor
<b>CVD</b>	chemical vapor deposition
<b>DIMES</b>	Delft Institute of Microsystems and Nanoelectronics
<b>DFVS</b>	distortion-free varactor stack
<b>DUV</b>	deep-ultraviolet
<b>ECTM</b>	Electronic Components, Technology, and Materials
<b>EUV</b>	extreme-ultraviolet
<b>FTIR</b>	Fourier-transform infrared spectroscopy
<b>FWHM</b>	full-width-at-half-maximum
<b>HBT</b>	heterojunction bipolar transistor
<b>HRTEM</b>	high-resolution transmission electron microscopy
<b>HTRVS</b>	high tuning range varactor stack
<b>I-V</b>	current-voltage
<b>IC</b>	integrated circuits
<b>LCR</b>	inductance, capacitance, resistance
<b>LED</b>	light-emitting diode
<b>LPCVD</b>	low-pressure chemical vapor deposition
<b>ML</b>	monolayer
<b>MOS</b>	metal-oxide-semiconductor
<b>MOSFET</b>	metal-oxide-semiconductor field effect transistor
<b>NTSVS</b>	narrow tone-spacing varactor stack
<b>PECVD</b>	plasma-enhanced chemical vapor deposition
<b>PTB</b>	Physikalisch-Technische Bundesanstalt
<b>PVD</b>	physical vapor deposition
<b>RF</b>	radio frequency
<b>RIE</b>	reactive ion etching
<b>RP</b>	reduced pressure
<b>scr</b>	space-charge region
<b>SEM</b>	scanning electron microscopy

<b>SIMS</b>	secondary ion mass spectrometry
<b>SOG</b>	silicon-on-glass
<b>SOI</b>	silicon-on-insulator
<b>TED</b>	transient-enhanced diffusion
<b>TEM</b>	transmission electron microscopy
<b>UV</b>	ultraviolet
<b>VUV</b>	vacuum ultraviolet
<b>WTSVS</b>	wide tone-spacing varactor stack
<b>XPS</b>	X-ray photoelectron spectroscopy

# Summary

## Characterization of pure boron depositions integrated in silicon diodes for nanometer-deep junction applications

by *Francesco Sarubbi*

Doping technologies for formation of ultrashallow and highly-doped  $p^+$ -junctions are continuously demanded to face the challenges in front-end processing that have emerged due to the aggressive downscaling of vertical dimensions for future semiconductor devices. As an alternative to implantations, current solutions are based on *in-situ* boron (B) doping during Si/SiGe chemical vapor deposition (CVD) by using diborane ( $B_2H_6$ ) as the dopant gas. In this context, a few studies have demonstrated  $p^+$ -like doping behavior of *n*-type (100)-oriented Si surfaces after exposure solely to  $B_2H_6$  in an oxygen-free atmosphere without any extra addition of silane-based sources. As illustrated in **Chapter 1**, this doping process relies on the thermal decomposition of the source gas, so that the available boron atoms may stick to the surface, chemically react with silicon atoms, and diffuse into the substrate. Contrary to other doping impurities, by appropriately varying the source gas parameters and the exposure time, the reaction kinetics can also cause the boron density at the silicon surface to significantly increase beyond the solid solubility in Si at the given processing temperature. Thus, a boron layer can be formed. However, this property has not been explored so far with respect to reliable integration in Si-based device technologies, since boron segregation has been commonly addressed as a drawback of this doping method.

This thesis presents the characterization of nanometer-thick B-layers formed during exposure to diborane in a commercially available CVD system at either atmospheric or reduced pressures down to 500 °C by using  $B_2H_6$  at high concentrations. The process, as described in **Chapter 2**, substantially differs from previous approaches both with respect to the low temperature used and the gas exposure conditions. The former is generally very attractive for versatile use of a doping technology, while the excessive B adsorption intentionally promoted on the Si surface, i.e. the deposition of a B-layer, is demonstrated to offer unprecedented advantages for the formation of ultrashallow and low leakage  $pn$ -junctions. Analytical techniques, such as transmission electron microscopy (TEM) and secondary ion mass spectrometry

(SIMS), in conjunction with an extensive electrical characterization are applied to investigate the material and electrical properties of the B-layers as a function of the deposition conditions. The experimental results are also validated by process and device simulations. The formation of B-layers is slower the lower the temperature and the diborane partial pressure, and mainly controlled by the exposure time at high gas flow rates that provide good conditions for segregation of boron atoms on the Si surface. While gas parameters can determine the transition from surface Si doping to B-deposition, the temperature mainly influences the final composition of the deposited film that can vary from amorphous boron ( $\alpha$ -B) to a boron-silicon compound, i.e. boron-silicide,  $(B_xSi_y)$ , for temperatures increasing from 500 °C to 800 °C. The deposition exhibits high selectivity to Si, isotropy, and uniformity for any surface topography and patterning. The time dependence of the B-layer growth is quite linear and a similar grading coefficient is observed for the boron surface density. The chemical reactivity of boron with  $HNO_3$ -based acid solutions can be used for the removal of the layer. Furthermore, the growing B-film will act as a source for boron thermal diffusion during the CVD process itself, and the crystalline Si substrate is *p*-doped up to the B solid solubility. The as-diffused active boron density is also shown to be quantitatively controlled by the exposure time. Moreover, both the relatively low deposition temperature and the absence of any defect formation, which could cause enhanced-diffusion effects, ensure junction depths lower than 10 nm even after prolonged depositions.

In **Chapter 3**, the properties of the deposited B-layers are further explored with respect to formation of high-quality, ultrashallow junctions in *p*<sup>+</sup>*n* diode configurations. Ohmic contacts, diodes, and *pnp* bipolar structures are fabricated and characterized under different  $B_2H_6$  exposure conditions. As B-deposition is commenced, the Fermi level of the exposed Si surface is rapidly shifted towards the valence band, as one would expect for electrically active *p*-type doping. This is beneficial for formation of very low-ohmic contacts on *p*-type surfaces, while *pn* diodes are formed on *n*-type Si substrates. In the latter case, the near-ideal saturation current can be tuned from high Schottky-like values to low deep-*pn*-junction-like values by increasing the deposited B-layer thickness by just a few nm. The integration of B-deposited emitters in *pnp* structures has shown that the presence of a distinct  $\alpha$ -B layer, which occurs for min-long exposures, is an effective way to suppress the electron minority carrier injection from the *n*-substrate. This results in an effective Gummel number 60 times higher than that of the diffused emitter only. The doping efficiency is also demonstrated to be superior to that in conventional B-doped Si epitaxy and comparable to  $B^+$ / $BF_2^+$  ion implants. Although for increasing thickness the series resistance through this high-resistive layer will eventually dominate the I-V behavior, processing conditions can be found where exceptionally low values of both series resistance and saturation current can be achieved. However, the high-ohmic property can be used as a means of fabricating very compact, small area, and non-linear resistors. The compatibility of the doping technique with standard Si device manufacturing is also proven. Also for the use of hard-mask materials other than  $SiO_2$  the selectivity of the B-layers to deposit only in the contact openings to the Si has been demonstrated. Furthermore, due to the excellent isotropic coverage, the B-deposition can be applied

to non-planar device schemes such as trenches and recessed-contact technologies.

Although the boron chemical concentration significantly exceeds the solid solubility at the silicon surface, for as-deposited B-layers the active dopants of the c-Si substrate is found to be essentially limited by substitutional incorporation at the deposition temperature. However, in **Chapter 4** the B-layer is demonstrated to act as a well-controlled source of dopant for solid-phase diffusion during any subsequent *in-situ* or *ex-situ* high-temperature annealing step. The presence of a sufficiently thick B-layer offers, due to its thermal stability, the additional advantage of being able to minimize boron evaporation. Thus, a higher dopant activation can be obtained with a good control of the resulting junction depth. Furthermore, the use of  $\text{B}_2\text{H}_6$  exposure and thermal anneal as post-processing gives more insights into the influence of processing parameters on the boron adsorption mechanism. In particular, at very low temperatures, hydrogen termination of the silicon surface is assumed to influence the sticking of boron atoms. In this respect, the carrier gas can play a significant role. Finally, thermal anneals are also applied to increase the doping efficiency of B-layers that act as emitters in *pnp* bipolar transistors.

The unique properties of the boron CVD deposition are exploited with great advantages in  $p^+n$  diodes fabricated at 700 °C for the integration of two distinct device technologies: varactor diodes for adaptive functions in radio frequency (RF) applications and photodiodes for detection of ultraviolet (UV) radiation. In the former case, B-deposition offers a defect-free, low-temperature process module within the silicon-on-glass (SOG) substrate-transfer technology to form one-sided  $p^+n$ -junctions that can preserve hyper-abrupt arsenic profiles needed for highly-linear tunable varactors. On the other hand, the fundamental advantages of the B-layers for use as a novel  $p^+$  front-layer in UV detectors are given by the extremely ultrashallow and highly-doped junction that is instrumental in the collection of the photogenerated carriers.

Since both devices operate in reverse biasing mode, in **Chapter 5** the electrical performance of the B-layers is investigated when reverse voltages are applied up to the expected diode breakdown limit. Device simulations demonstrate that the high electric field induced by the nm-deep  $p^+$ -junction at the anode contact edges is responsible for band-to-band tunneling current. Thus, the reverse I-V characteristics of as-deposited B-doped varactors would suffer from high leakage current and premature breakdown. Diffused  $p^+$  guard-rings are proposed as a solution to reduce the electric field crowding at the contact rim. In addition,  $n^+$  channel-stop implants are used to prevent the depletion region from extending excessively under the MOS structure formed by the anode metallization on the  $\text{SiO}_2$  isolation layer and approach regions with reduced generation-recombination lifetimes. Then, the silicon-on-glass varactor technology is illustrated along with the electrical characterization results. A noteworthy improvement of the reverse I-V performance is shown for varactor implementations with either uniform or hyper-abrupt  $1/x^2$  As profiles when  $\text{BF}_2^+$  and  $\text{P}^+$  implants are included in the process to form guard-rings and channel-stop regions, respectively. The devices have unprecedented low reverse current and an increased operating voltage range close to the theoretical breakdown limit. At the same time, the desired capacitance-voltage relationship is still preserved by the compatibility of the thermal processing steps with the As profiles.

**Chapter 6** describes the integration of B-layers in a silicon-based planar  $p^+n$  photodiode technology for radiation detection in the complete UV spectral range down to soft X-ray wavelengths. The  $B_2H_6$  exposure conditions for the formation of the sensitive surface are specifically optimized to minimize any possible quantum efficiency loss due to absorption and reflection of radiation in the front  $\alpha$ -B layer. Without compromising the optical conversion efficiency, the B-deposition can be combined with *in-situ* thermal annealing and/or selective epitaxial Si growth to reduce the series resistance of the front  $p^+$  layer. An optical coating can also be integrated to either reduce reflection losses or determine a filtering radiation pass-band. Outstanding photodiode performance is achieved, since comparison with the state-of-the-art silicon detector technology shows that B-deposited devices perform with superior electrical and optical characteristics. In fact, they exhibit an ideal diode behavior with lower dark current. Furthermore, the extremely shallow front active  $p^+$  region offers higher sensitivity over a wider UV spectral range with excellent reproducibility. In particular, they show near a theoretical responsivity at short-wavelengths that is also very stable under high-dose radiation exposure.

Finally, the main conclusions of the thesis are summarized in **Chapter 7**, which also provides recommendations for the future work. In particular, the research activity has shown that the B-layer can be seen as a new IC compatible doping material that owing to the unique properties can be both instrumental in the downscaling of bipolar/CMOS transistors and very attractive for many novel Si device configurations.

# Samenvatting

## Karakterisatie van pure boor depositie geïntegreerd in silicium diodes voor nanometerdiepte junc tie applicaties

door Francesco Sarubbi

Doterings technologie voor de formatie van zeer ondiepe en hoog gedoteerde  $p^+$ -juncties wordt continue gevraagd om de uitdagingen aan te gaan die in *front-end processing* zijn ontstaan door de agressieve miniaturisatie van de verticale dimensies voor toekomstige halfgeleider componenten. Huidige oplossingen die een alternatief vormen voor implantatie, zijn gebaseerd op *in-situ* boor (B) dotering gedurende Si/SiGe chemische dampdepositie (CVD) met gebruik van diboraan ( $B_2H_6$ ) als dotering gas. In deze context zijn er enkele studies die  $p^+$ -achtige doteringsgedrag van *n*-type (100) georiënteerde Si oppervlakken demonstreren na blootstelling aan uitsluitend  $B_2H_6$  in een zuurstofvrije atmosfeer zonder de toevoeging van extra op silaan gebaseerde brongassen. Zoals wordt geïllustreerd in **Hoofdstuk 1** vertrouwt dit dotering proces op de thermische dekompositie van het brongas, zodat het beschikbare boor zich kan vasthouden aan het oppervlak, chemisch kan reageren met silicium atomen en in het substraat kan diffunderen. In tegenstelling tot andere doterings onzuiverheden kan, door het adequaat variëren van de brongas parameters en blootstellingstijd, de reactie kinetiek ook leiden tot een significante stijging van de boor dichtheid verder dan de vaste oplosbaarheidsgrens in Si bij de gegeven verwerkings temperatuur. Er kan zich dus een boor laag vormen. Deze eigenschap is echter dusver niet onderzocht met betrekking tot de betrouwbare integratie in Si-gebaseerde componenten technologie, aangezien boor segregatie in het algemeen werd gezien als een nadeel van deze doteringsmethode.

Dit proefschrift presenteert de karakterisatie van nanometerdikke B lagen gevormd tijdens blootstelling aan diboraan in een commercieel CVD systeem bij zowel atmosferische als verlaagde druk tot temperaturen zo laag als 500 °C met behulp van hoge concentraties  $B_2H_6$ . Het proces, zoals beschreven in **Hoofdstuk 2**, verschilt aanzienlijk van vroegere benaderingen, zowel met betrekking tot de gebruikte lage temperatuur als de omstandigheden van de blootstelling aan het gas. Dit eerste is in het algemeen erg aantrekkelijk voor veelzijdig toepasbaarheid van een doting techniek, terwijl de excessieve opzettelijk bevorderde B adsorptie op het Si opper-

vlak, i.e. de depositie van een laag B, ongekende voordelen blijkt te bieden voor de vorming van zeer ondiepe en lage lek *pn*-juncties. Analytische technieken zoals transmissie elektronenmicroscopie (TEM) en secundaire ionen massaspectrometrie (SIMS), samen met een extensieve elektrische karakterisatie zijn toegepast om het materiaal en de elektrische eigenschappen van de B lagen te onderzoeken als functie van de depositie omstandigheden. De experimentele resultaten zijn ook gevalideerd door proces en component simulaties. De formatie van lagen B is trager bij een lagere temperatuur of partiële diboraan druk, en wordt voornamelijk gecontroleerd door de blootstellingstijd bij hoge gasstromen, die goede voorwaarden bieden voor de segregatie van boor atomen op het Si oppervlak. Terwijl de gas parameters de transitie van Si oppervlakte dotering tot B depositie kunnen bepalen, beïnvloedt de temperatuur vooral de uiteindelijke compositie van de gedeponeerde film welk kan variëren van amorf boor ( $\alpha$ -B) tot een boorsilicium legering, i.e. boorsilicide ( $B_xSi_y$ ), voor temperaturen stijgend van 500 °C tot 800 °C. De depositie toont hoge selectiviteit voor Si, isotropie en uniformiteit voor elke oppervlakte topografie en patroon. De tijd afhankelijkheid van de B laag groei is tamelijk lineair en een soortgelijke gradeerings coëfficiënt is waargenomen voor de boor oppervlakte dichtheid. De chemische reactiviteit van boor met op  $HNO_3$  gebaseerde zuuroplossingen kan worden gebruikt voor het verwijderen van de laag. Bovendien zal de groeiende B film fungeren als een bron voor thermische diffusie van boor tijdens het CVD proces zelf, en het kristallijne Si substraat is *p*-gedoteerd tot de vaste oplosbaarheid van B. Het is ook aangetoond dat de gediffundeerde actieve boor dichtheid kwantitatief gecontroleerd wordt door de blootstellingstijd. Bovendien verzekeren zowel de relatieve lage depositie temperatuur en de afwezigheid van enig defekt formatie, welk versterkte diffusie effecten kan veroorzaken, junc tie dieptes van minder dan 10 nm, zelfs na langdurige deposities.

In **Hoofdstuk 3** worden de eigenschappen van gedeponeerde B lagen verder verkend met betrekking tot de formatie van hoge kwaliteit, zeer ondiepe junc ties in *p<sup>+</sup>n* diode configuraties. Ohmse contacten, diodes en *pnp* bipolaire structuren zijn gefabriceerd onder verschillende condities van  $B_2H_6$  blootstelling. Zodra de B depositie begint schuift het Fermi niveau van het blootgestelde Si oppervlak snel richting de valentieband, zoals men zou verwachten van elektrisch actieve *p*-type dotering. Dit is gunstig voor de formatie van zeer laag-ohmige contacten op *p*-type oppervlakken, terwijl *pn* diodes gevormd worden op *n*-type Si substraten. In het laatste geval kan de bijna ideale saturatiestroom afgestemd worden van hoge Schottky-achtige waarden tot lage diepe *pn*-junctie achtige waarden door de gedeponeerd B laagdikte te verhogen met maar een paar nm. De integratie van B gedeponeerd emitters in *pnp* structuren heeft laten zien dat de aanwezigheid van een duidelijke  $\alpha$ -B laag, die optreedt bij minuten lange deposities, een effectieve manier is om de elektronen minderheidsladingen drager injectie van het *n*-type substraat te onderdrukken. Dit resulteert in een effectief Gummel getal dat 60 keer hoger is dan dat van de alleen gediffundeerde emitter. Het is ook aangetoond dat de dotering efficiëntie superieur is aan die van conventionele B-gedoteerde Si epitaxie en vergelijkbaar met  $B^+$ / $BF_2^+$  ionenimplantatie. Hoewel voor toenemende dikte de serie weerstand door deze hoog-ohmse laag uiteindelijk het I-V gedrag zal domineren, kunnen er condities worden gevonden waarbij uitzonderlijk lage waarden voor zowel de serie weerstand als saturatiestroom

kunnen worden behaald. Echter, de hoog-ohmse eigenschap kan worden gebruikt als een middel om zeer compacte, kleine en niet-lineaire weerstanden te fabriceren. De compatibiliteit van de dotoring techniek met standaard Si component vervaardigingsmethoden is ook aangetoond. Ook voor het gebruik van andere harde masker materialen dan  $\text{SiO}_2$  is de selectiviteit van de B laag om alleen gedeponeerd te worden in de contact openingen naar het Si gedemonstreerd. Bovendien kan de B depositie, door de uitstekende isotropische dekking, worden toegepast op niet-planaire component configuraties, zoals uitgeëtste sleuven en verzonken-contacten.

Hoewel de chemische concentratie van boor de vaste oplosbaarheid aan het Si oppervlak significant overschrijdt, blijkt dat de actieve dotoring van het c-Si substraat vanuit gedeponeerde B lagen in wezen gelimiteerd wordt door substitutionele opname bij de depositie temperatuur. In **Hoofdstuk 4** wordt echter gedemonstreerd dat de B laag kan optreden als een goed gecontroleerde bron van dotoring voor vaste-fase diffusie gedurende elke opeenvolgend *in-situ* of *ex-situ* hoge temperatuur gloeistap. De aanwezigheid van een toereikende dikke B laag biedt het extra voordeel dat het, vanwege zijn thermische stabiliteit, de boor verdamping kan minimaliseren. Er kan dus een hogere dotoring activatie worden behaalt met een goede controle over de resulterende juncie diepte. Bovendien geeft het gebruik van  $\text{B}_2\text{H}_6$  blootstelling en thermisch gloeien als nabewerking meer inzicht in de invloed van de verwerkings parameters op de boor adsorptie mechanismen. Er wordt met name verondersteld dat bij zeer lage temperaturen waterstof beïndiging van het silicium oppervlak het kleven van boor atomen beïnvloed. In dit opzicht kan de draaggas een grote rol spelen. Tenslotte wordt thermisch gloeien ook toegepast om de dotorings efficiëntie van B lagen welke fungeren als emitters in *pnp* bipolaire transistoren te verhogen.

De unieke eigenschappen van de boor CVD depositie worden met grote voordelen uitgebuit in  $p^+n$  diodes gefabriceerd bij 700 °C voor de integratie van twee verschillende component technologieën: varicap diodes voor adaptieve functies in radio frequentie (RF) applicaties en fotodiodes voor de detectie van ultraviolette (UV) straling. In het eerste geval biedt B depositie een defect vrije, lage temperatuur procesmodule voor silicium-op-glas (SOG) substraat overdracht technologie waarmee enkelzijdige  $p^+n$ -juncties gevormd kunnen worden met behoud van hyper abrupte arseen profielen die nodig zijn voor het maken van zeer lineaire afstembare varicaps. In het andere geval worden de fundamentele voordelen van de B lagen, ingezet voor gebruik als een nieuwe  $p^+$  voorkant laag in UV detectoren voor welke de extreme ondiepe en hoog gedoteerde juncie van belang is bij de collectie van fotogegeneerde ladingsdragers.

Aangezien beide componenten in sperrichting opereren wordt in **Hoofdstuk 5** de elektrische prestaties van de B lagen onderzocht wanneer sperspanningen worden aangelegd tot de verwachte diode doorslags limiet. Component simulaties demonstreren dat het sterke elektrische veld geïnduceerd door de nm diepe  $p^+$ -juncie aan de anode contactranden verantwoordelijk is voor een band naar band tunnel stroom. De I-V sperkarakteristieken van de gedeponeerde B gedoteerde varicaps lijden dus aan hoge lekstromen en premature doorslag. Gediffuseerde  $p^+$  beschermringen worden voorgesteld als een oplossing om elektrisch veldverdringing aan de contactrand te verminderen. Daarnaast worden  $n^+$  kanaalstop implantaten gebruikt om te voorkomen dat de depletie regio excessief uitbreid onder de MOS structuur gevormd

door de anode metallisatie op de  $\text{SiO}_2$  isolatielaag en regio's nadert met gereduceerde generatie-recombinatie levensduur. Daarna wordt de silicium-op-glas varicap technologie geïllustreerd samen met resultaten van de elektrische karakterisatie. Een opmerkelijke verbetering van de sper I-V prestaties wordt getoond voor varicap implementaties met óf uniforme óf hyper abrupte  $1/x^2$  As profielen, wanneer  $\text{BF}_2^+$  en  $\text{P}^+$  implantaten worden opgenomen in het proces voor respectievelijk de formatie van beschermringen en kanaalstop regio's. De componenten hebben een ongekend lage sperstroom en een vergroot werkspanning bereik dicht bij de theoretische doorslags limiet. Tegelijkertijd is de gewenste capaciteit-spanning relatie nog steeds bewaard door de compatibiliteit van de thermische verwerkingsstappen met de As profielen.

**Hoofdstuk 6** beschrijft de integratie van B lagen in een op silicium gebaseerd planaire  $p^+n$  fotodiode technologie voor straling detectie in het complete UV spectrum tot de golflengte van zwakke röntgenstraling. De  $\text{B}_2\text{H}_6$  blootstellings condities voor de formatie van het gevoelige oppervlak zijn specifiek geoptimaliseerd om elk mogelijk kwantum effectiviteit verlies door de absorptie en reflectie van straling in de voorste  $\alpha$ -B laag te minimaliseren. Zonder de optische conversie efficiëntie te comprimeren kan de B depositie worden gecombineerd met *in-situ* thermisch gloeien en/of selectieve epitaxiale Si groei om de serie weerstand van de voorste  $p^+$  laag te reduceren. Een optische coating kan ook worden geïntegreerd om de reflectie verliezen te reduceren, of een filterende doorlaatband voor straling te bepalen. Uitstekende fotodiode prestaties zijn bereikt, aangezien vergelijking met een *state-of-the-art* silicium detector technologie aantoont dat B gedeponeerde componenten presteren met superieure elektrische en optische kenmerken. In feite vertonen ze ideaal diode gedrag met lagere *dark current*. Bovendien biedt de extreem ondiepe voorste actieve  $p^+$  regio hogere gevoeligheid over een bredere UV spectrale band met uistekende reproduceerbaarheid. In het bijzonder tonen ze een bijna theoretische respons bij korte golflengten welke ook erg stabiel is na blootstelling aan een hoge dosis straling.

Tenslotte worden de voornaamste conclusies van het proefschrift samengevat in **Hoofdstuk 7**, welk ook aanbevelingen voor toekomstig werk bevat. Met name heeft het onderzoek aangetoond dat de B laag gezien kan worden als een nieuw IC compatibel dotering materiaal dat als gevolg van de unieke eigenschappen zowel bevorderlijk kan zijn in het miniaturiseren van bipolair/CMOS transistoren en erg aantrekkelijk kan zijn voor vele nieuwe Si component configuraties.

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