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Toth, N. G., & Makinwa, K. A. A. (2026). A Background-Calibrated NPN-Based Temperature Sensor with 0.05°C (3σ) Inaccuracy from -70°C to 125°C. In *2026 IEEE International Solid-State Circuits Conference, ISSCC 2026* (pp. 370-372). (Digest of Technical Papers - IEEE International Solid-State Circuits Conference; Vol. 69). IEEE. https://doi.org/10.1109/ISSCC49663.2026.11409074

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21.4 A Background-Calibrated NPN-Based Temperature Sensor with 0.05°C (3σ) Inaccuracy from -70°C to 125°C

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Abstract

In this work, an NPN-based temperature sensor is presented that introduces a background-calibration scheme to correct all current-domain errors in its front-end. It achieves an inaccuracy of 0.05°C (3σ) from -70°C to 125°C (RIA=0.05%) after a one-point trim, which represents the state-of-the-art energy efficiency (100fJ·K²) and power supply sensitivity (PSS) (0.004°C/V).

After a 1-point trim, BJT-based temperature sensors can be very accurate, with many designs achieving better than 0.2°C inaccuracy from -55°C to 125°C [1]. However, achieving sub-0.1°C accuracy has proven extremely challenging, having been reported only once before according to a comprehensive survey [1]. This is mainly due to the difficulty in completely correcting for errors caused by the decrease in BJT current gain (β) at low temperatures and the exponential increase of leakage currents at high temperatures. This paper proposes an NPN-based temperature sensor that uses a background calibration technique to correct such errors over a wide temperature range. It achieves a 1-point trimmed inaccuracy of 0.05°C (3σ) from -70°C to 125°C (RIA=0.05%), which represents the state of the art. In addition, it also achieves state-of-the-art energy efficiency (100fJ·K²) and power supply sensitivity (PSS) (0.004°C/V). Compared to [2], it is 78× more energy efficient, and, compared to more recent designs [3-5], it is 2× more accurate and has 2.5× better PSS.

A simplified block diagram of the proposed temperature sensor is shown in Fig. 21.4.1. A PTAT current (I_{PTAT}) is generated by forcing the difference in the base-emitter voltages (ΔV_{BE}) of two NPNs ($Q_{1,2}$) across a resistor (R_1). This current is then mirrored (I_1) to the virtual ground of the 1st integrator of a ΔΣ-modulator, which is also used to generate a CTAT current (I_2) by forcing V_{BE} across a resistive DAC (R_2). The modulator's bitstream output then drives the RDAC such that, on average, I_2 exactly balances I_1. As a result, the bitstream average (μ_1) will be a function of temperature [3].

In the proposed sensor, a significant source of I_1-error is the spread in the R_2/R_1 ratio. In [6], this was partially corrected with the help of a room-temperature (RT) calibration. However, this does not correct for its temperature dependence, e.g., due to the finite R_{ON} of the RDAC switch. Another source of I_1-error is the base current (I_{B1}) of Q_1, which is most problematic at low temperatures. Although this can be mitigated by the β-compensation technique proposed in [6], the dependence of β on collector current density still causes a residual error related to $\Delta\beta = \beta_{Q2} - \beta_{Q1}$. The net leakage current (I_L) of the junction-isolated source/drain regions of the PMOS current mirrors and the collectors of the NPNs is yet another source of error, especially at high temperatures. In consequence, I_1 can be expressed as $(1+\varepsilon)\cdot I_{PTAT}$, where ε is a temperature-dependent parameter that contains all sources of error (Fig. 21.4.1).

In this work, the error component (1+ε) is extracted by a background-calibration (B-CAL) technique. This involves performing a calibration conversion in which the 1st integrator's virtual ground is switched to ΔV_{BE}, instead of V_{BE}, so that $I_{2,cal} = \Delta V_{BE}/R_2$ (Fig. 21.4.1, bottom). Since $I_{2,cal} < I_1$, charge balancing is performed by using a current DAC (IDAC) to switch I_1, while constantly enabling the RDAC to keep $I_{2,cal}$ constant. As a result, the modulator's bitstream average (μ_2) will now be equal to $1/(R_2/R_1\cdot(1+\varepsilon))$. This can then be used to digitally trim μ_1 by simply computing $\mu_{TRIM} = \mu_1\cdot\mu_2$, which only depends on $\Delta V_{BE}/V_{BE}$ and is thus insensitive to any I_1-error over PVT.

A simplified block diagram of the proposed sensor is shown in Fig. 21.4.2. Q_1 and Q_2 are biased at a current ratio of 1 and an area ratio of 7, which, in combination with R_1 (=130kΩ), results in I_{PTAT} = 390nA at room temperature (RT). A feedback loop containing transistor M_1 and a base-current mirror sets the collector of Q_2 to $V_{GS,M1}$ (~V_{BE}), while an amplifier (A_1) drives the PMOS collector-current mirrors to equalize both collector voltages. To save power, I_{PTAT} is mirrored to the ADC with a 2:1 ratio. In this work, R_2/R_1=13, and so $\mu_1 = 6.5\cdot\Delta V_{BE}/V_{BE}$, which ranges from 0.24 to 0.92 from -70°C to 125°C. Since the RDAC is quite large (R_2=1.7MΩ), it is segmented to minimize switching transients due to the charge stored in its parasitic capacitance [3]. During calibration, when I_1 is switched, switching transients are minimized by dumping unused current into $2\cdot R_1$, thus maintaining the IDAC output at ~ΔV_{BE}. Lastly, the mismatch of the NPNs and PMOS current mirrors is mitigated by barrel-shifting their unit elements at $f_s/320$ and $f_s/160$, respectively.

For a maximum calibration error of 0.01°C (3σ) after an RT trim, the resolution of μ_2 must be less than 30ppm (σ). Furthermore, the errors in $I_{2,cal}$, e.g. due to DAC switch leakage, must be less than 1.2pA (σ) at 125°C. During calibration, $\mu_2 \approx 1/6.5 = 0.15$, which means that the noise of I_1 is averaged for only 15% of the total conversion time. Since the modulator enforces charge balancing, more noise averaging, and thus, more resolution can be obtained by increasing $I_{2,cal}$ (= $\mu_2\cdot I_1$). To accomplish this, R_2 is folded into 2 equal segments that are connected in parallel (Fig. 21.4.2). This increases $I_{2,cal}$ by 4× and proportionally increases the averaging of I_1's noise. This, in turn, results in a 4× reduction in the conversion time needed to achieve a given resolution, and in the sensitivity of $I_{2,cal}$ to DAC switch leakage. It is also very accurate; a segment mismatch of 0.12% (σ) results in only a small additional error ($\Delta R_2/R_2$ ~ 1ppm (σ)) after folding.

The RDAC consists of 4 resistor segments and 5 HVT NMOS switches. The R_{ON} of these switches, as well as the R_{ON} of the NPN DEM switches, will introduce temperature-dependent errors in the R_2/R_1 ratio. To reduce these errors, the switches are driven by boosted clocks generated by level-shifters (LS) connected to a high-voltage rail (V_H). As shown in Fig. 21.4.2 (right), V_H is generated by a regulated charge-pump (RCP), which consists of two cascaded voltage doublers that boost the V_{GS} (~0.95V) of an I_{PTAT}-biased diode-connected HVT NMOS by 4×. V_H thus tracks the HVT NMOS process corner, making R_{ON} robust to PVT variations. This allows the use of smaller DEM and DAC switches, which reduces their leakage and charge injection. In simulations, the RCP reduces R_{ON}-spread by about 2.5× while consuming only 85nA (at RT).

The ΔΣ-modulator employs a 2nd-order CIFF loop filter, which consists of a continuous-time 1st integrator and a compact switched-capacitor 2nd integrator. It is clocked at f_s = 50kHz. The 1st integrator is based on a current-assisted two-stage amplifier (A_2) consisting of a folded cascode input stage and a source-follower output stage [3]. Its high DC gain and GBW (>78dB and >1.3MHz) ensure a stable virtual ground, reducing errors in I_{CTAT} and $I_{2,cal}$. To achieve less than 30ppm (σ) error during calibration, the offset of A_2 must be less than 1μV (σ) at -70°C. To ensure this, nested chopping is applied, with the inner choppers clocked at f_s, while the outer choppers are clocked at $f_s/320$. During calibration, the bias current of A_2 is doubled to increase its GBW (> 2.5MHz) and reduce settling errors. In simulation, such errors correspond to equivalent errors of <1mK (σ) during a regular conversion and <20ppm (σ) during calibration.

The sensor was fabricated in a 0.18μm CMOS process and occupies 0.063mm² (Fig. 21.4.7). It draws 1.9uA (61% front-end, 33% ADC, 6% digital) from a supply ranging from 1.4V to 2.2V. Two identical sensors were placed on each die to enable differential temperature measurements, which cancels the effect of ambient temperature drift. The sinc² decimation filter was implemented off-chip for flexibility.

To measure the sensor's resolution, a long bitstream (2^{21} bits) is decimated by a sinc² filter while the modulator is operated in free-running mode. As shown in (Fig. 21.4.3, top left), the sensor becomes thermal-noise limited for T_{conv} > 30ms and remains immune to drift and 1/*f* noise up to T_{conv} < 5s. With T_{conv} = 38.4ms, the sensor achieves 1mK (σ) resolution, resulting in a resolution FoM of 100fJ·K². Figure 21.4.3 (top right) shows the resolution during calibration expressed in ppm (σ). As expected, folding R_2 reduces the conversion time required to achieve 30ppm (σ) by 4×: from 76.8ms to 19.2ms, thus significantly reducing the calibration overhead. If calibration is performed after every conversion, which is not strictly necessary, the resolution FoM increases to 2pJ·K² due to the increased noise and conversion time.

30 sensors on 15 dies in ceramic DIL packages were characterized from -70°C to 125°C in a temperature-controlled oven. To suppress ambient temperature drift, the samples were placed in good thermal contact with a large aluminum block. The decimated data of a regular conversion (μ_1) before and after B-CAL is shown in Fig. 21.4.3 (bottom left). The results of calibration ($1/\mu_2$) are shown in Fig. 21.4.3 (bottom right) with β-compensation [6] both enabled and disabled. It can be observed that (Δ)β-errors at low temperatures and I_L-errors at high temperatures cause significant deviations in $1/\mu_2$ from the expected value of 6.5.

After a batch calibration, the master curves in Fig. 21.4.3 (bottom left) are mapped to a fixed 5th-order polynomial. After an RT trim and an RT calibration, the resulting temperature spread is 0.4°C (3σ) (Fig. 21.4.4, top left), which is mainly limited by β-error at low temperatures. This improves to 0.1°C (3σ) with β-compensation (Fig. 21.4.4, top right), but is still limited by Δβ and I_L-errors. Employing the proposed B-CAL technique results in a state-of-the-art 0.05°C (3σ) inaccuracy (Fig. 21.4.4, bottom left). Similar results are obtained with β-compensation, demonstrating its redundancy after applying B-CAL.

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Another low-cost calibration technique is voltage calibration (V-CAL) [7]. This obviates the need for calibrating at a known temperature by leveraging the accuracy of ΔV_{BE}. In this design, V-CAL can be implemented by connecting an external voltage reference (V_{EXT}) to the virtual ground of the 1st integrator (Fig. 21.4.2). As a result, the bitstream average is $6.5 \cdot \Delta V_{BE}/V_{EXT}$, from which ΔV_{BE}, and thus the die temperature, can be determined. For the proposed sensor, V-CAL results in an inaccuracy of 0.08°C (3σ), which is 2× better than previously reported [2,8,9].

The measured PSS of the proposed sensor is shown in Fig. 21.4.5. With V_H fixed at $2 \cdot V_{DD}$ and without B-CAL, the PSS is 0.43°C/V from 1.4V to 2.2V (top left). B-CAL reduces the temperature dependence of R_2/R_1 and thus improves the PSS to 0.15°C/V (top right). Using the RCP improves the PSS significantly, to 0.025°C/V without B-CAL (bottom left) and even to 0.004°C/V with B-CAL (bottom right), which is the lowest reported in [1].

In Fig. 21.4.6, the performance of this sensor is benchmarked against state-of-the-art BJT-based temperature sensors. It achieves the lowest 1-point trimmed inaccuracy (0.05°C (3σ) from -70°C to 125°C), the lowest voltage calibrated inaccuracy (0.08°C 3σ from -70°C to 125°C), and the lowest PSS (0.004°C/V), while its area (0.063mm²) and energy efficiency (100fJ·K²) are in line with the state-of-the-art. This performance is enabled by the combination of an accurate current-mode front-end and the proposed background calibration technique.

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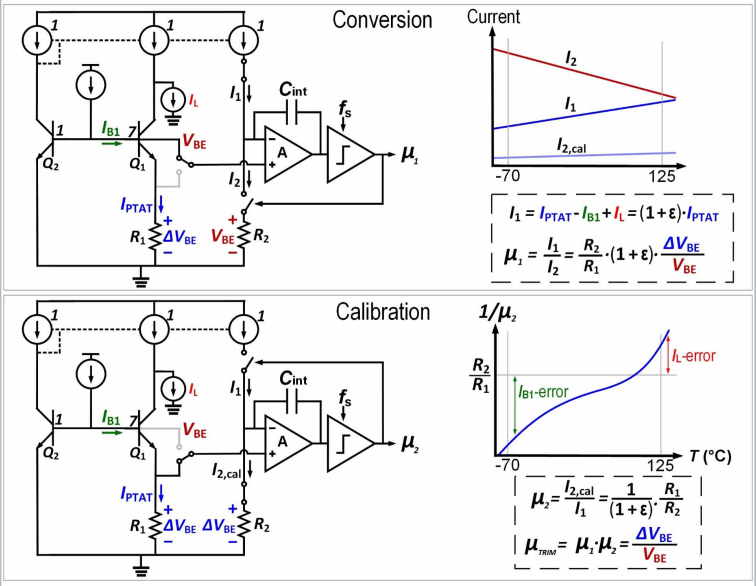

Figure 21.4.1: Operation of the proposed background calibration (B-CAL) technique.

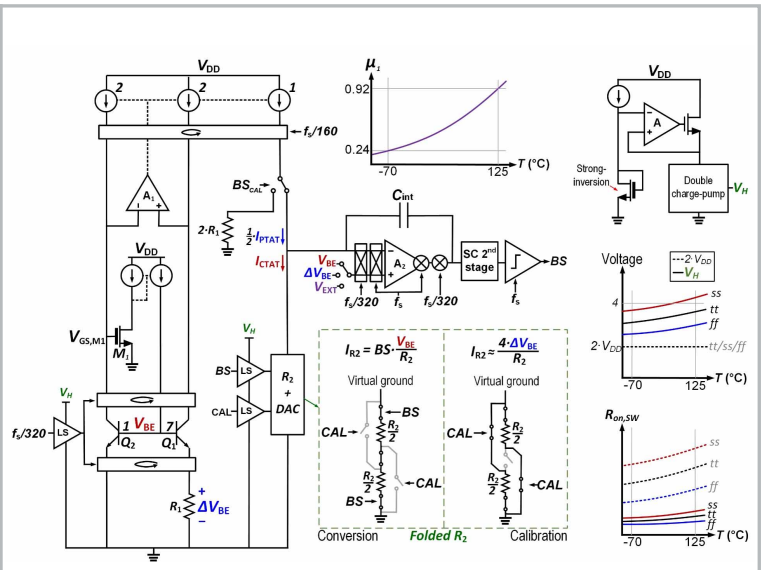

Figure 21.4.2: Block diagram of the proposed sensor (left), the RCP and its effect on the R_{ON} of the HVT NMOS switches (right).

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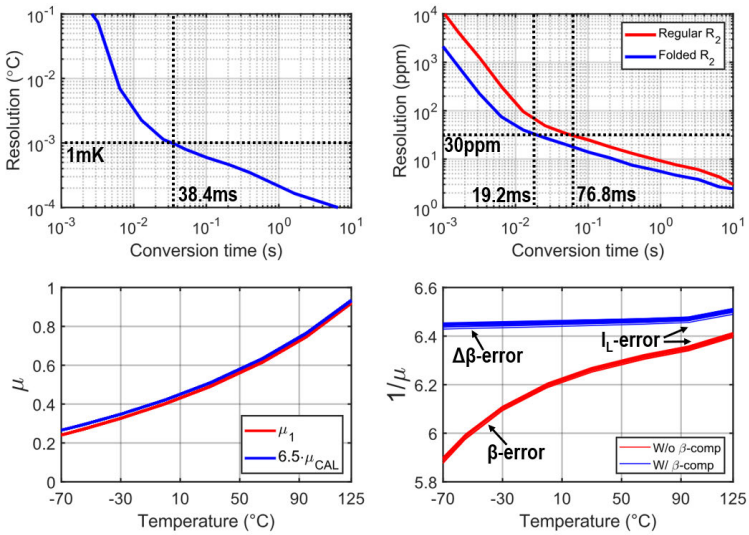

Figure 21.4.3: Resolution vs. conversion time during conversion (top left) and calibration (top right), and the decimated data over temperature during conversion (bottom left) and calibration (bottom right).

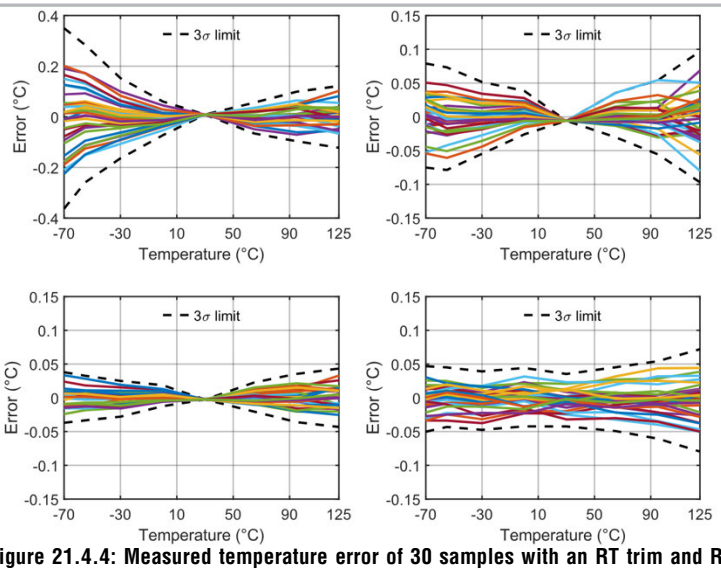

Figure 21.4.4: Measured temperature error of 30 samples with an RT trim and RT calibration (top left), with an RT trim, RT calibration and β-compensation (top right), with an RT trim and B-CAL (bottom left), with a voltage calibration and B-CAL (bottom right).

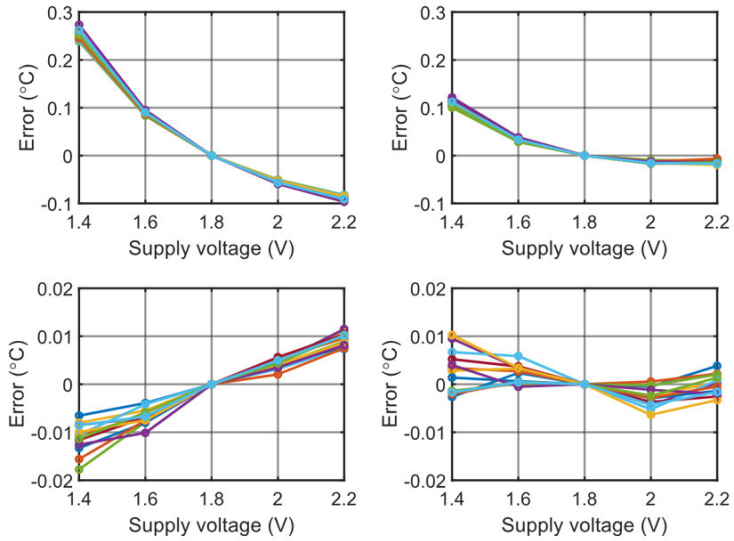

Figure 21.4.5: PSS without B-CAL and RCP (top left), with B-CAL and without RCP (top right), without B-CAL and with RCP (bottom left), and with B-CAL and RCP (bottom right).

	Wang JSSC'22 [10]	Shalmany ISSCC'20 [5]	Tang JSSC'23 [4]	Yousefzadeh JSSC'17 [2]	Toth ISSCC'25 [3]	This work
Sensor type	PNP	NPN	PNP	PNP	NPN	**NPN**
Technology	0.18μm	0.11μm	0.18μm	0.16μm	0.18μm	**0.18μm**
Chip area [mm²]	0.42	0.2	0.25	0.16	0.05	**0.063**
Supply current [μA]	2.5	550	0.85	4.6	1.8	**1.9**
Supply voltage [V]	1.5 to 2	1.125	0.95 to 1.4	1.5 to 2	1.4 to 2.2	**1.4 to 2.2**
Supply sensitivity [°C/V]	0.44	-	0.2	0.01	0.025	**0.004**
Temperature range	-50°C to 180°C	-35°C to 95°C	-55°C to 125°C	-55°C to 125°C	-70°C to 125°C	**-70°C to 125°C**
3σ Inaccuracy [°C] after a 1-pt trim	±0.45	-	±0.15	±0.06	±0.1	**±0.05**
Relative inaccuracy [%]	0.39	-	0.17	0.07	0.11	**0.05**
3σ Inaccuracy [°C] after voltage calibration	-	-	-	±0.17[2]	-	**±0.08**
Resolution [mK]	17.6	0.72	1.8	15	0.79	**1**
Conversion time [ms]	8.3	0.65	128	5	51	**38.4**
Resolution FoM[1] [fJ·K²]	9700	190	340	7800	80	**100**

[1] FoM = Energy/Conversion · Resolution²
[2] From a single batch, estimated from Fig. 13

Figure 21.4.6: Performance summary and comparison table.

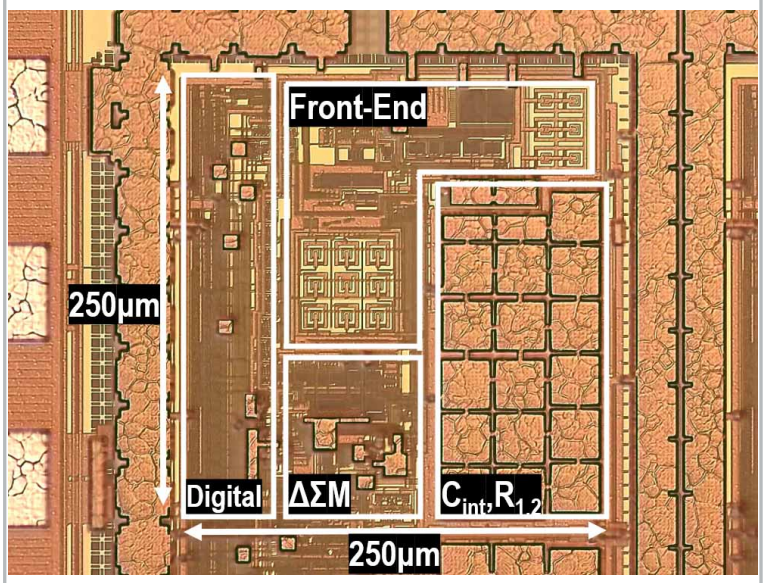

Figure 21.4.7: Die micrograph of the sensor.

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