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Evdokia Pilavaki , *Student Member, IEEE*, Virgilio Valente , *Member, IEEE*, and Andreas Demosthenous , *Fellow, IEEE*

Abstract—**Point-of-care (POC) systems for the detection of infectious diseases are in great demand especially in developing countries. Lateral flow immunoassays are considered ideal biosensors for POC diagnostics due to their numerous advantages. However, to quantify their results a low power, robust electronic reader is needed. A low power CMOS image sensor is presented that can be used in quantitative lateral flow immunoassay readers. It uses a single low power processing capacitive transimpedance amplifier architecture which includes noise cancellation. A chip containing 4 × 64 pixels was fabricated in CMOS 0.35-μm technology. With uniform illumination at 525 nm and 67 frames/s the chip has 1.9 mV$_{\text{rms}}$ total output referred noise and a total power consumption of 21 μW. In tests with lateral flow immunoassays the chip detected concentrations of influenza A nucleoprotein from 0.5 ng/mL to 200 ng/mL.**

Index Terms—**CMOS image sensor, capacitive transimpedance amplifier, lateral flow immunoassays, point-of-care.**

I. INTRODUCTION

INFECTIOUS diseases like HIV (human immunodeficiency virus), tuberculosis and influenza are among the deadliest causes of death especially in developing countries. Abundant diagnostic systems can been found in developed countries, but this is not the case for the poorest parts of the world. The main reasons are that these systems are usually bulky and difficult to carry around in the field, they are expensive and specially trained personnel are required to operate them. Handheld point-of-care (POC) diagnostic systems can bridge this gap. They must be robust, easy to operate, rapid, low cost and have good accuracy and low power consumption.

Lateral flow immunoassays (LFIAs) as shown in Fig. 1 are biosensors that can be used for the detection of proteins which are biomarkers of diseases [1], [2]. If the analyte of interest is present in the sample while it flows along the LFIA strip, it will initially bind with the conjugated gold nanoparticles

and then again bind with the antibodies in the test band. The increase of gold nanoparticles in the test band generate the color test line, indicating that the sample is positive. The intensity of the test line is directly related to the concentration of existing analyte in the fluid sample [2]. The control line is used for confirmation of the correct operation of the tests. Although by visual observation of the strip qualitative results can be obtained, this is not the case when the test line is very faint or quantification is required. Thus, an electronic reader is required for the quantification of the analyte in the sample and the detection of low concentrations by reading the intensity of the color test line.

The most common electronic readers use the camera of a mobile phone to take a photograph of the strip [3]. Then the photograph is processed either on site using a specially designed application and mobile phone resources or it is sent to a healthcare center for processing off-site (telemedicine) [4]. However, both these solutions have reproducibility and compatibility issues between the various models of mobile phones which have different camera specifications. In addition, mobile phone based readers have standardization and regulatory issues when used for biomedical sensing applications [5]. Another type of reader is based on the use of a single photodiode that is fixed to detect the light at the position where the test line is expected to be. However, these systems are susceptible to positioning displacement errors [6]. Also, optical components such as lenses and light splitters are often added in these systems to improve their sensitivity, but this can make the system susceptible to damage when carried around in the field.

The proposed reader uses a CMOS image sensor (CIS) that is specifically designed to provide a low cost solution for this application. An appropriate number of pixels is used in contrast to a mobile phone CIS with millions of pixels. Consequently, the total power consumption of the CIS and the processing of its output signals is less. The system uses a new compact pixel design achieving low noise and high SNR for detection of the signal from the LFIA, while operating in subthreshold for power reduction. No moving parts are required and no optical accessories are used in the system making it robust and very suitable as a POC reader. This brief is an extension of [2]. It includes measured results of a fabricated CIS chip and its successful application to the detection of Influenza A nucleoprotein using LFIAs.

The rest of this brief is organized as follows: Section II describes the chip architecture. In Section III measurements from the fabricated chip are presented and tests using LFIAs. Section IV concludes this brief.

E. Pilavaki and A. Demosthenous are with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, U.K. (e-mail: evdokia.pilavaki.13@ucl.ac.uk; a.demosthenous@ucl.ac.uk).

V. Valente was with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, U.K. He is now with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: v.valente@tudelft.nl).

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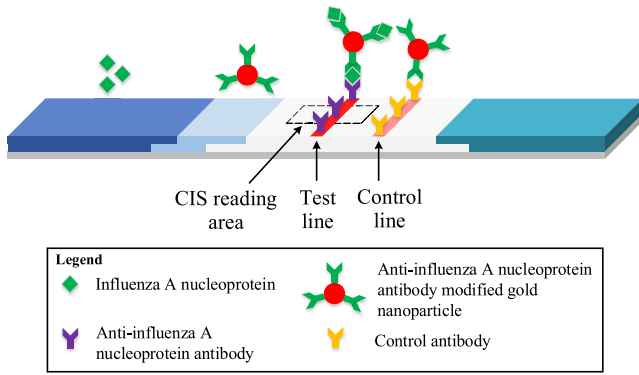
Fig. 1. LFIA for the detection of Influenza A nucleoprotein. The dashed box indicates the area of interest where the CIS is be used for measurements.
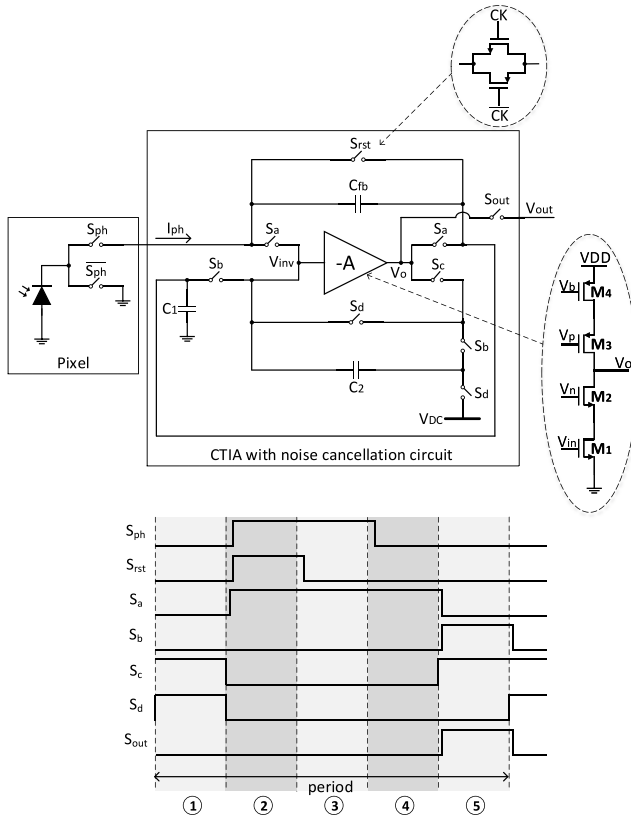

Fig. 2. Schematic of the pixel and processing architecture, and timing diagram.

Fig. 3. Simulation of the CTIA in Fig. 2 for two different photocurrents at node V_o The circled numbers indicate the five different phases required for the processing of the photocurrent. In phase 5 the S_{out} pulse is enabled allowing the voltage to exit the processing circuit (V_{out}). The simulations used $T_{int} = 50$ μs and $V_{DC} = 2$ V and $I_{ph} = 50$ pA and $I_{ph} = 100$ pA. The higher the photocurrent the lower the output voltage based on (3).

output voltage V_{int} of the transconductor is

$$V_{int} = \frac{1}{C_{fb}} \int I_{ph} dt. \tag{1}$$

The CIS can then detect low values of I_{ph}. For example for $C_{fb} = 10$ fF, $I_{ph} = 50$ pA and integration time $T_{int} = 50$ μs, $V_{int} = 0.25$ V.

In Fig. 2 all the switches are complementary for minimum charge injection [2], [7]. Transistors M_1–M_4 operate in subthreshold and are biased at 10 nA.

Read noise due to thermal and flicker readout circuit noise, reset noise due to *KT/C* noise from the feedback switch and fixed pattern noise (FPN) due to device mismatches are commonly found in CISs affecting their performance [8]. The proposed processing circuit in Fig. 2 implements the CTIA architecture with noise cancellation reusing the same amplifier for both operations to facilitate very low power consumption. As shown in Fig. 2 five phases are used to generate a voltage at the output node V_{out} in response to the incident photons at the input. In phase 1 the charge stored on C_2 is $V_{inv} - V_{DC}$, where V_{DC} is an external reference dc voltage level and V_{inv} is the inverse voltage level from the amplifier. In phases 2 and 3 the reset and integration operations are performed respectively, similar to a conventional CTIA topology. In phase 4 the integrated voltage is held constant and stored on C_1.

Subtraction of the charges is performed in phase 5. The output voltage V_{out} is given by

$$V_{out} = V_{DC} + V_{inv} - V_{int}. \tag{2}$$

where V_{int} is the integrated voltage as described in (1) plus the V_{inv}. This is because the photocurrent in CTIA starts to integrate form the V_{inv} level. This results in an output voltage independent of the V_{inv} voltage level as in (3). Fig. 3 shows the voltage at the node V_o for all the 5 stages, where

$$V_{out} = V_{DC} - \frac{I_{ph} \times T_{int}}{C_{fb}}. \tag{3}$$

The FPN related to process and mismatch variations has been examined using Monte Carlo analysis [9] in Fig. 4 for both the proposed architecture and the conventional CTIA pixel architecture. The conventional CTIA pixel without

II. CHIP ARCHITECTURE

The processing circuit for measuring the photocurrent uses a capacitive transimpedance amplifier (CTIA) architecture [2]. It is based on a single-stage transconductor amplifier shown circled in Fig. 2. The available drain current to M_1 is defined by bias voltage V_b and M_4 (chosen as 10 nA). The initial dc value of the gate of M_1 is set by short-circuiting its output to its input by switch S_d. The value is thus defined by the drain current of M_4. This voltage is connected to a selected (inversely biased) photodiode by switches. When the reset switch S_{rst} opens, the diode photocurrent I_{ph} charges the feedback capacitor C_{fb} [7]. By the choice of a small value capacitor, the
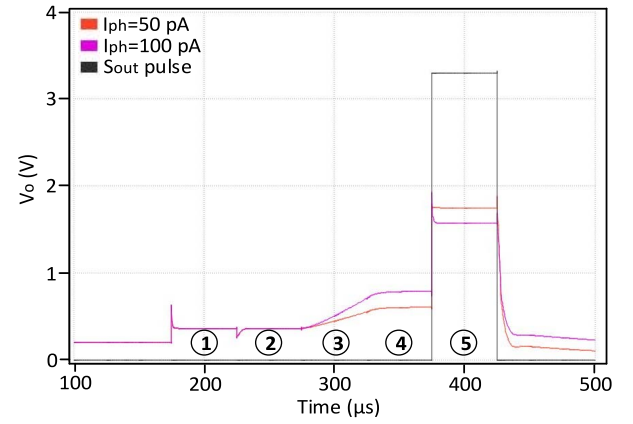
TABLE I
COMPARISON OF CIS FOR BIOSENSING APPLICATIONS

| Reference	[11]	[7]	[12]	[13]	[14]	[15]	This work
Application	Fluorescent contact imaging	Brain spectroscopic imaging	Fluorescence imaging	Micro-computed tomography	Contact imaging	Fluorescence lifetime microscopy	Reader for LFIAs
CMOS technology	0.35 μm	0.35 μm	0.5 μm	0.18 μm	0.5 μm	65 nm	0.35 μm
Array size (pixels)	128 × 128	144 × 144	132 × 124	256 × 256	96 × 96	32 × 32	4 × 64
Fill factor (%)	28	26	42	37	17	37	18
Read noise (mV$_{rms}$)	-	1.9	0.82	3.1	2.5	-	1.9
SNR (dB)	-	49	44	-	-	-	50
Frames rate (fps)	30	60	70	1500	-	20	67
Power per pixel (μW)	1.59	4.16	20.16	5.95	7.59	8.06	0.32
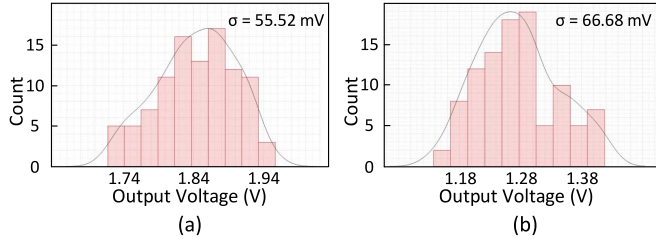
Fig. 4. Output voltage (V_{out}) variation with Monde Carlo analysis in (a) the proposed architecture and (b) the output of the conventional CTIA architecture.
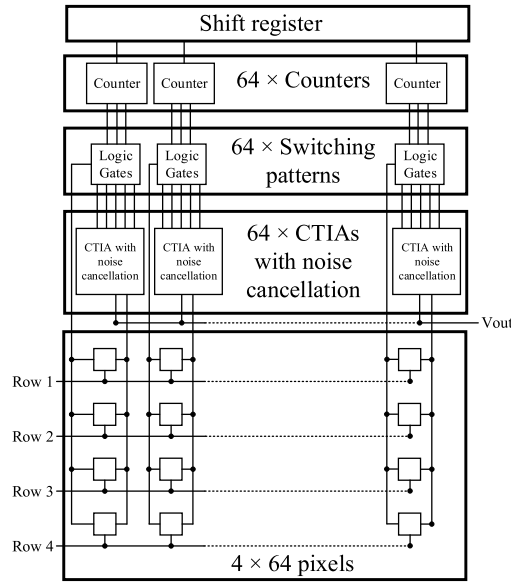

Fig. 5. System diagram of the CIS chip.

the noise cancellation circuit has been implemented using the same transconductor amplifier as in Fig. 2, with only the feedback capacitor C_{fb} and the reset switch S_{rst} in the feedback loop. Due to the subtraction of the signals in the proposed pixel topology the output voltage variation is less than in the conventional CTIA architecture. Capacitors C_1 and C_2 are each 200 fF to minimize their sampling noise and C_{fb} is 10 fF.

Fig. 5 shows the architecture of the CIS using the proposed pixel architecture in Fig. 2. It comprises 4 × 64 pixels, a shift register with 64 outputs that are connected to 64 3-bit counters which generate the signals to control various gates. The array of pixels is sufficient to cover the test line and some

area around it as shown in Fig. 1, so that the system will not be susceptible to erroneous measurements when the test line is slightly shifted. Lengthwise of the test line no more than 4 rows of pixels are required since the expected intensity in the test line is uniform.

Each pixel has of a 20 μm × 20 μm photodiode with two logic gates and two switches to enable the column and row selection. The overall pixel array area is approximately 3.9 mm × 0.14 mm which is sufficient to detect the test line in LFIAs without the need of lenses (Fig. 1). The processing circuit in Fig. 2 is shared between the 4 photodiodes in the same column [2]. The CIS has four rows which are sufficient for this application. The binning technique can also be implement for every 2 or 4 pixels of the same column. The row selection is controlled externally whereas the column selection is performed serially on chip. Once the row is selected the pixel of the first column is selected and its photocurrent is sensed and processed by the circuit. While the processing is in progress the pixel of the next column is enabled, sending its photocurrent to its respective column processing circuit. When the output of the first pixel is available the second pixel is still in the processing mode. The output of each column has an integration time (T_{int}) delay from its previous column, where T_{int} can be between 40 μs-4 ms. All outputs of the processing circuits are multiplexed to a pad. The column control selection is performed using a serial-input serial-output shift register to generate 64 master clocks for each column. In every column there is a 3-bit counter that has as input clock the master clock generated from the shift register. The generated 3-bit signal is then used to control various logic gates configurations to generate the switching pattern of Fig. 2.

III. MEASURED RESULTS

A. Chip Performance

The CIS was fabricated in the AMS 0.35-μm 4-metal CMOS process technology. Fig. 6 shows the chip micrograph; the overall chip area is 12.28 mm^2 including the pads. The pads were arranged on two sides for maximum area efficiency.

All the digital signals required for the operation of the chip were generated using a complex programmable logic device (CPLD, Xilinx). The interface of the chip to the PC and the digitization of the analog signal from the chip were performed using a data-acquisition system (DAQ, National Instrument) and custom LabView code for signal recording. For the characterization of the chip a light emitting diode (LED) source
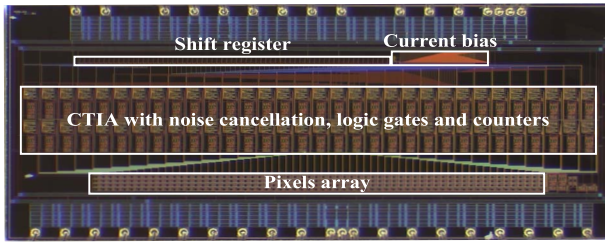
Fig. 6.   CIS chip micrograph.

was used to create varying irradiances in the active area and the chip responses were measured. The LED source was positioned on top of the chip to create uniform irradiance in the active area. The LED has 525 nm center wavelength and its irradiance was measured using a power meter. The CIS chip operated at 67 frames per second (fps) with $V_{DC} = 2$ V. A total number of 100 frames were sampled for each irradiance for analysis. The average output voltage of all the pixels over the 100 frames for different irradiances is shown in Fig. 7(a). The linear range of operation is approximately 1.7 V. Beyond that point the change in output voltage reduces and finally saturates at about 1.9 V. The calculation of the FPN was performed by producing an average image from the 100 frames of the same irradiance and then calculating the standard deviation of all pixels in that frame normalized by the saturation voltage [7]. The FPN in the dark (no light) is 1.8% and at 2.1 mW/cm^2 irradiance is 1%. This is due to mismatches in the C_{fb} and in the ratio of C_1 and C_2 capacitors of the processing circuit (due to limited space no matching techniques were used in the layout).

The SNR was calculated using (4) for $N = 100$ and the results are shown in Fig. 7(b).

$$\text{SNR} = 20\log \frac{\sqrt{\left(\sum_{i=1}^{N} \left(\mu_{i,D}^2 - \mu_i^2 \right) \right)/N}}{\sqrt{\left(\sum_{i=1}^{N} \sigma_i^2 \right)/N}} \quad (4)$$

where μ_i is the ith mean output pixel value, $\mu_{i,D}$ is the ith mean output pixel value at dark and σ_i the ith standard deviation. N is total the number of pixels. As shown in Fig. 7(b) the peak SNR is approximately at 50 dB at irradiance 2.1 mW/cm^2 and the dynamic range is approximately 45 dB.

The measured output-referred read noise is 1.9 mV$_{rms}$ and the input-referred charge noise 119 e$^-$. The chip requires 4.1 μA current and 2.3 μA current from the 3.3 V analog and digital supplies, respectively. Table I summarizes the parameters of the chip and compares with the parameters of other CIS developed for biosensing applications. The CIS in this brief has low read noise and the lowest power consumption per pixel.

B. Tests With LFIA

The CIS was experimentally tested using LFIA strips with Influenza A nucleoproteins of various concentrations. Prior to the tests, OpticStudio design software (Zemax) was used to determine the optimum setup. This is important in order for the light from the LEDs to uniformly impinge on the LFIA
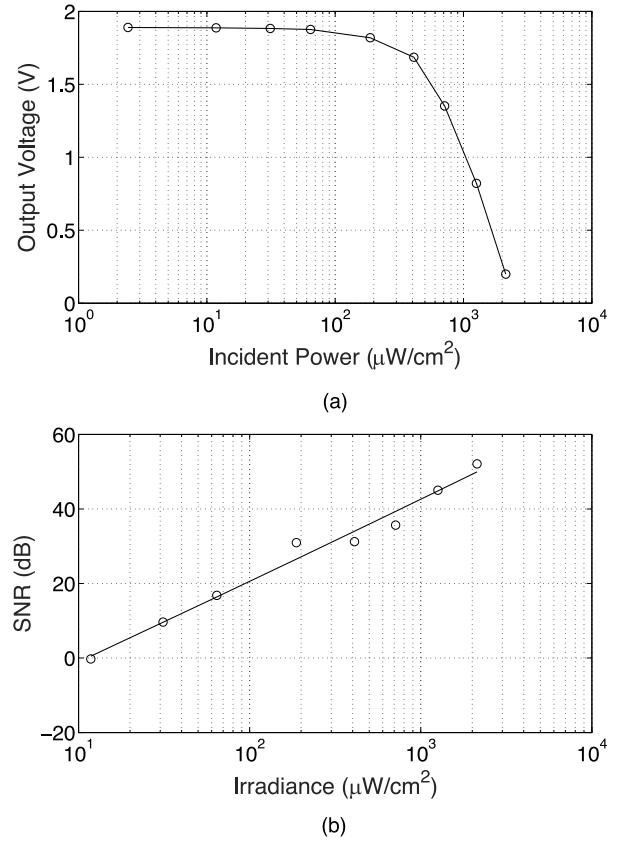

(a)

(b)

Fig. 7.   (a) Output voltage (V_{out}) of all pixels and (b) SNR of all pixels. Both measurements were performed using 100 frames at increasing light intensity. The CIS integration time was set to 50 μs. The center light wavelength was 525 nm.
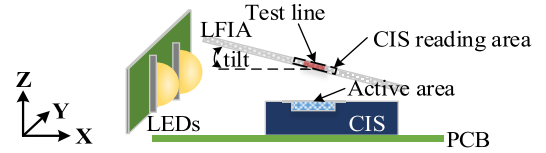

Fig. 8.   Experimental test setup for the measurements of the concentration in LFIAs using the developed CIS. The setup was optimized using ray trace simulations.

and then most of the reflected light from the LFIA to be collected from the CIS. Due to chip package size constraints the LEDs could not be optimally placed in close proximity around the chip, as considered in [10]. For simulations the exact dimensions of all the critical components (chip active area, LFIA detection pad area, LEDs and chip socket size) were considered. The optimum number of LEDs required to achieve uniform illumination is two as shown in Fig. 8. The LED used in the chip performance section have different size, viewing angle and position than the LEDs used for the tests of the chip with LFIAs in order to comply with the simulation results. The wavelength of both LEDs (525 nm) is in the range of maximum absorption from the gold nanoparticles present in the test line. Therefore, for higher concentrations of analyte in the LFIA, the light absorption is higher and less light is reflected from the test line to the CIS. The white areas of LFIA around the test line have higher reflection and therefore the output voltages for these areas are lower. The chip
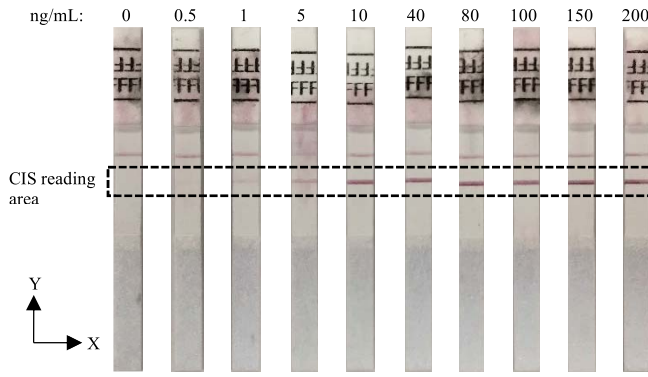
Fig. 9. Photographs of the tested LFIAs in various concentrations of Influenza A nucleoprotein.
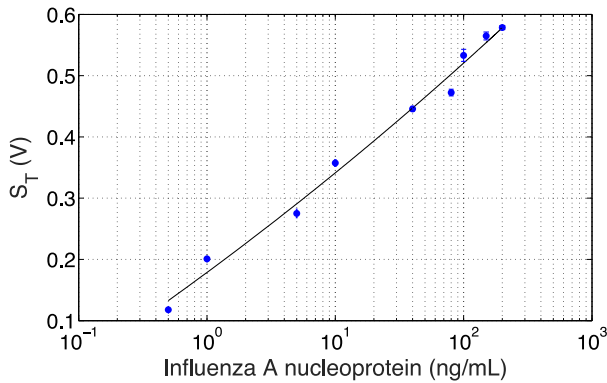

Fig. 10. Measured S_T signal after background correction for various concentrations of Influenza A nucleoproteins using the CIS chip.

was placed on a printed circuit board (PCB) along the X-Y plane; the LEDs were positioned vertically the Y-Z plane. The optimum distance between the middle of the LFIA strip and the LEDs is 8.6 mm where the sensor can detect the presence of a line with highest variation. The system was mounted in a custom made 3D printed enclosure to remove any ambient light interference during the readings. Also, a special receptacle was developed, which accurately placed the strip above the chip with a 10 degree tilt to match the simulation results. For the measurements the binning technique was implemented. The photocurrents from all 4 pixels in the same column were added and processed together. The total pixel active area of the CIS is 1600 μm^2 with overall 1×64 pixels. The integration time was 50 μs and $V_{DC} = 2$ V.

The LFIA strips used for the tests are shown in Fig. 9 with concertation of Influenza A nucleoprotein in saline buffer varying from 0.5 ng/mL to 200 ng/mL. Each strip was measured ten times and background correction was performed using the averaged data from ten measurements from a blank strip with 0 ng/mL concentration. The peak value was automatically detected and the average value of this maximum and the values of ± 5 adjacent pixels were calculated (S_T). The signals from these 11 pixels were used because they receive most of the reflected light from the test line of the LFIA [10]. Fig. 10 shows the average signal from each strip after ten measurements. The reader can distinguish the various concentrations of Influenza A nucleoprotein in LFIAs. The limit

of detection is 0.5 ng/mL where the line is very faint. The error bars in Fig. 10 indicate the calculated standard deviation. The cut-off signal which defines when there is no analyte in the sample, was calculated using the mean signal from the strip with 0 ng/mL concentration plus three times the standard deviation (3σ). The cut-off signal was 9.27 mV.

IV. CONCLUSION

A low power, low noise CIS has been presented for LFIA readers. Its photocurrent processing circuit combines the CTIA topology with noise cancellation using a single amplifier. The CIS was fabricated in 0.35-μm technology and achieves an output-referred read noise of 1.9 mVrms and a total measured power consumption 21 μW. The CIS has been tested with Influenza A nucleoprotein in LFIAs and showed good quantification capabilities with the ability to detect concentrations as low as 0.5 ng/mL.

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