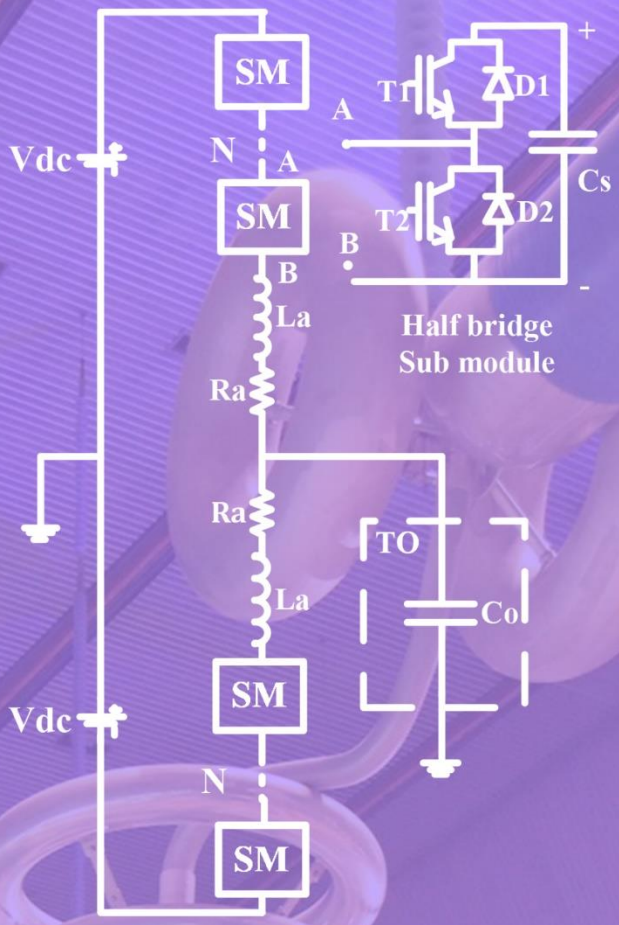
Master's thesis – Electrical Engineering

Modular Multilevel Converter (MMC) based High Voltage Test Source

Demonstration of a proof of concept with a mathematical model and simulation study for arbitrary wave shapes generation



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DNV·GL

Modular Multilevel Converter (MMC) based High Voltage Test Source

Demonstration of a proof of concept with a mathematical model and simulation study for arbitrary wave shapes generation

By

D.A. Ganeshpure

in partial fulfilment of the requirements for the degree of

Master of Science

in Electrical Engineering

at the Delft University of Technology,

to be defended publicly on Friday August 10, 2018 at 14:00.

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This thesis is confidential and cannot be made public until August 10, 2020.

An electronic version of this thesis is available at http://repository.tudelft.nl/.

ACKNOWLEDGMENT

This master's thesis is the first step towards power electronics-based high voltage test source. It could not have taken shape without the guidance and support of many people from both, high voltage and power electronics domain. I would like to take this opportunity to express my sincere gratitude to all of them.

I am deeply indebted to **Prof. Ir. Peter Vaessen** for his invaluable guidance and constant encouragement throughout the master's program. His constructive feedback and sustained motivation have been very crucial in accomplishing this master's thesis. I would like to express my sincere gratitude towards my daily supervisor **Dr. Ir. Mohamad Ghaffarian Niasar** for his constant support and counsel. I am very grateful to him for patiently addressing my queries from both high voltage and power electronics domain.

I am also very grateful to my supervisors from DNV GL for helping me with the thesis. I am grateful to **Dr. Cornelis Plet** for sharing his insights on the power electronic converter design. I am also grateful to **Ir. Rick Scharrenberg** and **Dr. Erik de Jong** for their support with respect to power electronics testing. Apart from the technical guidance, DNV GL provided a friendly work environment which motivates innovation.

I am much obliged to **Dr. Ir. Babak Gholizad** and **Ir. Aditya Shekhar** for their academic support in understanding the converter and the simulations.

I am also very grateful to all my friends and my family for their immense support and constant faith in my abilities to accomplish this thesis.

Dhanashree Ganeshpure
Delft, August 2018

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LIST OF ABBREVIATIONS

MMC = Modular Multilevel Converter

PWM = Pulse Width Modulation

HVDC = High Voltage Direct Current

PLL = Phase-Locked Loop

PR = Proportional Resonant

SHE = Selective Harmonic Elimination

NLC = Nearest Level Control

PSC = Phase Shifted Control

SVM = Space Vector Modulation

HV = High Voltage

TO = Test Object

PD = Partial Discharge

KVL = Kirchhoff's Voltage Law

EMF = Electromotive Force

LIST OF SYMBOLS

Chapter 1:

N = Number of submodules

i_s = Output current

i_u = Upper arm current

i_l = Lower arm current

i_c = Circulating current

N_u = Number of submodules inserted from upper arm (Integer value varies between 0 and N)

N_l = Number of submodules inserted from lower arm (Integer value varies between 0 and N)

$2V_{dc}$ = DC link voltage

C_s = Submodule capacitance

L_a = Arm inductance

R_a= Arm resistance

Chapter 2:

$\alpha = \frac{di}{dt}$ limit of the semiconductor devices

k_{max} = Upper limit for the submodule capacitor voltage

k_{dc} = Compensating factor for the time average of the stored energy in the submodules

ΔE_{max}= Maximum amount of excess energy that can be stored in each arm

V_{avg} = Average submodule capacitance voltage

m_{req}= Modulation index

f_{req} = Frequency of reference signal

φ = Phase difference between output current and output voltage

S = Apparent power rating of the converter

v_c = Circulating voltage

v_c^* = Reference of circulating voltage

v_a = Converter output voltage

v_a^* = Reference of Converter output voltage

v_s = Inner electromotive voltage (emf)

v_s^* = Reference of inner electromotive voltage (emf)

n_u^i = Insertion index of i^{th}submodule in the upper arm (1 or 0 value)

n_l^i = Insertion index of i^{th}submodule in the lower arm (1 or 0 value)

n_u = Average of insertion indices of upper arm submodules (continuous value varies between 0 and 1)

n_l = Average of insertion indices of lower arm submodules (continuous value varies between 0 and 1)

v_u^i = Instantaneous capacitor voltage of i^{th}submodule in the upper arm

v_l^i = Instantaneous capacitor voltage of i^{th}submodule in the lower arm

v_u = Instantaneous upper arm voltage

v_l = Instantaneous lower arm voltage

v_{cu}^{Σ} = Maximum upper arm voltage when all submodules are inserted from upper arm

v_{cl}^{Σ} = Maximum lower arm voltage when all submodules are inserted from lower arm

W_u = Upper arm energy

W_l = Lower arm energy

W_{Σ} = Total energy in the leg

W_{Δ} = Imbalance energy between upper and lower arm energy

P = Mean active input power

C_{load} = Load capacitance

Chapter 3

F_s = Switching frequency

$error$ = Error signal

A_{error} = Area covered under the curve $abs(error)$ graph

t_{signal} = Duration of signal generated

$\% E$ = Percentage error in the converter output signal

δ = Tolerance band in the capacitor voltage

$UA_1 \dots UA_N$ = Upper arm submodule number 1 to N

$LA_1 \dots LA_N$ = Upper arm submodule number 1 to N

Chapter 4

s_1 & s_2 = Two roots of solution to the differential equation of output current

A_1 & A_2 = Constants in the output current expression

$v_{us}^{i}(t)$ = Instantaneous capacitor voltage in i^{th} submodule in upper arm due to output current

$v_{u}^{i}(0)$ = Initial capacitor voltage in i^{th} submodule in upper arm

$i_{us}(t)$ = Output current component of upper arm

$i_{ls}(t)$ = Output current component of lower arm

Δv_{us}^{i} = Change in capacitor voltage in i^{th} submodule in upper arm due to output current

r_1 & r_2 = Two roots of solution to the differential equation of circulating current

B_1 & B_2 = Constants in the circulating current expression

$v_{uc}^{i}(t)$ = Instantaneous capacitor voltage in i^{th} submodule in upper arm due to circulating current

Δv_{uc}^{i} = Change in capacitor voltage in i^{th} submodule in upper arm due to circulating current

Δv_{usT1}^{i} = Maximum capacitor voltage variation in i^{th} submodule in upper arm in positive polarity of signal due to ***output current***

Δv_{ucT1}^{i} = Maximum capacitor voltage variation in i^{th} submodule in upper arm in positive polarity of signal due to ***circulating current***

Δv_{uT1}^{i} = Maximum capacitor voltage variation in i^{th} submodule in upper arm in positive polarity of signal

Δv_{uT2}^{i} = Maximum capacitor voltage variation in i^{th} submodule in upper arm in negative polarity of signal

Δv_{uT}^{i} = Total capacitor voltage ripple in i^{th} submodule in upper arm

I_{omax} = Maximum output current

I_{cmax} = Maximum circulating current

Chapter 5

C_f = Filter capacitance

R_f = Filter resistance

v_o = Voltage across filter capacitance/test object

f_c = Cut-off frequency

Chapter 6

$I_{s@fault}$ = Fault current drawn from the converter when the TO breaks down

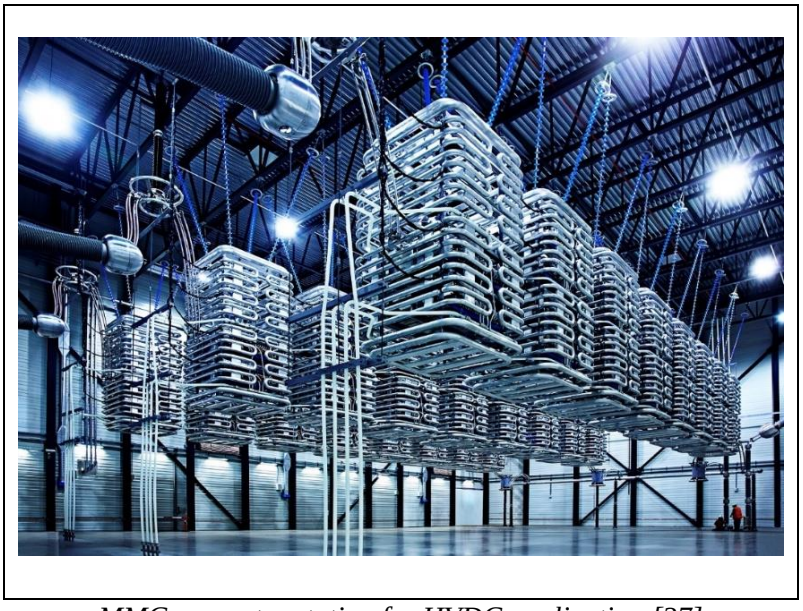
$I_{u@fault}$ = Fault arm current when the TO breaks down

R_{fault} = Fault resistance

ABSTRACT

Conventional high voltage test sources, i.e., transformers (cascaded and resonant), impulse generators, and rectifier circuits generate 50 Hz/60 Hz sinusoidal, lightning and switching impulses, and DC respectively. For arbitrary wave shapes, function generator and HV amplifier setup are available up to 50 kV and few kHz signal bandwidths. Superimposed signals (impulses or transients on a sinusoidal or DC) are generated from a careful design of superposition of two voltage sources. The demand of these unconventional test sources is increasing as new electric stresses are introduced in the current electrical power network due to the rise of power electronics. This motivates the search for a novel high voltage test source which can generate arbitrary wave shapes with larger signal bandwidth at higher voltage level. Modular multilevel converter (MMC) topology is a promising solution for high power applications because of its high efficiency, modular structure, and reduced filter requirement. Hence, the idea of a MMC-based high voltage test source is proposed for arbitrary wave shape generation. Such a converter-based test source can also be adapted as a mobile test system for site acceptance and diagnostic testing and opens an entire new high voltage research area.

This master's thesis demonstrates the proof of concept of a MMC-based high voltage test source using a mathematical and simulation model. The first step is to identify critical differences between existing MMC applications versus high voltage testing applications. Based on this analysis, control methodology and converter parameter design are adapted for high voltage testing application. Since a power electronic converter generates an output signal with harmonics, a filter is required to obtain a smooth signal that can be applied to the test objects. The quality of the generated signal is measured in terms of the peak value and the slope of the output voltage. Also, the protection system and DC source requirements are investigated briefly for a comprehensive picture of the MMC-based high voltage test system. The thesis demonstrates the feasibility of the MMC-based high voltage test source with a proof of principle on paper and with simulations. Recommendations are given for the next steps to realize a high voltage test source for arbitrary wave shape generation.



MMC converter station for HVDC application [37]

1. INTRODUCTION

1.1 Background and motivation

High voltage (HV) testing is a well-established field of electrical engineering, with many proven technologies. Many structural changes in the electrical power network are creating new electrical stresses, leading to different test requirements. Also, HV research demands for unconventional test sources to discover new findings. Hence there is always a room for innovation to work on the limitations of current technologies. This section sketches the current scenario of HV test sources with their limitations, discusses current developments in the power electronics, and chooses a promising converter topology for developing a novel HV test source.

1.1.1 Current scenario of high voltage test source

Testing HV equipment electrically, mechanically, and thermally is of utmost importance for both prototypes and commercial products. Table 1-1 shows type of tests conducted on HV equipment, with their characteristics and purpose.

Table 1-1: Types of tests conducted on HV equipment

Type of testing	Characteristics	Purpose
High voltage testing (Dielectric testing)	High voltage and low current	To determine insulation properties such as dielectric strength, dielectric losses, partial discharge (PD) and space charge
Nominal power testing	Nominal voltage and nominal current	To evaluate the performance (efficiency, thermal behavior, etc.) of HV equipment when deployed in the field
High power testing	High voltage and short circuit current	To inspect switchgear interruption capability and to analyze thermal and mechanical stresses due to short circuit current

For high voltage testing, various test sources such as transformers (resonant and cascaded), impulse generators, rectifier, and multiplier bridge circuits are available to generate 50 Hz/60 Hz sinusoidal, switching and lightning impulse, and DC respectively. These conventional HV test sources can generate a wide range of output voltage in different wave shapes, from low voltage to ultra-high voltage and traditionally spark gaps are used as fast switching devices.

Apart from these conventional signals, arbitrary wave shapes can be generated from a combination of a function generator and a HV amplifier which are shown in figure 1-1. The function generator can be programed for a specific wave shape. The output of such a function generator is in the range of 10 V and it is amplified to a desired high voltage level by a HV amplifier. These HV amplifiers are available up to 50 kV, 12 mA current rating and a signal bandwidth of 1.4 kHz [1]. To conduct testing with arbitrary wave shapes at higher voltage level with larger signal bandwidth, a new test source is required. This will facilitate research in partial discharge (PD) measurement [2] [3] and space charge measurement [4].

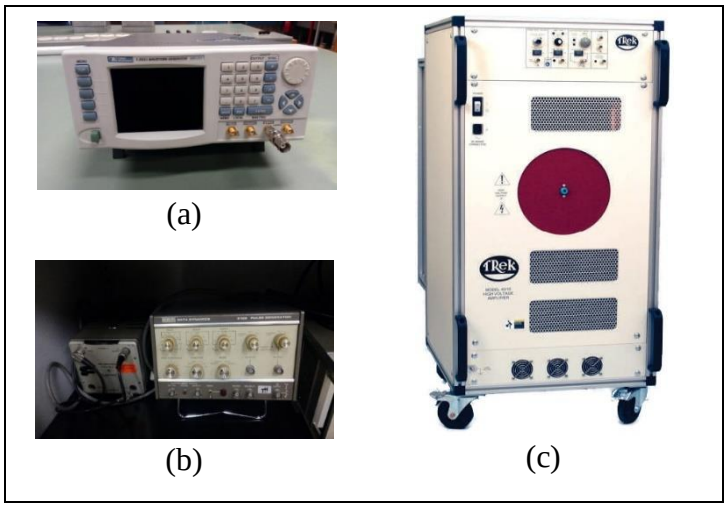


Figure 1-1: (a) Advanced function generator (b) Old function generator (c) HV amplifier setup [1]

It is common to design a customized small-scale test source to generate desired superimposed wave shapes in the range of a few kV [5] [6]. It requires careful design of superposition of two HV sources without one influencing the other one. Designing a new test environment every time for conducting research with superimposed signals is a cumbersome task. Novel ideas should be explored to have a single test source which can generate superimposed wave shapes.

All mentioned conventional test sources are bulky and designed for indoor testing (lab based). For site acceptance tests and failure investigations of bulky HV equipment e.g. power transformers, mobile test sources are developed. One of such a mobile test system [7] is capable to generate variable frequency from 40 Hz to 200 Hz up to 700 kV voltage rating. This mobile test system contains a converter, transformer and HV filter. The required input supply to the converter can be made available by the local grid or a diesel generator. Arbitrary wave shape generation on a mobile test system can open new test procedures for bulky HV equipment.

From this analysis, it can be concluded that the new HV test source should have the following characteristics:

- ✓ Generation of arbitrary wave shapes with higher signal bandwidth than few kHz,
- ✓ Scalable to higher voltage levels
- ✓ Usable as a mobile test system

With significant growth of power semiconductor device industry in the past, many semiconductor-devices-based equipment e.g. HV amplifiers are manufactured for high voltage testing application. Hence innovative ideas for the required test source are explored in power electronics domain in the following section.

1.1.2 Current scenario of high voltage power electronic converters

2-level voltage source converters (VSCs) are very common for AC to DC and DC to AC conversion at low power and low voltage rating. With the continued increase of power and voltage levels, multilevel topologies like diode clamped and flying capacitor topologies have been developed for medium voltage range (<10kV) [8]. To achieve the conversion at the higher voltage level (>10kV), cascaded multilevel topologies are getting developed such as cascaded half-bridge topology. In 2003, Prof. Dr. Rainer Marquardt has developed another cascaded multilevel topology, named as modular multilevel converter (MMC) for transferring power at

high voltage range [9]. Due to its scalability, high efficiency, and reduced filter requirement compared to line commutated converter [10], MMC is proving to be a promising solution for high power application e.g. HVDC and high voltage drives.

The 2-level and 3-level converters are available for low voltage and medium voltage respectively. Also, the output of a 2-level and 3-level converter is a pulse width modulated (PWM) signal and filter design to extract smooth arbitrary wave shapes from the PWM signal is very difficult. For sinusoidal output signal, various low pass filter designs are developed [11]. But, it is not possible to directly use the same filter design for non-sinusoidal wave shapes. With higher number of levels in the output signal, it can reduce the filter requirement and make it possible to generate arbitrary wave shape at high voltage range. Hence it is decided to explore one of the most promising multilevel topology i.e. MMC.

Figure 1-2 presents the single leg structure of MMC, where it has an upper and lower arm stacked with several series-connected submodules (N). The output current (i_s) is the result of the difference between the upper arm current (i_u) and lower arm current (i_l). Beside the output current of the MMC, a circulating current (i_c) is present in the converter, which circulates between the leg and the DC link. However, the circulating current has no direct impact on the output current. Figure 1-2 shows the positive direction of i_u, i_l, i_s and i_c.

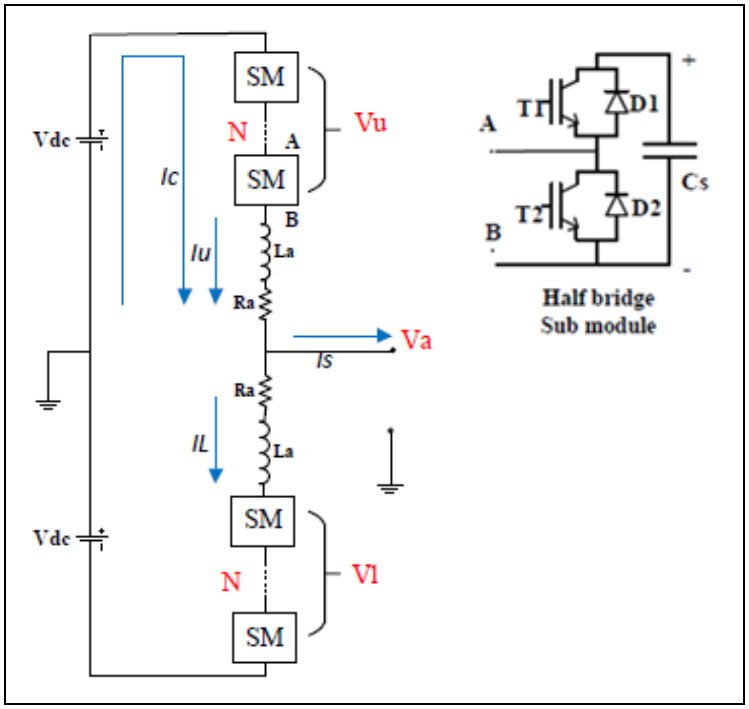


Figure 1-2: Single leg of MMC topology

In an ideal condition, a total of N out of $2N$ submodules are always inserted from the converter leg. A submodule consists of a capacitance which can be either inserted or bypassed by switching semiconductor devices T1 and T2. The difference in the number of submodules inserted from upper and lower arm generates output voltage (v_a). For example, if all submodules are inserted from the lower arm and all submodules are bypassed from the upper arm, it generates V_{dc} output voltage. All possible output voltage levels with $N = 6$ are shown

in table 1-2, where N_u & N_l are the number of submodules inserted from upper and lower arm respectively.

Table 1-2: States of the converter with N=6

N_u	N_l	v_a
6	0	$-V_{dc}$
5	1	$-\frac{2V_{dc}}{3}$
4	2	$-\frac{V_{dc}}{3}$
3	3	0
2	4	$\frac{V_{dc}}{3}$
1	5	$\frac{2V_{dc}}{3}$
0	6	V_{dc}

Ideally, average voltage magnitude across each submodule capacitance is $2.V_{dc}/N$ since the total DC link voltage ($2V_{dc}$) is divided into N submodule capacitance at every instant. MMC is a voltage source converter which maintains a constant output voltage. But the output current is dictated by the load impedance and it is supplied by the arm current. When arm current flows through these submodule capacitances, it deviates the capacitor voltage from the average value This introduces an imbalance between the DC link and total sum of capacitor voltage in the leg, resulting in a circulating current. This is a natural cause of circulating current, but some modulation techniques insert $N+1$ or $N-1$ submodules which can introduce significantly large circulating current (value comparable to output current). Large circulating current can introduce large submodule capacitor voltage ripple. Both quantities are coupled hence both should be controlled for proper operation of the converter.

1.1.3 Summary

From all mentioned HV converter topologies, MMC is chosen for further investigations to address limitations in current HV test sources. Three main motivations behind a MMC-based test source are discussed in subsection 1.1.1 and figure 1-3 summarizes them. The figure 1-3 also mentions that the conventional AC, impulse, and DC generators consumes space and time to change the test setup.

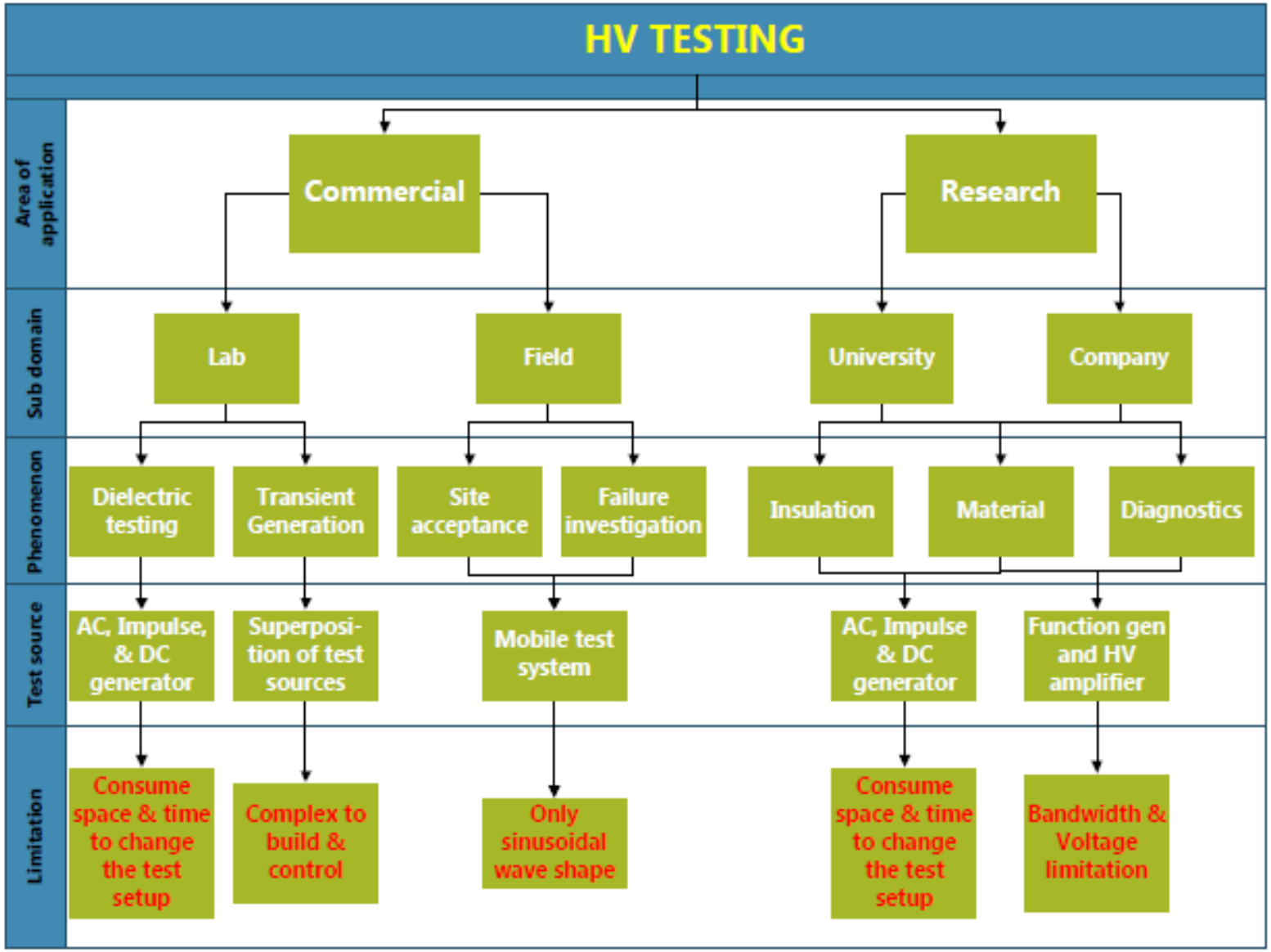


Figure 1-3: Overview of HV test sources

1.2 Bird's eye view

It is not very easy to develop a HV test source. Hence the process is divided into the following steps. First, the idea should be proven on paper with a mathematical model and simulation results. Then, the on-paper design of the control methodology should be tested on a small-scale prototype of 400 V and a low number of submodules. A small-scale model of MMC is implemented by many universities to understand the behavior of the converter without investing a lot of money and space [12]. The same idea can be borrowed to verify the proposed control methodology for the test source. As a next step, the small-scale prototype should be extended to e.g. 10 kV voltage level. When this idea is proven on both small-scale and medium-scale prototype, the test source can be realized at a much higher voltage level e.g. 150 kV. When all steps are successfully implemented, this test source can open a new possibility of conducting tests at equipment location instead of all the equipment getting transported to the testing facility. The mobile testing will be possible only if the power electronic test generator is compact and light enough to fit in a transport vehicle. Figure 1-4 summarizes the step in a block diagram.

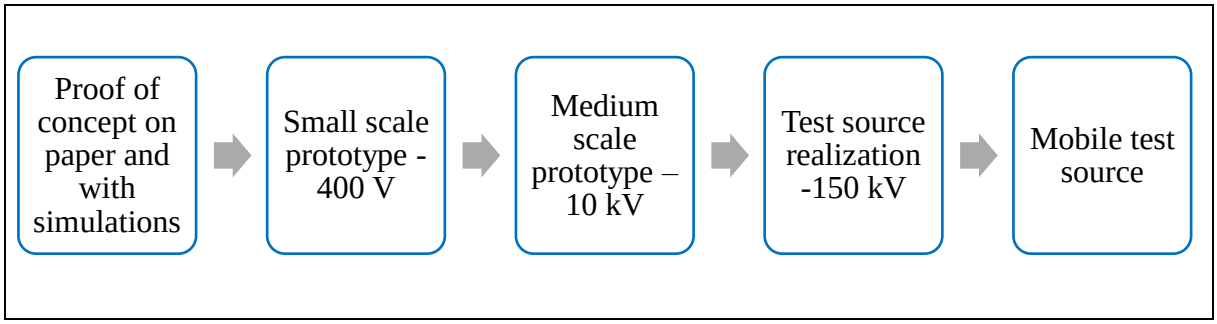


Figure 1-4: Bird's eye view of MMC-based test source

1.3 Research objective

This thesis is a first step towards investigating the technical viability of an MMC-based HV test source. Hence it aims to demonstrate the proof of concept using a mathematical model and simulation results. Figure 1-5 shows the proposed MMC-based test environment. MMC needs a DC source as the input, and the control system generates the gate pulses to obtain the desired output signal. A filter is important to remove the switching harmonics from the converter output signal. The filter implementation is important for small-scale prototype since it will have limited number of submodules.

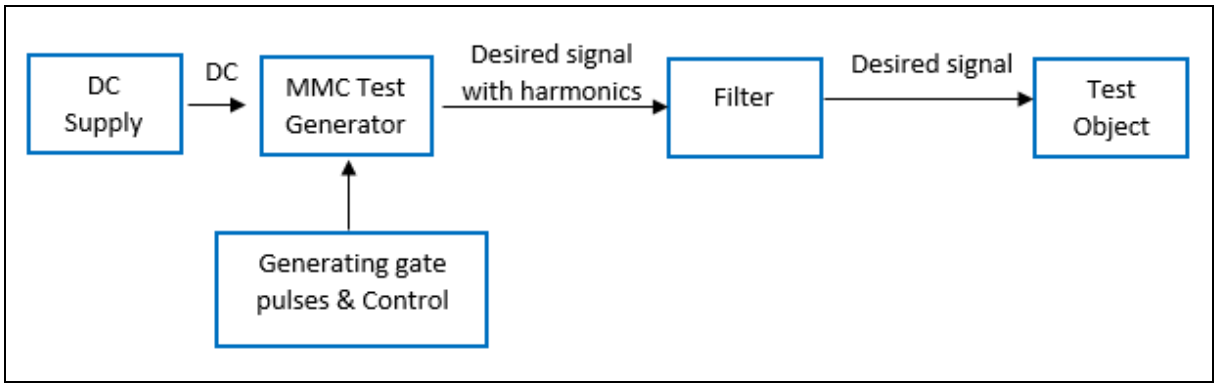


Figure 1-5: MMC based test environment

At the end of this master's thesis, the following research goals are achieved with a mathematical model and simulation results of the test source:

- To identify key differences in the design and control methodology of MMC used for power application and high voltage testing application
- To adapt the control methodology of the MMC for the high voltage testing application based on the identified key differences
- To develop the mathematical model to design the converter parameters, i.e. submodule capacitance, arm inductance and arm resistance for optimal operation of the test source
- To design a suitable filter to remove the unwanted harmonics from the converter output
- To study the protection system and DC source requirement for the MMC-based high voltage test source.

These research goals are defined for a small-scale prototype with 400 V voltage rating. Most HV equipment (transformers, reactors, cables, and bushings) behave as a capacitor when their insulation is tested with HV voltage. That is why the test object is modeled as a capacitance (C_{load}) in the range of 0.5 to 50 nF. Table 1-3 describes signals expected to be generated by the test source. The list looks similar to the type of signal generated from a traditional function generator. Periodic signal can be programmed for variable frequency from 0.1 Hz to 1000 Hz. With 0.1 Hz sinusoidal, HV equipment with very high capacitance are tested so that input current requirement is reduced. Whereas, the upper limit on the frequency (1000 Hz) is chosen based on the switching transients in the power system. These switching transients are standardized in IEC 60060-1 document by a switching impulse wave shape which has 250 µs rise time & 2500 µs fall time. The rise time explains the upper limit on the frequency for the periodic signals.

Table 1-3: List of arbitrary waveshapes expected to be generated by the test source

Periodic and bipolar wave shapes	**Non-periodic and single polarity wave shapes**
Sinusoidal (0.1-1000 Hz)	Square pulses (Periodic with duty ratio)
Square uniform (variable duty ratio & 0.1 Hz-1000 Hz)	Switching impulse (250 µs rise time & 2500 µs fall time)
Triangular - symmetric and unsymmetrical (variable duty ratio & 0.1 Hz-1000 Hz)	
Trapezoidal (Variable rise in voltage & 0.1 Hz - 1000 Hz)	

The above-described test environment is developed based on following assumptions:

- Losses are calculated for the designed system to check whether the design is feasible or not, but the system performance is not optimized to obtain more efficient system. It is not considered as a primary concern.
- The converter model is developed and simulated considering ideal semiconductor devices.
- The steady-state behavior of the converter is studied assuming the submodule capacitances are charged to their average value.

1.4 Outline of thesis report

An overview of each chapter is described in this section:

Chapter 2 discloses key differences between power applications and high voltage testing application of MMC in terms of their philosophies, overall structures, submodule topologies, control systems, converter design, mathematical modelling and measuring the quality of the converter output signal.

Chapter 3 discusses the control system of the converter in detail. The performance of modulation techniques is compared, and an open loop control system is designed for the high voltage testing application. An optimal number of submodules are chosen for the small-scale prototype design.

Chapter 4 derives the mathematical model of MMC with discontinuous output current pulses. The model focuses on deriving submodule capacitor voltage ripple. Based on this mathematical analysis of MMC, converter parameters, i.e. arm inductance, submodule capacitance, and arm resistance are designed. Current and voltage rating of the semiconductor devices requirements are studied based on the converter operation.

Chapter 5 analyzes the frequency spectrum of the converter output signal and design a suitable low pass filter topology to obtain a smooth output signal. This filter will act like a load in combination with the test object for the converter, and hence its effects on the converter operation are studied analytically and with simulations.

Chapter 6 discusses the fault characteristics of the MMC-based test source and how to protect the system when a fault occurs. Next, alternative DC source arrangement is proposed in place of ideal DC sources for higher voltage level, and its requirements are briefly discussed.

Chapter 7 is the last chapter of this thesis report. It concludes the work of this master's thesis with recommendations for future work with a PhD proposal to DNV GL.

2. KEY DIFFERENCES BETWEEN POWER APPLICATION AND HIGH VOLTAGE TESTING APPLICATION

This chapter discloses key differences between power applications and high voltage testing application of MMC in terms of their philosophies, overall structures, submodule topologies, control systems, converter design, mathematical modelling and measuring the quality of the converter output signal

2.1 Philosophy

The MMC based test generator is designed for non-power application where arbitrary wave shapes are generated at high voltage, with rather small current magnitude. Due to small magnitude of the output current, power transfer between converter and load is trivial compared to power application of MMC. Conventional HV test sources like impulse generators do not have closed-loop control for both, output current and voltage since it generates very fast signals. Hence the output current control loop in existing MMC technology, which controls real and reactive power transfer, is not required for the test generator. Without the output current control loop, the output current is determined by the test source output voltage and the impedance of the TO. In case the TO is capacitive, this output current is there to charge or discharge the load capacitance and vanishes to nearly zero once the charging or discharging process is over. This pulse, shaped output (discontinuous) current causes discontinuous power transfer between the load (TO) and converter.

Discontinuous power transfer with small magnitude is the biggest difference between existing MMC application and the adaption for testing application. With little power transfer, losses and efficiency of the converter are not of primary concern in the test source design.

2.2 Overall circuit structure

MMC was introduced as a three-phase AC to DC and DC to AC converter topology where each leg represents one phase of the AC side. To generate non-sinusoidal single-phase wave shapes across the test object with small current magnitude, a single leg of the MMC will be sufficient. Since the converter control is implemented per phase, it would not be a completely different control structure for a single leg MMC compared to conventional three leg structure of MMC. But, DC link requirements for the single leg test generator and conventional three legs MMC are different. In case of power applications of a MMC, it is possible to remove bulky DC link capacitances by controlling the circulating current to a constant value [8]. The circulating current has an even order harmonic component with the highest magnitude for the second-order harmonic [13]. That is why various circulating current control loop are studied in the technical literature to maintain the DC link voltage [14].

In case of the MMC based test source, the discontinuous output current pulses must be provided by the DC source without excessively varying the DC link voltage. Though the DC link provides these current pulses, the magnitude of these pulses is small. Hence the variation in the DC link voltage will be very small, and hence the DC link is modeled as an ideal DC source in this thesis.

2.3 Submodule topology

In power applications of MMC, submodule topology is chosen based on the DC short circuit characteristics. It is important that the submodule topology has DC fault handling ability since DC circuit breakers are not yet accepted in the market for high voltage application. DC fault handling ability of the submodule makes sure that the DC fault current is limited or controlled to a threshold value.

The half-bridge topology is simplest choice with respect to losses and cost. Full bridge topology is a better choice with respect to dc fault handling ability at the cost of doubling the number of semiconductor devices and with that increasing cost and losses. Other fault tolerant topologies have been proposed [8], which represents intermediate solutions between the half bridge and full bridge solution.

Complex fault tolerant topologies are not considered for the high voltage testing application, because it is assumed the test object cannot supply fault current. A protection switch will be installed to disconnect the DC supply in case of a DC link fault. The half bridge topology has three different states, as shown in figure 2-1. When switch T1 is on, the submodule capacitor is inserted, and when the switch T2 is on, the submodule capacitor is bypassed. The behavior of these two switches is complimentary. When both switches are off, the submodule is blocked, and this state is used for protection of semiconductor devices in case of a fault condition outside the submodule.

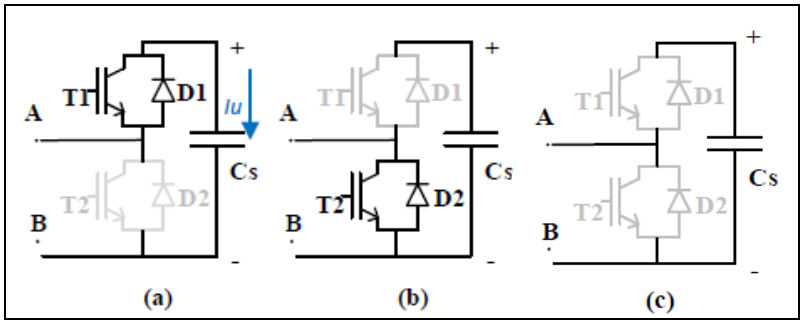


Figure 2-1: Half bridge topology (a) Submodule inserted (b) Submodule bypassed (c) Submodule blocked

The off-state of the submodule is used in case of DC side fault without a DC circuit breaker implementation. The DC side fault is detected and isolated by the AC side circuit breaker, hence the fault current flows through the converter. The IGBTs are protected from the fault current by turning them off, and a thyristor switch is inserted to conduct the fault current, in parallel to switch T2. A thyristor switch has better current conducting capability than a IGBT. The thyristor switch is shown in figure 2-1. For high voltage testing application, it will not be necessary to install such a switch since the test object cannot provide fault current.

For power applications of MMC, continuous operation is of utmost importance. Hence, when a submodule experiences a failure in its capacitance or any switch, the submodule is short-circuited, and another redundant submodule is added to maintain the total number of submodules using a bypass switch. The bypass switch is parallel to the thyristor switch and it is shown in figure 2-2. The decision about the use of redundant submodule for high voltage

testing application can be done based on trade-off between the need for continuous operation and space and cost it adds.

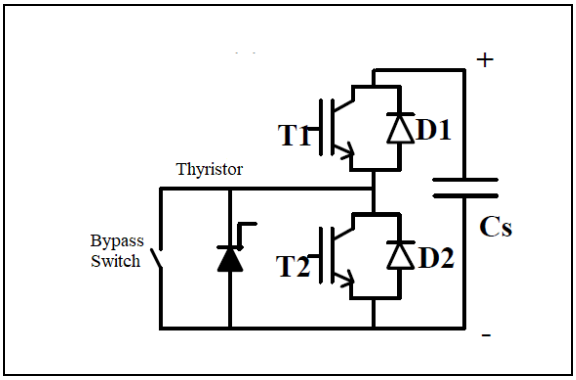
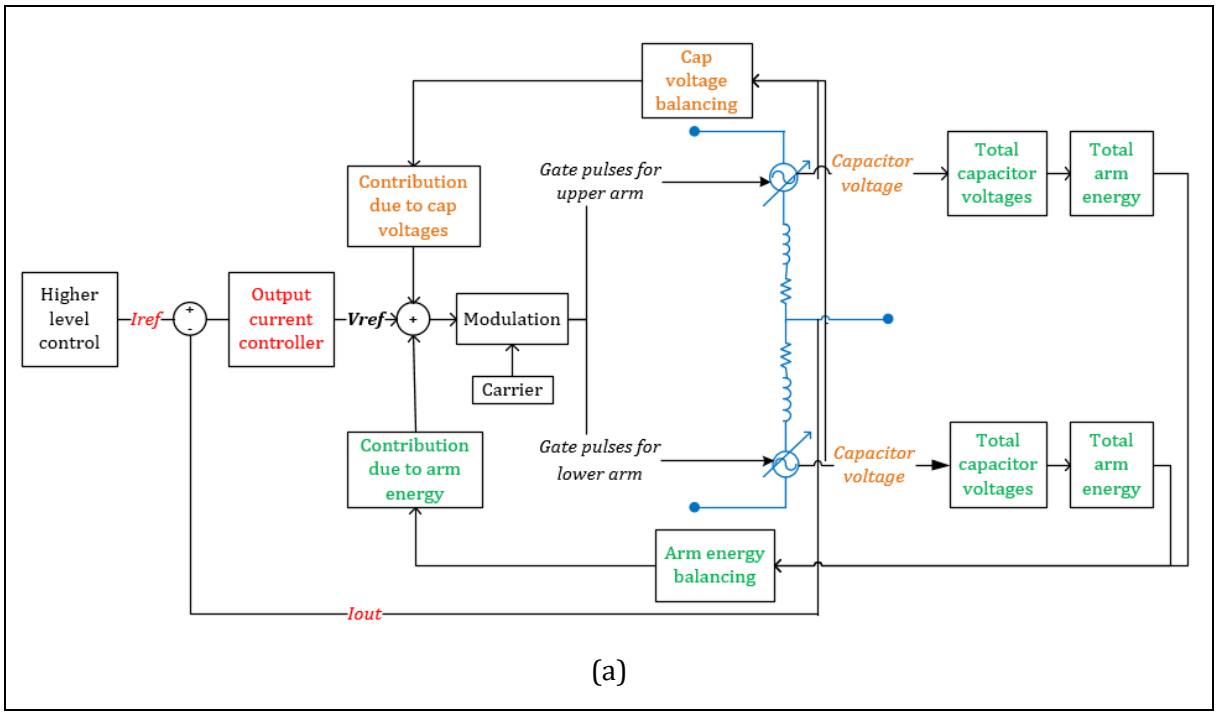


Figure 2-2: In built protection within a submodule

2.4 Control scheme

Figure 3 gives an overview of the control system used for MMC in power applications [8]. It involves many interleaved closed loops. Higher-level control involves time synchronization with the DC side and the AC side grid with open loop control of active and reactive power. A phase-locked loop (PLL) synchronizes the converter control system with the AC bus voltage vector. DC bus voltage is maintained by active power control, whereas reactive power decides the output reference current. The next level of control calculates the output voltage reference based on the output current reference and feedback of output current control using a proportional resonant (PR) controller [8]. Depending upon the modulation technique chosen, arm balancing and submodule capacitor voltage balancing are implemented.

Without power transfer and without output current control, the control system for the test generator simplifies significantly and the overview is shown in figure 2-3. Detailed discussion about the control system and design choices made is provided in chapter 3.



(a)

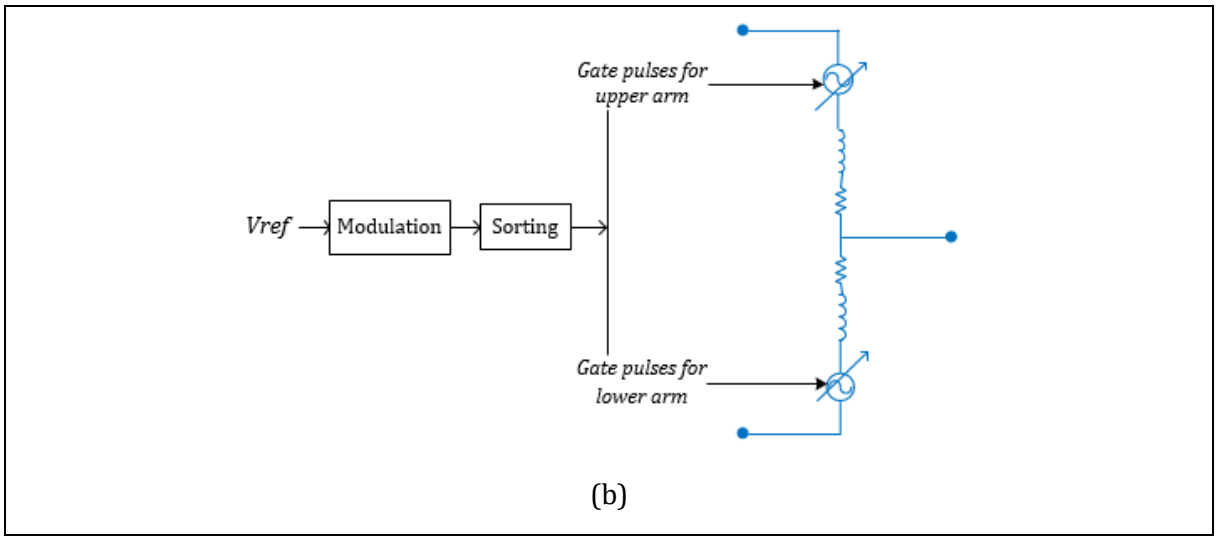


Figure 2-3: Overview of the control system (a) Power application (b) High voltage test application

2.5 Converter parameter design

Submodule capacitance, arm inductance, and arm resistance are three important converter parameters and the converter response to switching submodules is dictated by these parameters.

In power applications, the arm inductance value is chosen based on two criteria. The first one is to reduce the second order harmonic in the arm current to reduce losses in the semiconductor devices [15]. This is not applicable for high voltage testing application because the output current or arm current is not sinusoidal. The second criterion is to design the inductor value which restricts the rate of change of current based on the semiconductor devices limit [16]. The second criterion can be used for choosing the arm inductance for high voltage testing application. If α is the $\frac{di}{dt}$ limit of the semiconductor devices, then the inductor value can be designed based on the worst-case scenario of DC link has fault. In this situation, KVL across the test generator leg will yield equation 2.1. Substituting $\frac{di_u}{dt} = \frac{di_l}{dt} = \alpha$ in equation 2.2, the inductor value can be calculated as shown in equation 2.2

$$L_a \frac{di_u}{dt} + L_a \frac{di_l}{dt} - 2V_{dc} = 0 \tag{2.1}$$

$$L_a = \frac{V_{dc}}{\alpha} \tag{2.2}$$

The submodule capacitor should be designed to have a minimum voltage fluctuation. The fluctuation is proportional to the value of the capacitance. On the other hand, the capacitance should not be too big, otherwise, it would add an unnecessary extra cost to the system. To maintain the capacitor voltage ripple within a fixed band, the minimum requirement for the capacitance value is calculated as follows for power applications [17].

$$C_{smin} = 2.N.\frac{\Delta E_{max}}{V_{dc}^2(k_{max}^2 - k_{dc}^2)} \tag{2.3}$$

Where, k_{max} = upper limit for the submodule capacitor voltage

k_{dc} = compensating factor for the time average of the stored energy in the submodules

ΔE_{max}= maximum amount of excess energy that can be stored in each arm

In power applications of MMC, amount of energy stored in each arm can be varied by varying the k_{dc}value. Hence the average submodule capacitor voltage (V_{avg}) and instantaneous capacitor voltage ($v_{u,l}^{i}$) can be expressed as follow:

$$V_{avg} = k_{dc}\frac{2V_{dc}}{N} \qquad\qquad v_{u,l}^{i} \leq k_{max}\frac{2V_{dc}}{N} \tag{2.4}$$

For steady-state operation, k_{dc} can be chosen as 1. ΔE_{max} can be calculated from equation 2.5 and its derivation can be found in [17].

$$\Delta E_{max} = \max\left(\frac{S}{24\pi m_{req} f_{req}}\left[4\,sin\left(2\pi f_{req}t-\varphi\right) - m_{req}\,sin\left(2\pi f_{req}t-\varphi\right) - 2m_{req}^{2}\,sin\left(2\pi f_{req}t\right)cos(\varphi)\right]\right) \tag{2.5}$$

Where, m_{req}= modulation index of reference signal

f_{req} = frequency of reference signal

φ = Phase difference between output current and output voltage

S = Apparent power rating of the converter

Equation 2.5 contains sinusoidal terms which are there because of sinusoidal voltage and current expressions. Hence this approach of submodule capacitance cannot be used for high voltage testing application directly since the output current is not sinusoidal in that case. A new approach must be explored to design the submodule capacitance for high voltage testing application.

For power application, the efficiency of MMC is very important and, hence arm resistance is chosen to be as small as possible. For high voltage testing, this arm resistance value is chosen to obtain the desired response from the equivalent RLC circuit. If R_{eq}, L_{eq} and C_{eq} are equivalent impedances of the mathematical model of the MMC for HV testing application, then a critically damped system gives the fastest response. Hence equation 2.6 shows the criteria for a critically damped circuit for series RLC circuit with R_{eq}, L_{eq} and C_{eq} parameters,

$$R_{eq} = sqrt\left(\frac{8L_{eq}}{C_{eq}}\right) \tag{2.6}$$

2.6 Mathematical modeling

The circuit behavior of MMC, with so many submodule capacitances, is complex. The following section derives dynamic equations and simplifies them by introducing linear transformations, averaging principle and insertion indices. At the end of this section, the

capacitor voltage ripple calculations are performed with an assumption that the output current is sinusoidal with a phase difference as per connected load. Hence this analysis does not help for high voltage testing application directly, but it has been used partially later in chapter 4 to derive the mathematical model of the test source.

2.6.1 Dynamic equations of MMC

If Kirchhof's Voltage Law (KVL) is applied in the upper and lower arm, dynamic equations of the MMC can be obtained (Refer to figure 2-4). Equation 2.9 can be obtained by adding equation 2.7 and 2.8, whereas equation 2.10 can be obtained by subtracting equation 2.7 from equation 2.8.

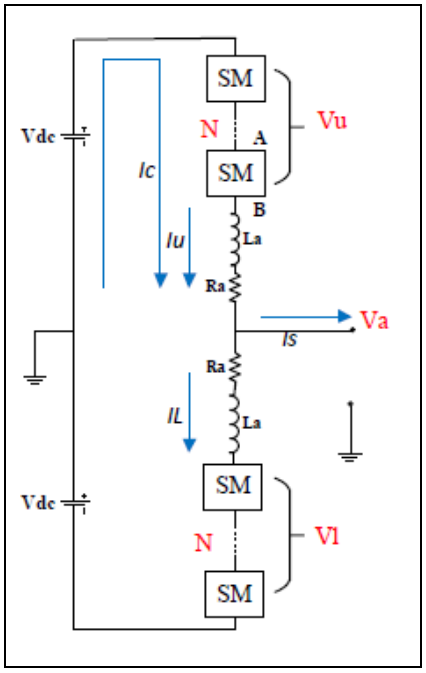


Figure 2-4: Schematic of single leg of MMC

$$V_{dc} - v_u - R_a.i_u - L_a.\frac{di_u}{dt} - v_a = 0 \tag{2.7}$$

$$V_{dc} - v_l - R_a.i_l - L_a.\frac{di_l}{dt} + v_a = 0 \tag{2.8}$$

$$2V_{dc} - v_u - v_l - R_a.(i_u + i_l) - L_a.\left(\frac{di_u}{dt} + \frac{di_l}{dt}\right) = 0 \tag{2.9}$$

$$v_l - v_u + R_a.(i_l - i_u) + L_a.\left(\frac{di_l}{dt} - \frac{di_u}{dt}\right) - 2.v_a = 0 \tag{2.10}$$

Equations (2.9) and (2.10) are coupled equations with four variables v_u, v_l, $i_u$and i_l. Linear transformation described in [8] can be used to simplify the coupled differential equations.

$$i_s = i_u - i_l \qquad\qquad i_c = \frac{i_u + i_l}{2}$$

$$v_s = \frac{v_u - v_l}{2} \qquad v_c = \frac{v_u + v_l}{2} \tag{2.11}$$

i_s is output current and v_s can be understood as inner electromotive force (emf). i_c represents circulating current and this current is driven by the circulating voltage (v_c). After substituting the linear transformation 2.11 into equation 2.9 and 2.10, decoupled differential equations can be obtained:

$$V_{dc} - v_c - R_a.i_c - L_a.\frac{di_c}{dt} = 0 \tag{2.12}$$

$$-2.v_s - R_a.i_s - L_a.\frac{di_s}{dt} - 2.v_a = 0 \tag{2.13}$$

Equation 2.12 has circulating current as a state variable and equation 2.13 has output current as a state variable. After rearranging equation 2.12 and 2.13, equations 2.14 and 2.15 are obtained

$$L_a.\frac{di_c}{dt} = V_{dc} - v_c - R_a.i_c \tag{2.14}$$

$$\frac{L_a}{2}.\frac{di_s}{dt} = -v_s - \frac{R_a}{2}.i_s - v_a \tag{2.15}$$

2.6.2 Averaging principle

To represent the switching behaviour of the converter, the concept of insertion indices is introduced. n_u^i and n_l^i are insertion indices and their value can be either 1 or 0, where 1 represents the submodule is inserted and 0 represents the submodule is bypassed. Instantaneous upper and lower arm voltage can be represented by

$$v_{u,l} = \sum_{i=1}^{N} n_{u,l}^i.v_{u,l}^i \tag{2.16}$$

It is a good approximation to assume instantaneous submodule capacitor voltage to $v_{cu,l}^{\Sigma}/N$ [8]. Here, $v_{cu,l}^{\Sigma}$ represents sum of all submodule capacitor voltages and ideally this value should be equal to DC link voltage. But, when the arm current flows through submodule capacitance, it introduces a submodule capacitor ripple around $2V_{dc}/N$ for each inserted submodule. If this constant value ($v_{cu,l}^{\Sigma}/N$) is substituted in expression 2.16, it simplifies the equation as follows:

$$v_{u,l} = \frac{v_{cu,l}^{\Sigma}}{N}\sum_{i=1}^{N} n_{u,l}^i \tag{2.17}$$

$$v_{u,l} = n_{u,l}v_{cu,l}^{\Sigma} \tag{2.18}$$

$$n_{u,l} = \frac{1}{N}\sum_{i=1}^{N} n_{u,l}^i \tag{2.19}$$

Here, $n_{u,l}$ is a new term representing the average number of submodules inserted in upper and lower arm. Different switched states of converters are expressed using a continuous expression 2.19. It is called the averaging principle.

2.6.3 Submodule capacitor dynamics

Apart from circulating current and output current, $2N$ more state variables will be present for each submodule capacitance voltage ($v_{u,l}^{i}$). It is possible to reduce $2\mathrm{N}+2$ differential equation into 4 by extending the averaging principle for submodule capacitor voltage and mathematical steps are explained below. The basic physics behind capacitance governs equation 2.20 and the effect is summed for all submodules in the upper and lower arm as shown in equation 2.21. If equation 2.18 is substituted into equation 2.21, it simplifies the analysis from $2N$ differential equations into 2 differential equations. If the inverse linear transformation is derived from equation 2.11 and substituted in equation 2.21, the dynamic behaviour of the submodule capacitance can be derived.

$$C_s \frac{dv_{cu,l}^{i}}{dt} = n_{u,l}^{i}.\, i_{u,l} \text{ for } i = 1,2, \dots, N. \tag{2.20}$$

$$C_s \sum_{i=1}^{N} \frac{dv_{cu,l}^{i}}{dt} = \sum_{i=1}^{N} n_{u,l}^{i}.\, i_{u,l} = i_{u,l} \sum_{i=1}^{N} n_{u,l}^{i} \tag{2.21}$$

$$\frac{C_s}{N} \frac{dv_{cu,l}^{\Sigma}}{dt} = n_{u,l}.\, i_{u,l} \tag{2.22}$$

$$\frac{C_s}{N} \frac{dv_{cu}^{\Sigma}}{dt} = n_u \left(\frac{i_s}{2} + i_c \right) \tag{2.23}$$

$$\frac{C_s}{N} \frac{dv_{cl}^{\Sigma}}{dt} = n_l \left(-\frac{i_s}{2} + i_c \right) \tag{2.24}$$

2.6.4 Selection of insertion indices

The expression of insertion index can be derived using equation 2.18 and linear transformation equation 2.11. Equation 2.27 can be used to derive an expression for insertion indices and their values are calculated based on reference values of v_c^* & v_s^*. Equation 2.28 is showing general selection of values for reference voltages of v_c^* & v_s^*, and v_{cu}^{Σ}.

$$v_s = \frac{-n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} \qquad v_c = \frac{n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} \tag{2.25}$$

$$n_u = \frac{v_c - v_s}{v_{cu}^{\Sigma}} \qquad n_l = \frac{v_c + v_s}{v_{cl}^{\Sigma}} \tag{2.26}$$

$$n_u = \frac{v_c^* - v_s^*}{v_{cu}^{\Sigma}} \qquad n_l = \frac{v_c^* + v_s^*}{v_{cl}^{\Sigma}} \tag{2.27}$$

$$n_u = \frac{V_{dc} - v_a^*}{2V_{dc}} \qquad n_l = \frac{V_{dc} + v_a^*}{2V_{dc}} \tag{2.28}$$

2.6.5 Sum-capacitor-voltage ripple ($\Delta v_{cu,l}^{\Sigma}$)

The averaging principle can be extended for calculating sum-capacitor-voltage ripple ($\Delta v_{cu,l}^{\Sigma}$). The optimal value of submodule capacitance can be chosen using this expression as well. Equation 2.23, 2.24 and 2.28 can be combined to obtain equation 2.29. Equation 2.30 can be written by multiplying both sides by $v_{cu,l}^{\Sigma}$. The right-hand side of equation 2.31 can be written in terms of arm energies ($W_{u,l} = C_s\left(v_{cu}^{\Sigma}\right)^2/2N$) and it is replaced in equation 2.32. Calculation of the voltage ripple becomes easier by introducing the variable energy per leg energy (W_{Σ}) and imbalance energy (W_{Δ}). Equations 2.33 represents the result of addition and subtraction of two equations.

$$\frac{C_s}{N}\frac{dv_{cu}^{\Sigma}}{dt} = \frac{v_c^* - v_s^*}{v_{cu}^{\Sigma}}\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C_s}{N}\frac{dv_{cl}^{\Sigma}}{dt} = \frac{v_c^* + v_s^*}{v_{cl}^{\Sigma}}\left(-\frac{i_s}{2} + i_c\right) \tag{2.29}$$

$$\frac{C_s}{N}v_{cu}^{\Sigma}\frac{dv_{cu}^{\Sigma}}{dt} = (v_c^* - v_s^*)\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C_s}{N}v_{cl}^{\Sigma}\frac{dv_{cl}^{\Sigma}}{dt} = (v_c^* + v_s^*)\left(-\frac{i_s}{2} + i_c\right) \tag{2.30}$$

$$\frac{C_s}{2N}\frac{d\left(v_{cu}^{\Sigma}\right)^2}{dt} = (v_c^* - v_s^*)\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C_s}{N}\frac{d\left(v_{cl}^{\Sigma}\right)^2}{dt} = (v_c^* + v_s^*)\left(-\frac{i_s}{2} + i_c\right) \tag{2.31}$$

$$\frac{dW_u}{dt} = (v_c^* - v_s^*)\left(\frac{i_s}{2} + i_c\right) \qquad \frac{dW_l}{dt} = (v_c^* + v_s^*)\left(-\frac{i_s}{2} + i_c\right) \tag{2.32}$$

$$\frac{dW_{\Sigma}}{dt} = 2v_c^* i_c - v_s^* i_s \qquad \frac{dW_{\Delta}}{dt} = v_c^* i_s - 2v_s^* i_c \tag{2.33}$$

Further simplification of equation 2.33 is done by substituting $v_s^* = V_s\cos(w_1 t)$ for the reference output voltage, $i_s = I_s\cos(w_1 t - \varphi)$ for the output current with inductive load, $v_c^* = V_{dc}$, and $i_c = P/6V_{dc}$ for circulating current. From here, it can be concluded that it is not possible to adapt this proof for high voltage testing application since it is not possible to represent the output current with a continuous expression. Hence a different approach should be used to understand the discrete behaviour of MMC and it is done in chapter 4.

2.7 Analysis of the output voltage

Generally, the converter output is a switching waveform which contains higher order harmonics in addition to the fundamental frequency. The quality of such a waveform can be determined by means of Fourier analysis, when the signal is sinusoidal. The detail about Fourier analysis

can be found in this reference [18], but the most important factor is total harmonic distortion (THD). The mathematical expression of THD is as follows:

$$\% THD = 100 \times \frac{I_{dis}}{I_{s1}} \tag{2.34}$$

Here I_{dis} is the amount of distortion in the waveform. I_{s1} is fundamental harmonic of the waveform, and $\% THD$ expresses the amount of distortion in the output signal. It is not possible to use this criterion for non-sinusoidal signals since the frequency spectrum contains many frequencies unlike pure sinusoidal waveforms. Chapter 3 discusses the time domain criterion for calculating the optimal number of submodules for both sinusoidal and non-sinusoidal wave shapes. The quality of HV test signals is measured in terms of its steepness and maximum voltage level rather than the harmonic performance.

2.8 Summary

The key difference lies in their philosophies. For conventional MMC, it is **"*sinusoidal and continuous output current with closed loop control to transfer power*"**. For HV testing application, it is **"*pulse shaped and discontinuous output current with open loop control to generate arbitrary wave shapes across HV TO with low output current*"**. This makes the overall structure of the MMC single phase with half bridge submodule topology. Design choices regarding control systems and converter parameters becomes more complicated and addressed separately in the following chapters.

Table 2-1: Summary of key differences between power application and high voltage testing application

	Power	**High voltage testing**
Philosophy	To achieve power conversion from AC to DC and DC to AC at high voltage	To generate arbitrary wave shapes at high voltage
Overall circuit structure	3 legs	1 leg
Submodule topology	Depending on the circuit requirements, DC fault-tolerant topology can be preferable over half bridge topology	Half bridge topology can be a satisfactory choice
Control scheme	Interleaved and closed loop control	Open loop control
Arm resistance	Stray component	Not a stray component. A new design criterion must be proposed
Arm inductance	• Reduce circulating current • Limit the steep rise in current (di/dt)	• It is not applicable • The same criteria can be used
Submodule capacitance	Design criterion based on the power rating of the converter	A new design criterion must be developed

Mathematical model	The model is developed based on continuous operation of the converter with sinusoidal output current	A new model must be developed for discontinuous operation of the converter with pulsed shape output current
Analysis of output voltage	The quality of the generated voltage signals is measured in terms of THD	Steepness and peak magnitude determines the quality of the generated non-sinusoidal voltage signals

3. CONTROL SYSTEM OF THE TEST SOURCE

The control system of an MMC is complex with many control loops interleaved as discussed in the last chapter. This chapter aims to compare the performance of modulation techniques and proves that it is possible to have an open loop control system for high voltage testing application. An optimal number of submodules is chosen for the small-scale prototype design.

3.1 Review of modulation techniques

MMC is introduced as alternative for many multilevel and cascaded topologies for medium and high voltage power applications. Modulation techniques for these existing topologies have been adapted for MMC and its classification is shown in figure 3-1.

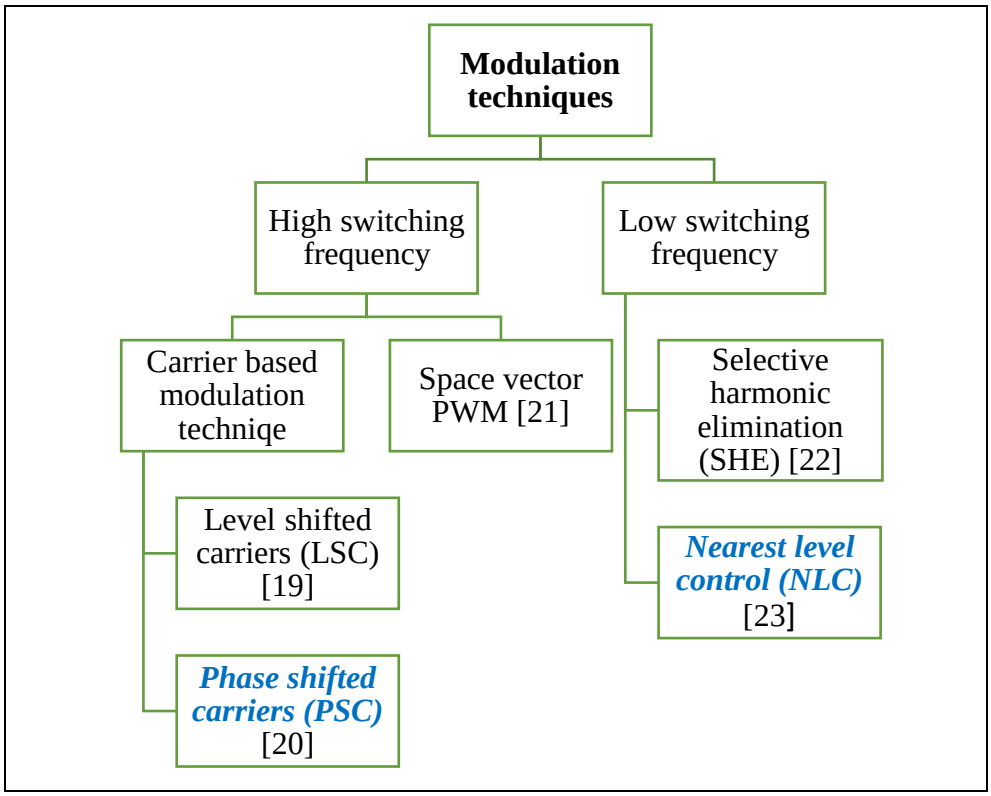


Figure 3-1: Classification of modulation technique

The modulation techniques are broadly classified based on the switching frequency obtained in the output signal. High switching modulation techniques generate PWM signal with switching frequency in the range of kHz, whereas low switching modulation techniques generate a stair case signal with switching frequency comparable to the fundamental frequency (50 Hz).

Modulation techniques with high switching frequency involves the classical approach of using carrier signals or using space vectors. In the carrier-based modulation, every submodule in the MMC has a separate carrier and gate pulses are generated by comparing it with a reference signal. Carriers for different submodules can be either level shifted in amplitude or phase shifted in the time domain as shown figure 3-2. Lower submodules are used more than higher submodules in case of level shifted carrier (LSC) modulation, whereas phase shifted carrier (PSC) modulation divides the use of submodules evenly by itself. That is why PSC is chosen for implementing high frequency switching modulation over LSC.

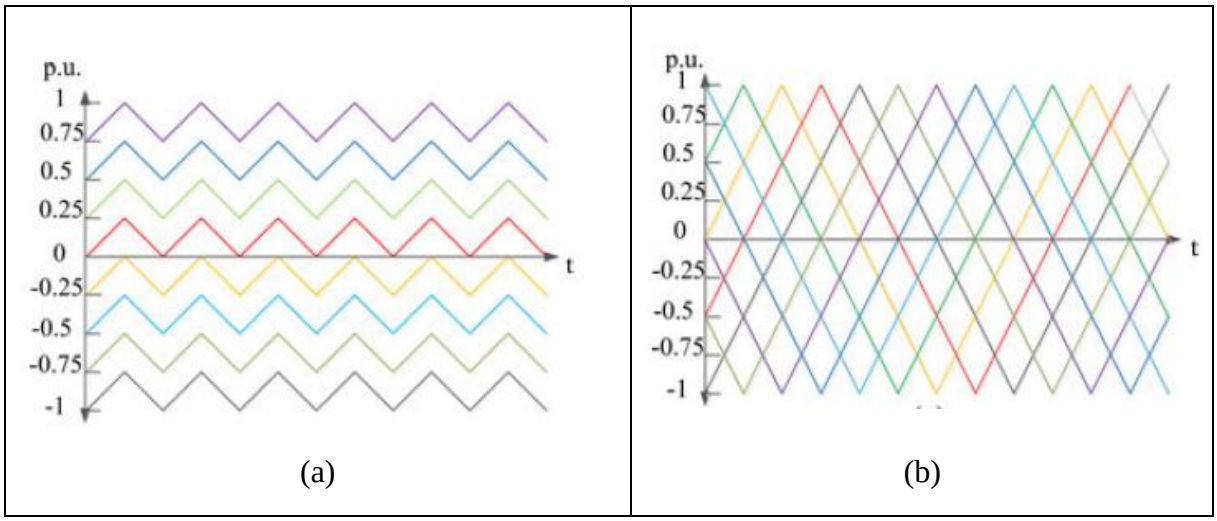


Figure 3-2: Carrier signals for (a) LSC (b) PSC [24]

In space vector modulation (SVM), duty cycles of switches to synthesize a desired output voltage on average are calculated without the use of a carrier waveform. For two level converters, the reference signal can be constructed using 8 possible states of switches, as shown in figure 3-3. 8 possible states are present since there are 6 switches (2 per each phase) and their behavior is complementary. Figure 3-3 displays a space vector ($\overrightarrow{U_S}$) which is constructed by the time average of adjacent vectors $\overrightarrow{U_S}(110)$ and $\overrightarrow{U_S}(100)$. For two level SVM, the implementation effort is significantly reduced since there are no carrier waveforms. For multilevel SVM, the simple hexagon structure is replaced by multiple concentrated hexagon structure as shown in figure 3-3(b). With such a complex structure for multilevel converter, the implementation effort does not reduce. For this reason, this modulation technique is not investigated further in this thesis.

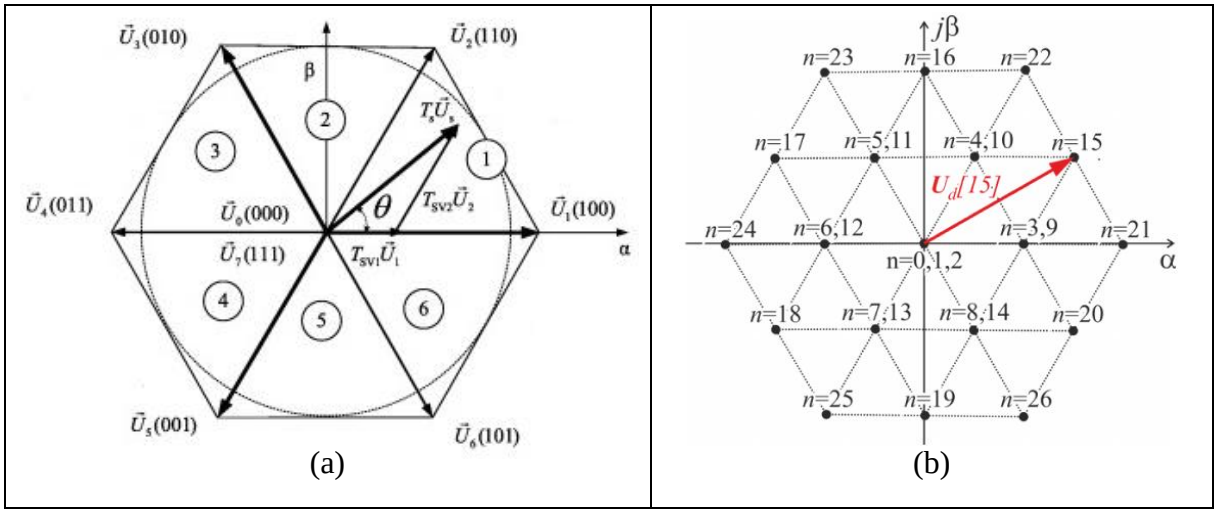


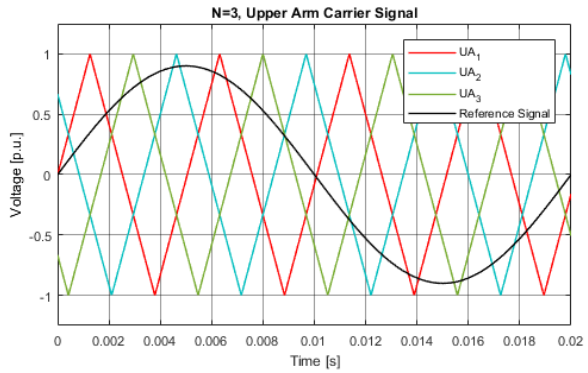
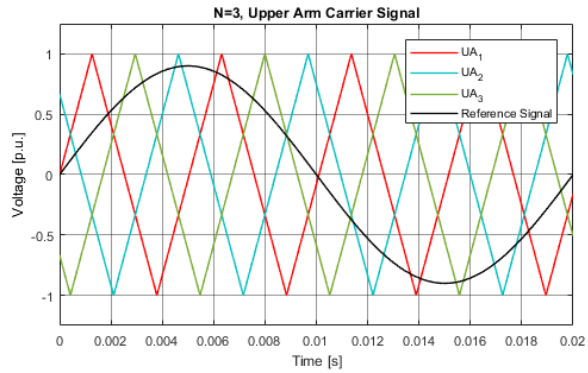
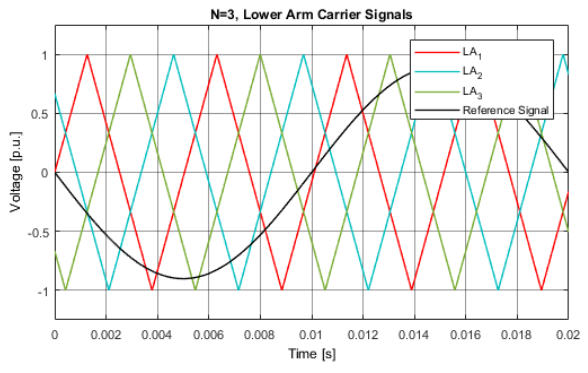
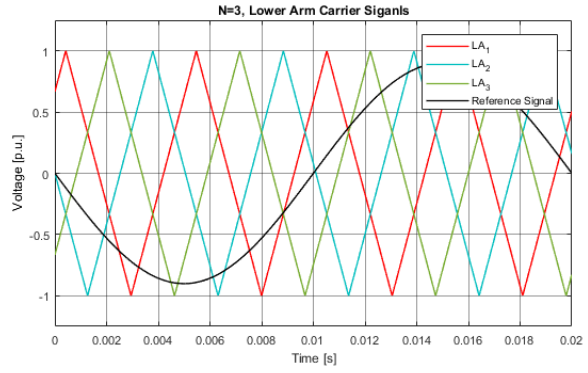
Figure 3-3: SVM for (a) 2 level converter [25] (b) 3 level converter [26]

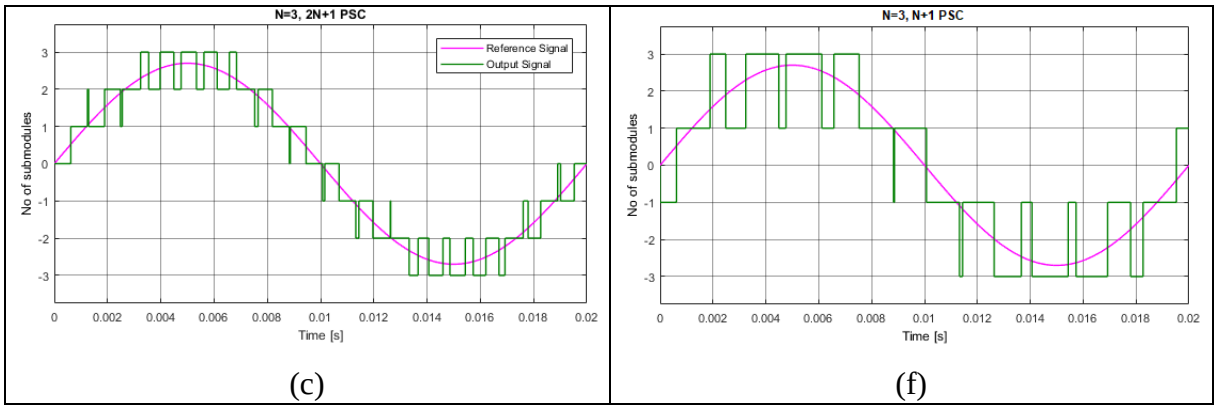
Modulation techniques with low switching frequency don't use carrier signals, but gate pulses are preprogramed to obtain the desired signal. Low switching modulation techniques include selective harmonic elimination (SHE) and nearest level control (NLC). In SHE, gate pulses are generated to obtain the desired harmonic performance and hence it is suitable for power applications of MMC with sinusoidal wave shape. That is why only NLC can be chosen from

low switching frequency modulation technique for high voltage testing application. Many researchers have worked on comparing the performance of these modulation techniques for the optimal converter operation. The focus in this thesis is to prove that the MMC can generate non-sinusoidal signals across a high voltage test object. Hence two modulation techniques are chosen and further investigated, one from the high frequency switching techniques (PSC) and one from the low frequency switching techniques (NLC). Each modulation technique is studied in detail in the following section.

3.2 Phase Shifted Carrier (PSC)

In PSC, each submodule is assigned with a carrier signal and they are phase shifted by $2\pi/N$ for the submodules in an arm. Upper arm and lower arm can use the same carrier signals, or they can be phase shifted by π or π/N. It is analytically proven that optimal harmonic performance can be obtained with π/N phase difference in case N is even and 0 phase difference in case N is odd [27]. With the mentioned phase difference, $2N+1$ levels can be obtained from N submodules and hence it has better harmonic performance. PSC modulation for $N=3$ is simulated for both phase difference and the results are shown in figure 3-4.

$2N+1$ PSC	**$N+1$ PSC**
 (a)	 (d)
 (b)	 (e)



(c) (f)

*Figure 3-4: **2N+1 PSC** (a) Carrier signals for upper arm (b) Carrier signals for lower arm (c) Output voltage; **N+1 PSC** (d) Carrier signals for upper arm (e) Carrier signals for lower arm (f) Output voltage*

In figure 3-4, two reference signals are used with same magnitude, but phase shifted by π. With the half bridge submodule topology, it is possible to generate gate pulses using only one reference signal [28], by taking advantage of the complimentary behavior of switches. The output waveform is generated by adding the gate pulses generated and hence it is shown in terms of number of submodules. For a modulation index of 0.9, the output waveform has 7 and 4 levels for $2N + 1$ PSC and $N + 1$ PSC respectively.

The information about the required phase differences for odd and even number of submodules is tabulated in table 3-1.

Table 3-1: Carrier signal details for PSC

	2N+1 PSC	**N+1 PSC**
N is Odd	Same carrier signals for upper and lower arm	Carrier signals are phase shifted by π/N for upper and lower arm
N is even	Carrier signals are phase shifted by π/N for upper and lower arm	Same carrier signals for upper and lower arm

3.3 Nearest level control (NLC)

Nearest level control calculates how many sub modules should be inserted to generate the required voltage waveform. The calculation of insertion indices is shown in equation 2.23 and the same equation is used with an added operation of rounding. The number of submodules to be inserted must be an integer and hence the rounding operation is important.

$$N_u = round\left(\frac{N\left(V_{dc} - V_{ref}\right)}{2V_{dc}}\right) \tag{3.1}$$

$$N_l = round\left(\frac{N\left(V_{dc} + V_{ref}\right)}{2V_{dc}}\right) \tag{3.2}$$

After implementing this mathematical expression in MATLAB-Simulink, the desired waveform can be generated as shown in figure 3-5.

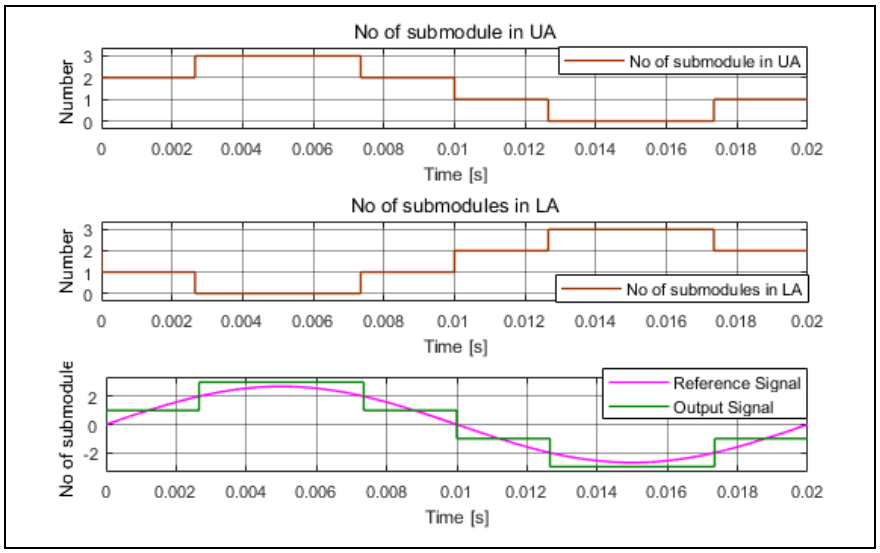


Figure 3-5: Working principle of NLC

3.4 MATLAB-Simulink implementation

The gate pulses generated by the mentioned modulation techniques are directly applied to the converter modules' switches for realizing the converter behavior under open loop control. From the mentioned range of test objects in the introduction, 50 nF capacitance is used in the simulation as the extreme case. Converter parameters (C_s, L_a, R_a & F_s) are not optimized since the focus is to study the modulation techniques. Converter parameters used for these simulations are shown in table 3-2. Details about the Simulink implementation can be found in Appendix A.

The converter behavior is studied using output current, circulating current and submodule capacitor voltages. With direct modulation, the first submodules from both arms get inserted most and hence only capacitor voltage waveforms of only those submodules are shown. For all mentioned waveforms in the introduction, the converter behavior is studied for 50 Hz sinusoidal (normal case) and switching impulse (extreme case).

Table 3-2: Converter parameters

Parameter name	**Parameter value**
Number of submodules (N)	3
Submodule capacitance (C_s)	10 µF
Arm inductance (L_a)	10 µH
Arm resistance (R_a)	100 Ω
Switching frequency (F_s)	498 Hz
Load capacitance (C_o)	50 nF

3.4.1 2N+1 PSC

As expected, the output voltage waveform of sinusoidal signal (bipolar) in figure 3-6 has 2N+1 voltage levels. For the case of a switching impulse (unipolar), the number of levels is an integer number calculated using $\left(\frac{2N+1}{2}\right)$. An additional N number of levels are produced because the converter consists of additional states apart the ones which are mentioned while introducing the converter. As discussed in the introduction to the converter, total number of inserted submodules in the upper and lower arm is constant. In case of 2N+1 PSC modulation technique,

the number of inserted submodules can be N, N+1 or N-1. In these situations, the imbalance between the DC link and converter leg creates a large circulating current resulting in a large capacitor voltage ripple. Both these conditions can be observed from figure 3-6 for both signal waveforms. This is the reason why conventional PSC modulation is implemented with a closed loop control to maintain circulating current and average submodule capacitor voltage [29]. The idea is to modify the reference voltage signal to maintain these two quantities for each submodule. Hence multiple reference voltage signals are required for each submodule in the converter.

Since the output current is not controlled, current is discontinuous, and it is pulse shaped. These current pulses charge/discharge the load capacitance when the output voltage changes a level.

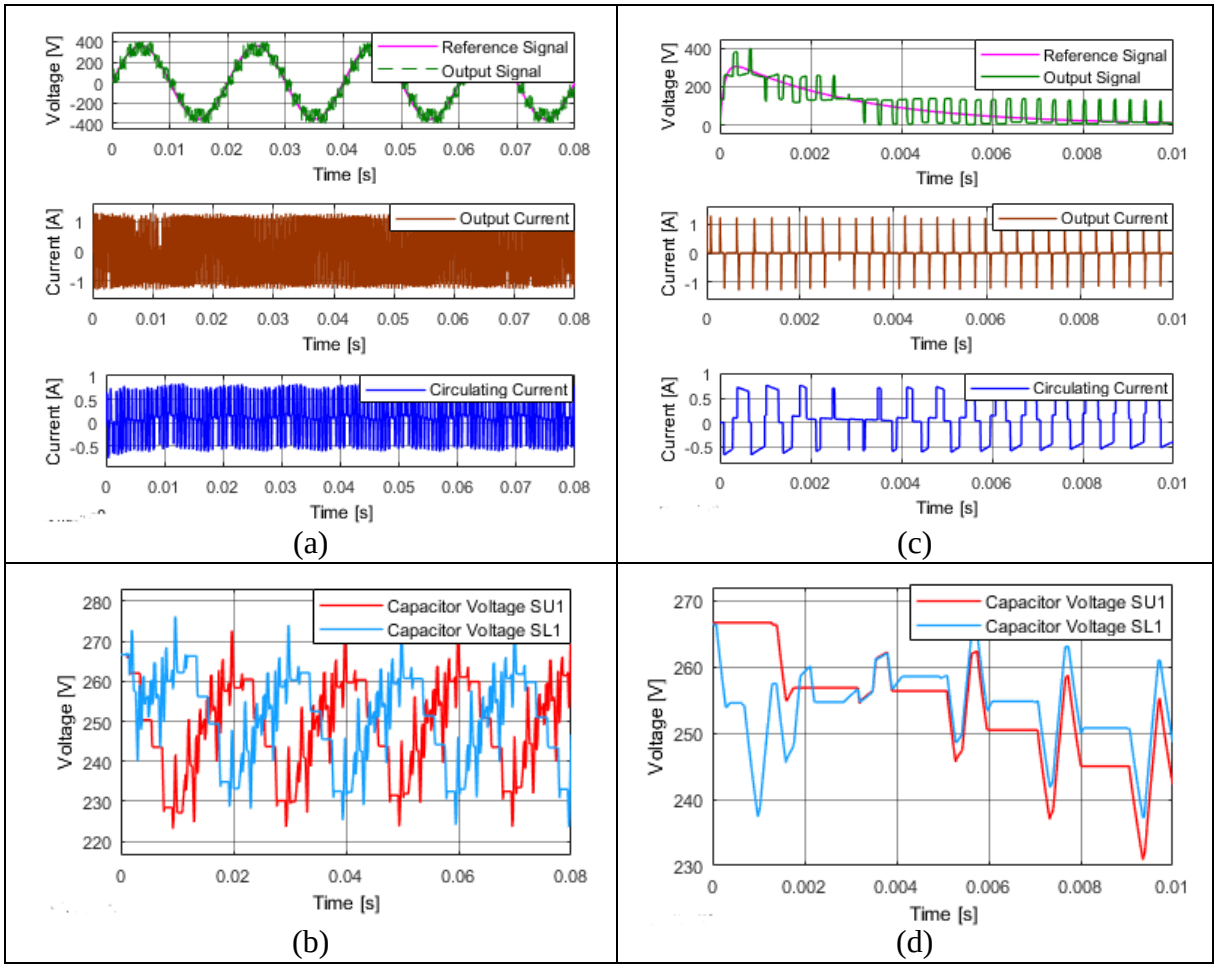


Figure 3-6: 2N+1 PSC with N=3 for 50 Hz sinusoidal (a) output current and circulating current response (b) capacitor dynamics, and for Switching impulse (c) output current and circulating current response (d) capacitor dynamics

3.4.2 N+1 PSC

In case of N+1 PSC, total number of submodules in the upper and lower arm are maintained at N and hence it can be observed from figure 3-7 that the circulating current magnitude is very small (in mA). With small circulating current, the submodule capacitor voltage ripple is small. But, the submodule capacitor voltage waveforms are drifting away from the average value over the period of time. Hence this type of modulation technique should be implemented with accurate sorting or submodule selection process [30] cycles.

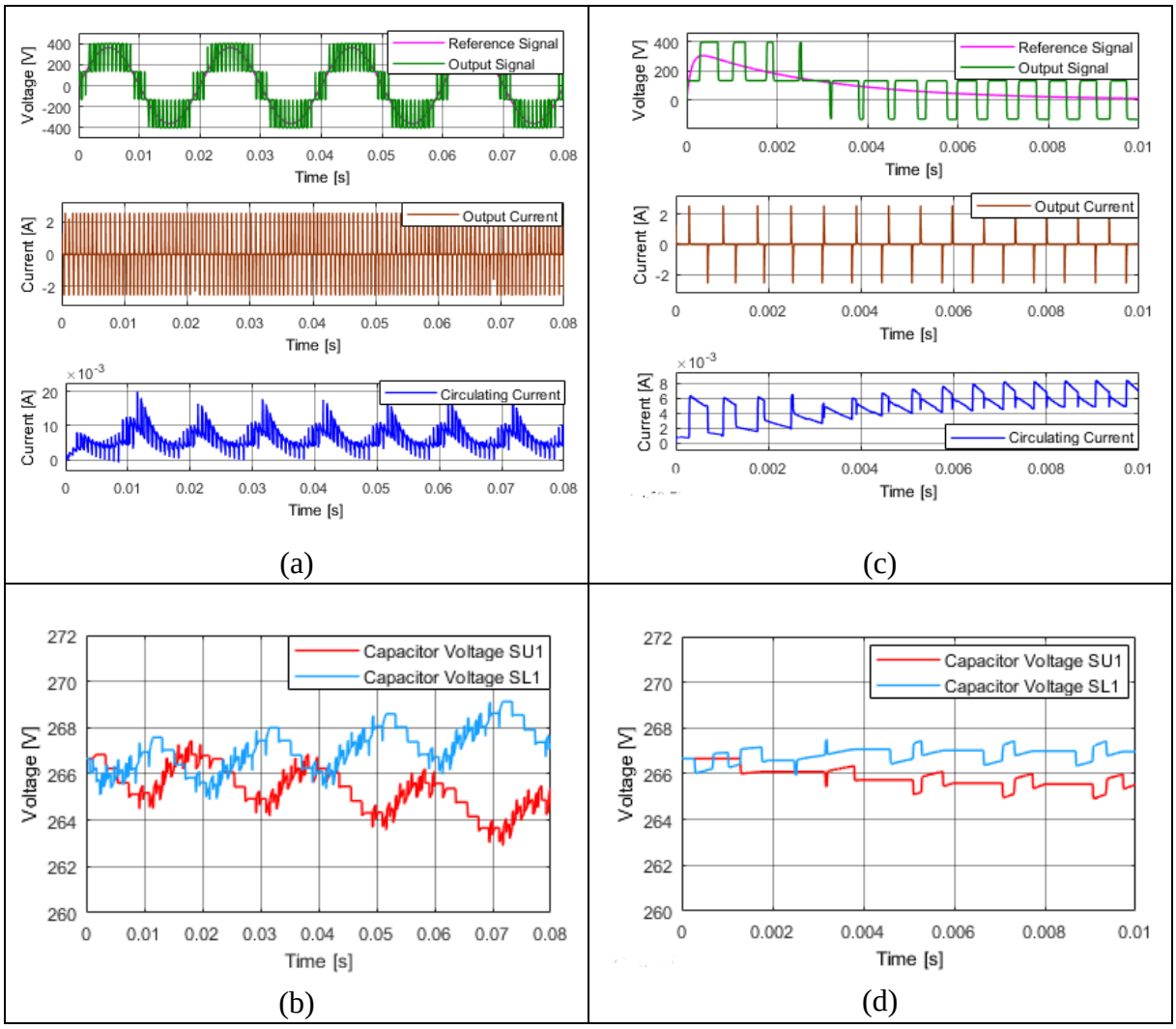


Figure 3-7: N+1 PSC with N=3 for 50 Hz sinusoidal (a) output current and circulating current response (b) capacitor dynamics, and for Switching impulse (c) output current and circulating current response (d) capacitor dynamics

3.4.3 NLC

The effect of low frequency modulation technique is clearly seen with the stair case output voltage waveform in figure 3-8. Here, the switching frequency depends upon the modulation index (m_{req}) and the number of submodules. A pulse shaped output current is present only when there is a level change in the output voltage. Within this modulation technique, the nature of the circulating current is like the output current with a slower response and small magnitude. The submodule capacitor voltage ripple is small, and not drifting away from the average value.

When m_{req} changes to a smaller value, not all submodules from an arm will get inserted. It means that some submodules from an arm will be always inserted if the sorting algorithm is not implemented. This case is studied with m_{req}=0.65 and it can be seen from figure 3-9 that the submodule capacitor voltage is deviating away from the average value. When the output signal is generated by the converter for a longer time, these voltage magnitudes will keep deviating which is not desirable. Hence usually NLC is implemented with a sorting algorithm and that includes conventional sorting [9], tolerance band sorting [31], and predictive sorting [32].

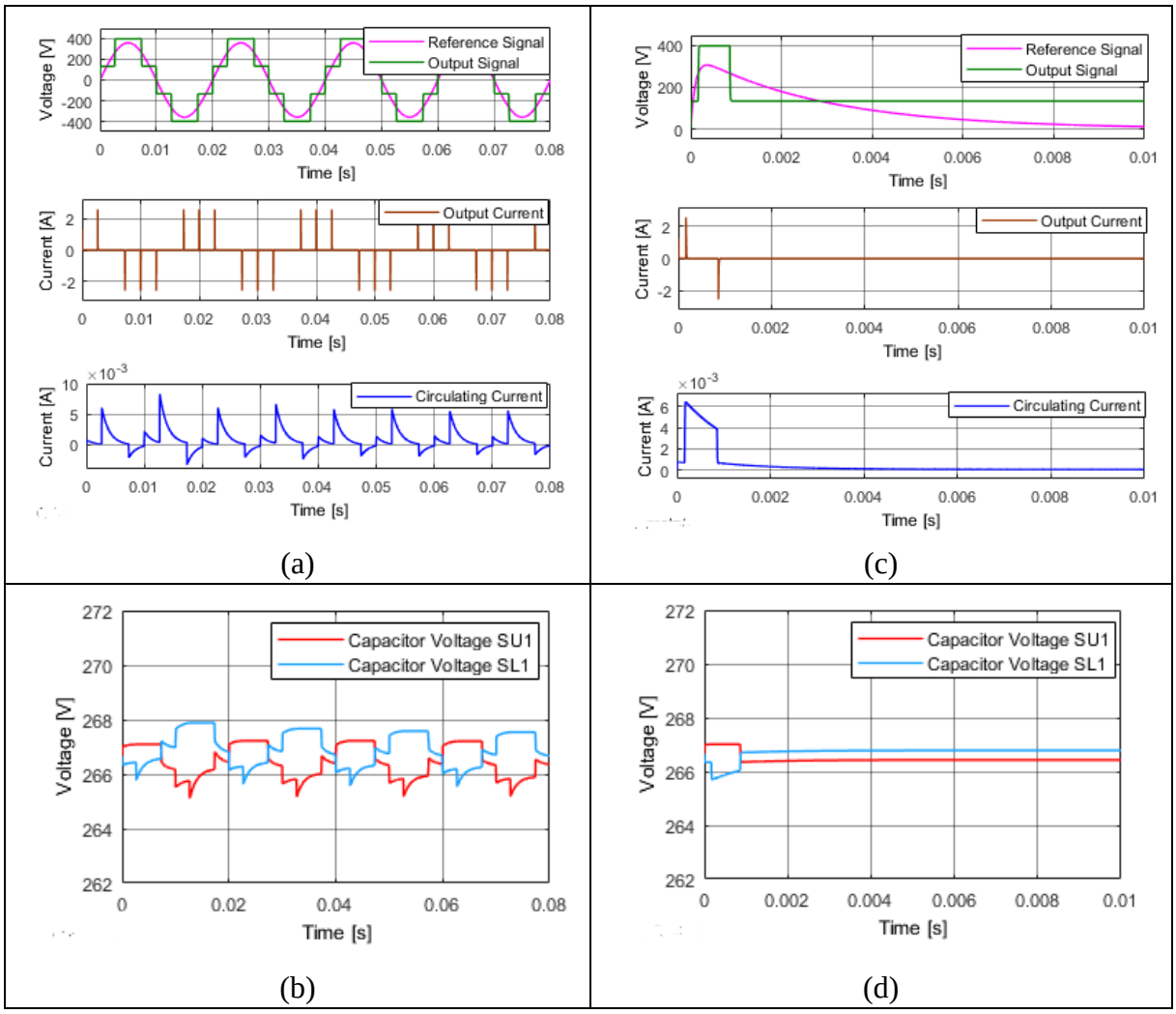


Figure 3-8: NLC with N=3 and m_{req} = 0.9 for 50 Hz sinusoidal (a) output current and circulating current response (b) capacitor dynamics, and for Switching impulse (c) output current and circulating current response (d) capacitor dynamics

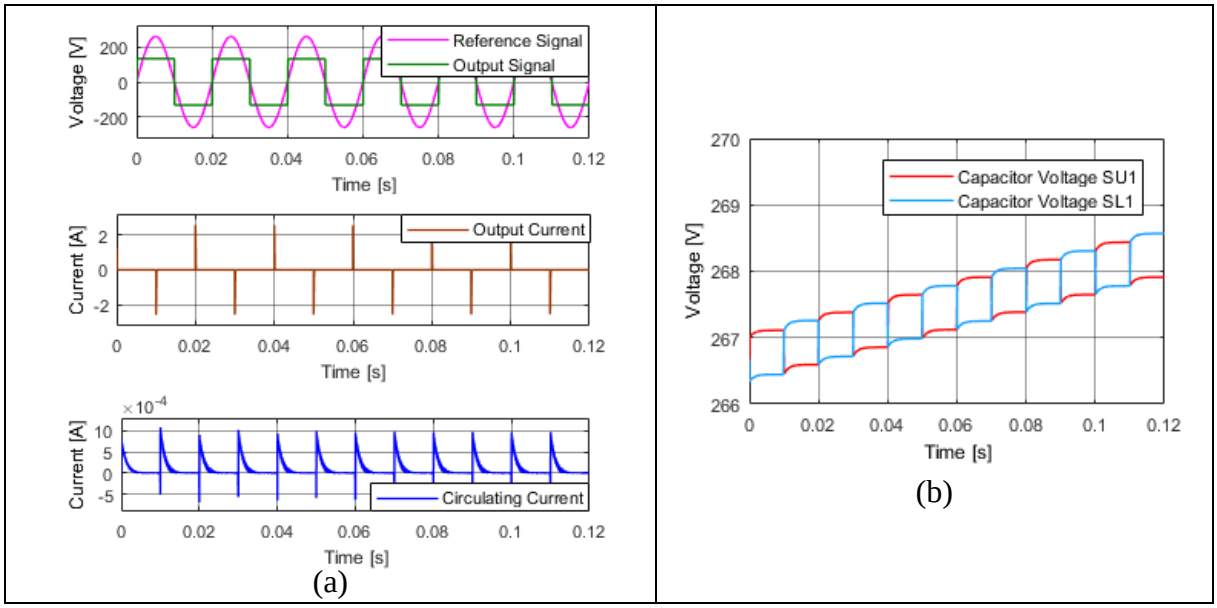


Figure 3-9: NLC with N=3 and m_{req} = 0.65 for 50 Hz sinusoidal (a) output current and circulating current response (b) capacitor dynamics

3.5 Comparison of NLC and PSC

From the above observations, the performance of these modulation techniques based on the following points as shown in table 3-3.

Table 3-3: Comparison of modulation techniques

	2N+1 PSC	**N+1 PSC**	**NLC**
No of reference signal	Multiple	One or two	Two
No of carrier signals	N is odd – N N is even – 2N	N is odd – 2N N is even – N	Not applicable
Additional controller required	Yes	No	No
Circulating current present	Yes	Very low	Very low
Implementation effort	High as $N \uparrow$	Moderate	Low
Filter requirement	High	High	Comparatively low

The implementation complexity decision is based on the computational efforts to generate gate pulses. The computational efforts increase with the of submodules due to comparison operation getting performed for every submodule. In case of 2N+1 PSC modulation technique, a closed loop control methodology implemented per submodule with the feedback of submodule capacitor voltage and circulating current increases computational efforts even further. Whereas, implementing NLC with predictive sorting will make the physical implementation much easier for large value of N. This is important since the HV test source is envisioned to generate voltage wave shapes in the range of kV and MV which requires large number of N.

Secondly, the filter requirement to obtain a smooth output signal should be studied. PSC generates a PWM output signal, whereas NLC generates a stair case output signal. These higher order harmonics from the converter output must be removed using an appropriate design of a filter. With PSC modulation technique, these carrier harmonics shift to $N.F_s$ frequency [8]. This makes the filter realization easier for sinusoidal signals since they contain only one frequency. For other non-sinusoidal signals, it could be hard to filter the higher order switching harmonics. The stair case signal of NLC with large number of submodules will have small step in the output signal which will make the output signal closer to the desired reference signal. Considering these two facts, NLC is chosen as a modulation technique to generate arbitrary wave shapes from a MMC.

3.6 Choice of number of submodules

For power applications of MMC, number of submodules is chosen based on the DC link voltage and available blocking capability of switches. State of the art IGBTs used in HVDC application can block 4.5 kV, even though 6.5 kV devices are available. With a higher number of submodules, the output voltage waveform is closer to desirable wave shape. Figure 3-10 shows converter output signal with N=100. The output signal is following the reference signal closely

since the voltage step is very small with N=100. But large value of N might increase the cost and size of the converter.

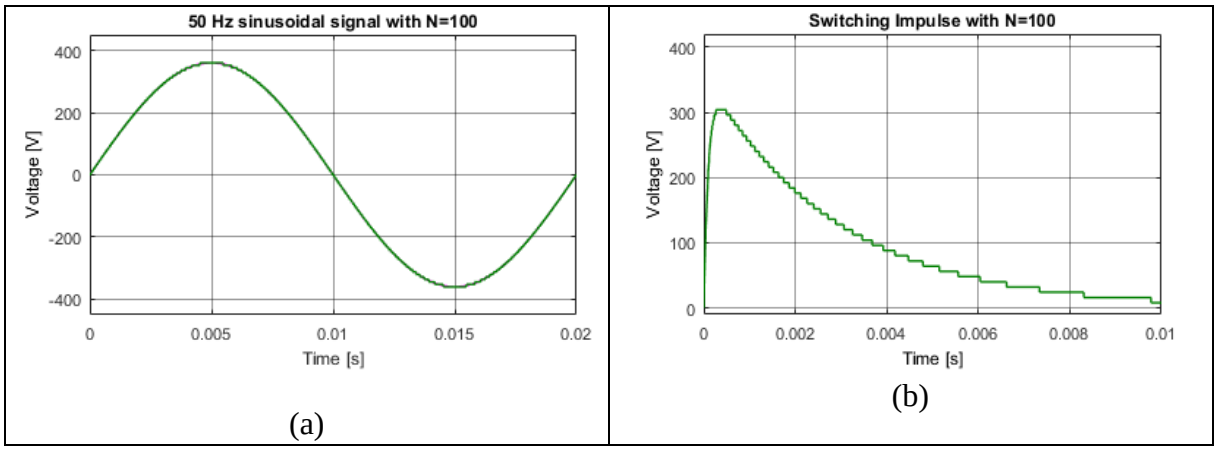


Figure 3-10: Converter output signal with N=100 (a) 50 Hz sinusoidal (b) Switching impulse

For the small-scale prototype (400 V), the choice of N is not constrained with the available blocking capability of switches. Hence the choice of N is decided based on a trade-off between circuit complexity and significant cost combined with filter requirement to obtain a smooth wave shape for testing. Harmonic performance of the converter output signal is decided based on the THD value for sinusoidal signal. Since it is not possible to use THD for non-sinusoidal signal, the optimal value of N is found by performing error analysis on output signal and reference signal in time domain. When the output signal is subtracted from the reference signal, it gives an error signal. Area under the absolute of error signal can be used to quantify how well the output signal is following the reference signal. Even number of submodules are preferred since it generates odd number of levels (N+1) in the output signal. Odd number of levels in the output signal are better for the harmonic performance since zero voltage level is inserted

3.6.1 Error analysis

To perform error analysis on the output signal in time domain, the following steps should be followed:

1. The error signal ($error = v_{ref} - v_s$) is calculated by subtracting the reference signal from output signal. All these three signals are shown in figure 3-11 for sinusoidal signal.
2. The area (A_{error}) covered under the absolute of this error signal ($abs(error)$) will quantify the error for the generated output signal.
3. To make the error quantity independent of time, the area under curve is divided by the time duration of the signal (t_{signal}). This helps to compare signals with different time durations.
4. The percentage error with respect to DC link voltage is calculated from the error quantity calculated in step 3. Final expression of the error analysis is follows:

$$\% E = \frac{\int_0^{t_{signal}} abs(error).dt}{t_{signal}} . \frac{1}{2V_{dc}} \times 100 \tag{3.3}$$

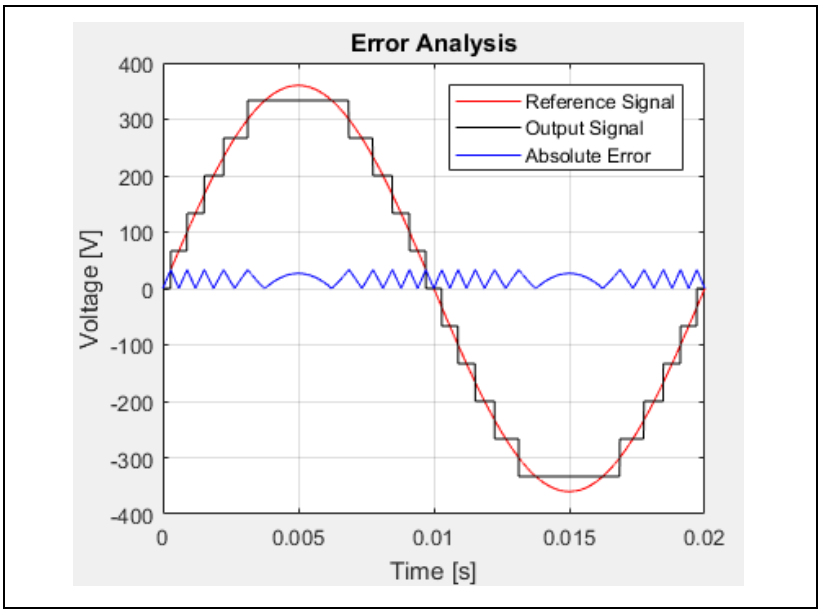


Figure 3-11: Error Analysis

3.6.2 Results of error analysis

The error expression (3.3) is used here to find the optimal value of N among the following even values of N, for sinusoidal and switching impulse.

Table 3-4: 50 Hz sinusoidal signal with m_{req} = 0.9, f_{req}=50, V_{dc} = 400V

% Error with respect to DC link voltage	N=6	N=12	N=18	N=24	N=30
NLC	9.4345	4.208	2.526	2.158	1.75

Table 3-5: Switching impulse with m_{req} = 0.9, V_{dc}=400V

% Error with respect to DC link voltage	N=6	N=12	N=18	N=24	N=30
NLC	8.029	4.604	3.072	2.249	1.782

It is obvious that percentage error value (% E) is reducing with more number of sub modules. It can be observed from table 3-4 and 3-5 that the drop-in percentage error is getting decreases after N=18 and this is true for both sinusoidal signals and switching impulses. To find more precisely the tipping point, a more detailed graph of percentage error values along with its slope is plotted in the figure 3-12. For sinusoidal signal, the slope of error value goes to zero at N=20, whereas it takes N=50 to reach zero for the switching impulse.

Assuming 3 % error value is acceptable and remaining error can be filtered later, N=14 and N=16 is the optimal value of N for sinusoidal and switching impulse.

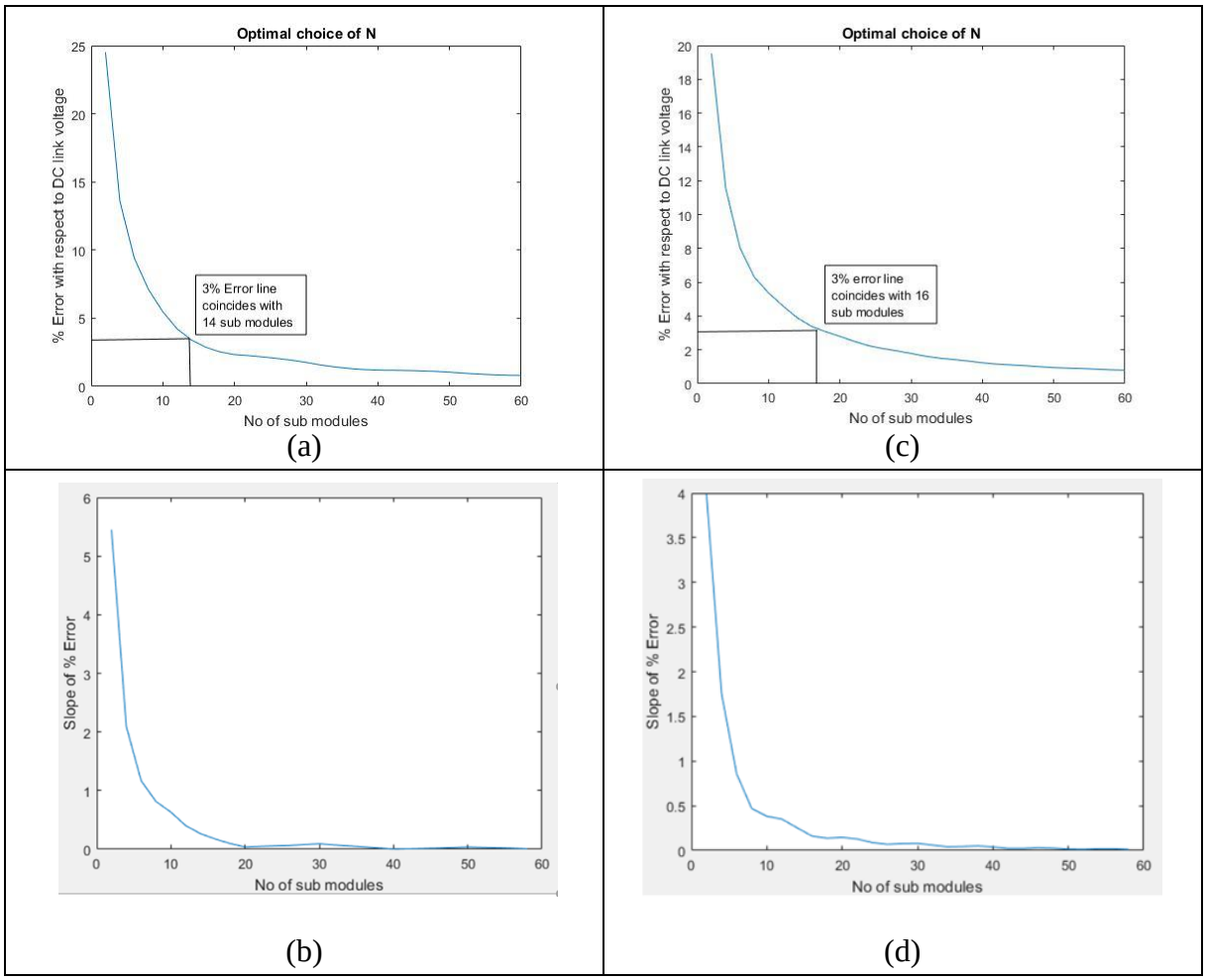


Figure 3-12: Error analysis (a) 50 Hz sinusoidal signal (c) Switching impulse, Analysis of slope of error (b) 50 Hz sinusoidal (d) Switching impulse

Considering the history of digital signal processing and how it started with 5-bit digitization, a multiple of 2 i.e. N=16 is chosen for the prototype design.

3.7 NLC + Sorting algorithm implementation

With the decision of modulation techniques and number of submodules is completed, the control system of the test source is implemented in the MATLAB-Simulink. Though NLC is chosen as a modulation technique, a discussion regarding the choice of sorting algorithm for the testing application is provided here.

Out of three mentioned sorting algorithms, conventional sorting and tolerance band sorting require capacitor voltage measurements from each submodule. The conventional sorting algorithm uses the submodule capacitor voltage and output current direction to decide which submodules are to be inserted at a given moment. When the output current is positive, submodules with lowest capacitor voltage will be inserted and vice versa. The algorithm is shown in figure 3-13. Since the submodules are sorted at each sampling instant, the algorithm is not efficient in terms of switching losses of the converter. But the algorithm has the big advantage of simple computational implementation.

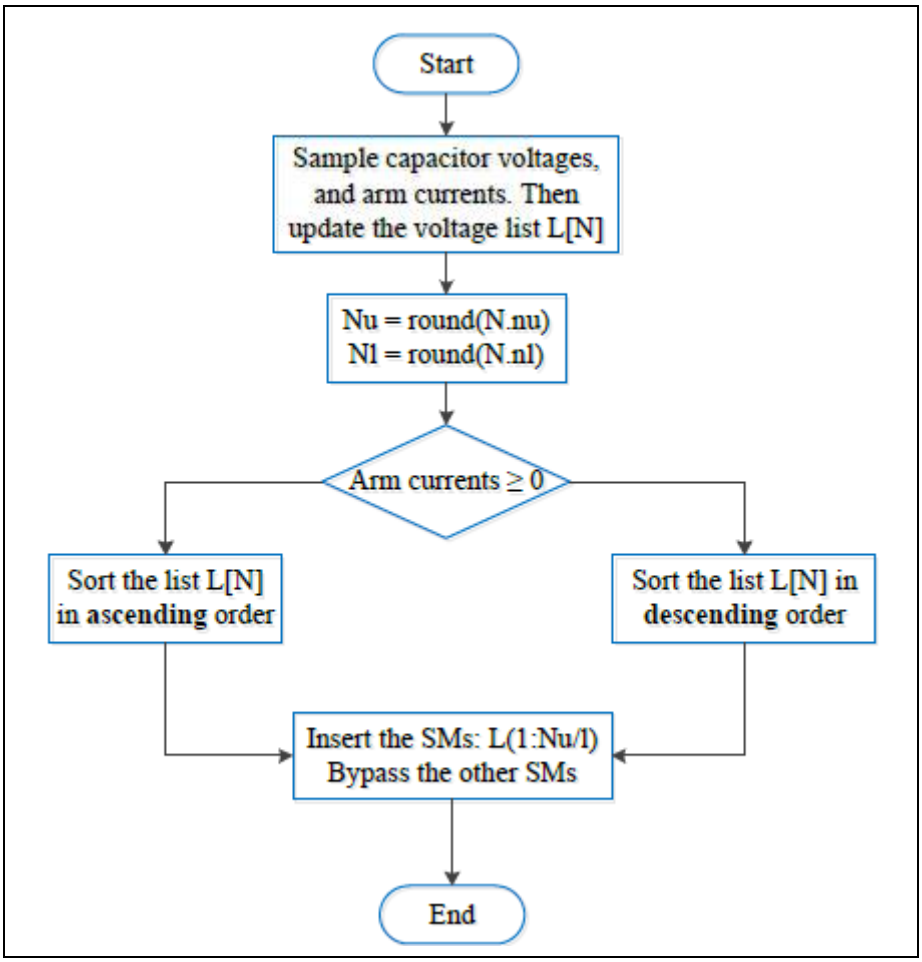


Figure 3-13: Flowchart of NLC with conventional sorting algorithm

In the tolerance band sorting algorithm, the switching losses are reduced by putting a tolerance band of δ on the capacitor voltage. Submodules are bypassed only if their capacitor voltages exceed this tolerance band $\left(\frac{v_{cu,l}^{\Sigma}}{N} + \delta\right)$. It means that the submodule will not get bypassed until it exceeds the tolerance band in either direction. The detailed steps in this algorithm is shown in figure 3-14.

Both sorting algorithms requires measurements of all submodule capacitor voltages. In contrast, predictive sorting algorithm controls the converter in such a way that the stored charge in the submodule capacitors is evenly distributed among all the submodules. The detailed mathematical analysis can be found in [32]. Though the predictive sorting algorithm does not need submodule capacitor voltage, it requires output current direction to decide whether it is charging period or discharging period.

A new modulation method has been proposed in [33] which does not require any feedback from the converter for balancing the submodule capacitor voltages. A fixed pulse pattern is chosen in such a way that the stored energy in each submodule constant. The proposed scheme changes the sequence of submodules getting inserted after every cycle. Suppose, the N^{th} submodule is inserted last in the first cycle, then N^{th} submodule will be inserted first in the second cycle. Subsequently in each cycle, the insertion of N^{th} submodule is moved to the next position. Basically, the ranking of the submodules is changed in each cycle to obtain a constant capacitor voltage.

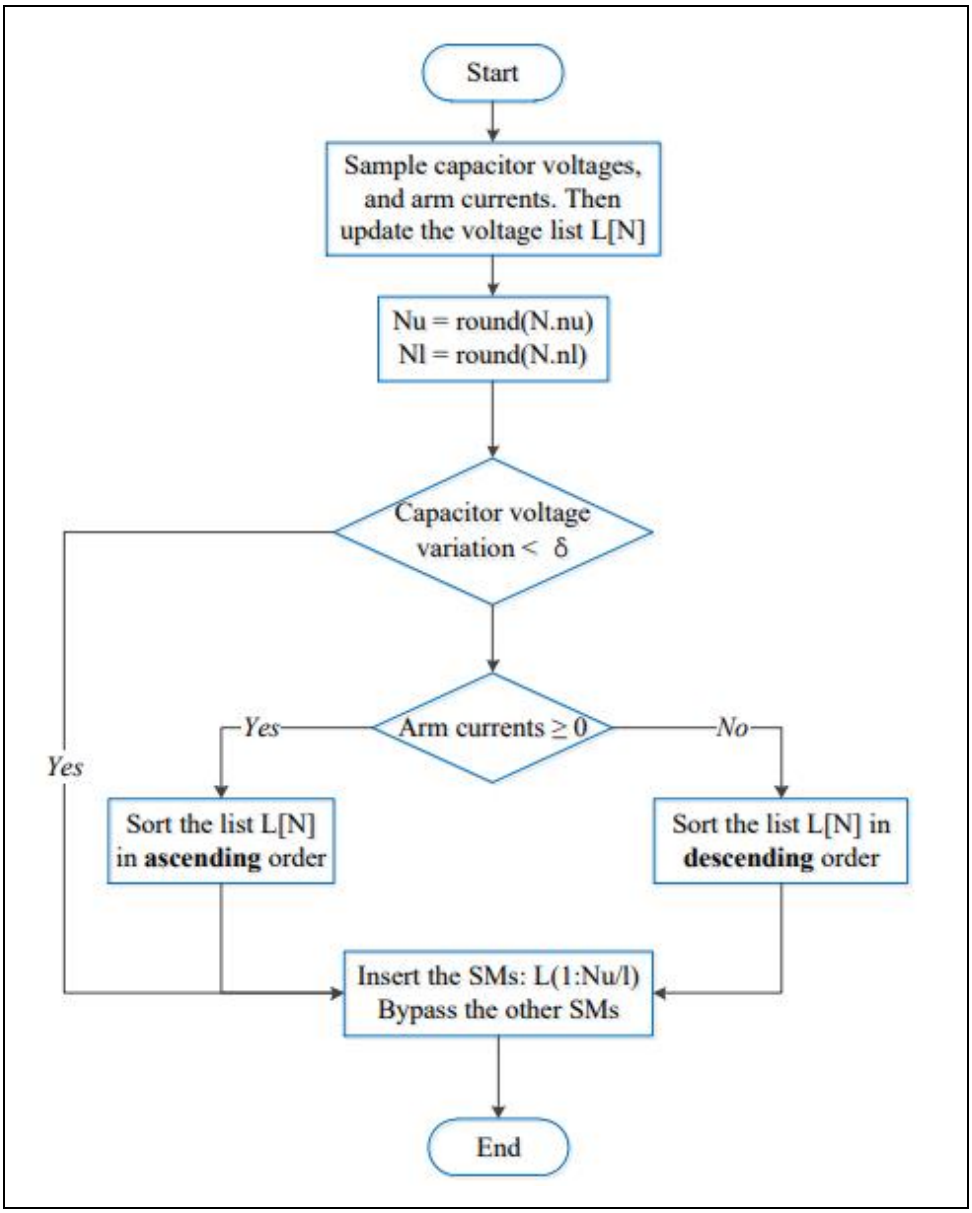


Figure 3-14: Flowchart of NLW with tolerance band sorting algorithm

The fixed pattern for N cycles is shown in the matrix expression (P) in 3.4. This pattern uses the least used submodules most in the next cycle. After implementing this algorithm to sort the submodules, for N=16 submodules with m_{req}=0.4, a constant capacitor voltage waveform is shown in figure 3-15 compared to the waveform obtained without sorting. For periodic waveform, the sequence is changed after every cycle. When a non-periodic waveform e.g. switching impulse is generated from the test source, the sequence should be changed after every impulse fired.

$$P = \begin{bmatrix} UA_1 & UA_2 & UA_3 & \cdots & UA_N \\ UA_N & UA_1 & UA_2 & \cdots & UA_{N-1} \\ UA_{N-1} & UA_N & UA_1 & \cdots & UA_{N-2} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ UA_2 & UA_3 & UA_4 & \cdots & UA_1 \end{bmatrix} \quad (3.4)$$

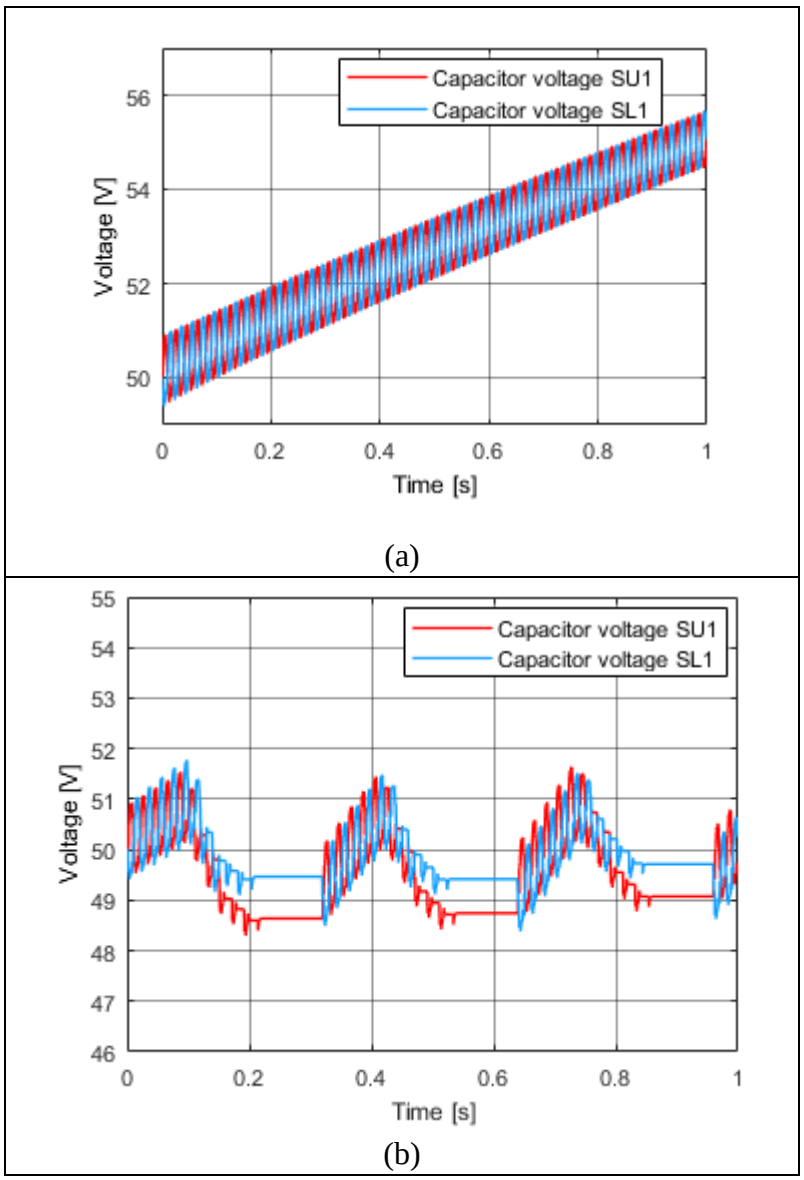


Figure 3-15: Submodule capacitor voltage SU1 and SL1 (a) without sorting (b) with sorting

The MATLAB-Simulink implementation of NLC plus sorting is discussed in Appendix A 3. One of the important consideration is the sampling frequency during sorting. It should be decided based on the switching frequency (N and f_{req}). The sampling frequency should be higher than the switching frequency not to lose any information (Nyquist criteria in signal processing).

3.8 Summary

The MMC can generate arbitrary wave shapes by substituting the desired signal as a reference and modulation technique controls switches accordingly. The performance of MMC with three different direct modulation techniques are compared based on implementation effort and filter requirement. ***Nearest level control (NLC) satisfies both criteria with added advantage of scalability of test source to higher voltage levels.*** With this modulation technique, the number of submodules is optimized to 16 for a small-scale prototype implementation (few 100 V).

4. PARAMETER DESIGN OF THE TEST SOURCE

With the control scheme and number of submodules determined, this chapter aims to derive the mathematical model of MMC with discontinuous current pulses. The model focuses on deriving submodule capacitor voltage ripple. Based on this mathematical analysis of MMC, converter parameters i.e. arm inductance, submodule capacitance, and arm resistance are designed. Current and voltage ratings of the semiconductor devices are studied based on the converter operation.

4.1 Mathematical modeling

Equation 2.14, 2.15, 2.23 and 2.24 describe the dynamic behavior of the converter. Equations 2.12 and 2.13 decouples the output current and circulating current response of the converter. Both these current values affect submodule capacitor voltages and therefore a detailed discussion about the submodule capacitor dynamics is given in the following section.

4.1.1 Output current response

The output current response is governed by equation 2.12. Equation 2.12 is rewritten with a division factor of 2 in equation 4.1. From equation 4.1, the equivalent circuit of the output current response can be drawn as shown in figure 4-1.

$$-v_s - \frac{R_a}{2}.i_s - \frac{L_a}{2}.\frac{di_s}{dt} - v_a = 0 \tag{4.1}$$

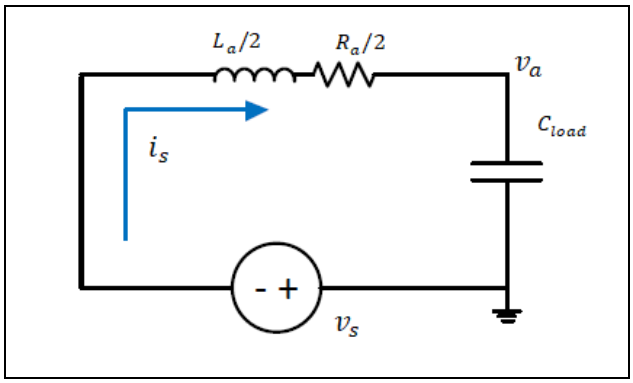


Figure 4-1: Equivalent circuit of the output current response

The inner emf v_s is built by inserting submodules from both arm and figure 4-2 shows the graph of v_s for a sinusoidal signal. It can be observed that the signal is a stair case signal. It means that the output current response can be studied by assuming v_s a step input. Since the converter operation is discontinuous, step response of the output current is important. Hence, the step response of the output current is analysed below.

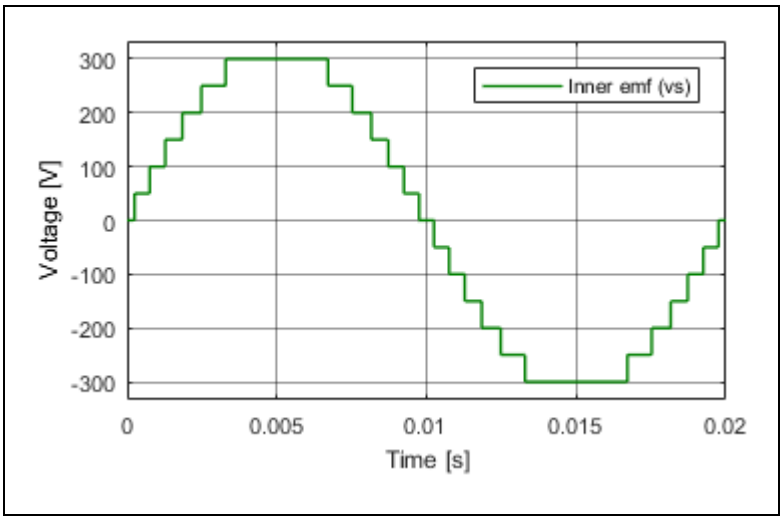


Figure 4-2: Inner emf of the converter (v_s)

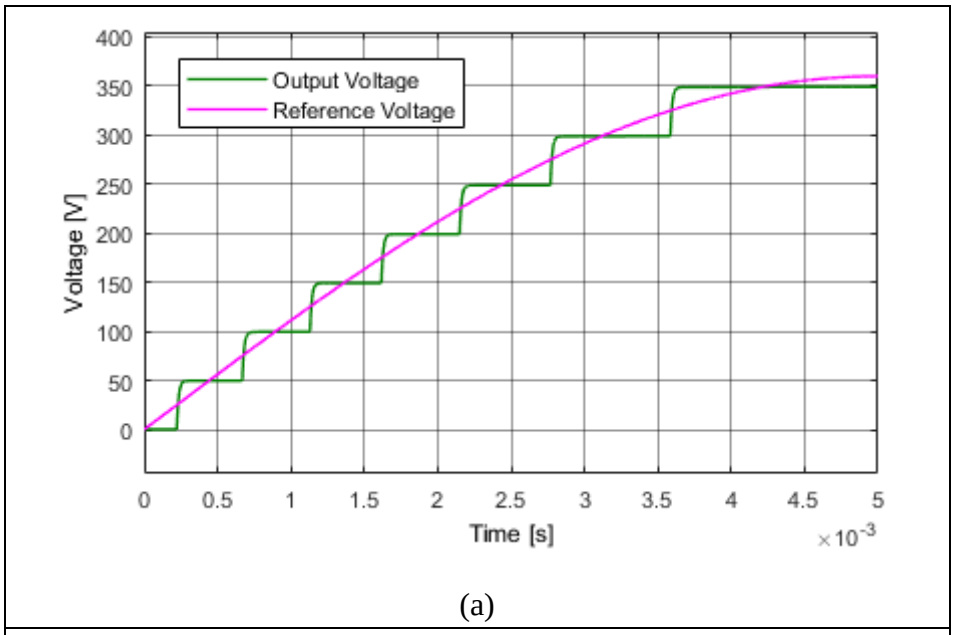
Considering ideal switches, submodules are inserted or bypassed instantly in both arms. Hence, when the switch receives the gate pulse, the action of insertion or bypassing is executed instantly. The unbalanced voltage in the arm, due to this action, comes across the arm inductance. In case of insertion of submodule capacitance, arm inductance experiences negative voltage which leads to negative arm current. Opposite phenomenon occurs in the other arm, where positive voltage is built up due to bypassing a submodule capacitance and positive arm current is generated.

Equation 4.1 can be transformed into equation 4.2 by substituting the inner emf ($v_s = -v_{cu,l}^{\Sigma}/N$) and output voltage ($v_a = \int i_s\, dt\, /C_{load}$) for a positive level change in the output voltage. Equation 4.2 can be differentiated with respect to time to obtain second order differential equation in terms of output current.

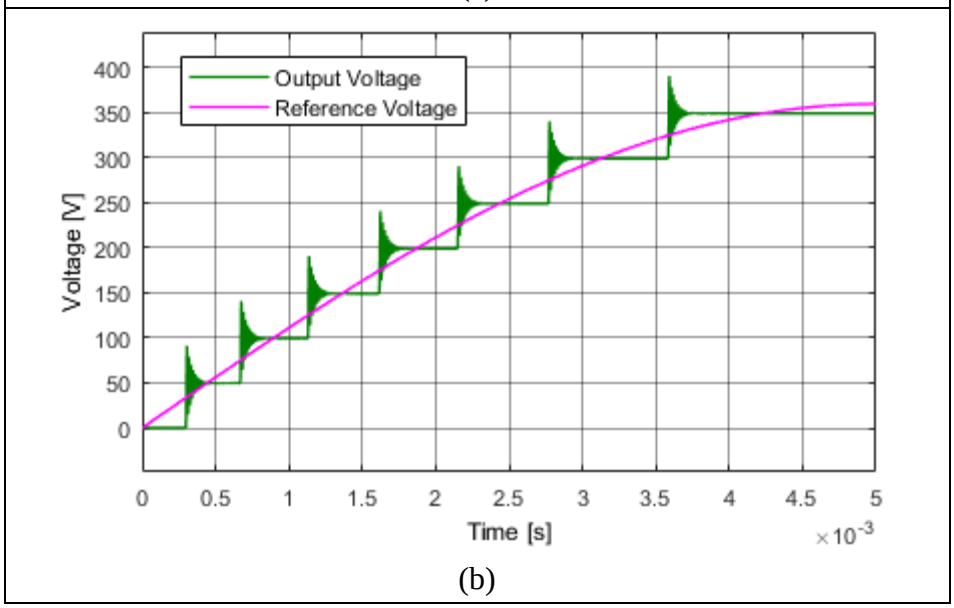
$$\frac{2v_{cu,l}^{\Sigma}}{N} - R_a.i_s - L_a.\frac{di_s}{dt} - \frac{2}{C_{load}}.\int i_s\, dt = 0 \tag{4.2}$$

$$\frac{L_a}{2}.\frac{d^2i_s}{dt^2} + \frac{R_a}{2}.\frac{di_s}{dt} + \frac{i_s}{C_{load}} = 0 \tag{4.3}$$

The homogenous solution of this second order differential equation can have three types of solution i.e. overdamped case, critically damped case and underdamped case. The last case will introduce oscillations in the output voltage which will be hard to filter to generate a smooth waveform for testing. The overdamped system will reduce the response time of the converter hence the arm resistance should be chosen to obtain critically damped system response.



(a)



(b)

Figure 4-3: Output voltage of the converter (a) Overdamped system (b) Underdamped system

The general solution of second order differential equation 4.3 is known, and it is shown in equation 4.4.

$$i_s(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{4.4}$$

where s_1& s_2 are two roots and mathematically represented as following

$$s_1 = -\frac{R_a}{2L_a} + \sqrt{\left(\frac{R_a}{2L_a}\right)^2 - \frac{2}{C_{load}.L_a}} \;\&\; s_2 = -\frac{R_a}{2L_a} - \sqrt{\left(\frac{R_a}{2L_a}\right)^2 - \frac{2}{C_{load}.L_a}}$$

If two roots of the equation are equal, then the system response is critically damped. To get the critically damped response, the values of the circuit parameters are chosen to obey the condition in equation 4.5.

$$\left(\frac{R_a}{2L_a}\right)^2 = \frac{2}{C_{load}.L_a} \tag{4.5}$$

$$R_a = \sqrt{\frac{8L_a}{C_{load}}}$$

From the output current response, it is possible to calculate the output voltage from the basic expression of capacitance. Constants A_1, A_2 & C_{int} can be calculated from the initial conditions.

$$v_a(t) = \frac{1}{C_{load}}.\int A_1 e^{s_1 t} + A_2 e^{s_2 t} dt = \frac{1}{C_{load}}\left[\frac{A_1}{s_1} e^{s_1 t} + \frac{A_2}{s_2} e^{s_2 t}\right] + C_{int} \tag{4.6}$$

4.1.2 Effect of output current on submodule capacitor

The output component of upper arm ($i_{us}(t)$) and lower arm current ($i_{ls}(t)$) have a magnitude of half of the output current, with opposite signs. For a positive change in level with positive voltage magnitude, the expression will be as follows:

$$i_{us}(t) = \frac{i_s(t)}{2} = \frac{A_1}{2} e^{s_1 t} + \frac{A_2}{2} e^{s_2 t} \tag{4.7}$$

$$i_{ls}(t) = -\frac{i_s(t)}{2} = -\frac{A_1}{2} e^{s_1 t} - \frac{A_2}{2} e^{s_2 t} \tag{4.8}$$

This shows that the effect on upper and lower arm submodule capacitance will be equal and opposite in magnitude. Considering this, the following mathematical expression is derived for upper arm current and the same magnitude with opposite sign will be assumed for lower arm submodules.

The initial conditions for the output current component of upper arm current are shown in equation 4.9. First initial condition is obvious since current is present only when there is switching, otherwise it is zero. The second initial condition comes from the arm inductance dynamics ($L_a di_{us}/dt$) since average submodule capacitor voltage $v_{cu,l}^{\Sigma}/N$ is experienced by the arm inductance as explained above. Using these two initial conditions, it is possible to derive expressions for A_1 & A_2.

$$i_{us}(0) = 0\,; \qquad \frac{di_{us}}{dt}(0) = \frac{v_{cu,l}^{\Sigma}}{N}.\frac{1}{L_a} = k_1 \tag{4.9}$$

$$A_1 = \frac{2k_1}{s_1 - s_2}\,; \qquad A_2 = -A_1 = \frac{-2k_1}{s_1 - s_2} \tag{4.10}$$

The arm current flows through the inserted submodule capacitances. The capacitor voltage expression for the i^{th} submodule can be derived from the arm current expression.

$$v_{us}^{i}(t) = \frac{1}{C_s}\int_0^t i_{us}\, dt + v_u^i(0) \tag{4.11}$$

$$v_{us}^{i}(t) = \frac{1}{2.C_s}\int_0^t A_1 e^{s_1 t} + A_2 e^{s_2 t}\, dt + v_u^i(0) \tag{4.12}$$

$$v_{us}^{i}(t) = \frac{1}{2.C_s}\left[\frac{A_1}{s_1}e^{s_1 t} + \frac{A_2}{s_2}e^{s_2 t}\right] - \frac{1}{2.C_s}\left[\frac{A_1}{s_1} + \frac{A_2}{s_2}\right] + v_u^i(0) \tag{4.13}$$

For critically damped condition, s_1 & s_2 are two equal negative values. When t is larger than s_1 & s_2 (steady state), then the first term in equation 4.13 becomes zero. A change in capacitor voltage (Δv_{u1}^{i}) due to the arm current is calculated below:

$$v_{us}^{i}(t) - v_u^i(0) = -\frac{1}{2.C_s}\left[\frac{A_1}{s_1} + \frac{A_2}{s_2}\right] \tag{4.14}$$

$$v_{us}^{i}(t) - v_u^i(0) = -\frac{1}{2.C_s}.\frac{k_1}{s_1 - s_2}.\left[\frac{1}{s_1} - \frac{1}{s_2}\right] = \frac{k_1}{2C_s}.\frac{1}{s_1 s_2} = \frac{k_1}{4C_s}.L_a C_{load} \tag{4.15}$$

$$\Delta v_{us}^{i} = v_{us}^{i}(t) - v_u^i(0) = \frac{v_{cu,l}^{\Sigma}}{2NC_s}\, C_{load} \tag{4.16}$$

From equation 4.16, it can be concluded that the capacitor voltage variation directly depends upon the DC link voltage and load capacitance and inversely depends upon a number of submodules and submodule capacitance. Every inserted submodule experiences this voltage variation when there is a level change in the converter output. The typical response of the system can tell that arm current or output current rise will be dictated by $R_a/2L_a$ and a drop of this current or rise of submodule capacitor voltage rise is dictated by $R_a C_{load}/2$.

4.1.3 Circulating current response

When the submodule capacitor voltage starts deviating from the average value, then the DC voltage source starts supplying the necessary energy to balance this variation. This balancing action is carried out without affecting the connected load. Equation 2.13 can be adapted by substituting circulating voltage as $v_c = N\int i_c dt\,/2C_s$. The circulating voltage expression is derived by considering there are a total of N submodules inserted from the upper and lower arms. Hence the voltage which drives the circulating current can be calculated by integrating circulating current divided by equivalent capacitance.

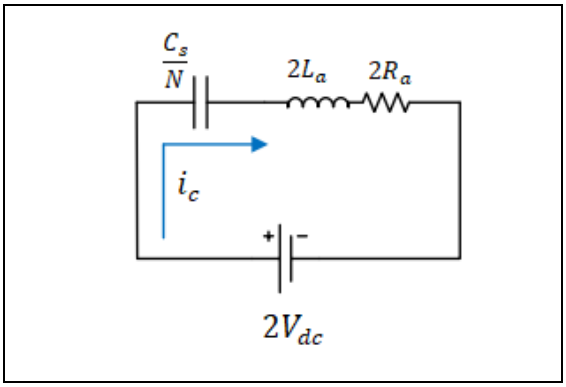


Figure 4-4: Equivalent circuit of circulating current

$$2V_{dc} - \frac{N.\frac{1}{C_s}\int i_c dt}{2} - R_a.i_c - L_a.\frac{di_c}{dt} = 0 \tag{4.17}$$

$$2L_a.\frac{d^2 i_c}{dt^2} + 2R_a.\frac{di_c}{dt} + \frac{N}{C_s} i_c = 0 \tag{4.18}$$

Equation 4.17 is differentiated to obtain a second order differential equation in terms of circulating current. The general solution of the system is a double exponential function as shown in equation 4.19.

$$i_c(t) = B_1 e^{r_1 t} + B_2 e^{r_2 t} \tag{4.19}$$

where r_1 & r_2 are two roots and can be mathematically represented as follows:

$$r_1 = -\frac{R_a}{2L_a} + \sqrt{\left(\frac{R_a}{2L_a}\right)^2 - \frac{N}{2C_s.L_a}} \;\&\; r_2 = -\frac{R_a}{2L_a} - \sqrt{\left(\frac{R_a}{2L_a}\right)^2 - \frac{N}{2C_s.L_a}}$$

Calculation of constants B_1 & B_2 is done based on initial conditions which are shown in equation 4.20. When all inserted submodule voltages are balanced, then the circulating current is zero, which is considered as initial condition. The initial voltage that the arm inductor hence experiences is the unbalance between DC link and total submodule capacitor voltage. The magnitude depends upon number of submodules inserted from the upper (N_u) and lower arm (N_l).

$$i_c(0) = 0 \;\&\; \frac{di_c}{dt}(0) = \frac{(N_u - N_l)\Delta v_{u1}^i}{L_a} = k_2 \tag{4.20}$$

$$B_1 = \frac{k_2}{r_1 - r_2} \;\&\; B_2 = -B_1 = \frac{-k_2}{r_1 - r_2} \tag{4.21}$$

4.1.4 Effect of circulating current on submodule capacitor

As mentioned in the introduction of 4.1.3, the circulating current tries to balance the difference in DC link voltage and submodule capacitor voltage. Each inserted submodule will experience a voltage variation to balance the difference and it is calculated using the following mathematical expressions.

$$v_{uc}^i(t) = \frac{1}{C_s}\int_0^t i_c\, dt + v_u^i(0) \tag{4.22}$$

$$v_{uc}^i(t) = \frac{1}{C_s}\int_0^t B_1 e^{r_1 t} + B_2 e^{r_2 t}\, dt + v_u^i(0) \tag{4.23}$$

$$v_{uc}^i(t) = \frac{1}{C_s}\left[\frac{B_1}{r_1} e^{r_1 t} + \frac{B_2}{r_2} e^{r_2 t}\right] - \frac{1}{C_s}\left[\frac{B_1}{r_1} + \frac{B_2}{r_2}\right] + v_u^i(0) \tag{4.24}$$

The steady state value of the i^{th} submodule capacitor voltage can be calculated by ignoring the first term in equation 4.24, as explained in the output current case.

$$v_{uc}^{i}(t) - v_{u}^{i}(0) = -\frac{1}{C_s}\left[\frac{B_1}{r_1} + \frac{B_2}{r_2}\right] \tag{4.26}$$

$$v_{uc}^{i}(t) - v_{u}^{i}(0) = -\frac{1}{C_s}.\frac{k_2}{r_1 - r_2}.\left[\frac{1}{r_1} - \frac{1}{r_2}\right] = \frac{k_2}{C_s}.\frac{1}{r_1 r_2} = \frac{k_2}{C_s}.\frac{1}{\frac{N}{2C_s.L_a}} \tag{4.27}$$

$$\Delta v_{uc}^{i} = v_{uc}^{i}(t) - v_{u}^{i}(0) = \frac{2(N_u - N_l)\Delta v_{u1}^{i}}{N} = \frac{2(N_u - N_l)v_{cu,l}^{\Sigma}}{4N^2 C_s} C_{load} \tag{4.28}$$

The main difference between the general solution shown in 4.4 and 4.19 is the capacitance value. The load capacitance is present in the output current analysis whereas equivalent submodule capacitance is present in the circulating current analysis. The submodule capacitance is always larger than the load capacitance hence the circulating current response will be always slower compared to the output current response. If the circulating current response is slower than the fundamental sampling frequency for the given number of submodules, then the circulating current cannot charge the disbalanced voltage introduced due to arm current or output current. Hence the time constant for the rise/fall in capacitor voltage is dictated by $2C_sR_a/N$. If this time constant is less, incomplete charging or discharging of submodule capacitor voltage will drift the capacitor voltage more away from average value of the submodule capacitor voltage.

4.1.5 Summary of the mathematical modeling

The above mathematical analysis is done for the positive level change in the output voltage with positive magnitude. The converter behavior to this change is summarized in a flow chart as shown in figure 4-5. The magnitudes of lower arm current and voltage deviations are expressed in terms of upper arm current and voltage deviations (Δv_{us}^{i} & Δv_{uc}^{i}).

To generate positive voltage magnitude, lower arm submodules are inserted and hence the number of submodules inserted from the lower arm will be higher than those from the upper arm, resulting in a circulating voltage less than the DC link voltage. Hence it generates positive circulating current which aims to balance the voltage deviation introduced due to voltage variation $(N_u - N_l)\Delta v_{us}^{i}$. The higher the difference $(N_u - N_l)$, the larger is the magnitude of the circulating current. It should be noted that the circulating current will not entirely balance the capacitor voltages of the lower arm to an average value unless $N_u = 0$. When $N_u - N_l = 2$ which is the minimum value, it will not be able to restore the capacitor voltage to an average value. But it will diverge the submodule capacitor voltage from average value after each cycle. When all submodules are used i.e. when $max(N_u - N_l)$ is N, then the divergence from the average will be very small. Similar analysis can be extended for other three cases of the converter operation. Case 2 represents the negative level change for positive voltage magnitude, case 3 is negative level change for negative voltage magnitude and case 4 is positive level change for negative voltage magnitude. The flowchart for these cases can be found in appendix B.

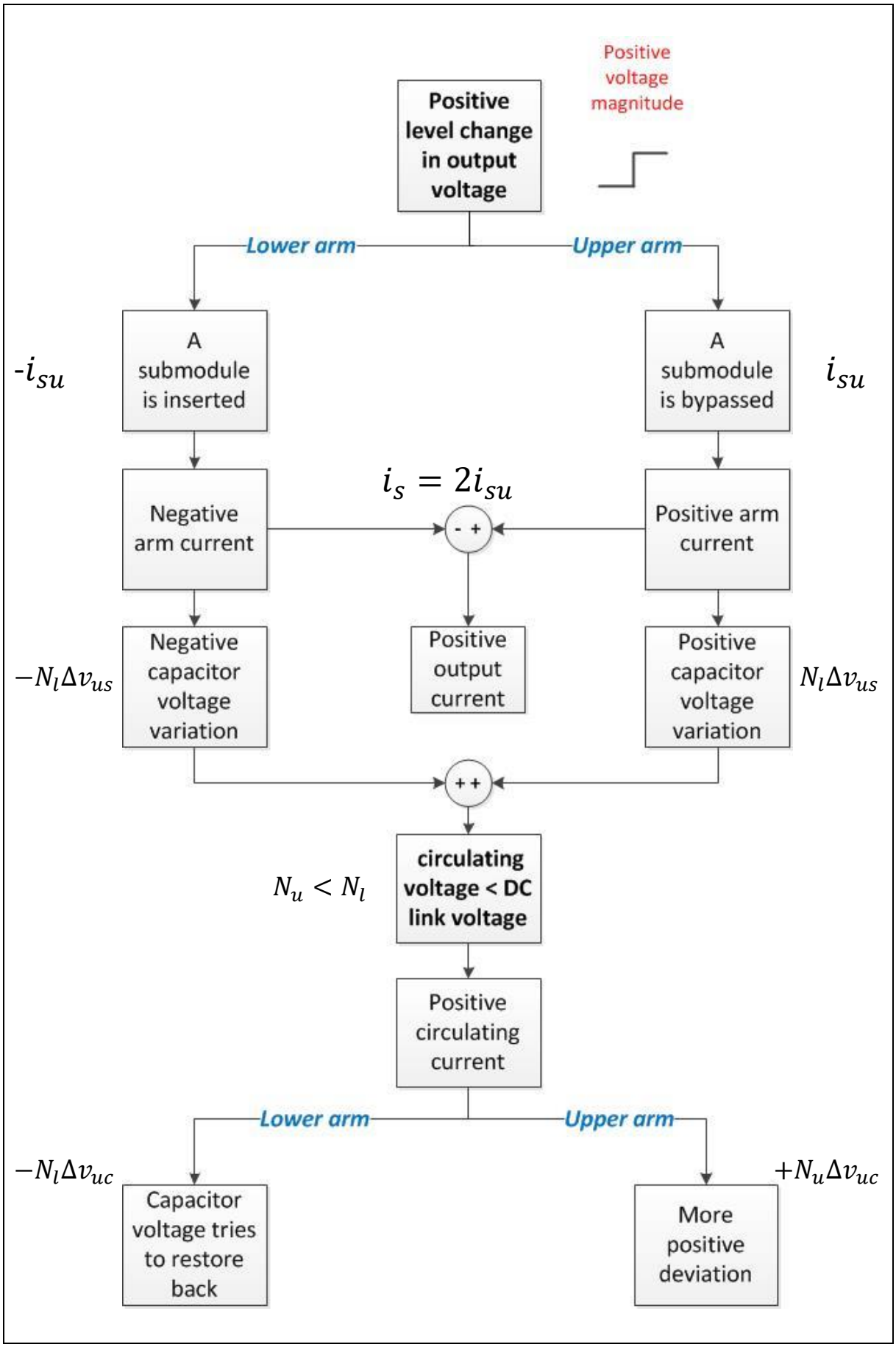


Figure 4-5: Sequence of operation for case 1 (Positive level change for positive magnitude)

4.2 Converter parameter design

Based on the mathematical analysis, the submodule capacitor and arm resistance value can be chosen. Arm inductance is designed based on current rise limitation put by switching devices in the converter.

4.2.1 Arm inductance

As discussed in chapter 2, the arm inductance can be obtained from equation 2.2 ($L_a = V_{dc}/\alpha$). α is chosen as 20 kA/s, keeping the reference of MMC in the Electrical Sustainable Lab, TU Delft [18]. Therefore, L_a will be 20 mH for $V_{dc} = 400\ V$. At higher voltage level, the switches are available with α as high as 2 kA/μs at 4.5 kV blocking voltage capability.

4.2.2 Submodule capacitance

The mathematical analysis predicts the capacitor voltage ripple which helps to design the submodule capacitance value. Modulation index is assumed to be maximum as worst-case scenario. Because when all submodule is inserted, one submodule will be inserted for the longest time and experience larger capacitor voltage ripple. That maximum ripple calculation will be addition of variation introduced due to output current and circulating current. Effect of circulating current will become significant as the amplitude of the output signal increased. Also, if the switching frequency of the stair case signal is higher than the time constant of the circulating current response, then the effect of circulating current should be neglected. Since variable frequency signals are generated from the converter, worst case scenario of slowest signal of 0.1 Hz frequency signal is considered and hence the circulating current effect must be considered.

When the bipolar signal is generated, upper arm generates negative polarity and lower arm generates positive polarity. During positive polarity of the signal, upper arm experiences voltage variation (Δv^i_{uT1}) due to effect of circulating current (Δv^i_{ucT1}) and output current (Δv^i_{usT1}) both. During negative polarity, circulating current tries to restore the upper arm inserted submodule to average value. Hence the submodule capacitor voltage (Δv^i_{uT2}) experiences capacitor voltage variation ($-\Delta v^i_{usT1}$) only because of output current with an opposite sign. It is because of opposite direction of output current. Before writing mathematical equations, figure 4-6 describes the terminologies used for ripple calculations.

$$\Delta v^i_{uT1} = \Delta v^i_{usT1} + \Delta v^i_{ucT1}$$

$$\Delta v^i_{uT1} = round\left(\frac{N+1}{2}\right).\Delta v^i_{us} + [2 + 4 + .. + N].\frac{2\Delta v^i_{uc}}{N} \tag{4.30}$$

$$\Delta v^i_{uT2} = -\Delta v^i_{usT1} = -round\left(\frac{N+1}{2}\right).\Delta v^i_{us} \tag{4.31}$$

$$\Delta v^i_{uT} = \Delta v^i_{usT1} + \Delta v^i_{uT2} \tag{4.32}$$

$$\Delta v^i_{uT} = 2.round\left(\frac{N+1}{2}\right).\Delta v^i_{u1} + (N+2)\frac{\Delta v^i_{u1}}{2}$$

$$\Delta v_{uT}^{i} = \left[2.round\left(\frac{N+1}{2}\right) + \frac{N+2}{2}\right].\frac{v_{cu,l}^{\Sigma}}{2NC_s}\ C_{load} \tag{4.33}$$

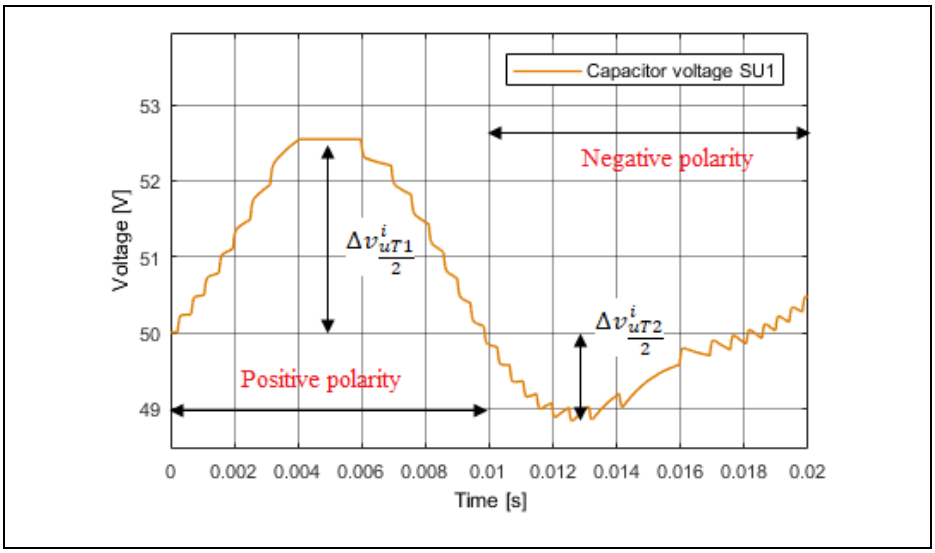


Figure 4-6 Submodule capacitor voltage ripple calculation

To keep the total voltage variation within 10% for $N = 16\ and\ v_{cu,l}^{\Sigma} = 2V_{Dc} = 800\ V$, the submodule capacitance value is calculated from equation 4.32 with $C_{load} = 50\ nF$ as worst-case scenario.

$$C_s = 5.25\ uF$$

4.2.3 Arm resistance

With the given value of arm inductance and submodule capacitance, the arm resistance value should be chosen in such a way that we obtain oscillation free output voltage waveform. The arm resistance value will be calculated from equation 4.4 and it is as follows

$$R_a = 1788.8\ \Omega$$

4.3 Simulation results with the designed parameters

The designed converter parameters are implemented in Simulink and simulation results are discussed in this section. Output current response and circulating current response are same for all waveforms and their analysis is shown together at once. Capacitor voltage variations and loss calculations are studied differently for 50 Hz sinusoidal and switching impulse.

4.3.1 Output current response

The pulsed shape output current with a level change in the output voltage is shown in figure 4-7. As discussed, rise in the output current is dictated by ratio of arm resistance and arm inductance ($2L_a/R_a = 25\ \mu s$). The fall in the pulse shaped output current is dictated by the arm resistance and load capacitance value ($R_a C_{load} = 80\ \mu s$). The output voltage level change occurs at the same slope of output current falling. The peak of the output current depends upon DC voltage source, number of submodules and arm resistance. Figure 4-7 shows how opposite

magnitude upper arm current and lower arm current forms the output current. The output current pulses are shown for 50 Hz sinusoidal signal is shown in figure 4-7 (c).

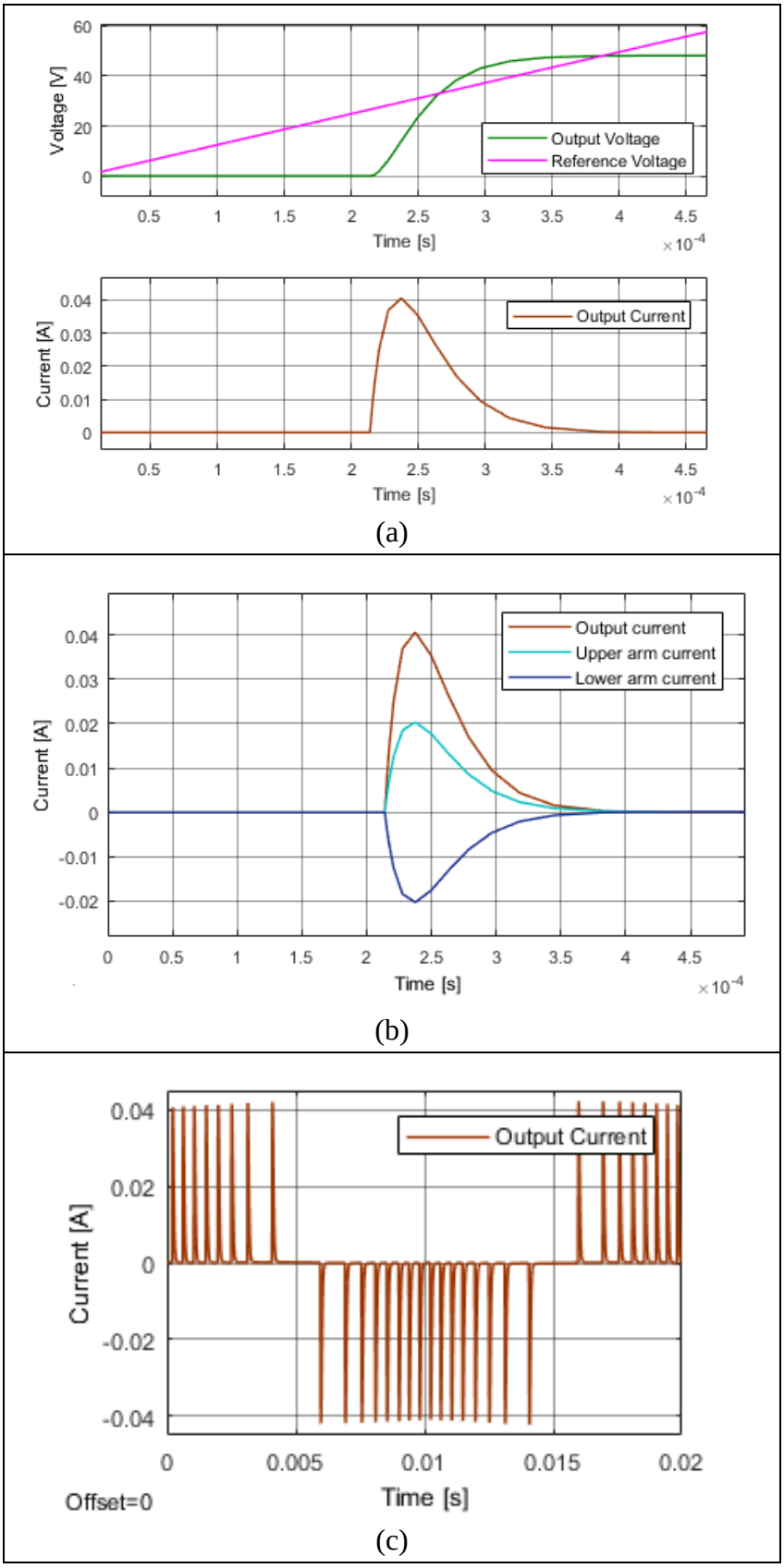


Figure 4-7: (a) Output Voltage (b) Output current and arm current (c) Output current pulses for a cycle of 50 Hz sinusoidal

4.3.2 Circulating current response

The slow response of the circulating current is evident in figure 4-8. The circulating current does not go to zero before the next level change in the output voltage. It is because of higher submodule capacitance value compared to the load capacitance. The magnitude of circulating current is increasing around the peak of sinusoidal waveform. Since the difference in the number of submodules inserted from the upper and lower arm increases, larger circulating current is required to compensate the voltage variation near the peak of sinusoidal signal.

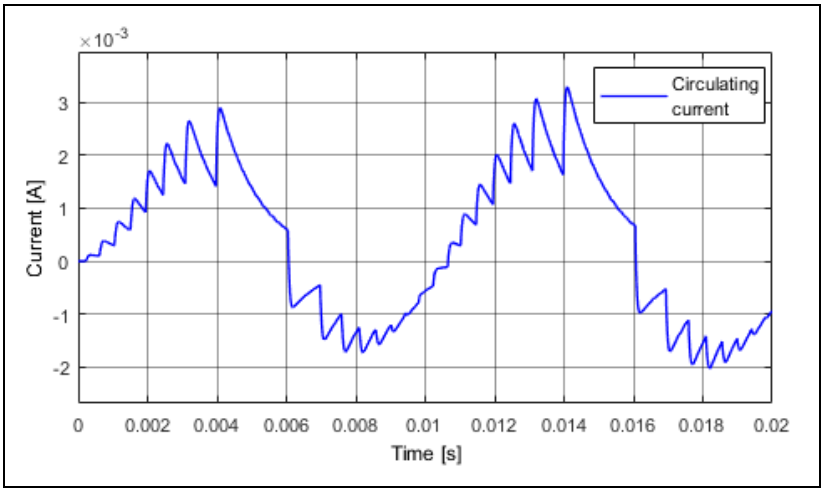


Figure 4-8: Circulating current for a cycle of 50 Hz sinusoidal

4.3.3 Submodule capacitor voltage variation

The capacitor voltage of one submodule from each arm is shown in figure 4-9. It can be observed that the magnitude of capacitor voltage ripple is within the allowed value (5 V). Also, the behavior of capacitor voltages in SU1 and SL1 is complementary. During the positive polarity of sinusoidal signal, the output current and circulating current adds together to increase the capacitor voltage of upper arm. In the lower arm submodule, the effect of two types of current is opposite keeping the voltage variation small. The role of upper arm and lower arm submodules are reversed when the polarity is changed.

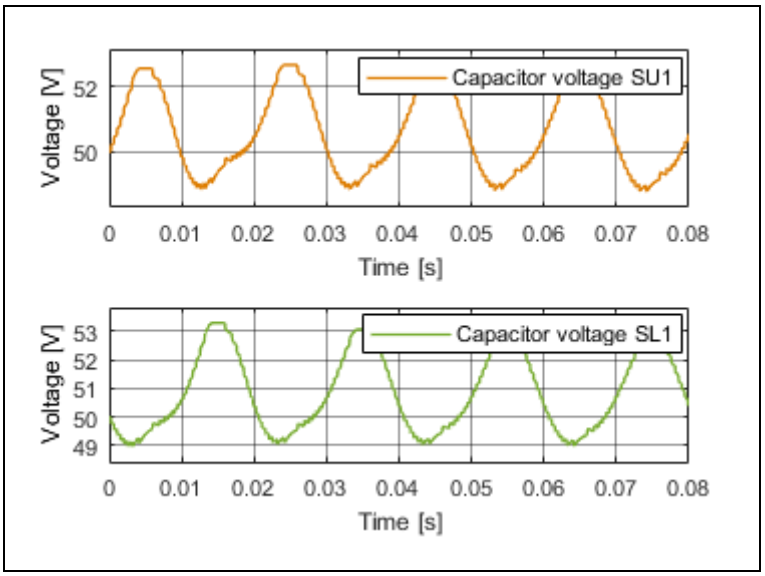


Figure 4-9: Submodule capacitor voltage for 50 Hz sinusoidal

For the switching impulse, the capacitor voltage variation is shown in figure 4-10. The graph shows that the capacitor voltage comes back to the value which is nearer to the average value. Since the impulse must be generated repeatedly, it is important to consider the magnitude of the capacitor voltage before generating the impulse for many times. It must be included in the starting algorithm of the test source.

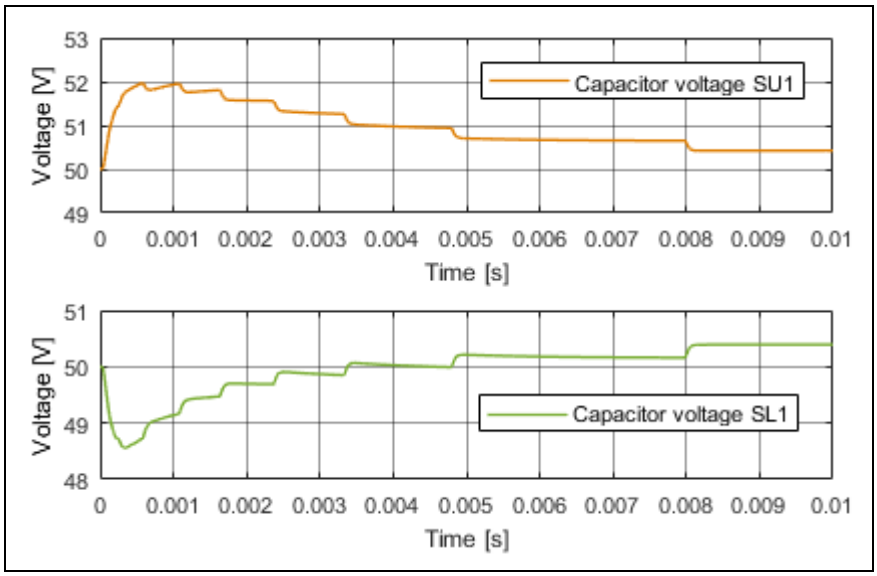


Figure 4-10: Submodule capacitor voltage for switching impulse

4.3.4 Losses calculations

With this high resistance value in the circuit, losses can become very high. Hence the instantaneous power dissipated in the resistor is calculated from the simulated waveform and it is shown in figure 4-11. It is seen that the instantaneous power dissipated is less than 1W. From the power dissipation curve, the energy lost can be calculated by integrating the waveform with respect to time. The energy lost in the resistance for one 50 Hz sinusoidal cycle comes out to be 0.0011 J. If this test signal is generated for 24 hours, the energy dissipation increases up to 95 J. For switching impulse, the energy dissipation is calculated in the range of mJ. The energy dissipation is not large; hence the resistor will not require special design for 400 V prototype.

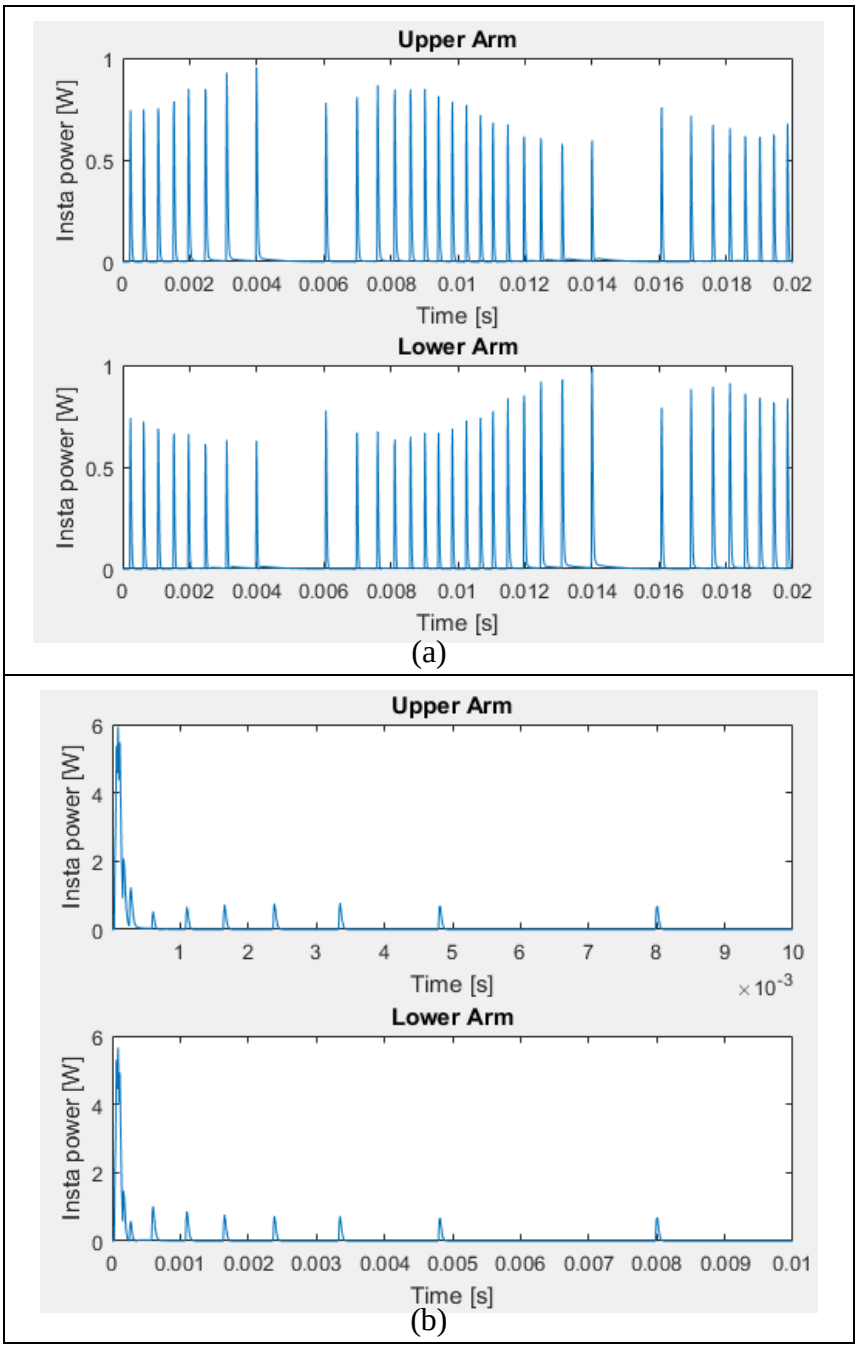


Figure 4-11: Power dissipated in the arm resistor (a) 50 Hz sinusoidal signal (b) Switching impulse

4.4 Semiconductor device rating

A half-bridge submodule has two complementary switches. The limited di/dt requirement on these switches is discussed above for arm inductance design. But, the current rating and blocking voltage capability are not discussed and hence they are addressed here.

The mathematical model derived in the previous section can give maximum current that will flow through these switches. To get the maximum current values from equations 4.5 and 4.10, first they should be differentiated with respect to time, and equated to zero to obtain a time instant at which maximum current is flowing. The derived time instants (t_{omax} and t_{cmax}) are substituted in the output current and circulating current expressions, as shown in equation 4.33.

$$t_{omax} = \frac{1}{s_2 - s_1} \ln\left(-\frac{A_1 s_1}{A_2 s_2}\right) \qquad t_{cmax} = \frac{1}{r_2 - r_1} \ln\left(-\frac{B_1 s_1}{B_2 s_2}\right) \tag{4.34}$$

$$I_{smax} = A_1 e^{s_1 t_{omax}} + A_2 e^{s_2 t_{omax}} \qquad I_{cmax} = B_1 e^{r_1 t_{cmax}} + B_2 e^{r_2 t_{cmax}} \tag{4.35}$$

Constant, B_1 and B_2 must be calculated by substituting $N_u - N_l = N$ as the extreme case. From equation 4.33, the current rating can be calculated as shown in equation 4.34.

$$I_{rating} = \frac{I_{smax}}{2} + I_{cmax} \tag{4.36}$$

In power applications of MMC, the semiconductor devices need to block the submodule capacitance voltage which is made up of average voltage plus the ripple. Figure 4-12 shows one of the converter state with 1 submodule inserted from upper arm and 2 submodules inserted from lower. When the submodule is inserted, then the lower semiconductor devices (T2 and D2) must block the submodule capacitor voltage. Similarly, upper semiconductor devices (T1 and D1) must block the submodule capacitor voltage when the submodule is bypassed. For better realization of blocking voltage, figure 4-12 is added. These are the requirements on these devices for steady state operation. Their requirement during fault and other abnormal condition must be verified to make a final decision.

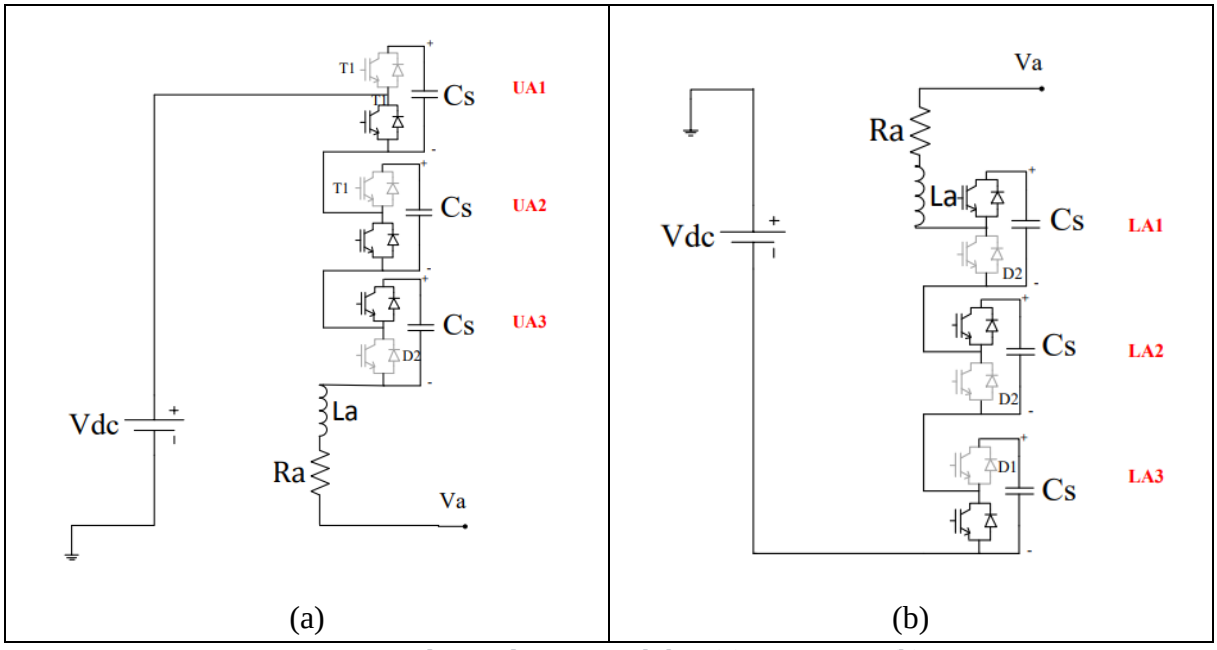


Figure 4-12: Semiconductor device capability (a) Upper arm (b) Lower arm

Table 4-1: Semiconductor device rating

	T1, D1, T2, D2	**Value**
Blocking voltage	$\frac{v_{cu}^{\Sigma}}{N} + \Delta v_{uT}^{i}$	55 V
Current rating	I_{rating}	0.03 A
$\frac{di}{dt}$ rate	20 kA/s	20 kA/s

The value of the current and blocking voltage rating are calculated for 400 V. With the low current magnitude, cooling requirement on the semiconductor devices reduce greatly.

4.5 Summary and extrapolation to higher voltage level

Since the output current is discontinuous and pulse shaped, the mathematical model analyzes each state of the converter separately. The mathematical analysis delivers an expression (***Equation 4.33***) which calculates the value of submodule capacitance to keep the capacitor voltage ripple within 10 %. Arm inductance value is calculated based on di/dt requirement imposed by semiconductor devices in the converter (***Equation 2.2***). Arm resistance is chosen to obtain critically damped system response (***Equation 4.5***). Current and voltage rating for the semiconductor devices are determined with the designed converter parameters.

The simulation results are shown for 400 V prototype. The extrapolation of the prototype design is explained here.

- At higher voltage levels, the number of submodules can be designed by the peak voltage to be produced and the IGBTs blocking capability. IGBTs are available for 1.2 kV, 3.3 kV, ***4.5 kV***, and 6.5 kV. Hence for 200 kV source, number of submodules can be chosen as 100, each submodule capacitance having average voltage of 4 kV.

- The submodule capacitance value is directly proportional to the number of submodules and test object capacitance. For a 200 kV test source with 100 submodules and 1µF load capacitance, the submodule capacitance will come around ***150 µF***.

- Arm inductance depends upon IGBT di/dt rating and they are available as high as ***2 kA/µs for 4.5 kV***. For a 200 kV test source, the arm inductance is in the ***100 µH*** range.

- Based on arm inductance and submodule capacitance, arm resistance can be calculated as ***26 Ω***. The value is on lower range because of the lower inductance value. This will increase the current peaks and hence increasing the losses significantly (peaks till MW).
    - *One solution*: Use overdamped system instead of critically damped
    - *Second solution*: Use higher value of arm inductance in mH than µH so that arm resistance for critically damped system is higher

5. FILTER DESIGN

For the small-scale prototype, it is important to remove the switching harmonics from the staircase output signal of the converter. Hence this chapter analyzes the frequency spectrum of the converter output signal and designs a suitable low pass filter to obtain a smooth output signal. This filter will act as a load for the converter and hence its effects on the converter operation are studied analytically and with simulations.

5.1 Frequency spectrum of output signal

The MMC based test source is designed to generate different periodic and non-periodic wave shapes using NLC control methodology. Out of all the wave shapes mentioned in the objective, square waveform and pulses do not require any filter since the staircase signal from the converter constructs them exactly with a maximum magnitude error of one submodule voltage (6.25 % with N=16). To implement a filter for the remaining signals, the frequency spectrums of these signals are analyzed to decide the cut-off frequency. These signals are generated from the 16-level converter with a modulation index of 0.9. For periodic signals, the frequency spectrum of the 50 Hz signal is analyzed out of all frequencies. Because the frequency spectrums of the periodic signal with different time periods (T=1/Fs) look the same, but with a different frequency range. It can be observed in figure 5-1 that the frequency range is between 0-10 Hz for the 0.1 Hz sinusoidal signal and the frequency range is between 0-100 kHz for the 1000 Hz sinusoidal signal. For two different frequency ranges, the frequency spectrum looks the same.

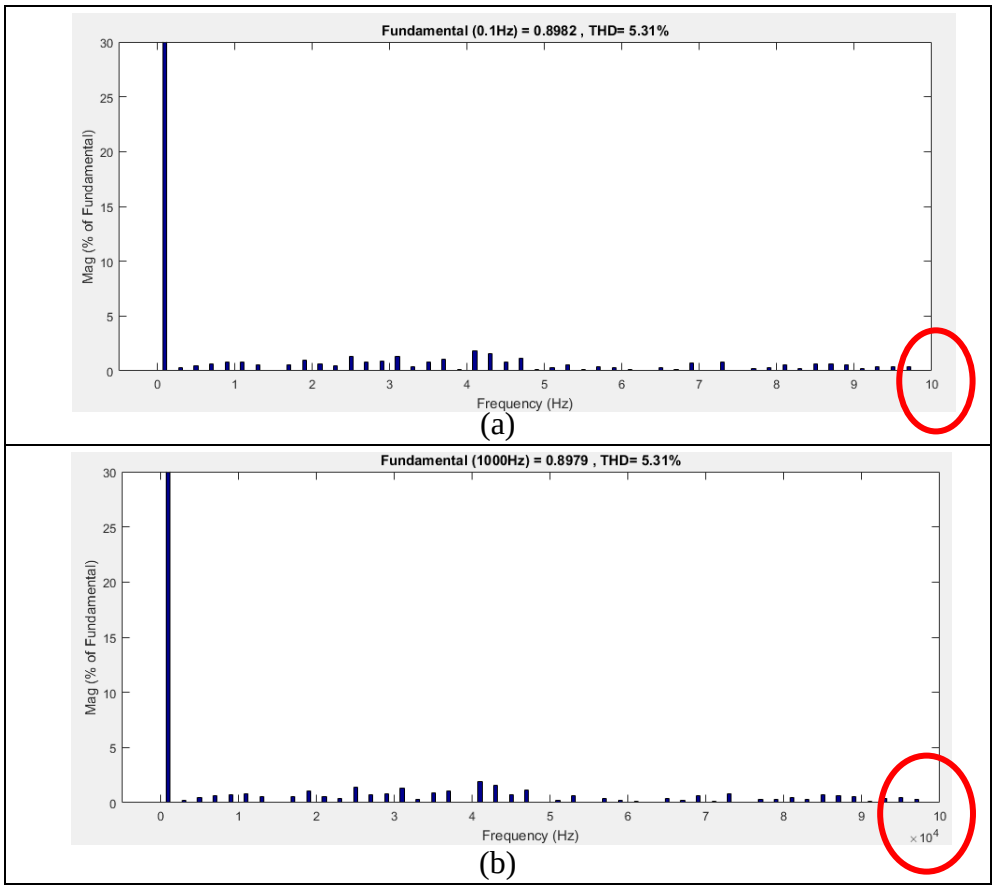


Figure 5-1: Frequency spectrum of converter output signal (a) 0.1 Hz Sinusoidal (b) 1000 Hz Sinusoidal

From this analysis, it can be concluded that it is sufficient to analyze one frequency out of the desired frequency range for all periodic signals. Henceforth, the converter output signal is shown along with the frequency spectrum of 50 Hz periodic signals.

5.1.1 Sinusoidal signal

The frequency spectrum of a pure sinusoidal has a spike at the fundamental frequency with other frequency components zero. But, sinusoidal with a staircase waveform will have harmonics present and they are shown in figure 5-2. Apart from the fundamental frequency, other frequencies must be filtered. Hence, the cut-off frequency for the filter is chosen as close as possible from the frequency spectrum i.e. 100 Hz for 50 Hz signal. The expression of the cut-off frequency can be generalized for any fundamental frequency (f_{req}) as $2f_{req}$.

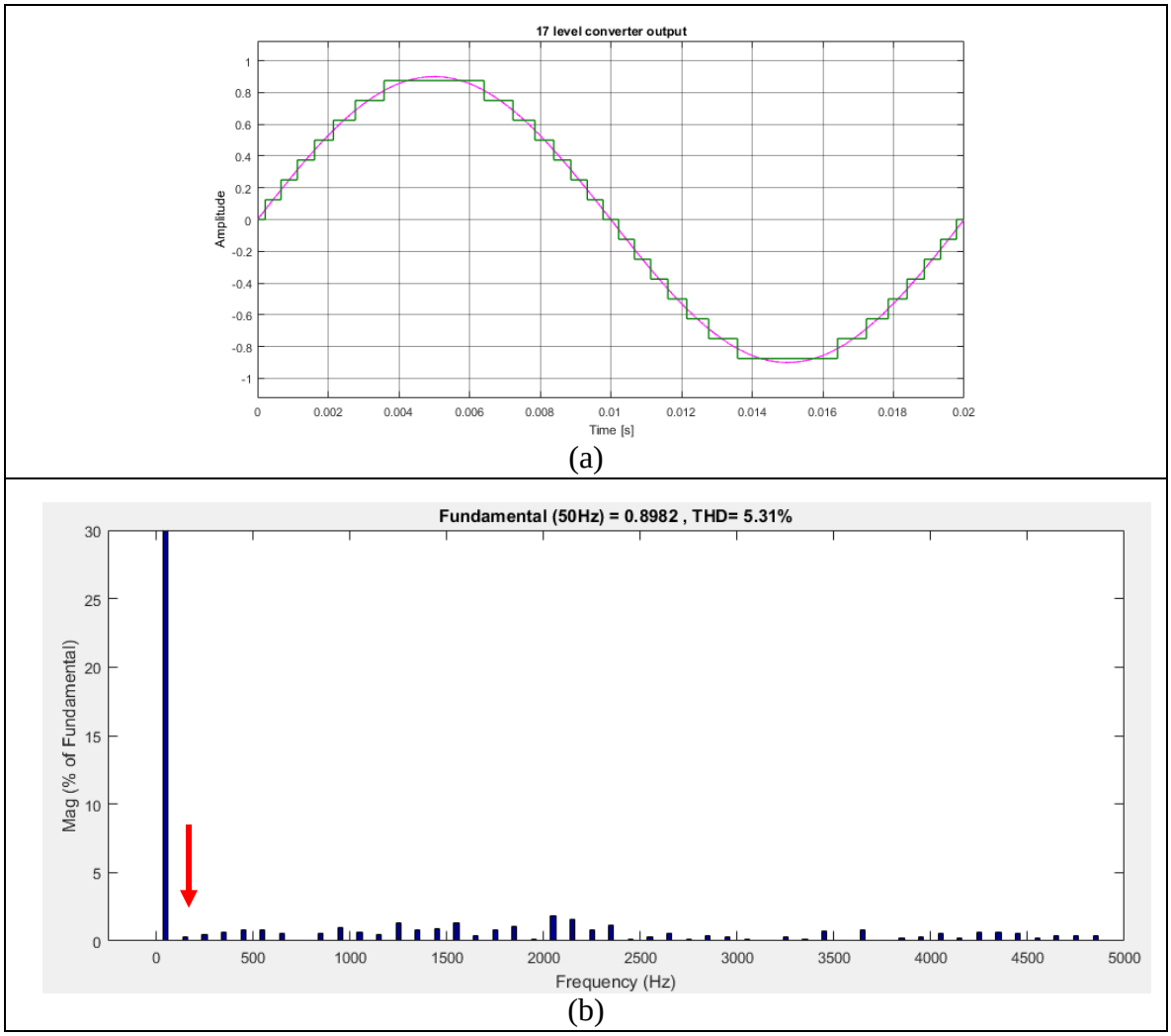
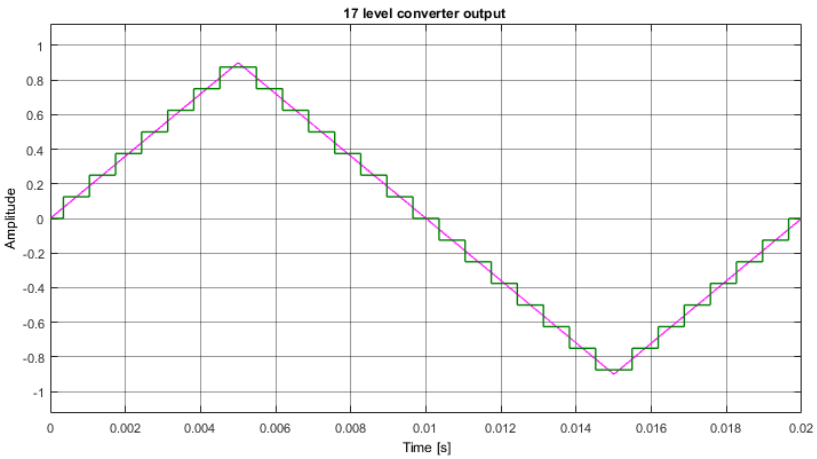


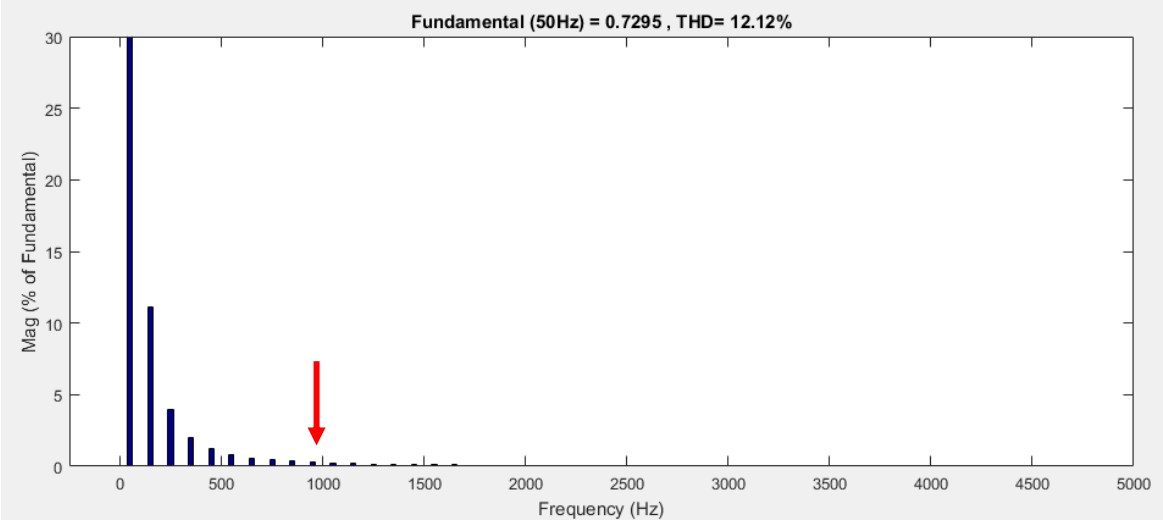
Figure 5-2: Sinusoidal (a) converter output signal (b) frequency spectrum of the converter output signal

5.1.2 Triangular signal with 50 % duty cycle

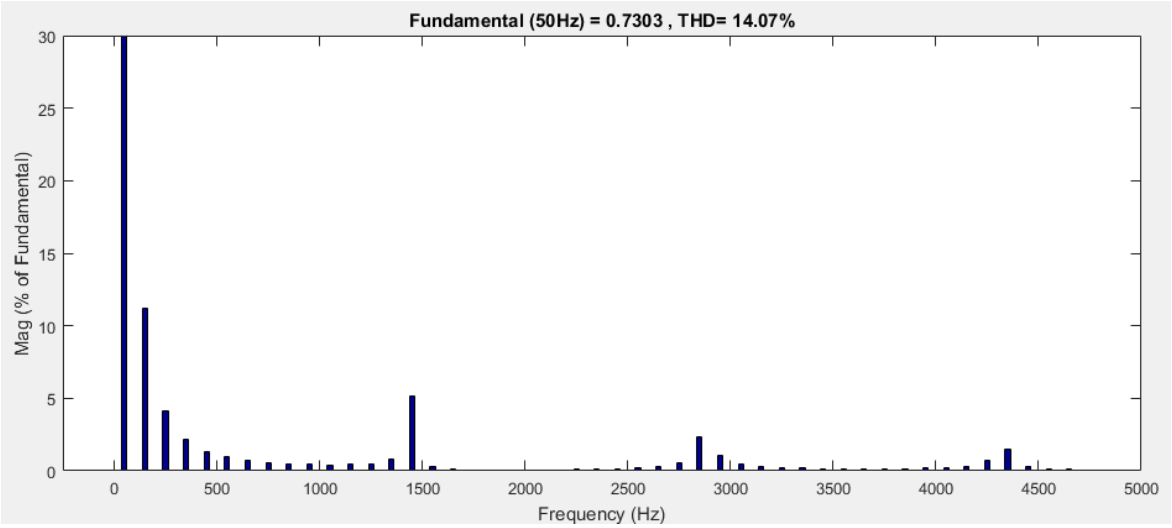
Figure 5-3 shows the frequency spectrum of a uniform triangular signal and converter output signal. It can be observed that the triangular signal contains different frequencies and their magnitudes are significant till 1000 Hz. The effect of the switching frequency in the converter output signal can be observed as spikes at 1400 Hz, 2800 Hz, etc. Hence the cut-off frequency for a uniform triangular signal can be chosen between 800-1000 Hz (16-$20f_{req}$).



(a)



(b)



(c)

Figure 5-3: Triangular signal with 50 % duty cycle (a) converter output signal (b) frequency spectrum of the reference signal (c) frequency spectrum of the converter output signal

5.1.3 Triangular signal with 10 % duty cycle

The frequency spectrum of the asymmetric triangular signal has a larger frequency spectrum, spread up to 1700 Hz. Hence the cut-off frequency should be increased to 1500-1700 Hz ($30f_{req}$ – $34f_{req}$) which is higher compared to the uniform triangular signal. Larger cut-off frequency might not filter the low switching harmonic present in the falling edge of the triangular signal. In the frequency transform, the magnitude of 1300 Hz -1600 Hz harmonics are higher compared to the original signal. Hence the filter design is problematic for signals with two different slopes.

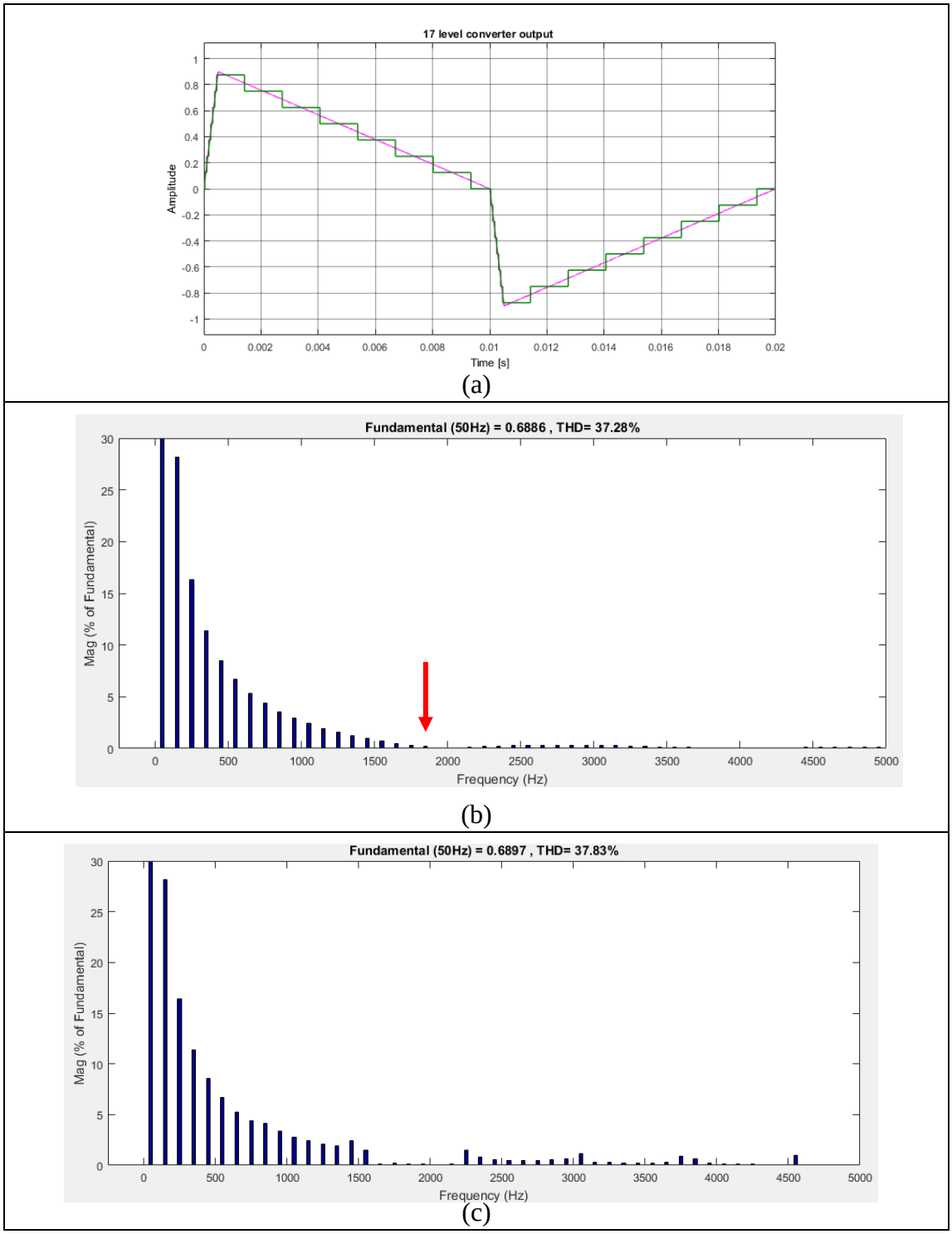


Figure 5-4: Triangular signal with 10 % duty cycle (a) converter output signal (b) frequency spectrum of the reference signal (c) frequency spectrum of the converter output signal

5.1.4 Trapezoidal signal with 0.001 s rise time

For the trapezoidal signal, the analysis is similar to the uniform triangular signal. The cut-off frequency can be chosen around 1000 Hz -1500 Hz ($20f_{req}$-30 f_{req}) which can be understood from figure 5-5.

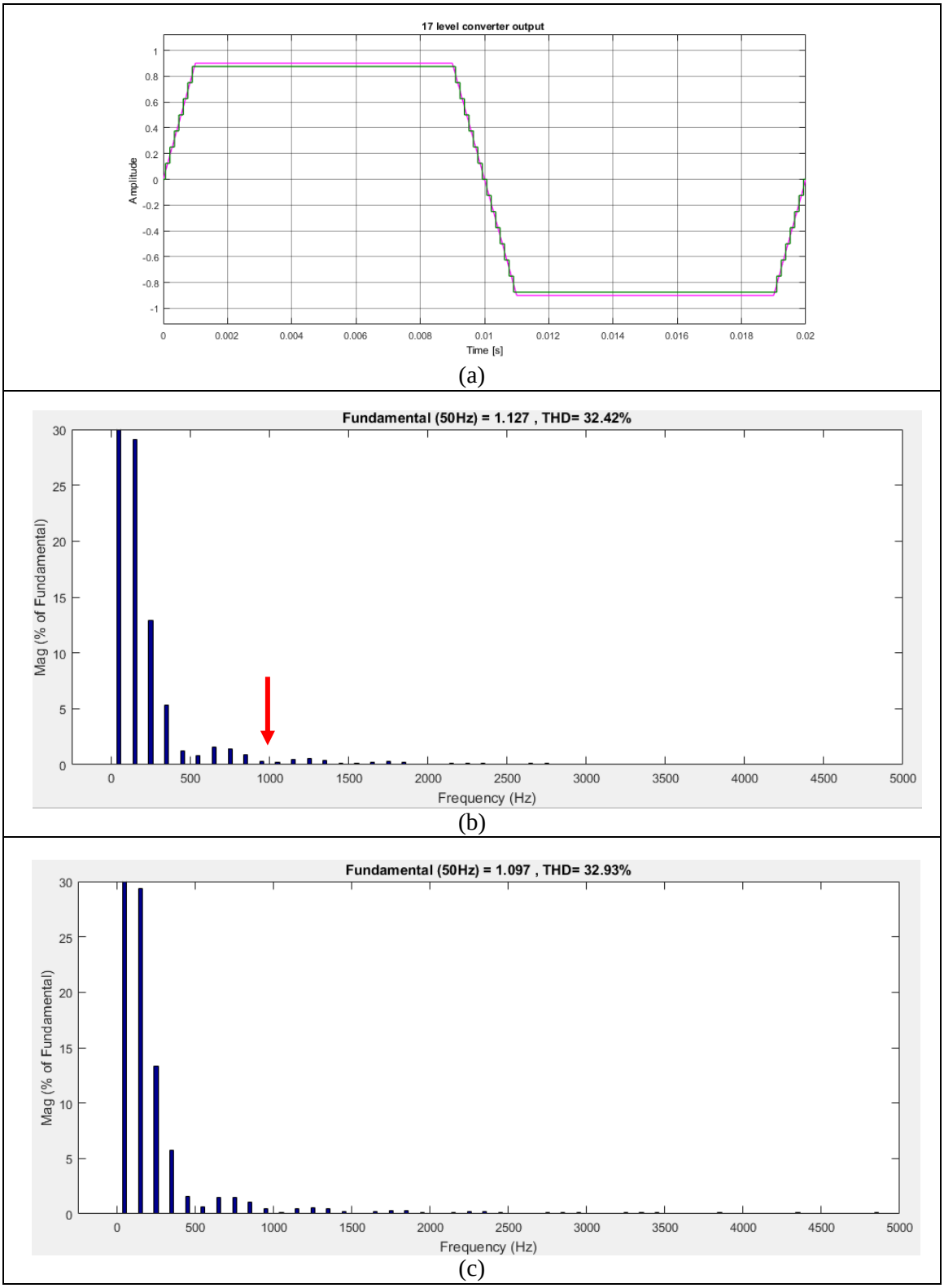


Figure 5-5 Trapezoidal signal with 0.001s rise time (a) converter output signal (b) frequency spectrum of the reference signal (c) frequency spectrum of the converter output signal

5.1.5 Switching impulse

For the switching impulse, the analysis is similar to the asymmetric triangular signal since it has two different slopes for rising and falling. But, the frequency spectrum of the switching impulse is wider than the asymmetric triangular signal. Hence the cut-off frequency should have a higher value such as 5000 Hz or more. Larger cut-off frequency will allow higher frequencies which are important for the initial voltage rise.

Switching impulse is a non-periodic signal and frequency spectrum of the signal is drawn assuming the signal is periodic after 0.01 s. Also, it should be noted that the magnitude of the frequency spectrum is shown with respect to the DC component of the signal in figure 5-6.

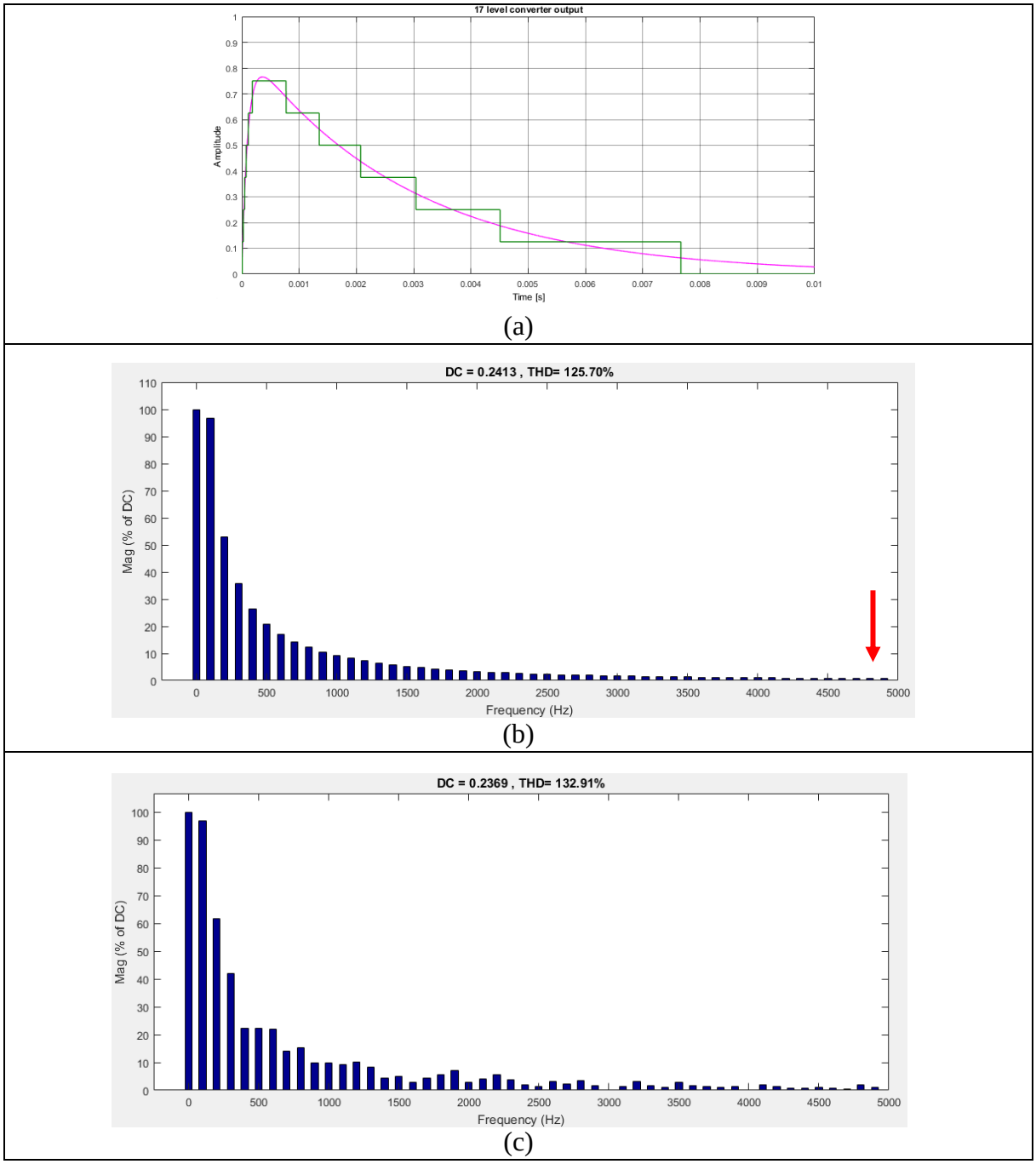


Figure 5-6: Switching impulse (a) converter output signal (b) frequency spectrum of the reference signal (c) frequency spectrum of the converter output signal

From this analysis, it can be concluded that the frequency spectrum analysis is very specific to the generated converter output signal. Hence any variation in the converter output signal (modulation index, duty ration, rise time, etc.), this analysis should be repeated, and filter parameters should be designed accordingly.

5.2 Filter topology and filter parameter design

Low pass filter design is very common with the increase in the use of power electronic converters getting installed in the field. Possible topologies of the low pass filter implemented for a DC-DC converter are shown in figure 5-7. Use of resistor in the filter is not a most efficient choice for power transfer application since the filter resistance is a lossy component. Hence the use of other components i.e. inductor and capacitor need to be explored. But these components can introduce resonance phenomenon in the system making it unstable. Hence figure 5-7 contains LC topologies with different damper circuits. Criteria for comparing their performance is time domain response, frequency domain response of the output signal, and power loss through the damper circuit. Frequency domain analysis is done by deriving a mathematical expression of the transfer function. Filter parameters are optimized depending upon the time domain response of the filter. The detailed mathematical analysis is conducted in [35].

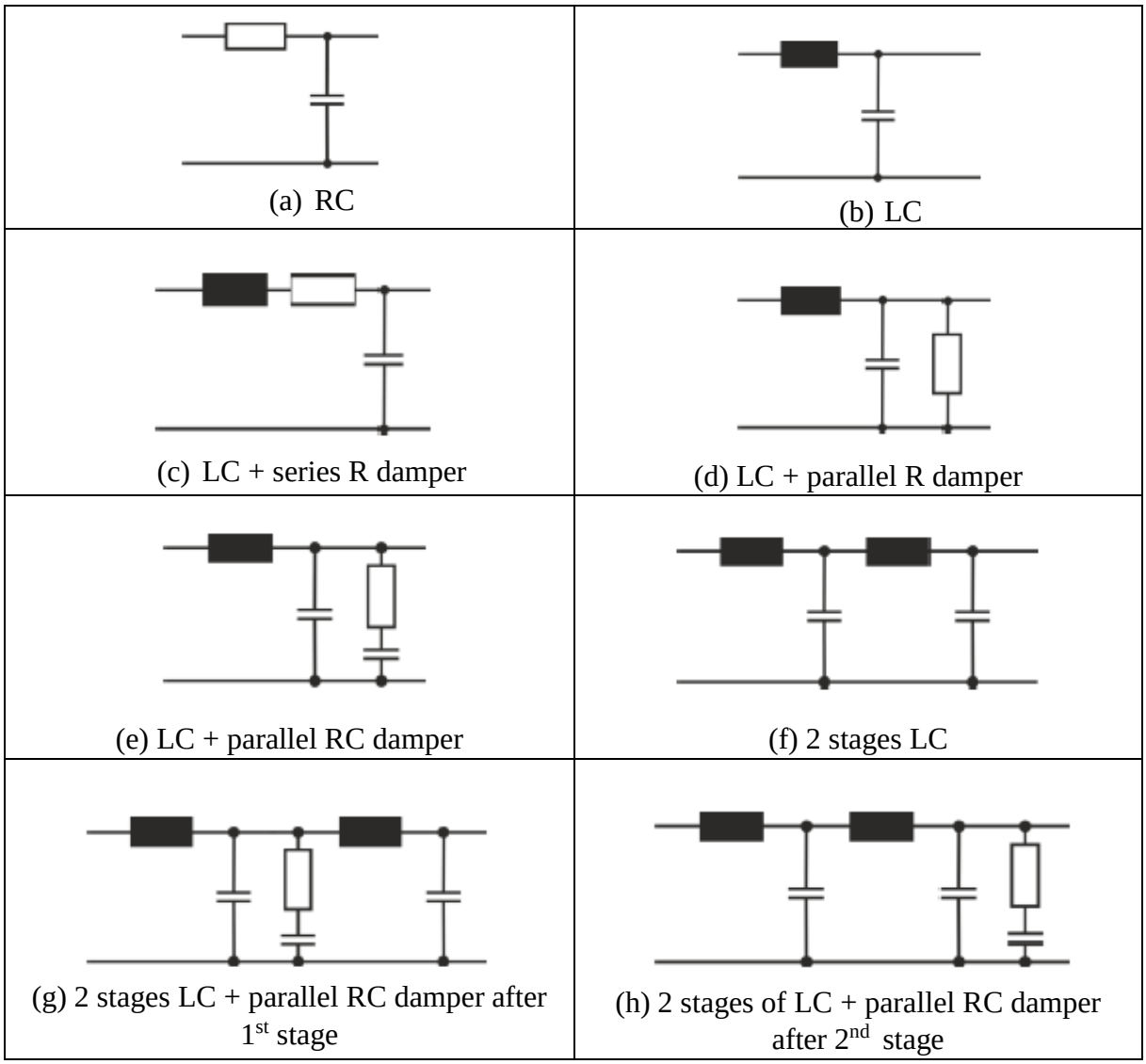
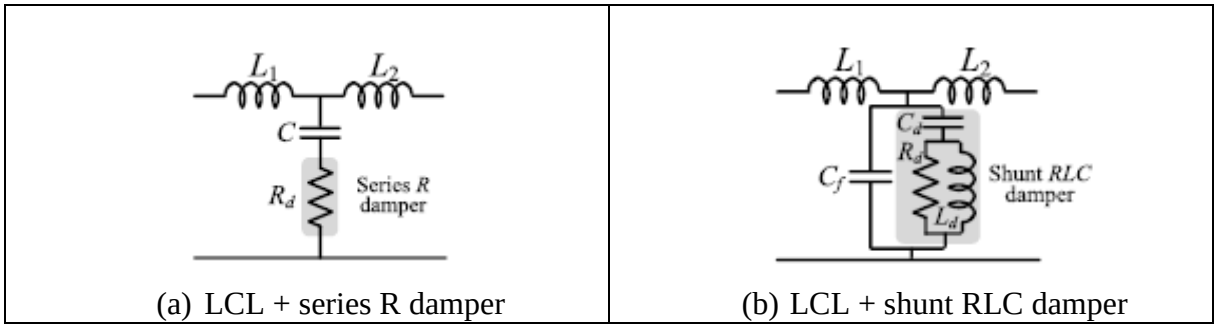


Figure 5-7: Low pass filter topologies for DC-DC converter

For 2-level converters, LCL filter implemented with a damper circuit [36] is a conventional choice. This topology is suitable for the inductive load and must be implemented carefully to avoid unnecessary resonance phenomenon which might affect the stability of the system.



(a) LCL + series R damper (b) LCL + shunt RLC damper

Figure 5-8: Low pass filter topologies for grid connected 2-level converter

For the MMC based HV test source, main objective is not to transfer power, but it is to apply arbitrary high voltage wave shapes across test objects. Hence the simplest topology of RC circuit (figure 5-7 (a)) is examined first.

5.2.1 Investigation of RC filter topology

Figure 5-9 shows the schematic of the RC filter with the converter output shown as a variable voltage source. Generally, the filter response is studied in frequency domain. Here, the time domain analysis is chosen since the quality of the filtered signal needs to be measured in terms of peaks and slope of the signal.

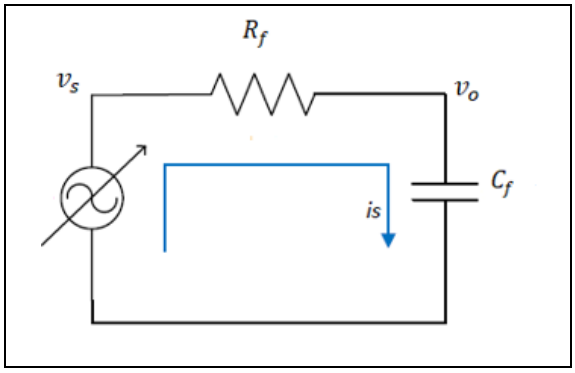


Figure 5-9: Schematic of RC filter

In time domain analysis, the filter response can be determined by convoluting the converter output signal (filter input) and transfer function of the filter. It is shown in the expression:

$$v_o = conv(v_s, h) \tag{5.1}$$

The transfer function of RC filter (h) is shown in equation 5.2

$$h = \frac{1}{R_f C_f} e^{\frac{-1}{R_f C_f} t} u(t) \tag{5.2}$$

The cut-off frequency of the RC filter is given by $f_c = \frac{1}{2\pi R_f C_f}$. For 50 Hz sinusoidal signal, a filter with $f_c = 100\ Hz$ is designed with $R_f = 1.6\ k\Omega$ and $C_f = 1\ uF$. Figure 5-10 shows the converter output signal, transfer function and the filter output signal

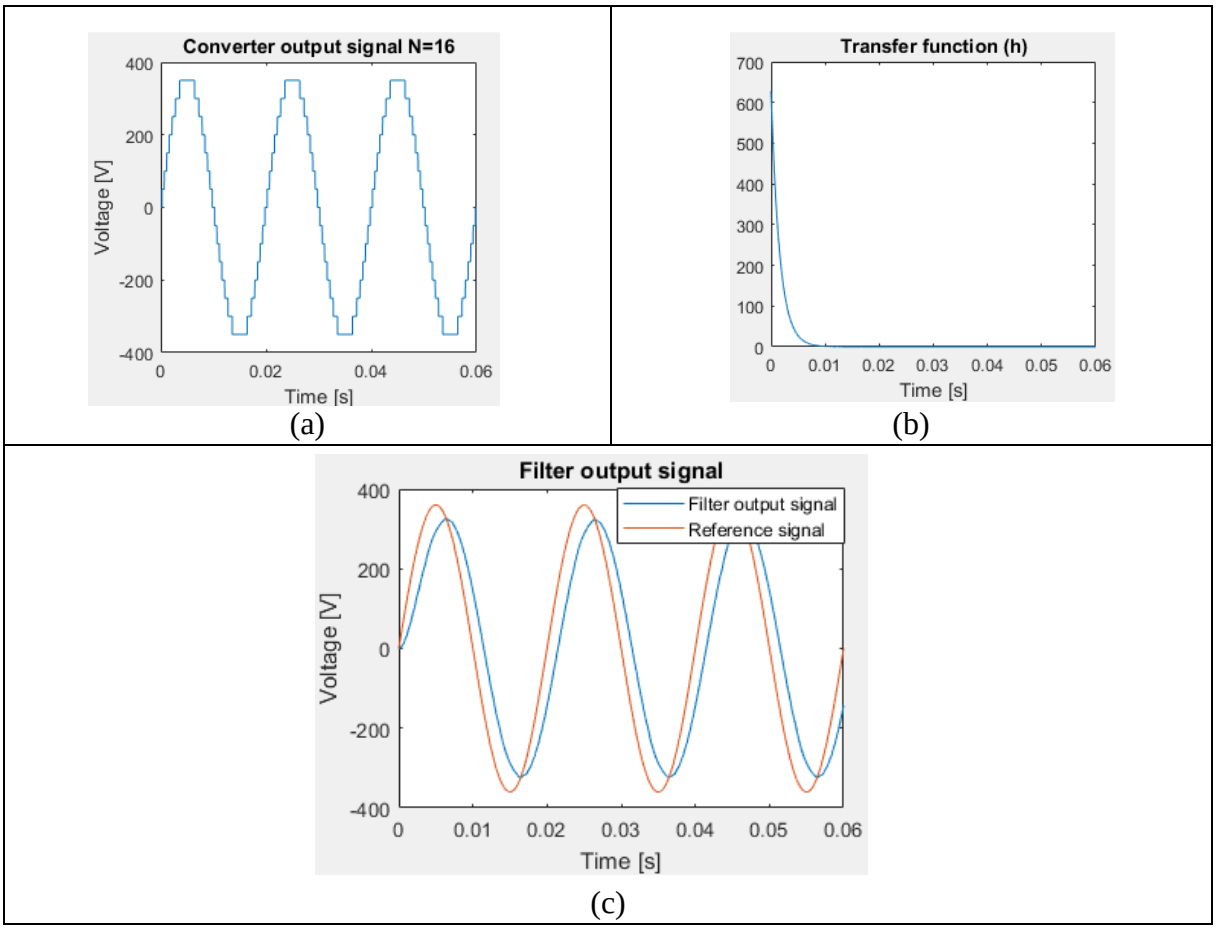
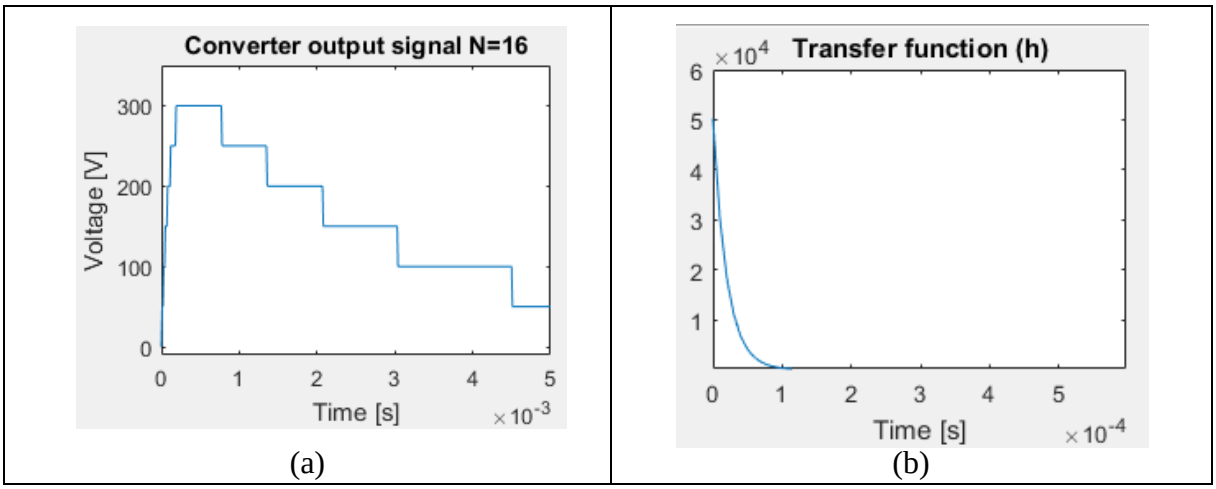
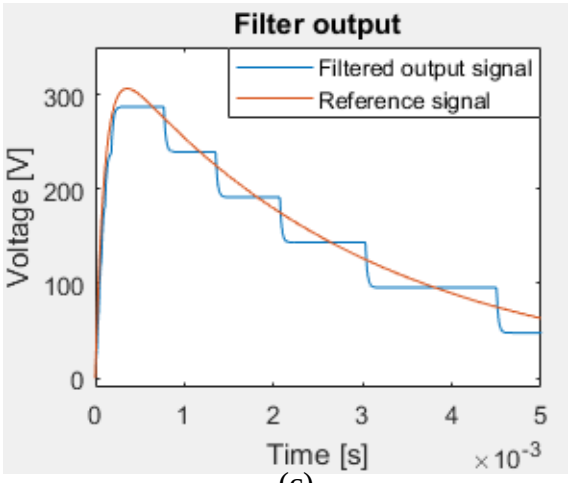


Figure 5-10: 50 Hz sinusoidal (a) Converter output signal with N=16 and m_{req}=0.9 (b) Transfer function (c) Filtered signal

For switching impulse, the cut-off frequency has higher magnitude, $f_c = 5000\ Hz$. The RC filter can be realized for the given cut-off frequency with $R_f = 20\ \Omega$ and $C_f = 1\ \mu F$. Figure 5-11 shows that the switching harmonics from the initial rise are removed, but the switching harmonics from the falling slope cannot be removed without affecting the initial rise. For high voltage testing, the initial slope plays the significant role in determining the dielectric strength of the insulation. Hence the lower switching harmonics in the falling slope are not considered a problem assuming the problem will be vanished with higher submodules for higher voltage level.





(c)

Figure 5-11: 50 Hz sinusoidal (a) Converter output signal with N=16 and m_{req}=0.9 (b) Transfer function (c) Filtered signal

From the above two implementations, it can be concluded that the RC filter can be used to obtain smooth output signals. The next challenge in the filter design is the realization of filter components for such a vast range of wave shapes. Since the filter is designed for various signals, extreme cases are analyzed.

Table 5-1: Cut-off frequency for extreme

	Cut-off frequency	C_f	R_f
0.1 Hz Sinusoidal ($2f_{req}$)	0.2 Hz	1 µF	796 kΩ
Switching impulse	5 kHz	0.1 µF	318 Ω
1000 Hz asymmetric triangular signal ($30f_{req} – 34f_{req}$)	30 kHz	0.1 µF	53 Ω

From the table 5-1, it can be deduced that the slow signal requires very high resistance value. This value can be reduced by increasing the cut-off frequency till 1 Hz for 0.1 Hz sinusoidal. Second challenge is how these components affect the converter operation.

5.3 Effect of filter on converter operation

From the mathematical model, it can be understood that the effect of filter will be seen only on the output current response and not on the circulating current. The series resistance R_{filter} will get added in the output current circuit, as shown in figure 5-12. Addition of an extra resistance in the circuit will reduce current's peak in the circuit and giving a faster output current response.

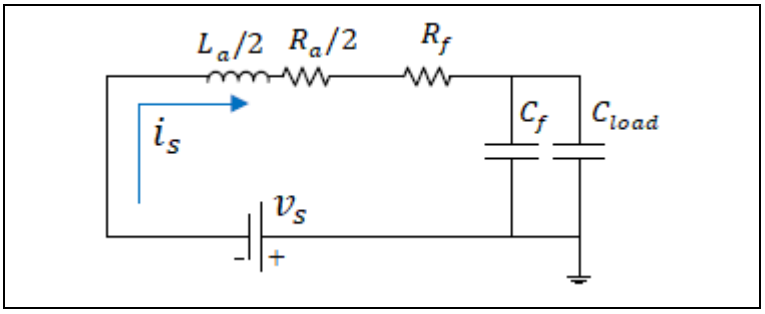


Figure 5-12: Output current response with filter implemented

Since the load conditions are changed, it is important to find optimal values of converter parameters for the given load conditions. Expression 4.33 determines the submodule capacitance value for the given load conditions. With the filter capacitance of 1 µF, the submodule capacitance value is recalculated to keep the voltage ripple within the bound. The value is calculated as follows:

$$5 = \left[2.round\left(\frac{16+1}{2}\right) + \frac{16+2}{2}\right] \times \frac{800}{2 \times 16 \times C_s} \times 1.5\ 10^{-6}$$

$$\Delta v_{uT}^{i} = 10\%\ of\ \frac{v_{cu,l}^{\Sigma}}{N} = 5\ V$$

$$C'_{load} = C_f + C_{load} = 1.05\ \mu F$$

$$C_s = 131.25\ \mu F$$

The arm resistance value will change, and it can be calculated as it is done in chapter 4.

$$R_a = 390\ \Omega$$

The arm resistance also plays a role in the filtering. The arm resistance gets added up in the filter resistance and changes the cut-off frequency. In case of 1000 Hz asymmetric triangular $R_a = 390$ will change the cut-off frequency from 30 kHz to lesser value as 5 kHz. In such a case, the lesser value of the filter capacitance should be chosen.

5.4 Filter output signal

5.4.1 50 Hz sinusoidal signal (R_f = 1.6 kΩ and C_{filter} = 1 µF)

Figure 5-13 shows the filter output result for 50 Hz sinusoidal signal. The quality of the filtered signal is verified with the THD value. While calculating this THD, the last two cycles of sinusoidal signal (0.02 s-0.06 s) is chosen. It is found that the THD value is reduced to 0.77 % (filtered signal) from 5.18 % (converter output signal). Since a resistance is added in series, a small drop in voltage magnitude is observed from 335 V to 310 V (7.5 %). The voltage drop is present because of the high filter resistance.

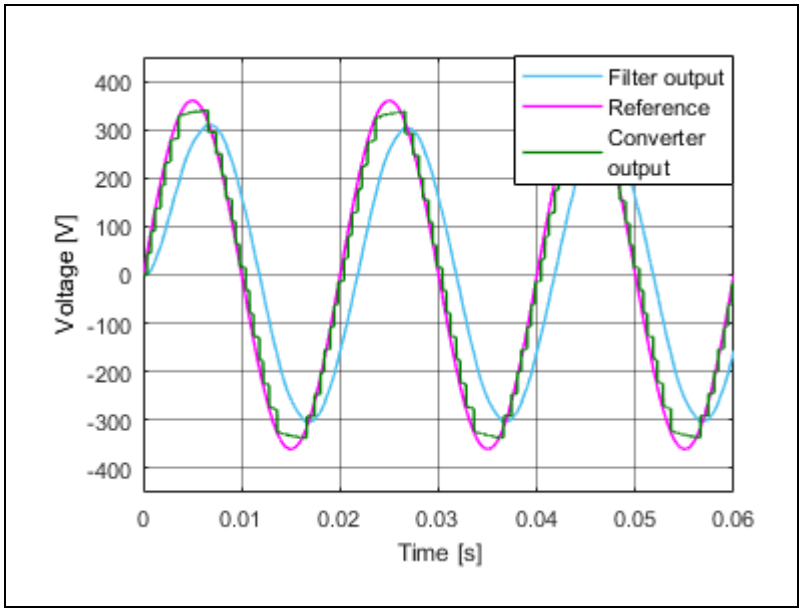


Figure 5-13: Filter output for 50 Hz sinusoidal

It is important to monitor the energy getting lost in the filter resistors. Hence the power absorbed by three resistors are shown in figure 5-14 and the energy lost values are as follows:

Energy loss through the upper arm resistance (400 Ω) = 0.03 J
Energy loss through the lower arm resistance (400 Ω) = 0.03 J
Energy loss through the upper arm resistance (1.6 kΩ) = 0.1 J

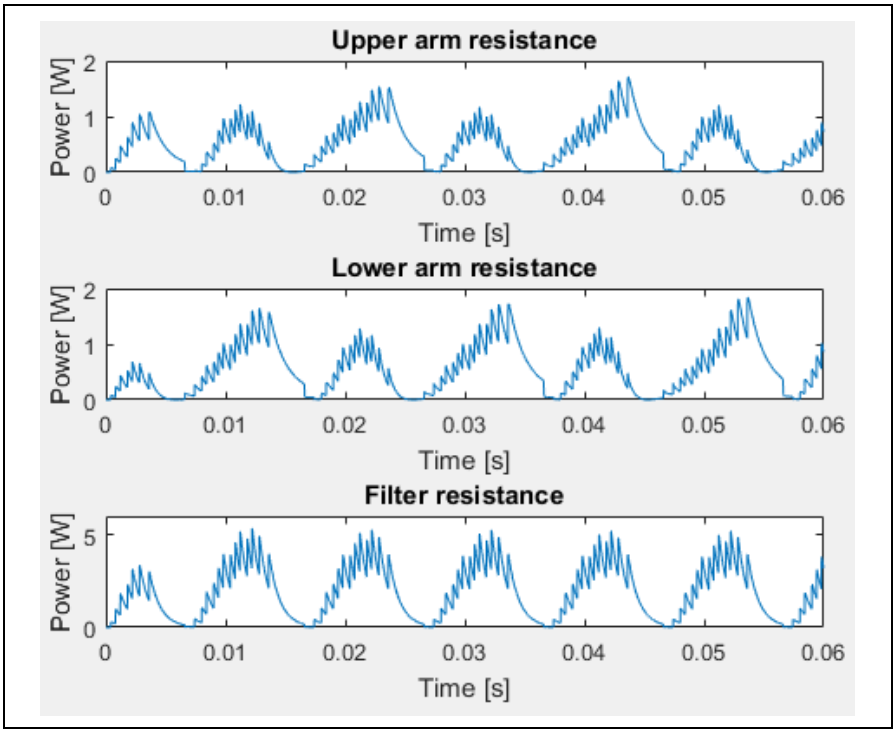


Figure 5-14: Power dissipation – 50 Hz sinusoidal signal

5.4.2 0.1 Hz triangular signal with 50 % duty cycle (R_f = 318 kΩ and C_f = 1 µF)

Figure 5-15 shows the filter output for symmetric triangular signal with 0.1 Hz frequency. The peak magnitude of reference signal is 360 V and that of filtered signal is 330 V. The percentage error in the voltage magnitude is 8.3 %. The reason behind this voltage drop is the filter resistance again. Though the higher value of the filter resistance reduces the peak output current, it introduces the error in the voltage magnitude thereby reducing the efficiency of the test source with respect to the peak voltage. The slope of reference signal is 144 V/s and the slope of the filtered signal is 140.3 V/s. The percentage error in the slope is 2.6 %.

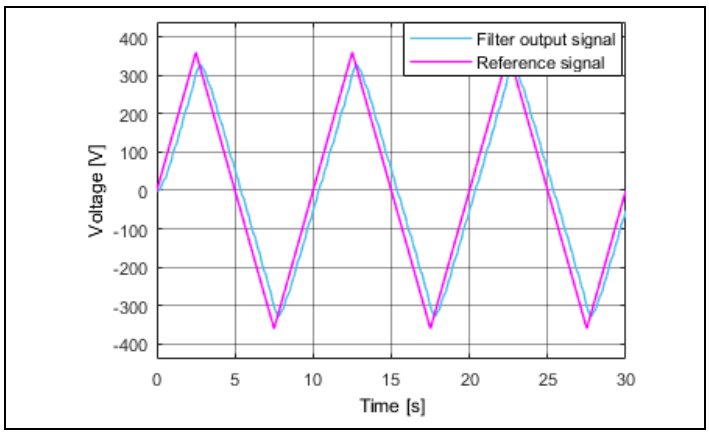


Figure 5-15: Filter output for 0.1 Hz symmetric triangular signal

The power dissipated in the converter to generate the given signal is shown in figure 5-16 and the energy lost for three cycles of the triangular signal is shown below. It should be observed that the larger value of filter resistance reduces energy consumption drastically.

Energy loss through the upper arm resistance (400 Ω) = 0.35 mJ
Energy loss through the lower arm resistance (400 Ω) = 0.28 mJ
Energy loss through the upper arm resistance (318 kΩ) = 0.25 mJ

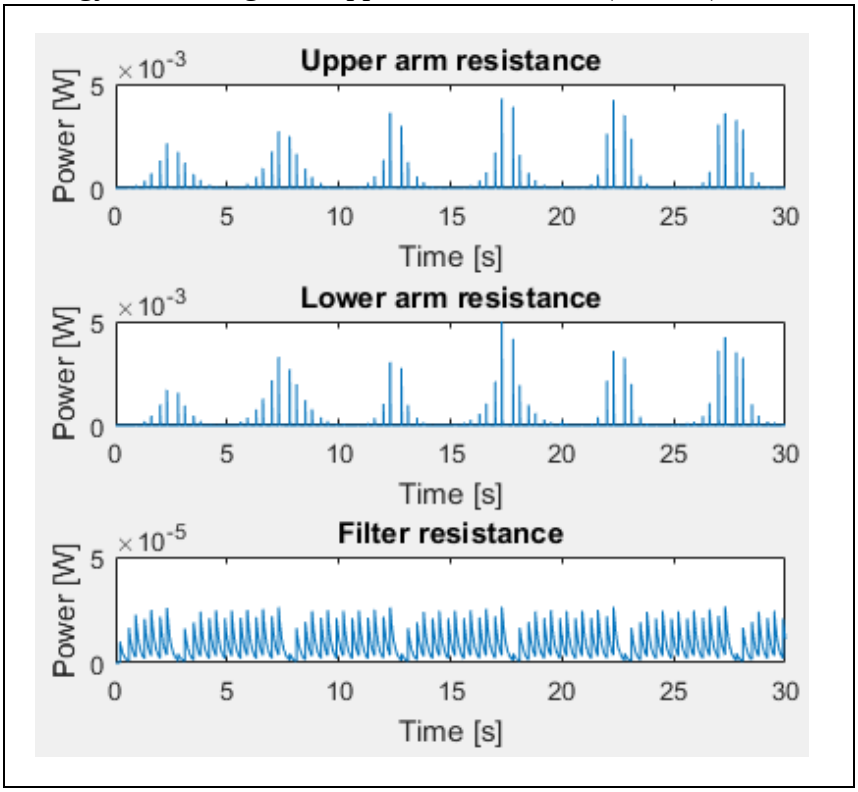


Figure 5-16: Power dissipation – 0.1 Hz symmetric triangular signal

5.4.3 1000 Hz triangular signal with 10 % duty cycle (R_f = 530 Ω and C_f = 10 nF)

This is one of the extreme cases for the filter implementation. The values calculated in table 5-1 has the filter resistance less than the arm resistance. Hence the value of filter capacitance is reduced to nF and the filter resistance is calculated for the reduced filter capacitance. The peak magnitude of the reference signal is 335 V and that of the filtered signal is 300 V. The percentage error in the voltage magnitude is 10.44 %. Apart from the filter resistance, one more reason for the voltage drop is that the load capacitance could not charge fully when the next submodule switching occurs. This drop is added leading to higher percentage error in the voltage magnitude.

The slope of the reference signal is 4.3 MV/s and the slope of the filtered signal is 3 MV/s. The percentage error in the slope is 30.23 %. In high voltage testing to generate a fast signal with the desired slope, it is common to use the reference slope higher than the desired one. Hence the obtained output voltage signal will not have high percentage error in the slope. Also, a significant delay in the output signal is seen. The reason behind this is the sampling frequency of the sorting algorithm implemented. The sample frequency used here is in kHz frequency range which is comparable to the fundamental frequency in this case.

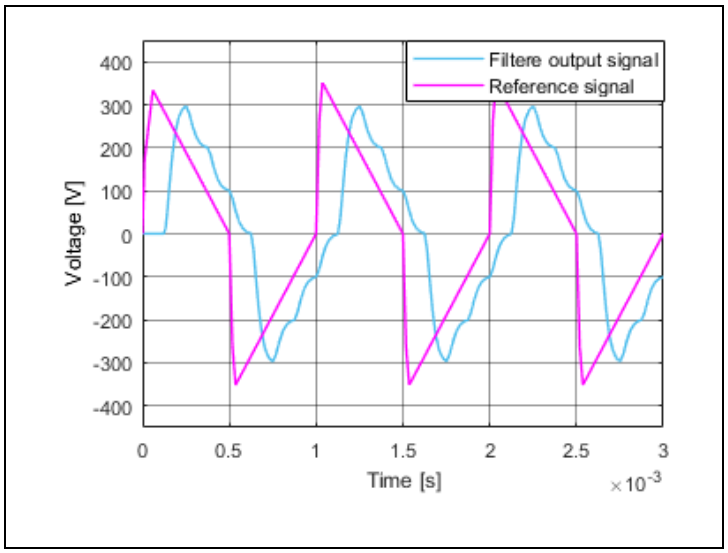


Figure 5-17: Filter output for 1000 Hz asymmetric triangular signal

The power dissipated in the converter to generate the given signal is shown in figure 5-18 and the energy lost for three cycles of the triangular signal is shown below:

Energy loss through the upper arm resistance (400 Ω) = 2.9 mJ
Energy loss through the lower arm resistance (400 Ω) = 2.9 mJ
Energy loss through the upper arm resistance (530 Ω) = 11.6 mJ

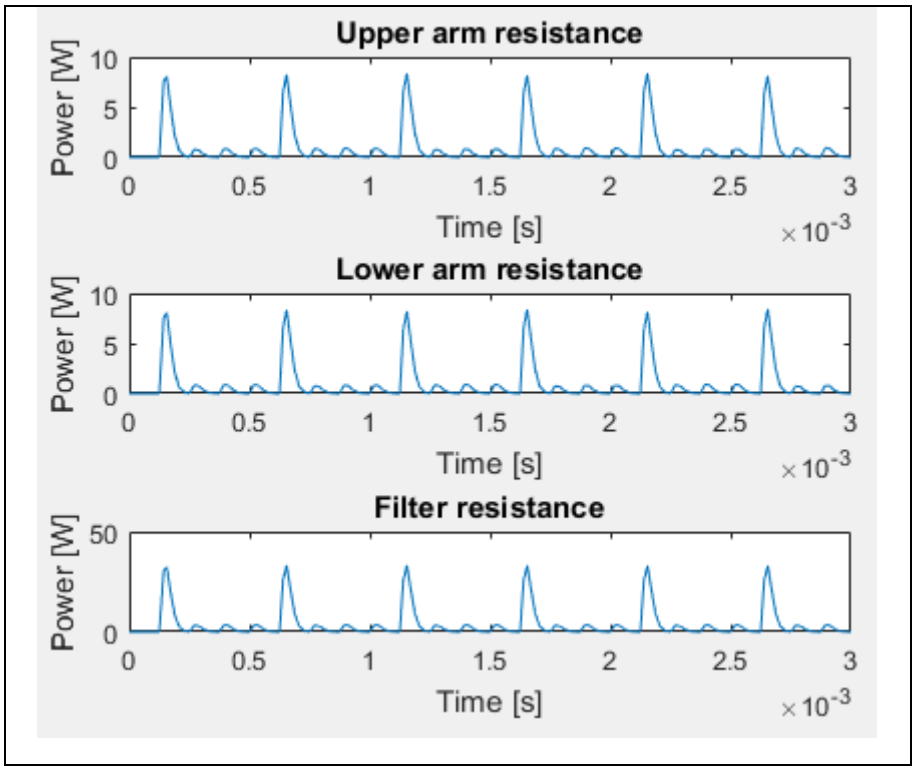


Figure 5-18: Power dissipation – 1000 Hz non-symmetric signal

5.4.4 Trapezoidal signal with 0.001s rise time – 50 Hz (R_f = 160 Ω and C_f = 1 µF)

In figure 5-19, the filtered output signal is shown with the reference signal. The magnitude of the reference signal is 360 V and that of the filtered signal is 345 V. The percentage error in the

voltage magnitude is 4.1028%. The slope of the reference signal is 0.36 MV/s and slope of the filtered signal is 0.24 MV/s. The percentage error in the slope is 31 %. The similar trick of the use of reference signal with a higher slope can be used here too.

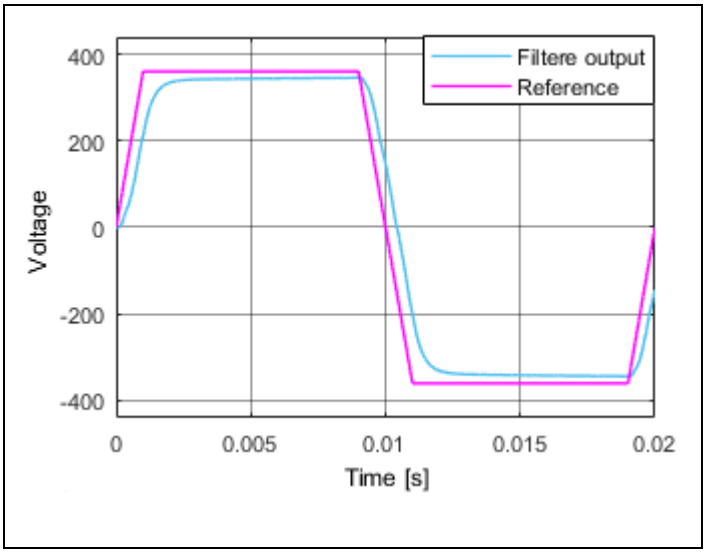


Figure 5-19: Filter output for 50 Hz trapezoidal signal

The power dissipation happening in the arm resistances and the filter resistance is shown in figure 5-20 and the energy lost for one cycle of the trapezoidal signal is shown below:

Energy loss through the upper arm resistance (400 Ω) = 0.0384 J
Energy loss through the lower arm resistance (400 Ω) = 0.0396 J
Energy loss through the upper arm resistance (160 Ω) = 0.1506 J

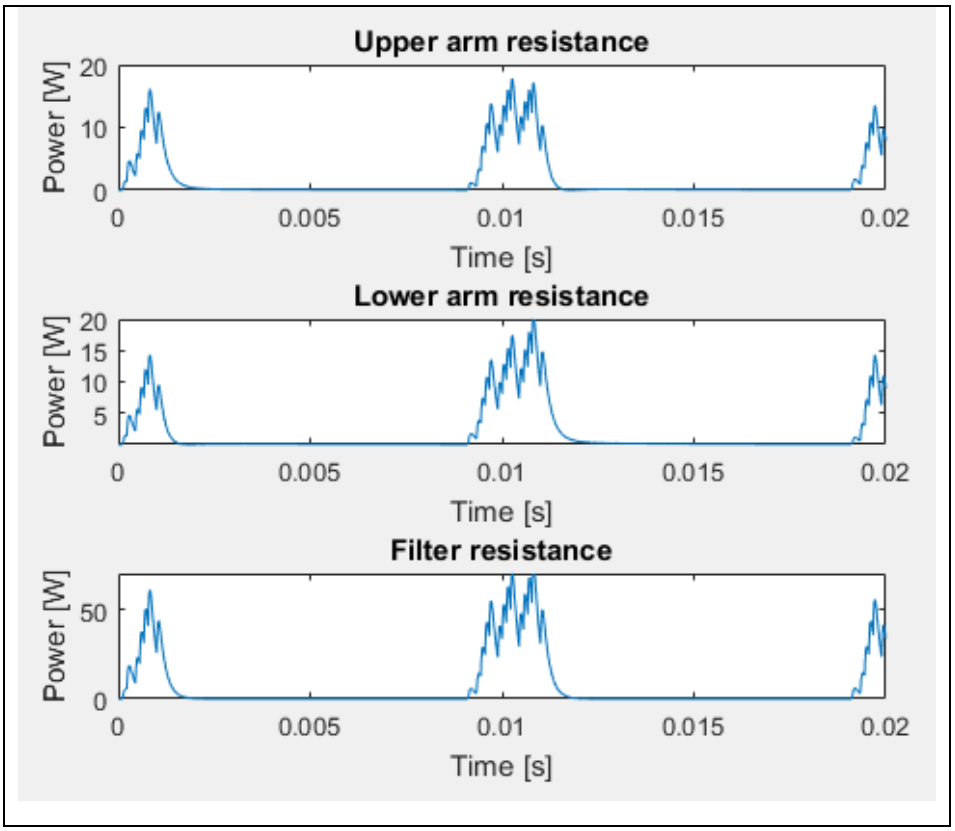


Figure 5-20: Power dissipation – 50 Hz trapezoidal signal

5.4.5 Switching impulse (R_{filter} = 200 Ω and C_{filter} = 0.1 µF)

Figure 5-21 shows the switching impulse generated from the converter and filter setup. IEC 60061 standardized the switching impulse with following tolerances. These parameters are calculated for the filtered output signal as per standard and it can be observed that the generated signal is well within the standard.

Table 5-2: Comparison between Standard and obtained switching impulse

	Tolerance for standard switching impulse	Obtained switching impulse
Voltage magnitude	3 %	2.58 %
Time to peak	20 %	12.28 %
Time to half value	60 %	26.53 %

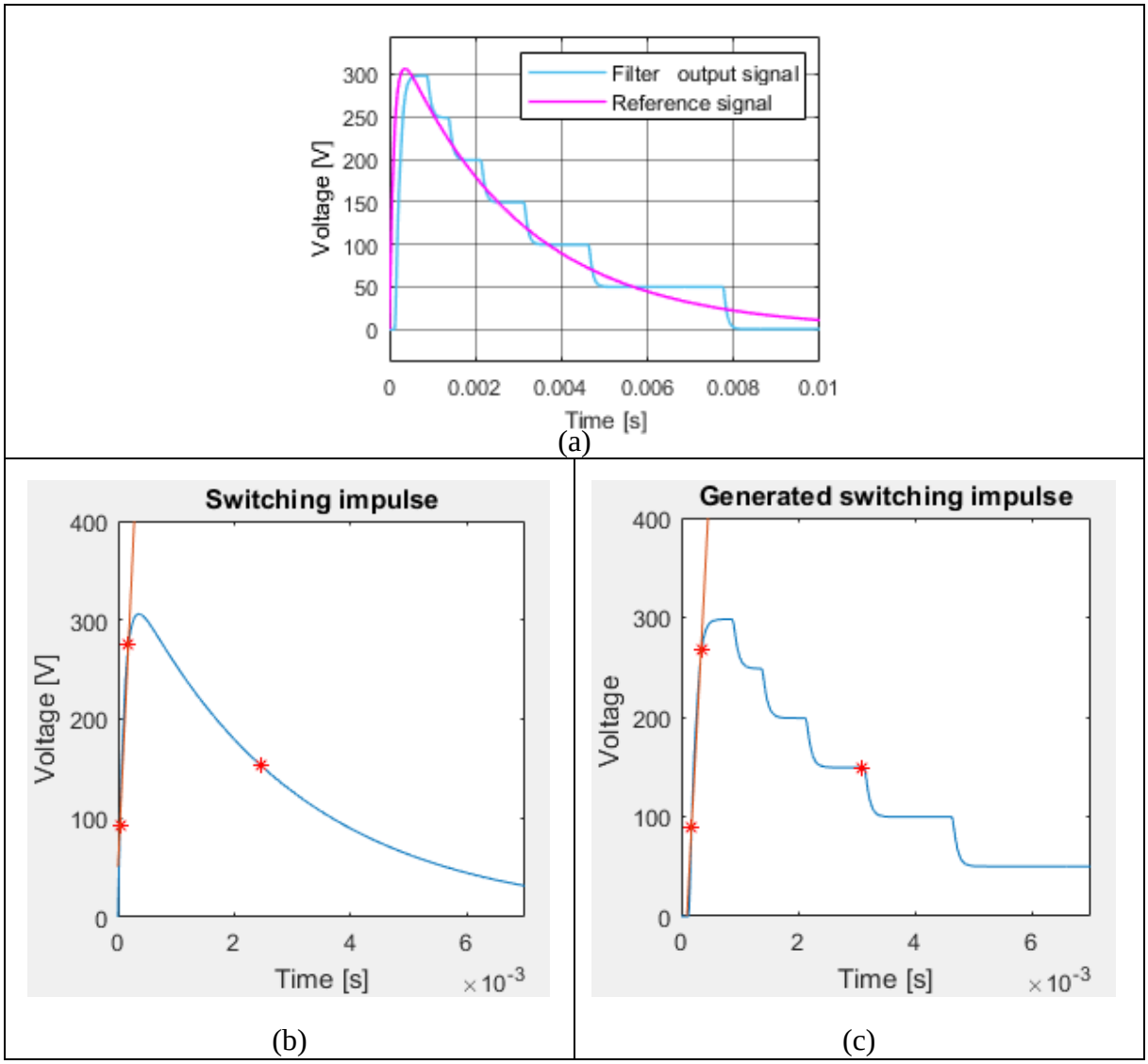


Figure 5-21: (a) Filter output (b) Tolerance calculation for standard SI (c) Tolerance calculation for obtained SI

The power dissipation in both arm resistances and filter resistance is shown in figure. Energy lost in them is also calculated by integrating these waveforms:

Energy loss through the upper arm resistance (400 Ω) = 0.0021 J
Energy loss through the lower arm resistance (400 Ω) = 0.0021 J
Energy loss through the upper arm resistance (200 Ω) = 0.0085 J

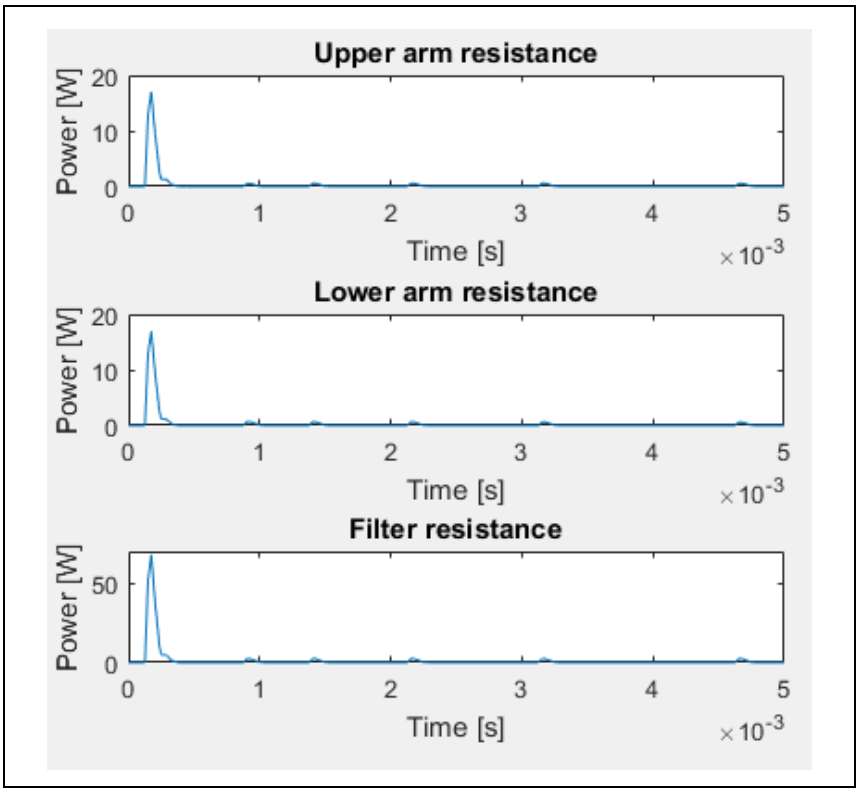


Figure 5-22: Power dissipation – switching impulse signal

5.5 Summary

A simple RC low filter topology is chosen to remove the unwanted harmonics from the converter output signal with 16 submodules. For the small-scale prototype, this topology is an acceptable choice with respect to the power loss in the system. The percentage error in the peak voltage depends upon the type of signal (filter resistance, fundamental frequency, switching frequency etc.). For arbitrary wave shapes from 0.1 Hz to 1000 Hz frequency, the filter parameters are chosen as per cut-off frequency requirement. The filter resistance ranges from 100 Ω and 800 kΩ with three different filter capacitances (0.01 µF or 0.1 µF or 1 µF).

When the small-scale prototype is extended to higher voltage level, number of submodules will increase. The voltage step with high number of submodules reduces, making the generated output voltage resemble to the desired signal. The remaining small voltage step will be removed by the arm inductance and resistance. Hence filter design will not be necessary at higher voltage level.

6. PROTECTION SYSTEM AND DC SIDE SOURCE REQUIREMENT

This chapter discusses the fault characteristics of the MMC-based test source and how to protect the system when a fault occurs. Next, an alternative DC source arrangement is proposed instead of ideal DC sources for higher voltage levels, and its requirements are briefly discussed.

6.1 Protection system design

This section discusses types of faults that can occur in the test setup, their characteristics and how to protect the system from all these faults. Generally, there are four types of fault experienced by MMC used for power applications and those are mentioned below [8]:

- AC network faults at point of common coupling
- AC faults inside the converter station
- DC faults, e.g. pole-to-pole or pole-to-ground faults;
- Converter internal faults, e.g. submodule faults, modulation and control faults, phase-reactor fault

For the HV test source, the two types of AC side faults are not relevant since it is not a grid connected system. The following types of faults are considered for a single phase MMC-based test source and they are shown in figure 6-1:

- Breakdown of the test object
- Converter internal faults
- DC source fault

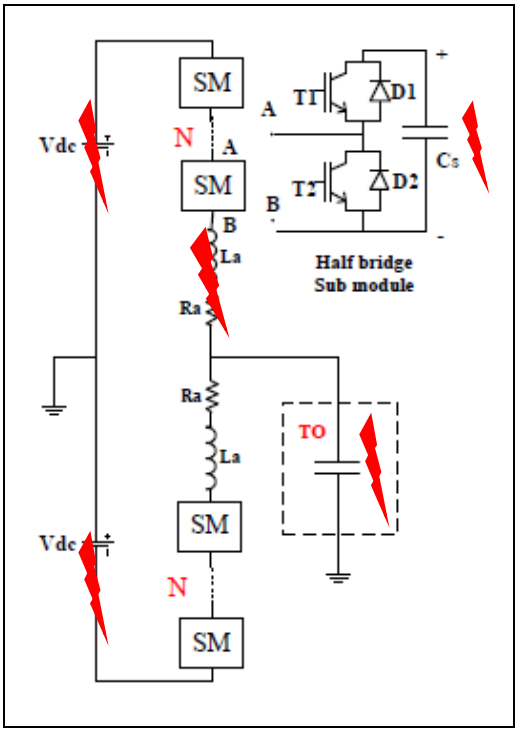


Figure 6-1: Different types of faults in MMC based HV test source

Often HV tests are destructive. It means that the test object breaks down when the HV test signal is applied. It is important that the protection system detects this breakdown and switches off the supply instantly. The converter response to this type fault is discussed in the next subsection. Converter internal faults include submodule semiconductor failure, submodule capacitor failure, arm inductance and resistance failure, and control signals and communication system failures. Since practical implementation of the semiconductor devices and control system is not discussed in this thesis, failures in semiconductor devices, control signals and communication system are not analyzed in the next sub section. Since HV test source is a load connected system, a DC fault can occur only if the DC source is short circuited.

6.1.1 Breakdown of the test object

When the test object breaks down, the equivalent circuit of the test source will reduce to arm inductance, arm resistance and filter resistance. Figure 6-2 shows the equivalent circuit. Since the test object is modeled as a pure capacitance, it can be observed that the filter capacitance is short circuited. In real test object, small resistance and inductance will be present and filter capacitance will not get shorted. In simulation results, a small fault resistance (R_{fault}) is programmed while implementing the fault.

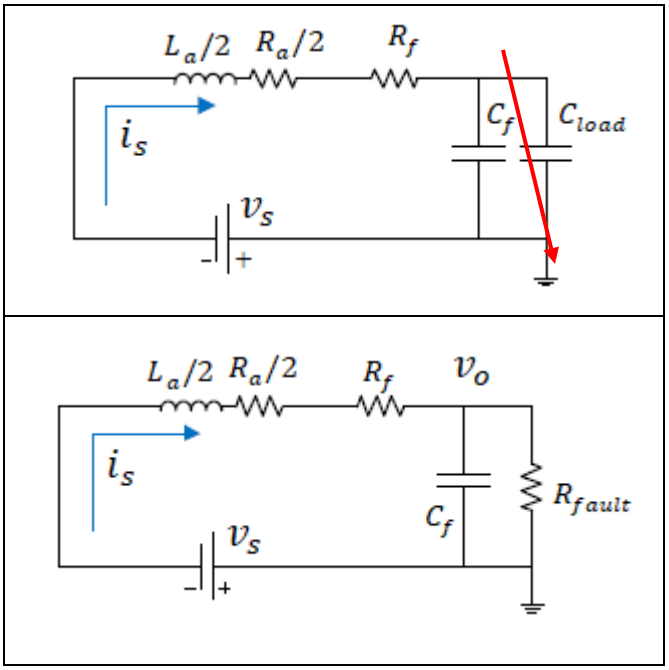


Figure 6-2: Equivalent circuit when there is breakdown in test object

When the test object breaks down, a large current (v_o/R_{fault}) will flow through the broken test object. This current will discharge the filter capacitance very fast (time constant = $R_{fault}.C_f$). The converter will operate as if there is only resistive load (R_f). Highest value of the fault current drawn from the converter will be when v_s is maximum and R_f is minimum. From the test cases in the 5th chapter, the 50 Hz trapezoidal with 0.001 s rise time had the smallest R_f as 160 Ω. For 400 V prototype, the fault current magnitude is calculated in equation 6.2:

$$I_{s@fault} = \frac{v_s}{\frac{R_a}{2} + R_f} = \frac{400\ V}{200 + 160\ \Omega} = 1.11\ A \tag{6.1}$$

$$I_{u@fault} = \frac{I_{s@fault}}{2} = 0.552\ A \tag{6.2}$$

From equation 4.33 and 4.34, the peak of upper arm current or lower arm current can be calculated as 0.24 A. The fault current drawn from the converter is comparable to the steady state current magnitude since the system resistance is high. It can be observed in the simulation results shown in figure 6-3. The red arrow in the figure indicates when the fault occurs.

For other wave shapes, the fault current magnitudes will be even lower since the filter resistance is higher. A more realistic case for the fault current calculation is with the converter at high voltage and without the filter resistance. In this situation, the fault current drawn from the converter will be in kA. Hence a similar fault current analysis should be conducted for the high voltage prototype. But, preliminary analysis with 400 V simulation model suggests that the slope (dv/dt) of the test signal can be monitored to operate the protection.

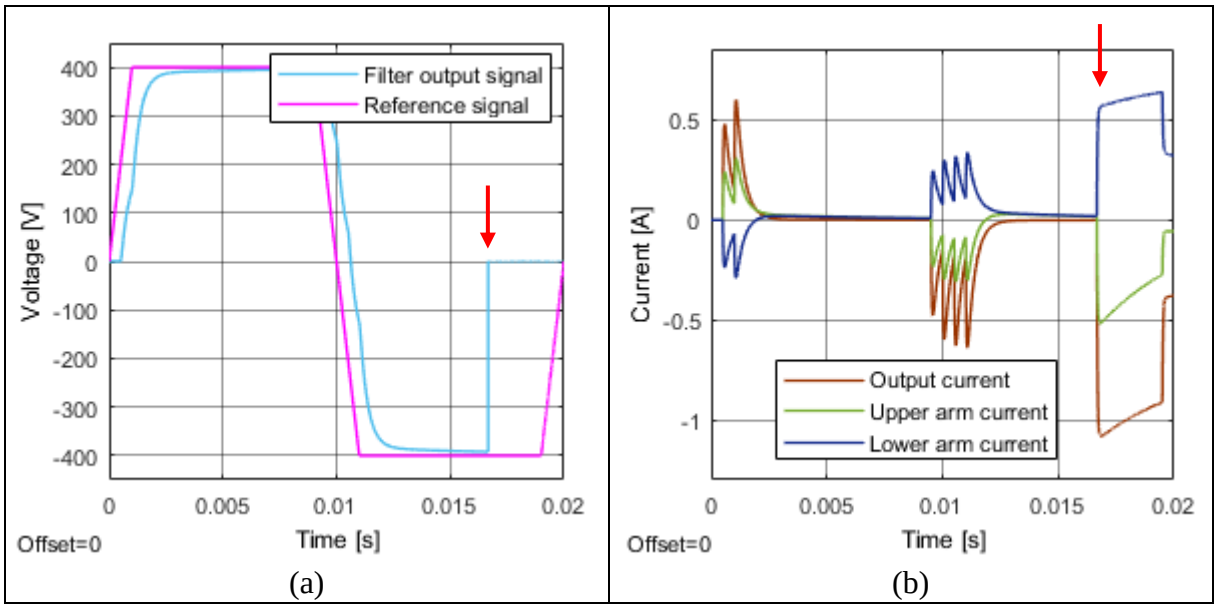


Figure 6-3: TO failure (a) Converter output signal (b) Current signals

6.1.2 Converter internal fault

Failures in converter components i.e. submodule capacitance, arm inductance, and arm resistance are discussed. The impact of these failures on the converter operation is investigated below:

- **Submodule capacitance failure**: The breakdown of SL1 capacitor is simulated in the Simulink model. The effect of the submodule capacitor failure is visible as voltage drop in the output signal. This phenomenon can be compared to the submodule bypassing and it will be reflected in arm currents and output current as pointed out in figure 6-4 (b) with a red arrow.

- **Arm inductance failure:** Figure 6-5 shows the effect of upper arm inductance failure on the converter operation. The effect of arm inductance failure is visible only if there is switching of submodules. Upper arm currents are falling instantly which will destroy the semiconductor device since they are not designed for this high value of di/dt. It introduces circulating current spikes abnormally in the system as shown in figure 6-5 (d).

- **Arm resistance failure**: Arm resistance failure will create the unbalance between upper and lower arm current which is evident in figure 6-6 (b). Large upper arm current will reduce the capacitor voltage which is responsible for the small dip in the output voltage signal.

From the above analysis, it can be understood that these failures do not increase the arm currents very much. Hence the current magnitude cannot be used for operating protection. In case of arm inductance failure, protection can be designed based on the di/dt threshold on the input current. For submodule capacitance and arm resistance failure detection, submodule capacitor voltages need to be monitored since both these failures introduce a large variation in the submodule capacitor voltage.

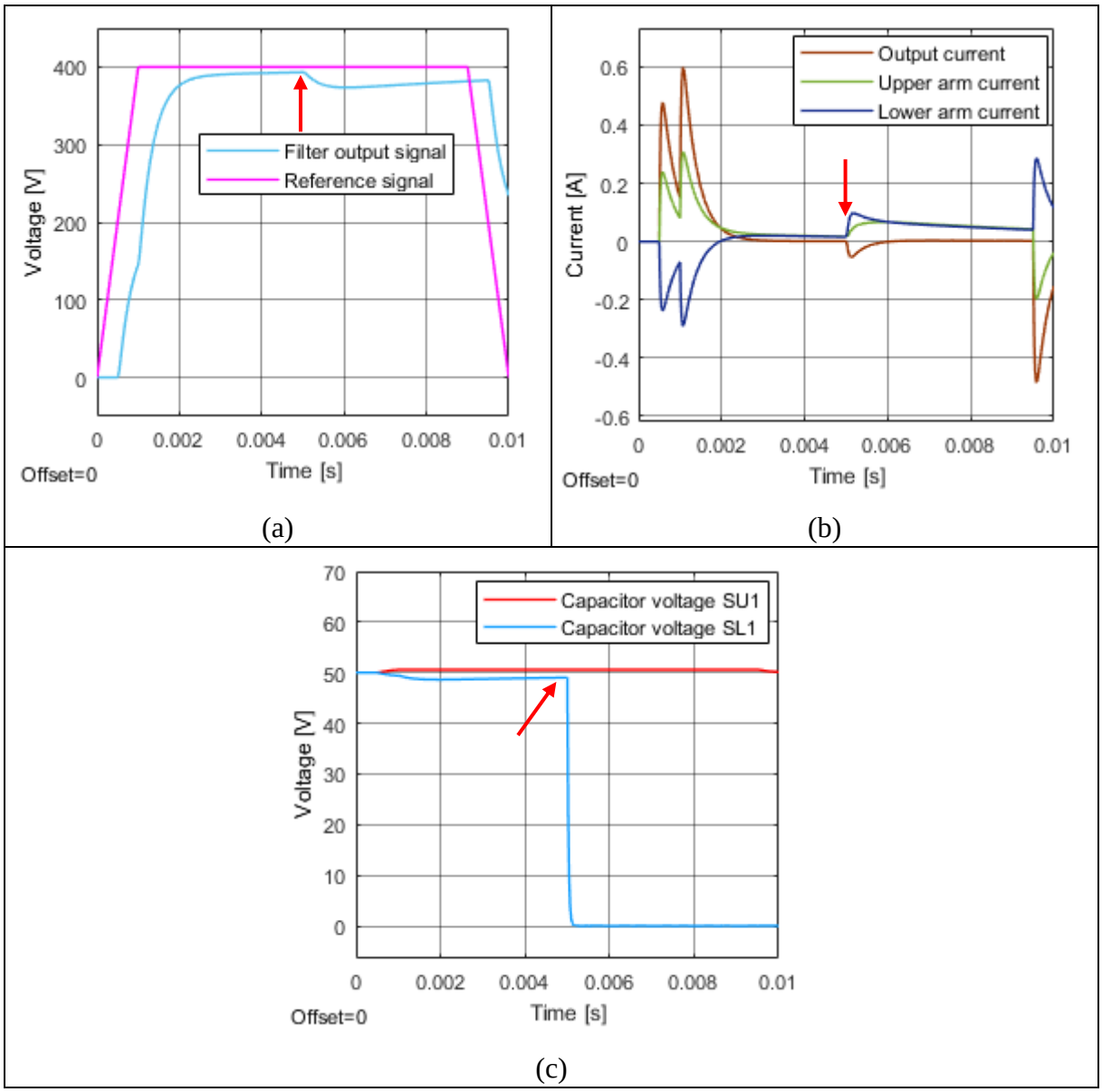


Figure 6-4: Submodule capacitor failure (a) Converter output signal (b) Current signals (c) Submodule capacitor voltage

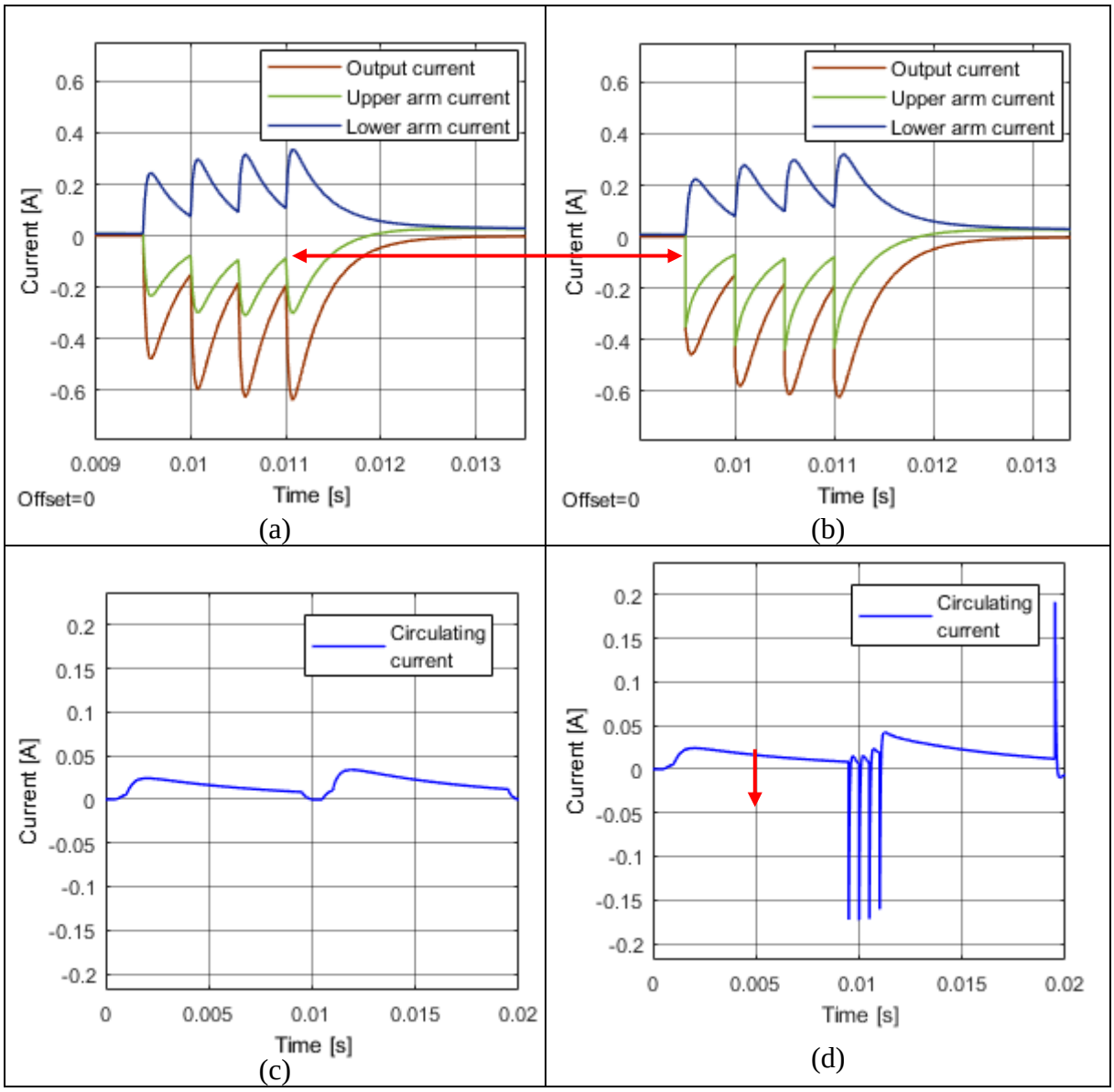
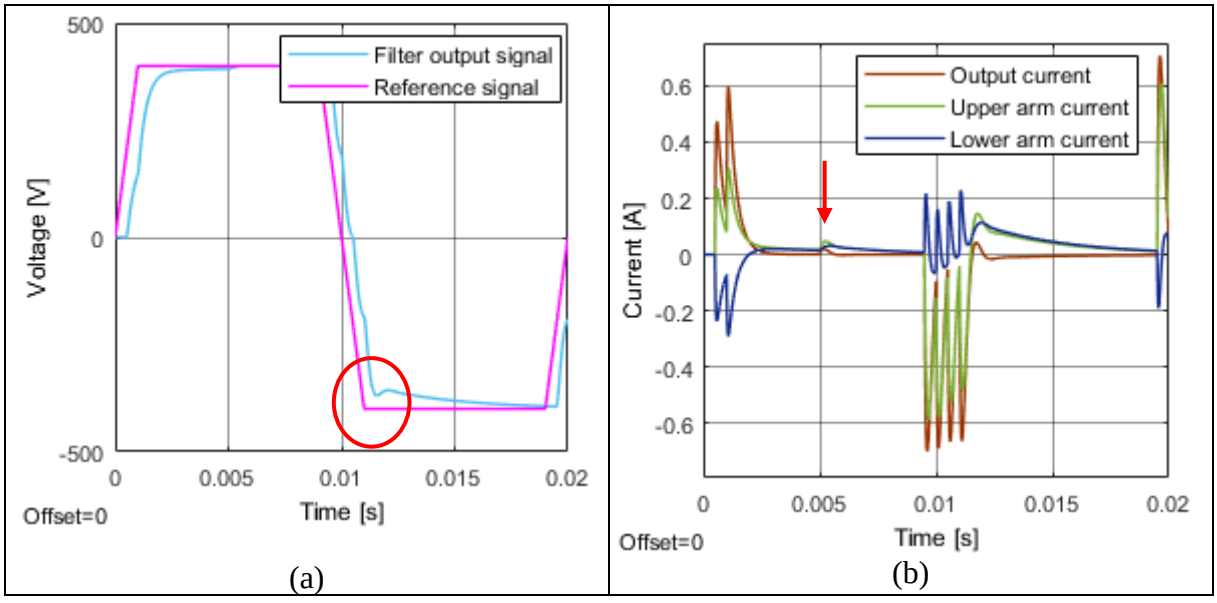
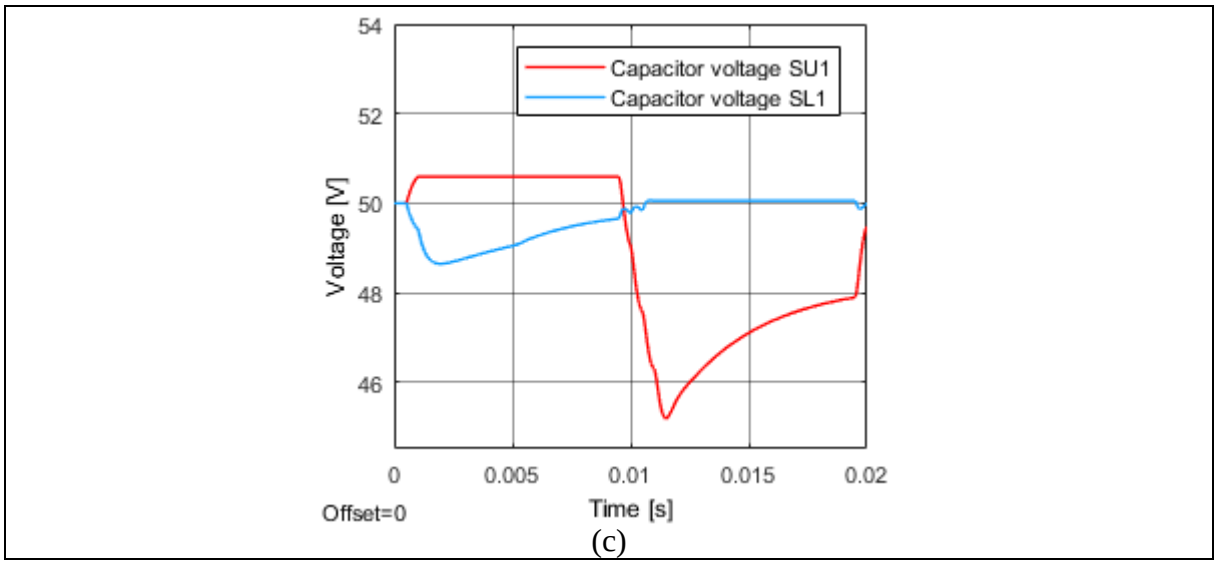


Figure 6-5: Before arm inductance failure (a) current signals (zoomed picture) (c) circulating current signal; After arm inductance failure (zoomed picture) (c) current signals (d) circulating current signal



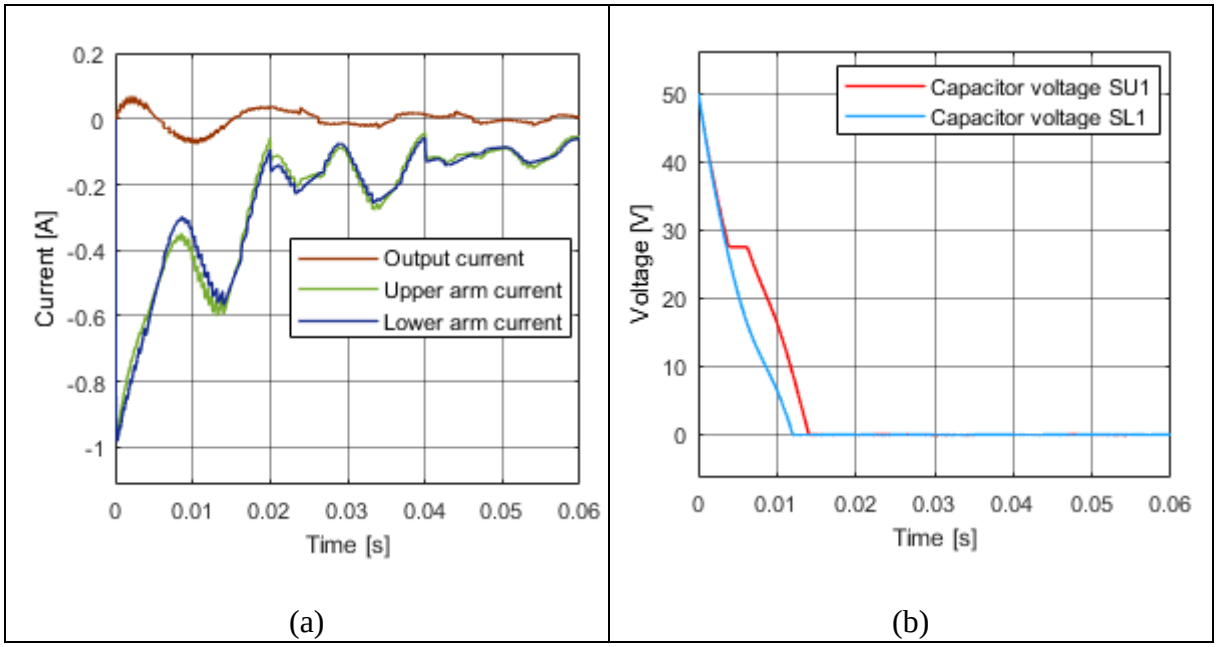


(c)

Figure 6-6: Arm resistance failure (a) Converter output signal (b) Current signals (c) Submodule capacitor voltage

6.1.3 DC source fault

When a DC side fault occurs, the input source of the converter is short circuited. Since the connected load is passive, the load side of the converter will not contribute in the fault current. But, the submodule capacitances will discharge and add to the fault current. The DC side short circuit is simulated in the Simulink model by substituting the zero DC source voltage. The arm current behavior is shown in figure 6-7.



(a) (b)

Figure 6-7: DC side short circuit (a) Arm current and output current (b) Capacitor voltage

In the case of the DC side short, the peak arm current becomes 5 times higher than the steady state peak value of arm current at the start. The magnitude of the arm current decreases since the stored energy in the submodule capacitances decreases. The DC source will have a self-protection for such a condition, but the drop-in capacitor voltage can detect the DC side short circuit.

6.1.4 Summary of the protection system

From the above discussion, it is important to monitor the following converter quantities to prevent the damage from any fault:

- dv/dt of the output voltage → Test object breakdown
- di/dt of the input current → Arm inductance fault
- Submodule capacitor voltages → Arm resistance and submodule capacitance fault

If any of these quantities exceed from the safety threshold, the input supply to the converter should be stopped by a controlled switch. For high voltage testing application, identifying the test object breakdown is most important since it is the most frequent phenomenon. The operation of the controlled switch is designed for only periodic signal which are generated continuously for many hours. For switching impulse, it will not be possible to operate the controlled switch because of the short duration of the impulse. Even the classical impulse generator is protected only if the current drawn from the AC source is above the threshold by cutting off the input AC supply.

The threshold value of di/dt (input current) and the submodule capacitor voltage is fixed since the converter component are designed for 20 kA/s of di/dt and 50±5 V of capacitor voltage ripple. The threshold value of dv/dt (output voltage) will depend upon the amplitude and frequency of the signal. When a signal with 400 V magnitude and 1000 Hz frequency is generated, signal dv/dt is 400 kV/s which can be used as threshold value. Hence the threshold value of dv/dt should be set differently according to the magnitude and frequency. Figure 6-8 shows the overview of the protection system.

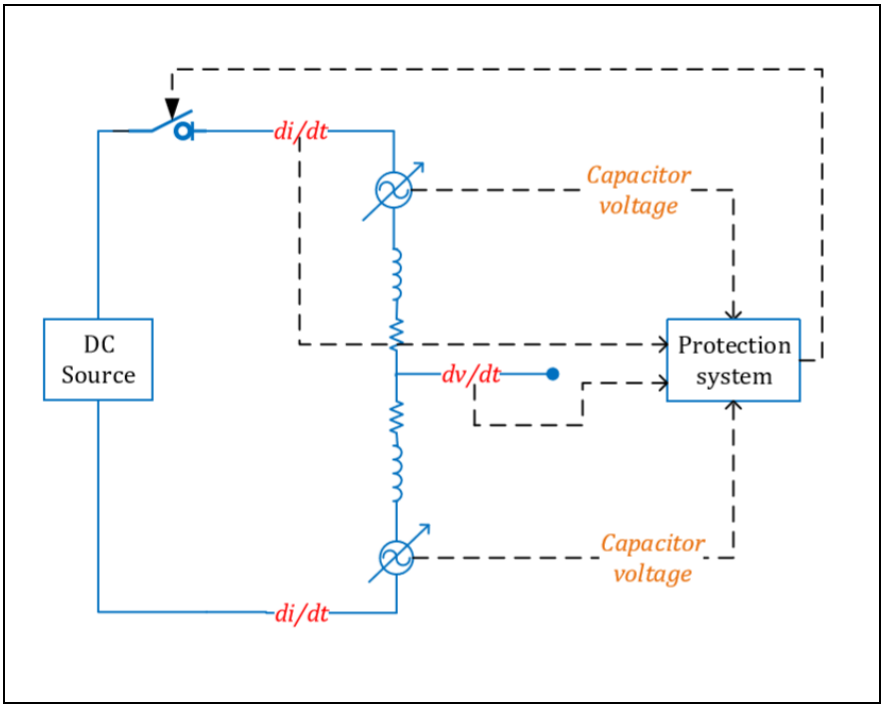


Figure 6-8: Overview of the protection system

6.2 DC side source requirement

The DC side source is assumed to be an ideal DC one till now. At higher voltage level, ideal DC source is not the most suitable option. Hence, a diode rectifier and DC link capacitance setup is proposed for lab testing, as shown in figure 6-9. It is important to study the behavior of the converter with DC link capacitances to understand what magnitude of capacitances to be used.

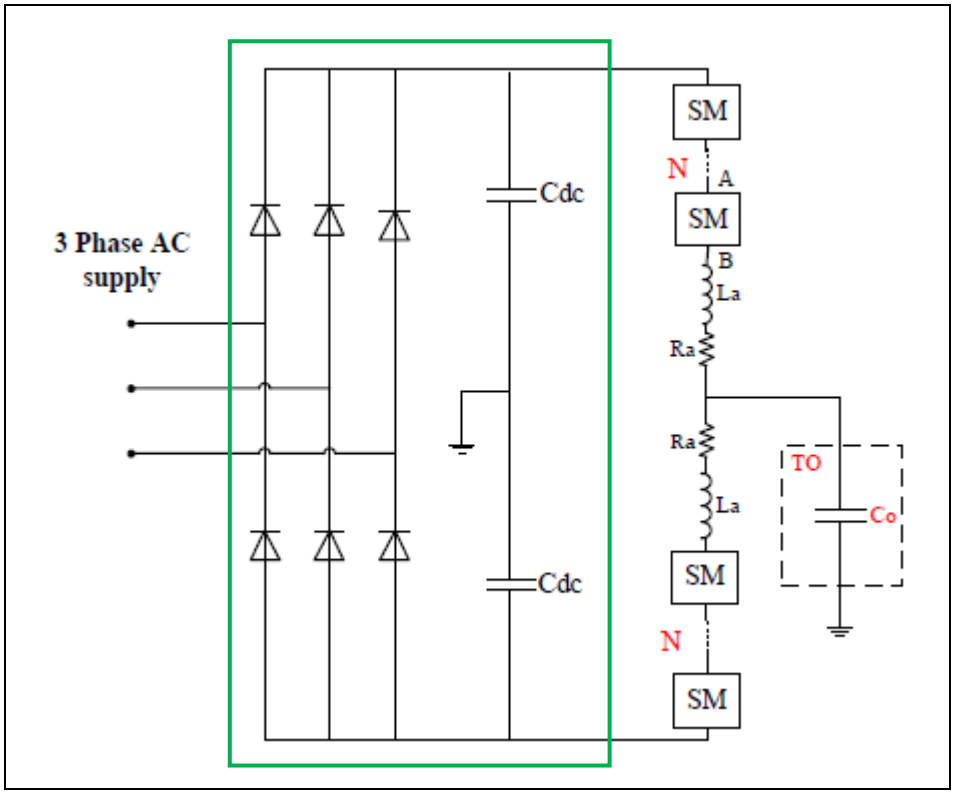


Figure 6-9: DC source realization

The DC link capacitances maintain the submodule capacitance voltage and provide/absorb the output current. Though the magnitude of power transfer is small, its direction depends upon the output current direction. When the load capacitance is charging up (positive slope of the output voltage), the positive output current needs to be provided by the DC link capacitance and power transfer occurs from the converter to load. When the load capacitance is getting discharged (negative slope of the output voltage), the output current direction is negative, and the power transfer occurs from the load to the converter. Table 6-1 summarizes the above description and figure 6-10 shows the current direction (blue) and power transfer direction (red).

Table 6-1: Direction of power transfer

Magnitude of output voltage	Slope of the output voltage	Output current direction	Power transfer direction
Positive	Positive	Positive	Converter to load
Positive	Negative	Negative	Load to Converter
Negative	Negative	Negative	Load to Converter
Negative	Positive	Positive	Converter to load

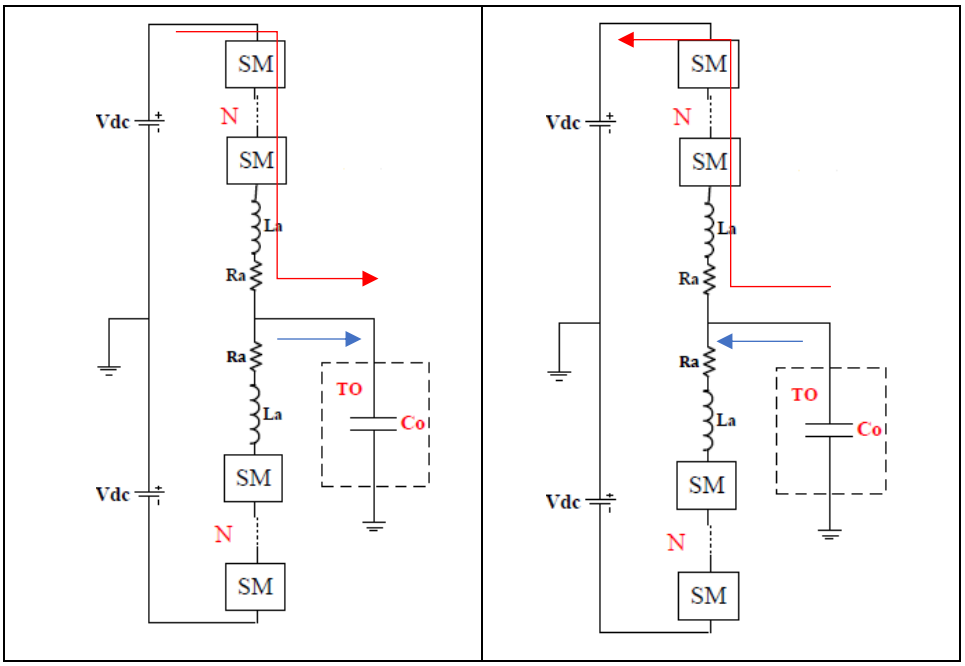


Figure 6-10: Power transfer direction and output current direction

The effect of DC link capacitance is studied by substituting the ideal DC source with 0.01 F DC link capacitance at 400 V. Simulation results of 50 Hz sinusoidal signal are shown in figure 6-11. As expected, the charging and discharging of the DC link capacitor depends upon the output current direction. At the end of 1st cycle of 50 Hz sinusoidal, the DC link capacitance experiences a voltage drop of 0.0025 %. This voltage drop continues linearly for more cycles as shown in figure 6.11 and its slope depends upon the system resistance. If the system resistance (arm resistance + filter resistance) is higher, the rate of change of the voltage is fast.

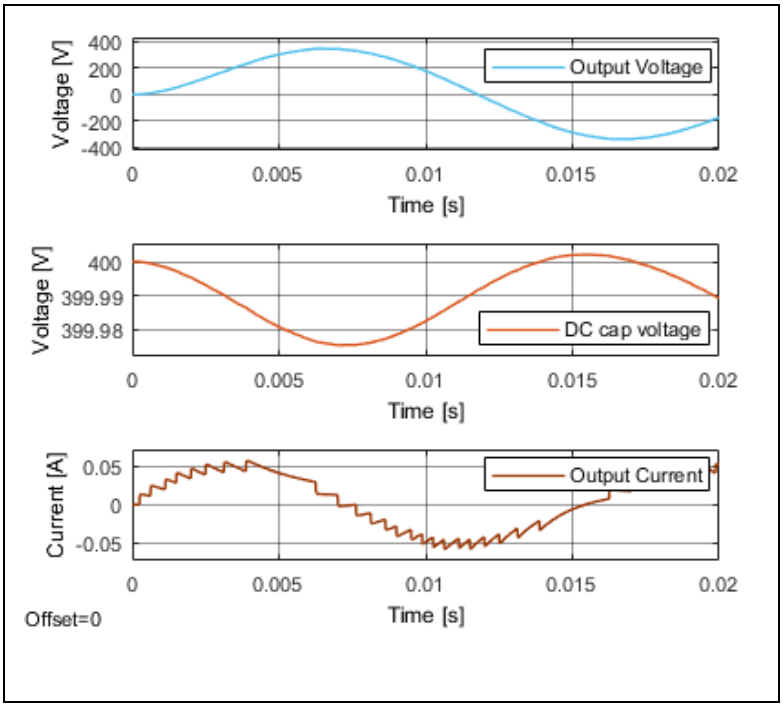


Figure 6-11: DC side capacitance voltage variation for 1 cycle

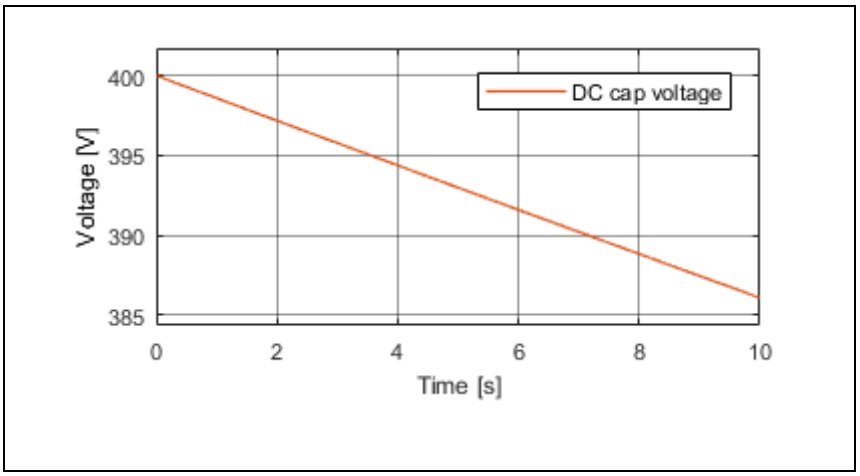


Figure 6-12: DC side capacitance voltage variation for 10 s duration

The 0.0025 % drop in the capacitor voltage suggests that the diode rectifier setup will not have large power requirement. Hence the droplet charging concept can be used. Though figure 6-11 shows a significant drop after 10 s, it is because of large filter resistance value for sinusoidal (1.5 kΩ). This voltage drop depends upon the system parameter and should be studied in detail to optimize the DC source requirement. The DC source is a major problem to tackle in realization of this test source, especially for developing a mobile test source.

6.3 Summary

The protection is designed for the test source from TO breakdown, internal faults, and DC source fault. The protection operates when the threshold is crossed by di/dt of the input current, dv/dt of the output voltage, and submodule capacitor voltages. Ideal DC sources are replaced with DC link capacitances to study the feasibility of diode rectifier setup. The brief discussion needs further investigations.

7. CONCLUSIONS AND RECOMMENDATIONS

This is the last chapter of this thesis report. It concludes the work of this master's thesis with recommendations for future work with a PhD proposal to DNV GL.

7.1 Conclusions

The main objective of this master's thesis is successfully achieved by proving the feasibility of a MMC-based high voltage test source for arbitrary wave shape generation, using the mathematical modeling and simulation results.

The control methodology and converter parameter design of existing MMC applications are adapted for high voltage testing application. A low pass filter is designed to obtain a smooth output signal with 16 submodules (small-scale prototype). The study of the new type of test source is completed by having a brief discussion regarding its protection system and DC side source requirement. The following conclusions can be drawn from this master's thesis work:

- The mathematical model and simulation results developed in this master's thesis demonstrate that the MMC can be used for generating arbitrary wave shapes with different magnitude and frequency at 400 V.
    - The simulation results demonstrate the open loop control of the MMC
    - The arm resistance can give an additional degree of freedom to obtain the desired system response.

- The preliminary analysis using literature (for the control methodology) and mathematical model (for the converter parameters) proves the scalability of the test source to higher voltage levels.

- For higher voltage levels, the number of submodules increases which eliminates the need of filter. An increased number of submodules will reduce the voltage step generated and the output voltage more resembled the desired signal. The remaining smaller voltage step can be removed by the arm inductance and arm resistance.

- The MMC-based test source can provide high flexibility in generating complex signals such as superimposed signals, bipolar impulses etc. It can eliminate the need for tedious design of a test setup for the superposition of two voltage sources.

- With the careful design of the DC source, it is possible to develop this MMC-based test source as a mobile test generator for onsite testing with the capability of arbitrary wave shape generation.

- It opens an entire new high voltage research area and can be revolutionary for the high voltage testing domain.

7.2 Recommendations

The following recommendations are made for further improvements:

- This master's thesis demonstrates the steady state behavior of the converter. A safe start up and shut down procedure should be prepared. Startup procedure will include charging submodule capacitances to an average value. Standard procedures adapted from existing MMC applications can be used directly for this application.

- The entire converter analysis is based on ideal semiconductor devices. Though the switching and conducting losses in these semiconductor devices will not be significant in this application unlike power application, it is important to consider the turning-on and turning-off time of these devices. It might impose a limitation on the maximum frequency to be generated from the converter. Hence, the mathematical model and simulation results should be validated on ***a small-scale prototype*** with real semiconductor devices.

- For scaling up to higher voltage, preliminary analysis indicates that losses in the arm resistance will become significant. Hence it might require a special design for the higher voltage level.

- For a mobile test source, a detailed study on the DC source design needs to be conducted so that the entire test system can fit on a truck.

This master thesis shows the potential of an MMC-based HV source for testing components and subsystems in an electronic rich future power system. As this development opens an entire new research area a PhD is proposed to DNVGL to further develop an ***EHV test source*****.** It will include

  - Business case
  - Specification of the requirements (voltage, bandwidth, mobility, accuracy etc.)
  - Design of the test source
  - Building a first prototype

The performance of this new HV test source will be compared with the existing test sources by conducting dielectric tests across different HV test objects. Also, the PhD will cover the new possibilities for testing and how to develop the DNVGL laboratory facilities to be fit for the power electronic dominated grid of the future

Appendix A: MATLAB-Simulink implementation

A 1 – PSC Implementation

As explained in chapter 3.2, gate pulses are generated by comparing reference signal with carrier signal and its Simulink implementation is shown in figure A 1.1. Carrier signals can be generated manually by feeding the phase shifts in the triangular signal Simulink block as shown in figure A 1.2.

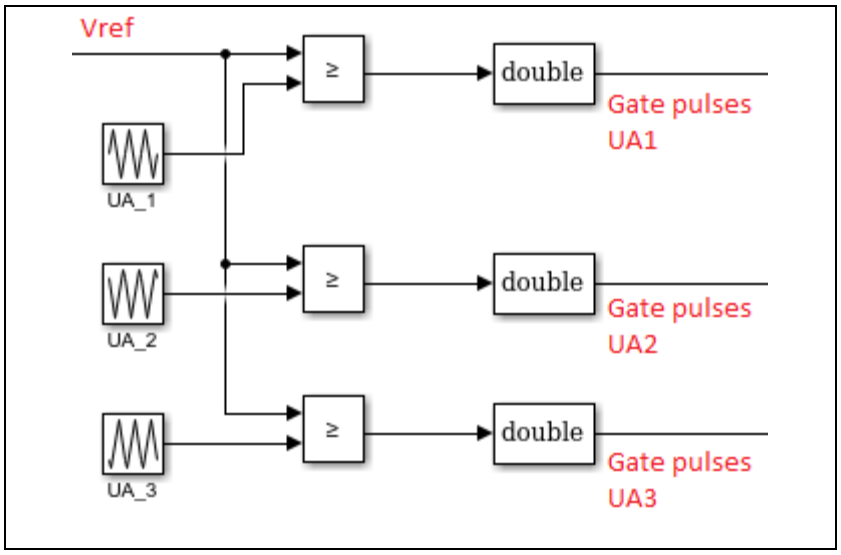


Figure A 1.1: PSC implementation in Simulink

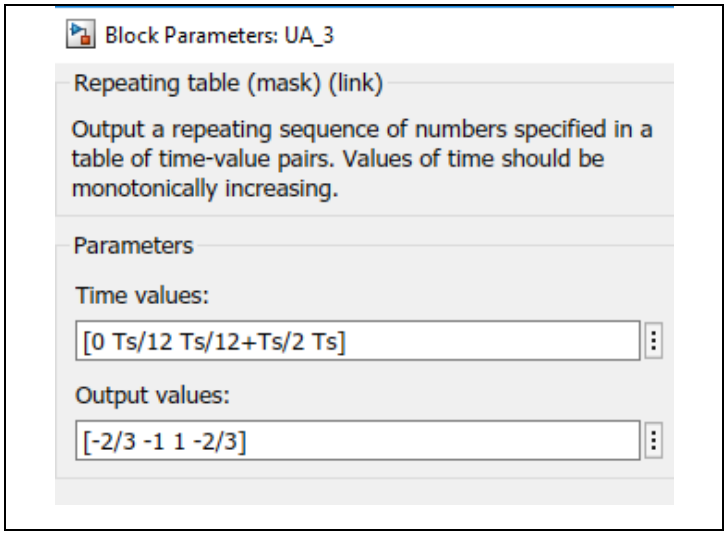


Figure A 1.2: Simulink implementation of triangular carrier signal

It is possible to avoid generating manually so many triangular signals using a in-built Simulink block of PSC generation for multilevel converter. The main limitation faced in this block representation was that the block generates gate pulses for upper arm and lower arm without any phase shift. Simulink does not allow to have two PSC blocks with different phase difference in the carrier signal. To generate 2N+1 PSC for even numbers and N+1 PSC for odd numbers, it was necessary to introduce phase shift between upper arm and lower arm. Hence the manual approach was followed, but figure shows the Simulink block for gate pulses generation.

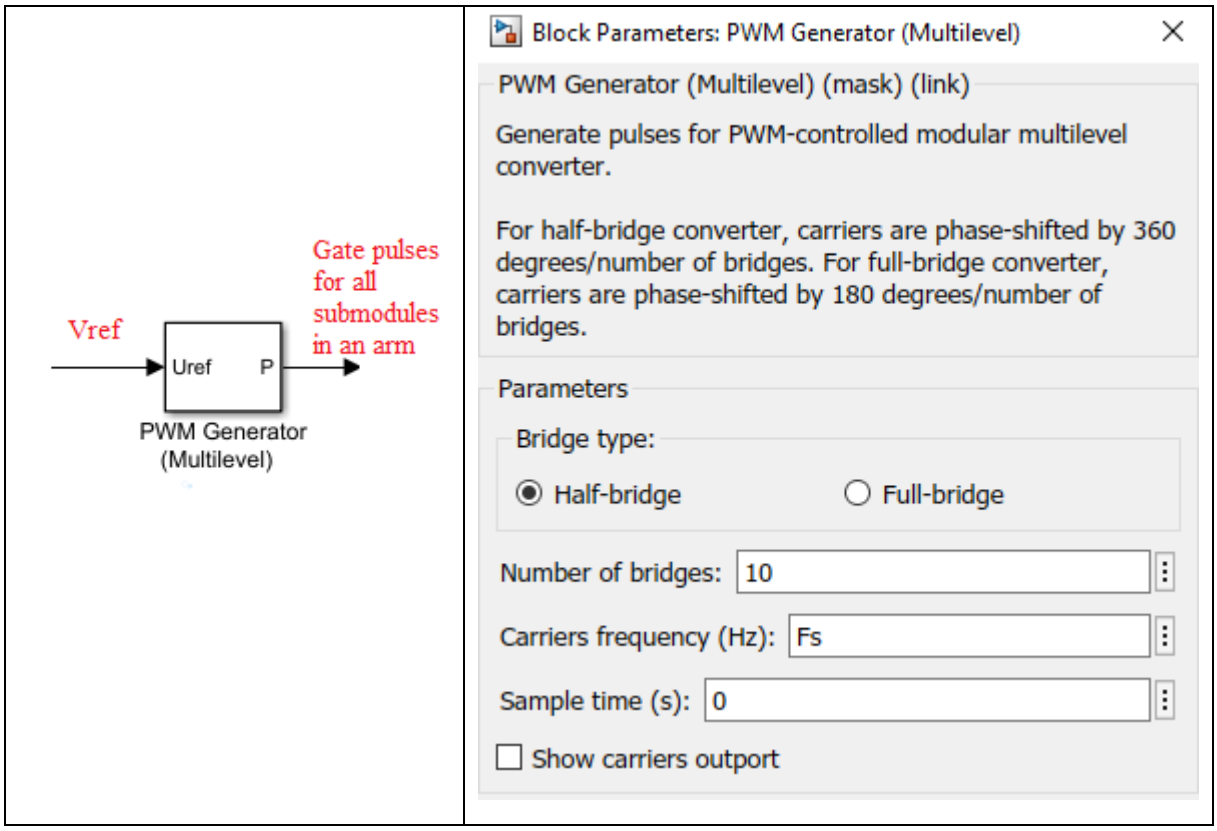


Figure A 1.3: In-built Simulink block for PSC implementation

A 2 – NLC Implementation without sorting

Equation 3.1 and 3.2 can be converted into a Simulink block implementation as shown in figure A 2.1.

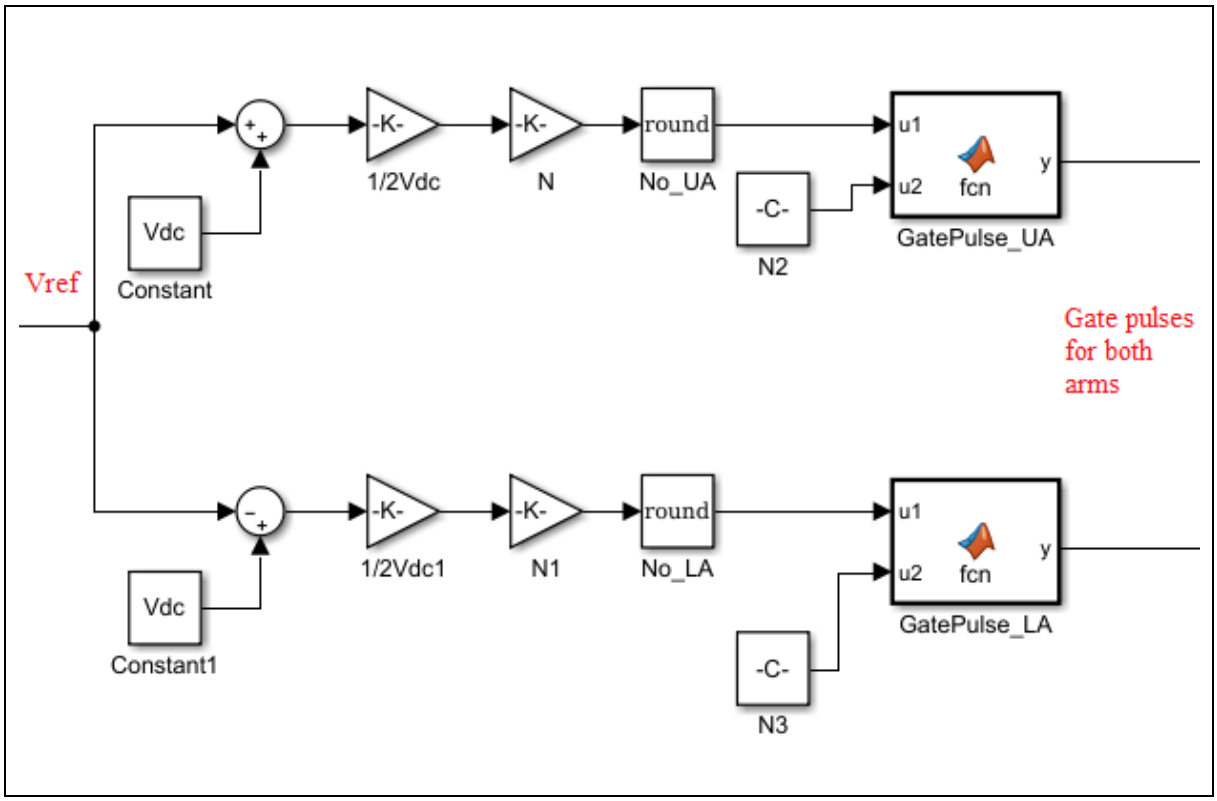


Figure A 2.1: NLC implementation without sorting in Simulink

Gate pulses can be generated from insertion indices by implementing following MATLAB code.

```
function y = fcn(u1, u2)
%u1 = No of submodules to be inserted
%u2 = Total number of submodules in MMC
i=0;
pwm=zeros(u2);
for i=1:u2
    if i<=u1
        pwm(i)=1;
    else
        pwm(i)=0;
    end
end
y=[pwm(1) pwm(2) pwm(3) pwm(4) pwm(5) pwm(6) pwm(7) pwm(8) pwm(9) pwm(10)
pwm(11) pwm(12) pwm(13) pwm(14) pwm(15) pwm(16)];
```

A 3 – NLC implementation with sorting algorithm

As discussed in chapter 3.7, a novel sorting algorithm which does not use any feedback from the converter is implemented as shown in figure A 3.1. To implement a sorting algorithm, it is important that the insertion indices are sampled so that the switching frequency can be kept independent to the simulation time step.

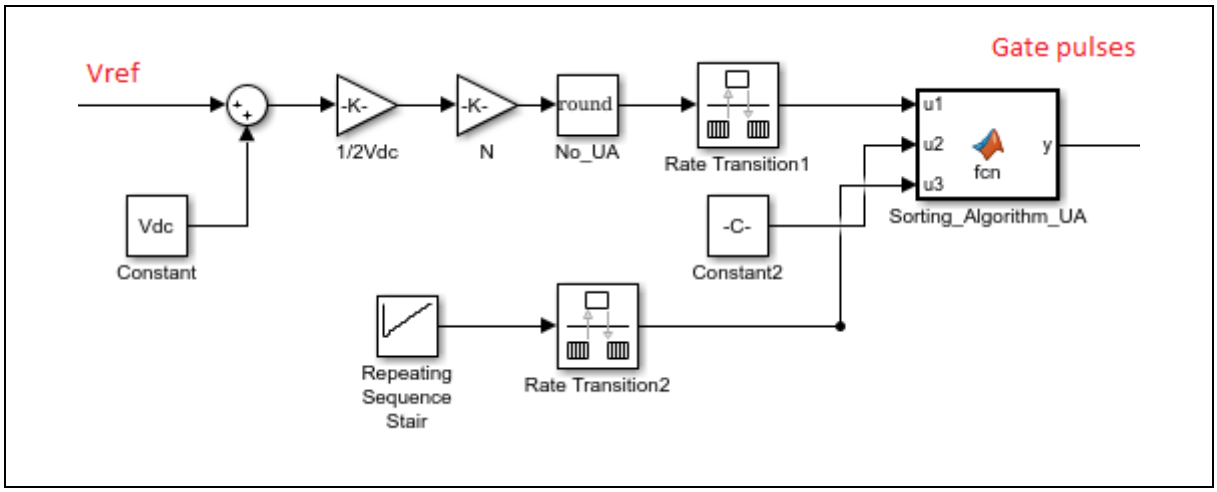


Figure A 3.1: NLC implementation with sorting algorithm in Simulink

The MATLAB code for the sorting algorithm is shown below:

```
function y = fcn(u1, u2, u3)
%u1 = No of submodules to be inserted
%u2 = Total number of submodules in MMC
%u3 = number of row input
i=0;
A = [1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16;
    16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15;
    15 16 1 2 3 4 5 6 7 8 9 10 11 12 13 14;
    14 15 16 1 2 3 4 5 6 7 8 9 10 11 12 13;
    13 14 15 16 1 2 3 4 5 6 7 8 9 10 11 12;
    12 13 14 15 16 1 2 3 4 5 6 7 8 9 10 11;
    11 12 13 14 15 16 1 2 3 4 5 6 7 8 9 10;
    10 11 12 13 14 15 16 1 2 3 4 5 6 7 8 9;
    9 10 11 12 13 14 15 16 1 2 3 4 5 6 7 8;
```

```
    8 9 10 11 12 13 14 15 16 1 2 3 4 5 6 7;
    7 8 9 10 11 12 13 14 15 16 1 2 3 4 5 6;
    6 7 8 9 10 11 12 13 14 15 16 1 2 3 4 5;
    5 6 7 8 9 10 11 12 13 14 15 16 1 2 3 4;
    4 5 6 7 8 9 10 11 12 13 14 15 16 1 2 3;
    3 4 5 6 7 8 9 10 11 12 13 14 15 16 1 2;
    2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 1];

pwm=zeros(u2);
row = u3;

for i=1:u2
    if i<=u1
        pwm(A(row, i))=1;
    else
        pwm(A(row,i))=0;
    end
end
y=[pwm(1) pwm(2) pwm(3) pwm(4) pwm(5) pwm(6) pwm(7) pwm(8) pwm(9) pwm(10)
pwm(11) pwm(12) pwm(13) pwm(14) pwm(15) pwm(16)];
```

A 4 – Switches Implementation

The performance of modulation techniques is studied by implementing the converter topology in Simulink. The schematic is shown in figure A 4.1 and the submodule implementation is shown in figure A 4.2. The schematic is shown for N=3 and the model is easily extended for more number of submodules by adding submodules on top of each other.

Simulation settings include continuous solver since behavior of the converter is studied using this model. Within continuous solver, ode45 gives most stable and accurate solution.

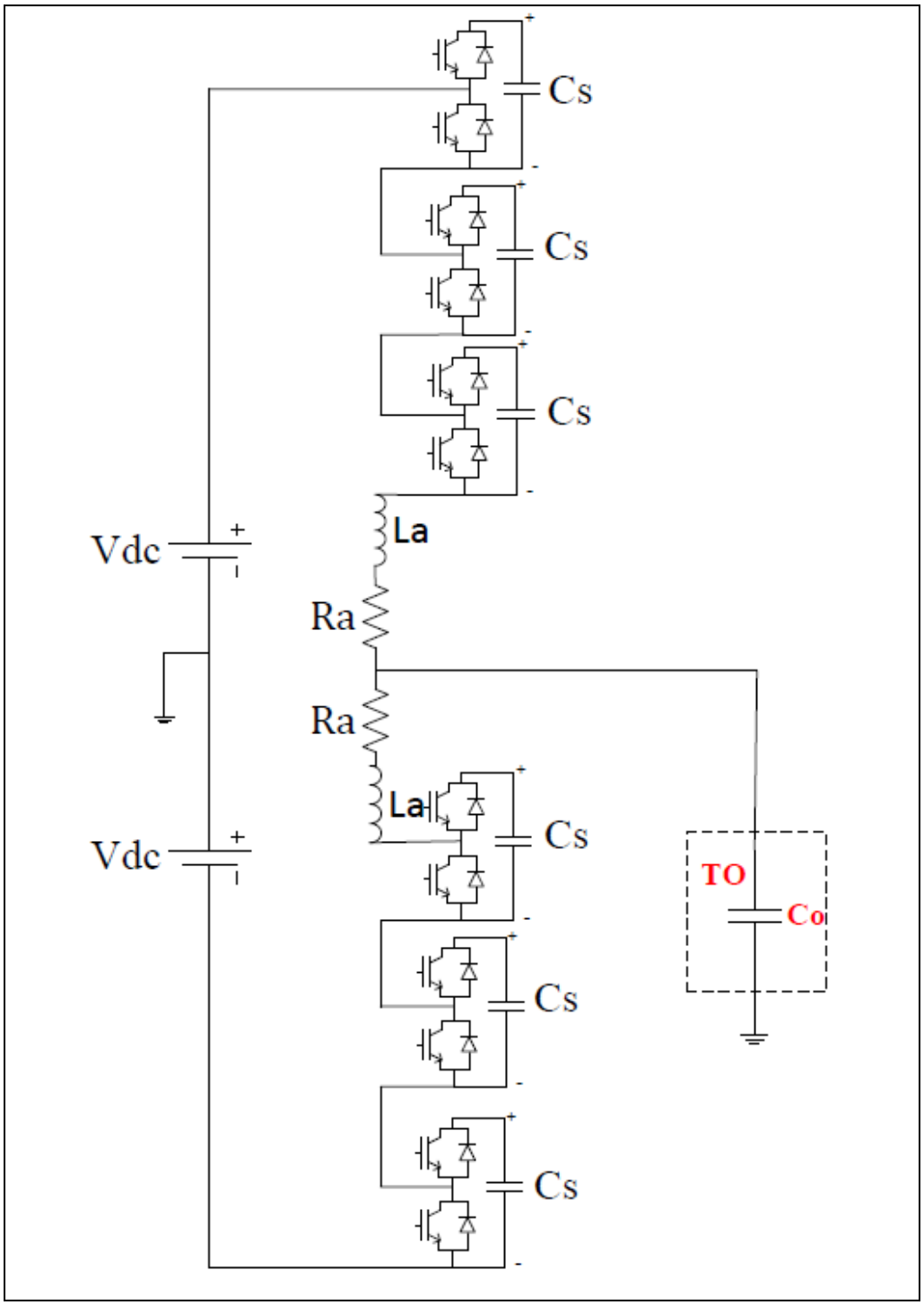


Figure A 4.1: Schematic of MMC for high voltage testing application

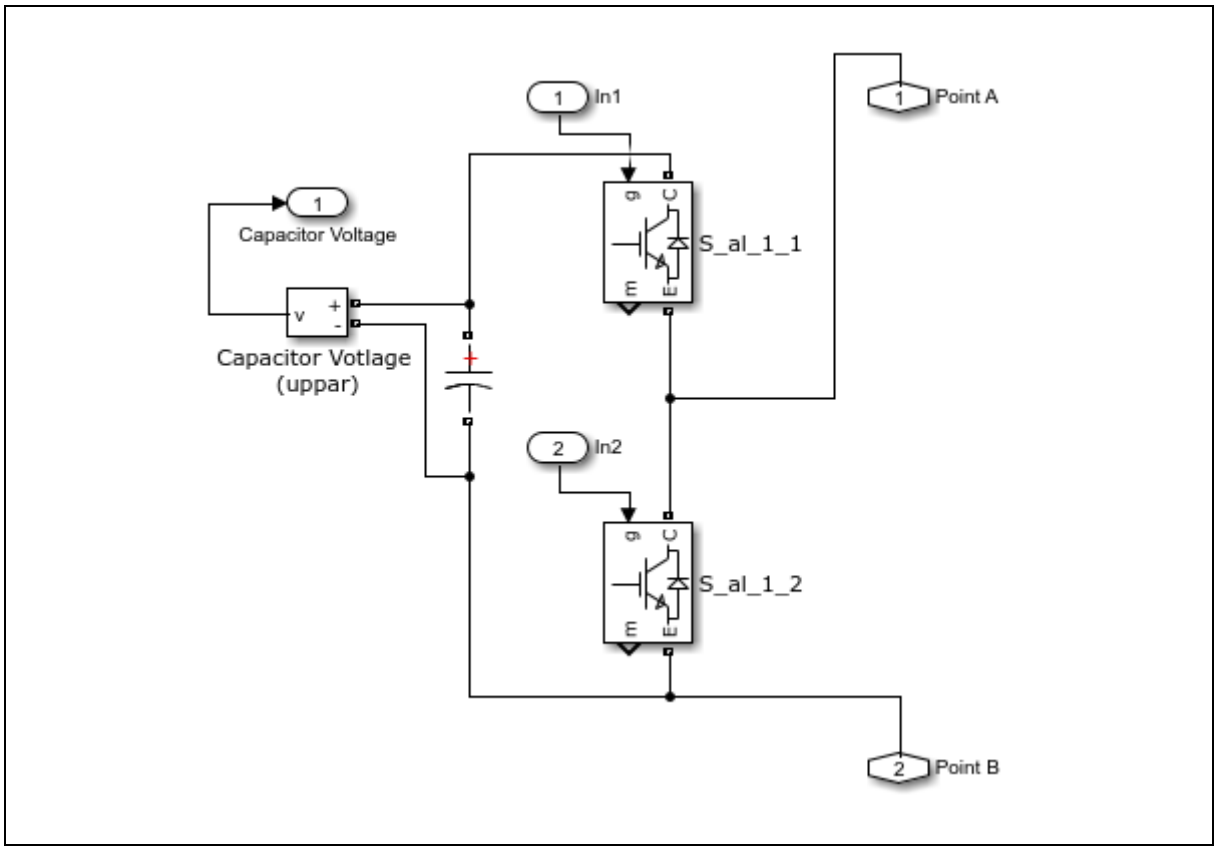


Figure A 4.2: Submodule implementation in Simulink

Appendix B: Summary of mathematical modeling

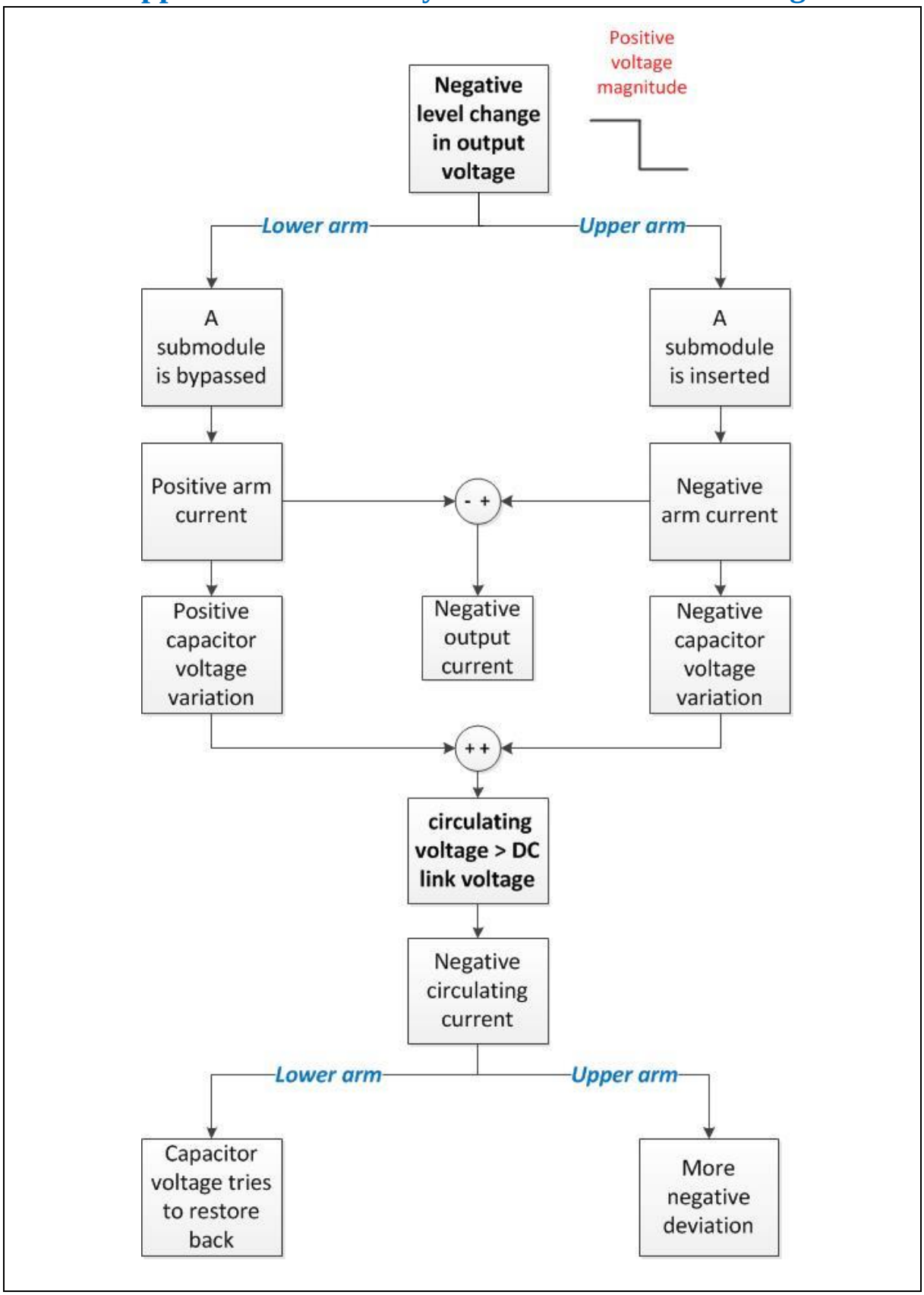


Figure B 1: Sequence of operation for case 2 (Negative level change for positive magnitude)

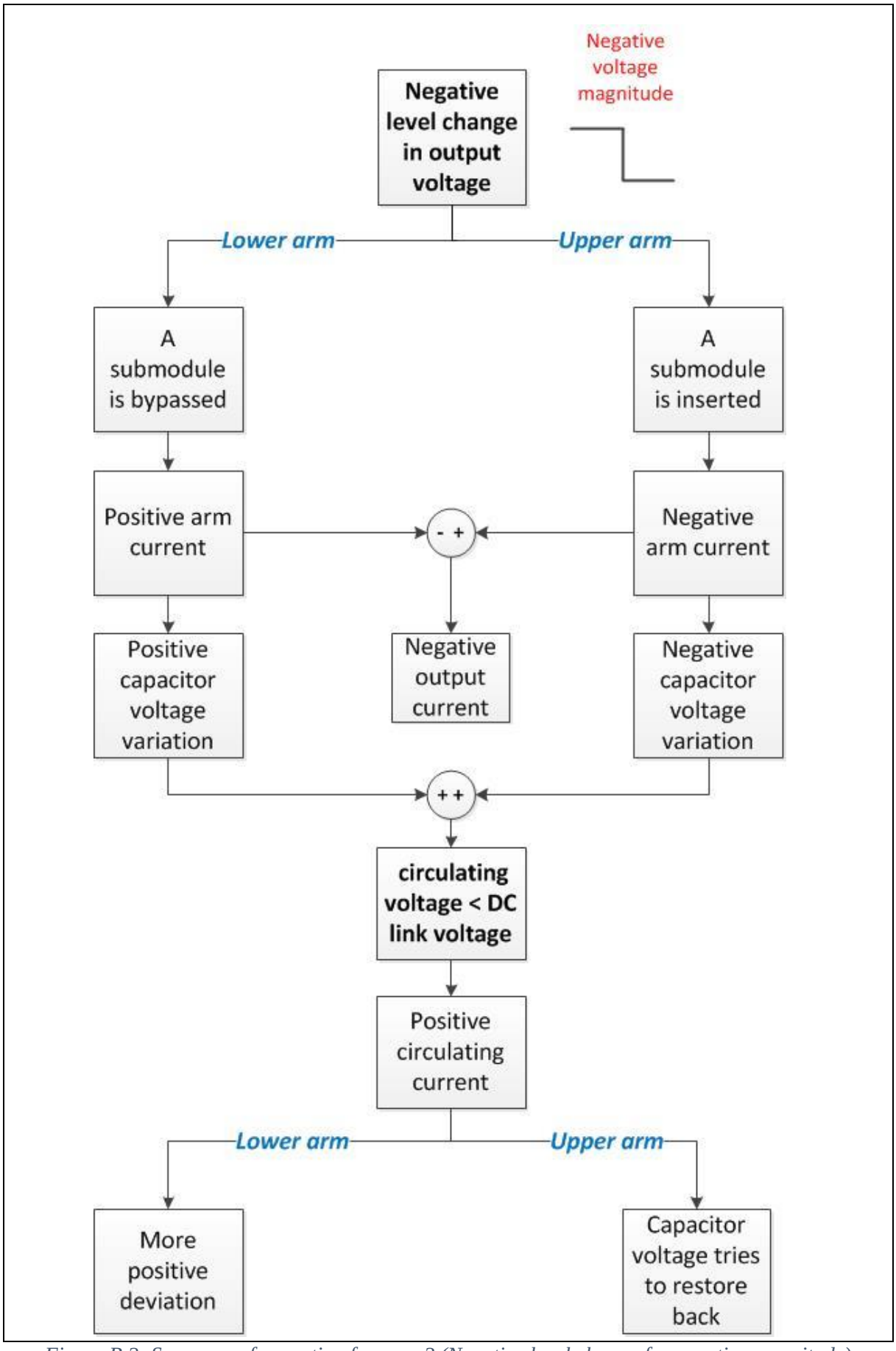


Figure B 2: Sequence of operation for case 3 (Negative level change for negative magnitude)

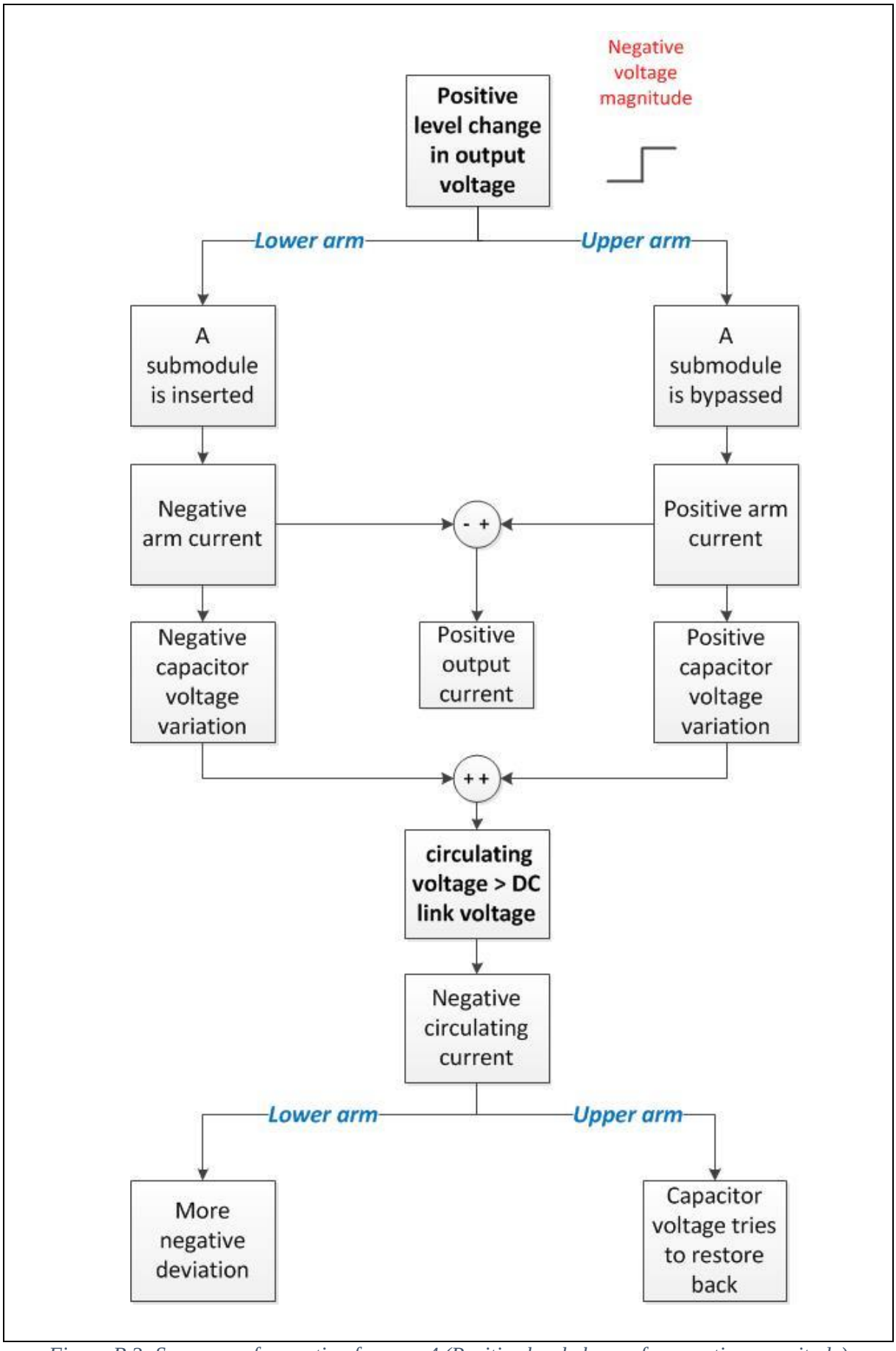


Figure B 3: Sequence of operation for case 4 (Positive level change for negative magnitude)

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