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Pinhole Defect Characterization and Fault Modeling for STT-MRAM Testing

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***Abstract*—The STT-MRAM manufacturing process involves not only traditional CMOS process steps, but also the integration of magnetic tunnel junction (MTJ) devices, the data-storing elements. This paper demonstrates a paradigm shift in fault modeling for STT-MRAMs by performing defect modeling and fault analysis for MTJ pinhole defects which are seen as a key type of STT-MRAM manufacturing defects. A Verilog-A compact model for defect-free MTJ devices is built and calibrated with electrical measurements on actual MTJ wafers. MTJs with a pinhole defect are extensively characterized, both during manufacturing test (t=0) and in the field (t>0), and the data is used to extend our defect-free MTJ compact model to include parameterized pinhole defects. The model is then used to perform single-cell static fault analysis and this shows not only what kind of faults can occur in an STT-MRAM, but also that the conventional fault modeling approach based on linear resistors cannot catch such behavior.**

I. Introduction

After years of downscaling, today's charge-based memories (e.g., SRAM, DRAM, and Flash) are facing major limitations such as increased leakage power and poor reliability [1]. This makes their further downscaling costly and impractical. Therefore, the semiconductor industry is seeking alternative memory technologies [2]. Among them, spin-transfer torque magnetic random access memory (STT-MRAM) is receiving extensive attention, as it features high density, nearly unlimited endurance, negligible leakage power, and CMOS compatibility [3]. Thus, many companies have been heavily investing in its commercialization. For example, Everspin Technologies announced the first STT-MRAM chip of 64Mb in 2012 [4]. Intel and Samsung also demonstrated their embedded STT-MRAMs in 2018 [5,6]. Providing sufficient outgoing product quality is essential for the commercialization of STT-MRAMs. This calls for effective, yet efficient test solutions.

Testing STT-MRAMs is still an emerging research topic. Azevedo et al. [7,8] injected resistive shorts and opens into a SPICE model of an MRAM cell and subsequently performed simulations to derive fault models. Su et al. [9] did intensive analysis of the excessive magnetic field during write operations and observed write disturbance faults; they validated those using chip measurements. Yoon et al. [10,11] have taken the fault modeling one step further by studying the impact of resistive defects while considering extreme process variation; they proposed a test algorithm and its built-in-self-test (BIST) implementation. Recently, Nair et al. [12] have reported detailed STT-MRAM fault analyses, based on injecting resistors into layout and netlist. Inspecting prior work reveals the following: (1) all published work assumes that defects in STT-MRAM devices can be modeled as *linear resistors*; however, none of these publications has validated this assumption; (2) there is a lack of measurements/characterization data of defective STT-MRAM cells; this is needed to accurately understand the physics of unique STT-MRAM defects and their electrical behavior, etc. It is worth noting that *accurate* fault modeling is a key enabler for high-quality and efficient test solutions, while inaccurate fault modeling may result in providing solutions for non-existing problems!

In recent work [13], we have shown *analytically* that using linear resistors to model STT-MRAM-specific defects is inaccurate. This paper follows up on [13] and confirms the above statement based on *silicon measurements*. In addition, we present a SPICE-compatible compact model for defect-free MTJ devices based on [14] which we calibrated using our measured silicon data. This model is then extended to cover defective MTJ devices as we show in this paper for pinhole defects, thereby enabling accurate fault analysis at the circuit level. Prior to that, a comprehensive characterization and analysis of MTJs with pinhole defects, both at t=0 and t>0, is performed to build a deep understanding of the defect. In summary, the contributions of this paper are as follows.

- Demonstrate using electrical measurements on actual MTJ devices that resistor-based modeling of MTJ defects is inaccurate.
- Improve and calibrate the Verilog-A compact model in [14] for defect-free MTJs based on measurement data.
- Characterize and analyze MTJs with pinhole defects both during manufacturing test (t=0) and in the field (t>0).
- Propose, calibrate, and validate a parameterized Verilog-A compact model for MTJs with a pinhole defect.
- Perform static fault analysis for 1T-1MTJ memory cells using our proposed pinhole defect model.

The rest of this paper is organized as follows. Section II provides a background on STT-MRAMs. Section III demonstrates the limitations of the conventional defect modeling approach. Section IV builds a calibrated Verilog-A compact model for defect-free MTJs. Section V presents characterization results of MTJs with pinhole defects. Section VI details the proposed pinhole-parameterized MTJ compact model. Sections VII shows how this model can be used for accurate fault modeling. Section VIII concludes this paper.

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II. Background

A. Working Principle of STT-MRAM

The *magnetic tunnel junction* (MTJ) is the core of STT-MRAM; it stores one-bit data in the form of binary magnetic configurations. As shown in Fig. 1(a), an MTJ device is composed of two CoFeB layers: a top layer called *free layer* (FL) and a bottom layer called *pinned layer* (PL), that sandwich a middle dielectric layer, usually an ultra-thin ($\sim$1 nm) MgO layer, called *tunnel barrier* (TB). Therefore, electrons moving from FL to PL or vice-verse have to tunnel through the MgO layer making the device akin to a tunneling resistor. The magnetization direction of the FL can be switched by applying a spin-polarized current flowing through the device, while that of the PL is strongly pinned to a certain direction (by an inner synthetic anti-ferromagnet) and cannot be switched. Therefore, the magnetization in the FL can be either parallel "P state" or anti-parallel "AP state" to that of the PL. Due to the tunneling magneto-resistance (TMR) effect [15], the MTJ's resistance is high in the AP state and low in the P state. The TMR ratio is defined by: $TMR{=}(R_{\rm AP}{-}R_{\rm P})/R_{\rm P}$, where $R_{\rm AP}$ and $R_{\rm P}$ are the resistances in the AP and P states, respectively. To evaluate the resistivity of MTJ devices, the *resistance-area* (RA) product is commonly used in the MRAM community, as it is independent of the device size.

Fig. 1(b) illustrates a bottom-pinned 1T-1MTJ memory cell and its corresponding write and read operations. The cell consists of an MTJ device and an NMOS selector. The NMOS gate is connected to a word line (WL) and the other two terminals are connected to a bit line (BL) and a source line (SL). The voltages above and below the three red arrows belonging to the BL and SL illustrate, under the assumption that the WL is active, the control of three operations: write "0", write "1", and read. For example, during a write "0" operation on a cell containing 1 (AP state), WL and BL are connected to $V_{\rm DD}$ and SL to ground, leading to a current $I_{\rm w0}$ flowing from BL to SL. If the current is larger than the critical switching current $I_{\rm c}$, the magnetization in the FL may, depending on the pulse width, switch to the other direction. It is worth noting that the actual switching time $t_{\rm w}$ is determined by the magnitude of the write current. The higher the write current over $I_{\rm c}$, the less time required for the magnetization in the FL to flip. During read operations, a read voltage $V_{\rm read}$ (significant smaller than $V_{\rm DD}$ to avoid read disturb) is applied; it leads to a read current ($I_{\rm rd}$) with the same direction as $I_{\rm w0}$ to sense the resistive state (AP or P) of the MTJ.

In summary, $R_{\rm P}$, $R_{\rm AP}$, $I_{\rm c}$, and $t_{\rm w}$ are four key electrical parameters determining the electrical behavior of MTJ devices.

B. Pinhole Defect Mechanism

The fabrication and integration process of MTJ devices is vulnerable to several defects [13]. A pinhole defect in the tunnel barrier is seen as one of the most important manufacturing defects that may take place during the multi-layer deposition [16–18]. In [16], Zhao et al. showed a transmission electron microscope (TEM) image of the cross-section of an MTJ device with a small pinhole in its MgO TB, as shown in Fig. 1(c). A pinhole defect can form due to unoptimized deposition processes [16]. This can cause the formation of metallic shorts in the MgO tunnel barrier, probably due to diffusion of Boron into the MgO barrier or other metallic impurities [18]. With a small pinhole filled with CoFeB material from the layer above, the tunneling current across the MgO barrier is shunted by a high-conductance path via the pinhole. As a result, it leads to a degradation of both RA and TMR parameters or even breakdown due to elevated Joule heating. Moreover, Oliver et al. [17] observed that pre-existing pinhole defects in the AlO_x-based barrier of an MTJ device grow in area over time because of Joule heating and/or an electric field across the pinhole circumference. Therefore, if even small pinhole defects are not detected during manufacturing tests ($t{=}0$), they might cause an early breakdown in the field ($t{>}0$).

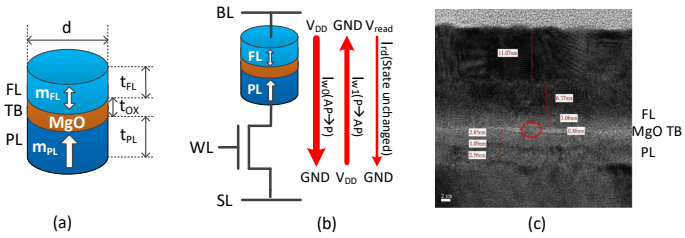


Fig. 1. (a) Simplified MTJ device organization, (b) 1T-1MTJ cell, and (c) Reprinted TEM image of a pinhole (in the red circle) in the MgO barrier [16].

III. Limitations of the Conventional Resistor-based Defect Modeling Approach

In the conventional defect-modeling approach, each defect in an MTJ device is assumed to manifest itself either as a resistor $R_{\rm sd}$ in series with or a resistor $R_{\rm pd}$ parallel to the MTJ device. To investigate the effect of this conventional resistor-based defect approach on the R-V hysteresis loop, we simulated an MTJ device for three cases: (1) defect-free case, (2) MTJ defect manifests itself as a series resistor $R_{\rm sd}{=}1\,{\rm k}\Omega$, and (3) MTJ defect manifests itself as a parallel resistor $R_{\rm pd}{=}10\,{\rm k}\Omega$. Fig. 2 compares the three cases, represented by green solid curve, blue dashed curve, and red dash-dot curve respectively. The figure shows that the R-V hysteresis loop enlarges for Case (2); the switching voltage $V_{\rm c}$ increases because there is a voltage division between the series resistor and the MTJ device. For Case (3), the R-V hysteresis loop moves downwards, as the overall resistance is pulled down. In this case, the switching voltage $V_{\rm c}$ across the device does not change, as the voltage over the MTJ device is not affected by the parallel resistor.

Fig. 3 presents the measured R-V hysteresis loops of four MTJ devices on the same wafer; the designed diameter is 60 nm, with a nominal $RA{=}4.5\,\Omega\cdot\mu{\rm m}^2$. The green curve (with the widest loop) represents a defect-free device, while the other three curves show defective devices with decreasing TMR and $R_{\rm P}$. Clearly the switching voltage of defective devices decreases depending on the defect size, compared to that of a good device. This trend is not captured by the injection of resistive defects, as Fig. 2 reveals. This is because

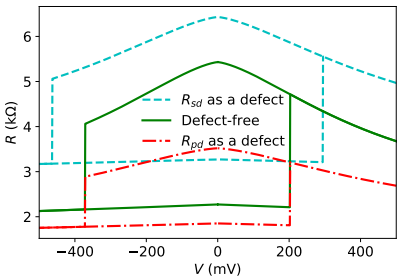


Fig. 2. Simulated R-V hysteresis loops.

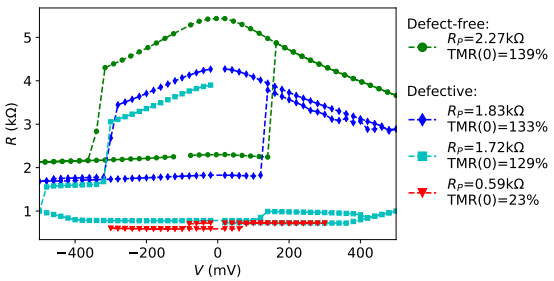


Fig. 3. Measured R-V hysteresis loops.

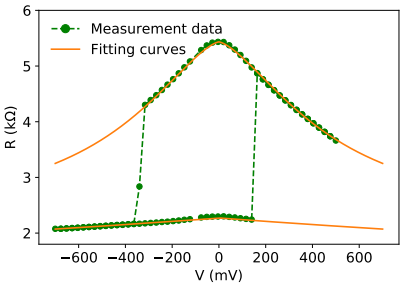


Fig. 4. Curve fitting of R_{P} and R_{AP}.

the resistor-based model fails to accurately incorporate the relationship between the four key electrical parameters of an MTJ device (i.e., R_{P}, R_{AP}, I_{c}, and t_{w}, as explained in Section II). Although the parallel resistor is qualified to model the decreasing trend of R_{P} and R_{AP}, the impact of defects on I_{c} and t_{w} is not captured. In order to capture the change of magnetic properties which are related to I_{c} and t_{w}, we need another method to accurately model MTJ-related defects.

In conclusion, linear resistors are unable to capture defect-induced changes in magnetic properties, which are as important as electrical ones for MTJ devices.

IV. Calibrated Compact Model for an MTJ Device

To accurately model defective MTJ devices, a good compact model for the defect-free MTJ device is required first; this is the topic of this section. The MTJ compact model outputs four electrical parameters: R_{P}, R_{AP}, I_{c}, and t_{w}. We first derive and calibrate the modeling results of R_{P}, R_{AP} at various bias voltages with measured R-V hysteresis data. Thereafter, we repeat the same thing for I_{c} and t_{w} by modeling and measuring the switching current for various pulse widths.

A. Bias Dependence of MTJ Resistance

We consider CoFeB/MgO/CoFeB MTJ devices [19] for our work. Despite this choice, our approach is generic and can be applied to any type of MTJ device.

The device tunneling conductance is bias-voltage dependent, as shown in Fig. 4 by the measured R-V hysteresis loop for a $\varnothing 60\,\mathrm{nm}$ sample device. The physical model in [20] shows that the resistance is mainly determined by the MgO barrier thickness and the interfacial effects between the barrier and neighboring CoFeB layers. We use two simplified Equations (1) and (2) from [21] to model R_{P} at varying bias voltage.

$$R_{\mathrm{P}}(V) = \frac{R_0}{1 + s \cdot |V|} \tag{1}$$

$$R_0 = \frac{t_{\mathrm{ox}}}{F \cdot \sqrt{\bar{\varphi}} \cdot A} \exp(\mathrm{coef} \cdot t_{\mathrm{ox}} \cdot \sqrt{\bar{\varphi}}) \tag{2}$$

where t_{ox} is the MgO barrier thickness, $\bar{\varphi}$ the potential barrier height of MgO, A the horizontal cross-section of the MTJ device. F, coef and s are fitting coefficients depending on the RA product as well as the material composition of the MTJ layers. TMR decreases with bias voltage; the relation is modeled with Equation (3) [21]:

$$TMR(V) = \frac{TMR(0)}{1 + \frac{V^2}{V_{\mathrm{h}}^2} + b \cdot V^{\frac{4}{3}}} \tag{3}$$

It is worth noting that we added a correction term (i.e., $b \cdot V^{\frac{4}{3}}$) in the denominator to get a better fitting result in comparison to the original equation in [21]. $TMR(0)$ is the TMR ratio at $0\,\mathrm{V}$, and V_{h} is the bias voltage when $TMR(V_{\mathrm{h}}) = 0.5\,TMR(0)$. Based on Equations (2-3), R_{AP} at certain bias voltage can be derived with Equation (4).

$$R_{\mathrm{AP}}(V) = R_0 \cdot (1 + TMR(V)) \tag{4}$$

The solid curves in Fig. 4 show our fitting results of R_{P} and R_{AP}, which match the measurement data.

B. Switching Current at Various Pulse Widths

Since the switching behavior of the MTJ state is intrinsically stochastic, we measured the switching voltage V_{c} in steps of $10\,\mathrm{mV}$ from 0% to 100% switching probability P_{sw} for a given pulse width. For example, we observed that V_{c} spans from $-0.7\,\mathrm{V}$ at P_{sw}=0% to $-0.9\,\mathrm{V}$ at P_{sw}=100% for the AP→P transition, at a pulse width of $12\,\mathrm{ns}$. Based on the measured V_{c} at various switching probabilities, we extracted V_{c} at P_{sw}=50% as the average switching voltage. Thereafter, we derived the switching current I_{w} based on the above-mentioned R-V fitting curves. Fig. 5 shows the derived I_{w} data for both P→AP and AP→P transitions at various pulse widths from $4\,\mathrm{ns}$ to $100\,\mathrm{ns}$.

The Landau-Lifshitz-Gilbert equation under the macrospin assumption is commonly used to model the switching dynamic of the magnetization in the FL [15]. Depending on the mechanism which dominates the switching event, the entire switching spectrum can be divided into two regimes: (1) precessional, (2) thermal activation regimes.

In the *precessional* regime, the STT effect is the main driving force flipping the magnetization in the FL with a pulse width less than $\sim 40\,\mathrm{ns}$. To switch the state, I_{w} has to be larger than the critical switching current I_{c} defined as [21]:

$$I_{\mathrm{c}} = 2\alpha \frac{\gamma e}{\mu_{\mathrm{B}} \cdot g} E_{\mathrm{B}} \tag{5}$$

$$E_{\mathrm{B}} = \frac{\mu_0 \cdot t_{\mathrm{FL}} \cdot M_{\mathrm{s}} \cdot A \cdot H_{\mathrm{k}}}{2} \tag{6}$$

$$g = \frac{\sqrt{TMR \cdot (TMR + 2)}}{2(TMR + 1)} \tag{7}$$

where α is the magnetic damping constant, γ the gyromagnetic ratio, e the elementary charge, μ_{B} the Bohr magneton, μ_0 the vacuum permeability, t_{FL} the thickness of the FL, M_{s} the saturation magnetization, H_{k} the magnetic anisotropy field, and g the spin polarization efficiency factor which can be

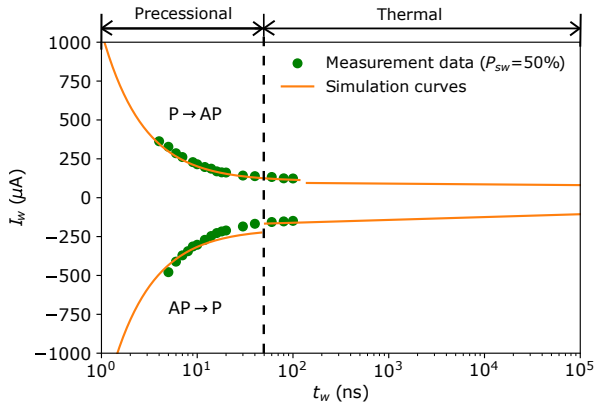


Fig. 5. Measured vs. simulated results of I_{w} at varying pulse width.

estimated by TMR. The switching time $t_{\mathrm{w}}^{\mathrm{pr}}$ in this regime can be estimated using Sun's model [22] as follows.

$$\frac{1}{t_{\mathrm{w}}^{\mathrm{pr}}} = \frac{2}{C + \ln(\frac{\pi^2 \Delta}{4})} \cdot \frac{\mu_{\mathrm{B}} P}{e \cdot m(1+P^2)} \cdot (I_{\mathrm{w}} - I_{\mathrm{c}}) \quad (8)$$

where $C{\approx}0.577$ is Euler's constant, $\Delta{=}\frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T}$ the thermal stability, P the spin polarization of the FL and the PL, and m the FL magnetization.

In the *thermal activation* regime where the pulse width increases above $40\,\mathrm{ns}$ (for our devices), a small current less than I_{c} is able to flip the magnetization due to the increased thermal fluctuation. The thermal fluctuation plays a main role in determining the switching behavior. In this regime, the Neel-Brown model can be used to describe the switching time $t_{\mathrm{w}}^{\mathrm{T}}$ [23]:

$$t_{\mathrm{w}}^{\mathrm{T}} = \tau_0 \exp(\Delta(1 - \frac{I_{\mathrm{w}}}{I_{\mathrm{c}}})) \quad (9)$$

Our model is based on combining the model of the precessional regime and the thermal activation regimes. Fig 5 shows clearly that by appropriately combining these regimes, we obtain simulation results which are in line with data measured on actual MTJ wafers. Note that the boundary between the two switching regimes is not strictly demarcated. It is significantly impacted by Joule heating. Given that R_{AP} is more than twice as large as R_{P}, the heat generated during an AP→P transition is much higher than the opposite direction. Therefore, the thermal activation regime of an AP→P transition shifts towards the left compared to a P→AP transition.

V. Electrical Characterization of MTJs with a Pinhole Defect

To develop an accurate compact model for the pinhole defect (presented in Section II.B), a deep understanding of the way such a defect manifest itself both at manufacturing stage ($t{=}0$) and in the field ($t{>}0$) is needed.

A. Pinhole Defect Characterization at $t{=}0$

To characterize the MTJ devices at $t{=}0$, we measured the R-H hysteresis loop to extract R_{P}, R_{AP}, and switching field H_{sw} of hundreds of virgin devices with diameter $60\,\mathrm{nm}$. During these measurements, ramped external fields were applied to the device under test; the magnetization in the FL flips when the external field reaches H_{sw}. After each field point, the resistive state was read out with a voltage of $20\,\mathrm{mV}$. As the measured devices were not subjected to any electrical operation before, we considered the measured parameters to be representatives for the MTJ state at $t{=}0$.

Fig. 6(a) shows the R-H hysteresis loops of four selected devices from the same wafer; each was measured ten times and the data was averaged to one loop. The widest green loop with $R_{\mathrm{P}}{=}2.2\,\mathrm{k\Omega}$ and $TMR{=}140.6\%$ represents a good device, while the other three loops represent three defective devices. It can be seen that the resistance and TMR of the three defective devices are significantly smaller than the good one; however, H_{sw} does not show the same trend. This indicates that the defects reside in the MgO barrier or at the MgO/CoFeB interface, whereas the FL is *undamaged*.

In addition to R-H hysteresis loops, we also measured R-V hysteresis loops. Fig. 3 shows the results of four other devices (one defect-free and three defective devices); obviously the loops of defective devices shrink, i.e., smaller R_{P}, TMR, and V_{c}. Note that the resistance of the cyan loop dives when the DC voltage reaches around $-500\,\mathrm{mV}$. This is because the existence of pinholes leads to an increase of current flow through them and in turn, a consequent increase in current-induced heating effects in the pinhole regions.

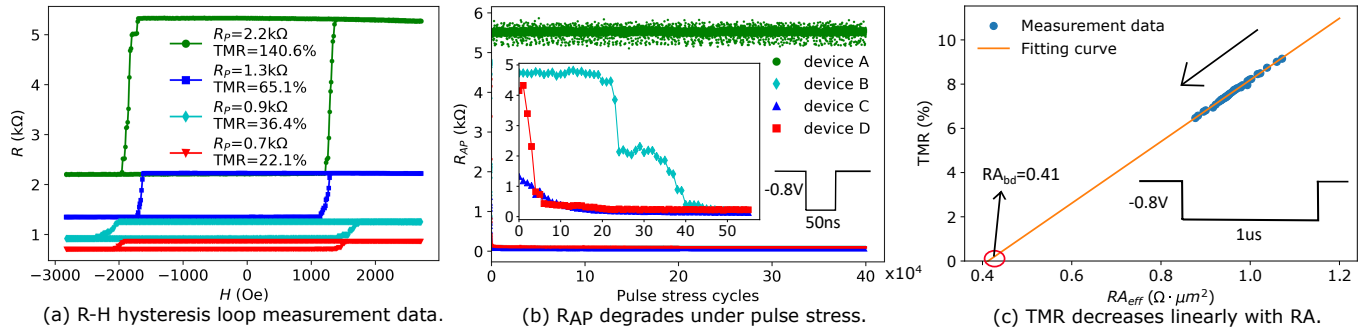
B. Pinhole Defect Characterization at $t{>}0$

To study how R_{P}, R_{AP}, RA, and TMR parameters of defective devices change over time ($t{>}0$), we stressed a large number of $\varnothing 60\,\mathrm{nm}$ MTJ devices with the following two test sequences.

First, we stressed hundreds of virgin MTJ devices with 400k cycles of P→AP switching (i.e., hammering of reset operations) to track how R_{AP} changes over time. During this test, pulse amplitude $V_{\mathrm{p}}{=}{-}0.8\,\mathrm{V}$ and pulse width $t_{\mathrm{p}}{=}50\,\mathrm{ns}$; note that the pulse width is more than twice the nominal value. After each pulse, we read back the MTJ resistance with a small ($V_{\mathrm{p}}{=}10\,\mathrm{mV}$) but long ($t_{\mathrm{p}}{=}0.7\,\mathrm{ms}$) pulse. We observed that all devices survived this stress test, except three devices broke down. Fig. 6(b) shows the results of four selected devices: one defect-free device A (green wide line on the top) and three devices which broke down within the first 40 cycles (denoted as B, C, D). This suggests that probably these three devices have pinhole defects in the MgO barrier, which caused the early breakdown due to the increased Joule heating.

Second, we selected a device with a suspected large pinhole ($R_{\mathrm{P}}{=}451\,\Omega$ and $TMR{=}9.1\%$) to investigate the impact on the effective RA and TMR over time. We increased the stress pulse width to $1\,\mu\mathrm{s}$ to speed up the degradation process, and measured R-H hysteresis loops after every 1k pulses. From the measured R-H hysteresis loop, we extracted the effective RA and TMR. Fig. 6(c) shows that the effective TMR decreases linearly with RA_{eff}. With a linear curve fitting, we obtained the breakdown resistance-area product $RA_{\mathrm{bd}}{=}0.41\,\Omega\cdot\mu\mathrm{m}^2$ by extrapolating the curve to the crossing point at x-axis.

In conclusion, small pinhole defects grow over time into larger pinholes which cause an early/extrinsic breakdown at



(a) R-H hysteresis loop measurement data. (b) R_{AP} degrades under pulse stress. (c) TMR decreases linearly with RA.

Fig. 6. Electrical characterization of MTJs with a pinhole defect.

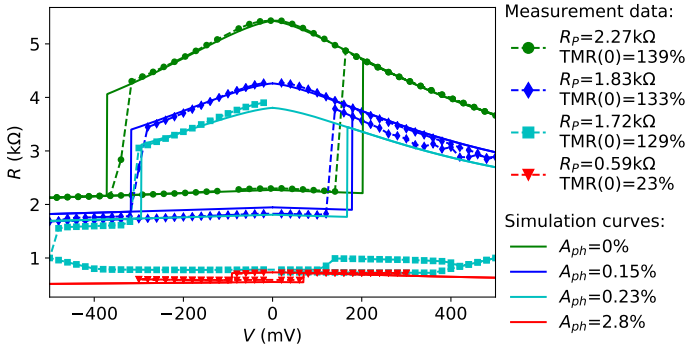


Fig. 7. Spectre simulation results vs. measurement data.

certain point. For devices with a small pinhole, the resistance and the TMR ratio drop dramatically with the applied pulses. As the pinhole grows up, their decrease rate becomes smaller.

VI. Parameterized and Calibrated Verilog-A Compact Model for MTJs with a Pinhole Defect

With the comprehensive characterization of pinhole defects in the previous section, we model the impact of pinhole defects on RA and TMR as follows [13].

$$RA_{\text{eff\_ph}}(A_{\text{ph}}) = \frac{A}{\frac{A(1-A_{\text{ph}})}{RA_{\text{df}}} + \frac{A \cdot A_{\text{ph}}}{RA_{\text{bd}}}} \tag{10}$$

$$TMR_{\text{eff\_ph}}(A_{\text{ph}}) = TMR_{\text{df}} \cdot \frac{RA_{\text{eff\_ph}}(A_{\text{ph}}) - RA_{\text{bd}}}{RA_{\text{df}} - RA_{\text{bd}}} \tag{11}$$

where $A_{\text{ph}} \in [0, 1]$ is the pinhole area normalized with respect to the cross-sectional area A of the MTJ device. RA_{df} and TMR_{df} are RA and TMR parameters of a defect-free MTJ (i.e., when A_{ph}=0), respectively. RA_{bd} is the resultant RA after breakdown. Then, we integrate Equations (10-11) into our defect-free MTJ compact model discussed Section IV, converting it into a Verilog-A compact model for MTJs with a pinhole defect. Fig. 7 shows the Spectre simulation results (solid lines) of R-V hysteresis loops with various A_{ph} values. It can be seen that the simulation results with our proposed defective MTJ model match the measured silicon data in terms of resistance and switching voltage. Note that our simulation results represent the green R-V loop (RA_{df}=4.52 $\Omega \cdot \mu\text{m}^2$, TMR_{df}=139%) with an injection of pinhole defects. However, the other three measured R-V hysteresis loops belong to three distinct defective devices, which have may different RA_{df} and TMR_{df} due to process variation.

VII. Fault Modeling of Pinhole Defects

We simulated a 2×2 1T-1MTJ memory array equipped with write drivers and precharge-based sense amplifiers. The predictive technology model (PTM) [24] for 45 nm transistors was adopted to build the memory array and peripheral circuits. We performed the simulation by injecting various pinhole defects and compared the results of our proposed model with that of the conventional resistive defect model.

A. Fault Space and Fault Analysis Methodology

To perform fault analysis, first we need to define the target fault space. For this work we limit ourselves to *single-cell static* faults [25]. A static fault is defined as a fault that can be sensitized by performing *at most* one operation. To describe such a fault in a systematic manner, we use the *fault primitive (FP)* notation [26]. An FP is defined as a deviation in the memory's logical behavior due to a list of performed memory operations called *sensitizing operation (S)*. An FP is denoted as a three-tuple $< S/F/R >$ where:

- S denotes the value/operation *sensitizing* the fault. $S \in \{0, 1, 0\text{w}0, 0\text{w}1, 1\text{w}0, 1\text{w}1, 0\text{r}0, 1\text{r}1\}$, where 0 (1) denotes a logic zero (one) value, 0w0 (1w1) denotes a write 0 (1) operation to a cell which contains a 0 (1), etc.
- F describes the value of the faulty cell; $F \in \{0, 1, U\}$. U denotes an undefined state. Note that it has been shown for defective STT-MRAM that when performing an operation, the cell may end in an undefined state, meaning that its device resistance value is not within the normal range of R_{P} or R_{AP} [17].
- R describes the output of a read operation (e.g., 0) in case S is a read operation. $R \in \{0, 1, ?, -\}$ where ? denotes a random read value (e.g., sensing current is very close to sense amplifier reference current), and "–" denotes that R is not applicable when S is a write operation.

Given the above, the *entire space* for single-cell faults can be defined; it can be easily derived that this consists of 28 FPs.

Next, the fault analysis of the 28 FPs is defined and performed for two cases: (1) using resistor-based defect model and (2) using our pinhole compact model. For the resistor-based defect model, we considered two types; a series resistor after or a parallel resistor parallel over the MTJ device. For both cases, the resistance is swept from 10^0 to 10^9 Ω using 45 steps which are equally distributed on a logarithmic scale. The

TABLE I. SINGLE-CELL STATIC FAULT MODELING RESULTS.

Defect Model	Value	Sensitized Fault Primitive
Series resistor R_{sd}	$0-310\,\Omega$	Undetectable
	$310-3.1\,\mathrm{k}\Omega$	IRF0=<0r0/0/1>
	$3.1\,\mathrm{k}-\infty\,\Omega$	IRF0=<0r0/0/1>, TF0=<0w1/0/−>, TF1=<1w0/1/−>
Parallel resistor R_{pd}	$0-1.1\,\mathrm{k}\Omega$	IRF1=<1r1/1/0> TF0=<0w1/0/−>, TF1=<1w0/1/−>
	$1.1\,\mathrm{k}-3.1\,\mathrm{k}\Omega$	IRF1=<1r1/1/0>, TF1=<1w0/1/−>
	$3.1\,\mathrm{k}-\infty\,\Omega$	Undetectable
Pinhole area A_{ph}	0-0.11%	Undetectable
	0.12-0.59%	USF1=<1/U/−>, URF1=<1r1/U/?>, UWDF1=<1w1/U/−>, UTF0=<0w1/U/−>
	0.6-100%	SF1=<1/0/−>, RDF1=<1r1/0/0>, WDF1=<1w1/0/−>, TF0=<0w1/0/−>

defect size for our pinhole compact model is swept between 0% and 100% of the MTJ tunnel barrier area. We simulated all sensing operations S and inspected the cell value to derive F as well as the value of R in case S is a read operation.

B. Simulation Results

Table I presents the simulation results of the single-cell static fault analysis; it gives the sensitized FPs and associated defect models with certain values. Note that only a subset of the 28 possible FPs are included in the table, viz. the FPs that show faulty behavior during our fault analysis simulations.

Simulation results with our pinhole model suggest that the bigger the pinhole, the larger its fault effect, and hence the easier to detect it. Sufficiently large pinholes (A_{ph}>0.6%) make R_{AP} fall into the resistance range of logic 0 state, thereby leading to static faults such as SF1 and WDF1. A small pinhole ($A_{\mathrm{ph}}\in$[0.12%,0.59%]) transforms an expected 1 into a U state, causing USF1, URF1, etc. Thus, a single read operation does not guarantee its detection, since reading a U state may return a random value. If the pinhole is even smaller (A_{ph}<0.11%), no fault primitive can be sensitized by a single operation. However, as shown in Fig. 6(b), subsequent write operations turn a small pinhole defect into a larger one, and hence pose a reliability risk. One way to test for this is to subject the STT-MRAM to lengthy write series, which is prohibitively expensive for high-volume testing.

Simulation results with the conventional approach results in some FPs (e.g., TF1 and IRF1) which do not occur in the simulation with our proposed pinhole defect model. This suggests that test algorithms developed with the conventional resistor-based defect modeling approach not only *cannot* guarantee the detection of pinhole defects, but also may waste test time and resources as they target non-existing faults.

VIII. CONCLUSION

This paper has demonstrated a paradigm shift in fault modeling for STT-MRAMs. It has been shown based on real measurements and circuit simulations using calibrated models that the conventional fault modeling approach is not only unable to accurately describe the faulty behavior of STT-MRAMs (such as WDF1 and UTF0 found with our approach), but it also even provides wrong fault models which are not applicable to STT-MRAMs; meaning that it cannot lead to a high-quality test solution. This clearly sets up a turning point in fault modeling for STT-MRAMs. As pinhole defects are considered as one of the most important STT-MRAM manufacturing defects, this paper presents a calibrated model for pinhole defects based on silicon data as well as the resultant fault effects. Other MTJ defects should also be modeled in the same manner as we did for pinhole defects in order to enable accurate fault modeling and development of high-quality tests for STT-MRAMs.

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