A 16-Channel CMOS Reconfigurable Recording Unit for Simultaneous In-Vitro Microelectrode Array (MEA) and Current-Clamp (CC) Measurements

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Preface

It was one of the happiest days of my life when I had been accepted by TU Delft as a master student, and now, I can literally see the reason of feeling such a happiness. It has been a long, yet enriching road for me, and I have met a lot of inspiring people along the way. First of all, I would like to thank Virgilio Valente not only for his continuous guidance on the project, but also for his kind and supportive approach all the time. Without his continuous help, this thesis would not have happened. I cannot express my gratitude enough to him for the last 2 years.

I also would like to express my sincere appreciation to Prof. Wouter Serdijn for participating in the committee, and being such a great head of Section: Bioelectronics. I believe that all of us feels like belonging to our section, and you make this happen.

I would like to thank all members of Bioelectronics section for their kind personalities, and joyful conversations during coffee breaks. I cannot name all of them here, since we are very big group fortunately, but I have to express my appreciation from bottom of my heart to Ronaldo Ponte for his great support in the project, and his open-mind and kind personality. And, thank you very much to Brian and Shengjie to make our office fun and comfortable place.

Last but not least for sure, I would like to express my deepest gratitude to my dear friends. Thank you very much, Andrea, Ata, Chris, Erdi, Hazal, Oguz and Sevilay. Even in the toughest days, I did not feel like I am doing this alone. You know that it means world to me.

I want to finish my acknowledgement with the life-altering quote for me:

The credit belongs to the woman who is actually in the arena, whose face is marred by dust and sweat and blood.

If she fails, at least fails while daring greatly, so that her place shall never be with those cold and timid souls who neither know victory nor defeat.

Asli Yelkenci
Delft, October 2020

Abstract

In-vitro cell culturing technique is widely used in many branches of science such as in neuroscience and cardiology to investigate the dynamics of large population of cells. Cultured cells can be studied by means of two fundamental recording techniques that are intracellular and extracellular recordings. Patch-clamp technique is the gold standard of high-fidelity action potentials (APs) and synaptic potentials of an individual cell. However, patch-clamp method suffers from very poor scalability. Approximately only 10 cells can be studied per day by experienced personnel working on a bulky and expensive setup. Microelectrode arrays (MEAs) have been proposed to perform multi-site and high-throughput extracellular recordings. Although MEA technology is utilized to understand network dynamics of large population of cells, MEA electrodes lack intracellular access to cell membrane which results in highly-attenuated potentials. Thus, MEA electrodes are only capable of recording action potentials (APs), and they are completely blind to synaptic events. Recent studies report that APs and synaptic potentials of an individual cell play a role in an increase in network activities as well as extracellular field potentials can induce a single-cell activity. Concurrent high throughput patch-clamp and MEA measurements are needed to gain insight into correlation between single-cell and network dynamics. The thesis project presents the design of 16-channel dual-mode recording unit for simultaneous measurements of intracellular and extracellular activities. The recording channel consists of capacitively-coupled instrumentation amplifier (CCIA) to reject DC offset of electrodes and unary-weighted current-steering DAC for stimulation of cells. The ratio of CCIA capacitors defines the gain of the amplifier, and the capacitors with MOS-based pseudo-resistors determine the low-frequency cut-off frequency. Single-stage single-ended 5T operational transconductance amplifier (OTA) is implemented in the core of CCIA. The unit current source of 4-bit thermometer-coded DAC copies 100 pA current from the reference and is localized in each channel. The injected current is increased by activating the adjacent unit current sources, and total current can reach to 1.6 nA. The reconfigurable recording channel has been designed in standard 0.18 μm CMOS technology. By post-layout simulations, the gain of the amplifier equals to 23.5 dB. The input-referred noise of the channel is 8.1 μV_{rms} in the frequency band ranging from 1.05 Hz to 10 kHz with NEF of 6.2. The power consumption of each individual recording unit is 7.18 μW. Each reconfigurable channel occupies 0.021 mm^2 area on a die. This thesis projects integrates dual-mode functionality which opens a door to high-throughput multi-site intracellular and extracellular recordings for further understanding of correlation between single-cell activity and network dynamics of cells.

Contents

1 Introduction

In-vitro cell culturing is an essential method to study large populations of cells [1]. In-vitro cell modelling systems are widely used in neuroscience to understand dynamics of neural networks [2]. For example, the morphology of the cells and different aspects of brain-functioning are enabled to be studied with in-vitro cell cultures [1] . Also, impact of added chemicals such as drugs or toxicants to cells can be investigated by means of in-vitro cell culturing technique [1]-[3]. The investigation of cultured cells can be done by 2 fundamentally different techniques: 1) intracellular recordings, and 2) extracellular recordings [4].

Intracellular recordings of electrogenic cells such as heart cells and neurons, carry tremendous importance to understand how a human body functions. The patch clamp technique is widely used in order to perform measurements of intracellular electrical activity of electrogenic cells. Fig. 1.1 shows the representation of how patch clamp technique is applied on cultured cells. The patch clamp method was first introduced by Neher and Sakmann in 1970s [5], and it is still considered the gold standard to perform intracellular recordings [6],[7],[8] [9]. The patch electrode is brought in close contact with the cell membrane, and a tight seal is formed between electrode and cell. The resistance between electrode and cell must be in the range of gigaohms to guarantee high-fidelity recording [10]. The resistance in gigaohms range provides good isolation of cell membrane. Also, leakage current is highly reduced by means of good coupling between cell and electrode. Thus, the resulting intracellular recording provides single-channel activities such as action potentials (APs), subhthreshold post-synaptic potentials (PSPs), and membrane oscillations [11] in real-time and with ultra-high resolution (in the order of 1 pA)[12].

An AP is a rapid voltage change in cell membrane from -70 mV to 30 mV because of changes of ion concentrations (Na^+, K^+) causing depolarization and hyperpolarization across the membrane. This 100 mV change in cell membrane because of an AP can be recorded with by patch-clamping (see Fig. 1.2). Moreover, subthreshold events such as excitatory and inhibitory PSPs are only accessible when cells are examined intracellularly. Excitatory and inhibitory PSPs play an important role in cell electrophysiology. For example, a neuron only fires when its membrane exceeds a certain threshold voltage (around -50 mV). Excitatory PSPs increase the likelihood of a neuron to generate APs since excitatory PSPs contribute depolarizing of the cells, i.e. increasing the cell membrane voltage (making it less negative voltage).

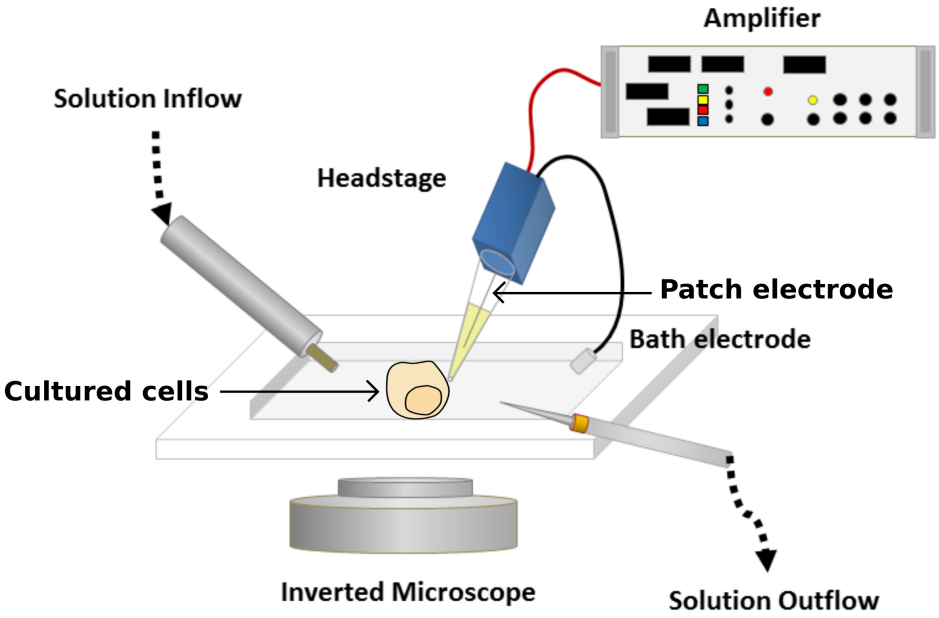


Figure 1.1: Representation of how patch clamp experiment is implemented (Adapted from [13].

On the contrary, inhibitory PSPs cause hyperpolarization that results in more negative membrane voltages. As a consequence of a decrease in membrane voltage, the neuron becomes less likely to fire an AP [14]. Excitatory and inhibitory PSPs with APs are highlighted in Fig. 1.2 [15].

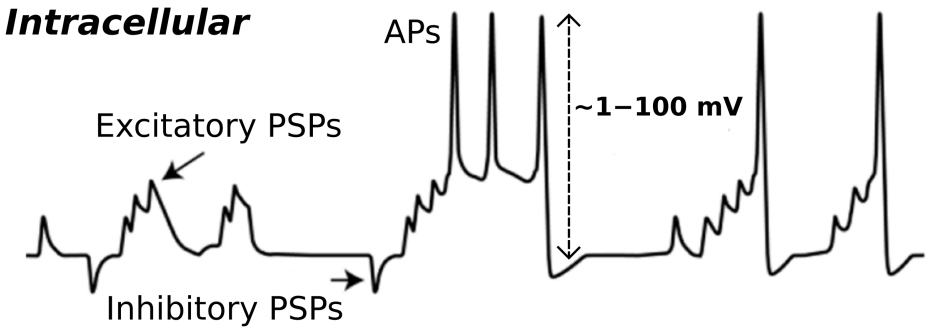


Figure 1.2: Intracellular recordings obtained by patch clamping (Adapted from [15])

In addition, the patch clamp method enables simultaneous voltage- or current-clamp stimulation of the cells. In current-clamp experiment, a known current (I_{inj}) is applied to the cell through the patch pipette inside electrolyte solution (see Fig 1.3). The resulting membrane voltage (V_{memb}) is measured by means of an amplifier which is connected to the pipette. The current-clamp technique is used to understand how the cell responds in voltages (such as APs) to a current stimuli. The voltage-clamp experiment is performed by applying a known voltage (V_{clamp}) to the membrane, and the current flowing through the membrane (I_{memb}) is measured. By means of voltage-clamp experiment, concentration of the voltage-sensitive

ion channels can be determined. These results are very useful for pharmaceutical applications such as drug discovery [16].

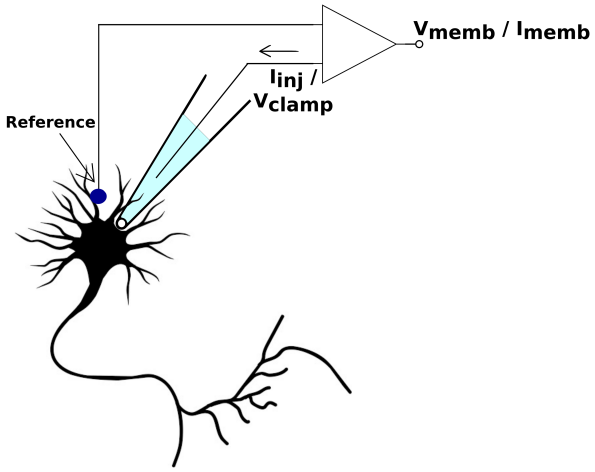


Figure 1.3: A neuron and patch pipette filled with electrolyte solution and an electrode connected to an amplifier. (Picture of neuron is taken from [17])

Although patch clamp technique offers nonesuch information about excitable cells and how they function, it suffers from considerably poor scalability. It has been reported that only 12 patch neuron recordings have been executed in parallel so far [18]. In addition, skilful personnel have to be trained to perform patch clamp experiments on a bothersome work station which mainly contains micromanipulators, optical microscope on a vibration-free table and a Faraday cage [6]. Fig. 1.4 shows a patch clamp work station which contains aforementioned tools [19].

Microelectrode array (MEA) technology has been proposed as an alternative cell study technique in 1972 [20] for the first time as passive planar-type electrodes. Since then, the technology is being used for in-vitro extracellular recordings of electrical activities of cultured excitable cells [21–27]. Planar MEA electrodes are usually fabricated on a glass wafer, and they are usually made of nontoxic metals such as gold (Au), iridium (Ir), platinum (Pt) or titanium nitride (TiN)[28]. They are relatively easy-to-fabricate because they use conventional photolithography techniques to pattern the electrodes on a silicon wafer [15]. An example of planar-MEA electrodes, and recorded signals from cultured neurons by means of metal electrodes are given in Fig. 1.5.

The extracellular recording by means of planar MEA electrodes are done in a non-invasive manner in contrast to patch-clamping. Therefore, long-term measurements are enabled with MEA technology. Moreover, multi-site recording is possible when MEA electrodes are used for recording which opens a door to have better understanding on network dynamics [4]. Also, MEA technology provides higher throughput than patch-clamping technique, since 60 electrodes can be easily fabricated on silicon wafer. However, because of a need to interconnect each passive electrode to the pads of a wafer, there is a certain limit of number of electrodes that can be integrated on silicon [29]. Also, MEA electrodes are completely blind to synaptic events shown in Fig. 1.2 [15]. Planar-MEA electrodes are only capable of recording APs as spikes (see Fig. 1.5). As it can be seen from Fig. 1.5, the recorded AP signals are in around

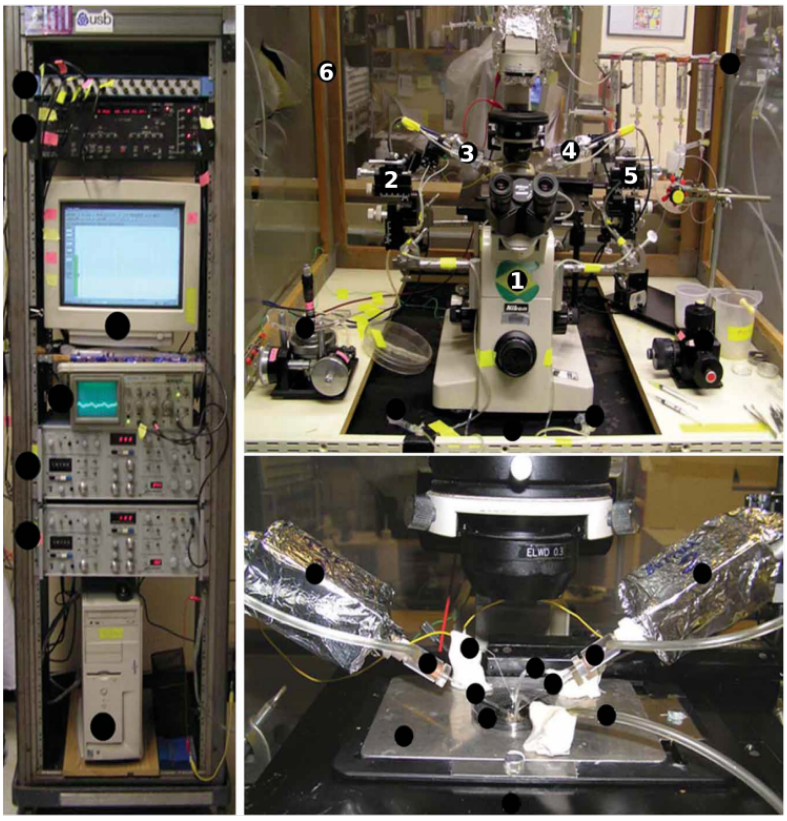


Figure 1.4: A patch clamp work station. (1) Inverted microscope. 2-5) Micromanipulators. (6) Faraday cage. Adapted from [19]

100 μV range in amplitude. Table 1.1 summarizes the amplitude and frequency ranges of extracellular and intracellular activities occurring within a neuron [14, 30].

3D micro- or nano-electrode arrays were introduced for intracellular recordings with high-spatial resolution [11, 31–34]. Some of them, e.g. gold mushroom-shaped microelectrodes provides in-cell recordings of subthreshold and APs from single-neuron (see Fig. 1.6a.) However, an external circuitry was used to record the signals [11]. This makes the 3D-MEA system dependant on the performance of external components that are not designated and optimized for the electrodes. Vertical nanowire electrode arrays (VNEAs) were proposed as a scalable platform for intracellular recording (see Fig. 1.6b.)[34]. However, subthreshold events could not be recorded by VNEAs until the recording electronics with current- and voltage-clamp capability are integrated on the same platform with the electrodes [35]. The reason can be

Table 1.1

Amplitude and Frequency Summary Table of Electrical Activities of Cells			
Features	**Extracellular**	**Subthreshold**	**APs**
Amplitude	10-1000 μV	1-4 mV	1-100 mV
Frequency	0.1 Hz- 10 kHz	300 Hz - 10 kHz	300 Hz - 10 kHz

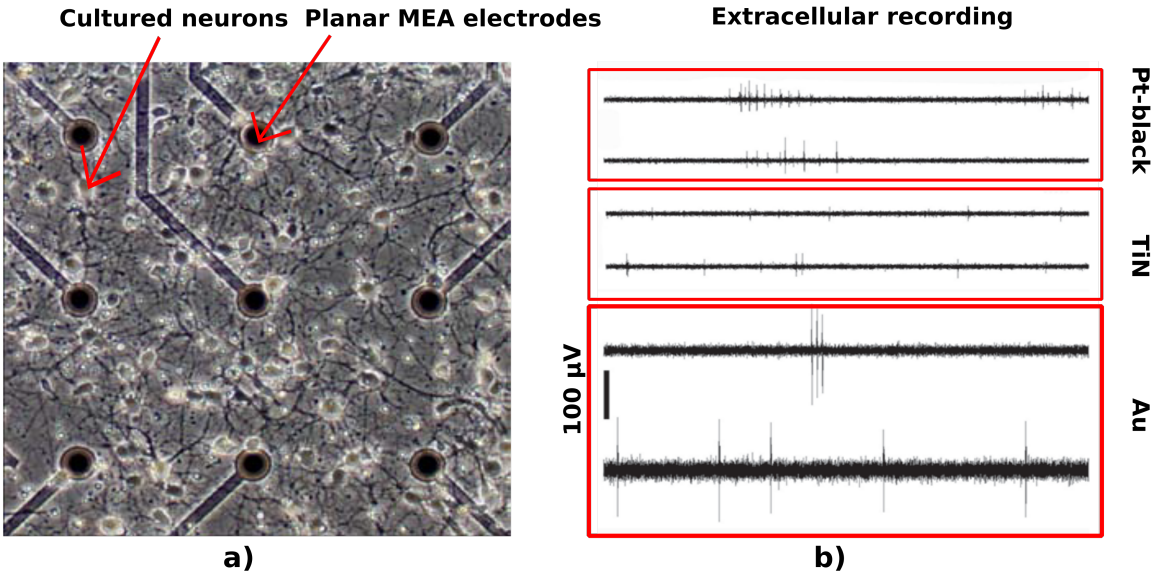


Figure 1.5: An example of planar MEA electrodes and extracellular recordings. a) Planar-type MEA electrodes. b) Extracellular recordings of cultured neurons from Pt-black, TiN, and Au electrodes. (Taken from [2])

explained by the intrinsic high impedance of such small electrodes lowers the signal-to-noise ratio (SNR). Nanotube field-effect transistors (nano-FETs) are also offered to provide intracellular access to cells ((see Fig. 1.6c.)[31]. A considerably high force (> 1 nN) had to be applied to nano-FETs to penetrate cell membrane. However, this force caused cell membrane to be compressed, and only APs were recorded by means of nano-FETs. In addition to not achieving high-resolution in recording, some of 3D-MEAs also suffer from complex microfabrication steps such as focused ion beam (FIB) deposition or electron beam lithography which make them hard-to-scale [15].

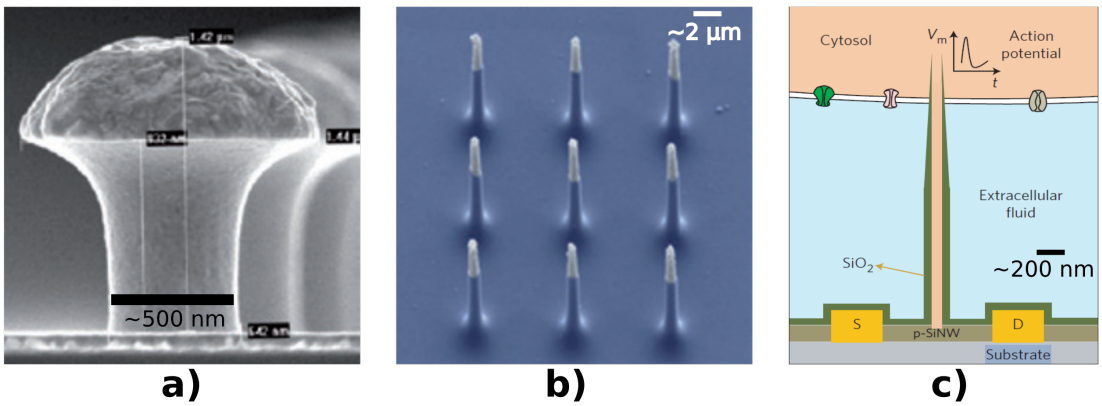


Figure 1.6: 3D-MEA electrode examples a) Gold mushroom-shaped MEAs [11] b) Vertical nanowire arrays (VNEAs) [34]. c) Intracellular nanotube field-effect transistor (FET) (Taken from [31])

Table 1.2

Table of Performance Comparison State-of-the-Art in Patch-Clamp					
Parameters	**Units**	**Multiclamp 700B [38]**	**MWSCAS, 2011 [16]**	**JNP, 2014 [36]**	**Nature El., 2019 [37]**
Technology	–	N/A	0.5 μm	0.35 μm	0.18 μm
Supply	V	N/A	3.3 V	N/A	3.3
Die size	mm × mm	N/A	4 × 8	4.7 × 3	3.23 × 2.73
No. of channel	–	N/A	4	1	1
CC Gain	V/V	50 MΩ - 5 GΩ	1	4	1
Injected current range	A	a few p - 200 n	less than 1 n	-5 p - 128 n	100 p_{pp}
VC (TIA) Gain	Ω	50 M - 50 G	49 k - 100 M	Nonlinear	0 - 225 M
Input-referred voltage noise	μV_{rms}	N/A	150	8.2	20
Power	mW	30000	30	N/A	7

1.1. State-of-the-Art in Patch Clamp and MEA Technologies

The state-of-the-art in patch clamp technology offers integrated circuit patch amplifier with both current- and voltage-clamp capability [16, 36, 37] to mitigate the problems in conventional bulky, expensive and non-scalable bench-top systems [38].

The first fully-integrated patch clamp amplifier with current-clamp capability was introduced by Goldstein et.al. [16]. The operation mode of the channel can be changed via digital control logic. The recording channel is in transimpedance amplifier (TIA) configuration when voltage-clamp modality is chosen. The channel is configured to a unity gain buffer when current-clamp mode is active. Although the channel is shared and uniquely configured for two different modalities, the channel occupies large areas on silicon with only 4 channels integrated on 4 mm × 8 mm die area. One of the reasons of large area occupation can be explained as using large resistances in the design. Besides the TIA and large resistances, there are compensation circuits to eliminate the non-linearities rising from the electrodes.

The second study example of a CMOS amplifier with both clamp capabilities is offered by Harrison et.al.[36]. Particularly in this study, nonlinear feedback elements (diodes) are used to avoid from the need of using large value resistances. However, since the nonlinear circuit elements are prone to process and temperature variations in manufacturing, additional calibration circuits had to be used.

Another example of CMOS amplifier for both patch clamping method was introduced by Shekar et. al.[37]. For current-clamp measurements, a unity gain buffer is used, whereas a TIA with resistive feedback is implemented as a separate block in the design. Since the IC still needs to be used with conventional patch pipettes, it can only be used for single-channel measurements. Fig. 1.7 shows the neural recording setup and the micrograph of offered amplifier. The die size is 3.23 mm × 2.73 mm. The resistance in the feedback of TIA ranges from 0-225MΩ. The summary comparison table of CMOS amplifier in patch-clamping and one of the bench-top system is given in Table 1.2.

Complementary-Metal-Oxide-Semiconductor (CMOS)-based MEAs are offered to overcome the issue of poor scalability of passive MEA electrodes and millimetre-sized CMOS patch-clamp amplifiers. Integrating 10000's of electrodes and recording electronics together

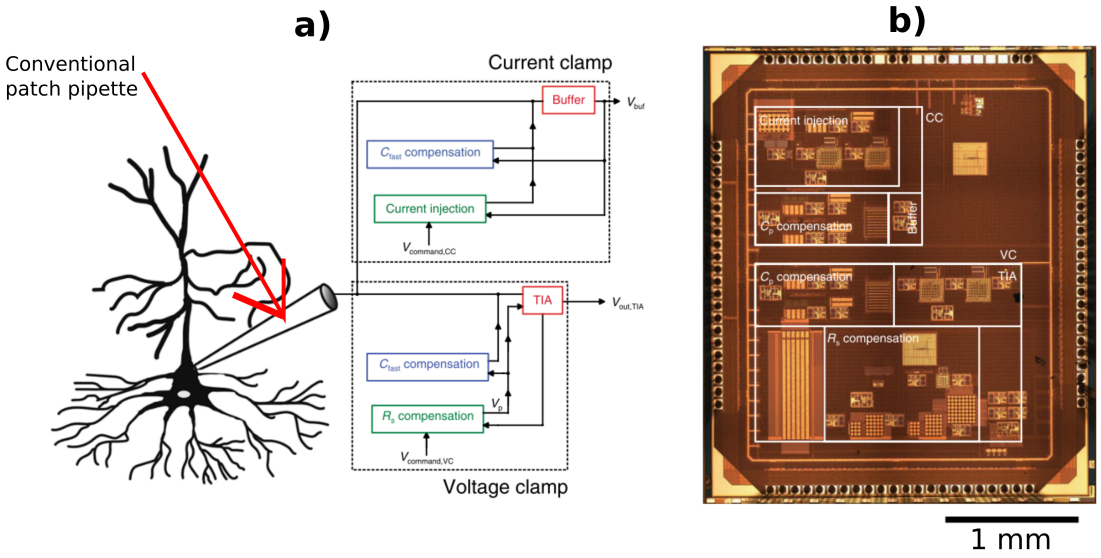


Figure 1.7: a) The setup for neural recording either in voltage- or current-clamp mode b) Micrograph of the amplifier (Taken from [37])

Table 1.3

Table of Performance Comparison State-of-the-Art in MEA Technologies					
Parameters	**Units**	**Lab on a Chip, 2009 [26]**	**JSSC, 2017 [41]**	**JSSC, 2018 [27]**	**Nature, 2020 [35]**
Supply	V	5/3.3	3.3 V	N/A	N/A
Technology	–	0.5 μm	0.18 μm	0.13 μm	0.18 μm
No. of. Electrodes	–	4096	59760	16384	4096
No. of channels	–	N/A	2048	1024	4096
Gain	dB	29.5-30.8	29.5-79.9	6-69.5	29.5-48.8
Bandwith	Hz	10 k	1 - 10 k	0.5 - 10 k	<1 - 30 k
Injected current range	N/A	N/A	N/A	N/A	±15 p
Input-referred voltage noise	μV_{rms}	13.3	5.4	12	23
Power	mW	132	86	95	1250

has been made possible on CMOS-Based MEAs [27, 39–41]. Therefore, CMOS-MEAs offer better performance than passive MEA electrodes on multi-site extracellular recordings from large populations of cells. This feature enables studying the network activities to understand synchronized activity and properties of very large number of cells. However, since CMOS MEAs record the signals in extracellular manner as it has done in passive MEAs, the signals that they can only capture are APs, they are highly attenuated (to around 100 μVs) [42]. The illustration of multi-functional CMOS-MEA with 59760 electrodes is given in Fig. 1.8a [41]. The recorded signals from rat cortical neurons are shown as averaged negative peak amplitudes and as APs around 100 μVs in Fig. 1.8b-c, respectively. It can be also seen that CMOS-MEAs cannot detect critical excitatory/inhibitory PSPs as it has been mentioned in Chapter 1.

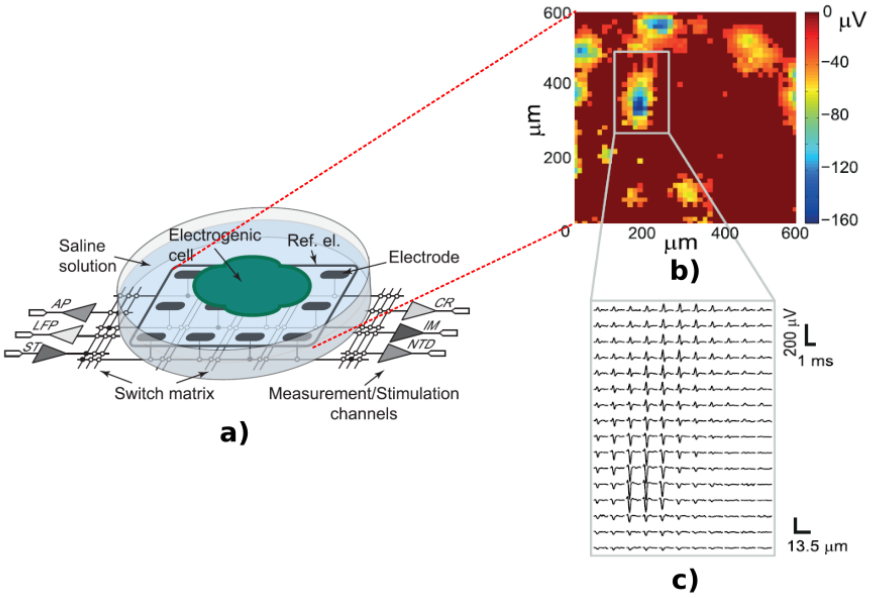


Figure 1.8: a) Illustration of Multi-functional MEA with 59760 electrodes b) Averaged negative peak amplitudes recorded from rat cortical neurons c) APs recorded by means of CMOS-MEAs. (Taken from [41])

1.2. Problem Statement

The extracellular field potentials are a combination of all ionic changes ranging from the slowest oscillations to APs. All ionic currents in cell membrane yields a contribution as intracellular and as extracellular activity. The amplitude and frequency of extracellular field potentials are dependant on multiple variations of multiple single current sources. For example, the distance from a current source play a role in magnitude of an extracellular potential. If the distance from a current source increases, extracellular potential amplitude decreases. Another important aspect of single current sources contributing extracellular potentials is the synchronicity of the sources. Overlapped synaptic potentials are the main contributors of extracellular current flow [43].

Table 1.4

Qualitative Comparison of Patch-Clamp, MEA, 3D MEAs, CMOS-MEA, and Proposed Platform					
Features	**Patch-Clamp**	**MEAs**	**3D MEAs**	**CMOS-MEAs**	**Proposed Platform**
Intracellular access	Yes	No	Yes	No	Yes
Network activity	No	Yes	Yes	Yes	Yes
High throughput	No	Yes	Yes	Yes	Yes
Scalability	No	Yes	No	Yes	Yes
Cost-effective	No	Yes	No	Yes	Yes

A simultaneous recording example of local field potentials (LFPs) from surface and deep regions of pyramidal neuron, and intracellular recordings is given in Fig. 1.9. In Fig. 1.9, intracellular activity in the deep regions of pyramidal neuron also reflects as synchronous activity in LFPs. In addition to that, Fig. 1.10 shows the contribution of a single AP on extracellular field potentials. Therefore, overlapped APs can have huge impact on extracellular field potentials. For instane, the study by Vardi et. al. reported that firing activity of a single neuron shows high-correlation or high anti-correlation with the network activity [44]. The research study used bench-top patch-clamp system (Multiclamp 700B) with bench-top MEA system (MEA2100) to record intracellular and extracellular activities simultaneously. The measurement setup is depicted in Fig. 1.11. It was also stated that multi-clamp system was required to shed the light especially on anti-correlation between intracellular and extracellular recordings [44]. Moreover, collective activity of large population of a cell can cause hyperpolarization in a single-neuron [43]. Therefore, multi-patch-clamp recordings combined with the multi-electrode-array recordings of a very large population of cells can be a key feature to understand the connectivity between cells and their organizational scheme [43, 44].

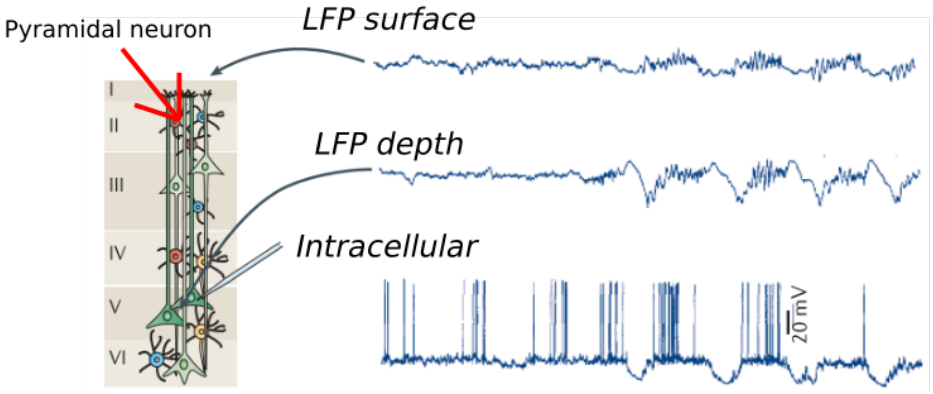


Figure 1.9: Simultaneous recordings of LFPs from surface and deep regions of neurons, and intracellular recordings (Adapted from [43]).

In order to offer a platform that can realize both extracellular and intracellular recordings simultaneously, firstly, a novel envisioned micro total analysis system (μTAS) that integrates flip-tip planar patch-clamp (FTPPC) electrodes and MEAs on the same wafer is proposed. MEA electrodes with 50 μm diameter with 400 μm distance between each other can be implemented on the front-side of the wafer. Funnel-shape planar patch clamps can offer a good coupling between cultured cells and electrodes on the tip. 2 μm tip diameter can be achieved by FTPPCs which mimics conventional patch pipettes. The microfabrication of this μTAS is a cost-effective process because it only uses 2-masks. In fact, it offers a scalable microfabrication process because it uses conventional photolithography. The proposed system is compared to patch-clamp, MEAs, 3D-MEAs, and CMOS-MEAs qualitatively in Table 1.4. The details of the microfabrication steps can be found in Appendix.

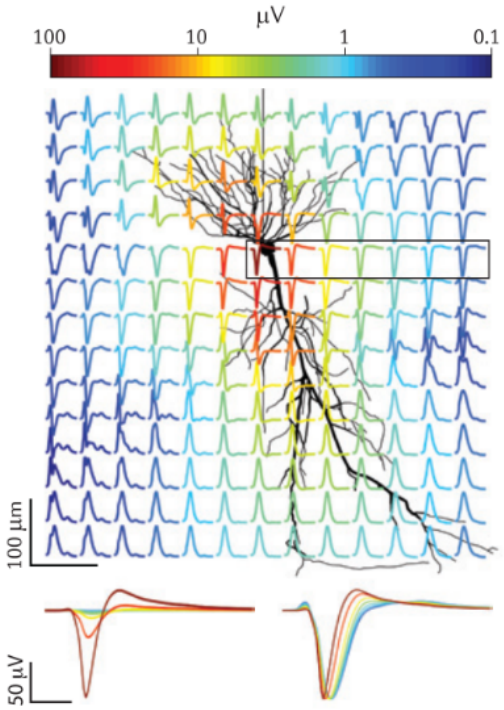


Figure 1.10: The contribution of a single AP on extracellular field potentials (Taken from [43]).

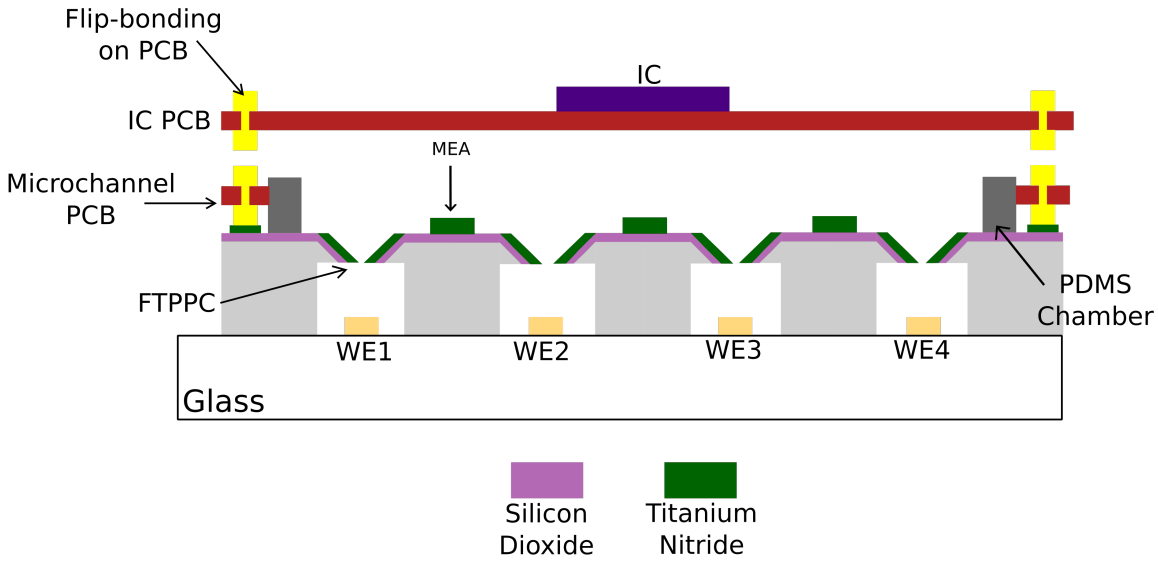


Figure 1.12: Stand-alone μTAS and CMOS IC.

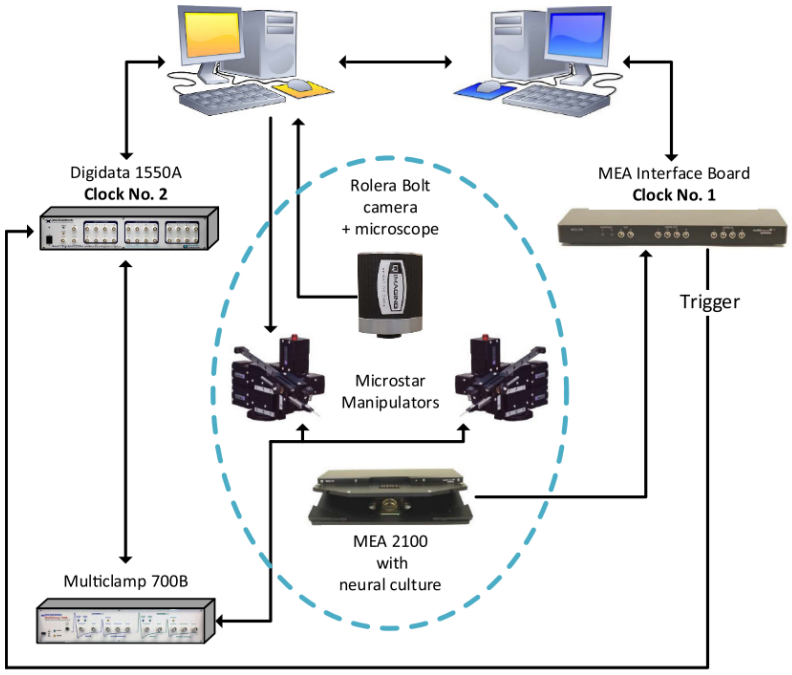


Figure 1.11: The setup used in simultaneous patch-clamp and MEA recordings (Taken from [44])

Table 1.5

Table of Targeted Specifications of Proposed Recording Unit		
Parameters	**Units**	**Targeted Specifications**
Supply	V	1.8
Technology	–	0.18 μm
No. of channels	–	16
Gain	dB	29.5
Bandwith	Hz	10 k
Injected current range	A	100 p to a few n
Input-referred voltage noise	μV_{rms}	Less than 10
Power	W	a few μ / channel

The proposed stand-alone μTAS must be combined and operated together with an integrated circuit (IC) designed for simultaneous extracellular recordings from MEA electrodes, and intracellular recordings from FTPPCs. The pads of both MEA and FTPPCs electrodes can be soldered to a printed-circuit-board (PCB) designed for μTAS. Another PCB that contains proposed IC can be connected by means of flip-bondings as it is shown in Fig. 1.12. By this project, we propose a dual-mode reconfigurable recording unit for both in-vitro measurements of MEA and current-clamp in channel-array operation. In doing so, each channel can be configured independently which enables simultaneous extra- and intra-cellular recordings. The envisioned μTAS consists of 16 of MEA electrodes and 16 of FTPPCs. Therefore, 16-channel operation is proceeded to have access to all electrodes. The gain of the recording channel must be high enough to amplify the extracellular potentials. At the same time, recordings of intracellular activities should not exceed the supply voltage 1.8 V. The seal resistance of envisioned patch electrodes cannot be known before fabricating. 3D-MEAs have provided intracellular potentials around 20 mVs. If the same value for intracellular activity is taken into account for proposed system, gain 30 V/V (or 29.5 dB) is chosen for both modalities to avoid clipping issues. As it is shown in Table 1.1, electrophysiological activities of cells occurs at frequencies ranging from 0.1 Hz to 10 kHz. Therefore, bandwidth of the recording channel must be at least 10 kHz. Also, the smallest possible signal in amplitude is around 10 μV (see Table 1.1). Therefore, input-referred noise level must be kept below 10 μV to record small extracellular signals. The current-clamp injection current mimics the currents generated by synaptic activities. The current value ranging from 100 pA to 1.6 nA to be able to measure subthreshold PSPs and APs. The proposed platform is designed for in-vitro measurements that mimic the body temperature of animal or human bodies. Therefore, low power consumption must be targeted to avoid heating issues which might result in killing cells [45]. Table of targeted specifications is given in Table 1.5.

2

Proposed Architecture and Circuit Design

2.1. System Level Architecture

Fig. 2.1 presents the top-level system architecture with a simplified representation of the dual-mode channel. The proposed architecture contains 16 recording channels (4×4) which form the channel array, Digital Control Unit, and Output Buffers. Fig. 2.1, MEA represents the MEA electrode assigned for the particular channel, whereas WE corresponds to each independent working electrode in the pore.

Each channel can be independently configured for 2 different modalities: 1) MEA-modality; 2) CC-modality. The (in total 8) switches (see Fig. 2.3)[1] select the operation modes of the channel out of these 2 possible options. Digital Control Unit programs and controls the switches. Each channel consists of a capacitively coupled instrumentation amplifier (CCIA) and current injector circuit. The output of the channel-under-duty is directed to output buffers to be post-processed. The detailed explanation regarding the each main block of the top-level system architecture is given in the following sections (Section 2.2- 2.3).

2.2. Digital Control Unit

Digital Control Unit is the logic circuit in charge of controlling the switches. Each channel is controlled by 7 switches which form the Digital Control Logic. The list below describes the duties of each individual switch.

- **MEA_SEL**: This switch is dedicated to connect the particular MEA electrode to the channel.
- **MEA_SEL!**: The all MEA electrodes except the one being investigated by the channel in MEA-modality is connected to the non-inverting node of the channel through MEA_SEL! to act as the reference electrode.
- **REF_SEL**: This switch connects reference electrode to the non-inverting node of the channel.

[1]Current injector switches are not shown here for simplicity. These switches will be explained in Section 2.3.2.

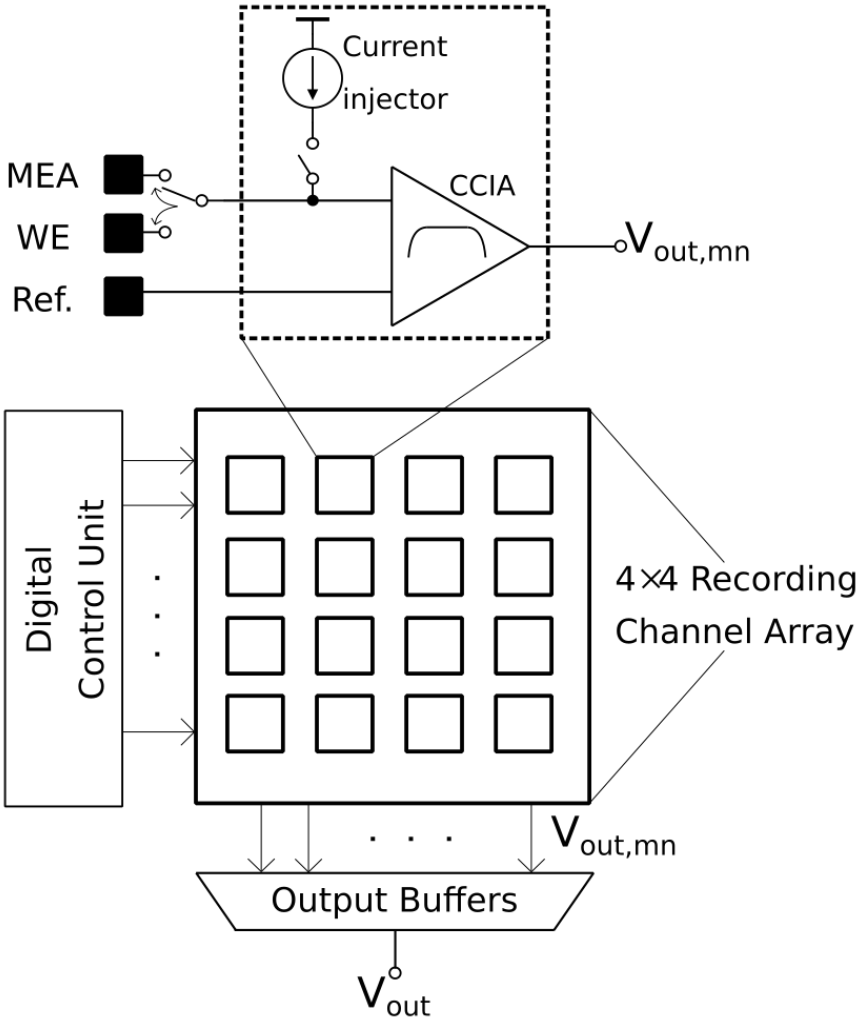


Figure 2.1: Top-level system architecture. (Figure inspired from [46])

- **COL_SEL**: After activating this switch, the output voltage of the channel is being directed to the output buffers.
- **WE_SEL**: There is WE_SEL to connect each working electrode to the inverting node of the channel.
- **CC_SEL**: This switch let current flowing from current injector DAC reach to the working electrode through the inverting node of the channel.
- $\mathbf{B}_n$, $\mathbf{B}_n$**!**: These switches are put in the circuit as complementary switches of the current injector DAC.

2.3. Recording Channel

Fig. 2.3 shows the schematic of dual-mode reconfigurable channel. The AC-coupled front-end amplifier (shown in dashed line in Fig. 2.3) is shared between MEA- and CC-modality. There are two main reasons to choose capacitively-coupled configuration for the channel: 1) The DC offset voltage rising from the electrode-electrolyte interface can reach up to 1 V [47]. This voltage level is considerably higher than the signal amplitudes generated from the cells. By means of this architecture, the DC offset voltage is removed. 2) the DC current that generated from the current injector circuit can flow through the working electrode (WE) to apply current-clamp technique on cells.

The transfer function of the AC-coupled front-end amplifier is given in Eq. 2.1. The mid-gain A_M is defined by the ratio of the capacitors C_s and C_f. The high-pass cut-off frequency (f_{HP}) corner sits at $\frac{1}{2\pi R_f C_f}$, and the low-pass cut-off frequency (f_{LP}) corner happens at $\frac{f_{unity}}{A_M}$ which is equal to $\frac{G_m}{2\pi C_{Load} A_M}$. Note that G_M is the transconductance of the front-end amplifier, whereas R_f represents the resistance in the feedback path which has done by the diode-connected PMOS transistors.

$$\frac{V_{out}}{V_{in}} = -\frac{sR_f \cdot C_s}{1 + sC_f \cdot R_f} \tag{2.1}$$

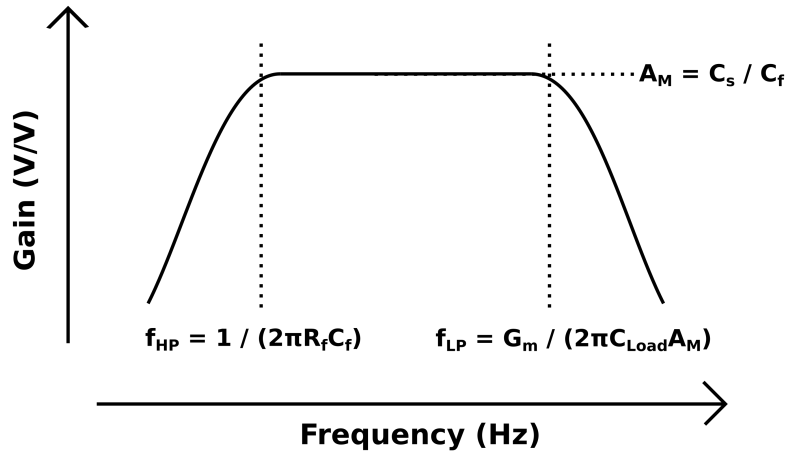


Figure 2.2: The closed-loop characterization of AC-coupled front-end amplifier shown in Fig. 2.3.

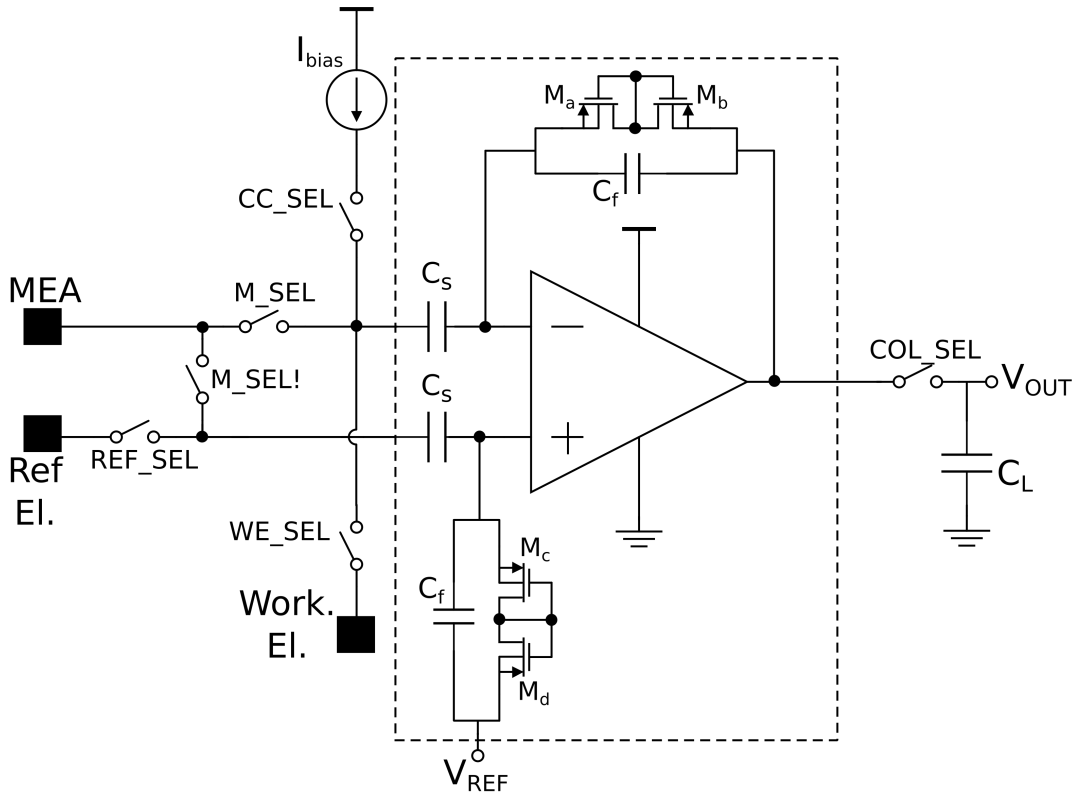


Figure 2.3: The circuit schematic of the dual-mode reconfigurable channel.

The channel configuration for the MEA-operation is depicted in Fig. 2.4. When the channel operates in MEA-modality, the switches CC_SEL and WE_SEL are inactive, while M_SEL, M_SEL!, REF_SEL are turned on. If the voltage is wanted to be read out, then the switch COL_SEL of this particular channel is being activated.

When current-clamp cell study technique is required to be applied, then the channel is configured as it is shown in Fig. 2.5. All the MEA electrodes are connected to the reference electrode node by means of M_SEL! as being on. Therefore, working electrode dedicated for the channel is connected to the inverting node of the AC-coupled amplifier. In addition, the switches REF_SEL, WE_SEL, CC_SEL are turned on. The switch COL_SEL is active, when the output voltage is asked to be read out.The position of the all switches for each modality is given in Table 2.1.

2.3.1. 5T Operational Transconductance Amplifier (5T-OTA) Design

Fig. 2.6 presents the schematic of single-ended 5T-OTA used in AC-coupled instrumentation amplifier. Transistors M1 and M2 consist of the input pair of the OTA. The active load is realized by means of transistors M3 and M4. The tail current of the circuit is supplied through transistor M0 which is connected to its current mirror pair biased with reference current. The figure does not show the biasing circuit.

5T-OTA, in other words, differential pair with an active load is a standard circuit topology. Yet, the circuit requires proper sizing of transistors to meet certain noise, power, and area

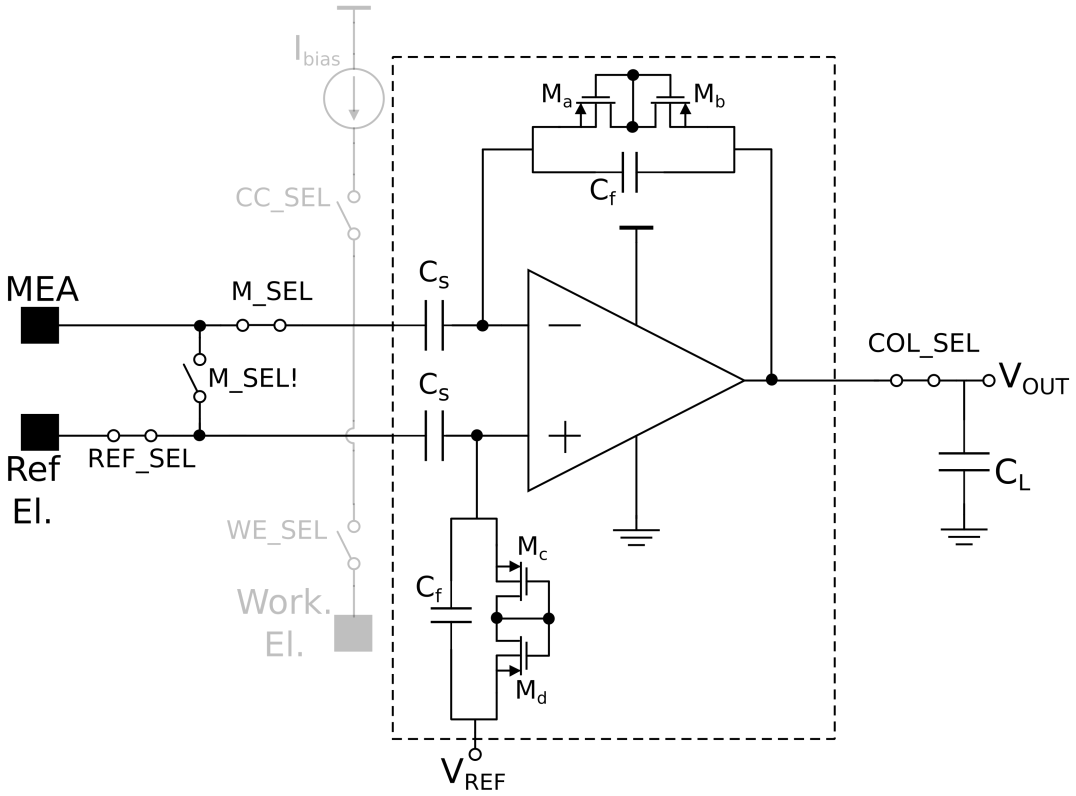


Figure 2.4: The dual-mode channel configured for MEA operation.

specifications. The tail current is specified as 2 μAs. Therefore, the current flows through left-branch (M1 and M3), and right-branch (M2 and M4) is equal and 1 μA.

The inversion coefficient (*IC*) defines how the channel of a MOS transistor is inverted. Depending on the bias voltage, the free carriers in the inversion channel differ in quantity. By changing *IC*, the operation region of the transistor can be set as weak, moderate or strong inversion [48].

Firstly, the device parameters of the transistors in TSMC 0.18 μm technology are determined to be able to move forward with design choices. Table 2.2 shows simulated and calculated process parameters of NMOS and PMOS transistors used in this technology. In Table 2.2, I_0 represents the technology current, whereas n_0 is the slope factor of devices. The term μ_0 corresponds to the low-field mobility, while C_{ox} defines the gate-oxide capacitance. The relation between *IC* and drain current is given in Eqn. 2.2 below, where S defines the aspect ratio (W/L) of the device [49].

$$IC = \frac{I_D}{I_0.S} \tag{2.2}$$

As it has mentioned before, *IC* is a numerical measure of the inversion level of the channel. For $IC < 0.1$, the channel is weakly inverted which means the device is in weak inversion. When $0.1 < IC < 10$, the device is now moved to moderate inversion. Strong inversion occurs when $IC > 10$ [48, 49].

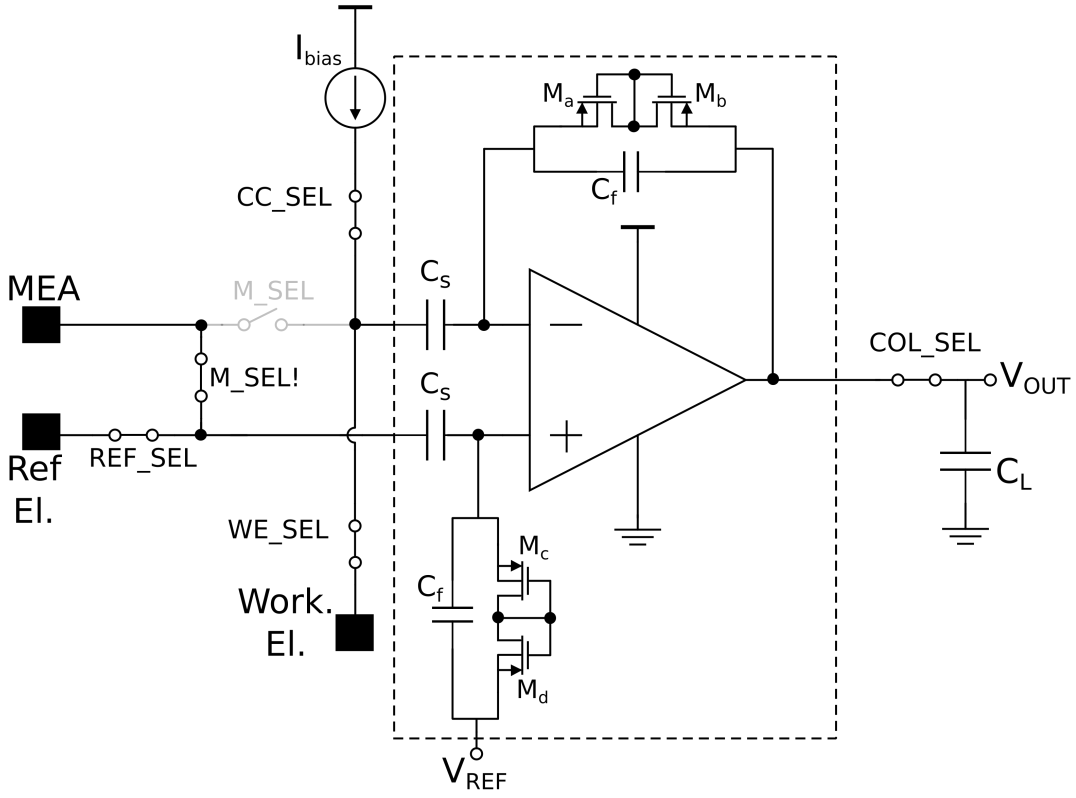


Figure 2.5: The dual-mode channel configured for CC operation.

As it can be seen from Table 2.3, the transconductance efficiency (g_m/I_D) reaches its highest when the device operates in weak inversion. The transconductance efficiency can be described as a quality factor of a transistor. It basically shows how much transconductance can be provided for a given current value [48]. Fig. 2.7 shows the relation between V_{EFF} and g_m/I_D. It is clearly observable that pushing the device into deeper weak inversion results in higher transconductance efficiency. Therefore, choosing lower *IC* must cause higher g_m/I_D. For a MOS transistor, transconductance efficiency in weak inversion is given as [49]:

$$g_m / I_D = \frac{1}{n \cdot U_T} \tag{2.3}$$

where transconductance equals to:

$$g_m = \frac{I_D}{n \cdot U_T} \tag{2.4}$$

Table 2.4 presents the sizes and operating points of 5T-OTA. It is challenging that to design a low-noise amplifier by not exceeding a certain power consumption. The input-referred thermal noise power of the OTA can be calculated as :

$$\overline{v^2_{thermal}} = \left[\frac{16kT}{3g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} \right) \right] \tag{2.5}$$

where g_{m1} corresponds to the transconductances of M1 and M2 (identical pair), and the transconductance of M3 and M4 (identical load) is represented as g_{m3}. In order to minimize

Table 2.1

Table of Positions of the Switches in CC- and MEA-modality		
Switches	**CC-Modality**	**MEA-Modality**
MEA_SEL	OFF	ON
MEA_SEL!	ON	OFF
CC_SEL	ON	OFF
REF_SEL	ON	ON
WE_SEL	ON	OFF
COL_SEL	ON	ON
B	ON	OFF
B!	OFF	ON

Table 2.2

Device parameters at 300 K for TSMC 0.18 μm Technology			
Parameters	**NMOS**	**PMOS**	**Units**
I_0	0.561	0.169	μA
n_0	1.4	1.4	N/A
μ_0	30	9.5	$\mu A/V^2$
C_{ox}	10	9.5	fF/ μm^2

the input-referred thermal noise, g_{m1} must be higher than g_{m3}, so that the term g_{m3}/g_{m1} can be very small. This aim can be achieved by using wider devices for input pair M1 and M2 such that W/L ratio is high. At the same time, aspect ratio of current mirror load devices must be decreased to decrease their transconductances. In other words, current mirror load must operate in strong inversion, whereas input pair operates in deep weak inversion. It can be seen in Table 2.4, transconductance of input pair reaches 28.9 μA/V with *IC* 0.01. To be able to push current mirror load devices into strong inversion, *IC* has been chosen as 50. Although increasing the aspect ratio of input pair results in higher transconductance, it also increases the input capacitance of the amplifier. The contribution of the OTA to the input-referred noise of the channel is given as follows:

$$\overline{v_{ni,ch}^2} = \left(\frac{C_s + C_f + C_{in}}{C_s}\right).\overline{v_{OTA}^2} \tag{2.6}$$

Therefore, an increase in the width of input pair causes higher input capacitances which results in higher input-referred noise. The reason of that is that the input capacitances play a role in signal division. In other words, it decreases the overall gain of the amplifier, so that increases the input-referred noise. On the other hand, it is advantageous to use wider devices to reduce the flicker noise contribution of the transistors. The flicker noise of the OTA is given in the equation below [50]. The optimization study have not been implemented to find the best ratio of W/L, preliminary schematic simulations show that increasing the width and the length with the same factor did not result in very lowered input-referred noise. For example, 360 μm / 2 μ m aspect ratio resulted in 11.2 μV_{rms}, where it is found as 11.4 μV_{rms} when aspect ratio is 180 μm / 1 μm. Considering also the area concerns, the latter W/L option is applied to the

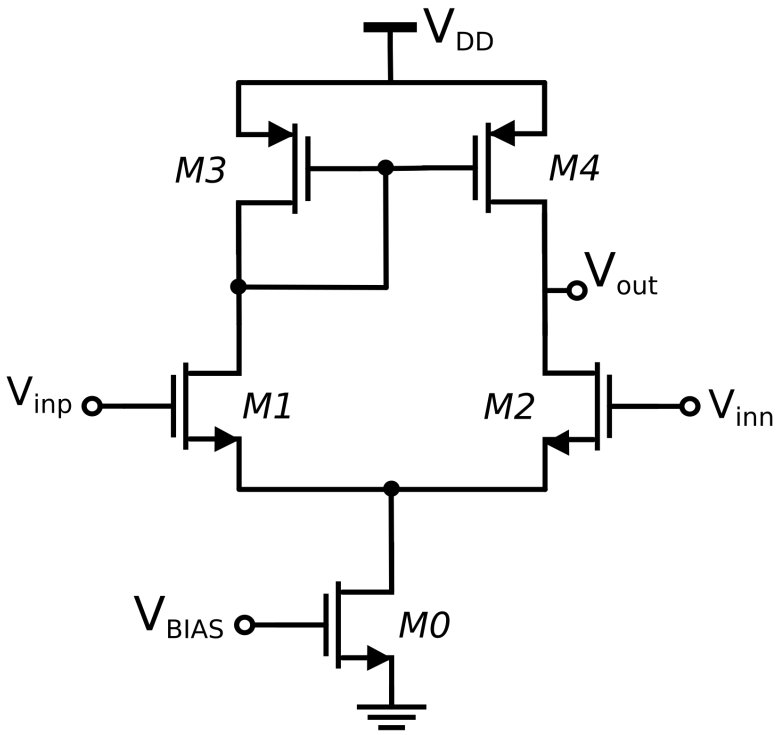


Figure 2.6: Schematic of 5T-OTA.

input transistors.

$$\overline{V_{1/f}^2} = 2\frac{K}{C_{ox}\cdot(WL)_3}\cdot\frac{1}{f}\cdot\left(\frac{g_{m3}}{g_{m1}}\right)^2 + 2\frac{K}{C_{ox}\cdot(WL)_1}\cdot\frac{1}{f} \tag{2.7}$$

Fig. 2.8 shows the gain and phase of 5T-OTA in AC analysis. The differential gain of the transconductance amplifier can be given as:

$$A_d = g_m \cdot r_{out} \tag{2.8}$$

where g_m is the transconductance value of one of the input pair devices, and r_{out} is the parallel combination of the r_{o1} and r_{o3} [51]. The transconductance (g_m) of 5T-OTA is 28.9 μA/V and the output impedance (r_{out}) is found and simulated as 6.72 MΩ. Therefore, the

Table 2.3

Expressions for W, g_m/I_D, V_{DSAT} and V_{EFF} [48]
$W = (L/IC)\cdot(I_D/I_0)$
$g_m/I_D = 1/\left(n\cdot U_T\cdot\left(\sqrt{IC+0.5\sqrt{IC}+1}\right)\right)$
$V_{DSAT} = 2U_T\cdot\sqrt{IC+0.25}+3U_T)$
$V_{EFF} = n\cdot U_T\cdot ln(IC)$

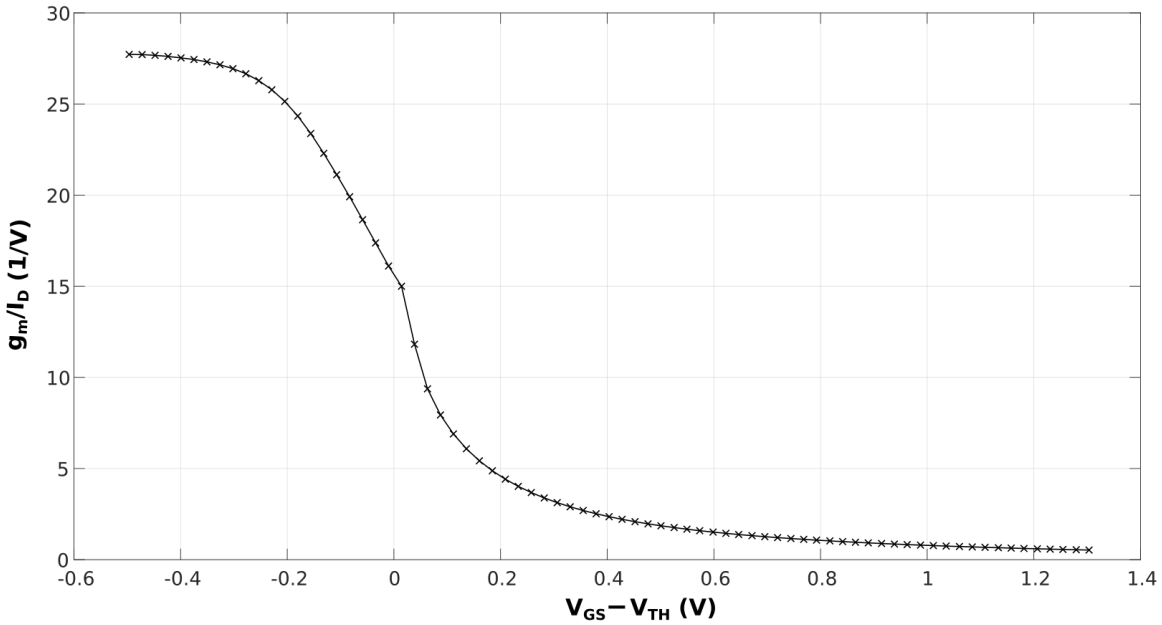


Figure 2.7: Simulated g_m/I_D of an NMOS as V_{GS} swept from 0 to 1.8 V.

Table 2.4

OTA Transistor Sizes and Operating Points					
Transistor	**W/L (μm)**	**I_D (μA)**	**g_m (μA/V)**	**g_m/I_D (V^{-1})**	**Inversion Coefficient**
M0	1/14	2	7.2	3.9	50
M1	180/1	1	28.92	29.1	0.01
M2	180/1	1	28.92	29.1	0.01
M3	1/8	1	3.57	3.59	50
M4	1/8	1	3.57	3.59	50

differential open-loop gain A_d is calculated as 45.8 dB. The calculated results can be confirmed by the both schematic and post-layout simulation results with a small deviation 0.18 dB and 0.29 dB where A_d is simulated as 45.59 dB and 45.47 dB with schematic and post-layout views, respectively. The phase margin of the OTA is 72.13 degree for schematic views, whereas 70,92 degree is simulated for phase margin of the amplifier. Since the amplifier is in a single-stage configuration, there is no stability issues existing.

Although gain-bandwidth product (GBW) is expected to be at $GBW = g_m/C_{out}$ where C_{Load} is the main contributor of C_{out}, the simulation results show that roll-off curve passes 0 dB earlier than expected. The calculations based on simulation results reflects that there is another parasitic capacitance which plays a role on GBW. Fig 2.9 shows the relation between C_{Load} and found $C_{composed}$ which is composition of C_{Load} and $C_{parasitics}$ in the circuit. $C_{parasitics}$ is found as 204 fF where C_{gd} is 69 fF. The junction-drain capacitance C_{jd} is simulated as 174 fF which might be playing a role on overall parasitics.

Transient analysis is run to simulate the settling time of the OTA. The OTA was used in

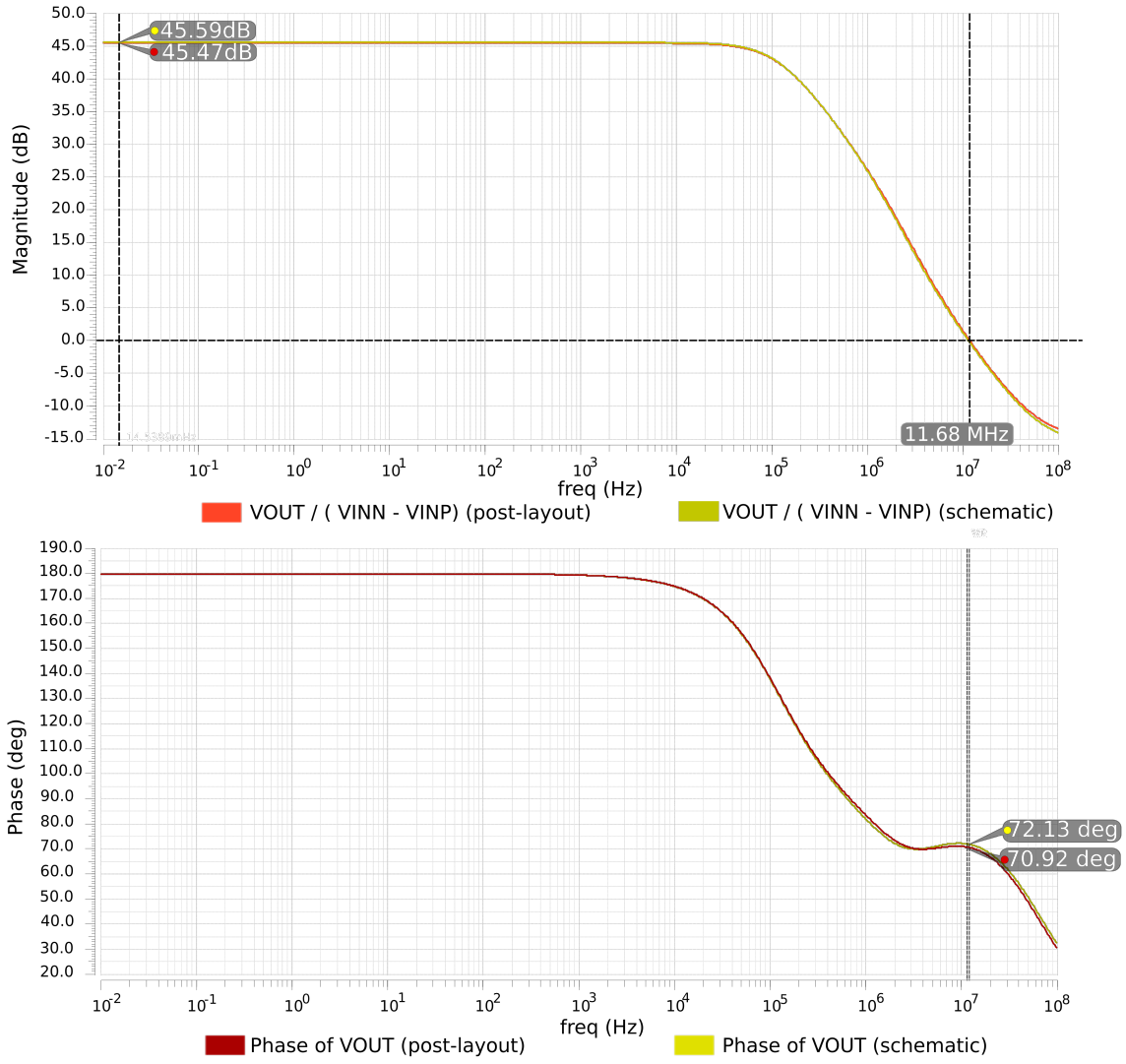


Figure 2.8: Gain and phase of 5T-OTA.

unity gain configuration where its inverting input is connected to the output node. For input signal at V_{INP} node, the extreme case scenario was thought which assumes presence of 10 mV of extracellular activity at a MEA electrode. A 10 mV input signal is amplified by the gain of the channel (23.5 dB in post-layout simulations). This will result in 150 mV at the output, and for the settling time analysis, this value is multiplied by 2 to enclose range of all possible input signals. A 300 mV with 1 ns of rising time input signal is applied to the non-inverting node of the OTA, and resulting step response simulation is given in Fig. 2.10. The output voltage reaches steady-state position (303.5 mV) with 0.4 mV tolerance in around 2 μs for both schematic and post-layout simulations.

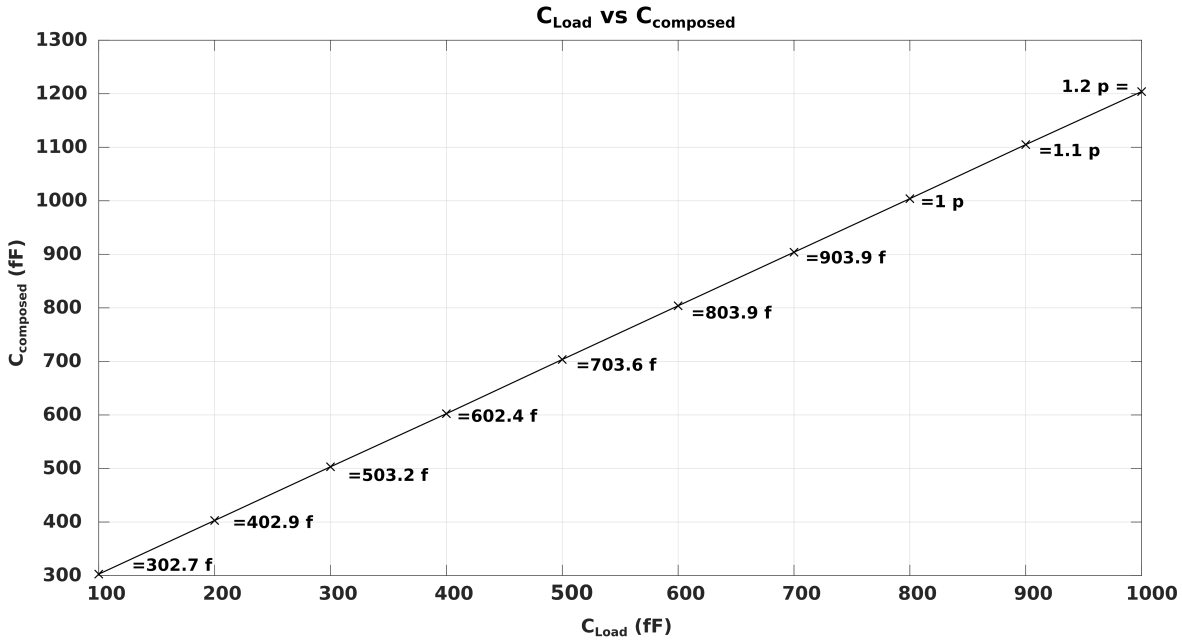


Figure 2.9: The relation between C_{Load} and $C_{composed}$ which is equal to C_{Load} + $C_{parasitics}$.

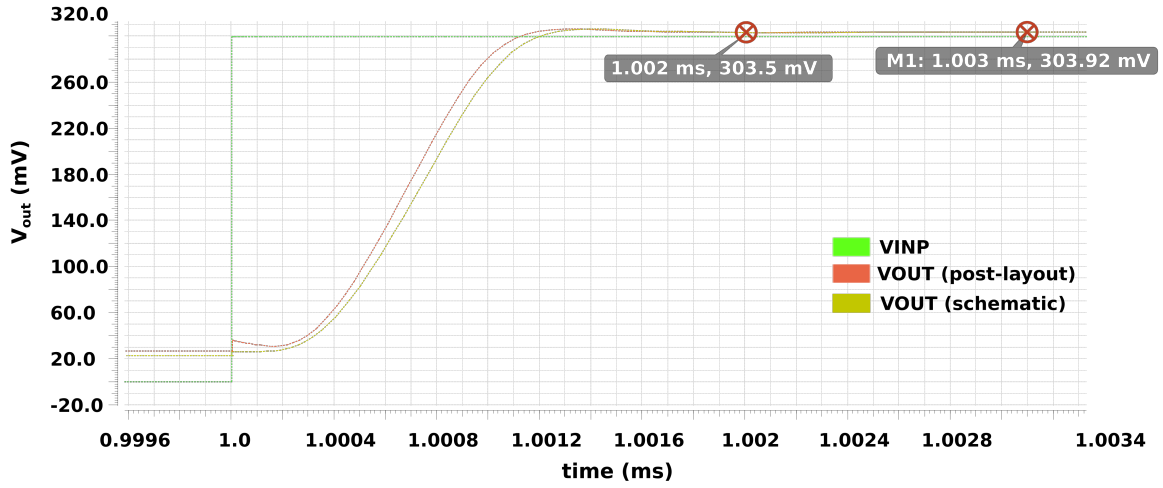


Figure 2.10: Settling time needed of 5T-OTA when 0.3 V input voltage applied with 1 ns rising time.

Fig 2.11 presents the layout of 5T-OTA. The input pair is the critical block to have good matching between two transistors. Parameter variations, e.g. oxide thickness, can occur across the wafer. These variations are most likely to happen linearly when devices are in short distance from each other. Common-centroid patterns are used to average out these variations, so that minimize the effect of errors happening during the fabrication processes. In our OTA design, therefore, common centroid patterns are applied to all sub-blocks which are input-, current mirror load-, and current mirror bias-pairs. The input pair is notated with "A" in Fig 2.11. Both M1 and M2 are divided into 2 pieces by using "multiplier=2" in Cadence Spectre to apply ABBA common-centroid pattern. Then, in the layout view, 10 fingers are used

for each input pair devices. The input nodes are connected in between with the same width and length of interconnections. The input pair sub-block is guarded with PSUB guarding to connect the bulks of devices to ground node. The letter "B" highlights the current mirror load devices, and ABBA common-centroid is also followed for these devices. In addition, NWELL taps are used in shared NWELL to be able to connect the bulks of PMOS transistors to VDD node. The third sub-block is presented with letter "C" in Fig 2.11. As in the other sub-blocks, the pattern ABBA is applied to current mirror bias devices. 5T-OTA consumes 55 μm × 55 μm of area on silicon wafer.

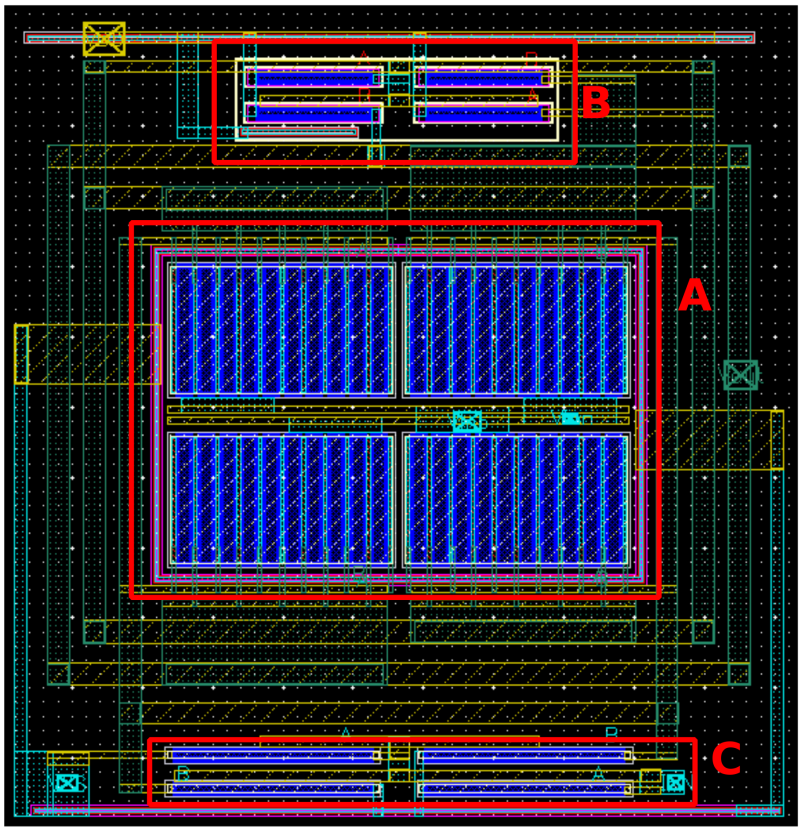


Figure 2.11: The layout view of 5T-OTA which covers 55 μm × 55 μm.

2.3.2. Unary-Weighted Current-Steering DAC Design

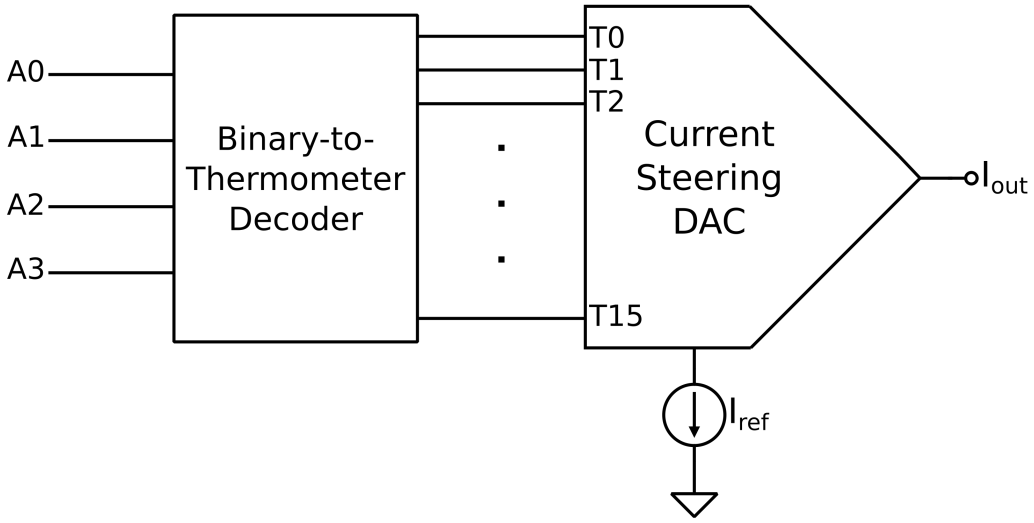


Figure 2.12: Block diagram of unary-weighted current-steering DAC.

In order to understand the operation principle of unary-weighted current-steering DAC, the conventional binary-to-thermometer-coded DAC must be introduced. The block diagram of unary-weighted current-steering digital-to-analog converter (DAC) is given in Fig. 2.12. The converter depicted is an example of 4-bit thermometer-coded DAC. The relation between input and output digital code of the converter is given in Table 2.5. As it can be seen in Table 2.5, In the case of conventional method, current-steering DAC contains 2^N digits consisting of thermometer code. Since the binary code is 4-bit, then there is $2^N = 16$ bits, and 16 current sources that are controlled by the thermometer code. For example, to replicate the I_{ref} of the DAC, the first current source must be turned on. Therefore, the binary code (A0, A1, A2, and A3) must be "0001", respectively. If the I_{ref} is wanted to be made tripled, then the binary code becomes "0011". In other words, the decimal representation of the binary code decides that how many of the unit current sources contribute to I_{out}.

There are several advantages of thermometer-coded DACs compared to binary-weighted DACs. The first advantage of thermometer-coded current DAC is guaranteed monotonicity. The current output of a monotonic current DAC always increases (decreases) as the digital input code increases (decreases). In the thermometer-coded current DAC, to increase (decrease) the output current (I_{out}), the digital code increases (decreases) by 1 Least Significant Bit (LSB). In other words, the output current always increases with the increasing digital input code which meets the definition of monotonicity [52].

The other advantage of unary-weighted thermometer-coded DAC is the relaxed matching requirements. To achieve differential nonlineartiy (DNL) <0.5 LSB, 50% matching of two unit current sources is good enough [52].

One of the advantages of thermometer-coded DAC is reduced glitch problem. In a 3-bit DAC, in order to turn on 3 unit current sources, the binary code must be "011". In order to have 4 unit current sources operating, the binary codes changes from "011" to "100". It means that

Table 2.5

Thermometer code representations for 4-bit binary values	
Binary code A0 A1 A2 A3	**Thermometer code T0 T1 T2 T3 T4 T5 T6 T7 ... T15**
0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
0 0 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
0 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1
0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1
0 1 1 0	0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1
. . .	. . .
1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

all binary bits change their current situation to the opposite one. However, this transition only means that one more additional current source is activated to contribute to I_{out}. Therefore, glitching is considerably decreased by this type of DAC architecture [52].

The proposed design of DAC for the dual-mode reconfigurable channel mainly uses the same operation principle of unary-weighted thermometer-coded DACs. As it is shown in Fig. 2.13, each channel contains unit current source as the current injector. The current injector is combination of a PMOS transistor which copies I_{ref}, and the control switches B_n, $B_n!$, and CC_n. All the unit current sources (PMOS transistors) are connected on their gates which guarantees the (almost) same V_{bias} for all of them. Also, the nodes after each B_n are shorted together as node I_{gen} as it has done in thermometer-coded DACs. Therefore, for example, to double I_{gen}, two of unit current sources are activated. To obtain $10 \times I_{ref}$, 10 of the switches B_n are switched ON. The switch represented in each individual channel to control current injector is called as CC_n in the unit current injector. In the case of CC_n is in active mode, then it means that the channel is connected to the WE_n through switch WE_{SEL}.

The schematic of each unit of unary-weighted DAC is depicted in Fig. 2.14. Since the minimum current used to stimulate the cells is determined as 100 pA, I_{ref} is set to 100 pA. To determine the sizes of PMOS current mirror devices, the equation below followed:

$$I_{Dp} = I_{0p}.\frac{W}{L}.exp((V_{GS} - V_T)/nU_T) \tag{2.9}$$

I_{0p} corresponds to technology current for PMOS, n is the slope factor in weak inversion (see Table 2.2), V_T is the threshold voltage of the PMOS device, and U_T represents thermal voltage. When the suitable values are substituted into the equation above, the aspect ratio of the PMOS current mirror device is found as 6. Note that to calculate W/L, the equation for drain current in weak inversion is used, since the current value dealt with is extremely small. In fact, I_{ref} is more than 1500 times less than the technology current. Since the aspect ratio is decided on, the next step is choosing the length of the device. The simulation results show that if the length of the device keep increasing, the leakage current rising from the current-mirror

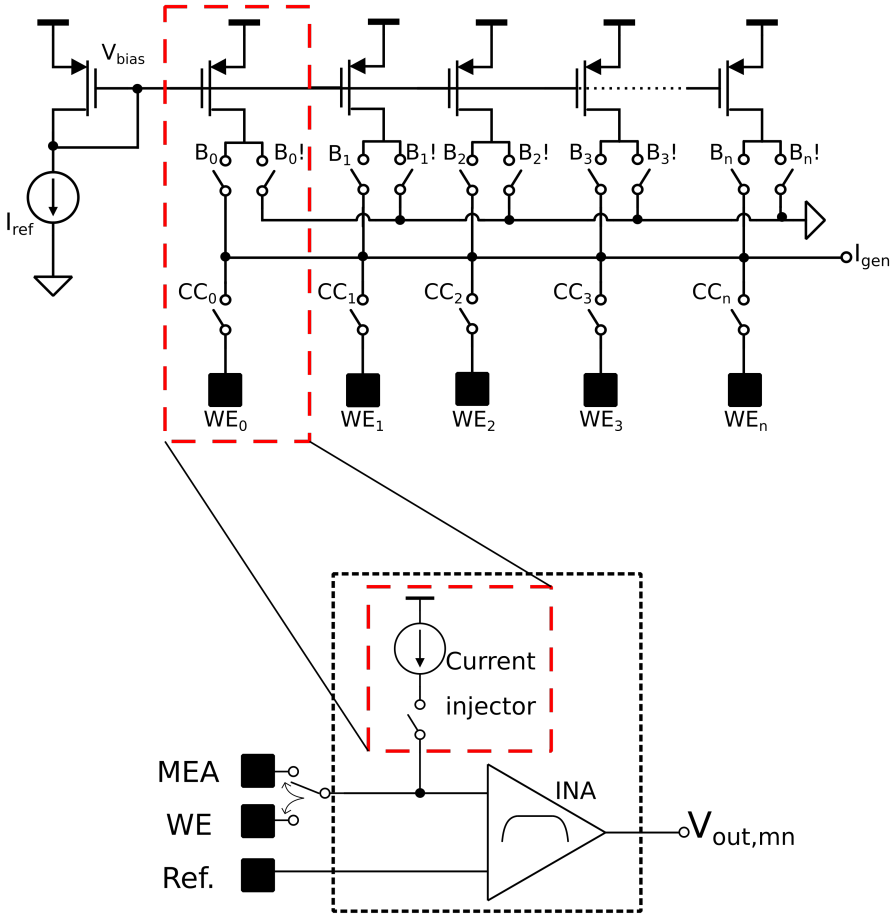


Figure 2.13: Current injector DAC.

devices is decreased. To be more specific, if the transistor has sizes as 6 μm/ 1μm, then, the resulting current at the drain of M5 is 115.5 pA. This means that only 1-bit of DAC gives 15.5% current error which can reflect around 250 pA error for a 16-channel array. At the same time, the area occupation of the unit current source in a channel must be taken into account. In this case, W/L ratio of PMOS current mirror transistor is chosen as 60 μm/ 10μm. The complementary (B_n and $B_n!$) and current-clamp selection switches (CC_n) are implemented by PMOS transistors in minimum size. The complementary switches are implemented to direct the current to the ground through $B_0!$, when B_0 is inactive. In doing so, the leakage currents at drain node of M3 and M5 are tried to be reduced.

The relation between digital input code and I_{out}/I_{ref} can be observed in Fig. 2.15. In order to characterize the DAC properly, firstly, one unit current injector has undergone Monte Carlo process and mismatch simulations. The number of samples is chosen as 200. The mean value for a single current injector is found as 107.7 pA when I_{ref} is 100 pA. Note that I_{ref} is always kept at 100 pA throughout all MC simulations mentioned here. The same analysis has done for the 4 unit current injectors shorted at I_{gen} node. When the simulations are applied, the mean current value is found as 110.6 pA. In the light of these simulations, we can assume that one unit current injector contributes around 1 pA as the leakage current. After that, to increase the

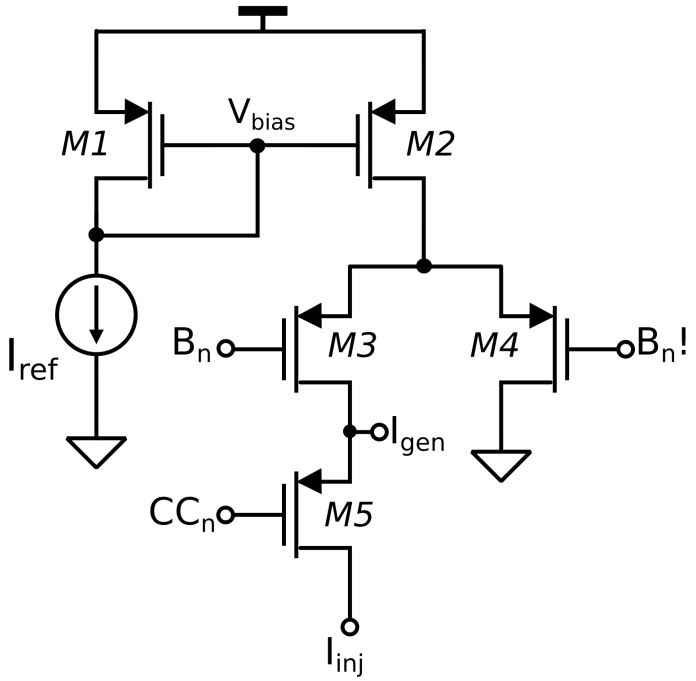


Figure 2.14: Schematic of unary-weighted DAC unit.

current in the first unit current source, the other current injectors were activated one by one. In that way, the current in the first current injector must be around 100 pA, 200 pA, 300 pA, and 400 pA by activating the adjacent current sources. The mean current values after the Monte Carlo (process and mismatch together) simulations are found as 219.6 pA, 333.6 pA, and 452 pA, respectively, when the ideal cases assume 200, 300 and 400 pA. By these simulations, the leakage current from an active unit injector is calculated as 11.38 pA which is the average value of 4 current injectors. The rest of the values are extrapolated according to these results.

In the light of MC simulations, Fig. 2.15 is generated to show the nonlinearities of the proposed DAC, and how it deviates from the ideal case. In ideal case, each output increment from one digital input code to the adjacent code. However, in proposed DAC, the increment does not happen ideally, but it increases with slightly higher values than 1 LSB (100 pA). The difference between the actual increment and ideal increment is defined as differential

Table 2.6

Unary-Weighted DAC Transistor Sizes		
Transistor	**W/L (μm)**	**I_D (A)**
M1	60/10	$100p$
M2	60/10	$100p$
M3	0.22/0.18	$100p$
M4	0.22/0.18	N/A
M5	0.22/0.18	$100p$

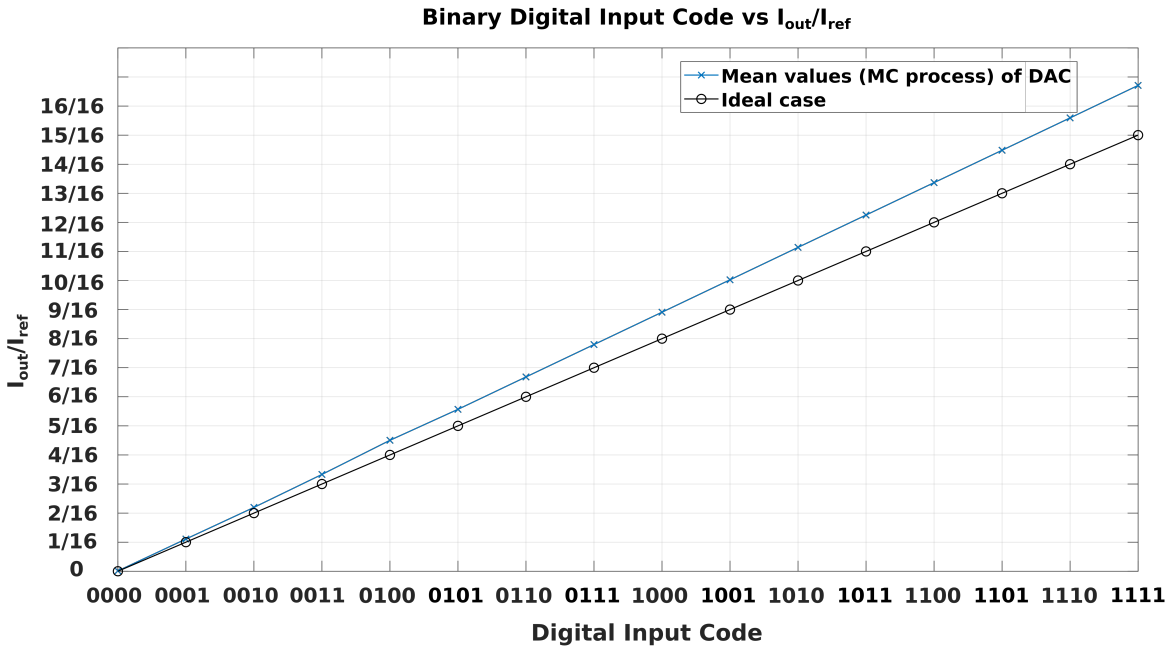


Figure 2.15: The relation between digital input code and I_{out}/I_{ref}.

nonlinearity (DNL), and it can be formulated as follows [53]:

$$DNL_n = \frac{I_{inc,n} - I_{inc,ideal}}{I_{inc,ideal}} \tag{2.10}$$

where $I_{inc,n}$ represents the actual increment at n^{th} digital input code, and $I_{inc,ideal}$ is equal to the ideal increment and 1 LSB which is 100 pA in this case. For instance, DNL_2 is the difference between actual increment (333.6p-219.6p=114pA) 114 pA and ideal increment 100 pA which results in as 0.14 LSB.

Another fundamental characteristic of DACs is the integral nonlinearity (INL) which can be defined as the difference between actual output values at an input code and the expected value at the same value according to the reference line drawn from the first point to the last point. INL can be formulated as follows [53]:

$$INL_n = \frac{I_{out,n} - I_{out,ref}}{I_{ref}} \tag{2.11}$$

where $I_{out,n}$ defines the actual output value at n^{th} digital input code, and $I_{out,ref}$ is the expected value at n^{th} code when a straight reference line is drawn between the first and the last points. I_{ref} represents the reference current (100 pA). When the reference line is drawn between the zero input code (0000) and "1111", the resulting line shows a trend according to the equation $y = 110.97n - 1.24p$, where n represents the n^{th} digital input code. For example, when the digital input code "0100" (4^{th} input code), then the expected output current of the DAC is 442.6 pA. However, the actual simulations reflects that the output current at the same input code is 452 pA. Therefore, INL_4 is 0.09 LSB for 4^{th} input code "0100".

Ideally, a current DAC gives 0 A output current when the digital input code is 0. Any difference from 0 A current at "0000" shows the offset error of the DAC [53]. Ten, the offset

Table 2.7

Summary of characteristics of proposed current DAC	
Characteristics	**Value (LSBs)**
DNL	0.18
INL	0.08
Offset error	0.013
Gain error	0.11

error is given as 1.25 pA or 0.013 LSB in proposed design since the current at I_{inj} node is found as 1.25 pA.

As the last but not least characteristic of the DAC given is the gain error. The gain error shows the deviation of the slope of transfer curve of output current from the ideal slope [53]. Therefore, it can be formulated as in Eq. 2.12. The slope of the actual transfer curve is 110.97 as it is mentioned above in Eq. 2.3.2. Therefore, the gain error is 0.11 LSB where ideal slope is 100 pA.

$$Gain\ error = Ideal\ slope - Actual\ slope \tag{2.12}$$

The characteristics of the proposed DAC is summarized in Table 2.7 by giving the worst-case results. These results are obtained by connecting 4 unit current sources, and then running MC process and mismatch simulations together as it is mentioned above. The output currents are extrapolated after digital input code "0101" based on the MC simulations. In order to fully characterize the proposed DAC, further simulations are needed where all unit current sources are connected.

Fig. 2.16 shows the layout of the unit current injector of each individual channel. Copying the reference current to the channel in a correct and reliable way is an important aspect in current mirror. Because of the fact that this importance should be considered carefully, common-centroid pattern is also applied to the unit current injector. Preliminary schematic results show that using 4 multipliers rather than 2 multipliers for each current mirror PMOS transistor will give more accurate copied current values. Therefore, "ABBABAAB" common-centroid pattern is used for the current injector. This is highlighted in Fig. 2.16 with a big red box and letter "A'. The minimum size switches are placed on the right-hand side of the current mirror transistors in an NWELL. Also, switches B_0 and $B_0!$ are in the same distance to the drain of M2. Switches B_0,$B_0!$, and CC_0 are shown in the smaller red box with letter "B". The unit current injector covers 56.5μm × 44μm of area on a die in total.

2.3.3. Pseudo-Resistor Elements

In order to achieve high value resistors in standard CMOS technology, large areas must be consumed on silicon. The doping levels of silicon and poly-silicon allows us to have a sheet resistance ranging from a few $\Omega\square^{-1}$s to a few k$\Omega\square^{-1}$s. For this reason, long resistors must be used in folded manner which increases the parasitic capacitances of the structure. The resulted parasitic capacitance might degrade the frequency response [54].

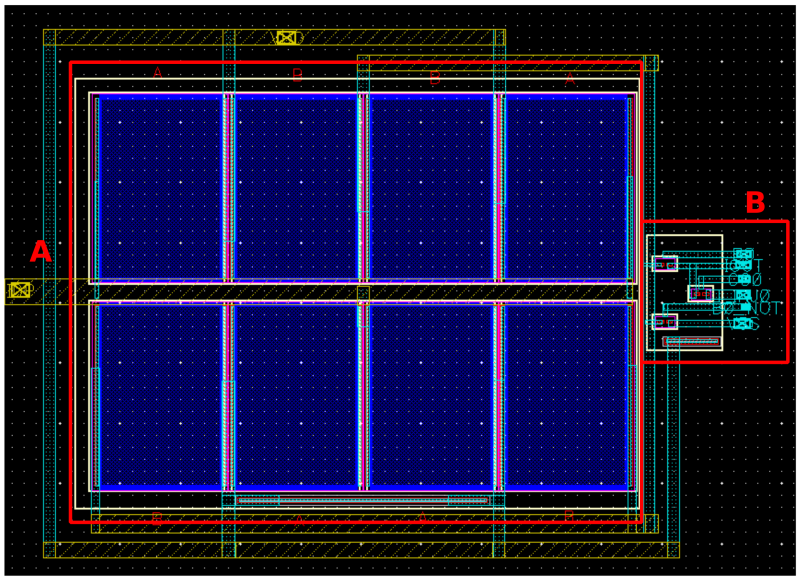


Figure 2.16: The layout of unit current injector which occupies 56.5μm × 44μm of area.

Pseudo-resistors based on MOS devices, therefore, are proposed as an alternative way of realizing high value resistors. In our design, we use pseudo-resistor elements to set the cut-off frequency of high-pass filter. The relation between the cut-off frequency and R_{pseudo} is given as:

$$f_{HP,cut-off} = \frac{1}{2\pi \cdot C_f \cdot R_{pseudo}} \tag{2.13}$$

As it can be seen from Eq. 2.13, the cut-off frequency and the resistance of pseudo-resistor element is inversely proportional to each other. The extracellular action potential can vary in frequency ranging from 0.1 Hz to 10 kHz. For example, in the presence of 100 fF capacitance in the feedback path, the resulting R_{pseduo} value is found as around 16 TΩs to achieve 0.1 Hz as cut-off frequency.

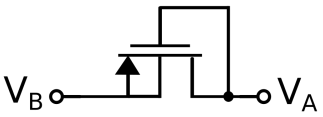


Figure 2.17: The schematic of single PMOS transistor as a non-tunable pseudoresistor element.

There are mainly two types of pseudo-resistors which are non-tunable and tunable structures. In non-tunable structures, one or even number of transistors in series are used in diode-connected configuration [54]. An example of single non-tunable PMOS device is presented in Fig. 2.17. The bulk and source of the device is connected together. This PMOS devices acts as a MOS transistor when $V_A < V_B$, and it has diode-like behaviour when $V_B < V_A$.

The device is operated in deep subthreshold regime to achieve very low current (in a few fAs range) flowing through the devices. In the case of fAs, the resistance can reach to TΩs

resistance values. In order to do that, the voltage difference between V_A and V_B must be close to 0 V. When the device acts as MOSFET in subthreshold operation region, then the current of the device can be calculated as follows [54]:

$$I_{SD} = I_{SD0} \cdot exp\left(\frac{V_{SG}}{n \cdot U_T}\right) \cdot \left[1 - exp\left(\frac{V_{SD}}{n \cdot U_T}\right)\right] \tag{2.14}$$

where [54]

$$I_{SD0} = 2n_{ox}\left(\frac{W}{L}\right)U_T^2 \cdot exp\left(\frac{|V_{th}|}{n \cdot U_T}\right) \tag{2.15}$$

Therefore, the resistance of the pseudo-resistors can be described as [55]

$$R \backsimeq 2\frac{L}{n\mu C_{ox} W U_T} exp\left(-\frac{(V_{GS} - V_{th} - nU_T)}{U_T}\right) \tag{2.16}$$

In the equations above, n is the slope factor, C_{ox} is the gate-oxide capacitance, μ presents the mobility of free carriers, U_T is the thermal voltage. W/L represents the aspect ratio of the transistors, and the threshold voltage of the device is given as V_{th}. As it can be interpreted from the equations, the longer devices give smaller current flowing through the channel which results in higher resistance values.

Although the single device pseudo-resistors are easy-to-implement in layout, they show asymmetric behaviour by their nature. To overcome this issue, tunable pseudo-resistors are proposed. Instead of connecting the gate to the drain, a voltage source is used to control the gate voltage of the device [54], [56] . This makes the device controllable, yet the resistance values that can be achieved by this kind of structures is reduced to MΩ-GΩ range [54]. That is a clear disadvantage for our design, where the cut-off frequency is wanted to be ideally at 0.1 Hz. Even with 100 GΩ feedback resistance, the cut-off frequency becomes around 16 Hz which might result in loss of valuable information about the cell activity.

Therefore, to be able to achieve at least hundreds of 100 GΩs with pseudo-resistors, non-tunable structure is chosen. The impedance can be further increased by using 2 PMOS transistors in series [54], [56]. Another advantage of using 2 PMOS transistors in series is that improved linearity can be achieved by means of this structure. The aspect ratio is decided as 250nm/18μm which gives the (almost) smallest value for W/L for each device. As a result of this small aspect ratio, the highest possible resistance value is expected. This expectation is confirmed by the simulation results. The schematic view is given Fig. 2.18, and Fig. 2.19 shows the layout of the pseudo-resistor elements. In Fig. 2.19, the letter "A" represents the transistor M_a, whereas M_b is highlighted with letter "B".

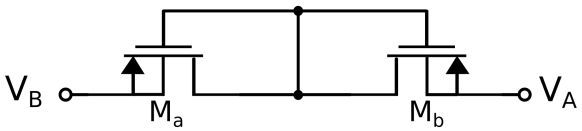


Figure 2.18: The schematic of pseudo-resistor designed in the system.

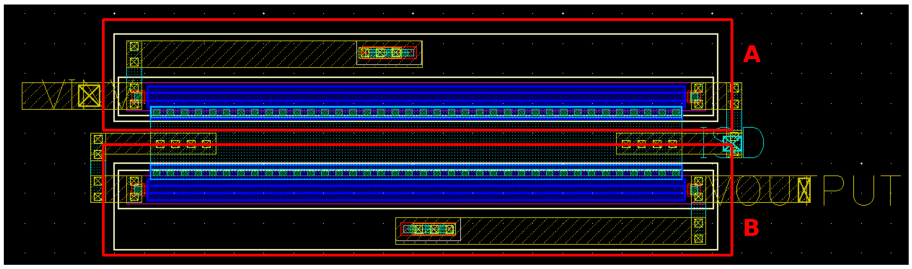


Figure 2.19: The layout view of pseudo-resistor elements designed in the system.

The schematic and post-layout simulation results of the resistance of pseudo-resistor elements are shown in Fig. 2.20. The resistance value is calculated as 688 GΩs with nominal transistors in schematic view. After laying out the devices, the resistance value is found as 763 GΩs. The reason of increased resistance value might be because of that the current that must flow through the channel may be directed to other nodes due to the parasitics. This might cause a decrease in current value which results in higher resistance values.

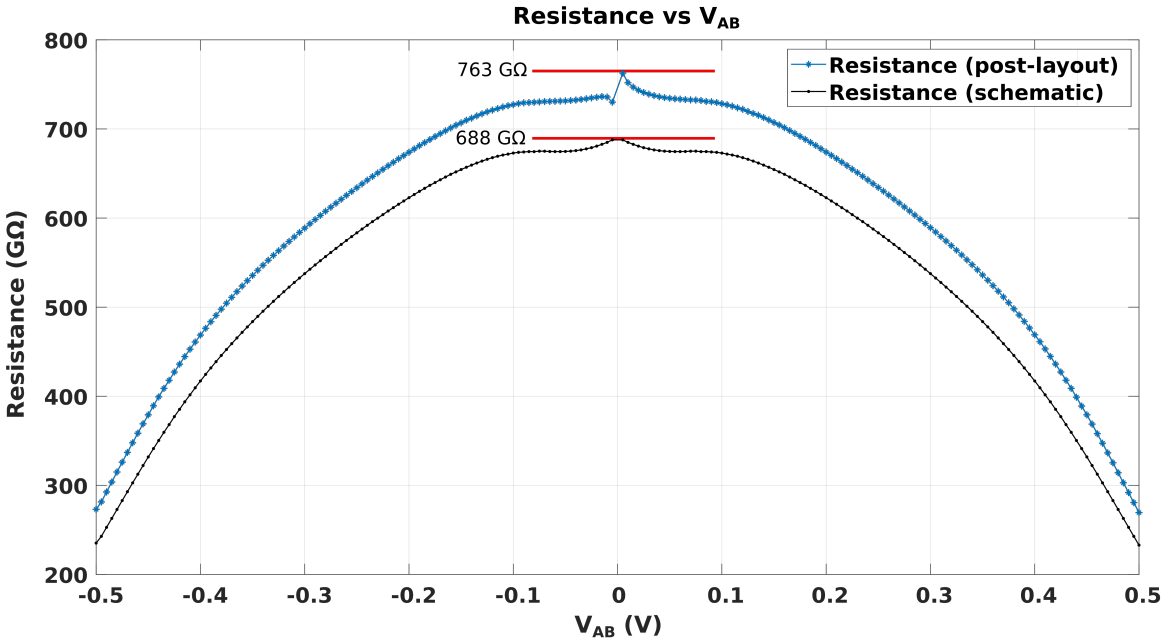
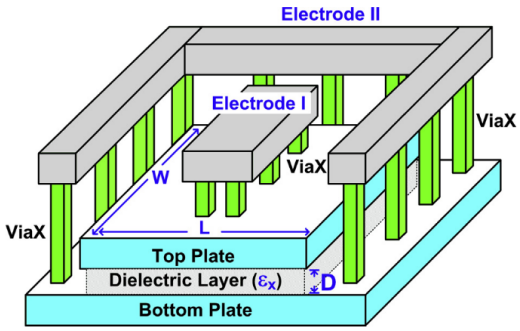
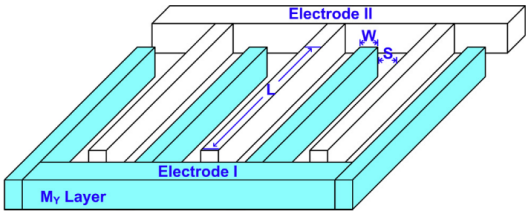


Figure 2.20: The comparison of schematic and post-layout simulation results of pseudoresistor elements.



(a) Schematic of MIM capacitor



(b) Schematic of MOM capacitor

Figure 2.21: The illustrations show MIM and MOM capacitor structures (Taken from [57]).

2.3.4. CCIA Capacitors

Capacitive feedback elements are the another critical sub-block in recording channel to be designed. In IC technology, three kinds of capacitance structures are widely used which are MOS capacitor, metal-oxide-metal (MOM) capacitor, and metal-insulator-metal (MIM) capacitor. MIM capacitors have a structure such that two parallel metal plates are insulated from each other with a dielectric material. MOM capacitor structures form the capacitance in metal interconnections in an interdigitated manner. The illustrations of these two kinds of capacitor are depicted in Fig 2.21 [57]. Due to the thin oxide layers in the gate, MOS capacitors provide the highest capacitance density among three structures. However, MOS capacitors show highly non-linear characteristics by their nature. Changes in gate voltage alter the gate capacitance. Also, they are very sensitive to process variations. As a result of that, MOS capacitors cannot be suitable for defining the ratio of C_s/C_f, so that the gain of the recording channel. This reduces the capacitance options from 3 to 2 as MOM and MIM capacitors.

There are two main important aspects of choosing the feedback capacitor value and type. The first aspect is that the cut-off frequency of the high-pass filter configuration. The cut-off frequency and the capacitor value is inversely proportional to each other. In other words, to increase the recording capability in a few Hz range, the capacitance value must be increased. However, this brings up one issue in terms of an increase in area occupation on silicon. Therefore, 100 fF is chosen as the feedback capacitance to achieve f_{HP} around a few Hzs in the presence of hundreds of GΩ of feedback resistance. Also, this makes the C_S 3 pF to maintain 30 V/V closed-loop gain in the recording channel. Among MOM and MIM capacitors, MIM capacitors provide the higher capacitance density per unit area which results in smaller area consumption. MIM capacitor models gives 1fF/1μm^2 capacitance density. 3 pF of C_s covers around 60 μm × 70 μm, when MIM capacitor (model: mimcap-2p0-sin) is used. The same capacitance value occupies around 80 μm × 80 μm area, when MOM capacitor (model: crtmom) is implemented. As a result of this analysis, MIM capacitor is chosen to implement the capacitors with 100 fF and 3 pF.

In order to have a good matching between capacitors C_f and C_S, C_f is placed in the middle in a 5 × 7 array of 100 fF unit capacitances. Since Cs is 30 × bigger than C_f, 30 of 100 fF unit capacitance forms 3 pF capacitance as C_s. In Fig. 2.22, C_f is highlighted with red box, whereas C_s is shown with green box. The unit capacitance at the edges of the array are dedicated as dummy capacitances to increase the matching. The 5 × 7 array of

100 fF unit capacitances occupies 78 μm × 68 μm on a die. The vertical interconnections of bottom-plate of capacitors are done by using METAL5, and horizontal interconnections which connects the top plates of capacitors are drawn by means of METAL6. Most of the interconnections are 2 μm in width unless the interconnection violates the DRC. Although wider than minimum-width interconnections cause larger area occupation, it is important to try to reduce the parasitics caused in long metal lines (up to 60 μm in length).

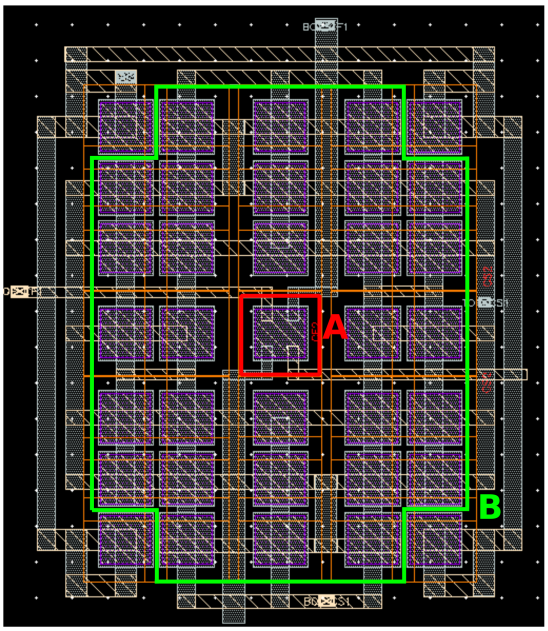


Figure 2.22: The layout view of capacitors C_s and C_f. The area occupations is equal to 78 μm × 68 μm.

3

Results

In the following Chapter, the performance of the recording channel is given by running DC, AC, noise and transient simulations on Cadence ADE L environment. DC, AC, and noise analyses were applied to both schematic and post-layout views of the system. Transient analysis results given here were obtained from post-layout views. The statistical results were obtained from schematic views of sub-blocks of the channel after running Monte Carlo (MC) process and mismatch simulations on Cadence ADE XL. The supply voltage was 1.8 V throughout all simulations.

3.1. DC Simulations

The setup configuration used in simulations of input-offset voltage (V_{os}) is given in Fig. 3.1. The operational amplifier (in schematic configuration) is used in open-loop configuration, and both inverting- and non-inverting-input of the amplifier is set to mid-supply 0.9 V. The resulting voltage at the output is simulated as 847 mV. The difference between the output voltage and mid-supply 0.9 is the output-referred offset voltage. Therefore, 53 mV is divided by the open-loop gain of the amplifier (45.5 dB) to find the input offset voltage which is 281 μV. The statistical analysis of input offset voltage of OTA is shown in Section 3.5.

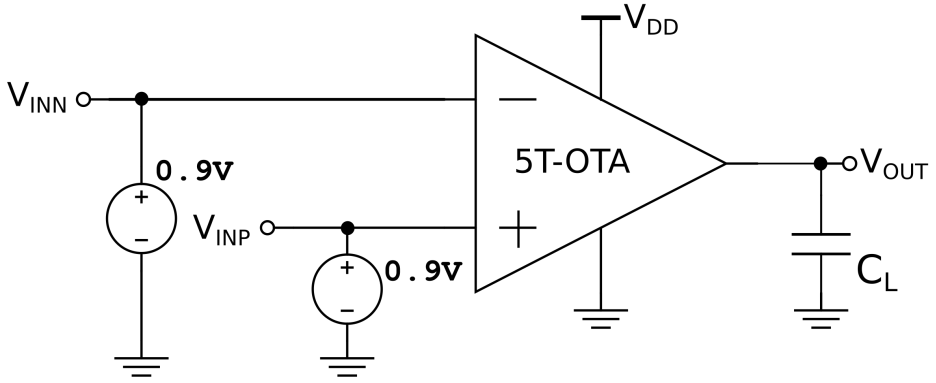


Figure 3.1: Setup configuration used in input-offset DC simulations.

The test bench used in DC simulations of the recording channel can be observed in Fig. 3.2. In this configuration, all switches are set to be inactive to simulate the power and current consumption, and input offset voltage when the recording channel is in quiescent mode. The power consumption is equal to 7.18 μW with a supply current of 3.99 μA. The transconductance of the OTA equals to 28.9 μA/V and as the same in schematic and post-layout simulations. The output resistance of the OTA (r_{out}) is equal to 6.72 MΩ in schematic views, whereas r_{out} is 6.63 MΩ in post-layout simulations. The output resistance of the channel (R_{out}) reaches to 6.95 MΩ with schematic views of all sub-blocks. The system-level output impedance R_{out} was estimated to be slightly lower in the case of post-layout simulations. The reason of not reporting the exact value of R_{out} in post-layout simulations is that DC operating points cannot be shown in this case in the simulator environment. The output DC voltage ($V_{o,os}$) is 450 mV in schematic simulations, whereas $V_{o,os}$ is found as 443 mV in the case of post-layout simulations (see Fig. 3.9). The output DC voltage sits at 443 mV instead of sitting at 0.9 V because COL_SEL was deactivated. There is a voltage drop as V_{DS} of NMOS transistor which is used as COL_SEL switch. Therefore, the voltage before COL_SEL switch is also inspected to assess the offset and voltage response of the recording channel carefully. Fig. 3.3 shows the transient response of the recording channel when MEA modality is followed by CC modality at the drain of COL_SEL switch. As it can be seen from the Fig. 3.3, the DC voltage at this node is 887 mV when there is no modality activated. Table 3.1 summarizes the obtained results after DC simulations. The transconductance, $I_{quiescent}$ and power/channel are the same for both schematic and post-layout simulations.

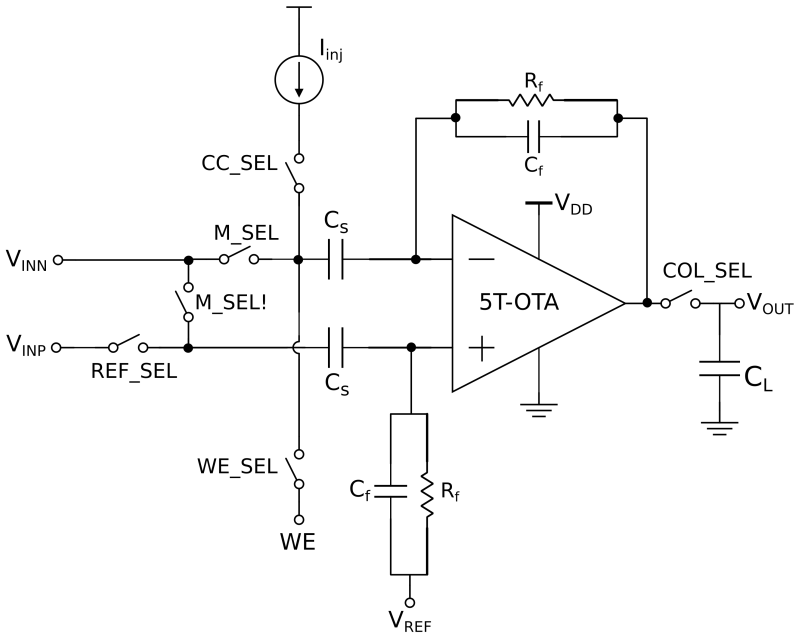


Figure 3.2: Setup configuration used in DC simulations of the recording channel.

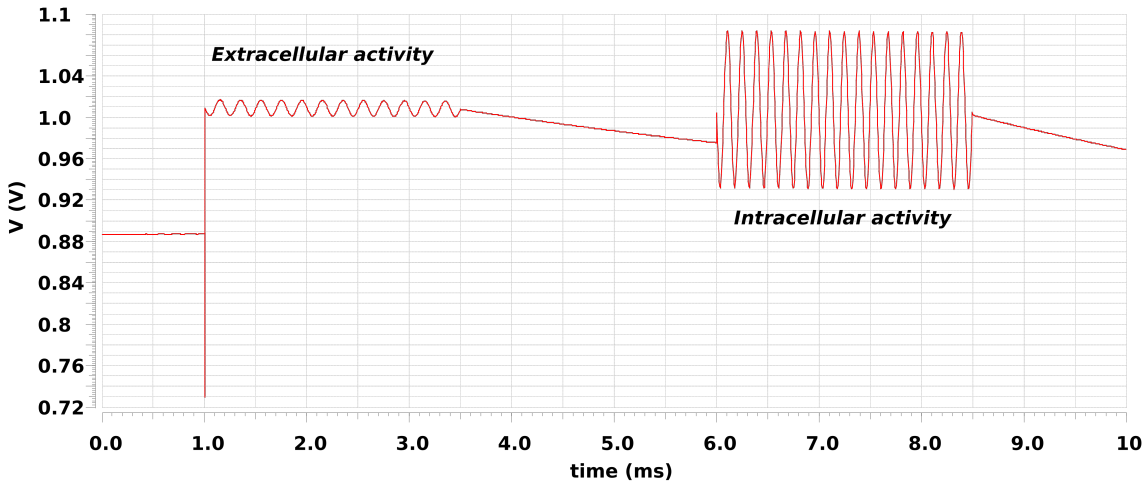


Figure 3.3: Transient analysis of the recording channel when MEA modality is firstly activated followed by CC modality. The voltage at drain of COL_SEL switch is shown here.

Table 3.1

Table of DC simulations Performance Comparison of Schematic and Post-layout			
Parameters	**Units**	**Schematic**	**Post-layout**
g_m	μA/V	28.9	28.9
r_{out} (OTA)	MΩ	6.72	6.63
R_{out} (System-level)	MΩ	6.95	< 6.95 (expected)
$V_{out,DC}$	mV	449.5	443
$I_{quiescent}$	μA	3.99	3.99
Power / Channel	μW	7.18	7.18

3.2. AC Simulations

The setup configuration used in the AC simulations for both schematic and post-layout views is given in Fig. 3.4. For simplicity, feedback resistances are shown as regular resistors, even though they are in pseudo-resistor configuration. The supply voltage V_{DD} is equal to 1.8 V, and V_{REF} is at mid-supply 0.9 V. The bias current is 2 μA. The AC magnitudes for V_{INN} and V_{INP} are 0.5 V and -0.5 V, respectively. The load capacitance is chosen as 200 fF of the gate capacitance of the next stage where it is assumed as output buffers.

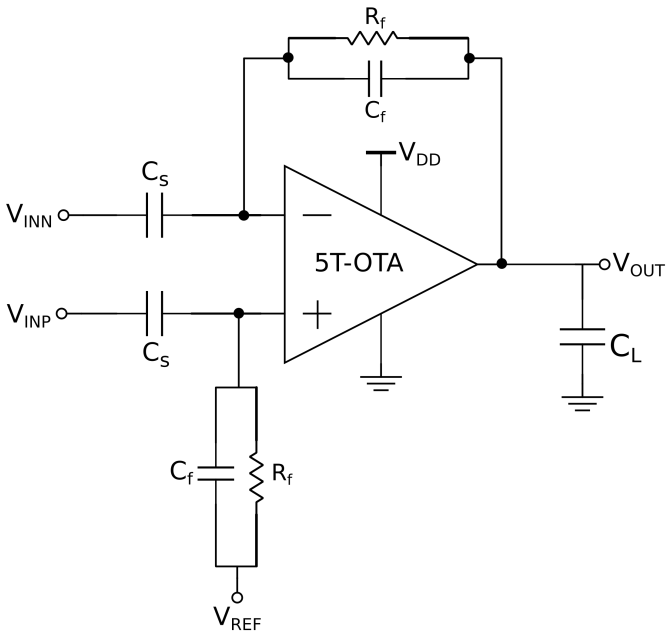


Figure 3.4: Setup configuration used in AC simulations.

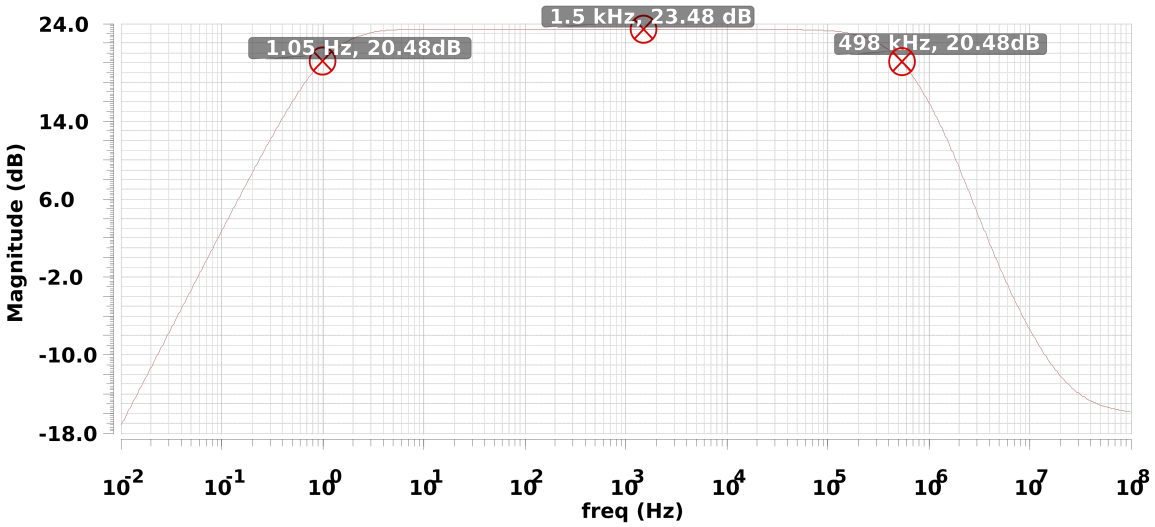


Figure 3.6: Post-layout simulation results of the total system.

The AC analysis results of schematic and post-layout simulations are given in Fig. 3.5 and Fig. 3.6, respectively. Table 3.3 summarizes the performance comparison between the schematic and post-layout AC simulation results. The cut-off frequency f_{HP} is equal to 1.2 Hz in schematic simulations, whereas it reduces to 1.05 Hz in post-layout results. According to hand-calculations, the high-pass cut-off frequency was calculated as 2.09 Hz where feedback capacitance was assumed as 100 fF and the post-layout results of resistance (763 GΩ) was used. The same calculations have been done for schematic views of the recording channel elements, and the cut-off frequency resulted as 2.51 Hz (C_f=100 fF, and R_f = 633 GΩ). To understand the reason of the difference between the schematic and post-layout simulation re-

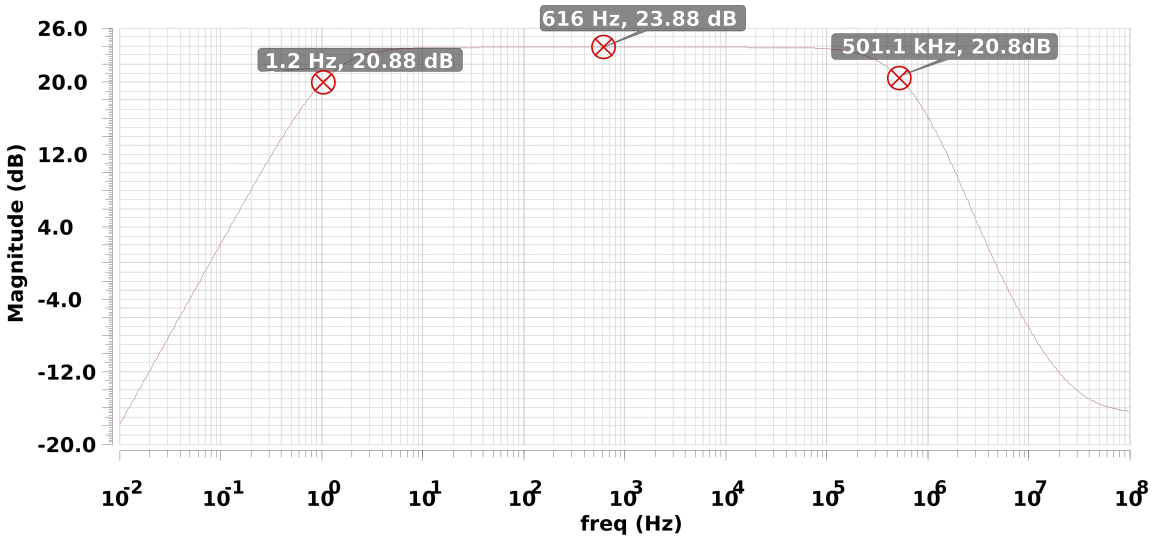


Figure 3.5: Schematic simulation results of the total system.

Table 3.2

Table of Performance Comparison of Schematic and Post-layout			
Contributors	**Type**	**% in Schematic**	**% in Post-layout**
Pseudoresistors	Thermal	42.23	38.07
Current mirror transistors	Flicker	10.03	10.96
Input transistors	Thermal	24.7	27.8
Input transistors	Flicker	19.91	23.02

sults, and hand-calculations, feedback resistance and capacitance were simulated separately with ideal circuit elements. To be more specific, feedback resistance (in calibre view on Cadence) was simulated in a configuration where the amplifier and the capacitances were ideal. By this analysis, f_{HP} resulted at frequency of 1.95 Hz which implies that the feedback resistance reached up to 816 GΩ. The reason why f_{HP} equa1s to 1.05 Hz in post-layout simulations is that the capacitance value reaches to 186 fF instead of (ideal) 100 fF. Parasitic capacitance of 86 fF has found where the amplifier is the main contributor to the input parasitic capacitance because of its wide transistors (W/L = 180 μm / 1 μm) in the input. The effect of input parasitic capacitance was also seen in achieved gain. The capacitance C_s / C_f is supposed to define the gain of closed-loop gain, and this value is 30 V/V. Instead of having a ratio as C_s / C_f, the gain approaches to $C_s/(C_f+C_{parasitics})$ which is equal to 24.15 dB. The resulting gain is 23.5 dB in the post-layout results.

3.3. Noise Simulations

The same setup shown in Fig. 3.4 was used in noise simulations. The input-referred noise in μV_{rms} is also given in Table 3.3. Although the gain of the amplifier is decreased to 23.5 dB from 23.9 dB, and the high-cut-off frequency becomes lower in post-layout simulations (1.05 Hz) than that of schematic results (1.2 Hz), there is an improvement seen in the input-

Table 3.3

Table of Performance Comparison of Schematic and Post-layout			
Parameters	**Units**	**Schematic**	**Post-layout**
f_{HP}	Hz	1.2	1.05
f_{LP}	kHz	500	498
Gain	dB	23.9	23.5
GBW	MHz	7.8	7.5
Input-referred noise (Full band)	μV_{rms}	30.2	30.3
Input-referred noise (AP-band)	μV_{rms}	8.3	8.09
NEF (Full-band)	–	3.3	3.3
NEF (AP-band)	–	6.4	6.2

referred noise value. The reason of lower input-referred noise can be explained by the fact that the contribution of the pseudo-resistors to the total noise is reduced. The current flowing the pseudo-resistors channel might be decreased in the post-layout configuration, so that causing an increase in the resistance value. Therefore, this might be the reason of the increase in the noise performance of the channel. The noise contributors and their percentages with noise types are given in Table 3.2.

The input-referred noise of the recording channel is obtained as 8.1 μV_{rms} in frequency band ranging from 1.05 Hz-10 kHz (AP-band) for post-layout simulations. As it can be seen from the equation Eq. 3.1, there is a certain trade-off between power consumption and noise. Noise efficiency factor (NEF) introduces this trade-off with numbers as in Eq. 3.1 [47].

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{3.1}$$

In this equation, $V_{ni,rms}$ represents the input-referred noise in a certain bandwidth in Hertz (BW), and I_{tot} is the total current used in the amplifier. When we substitute the suitable numbers from Table 3.3, NEF resulted as 3.3 in the full-band for the amplifier bandwidth for schematic and post-layout simulations, respectively. However, it is also important to calculate NEF for AP-band, since the valuable content of electrical signals are buried in this band. In the case of AP-band NEF increases to the 6.4 and 6.2 for schematic and post-layout simulations, respectively. The theoretical limit for NEF is reported as 2.02 [58] when only thermal noise is taken into account for NEF calculations.

Table 3.4

Table of Positions of the Switches in CC- and MEA-modality		
Switches	**CC-Modality**	**MEA-Modality**
MEA_SEL	OFF	ON
MEA_SEL!	ON	OFF
CC_SEL	ON	OFF
REF_SEL	ON	ON
WE_SEL	ON	OFF
COL_SEL	ON	ON
B	ON	OFF
B!	OFF	ON

3.4. Transient Simulations

The test bench configuration for transient analysis is given in Fig. 3.7 (same as in DC simulations). As usual, the supply voltage V_{DD} is set to 1.8 V, whereas V_{ref} is set to 0.9 V. For simplicity, the current injector is shown as a current source as I_{inj}. Resistance R_f corresponds to pseudo-resistors. All switches are shown in test bench are implemented as NMOS transistors in minimum size (W / L = 220 nm / 180 nm). For WE input, there is a sinusoidal voltage source which generates a signal in 5 mV in amplitude and 10 kHz in frequency (see Fig. 3.8 from 1 ms to 3.5 ms). To represent the reference electrode, an input signal with 100 μV amplitude and 10 Hz frequency is placed at node V_{INP}. . Input signal (see Fig. 3.8 from 6 ms to 8.5 ms) with 500 μV in amplitude and 1 kHz in frequency is applied to V_{INN}.

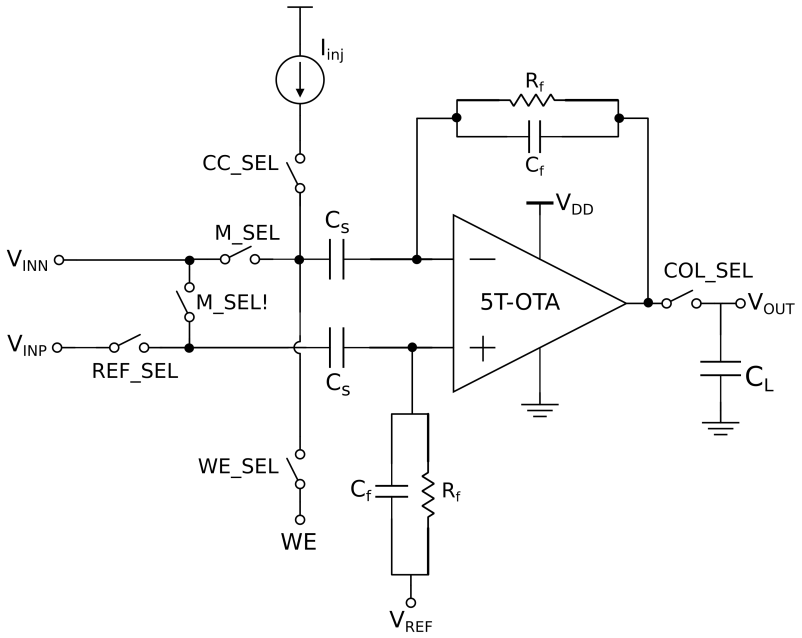


Figure 3.7: Setup configuration used in transient simulations of the recording channel.

Fig. 3.8 shows the switch activity of the switches MEA_SEL, REF_SEL, and CC_SEL.

Firstly, the CC modality is tested followed by MEA modality. In order to operate in CC modality, the PMOS switch of CC_SEL is activated. At the same time, REF_SEL NMOS switch is turned on, as it can be seen in Fig. 3.8. The resulting output signal can be observed in Fig. 3.9 from 1 ms to 3.5 ms. Then, the same channel is reconfigured for MEA modality at 6 ms of transient analysis. When CC-modality is turned off, switch REF_SEL was deactivated. To connect reference electrode to the non-inverting node of the channel, REF_SEL is activated with switch MEA_SEL. The simulated output voltage is given in Fig. 3.9 from 6 ms to 8.5 ms. For simplicity, not all the switch activities are shown as signals. The position of the all switches for each modality was given in Table 2.1. The smallest input signal in amplitude that can be recorded is 100 μV. The simulation result is given in Fig. 3.10.

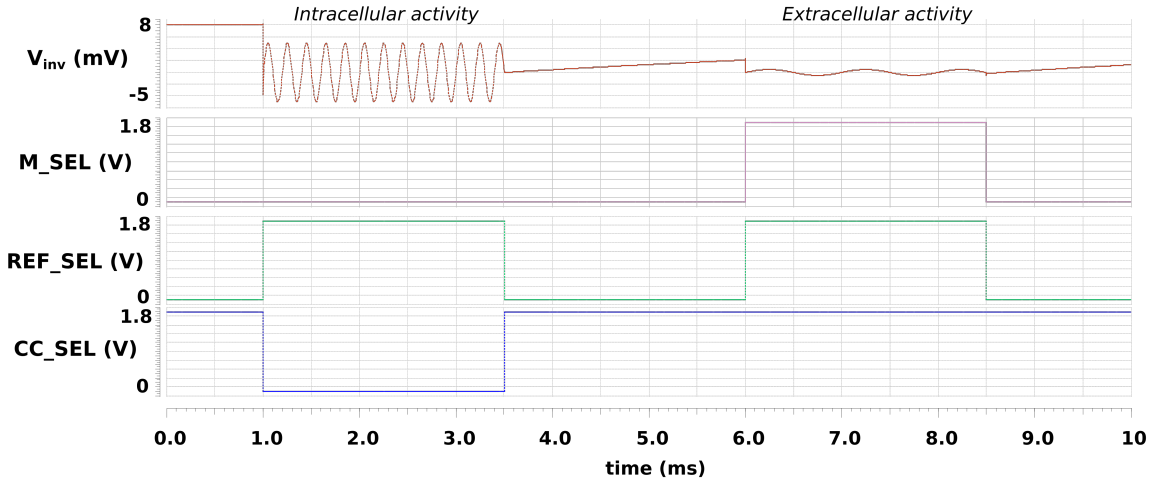


Figure 3.8: Transient analysis of the inverting node signal and switches MEA_SEL, REF_SEL, and CC_SEL.

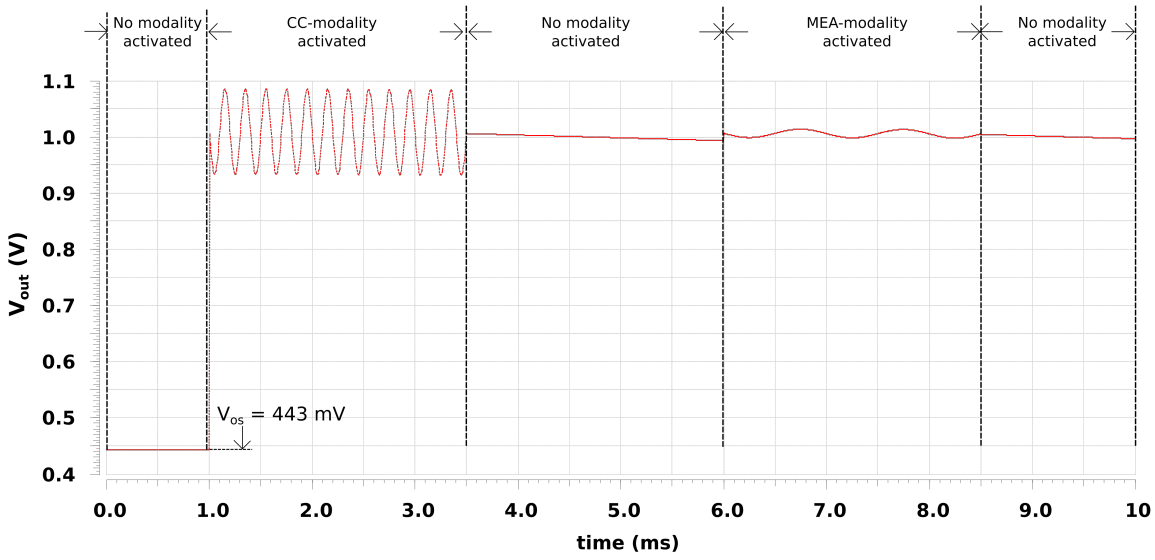


Figure 3.9: The resulting output voltage after transient analysis is applied in the switch conditions demonstrated in Fig. 3.8.

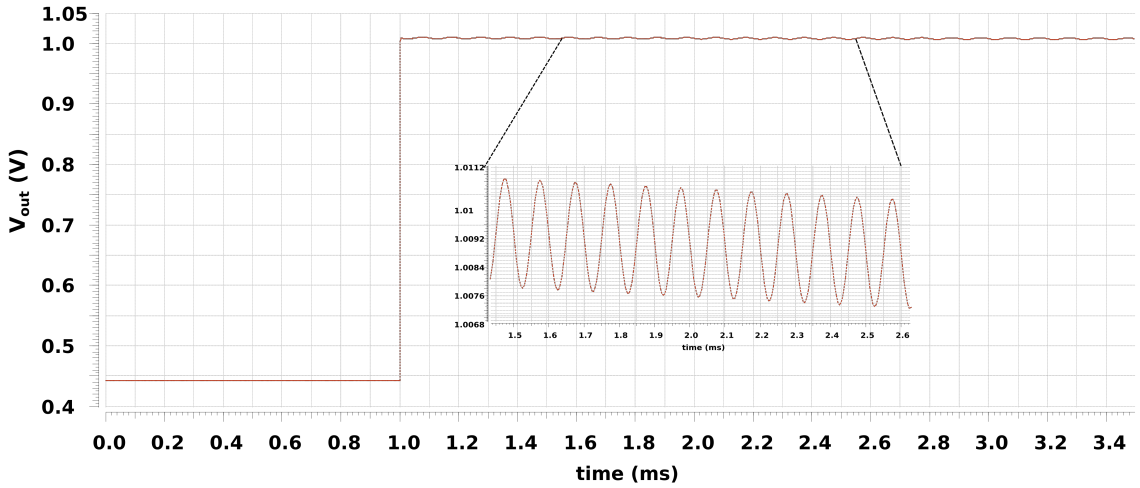


Figure 3.10: The resulting output voltage after 100μV with 10 kHz frequency of input signal is applied to V_{INN}. Inset figure shows zoomed-in view of the signal.

As it can be seen from Fig. 3.9, the DC output voltage does not sit at around 0.9 V. There is 100 mV DC offset at the output causing the output DC voltage is set to around 1 V when one of the modalities is being activated. The reason of such an offset voltage at the output can be explained by the presence of leakage current (2.9 pA) flowing from the unit current source which is charging the top plate of the input capacitance C_S. When the same amount of the leakage current is applied to top plate of C_S in the opposite direction as compensation current, DC voltage sits at around 0.9 V. This result is given in Fig. 3.11.

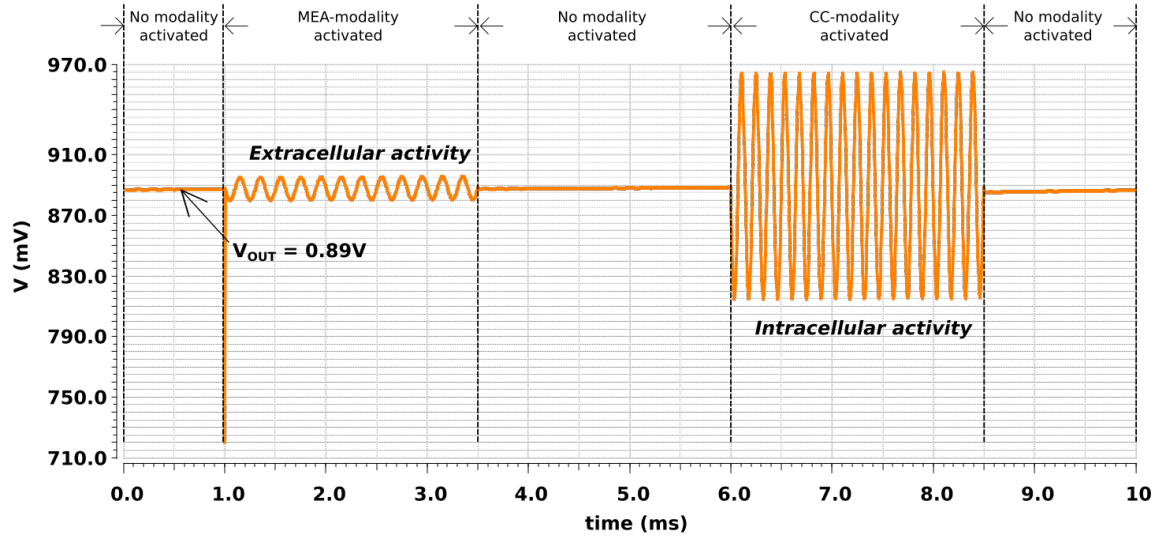


Figure 3.11: Transient analysis of the recording channel when compensation current (2.9 pA) is applied to the top plate of C_S.

3.5. Statistical Results

In order to test the robustness of the channel, Monte Carlo (MC) process and mismatch simulations are applied separately with 200 samples for each type of simulations. The MC simulation results are shown in here as histograms with bins of 10. MC process simulations take variations in technology parameters into account across the silicon wafer. For instance, gate-oxide thickness (t_{ox}) can vary in different regions of the wafer. An example of t_{ox} variations is given in Fig. 3.12. The variations in t_{ox} changes the threshold voltage of transistors, which affects the behaviour and performance of the devices. Apart from process variations, mismatch variations between devices is an important concern in IC design. The layout techniques such as common-centroid patterns can minimize the device mismatches, but cannot cancel them completely. MC mismatch simulations provide insight of the effects of these slight variations. Thus, MC analysis gives a realistic performance estimation of the devices based on statistical distribution when mismatch and process variations occur over a wafer.

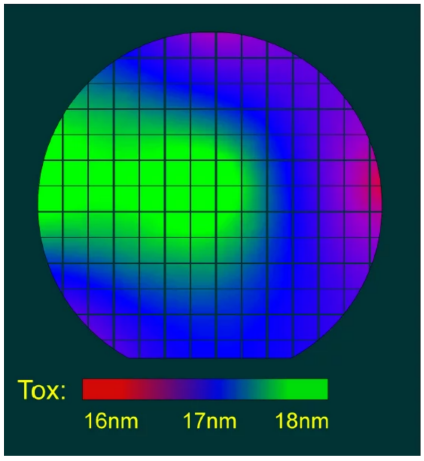


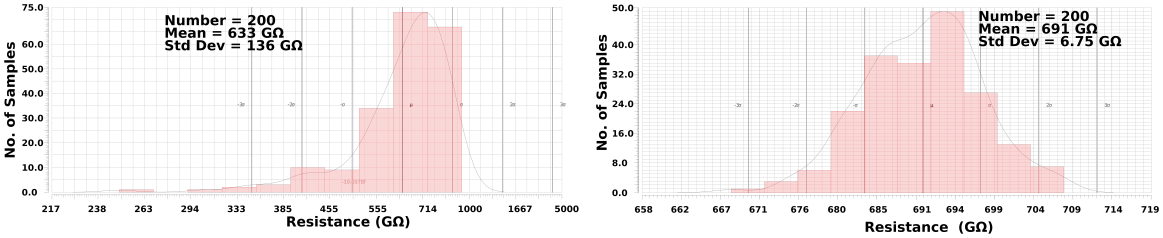
Figure 3.12: An example of variations of oxide thickness (t_{ox}) occurring across a wafer (Taken from [59]).

Firstly, MC analysis was applied to the pseudo-resistor elements. The voltage at node B is set to 900 mV, where as V_A is 0.905 mV (see Fig. 2.18). The current at node A is the value that is under MC process and mismatch simulations. The voltage difference between node A and B (V_{AB}) 5 mV is divided by the current at node A to find the resistance value of the pseudo-resistor elements. According to the MC process simulations, the mean value of pseudo-resistors is found as 633 GΩ with standard deviation of 136 GΩ. These results are depicted in Fig. 3.13a. Under MC mismatch variations, the resulting mean resistance of pseudoresistors is 691 GΩ, and standard deviation is less than %1 which is 6.75 GΩ. The MC mismatch results can be found in Fig. 3.13b.

As it has been stated in Table 3.3, the cut-off frequency of high-pass filter configuration is obtained as 1.05 Hz. The standard deviation in MC process of pseudoresistors is found as 136 GΩ, and it shows a pattern to be less resistant. Thus, the pseudoresistor might become 497 GΩ due to the process variations. When the nominal model of pseudoresistors is used in the feedback path (see Section 3), the resistant value is found as 815 GΩ in the case of 633 GΩ is expected. If we assume that there is direct proportion between the calculated resistance

Table 3.5

Summary of the resulting f_{HP} (Hz)		
Best-case scenario	**Mean value**	**Worst-case scenario**
0.85 Hz	1.05 Hz	1.9 Hz



(a) Histogram of Monte Carlo process simulation results of pseduoresistor elements.

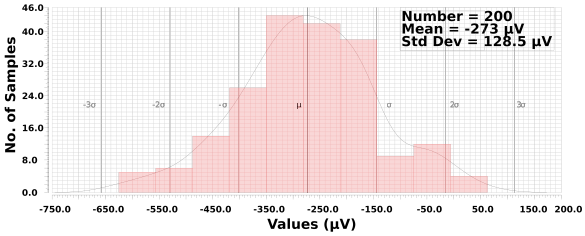
(b) Histogram of Monte Carlo mismatch simulation results of pseduoresistor elements.

Figure 3.13: The resulting histogram graphs of pseudo-resistor elements after MC analyses.

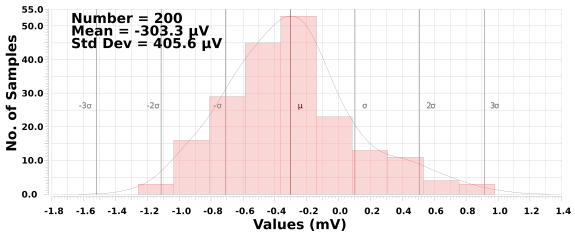
and the simulated resistance, then for 497 GΩ with 1σ deviation, the resulting resistance will be 639 GΩ when used in the feedback path. The change in resistance will reflect on the high-pass cut-off frequency as a 0.29 Hz change. In other words, the cut-off frequency becomes 1.34 Hz when process variations are dominant across the wafer. If the 3σ deviation is taken into account, then the resulting resistance of pseudoresistor reduces to 450 GΩ. In the case of 450 GΩ resistance, the cut-off frequency becomes 1.9 Hz, and this can be seen as the worst case scenario. On the other hand, if the best-case scenario is considered, then the cut-off frequency is improved to 0.85 Hz in the presence of 800 GΩ of resistance. The mean and best possible resistances provide an f_{HP} that is also compatible in the state-of-the-art (see Table 4.1). Note that MC mismatch variations give less than 1% deviation in 1σ which reflects less than 1% change in f_{HP}. Therefore, it can be neglected where process variations are much more dominant (more than 20% in resistance value).

Another MC process and mismatch analysis has run to simulate the input offset voltage of the OTA as it was promised in Section 3.1. The same setup configuration (see Fig. 3.1) and calculation method was used to obtain V_{os}. MC process simulations show in Fig. 3.14a that the mean value of V_{os} is -273 μV where the standard deviation is 128.5 μV. When MC mismatch simulations have run, the mean voltage value of V_{os} equals to -303 μV, and standard deviation is 405 μV in this analysis. The results of MC mismatch simulations are given in Fig. 3.14b.

To simulate the common-mode gain, both input nodes of the OTA are shorted together, and the DC level is set to 0.9 V, and the common AC signal with 1 V amplitude is applied. The resulting MC process analysis reflects that the mean value of common-mode gain is -36.9 dB, and standard deviation is simulated as 2 dB. According to the MC mismatch simulations, the mean value of common-mode gain is -29 dB, where it deviates from the mean value as much as 10 dB. Histogram graphs of both MC process and mismatch analysis can be observed from Fig. 3.15a and Fig. 3.15b, respectively. The MC process and mismatch simulations run for the differential gain of the OTA, too. The standard deviation is less than 1 dB for both type of simulations, and they are found as 246 mdB and 639 mdB, respectively. The MC process

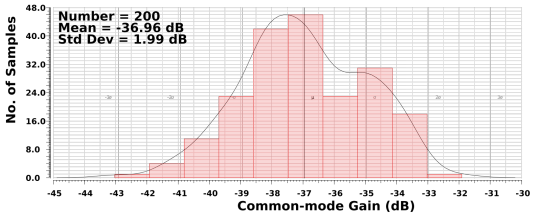


(a) Histogram of Monte Carlo process simulation results of V_{os}.

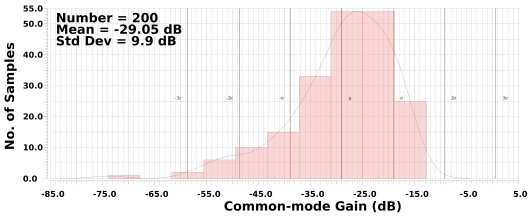


(b) Histogram of Monte Carlo mismatch simulation results of V_{os}.

Figure 3.14: The resulting histogram graphs of V_{os} after MC analyses.



(a) Histogram of Monte Carlo process simulation results of common-mode gain.



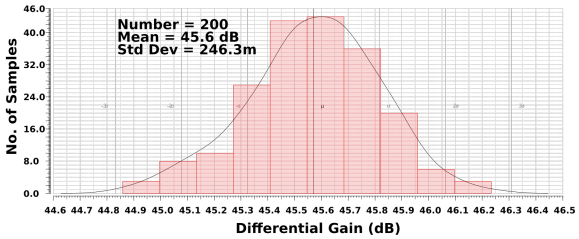
(b) Histogram of Monte Carlo mismatch simulation results of common-mode gain.

Figure 3.15: The resulting histogram graphs of common-mode gain after MC analyses.

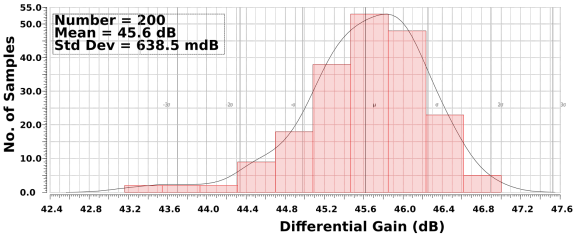
results are given in Fig. 3.16a, whereas Fig. 3.16b depicts the MC mismatch results. Common-mode rejection ratio (CMRR) shows the efficacy of a differential amplifier in terms of rejection of the amplifier to the common-mode signals. The CMRR of an amplifier is given by Eqn. 3.2 [51]. When CMRR is analysed in 1 σ deviation, CMRR of the amplifier is calculated around 64 dB as in the worst-case scenario (the worst differential gain combined with -20 dB A_{cm}), and around 84 dB when the best-case scenario (the best differential gain combined with 37 dB A_{cm}) is taken into account.

$$CMRR = 20log\frac{|A_d|}{|A_{cm}|} \tag{3.2}$$

The characterization table of current DAC was given in Chapter 2 in Section 2.3.2. The calculations of characteristics of the current DAC (DNL, INL, offset error, and gain error) are



(a) Histogram of Monte Carlo process simulation results of differential gain.

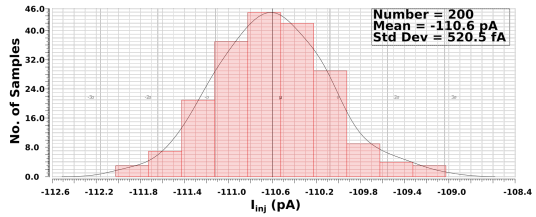


(b) Histogram of Monte Carlo mismatch simulation results of differential gain.

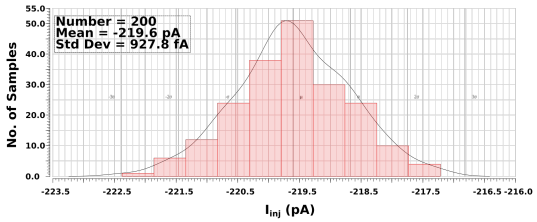
Figure 3.16: The resulting histogram graphs of differential gain after MC analyses.

Table 3.6

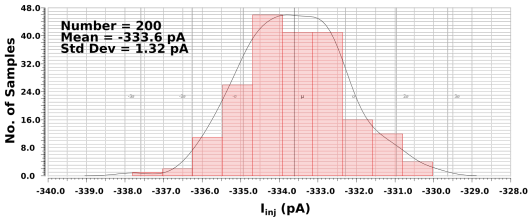
Summary of the resulting current values of DAC after MC process and mismatch simulations				
Digital input code	**Min**	**Max**	**Mean**	**Std. Dev.**
0001	109 pA	112 pA	110.6 pA	520.5 fA
0010	217.2 pA	222.4 pA	219.6 pA	928 fA
0011	330 pA	337.8 pA	333.6 pA	1.3 pA
0100	446.7 pA	457.5 pA	452 pA	1.78 pA



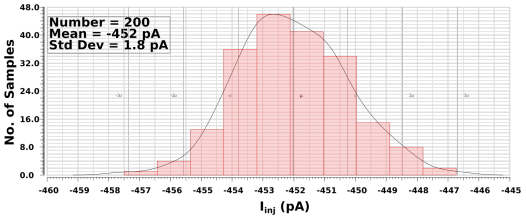
(a) MC process and mismatch simulation results of I_{inj}, when the digital input code is "0001".



(b) MC process and mismatch simulation results of I_{inj}, when the digital input code is "0010".



(c) MC process and mismatch simulation results of I_{inj}, when the digital input code is "0011".



(d) MC process and mismatch simulation results of I_{inj}, when the digital input code is "0100".

Figure 3.17: The histograms of MC process and mismatch simulations of current DAC.

based on the mean values of resulted currents after MC process and mismatch simulations. 4 of unit current sources were shorted together and MC analyses were applied as it has been stated in Chapter 2. Therefore, the histogram graphs of MC process and mismatch simulations with digital input codes from "0001" to "0100" are presented in Fig. 3.17a- 3.17b- 3.17c- 3.17d, respectively. The mean current values were resulted at 110.6 pA, 219.6 pA, 333.6 pA, and 452 pA for the digital input codes from "0001" to "0100", respectively. Table 3.6 presents not only mean values, but also shows minimum/maximum values and standard deviation of current values for the first 4 digital input code (after "0000").

4

Discussion

Understanding cell activities in extracellular-level requires investigation of characteristics of single-cells in real-time and in array operation, since extracellular field potentials are results of synchronous activity of many single-cells. Moreover, the collective activity of many cells may result in a decrease in the transmembrane voltage of a single-cell [43]. The studies that tried to understand the correlation or anti-correlation between a single-cell and population of cells used MEA platforms and conventional patch pipettes as separate tools [60],[44] as it was shown in Fig. 1.11 [44] in Chapter 1. Therefore, such a measurement setup used bench-top system (Multiclamp 700B) which is bulky and expensive. Also, parallel execution of single-cell experiments is not possible. Extracellular measurements are done by MEA2100 which is a commercial MEA-system [44]. In this project, we propose a system that enables concurrent in-vitro measurements of extracellular and intracellular recordings on the same platform. The proposed system eliminates the need of using two different tools with their amplifiers and data acquisition systems for both type of modalities. The envisioned μTAS offers the stand-alone silicon wafer platform that allows to culture cells atop it. Moreover, the dual-mode recording unit can record both intracellular and extracellular potentials by reconfiguring itself by means of minimum-sized NMOS switches.

The channel-array offers an opportunity of that each channel can be reconfigured independently. It means that it is not only possible to operate 16 channels in either MEA-modality or CC-modality, but also different modalities can be chosen for different areas of the array. The channel-array can realize 16 single-cell experiments on one run which is already higher than the throughput of conventional patch-clamp systems which can carry out around 10 single-cell experiments per day [61]. Assuming that all 16 micropores can trap a cell when a suction is applied, and a different cell is captured for each micropores for the next applied suction, then the throughput can reach to thousands of single-cell experiments. Moreover, for example, the channel-array can be reconfigured as one of the channels operate in CC-modality, while the other channels are in MEA-mode. This gives the opportunity to understand the impact of a single-cell firing AP on extracellular field potentials as well as to have significant insight into effect of extracellular field potentials on a hyperpolarization of a single neuron it has been mentioned above and in Chapter 1.

In this project, the dual-mode reconfigurable recording unit mainly consists of capacitively-coupled instrumentation amplifier and unary-weighted current DAC. By means of CCIA, the

electrode offset and drift voltages are cancelled. Given that, the supply voltage is 1.8 V, it is important to reject offset of electrodes which can go up to 1 V as it is stated in Section 2. Single-stage 5T-OTA forms the core of AC-coupled front-end amplifier. Single-stage configuration avoids using Miller capacitance and nulling resistor for stability concerns. Single-ended OTA does not require another CCIA capacitor in the feedback path by the expense of full-swing at the output. These two design choices contributes lower area consumption which is beneficial for targeted multi-site and high throughput array operation. NMOS transistors in subthreshold region are used as the input pair of the OTA. Using PMOS transistors as the input pair is beneficial for flicker noise concerns since PMOS transistors have intrinsicly lower flicker noise than NMOS transistors. However, aspect ratio (W/L) of a PMOS transistor must be more than 3 times higher than that of a NMOS transistor when the same amount of current is used as the tail current with the same *IC*. For example, for 2 μA tail current and *IC* of 0.01 would result in around 600 μm/ 1 μm aspect ratio for a PMOS transistor. In our design, *IC* of 0.01 is applied to the NMOS input pair which has 180 μm / 1 μm aspect ratio. Each recording channel (with current DAC) occupies 145 μm × 145 μm (0.021 mm^2) silicon area. PMOS input pair has been utilized by Harrison et. al. [47], and the neural amplifier in that study consumes 0.16 mm^2 of silicon area having 800 μm / 4 μm sizes for the input pair which is not suitable for multi-array operations. Harrison et. al succeeded to achieve 2.1 μV_{rms} input-referred noise, however the power consumption for a single neural amplifier goes up to 80 μW with tail current of 8μA (see Table 4.1).

A 16-channel array operation can be done with dimensions of 145 μm × 145 μm of an individual array on a 1 mm× 1 mm die. More than half of area is occupied by passive CCIA capacitors. The CCIA capacitors cover area of 80 μm × 140 μm on silicon. Using passive circuit elements such as capacitors in IC is a clear limitation for high-array operations. One solution to mitigate this issue which limits larger amount of channels on silicon might be utilizing the capacitors on top metal layers, and placing electronics underneath. This alternative layout was implemented by Abbott et. al. [42] in their most recent study. The implications of such a layout must be investigated since it might introduce significant parasitics which can have an influence on the performance of the amplifier.

The recording channel aims to amplify low-amplitude extracellular potentials while the intracellular action potentials from patch-clamp electrodes do not exceed the supply voltage (avoids clipping) due to high amplification factor of the channel. The signal amplitudes higher than 100 μV happening on top of the planar MEA electrodes can be recorded by means of the channel. The intracellular action potentials/subthreshold synaptic events at working electrode are also amplified to the output for further process. Therefore, the transient simulation results show promising evidence of that dual-mode reconfigurable recording channel is capable of amplifying both type of electrical activities. Although the recording channel shows promising results to capture both extracellular and intracellular signals of the cells, the gain and bandwidth of the amplifier are not reconfigured particularly for each type. For instance, when the recording channel is reconfigured for CC-modality, the bandwidth requirement is not as strict as it is in MEA-modality where 0.1 Hz level for high-pass cut-off frequency is targeted. The frequency for subthreshold events and AP ranges from 300 Hz to 10 kHz as it is stated in Table 1.1. Tuning high-pass cut-off frequency from sub-Hz to 300 Hz for CC-modality would also decrease the input-referred noise and improve NEF, since the bandwidth would range in a smaller window. Apart from bandwidth tuning, the gain of the amplifier could be a characteristic to tune for MEA-modality. The signal amplitudes reduces to hundreds of μV range in

extracellular recording with planar electrodes (see Table 1.1). The gain can be tuned to higher values to be able to record more silent extracellular signals such as ranging sub 100μV.

In the light of nominal and MC process simulation results (see Table 3.5), it can be guaranteed that the recording channel is able to cover the AP-band, and almost all extracellular activity-band with around 0.85 Hz difference between the mean values (1.05 Hz) and worst-case scenario (1.9 Hz) (see Table 1.1). The best-case scenario gives high-pass cut-off frequency of 0.85 Hz which would possibly provide more information on low-frequency activities unless flicker noise becomes too dominant to obscure the valuable content of potentials. In order to further increase the resistance in the feedback path, more than 2 long PMOS transistors can be used with compromising the more area occupation.

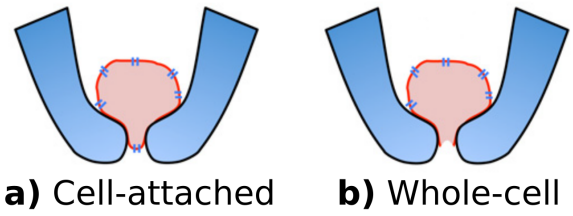


Figure 4.1: Different patch-clamp techniques a) Cell-attached configuration b) Whole-cell configuration (Adapted from [8])

One of the unique features of the proposed architecture is that it implements a localized current source for each working electrode for stimulation of the cultured cells. The DAC was implemented in unary-weighted configuration rather than binary-weighted configuration. Unary-weighted DAC guarantees monotonicity, while binary-weighted DAC might show non-monotonic behaviour because of nonlinearities occurring in layout design and fabrication processes [52]. Therefore, utilizing unary-weighted DAC ensures that the injected current will increase by activating adjacent current sources to make a trapped cell in apertures of μTAS generate an AP or synaptic potentials. In addition to monotonicity, unary-weighted DAC offers relaxed matching requirements [52] between the unit sources which is promising to reduce the time required for schematic and layout design of the DAC. Although large PMOS transistors (60 μm / 10 μm) are used to ensure matching between the transistors and to increase the linearity of the DAC, it occupies 56.5 μm × 44 μm silicon area which still makes the recording channel fall in the area specifications. For example, in [37], the injection current is 100 pA_{pp}, and the current injection circuitry covers around area of 0.5 mm × 1 mm on a silicon die as it is estimated from the die micrograph of the amplifier (see Fig. 1.7 in Chapter 1). Moreover, both DNL and INL of the DAC is less than 0.5 LSB, thus targeted 4-bit resolution is maintained by this architecture of DAC.

Table 4.1

Table of Performance Comparison in MEA Technologies									
Parameters	**Units**	**TBCAS, 2015 [62]**	**TBCAS, 2016 [63]**	**JSSC, 2003 [47]**	**TBCAS, 2015 [64]**	**JSSC, 2018 [27]**	**TBCAS, 2007 [46]**	**JSSC, 2020 [42]**	**This Work**
Technology	μm	0.35	0.18	1.5	0.13	0.13	0.35	0.18	0.18
Supply	V	3	1.8	2.5	3.3	3.3	3.3	N/A	1.8
No. of Channel	256	–	100	1	144	1024	256	4096	16
Gain	dB	53-72	52-66	40	23.5	6-69.5	46-74	29.5-49	23.5
C_{in}	pF	4	4	20	11.2	29.1	xx	3.5	3
f_{HP}	Hz	10	1	0.5	0.5	300	10	1	1.05
f_{HP} (min)	Hz	0.1	0.1	0.025	0.5	0.5	0.1	1	0.85
f_{LP}	kHz	5	10	7.2	10	10	10	30	498
Noise (AP-band)	μV_{rms}	7.99	4.07	2.1	12.7	7.5	13	5.6	8.1
NEF (AP-band)	–	8.99	3.51	3.8	N/A	N/A	N/A	N/A	6.2
Power (Total)	μW	12.9	9.1	80	165 (pxl OA)	95	6	1250	7.18
Area (Pxl/Channel)	mm^2	0.04	0.03	0.16	N/A	3.7 (4096 pxl)	N/A	0.025	0.021
Die Size	mm^2	12.8	13.4	0.16	0.128 (9 pxls)	192	13.5	200	2.25

Table 4.2

Table of Performance Comparison in Patch-Clamp Technologies						
Parameters	**Units**	**Multiclamp 700B [38]**	**MWSCAS, 2011 [16]**	**JNP, 2014 [36]**	**Nature El., 2019 [37]**	**This Work**
Technology	μm	N/A	0.5	0.35	0.18	0.18
Supply	V	N/A	3.3 V	N/A	3.3	1.8
No. of channel	–	N/A	4	1	1	16
CC Gain	V/V	50 MΩ - 5 GΩ	1	4	1	23.5 dB
Injected current range	A	a few p - 200 n	less than 1 n	-5 p - 128 n	100 p_{pp}	100 p - 1.6 n
Input-referred voltage noise	μV_{rms}	N/A	150	8.2	20	8.1
Power/channel	W	30	30m	N/A	7 m	7.18 μ

The resulting output current of the DAC when the digital input code is "1111" is 1.67 nA instead of 1.5 nA (with gain error of 0.11 LSB, see Section 2.3.2). Taking the current-clamp studies in the literature account where injected currents can go up to hundreds of nA (e.g. in [36]), it is most likely that 170 pA difference would not be fatal, while the cell membrane can maintain their structure (not removing the membrane). This configuration is called as cell-attached configuration (see Fig. 4.1a) [8]. However, when the recording array scales up to thousands of units, the accumulated leakage current might rise issues such as applying very high current to cells. The high stimulation currents might cause fatal consequences for cultured cells. For instance, for a 1024-channel recording array, when all current injection nodes are shorted together, even 1 pA of leakage current from each source would result in around 1 nA current in total. The current range (100 pA - 1.5 nA) is decided on by assuming cultured cells can be trapped in flip-tip pores and cell membrane in that pore (around 2μm) might be removed by means of applied suction (whole-cell recording configuration) (see Fig. 4.1b) [8]. If cell-attached configuration is achieved, then reference current I_{ref} must be increased to higher values than 100 pA since it is an external source.

The value of NEF (6.2 in AP-band) in our design for total input-referred noise (thermal and flicker noise) is compatible in state-of-the-art where NEF ranges from around 3 to 9 (see Table 4.1). The proposed recording channel uses the smallest input capacitance among other studies shown in Table 4.1. The input capacitance is kept as 3 pF to avoid from large area

occupations. However, relatively lower input capacitance (C_S) limit us to use larger input transistors to lower the flicker noise of these transistors. For example, in [64], the same gain value (23.5 dB) is achieved when 11.2 pF input capacitance is used. The input-referred noise spectral density is measured and reported as 12.7 μV_{rms} in the frequency range from 0.5 Hz to 10 kHz. The noise gain could have been further improved by using smaller feedback capacitance (C_f) instead of 0.68 pF to achieve lower input-referred noise in their study. In this study, the dual-mode reconfigurable channel achieves two third of input-referred noise level of [64] by having more than three times smaller input capacitance value (3 pF). The lower input-referred noise and improved NEF (lower than 6.2) could potentially have been obtained by using larger capacitances and wider transistors (or PMOS transistors). Yet, the input-referred noise is kept below 10 μV_{rms} as 8.1 μV_{rms} with 0.021 mm^2 area/channel as it has been targeted see (Table 1.5).

The simulation results of proposed work is compared to state-of-the-art in MEA and patch-clamp technologies separately in Table 4.1 and Table 4.2, respectively.

5

Conclusion

In this thesis project, we presented dual-mode reconfigurable recording unit which can record both intracellular and extracellular activities concurrently from cultured cells. The proposed 16-channel array offers many options on how the array operation is carried out. The three main operation options within the channel-array and the implications of each can be listed as follows:

- MEA-modality can be chosen for all channels: This operation mode opens a door for multi-site and high-density recordings of extracellular activities which is beneficial for understanding network dynamics of large population of cultured cells.
- CC-modality can be chosen for all channels: This operation mode enables 16 single-cell experiments for a single run. 16 single-cell experiments offers almost 2 times higher throughput than conventional patch-clamp systems. The envisioned μTAS proposes a platform where cells can be captured in micropores by means of applied suction without requiring a micromanipulator to position a patch pipette.
- One channel can be configured in CC-modality, while others operate in MEA-modality: This is very promising and important mode of operation which offers valuable insight into the correlation or anti-correlation between a firing single-cell with the large population of cells.

The recording channel can record electrical signals higher than 100 μV in amplitude. Since the action potentials mostly are recorded with amplitude of 100 μV on MEA platforms [30], this shows a promising result to capture valuable content of extracellular signals. The high-pass cut-off frequency has a value of 1.05 Hz as a mean value that is defined by the nontunable pseudo-resistors (816 GΩ), and CCIA capacitors (100 fF). The input-referred noise level of the channel is 8.1 μV_{rms} in the frequency band ranging from 1.05 Hz to 10 kHz with NEF of 6.2. The power consumption of each individual channel is 7.18 μW. Each individual channel occupies 0.021 mm^2 area on a die. It means that 10 × 10 channel-array can be utilized in a 1.5 mm × 1.5 mm die. The dual-mode reconfigurable recording channel was designed in TMSC 0.18 μm technology. 1.8 V supply voltage was used.

A localized current-DAC was also proposed within the scope of the thesis project. Each localized DAC was designed to copy 100 pA I_{ref} to its working electrode. All localized DACs were shorted in a way that activating CC_n switch of a particular channel enables 1 LSB (100 pA) current contribution of that channel to the total injected current. The characteristics of unary-weighted current-steering DAC were achieved by running MC process and mismatch simulations together when 4 unit current sources are connected together. Both resulting DNL and INL is under 0.5 LSB which is a promising result to have 4-bit resolution of DAC as it has been targeted. The localized DAC in each channel occupies area of 56.5 μm × 44 μ which does not violate area specifications.

Throughout this thesis project, a lot of focus has been put on to offer the system which can carry out dual-mode functionality for intracellular and extracellular activities of cultured cells without requiring two different bench-top systems. The need for such a system has also been pointed out throughout this thesis report. The dedicated focus on this particular need to advance science led to the main contributions listed below:

- Concurrent measurements from MEA and patch-clamp electrodes by means of dual-mode reconfigurable channel are potentially enabled to study single-cell experiments and field potentials on the potential envisioned μTAS platform.
- The recording channel offers opportunity to understand the impact of synaptic events of single-cells on extracellular field potentials.
- The recording channel shows promising results to enable understanding the impact of extracellular field potentials on a decrease in transmembrane voltage of a single neuron.
- The dual-mode recording channel occupies the smallest area with 0.021 mm^2 among the other multi-modal arrays reported in Table 4.1 which is a promising result to achieve high-density array operation.

5.1. Future Work and Recommendations

The recommendations to improve the performance of dual-mode reconfigurable recording unit, and future work can be listed as follows:

- Tunable Gain and Bandwidth: The gain and bandwidth of the recording channel should be tuned with respect to the two modalities. The high-pass cut-off frequency can go up to 300 Hz, and gain of the channel can be lowered to smaller values (around 10 V/V) when CC-modality is activated. Gain should reach up to larger values to record very small extracellular signals. The high-pass cut-off frequency should be reduced to record the content of all low-frequency field potentials. Tunable resistors can be introduced into the channel to adjust the bandwidth for the two different modalities. Tunable capacitors in the feedback path can be used to change the gain of the recording channel as well as to adjust the bandwidth.
- Compensation circuitry: The impact of leakage current from the current DAC on offset voltage of the channel was reported in Chapter 3. For larger-scale operations, this impact might cause more increase in offset voltage which can decrease the performance

of the channel drastically. Therefore, current compensation circuit techniques should be explored to prevent potential impact of leakage currents. Moreover, the IC and μTAS wafers are potentially operated together by means of connecting their pads on two different PCBs (see Fig. 1.12). The pads and interconnections on PCB will introduce parasitic capacitances and resistances which can increase the input parasitics of the channel. Such an increase in input parasitics might cause major troubles on amplification and input-referred noise level of the channel. Therefore, compensation circuits to eliminate the parasitics rising from external environment must be explored.

- System integration: It is foreseen that the problem about parasitics from PCBs can be considerably reduced by fully-integrating two potential platforms on a single wafer. Such an integration would eliminate the need of using capacitance and resistance compensation circuit for pads and interconnections on PCB. It might be made possible to integrate the IC on the silicon underneath MEA and FTPPC electrodes.

6

Appendix

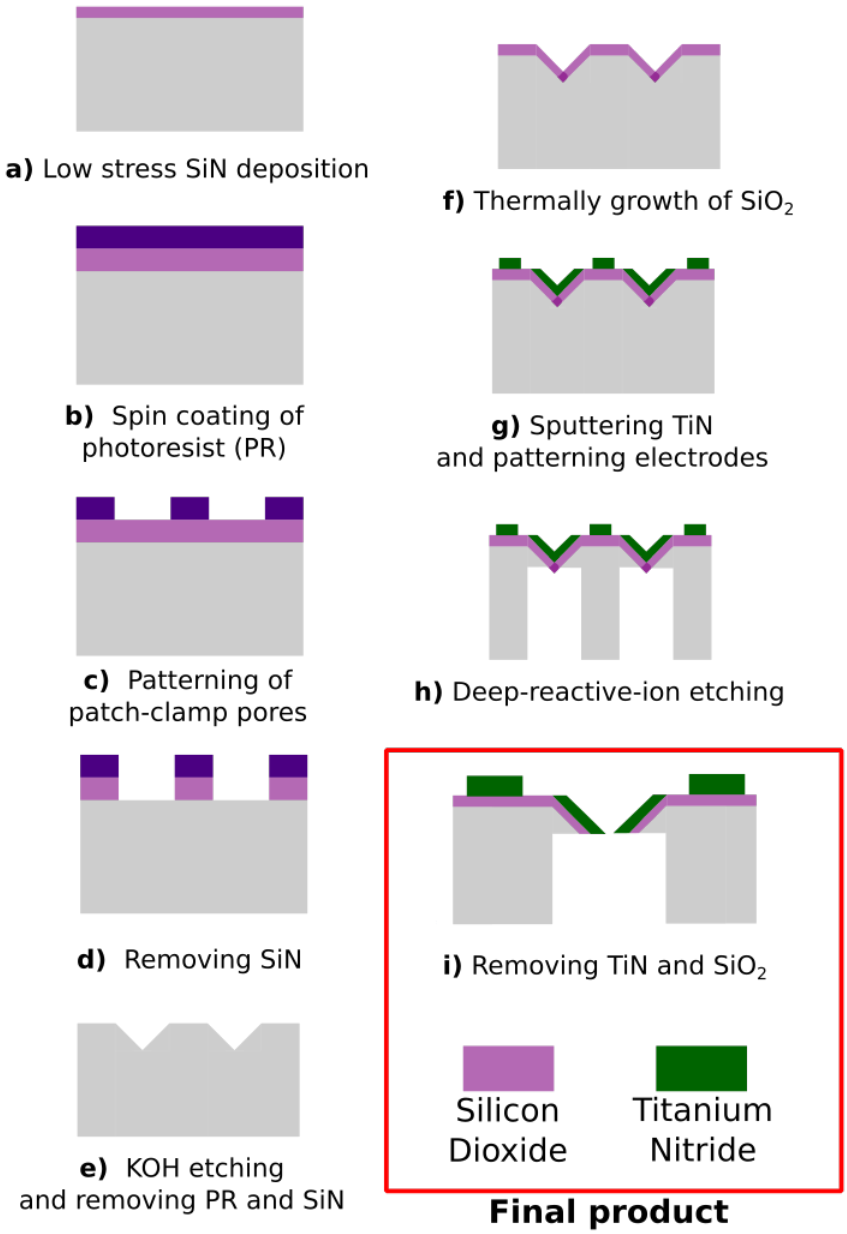


Figure 6.1: The microfabrication steps of envisioned μTAS.

Fig. 6.1 presents the simplified version microfabrication steps of cost-effective and scalable envisioned μTAS that was introduced in Chapter 1.

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