Ultra-Low-Power Event-Driven Radio Design

Xiongchuan Huang

Cover designed by Xiaofan Deng

Ultra-Low-Power Event-Driven Radio Design

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op dinsdag 18 maart 2014 om 12:30 Uur

door

Xiongchuan HUANG

elektrotechnische ingenieur
geboren te Mianyang, Sichuan, China

Dit proefschrift is goedgekeurd door de promotor:

Prof.dr.ir. J.R. Long

Samenstelling promotiecommissie:

Rector Magnificus, voorzitter

Prof.dr.ir. J.R. Long, Technische Universiteit Delft, promotor

Prof.dr.ir. R.B. Staszewski, Technische Universiteit Delft

Prof.dr.ir. B. Nauta, Universiteit Twente

Prof.dr.ir. P.G.M. Baltus, Technische Universiteit Eindhoven

Prof.dr.ir. C. Enz, Ecole Polytechnique Fédérale de Lausanne (Switzerland)

Prof.dr.ir. P. Kinget, Columbia University (USA)

Dr.ir. G. Dolmans, imec – Holst Centre, adviseur

Prof.dr.ir. K.A.A. Makinwa, Technische Universiteit Delft, reservelid

Ultra-Low-Power Event-Driven Radio Design / by Xiongchuan Huang

Technische Universiteit Delft

ISBN: 978-94-6203-557-7

Printed in The Netherlands

To my family

“Stay Hungry. Stay Foolish”

Stewart Brand

Summary

The emerging field of internet of things promises mankind an enhanced life quality, productivity and security. One critical technology enabler is ubiquitous and unobtrusive wireless connectivity activated by ambient events and operated with little human intervention for configuration and maintenance. Commercial off-the-shelf radio devices cannot achieve the desired performance, reliability and ultra-low power consumption around 100 µW at the same time. In this work, research is carried out on the design and implementation of an ultra-low-power radio for generic wireless event-driven applications including healthcare, information and entertainment, industrial and home automation, as well as environment monitoring.

To fulfill the stringent power budget, the envelope detection and the direct-modulation are the architectures of choice for receiver and transmitter front-ends, respectively. However, such radios suffer from poor sensitivity and frequency selectivity, and thus are unable to operate reliably across the desired link distance or in the presence of interference. This work investigated the root causes of insufficient sensitivity and selectivity in envelope detection receivers, and proposed design guidelines to optimize their performance. Furthermore, two novel envelope detection schemes have been proposed. The synchronized-switching technique improves the sensitivity by suppressing DC offset and 1/f noise in the receiver, while the 2-tone signaling technique enables in-band interference rejection which was not possible in prior arts.

Prototype circuits have been built to verify the proposed techniques. On a 90nm CMOS technology, a transmitter and a receiver front-end are designed to benchmark the performance of 2-tone envelope detection in practice. The digital-IF, direct-modulation transmitter carries out the 2-tone IF-PSK modulation with -6dBm output power while consuming 893 µW. The 2-tone envelope detection receiver realized up to 282 times improvement in interference rejection while dissipating between 63.5 µW and 121 µW. A link budget of over 80dB is realized

by this transceiver pair, which translates to a link span up to 30 meters in indoor environments and 100 meters outdoors.

By following a systematic approach, devising innovative architectures, and optimizing circuit performance, this work has confirmed the feasibility of ultra-low-power, autonomous and robust event-driven radios in low-cost and commercially available CMOS technologies.

Samenvatting

‘Internet of things’ is een opkomende markt waarvan een verhoogde kwaliteit van leven, productiviteit, en veiligheid te verwachten is. Een noodzakelijke technologie hiervoor is een alomtegenwoordig en onmerkbaar draadloos netwerk, dat geactiveerd wordt door naburige gebeurtenissen, en geringe menselijke interventie vereist voor zowel onderhoud als configuratie. Commercieel beschikbare radio’s kunnen momenteel de gewenste doelstellingen voor betrouwbaarheid en ultra laag vermogensverbruik beneden 100 µW niet gelijktijdig realiseren. Dit proefschrift beschrijft het onderzoek uitgevoerd naar het ontwerp en realisatie van een radio met een ultra laag vermogensverbruik voor generieke draadloze asynchrone applicaties, zoals medische zorg, informatievoorziening en vermaak, industriële en huis automatisering, en kwaliteitsmonitoring van de omgeving.

Om het uitdagende vermogensbudget te realiseren, is gekozen voor een omhullende detector voor de ontvanger en een direct-modulatie architectuur voor de zender. Een nadeel van deze keuze is de mogelijke achteruitgang in gevoeligheid en selectiviteit, hetgeen kan betekenen dat betrouwbare communicatie over grotere afstanden, of in de aanwezigheid van stoorbronnen, niet mogelijk is. Dit proefschrift onderzoekt de oorzaken van verminderde gevoeligheid en selectiviteit in ontvangstarchitecturen gebaseerd op een omhullende detector, en stelt twee oplossingen ter verbetering voor. De synchroon-schakel techniek reduceert de gevoeligheid voor DC offset en 1/f ruis, door deze te onderdrukken in de ontvanger, terwijl de twee-toon techniek het onderdrukken van in-band storing mogelijk maakt. Beide oplossingen verhogen zowel de gevoeligheid als de selectiviteit van bestaande omhullende-detector gebaseerde systemen.

Prototype schakelingen zijn gerealiseerd om de voorgestelde oplossingen te verifiëren. Een zender en een ontvanger front-end zijn in 90nm CMOS technologie ontworpen om de twee-toon techniek te vergelijken met bestaande, commercieel beschikbare systemen. De

digitale-IF direct gemoduleerde zender bestaat uit een twee-toon IF-PSK signaal met een uitgangsvermogen van -6dBm en een vermogensverbruik van 893 µW. De twee-toon omhullende detector ontvanger resulteert in 282 keer hogere selectiviteit met een vermogensverbruik tussen 63.5 µW en 121 µW. Met de zender - ontvanger combinatie is een link budget van meer dan 80dB mogelijk, hetgeen equivalent is aan een bereik van 30 meter in een huis omgeving en een bereik van 100 meter buitenshuis.

Door de systematisch aanpak, de vernieuwende architecturen en het optimaliseren van de circuits, bewijst dit proefschrift dat ultra laag vermogen, autonome en robuuste asynchrone radio's in een goedkope, commercieel beschikbare CMOS technologie mogelijk zijn.

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

As the information and communication technology (ICT) has expanded rapidly in recent years, tens, or perhaps hundreds of new devices and applications have changed our daily lives. Apart from expanding functionality and enhancing performance of the devices, more and more emphasis is placed on the energy efficiency. This is driven not only by a large number of mobile devices with limited battery power, but also a result of our awareness that the primary energy reserves on our planet are non-renewable. For battery-powered wireless devices, maintaining wireless connectivity is one of the most power-hungry operations. To address this problem, new industrial standards have been defined, focusing on low-power wireless connectivity applications. For example, the Bluetooth™ and Zigbee™ radios feature low data rates, short link distances, and low-complexity modulation schemes, all of which allow low power implementations. In addition, many proprietary ultra-low-power (ULP), short-range radio products (e.g.,[1]–[4]) have populated various market sectors, including consumer, industrial, security and healthcare. Among different applications, the requirements in performance, power consumption, cost and reliability vary significantly. In order to achieve energy-efficiency in wireless links, it is of critical importance to customize the device based on the characteristics of the targeted application.

Generally, two main categories of radio applications can be identified based on their usage and operation patterns. The first one is the data-driven application, which strives to exchange a large amount of data continuously at a high throughput. The other category is the event-driven application, which reacts to ambient events by transmitting, receiving and relaying information only when certain events occur. Traditionally, industry and academia have

focused on data-driven applications, while event-driven applications just started to emerge as a result of recent technology developments. Consequently, few radios are optimized for event-driven applications so far.

This work is dedicated to ultra-low-power radio design for event-driven applications. In this chapter, the characteristics of event-driven applications are introduced, and their system level requirements are identified. The specifications of typical event-driven radio transmitters (Tx) and receivers (Rx) are then derived. State-of-the-art ULP radios are also surveyed. At the end of this chapter, the organization of the thesis is described.

1.1 Event-Driven Radios

An event-driven radio responds to ambient events and shares information about the events. Typically, the communication between radios is unscheduled. On the other hand, the event information needs to be delivered in a timely manner, so that subsequent processing of the information can be carried out immediately. Wireless healthcare monitoring and alert systems [5]–[7] are examples where the event-driven radio is an enabling technology. Such systems monitor the condition of patients and send out an alarm signal if an emergency condition (e.g., cardiac arrest or epileptic episode) is detected. The occurrence of such critical events cannot be predicted in a given time interval. It could happen at any moment, or it might not happen at all. However, the event-driven radio must remain responsive all the times, so that an alert can be received and relayed to appropriate personnel and medical institutes once it is triggered with minimum delay.

In most cases, the amount of information relayed in event-driven communication is small since it only needs to indicate the type of the event and describe when, where and how it happened. As a result, event-driven radios do not need to transmit or receive a large amount of data for an extended period of time. Wake-up receivers (WuRx) in wireless sensor networks (WSN) are another example of event-driven radios [8]. The WuRx monitors the wireless channel, so that a main radio is activated for data communication when a wake-up bea-

con is detected. The wake-up beacon for the WuRx only needs to contain a predefined binary pattern together with several bits of address information [8].

Figure 1-1 illustrates the typical channel utilization of event-driven radios. The wireless channel is unoccupied for most of the time. The interval between wireless activities is irregular and the duration of the activities is short. The control overhead, which is the energy and time spent in establishing and controlling the communication (including timing synchronization and acknowledgement) should be minimized in order to reduce energy waste and time delay. This is contrasted with the wireless activity of typical data-driven radios illustrated in Figure 1-2. In a data-driven network, large amounts of data are exchanged in densely allocated timeslots, resulting in a congested wireless medium. Due to the longer duration of data exchanges, it is less problematic if the control overhead is not optimized in data-driven networks.

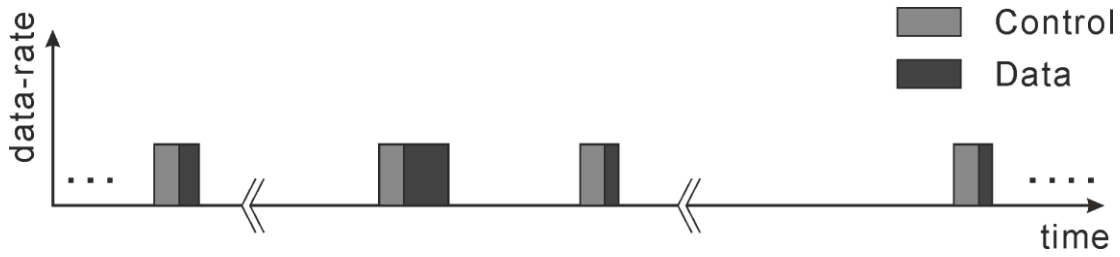


Figure 1-1: Wireless channel utilization of event-driven radio networks.

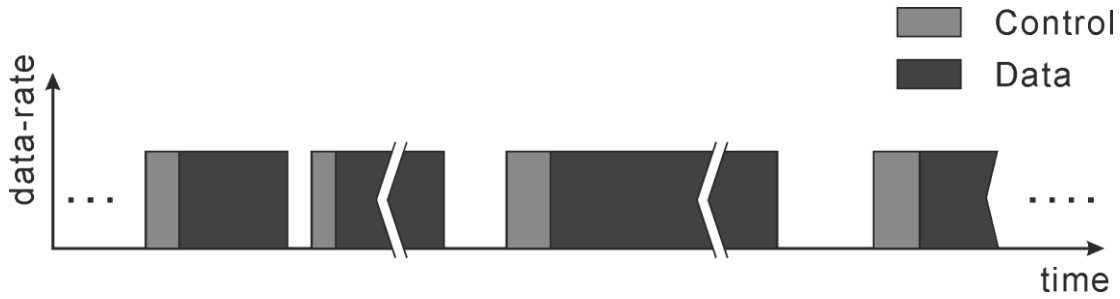


Figure 1-2: Wireless channel utilization of data-driven radio networks.

Conventional data-driven radios are not optimized for event-driven applications. This work focuses on the design, implementation, and optimization of event-driven radios. It starts by identifying the system level aspects of event-driven applications in the next section.

1.2 System Considerations

Due to the broad range of applications, the requirements of an event-driven wireless device have to be defined on a case-by-case basis. Nevertheless, some common features of event-driven applications can be summarized. This section will focus on these common features and consider the trade-offs among power consumption, system cost and functionality for a generic wireless event-driven node.

Typically, event-driven networks are deployed with limited source of energy. For example, in wireless healthcare monitoring applications, body sensors need to be small and light-weight, as they are attached to the patients' body and are often worn for a long time. Despite of advances in battery technology, the energy available to power the devices is expected to shrink due to the diminishing form factor of the batteries in miniaturized nodes [9]. On the other hand, long operation lifetime is preferred, since frequent battery replacement or recharging is inconvenient for the patients. Another example is in environmental monitoring applications. In such applications, ambient data, e.g., temperature, humidity and vibration, are sensed and processed to detect natural disasters such as a wildfire or a volcanic eruption [10]–[12]. Also, large quantities of sensor nodes need to be deployed over wide areas with reasonable cost. These systems are expected to be in service for years, while there is no practical way to replace the batteries in each node. Therefore, the power consumption needs to be optimized to maximize the battery lifetime or the battery must be supplemented by energy harvested from other sources.

Another important aspect is the system cost, which should be calculated not only for the initial hardware cost but also for deployment and maintenance. In terms of hardware cost, the event-driven nodes should be as compact as possible, with few discrete components and little dependency on expensive devices and technologies. The electronics in the device should therefore be integrated as much as possible using conventional technologies, for example in complementary metal–oxide-semiconductor (CMOS) technologies. To reduce the deployment and maintenance costs, the systems need to be autonomous, i.e., requiring minimum human

intervention. Frequent reconfiguration and calibration, as well as battery replacement or re-charging should be avoided since they inevitably increase the maintenance cost.

The functional aspect of event-driven devices is application dependent. Just as in many wireless sensor network applications, sensing and communication are indispensible functions for an event-driven node. In addition, signal processing capability is also required to process the ambient data and detect event occurrences. All of these functionalities should be supported by the power management module, which regulates the energy from batteries and/or energy harvesters and supplies it to other modules. A system controller oversees the operation of the other modules and serves as the interface to upper functional layers.

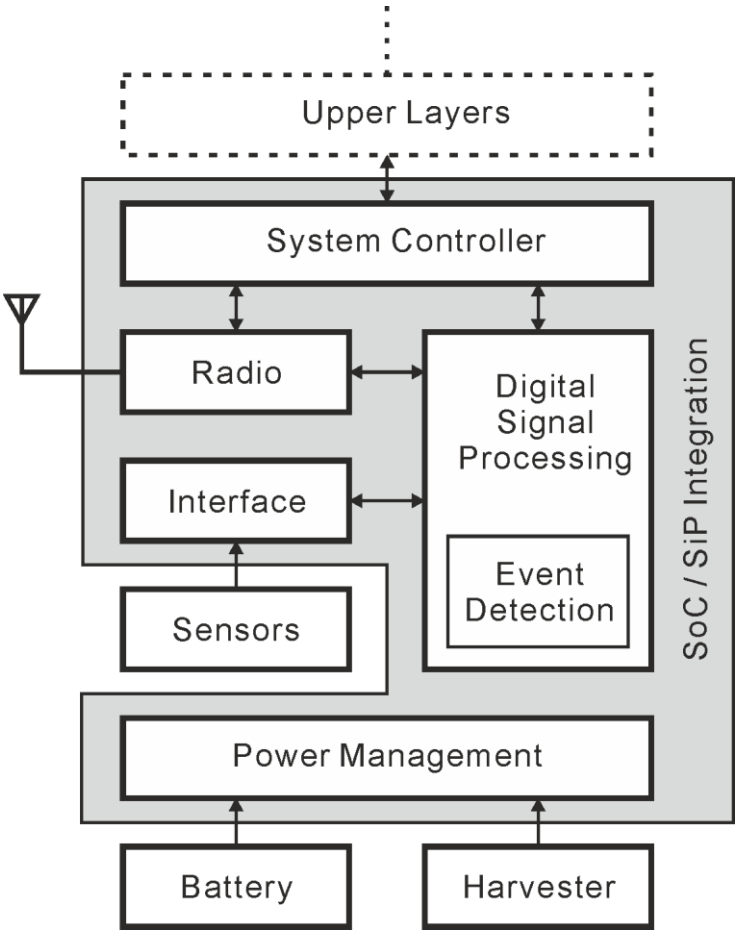


Figure 1-3: Typical block diagram of an event-driven wireless node.

Figure 1-3 shows a typical block diagram of an event-driven wireless node. In order to reduce hardware cost, most of the functionalities should be integrated into a single device

[13]–[17]. Modern CMOS technologies are especially suitable for this task, thanks to their low cost (in volume production) and versatility for mixed-signal functionalities. Both system-on-a-chip (SoC) and system-in-a-package (SiP) technologies should be considered, since they feature different trade-offs between cost, reliability, performance and time to market [18]–[20]. Functional modules which are difficult or impossible to integrate at present, e.g., many sensors, batteries and energy harvesters, may be integrated in the future as circuit or packaging technology evolves.

Beside radios, other devices such as ultrasound [21] and infrared [22] transceivers have also been reported for wireless communications. However, these devices are not as versatile as radio transceivers, due to the dependence on the media or constraint of line-of-sight (LOS) wireless links. To support a wide range of event-driven applications, this thesis adopts radio transceivers as the communication devices.

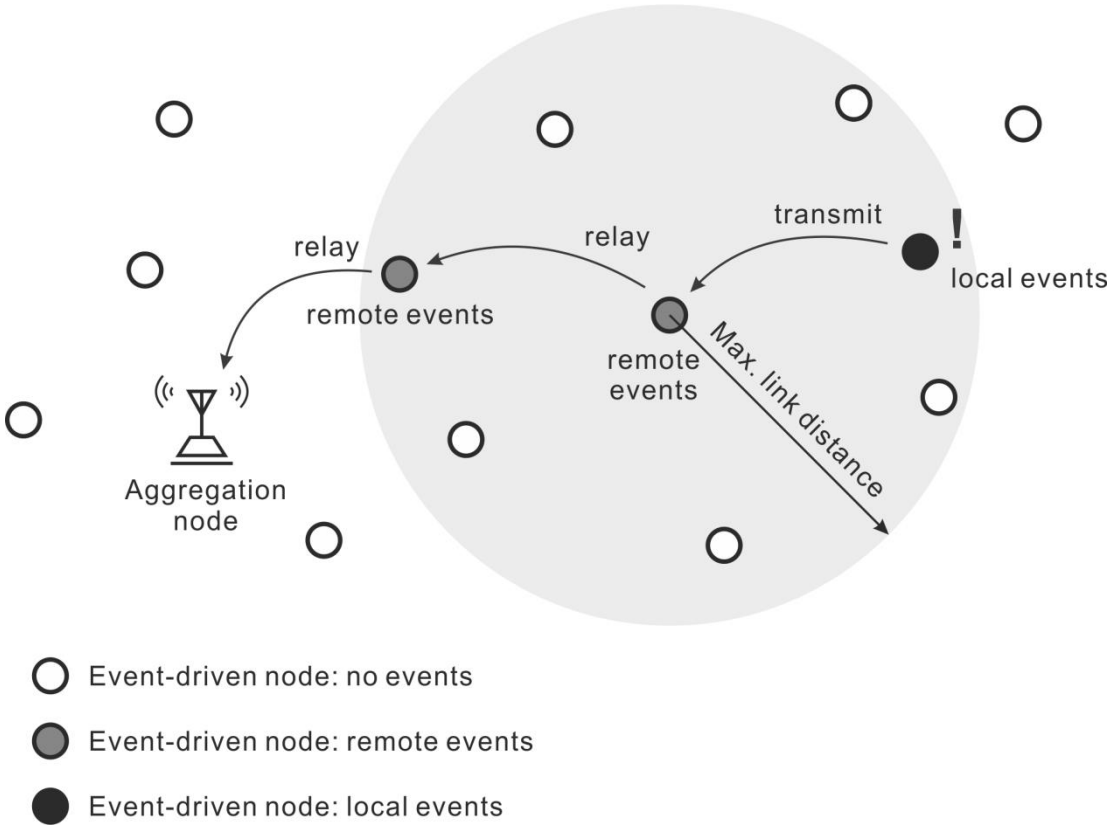


Figure 1-4: Event-driven nodes responding to remote events wirelessly.

As the energy available for an event-driven device is limited, the functional blocks in Figure 1-3 should be switched off whenever possible to reduce power consumption and prolong operation lifetime. To maintain responsiveness to ambient events, however, certain functionalities should be kept active while the rest of the system is asleep. For example, to remain responsive to local events triggered by the sensors, the sensor and interface circuits need to be active, together with a small portion of the digital signal processing (DSP) module which detects events based on sensor data. More challenging, is the need to remain responsive to remote events via the wireless channel. This occurs in applications where information about remote events must be relayed via a mesh of distributed event-driven nodes. Figure 1-4 illustrates such a scenario. To deliver the event information in a timely manner, all nodes in the event-driven network must be responsive to relay requests from the wireless channel. Therefore, the radio, the event detection routine in the DSP and the necessary power management should remain functional, while other modules can be switched off to save power as shown in Figure 1-5.

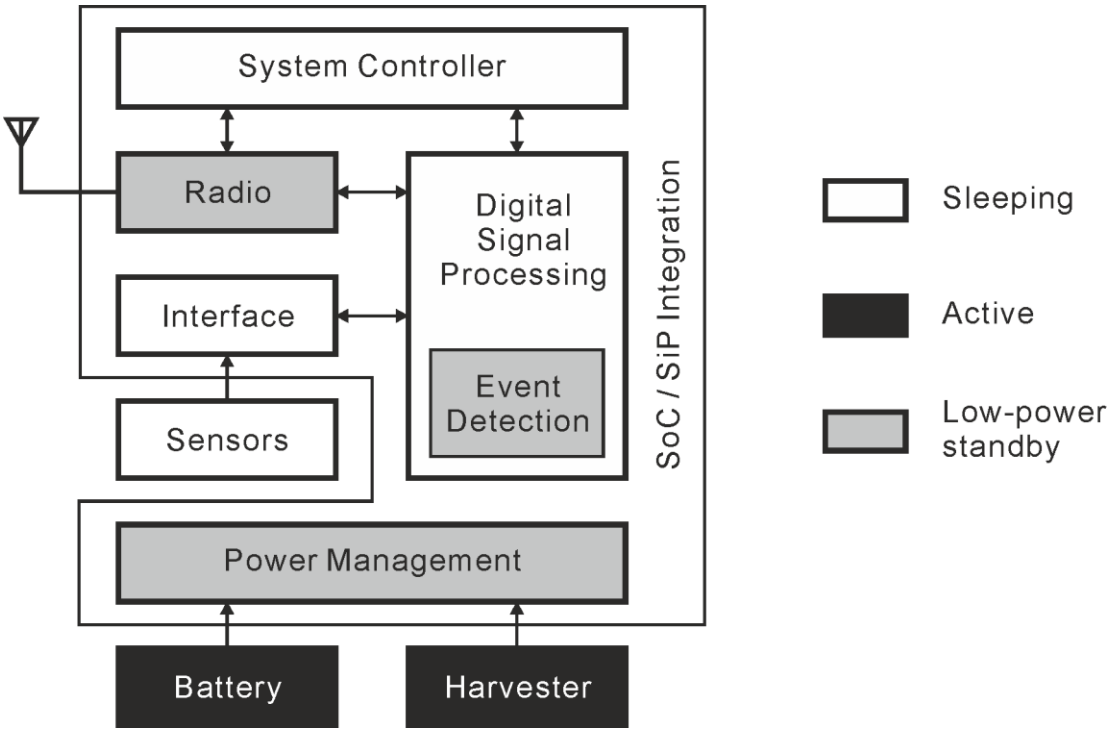


Figure 1-5: Block diagram of an event-driven node in reactive mode for wireless events.

The trade-off between power, cost and functionality at the system level does constrain the design choices made for individual blocks in an event-driven node. However, it will be shown in the next section that the trade-off becomes more pronounced when it comes to the event-driven radio design.

1.3 Radio Requirements

This section is devoted to the analysis of the specifications of a typical event-driven radio. Various parameters for the transceiver design, such as power consumption, link budget and data rate, are derived and summarized.

1.3.1 Power Consumption

The power budget for the event-driven radio varies considerably, depending on the available energy sources and desired operation lifetime. In [23] and [24], state-of-the-art battery and energy harvesting technologies have been investigated. Small sized / weight and low cost energy sources are mandatory due to the cost constraint. Under such constraints, 100μW is chosen as the system power budget, which allows approximately 1-year operation lifetime with a single coin battery [23]. Similar amount of energy can be also provided by commercially-available energy harvesters, such as a $1cm^2$ solar cell under indoor lighting conditions [24], [25].

Although other modules in an event-driven node consume power, their duty-cycle varies depending on the applications. Recent advances in circuit and system techniques make it possible to make their power consumption negligible in many applications [26], [27]. Similar to [23], it is assumed that the 100μW power budget can be completely allocated to the event-driven radio in this work.

1.3.2 Duty-Cycle

Duty-cycling can be applied to radios to reduce the average power consumption. The transceivers are switched off whenever possible, so their power consumption is reduced to the

leakage level, which can be lower than 1μW. Several wake-up schemes are proposed to switch on the transceivers only when necessary so that communication can be maintained with reduced average power consumption [28], [29].

In event-driven applications, duty-cycling the radio might be a viable solution because the amount of data transferred is small and the communication is infrequent. However, there is also a trade-off between the average power consumption and network latency [8], [30], [31]. In applications where the latency is critical, it is difficult to achieve the required latency with heavily duty-cycled radios [30]. In such cases, the event-driven radio receiver needs to always be activated to monitor the wireless channel and respond to remote events immediately.

The duty-cycle constraint applies differently to the transmitters. Despite the latency requirement, the transmitter can always be duty-cycled as long as its start-up is fast enough. It is enabled only when data is ready to send. Therefore, in many cases the transmitter can be designed to operate at higher peak power to benefit from duty-cycled operation. On the other hand, as the receiver might already consume the majority of the power budget, the average power consumption of the transmitter must be kept negligible compared to 100 μW. Assuming the average power consumption of 10 μW and a duty-cycle of 1%, the peak power consumption of the transmitter needs to be lower than 1mW. In addition, the start-up time of the transmitter should be much shorter than the typical packet length transmitted, to minimize energy waste during start-up.

To summarize, the event-driven radio receiver should be able to operate continuously with 100μW active power consumption in order to support some low-latency applications, while the transmitter can be designed with up to 1mW peak power consumption with duty-cycle below 1%. At the system level, it should be straightforward to ensure low duty-cycling transmission given the small amount of data and infrequent occurrence of events. In applications with relaxed latency requirement, the receiver can also be duty-cycled, and the resulting average power consumption further reduced.

1.3.3 Data Rate

In event-driven applications, the relatively low data rate can be exploited to achieve low power consumption in the transceiver [8], [23], [28]. An investigation carried out in [23] indicates that the average data rate of the transceivers in similar applications is lower than 1 kbps. Given such a low data rate, event-driven radios can adopt less complex modulation schemes and transceiver architectures, and can also benefit from relaxed specifications in the circuit blocks.

While the average data rate can be very low, the instantaneous data rate of the radio again has an impact on the network latency. The receiver needs to capture a packet of certain length to trigger subsequent operations, for example, relaying the data or activating other functional modules. For an event-driven radio with 100kbps data rate, a short payload of 50 bits together with 100% protocol overhead (e.g., preamble, synchronization header and address code) can be received in 1ms if the receiver is always on. This very short response time should be sufficient in most event-driven applications. In applications without strict latency requirements, the data rate of the radio can be further reduced, or the receiver can operate in a duty-cycled mode to decrease power consumption further.

In order to serve different application scenarios, this work aims to achieve data rates that are scalable between 1kbps and 100kbps at different power levels.

1.3.4 Range

The useful range of link span in event-driven applications is between 5 meters and 30 meters in indoor environments, and up to 100 meters outdoors. With such a range, the radios are able to communicate across 2 to 3 rooms in a typical residential building [32], and also cover moderate sized warehouses, supermarkets and factory buildings. When it comes to outdoor applications, such as environment monitoring for agriculture [33], [34] and natural disasters [10]–[12], the end-to-end distance may exceed 100 meters. As the path loss of a radio signal scales with distance raised to a power between 2 and 4, it is more efficient to implement multi-hop communication to cover large distances [27]. Multitudes of event-driven nodes can be distributed, so that information may be shared between any particular nodes in a large field

using relaying hops between multiple modes [35], [36]. The scenario of a multi-hop relay in an event-driven application is illustrated in Figure 1-4, where data from the remote event are relayed to an aggregation node beyond the range of a single event-driven node.

1.3.5 Carrier Frequency and Link Budget

Multiple factors influence the choice of carrier frequency. Firstly, the path loss of a radio signal increases as the carrier frequency increases. The path loss (L_s) and distance (d) are related by:

$$L_S = \left(\frac{\lambda}{4\pi}\right)^2 \frac{1}{d^n} = \left(\frac{c}{4\pi f}\right)^2 \frac{1}{d^n}, \tag{1.1}$$

where λ is the wavelength of the carrier, f is the carrier frequency, and c is the speed of light. The exponent n is an empirical factor between 2 and 4. To relax the link budget of the transceiver, it is therefore better to choose a lower carrier frequency. From a circuit design point of view, lower operating frequency of the front-end circuit also helps to reduce the power consumption of the circuits [23].

On the other hand, the size of the electrical and electromagnetic components such as antennas and inductors increases proportionally as the frequency decreases. To reduce the size of the event-driven node and achieve low deployment cost, a higher carrier frequency is desired so that small-sized antenna and integrated inductors can be used.

Another important consideration is the bandwidth available in the chosen frequency band. Many data-driven applications are moving to higher frequency bands for large available bandwidth. In event-driven applications, however, the data rate is relatively low, i.e., up to 100 kbps. This implies that the bandwidth occupied by the transmitted signal is in the range of hundreds of kilohertz, which is available in most of the unlicensed (i.e. the industrial, scientific and medical, ISM) frequency bands.

To reduce size and cost while maintain a reasonable link budget for the event-driven radio, this work proposes to utilize the sub-GHz carrier frequencies from 780MHz to 950MHz. At such frequencies, a low-cost, surface mounted antenna shorter than 1cm is available [37],

while the free-space path loss (FSPL) for a 100-meter span is around 72 dB. In a practical indoor environment, the path loss ranges from 57 to 80 dB for distances between 5 and 30 meters [38].

The link budget of up to 80dB needs to be provided by the event-driven radio. As analyzed in section 1.3.2, the receiver is facing the most stringent power constraint, as its power budget is 100μW. The transmitter can spend 1mW peak power thanks to duty-cycling. Assuming that the overall power efficiency of the transmitter is 20%, then only 0.2mW (-7dBm) is radiated from the transmitter. Consequently, the Rx sensitivity needs to be -87dBm. If the transmitter efficiency can be improved, the sensitivity of the receiver can be relaxed to the same degree.

1.3.6 Interference Rejection

Like other radios, the event-driven radio also suffers from interference. The homogeneous interference, i.e., the interference from other event-driven radios in the same network, is less problematic, because the data exchange is infrequent and the channel utilization is low, as shown in Figure 1-1. On the other hand, the heterogeneous interference cannot be ignored, since other radio devices in close proximity might also operate in the same frequency band at the same time. This is especially true in unlicensed frequency bands, which are populated by devices and systems from different manufacturers. While most state-of-the-art ultra-low-power receivers are able to reject out-of-band interference via front-end filtering [8], [39], [40], little suppression has been achieved for in-band interference. This work aims at more practical scenarios, where the event-driven radio operates in unlicensed frequency bands with in-band interference. The radio must be resilient to both in-band and out-of-band interferers to ensure proper operation of the event-driven network. The extent of interference suppression which can be achieved by the receiver remains an open question here, and will be discussed later in this thesis.

1.3.7 Summary

The requirements a typical event-driven radio are summarized in Table 1-1. It will be shown in the next section that it is very challenging to design a transceiver with 80dB link budget within 100μW that is still resilient to in-band interferers.

Table 1-1: Specifications of a typical event-driven radio

Carrier frequency	Sub-GHz unlicensed bands (780 / 868 / 915 / 950MHz)
Data rate	1kbps to 100kbps
Range	100m (free-space) / 30m (indoor)
Link budget	80dB
TX output power (P_{OUT})	Less than 0dBm
RX sensitivity (P_{MDS})	Better than -80dBm (P_{OUT} – 80dB)
Interference rejection	Resilient to both in-band and out-of-band interferers
Power consumption	100μW (Rx) / 1mW (Tx)

1.4 State-of-the-Art Ultra-Low-Power Radios

Recently there have been many publications in the field of ultra-low-power radio design. Many of them are placed in similar contexts, for example wireless sensor networks [23], [41], wake-up receivers [8], and wireless body-area networks [42]. Their performance is compared with the requirements of the event-driven radio listed in Table 1-1.

Figure 1-6 shows recently published ultra-low-power transmitters. They all adopt on/off keying (OOK) or frequency shift keying (FSK) as the modulation schemes to simplify the front-end circuitry and reduce power consumption. The low spectral efficiency of these two modulation schemes is not an issue due to low data rate in event-driven applications. The direct-modulation architecture is often adopted, which can achieve high overall power effi-

ciency for the transmitters. The power efficiency of the transmitters shown in Figure 1-6 is mostly between 10% and 40%. Compared to FSK transmitters, OOK transmitters can achieve better power efficiency as the modulation is applied conveniently by switching on and off the power amplifier (PA), or the transmitter as a whole.

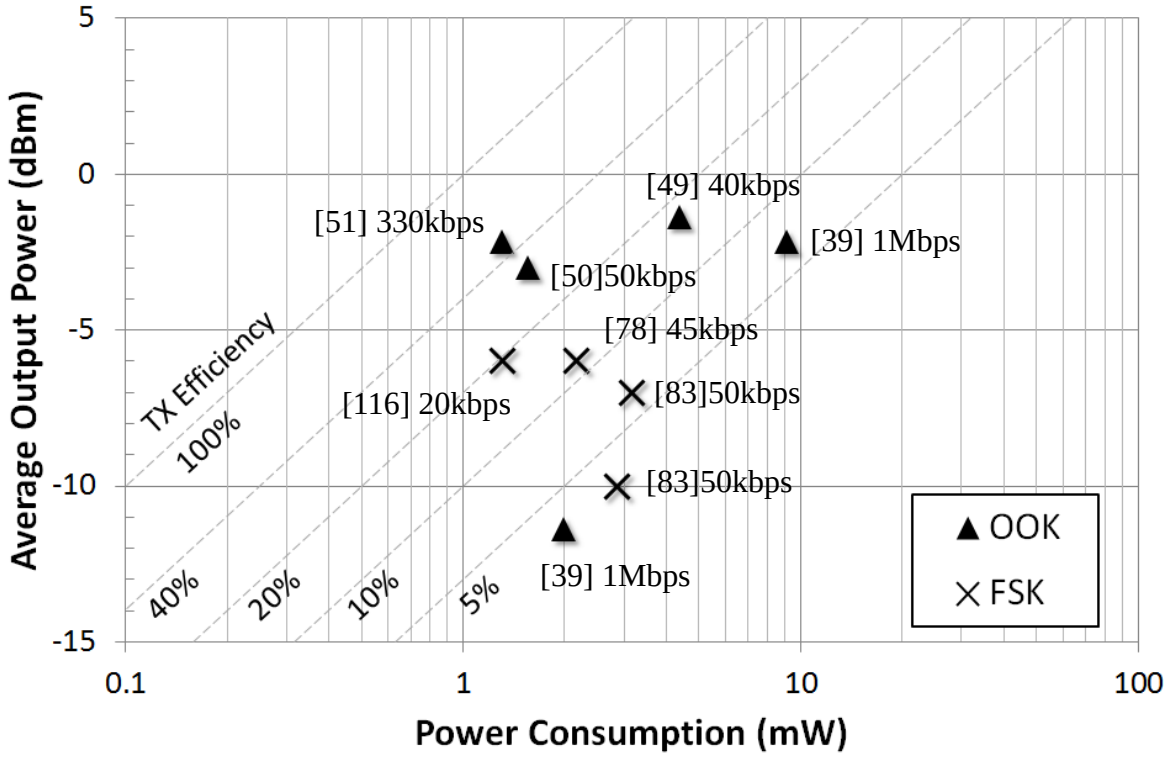


Figure 1-6: State-of-the-art ultra-low-power transmitter survey.

Figure 1-7 plots the performance and power consumption of recent ultra-low-power receivers. Again, OOK and FSK are often adopted for low complexity and consumption. Most of the ULP OOK receivers adopt envelope detection principle to detect the RF signal without the need of a local oscillator (LO). On the other hand, since the baseband information is mapped to the instantaneous frequency of the carrier in FSK modulation, FSK receivers require an accurate LO signal to downconvert the received RF signal. As a result, it is difficult to design an FSK receiver with the power budget of 100μW, which is already achieved by OOK receivers [43], [44]. In [45], a MICS-band FSK receiver achieves -90dBm sensitivity

with 120μW power consumption. However, the frequency multiplying technique in [45] is not suitable for radios operating at higher frequencies, i.e., around 1GHz or above.

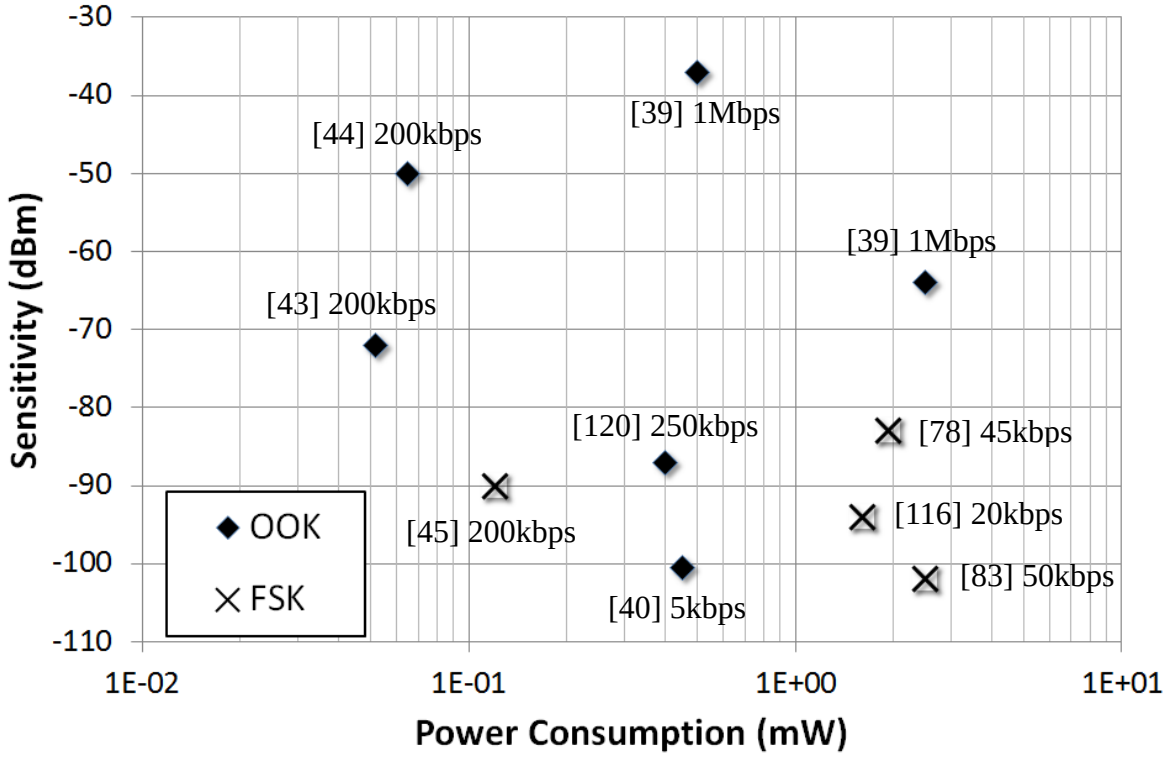


Figure 1-7: State-of-the-art ultra-low-power receiver survey.

The ultra-low-power transceivers surveyed in this section typically achieve data rates around 100kbps, which is suitable for event-driven applications. For radios with higher data rates, their sensitivity can be improved by reducing the data rate. However, data rate cannot be easily traded for power consumption, as when the radio is duty-cycled, there is always synchronization overhead [28] which prevents the power dissipation from scaling linearly with the data rate. As proposed in section 1.3.2, an event-driven receiver may need to monitor the channel continuously for remote events. In such a case, the power consumption of a receiver cannot be reduced even if lower data rate is required.

The forgoing observation is also applicable to ultra-wideband (UWB) radios [46]–[48]. These radios achieve very low energy-per-bit (i.e., below 1nJ/bit) thanks to their extremely low duty-cycled operations. They are well-suited for short-range and low-power data-driven

applications. On the other hand, prior to achieving synchronization with a transmitter, a UWB receiver needs to listen to the channel continuously. In [47], although the receiver consumes only 750μW when receiving 2Mbps data, it dissipates as much as 11.56mW when searching for incoming signals. In addition, UWB transceivers typically operate at frequencies above 3GHz, which results in higher path loss and smaller communication distance compared to narrowband radios with carrier frequencies around 1GHz. Therefore, it can be concluded that UWB radios may not be suitable for generic event-driven applications where the radio needs to monitor the wireless channel continuously with 100μW power budget.

Further investigation of the reported transceivers reveals the importance of passive components in ultra-low-power radios. Micromachined bulk acoustic wave (BAW) resonators are used in [40], [43], [44], [49]–[51]. In a transmitter, the resonator serves as the resonant tank for the carrier source. Thanks to the short-term stability of the BAW resonators, there is no need for a phase or frequency locked loop in the transmitter. In the receivers, the resonator is used as a high-Q RF bandpass filter to reject out-of-band interference.

Nonetheless, BAW resonators are not yet available for use in the unlicensed frequency bands, and integration of the micromachined BAW resonators and CMOS chips is still not cost effective. Due to the limits of cost and frequency band for event-driven applications, this work aims at radio front-ends without high-Q BAW resonators.

Another challenge is the performance of the event-driven receiver. Better than -80dBm sensitivity is required, which has not been reported with power consumption below 100μW. In addition, in-band interference rejection seems impossible in envelope detection receivers. In this work, novel circuit and system techniques have to be proposed and implemented to address these challenges within the ultra-low power budget.

1.5 Organization of This Thesis

This work has taken a systematic approach to address the challenges in event-driven radio design. Chapter 2 starts with the investigation of possible radio architectures and the analysis

of the advantages and drawbacks. It then identifies the most suitable transmitter and receiver architectures for ULP event-driven radios.

To justify the proposal from Chapter 2, two proof-of-concept designs are presented in Chapter 3: a 2.4GHz direct-modulation transmitter front-end consuming less than 4mW, and a 2.4GHz / 915MHz envelope detection receiver with 51μW power consumption.

In Chapter 4, the critical circuit blocks in this work are analyzed mathematically, offering insight from circuit design perspective. Furthermore, techniques to improve the performance are proposed, which are tailored for ultra-low-power operation in event-driven applications.

Based on the proposed techniques, the event-driven transmitter and receiver are presented in Chapter 5 and Chapter 6, respectively. The system architecture is presented, followed by implementation details. Measurement results are shown to prove the performance and functionality of the radio.

Finally, Chapter 7 concludes the thesis by highlighting its contributions and discusses directions for future work.

Chapter 2

Ultra-Low-Power Transceiver Design in nm-CMOS

This chapter identifies the design scope of the event-driven radio and investigates the strategies to tackle challenges. The characteristics of modern CMOS technologies are analyzed, focusing not only on active transistors, but also on passive components and logic gates. Next, the low-power radio architectures are surveyed. At the end of this chapter, the low-power techniques and architecture considerations are summarized.

2.1 Radio Transceiver in nm-CMOS

Due to cost and integration considerations, event-driven radios should be implemented in modern CMOS technologies. As the technology continuous to scale in the nanometer range, the performance of both active transistors and passive devices keeps improving, although at different paces. To see how the nanometer CMOS (nm-CMOS) technologies benefit the event-driven radio design, the characteristics of the devices are analyzed in the following sections.

2.1.1 Active transistors

High performance MOS transistors are provided in nm-CMOS technologies with different flavors, such as different threshold voltages (V_{TH}), different leakage levels, as well as different voltage ratings. With proper choice of devices and biasing points, these transistors can deliver sufficient performance for event-driven radios while dissipating low power.

As the technology evolves, the speed of transistors increases. In a commercial 90nm CMOS technology, the intrinsic (i.e., neglect parasitic effects from interconnection) transit frequency (f_T) of minimal-length NMOS transistors can be higher than 100GHz, which is 2 order of magnitude higher than the operating frequency of the event-driven radio in this work. To leverage the relatively lower operating frequency, the active transistors do not need to be biased in strong inversion where maximum f_T and f_{max} are obtained, but in moderate or weak inversion with lower current density to reduce power consumption [52].

Figure 2-1 shows the simulation result of the f_T of a nominal-V_{TH} NMOS transistor with minimum channel length. The gate-source voltage (V_{GS}) is swept to adjust the drain current I_D, while the drain-source voltage (V_{DS}) is fixed at 1.2V so the transistor stays in the saturation region (i.e., $V_{DS} > V_{GS} - V_{TH}$). The x-axis is the inversion coefficient (IC), which is defined as [53]:

$$IC = \frac{I_D}{2 \cdot \mu \cdot C_{ox} \cdot V_T^2 \cdot (W/L)}. \tag{2.1}$$

In (2.1), μ is the mobility of the carrier, in this case (i.e., NMOS) the electrons, C_{ox} is the oxide capacitance per unit gate area, I_D is the drain current, and W and L are the gate width and length, respectively. The thermal voltage V_T is approximately 26mV at the room temperature.

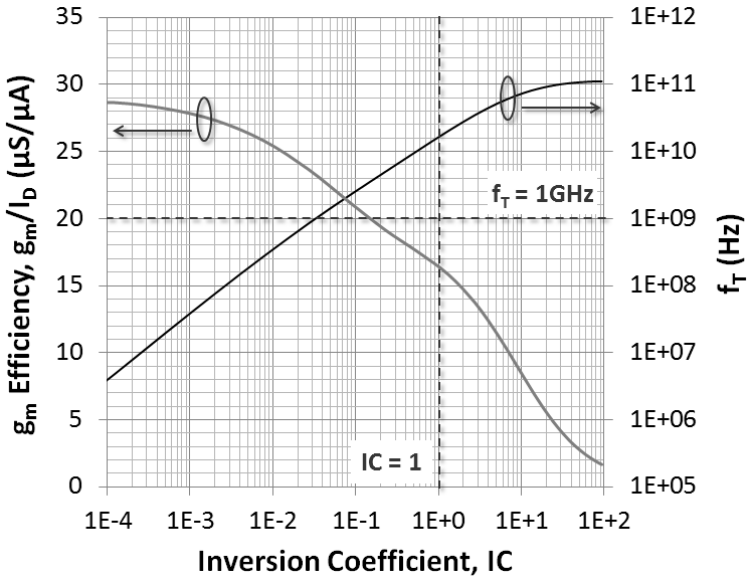


Figure 2-1: Simulated g_m efficiency and f_T of a minimum-length, nominal-V_T NMOS transistor in a commercial 90nm CMOS technology

When the inversion coefficient is much smaller than 1, i.e., the NMOS is biased in weak inversion [53], the f_T is below 1GHz and it increases linearly on a logarithmic scale as the drain current increases. The trend remains throughout the weak and moderate inversion regions (IC ≈ 1). In the strong inversion region (IC >> 1), f_T becomes higher than 100GHz at IC > 30, and then it starts to flatten out due to the velocity saturation and mobility reduction effects.

Figure 2-1 also shows the transconductance efficiency of the transistor as a function of the inversion coefficient. The transconductance (g_m) of a MOS transistor is defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \tag{2.2}$$

and the g_m efficiency is the ratio between g_m and I_D, which describes how much transconductance can be realized per certain current consumption. Higher g_m efficiency implies better power efficiency of the circuit. From Figure 2-1, the maximum g_m efficiency of 28S/A is achieved in the weak-inversion region. When the bias current increases, the g_m efficiency decreases gradually. In strong inversion, the efficiency is below 10S/A.

For ultra-low-power event-driven radio design, the transconductance efficiency is very important since a higher efficiency can reduce the current consumption. In the 90nm CMOS, the NMOS f_T is above 10GHz in moderate inversion, which is 10 times higher than the carrier frequency in this work. Therefore, subthreshold or moderate-inversion operation can be exploited to minimize the current consumption with sufficient speed [52], [54]. In [55], a 1.9GHz digitally-controlled oscillator (DCO) exploiting subthreshold operations achives 100 μW power consumption under 0.5V supply,.

Another important feature of the nm-CMOS technologies is the reduced supply voltage. In the 90nm CMOS technology, the core supply voltage (V_{DD}) is typically 1.2V. This is to be contrasted to older technology nodes such as 0.18μm CMOS, which requires 1.8V V_{DD}. On the other hand, the reduction of threshold voltage in MOS transistors is less aggressive due to leakage concerns [56]. As a result, the available voltage swing in analog circuits diminishes, making it difficult to maintain the dynamic range and signal-to-noise ratio (SNR) in the analog front-end. Nevertheless, for event-driven radios, the power level in the circuits is much

lower than the technology limitation. For example, assuming -7dBm (0.2mW) output power from the transmitter, the peak-to-peak voltage swing across 50Ω impedance is approximately 0.28V. Meanwhile, the low supply voltage can be utilized with proper design techniques to achieve low power consumption.

In analog baseband, the mismatch between transistors degrades circuit performance such as DC offset, common-mode rejection and immunity to supply / ground noise. As the technology scales down, the matching of transistors improves. The mismatch in MOS transistors is dominated by the threshold voltage difference ΔV_T, which has a normal distribution with zero mean and variance depending on the device area [57]:

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W \cdot L}, \tag{2.3}$$

where A_{VT} is a technology-dependent parameter, W and L are the transistor gate length and width, respectively. A_{VT} reduces as the technology scales down [57], [58]. For example, from 2.5μm to 0.18μm CMOS technologies, A_{VT} scales from 30mV ·μm to below 5mV ·μm [57]. For transistors of a given size, the threshold mismatch reduces by a factor of 6 in a 0.18μm technology compared to a 2.5μm technology. On the other hand, the reduction of A_{VT} is not as fast as the reduction of the feature size [59], [60]. Therefore, for minimal-sized devices, the threshold mismatch is worse in newer technologies. However, in analog baseband circuits, minimum-sized transistors are seldom used in radio front-end circuits. In RF front-end circuits where minimum-sized transistors are often used, mismatch performance is less critical.

The thermal noise performance of a transistor improves as the technology node scales down [60]. The minimal noise figure (NFmin) reduces from 0.4dB to 0.2dB as the technology scales from 0.25μm to below 100nm as a result of the improved device speed. However, in low-power and low data rate radios such as the event-driven radios, 1/f noise becomes a serious problem as it corrupts the baseband signal at low frequencies. For nm-CMOS technologies, the 1/f corner frequency for the minimum-sized transistors can reach 10MHz or above [61], while the data rate of event-driven radios is below 100kbps. Although the transistors can be scaled up to reduce 1/f noise level, attention still needs to be paid during the radio design.

2.1.2 Passive devices

In CMOS technologies, various passive components are available, including resistors, capacitors, inductors and transformers, although some require additional process steps, thus resulting in higher fabrication cost.

Resistors are often used in biasing circuits and feedback networks. Different types of resistors are available via CMOS front-end and back-end process steps, for example polysilicon stripes with N+ or P+ doping, N- or P-well diffusions and thin-film resistors. Although they typically have up to 20% deviation from their nominal resistance with processing variations their relative matching accuracy with respect to each other can be better than 1% [60].

Capacitors are available in nm-CMOS technologies in different forms. The gate to source and drain capacitance of a conventional MOS transistor can serve as a non-linear capacitor to ground or V_{DD}. The accumulation-mode MOS capacitors, e.g., n+ diffusion in an N-well or p+ diffusion in a P-well, offer a large tuning range (TR_C) defined as

$$TR_C = \frac{C_{\max}}{C_{\min}} \tag{2.4}$$

where C_{max} and C_{min} are the maximal and minimal capacitance, respectively. In a 0.18μm CMOS technology, TR_C is 2 [62], while in a 90nm CMOS technology, TR_C is higher than 4. At the same time, their quality factor (Q-factor, i.e., the ratio between the energy stored and energy loss per cycle when used in a resonance tank) can be higher than 50 at frequencies below 10GHz [63]. They are standard components in nm-CMOS technologies and often found in voltage-controlled oscillators (VCOs) as the variable capacitors (varactors). Linear capacitors can be realized by metal-insulator-metal (MIM) parallel plate capacitance [60]. They can achieve low voltage dependency and good temperature stability, as well as low leakage current. Since the metal patterns are defined with higher precision as backend technology scales, MIM capacitors can achieve better capacitance matching and density. Similar to on-chip resistors, accurate matching among capacitors can be achieved, while the absolute capacitance is controlled less accurately. As a result, the on-chip RC time constant may deviate by up to ±25% [64]. Sufficient margin and calibration techniques should be used in critical blocks to cover PVT variations [65].

On-chip inductors are implemented with metal traces using CMOS back-end interconnection metal layers [66]. To achieve high Q-factors, the upper metal layers are often used to reduce capacitive and magnetic loss to the substrate. As a result of advances in the CMOS backend technology, thick metal (TM) and ultra-thick metal (UTM) layers (up to 4.5μm in [59]) can be chosen for the top metal layers at extra cost. Due to the reduced metal loss, inductors implemented in UTM layers can achieve peak Q-factor above 20 [59]. The inductance can be well-defined, as it is determined by the diameter, number of turns, metal width and the spacing between turns, as well as the distance to a ground plane, which are accurately controlled in nm-CMOS technologies. However, care should be taken in chip floor planning to avoid Q-factor degradation and inductance shift due to magnetic coupling to other devices on-chip. In addition, inductors typically occupy large chip area, for example a 5nH inductor occupies 350μm by 350μm including its shielding structures in a 90nm CMOS technology. Therefore, the number of inductors in the circuits should be limited from the cost perspective in event-driven applications.

Transformers and distributed microwave components such as transmission lines can also be implemented on-chip with CMOS back-end metal layers [67]. Unlike standard resistors, capacitor and inductors, customized design is often required for transformers and transmission lines for performance optimization under different frequencies and specifications [66]. Transmission lines are seldom used on-chip at 1GHz or below as their physical size is proportional to the wavelength of the electromagnetic (EM) wave, which is around 15cm in silicon dioxide at 1GHz.

2.1.3 Digital circuits

Most of the properties in digital circuits improve as technology scales. The switching speed of logic gates improves as the f_T of the transistors increases [68]. As the typical supply voltage reduces from 1.8V in 0.18μm CMOS to 1.2V in 90nm CMOS technologies, the dynamic power consumption of digital circuits continues to decrease in newer technologies. In addition, various techniques such as high-k gate dielectric [69] and power gating [70] help to minimize the

power consumption due to leakage. Driven by Moore's law, the number of gates per unit area doubles for each technology generation, which reduces the size and cost of pure digital circuits and systems.

Digital intensive radio architectures, such as the all-digital phase-locked loop (ADPLL) based transmitter [71] and the direct-RF sampling, discrete-time receiver [72] have been proposed and implemented. These new architectures shift the signal processing from the traditional voltage domain to the time domain or charge domain to mitigate the limited dynamic range due to reduced voltage supply in nm-CMOS technologies. In addition, higher configurability to multiple modes and standards, better immunity to noise and PVT variations, as well as scalability toward newer technologies are all featured by digital intensive radio transceivers.

Another way for radios to incorporate and benefit from digital circuits is built-in self test (BIST) and calibration (BISC) of a transceiver front-end. The performance degradation in the analog domain can be detected and calibrated in the digital domain [73], [74]. Background calibration routines such as Tx pre-distortion [75] and analog-to-digital (ADC) offset / mismatch compensation [76] can run together with radio activity, so the overall performance is guaranteed despite non-idealities in the radio front-end, including component mismatch, PVT variations and non-linearity. In the event-driven radio design, this implies that the radio front-end can be designed with less performance margin and lower power consumption, while using digital calibration algorithms to ensure the proper operation of the front-end.

2.2 Low-Power Transceiver Architectures

The stringent power budget of event-driven radios cannot be achieved simply via advanced process technologies or low-power circuit techniques. Instead, it is more important to choose radio architectures which are optimized for low-power operation. In this section, several low-power radio architectures are investigated.

2.2.1 Transmitter architectures

In nm-CMOS technologies there is great flexibility in transmitter architectures. While the super-heterodyne transmitter achieves the best performance and reliability, its complexity and dependence on off-chip filtering is challenging for fully-integrated low-power implementations [77]. The two potential low-power Tx architectures, i.e., direct-conversion Tx and direct-modulation Tx, are analyzed for the event-driven radio design.

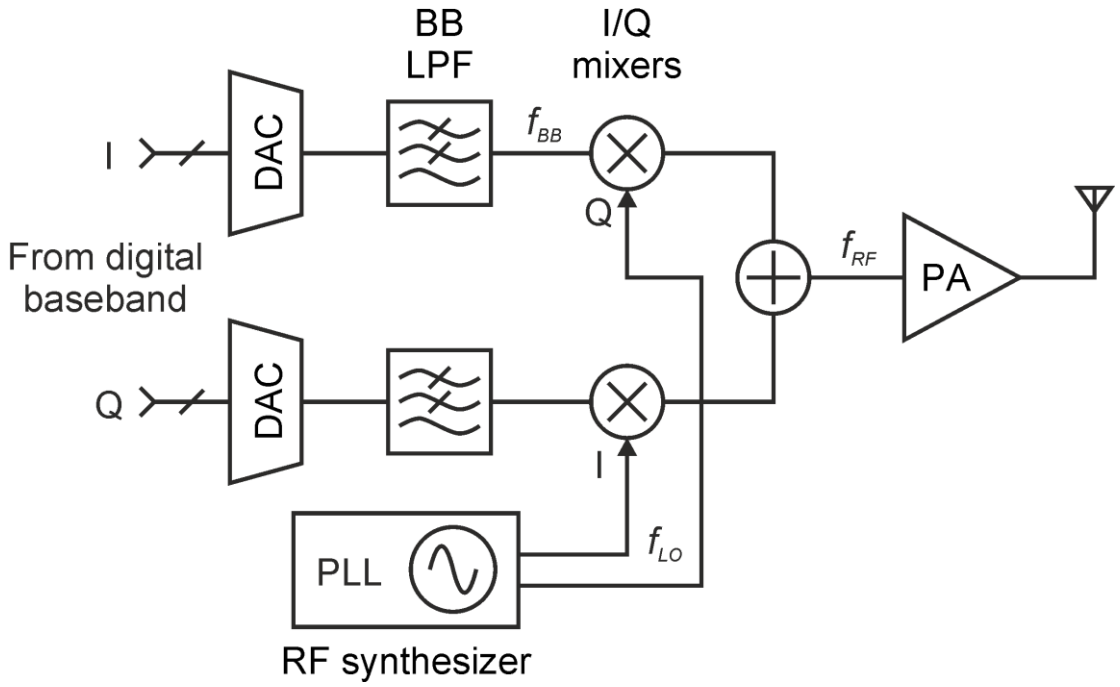


Figure 2-2: Block diagram of direct-conversion Tx front-end [77].

Figure 2-2 shows the block diagram of a direct-conversion Tx front-end. The complex digital baseband signals are firstly converted to two branches of analog baseband signals via a pair of digital-to-analog converters (DACs), which are followed by two low-pass filters (LPFs) to suppress clock aliasing. The analog baseband signals are upconverted by the quadrature local oscillator (LO) signal and then amplified by the power amplifier (PA) after summation.

The direct-conversion Tx front-end can support virtually all modulation schemes, as the modulation is carried out in the digital domain while the analog front-end just upconverts the modulated signal to the carrier frequency. It also obviates the need for off-chip components,

which enables low-cost and fully-integrated implementations. Since the baseband signal is directly upconverted to RF, such transmitters suffer from LO leakage and LO pulling effects [77].

An example of a low-power direct-conversion transmitter is given in [78]. The radio adopts frequency-shift-keying (FSK) modulation, and delivers -6dBm output power at 900MHz. Thanks to the constant-envelope modulation scheme, a nonlinear PA can be used to achieve a power efficiency of around 50%. However, the frequency synthesizer, operating at twice the carrier frequency to generate quadrature LO signals, consumes more than 1/3 of the total power consumption, degrading the overall power efficiency to below 10%.

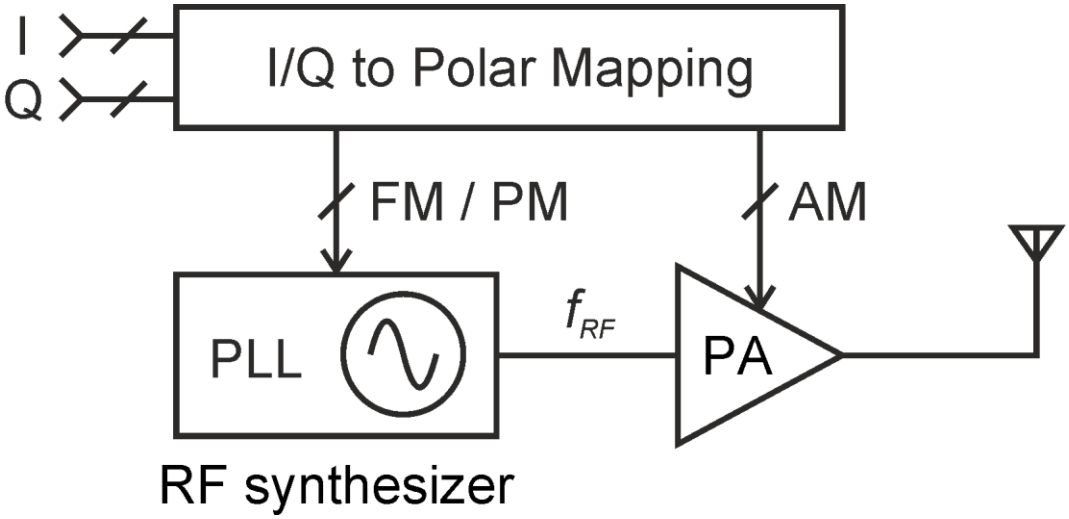


Figure 2-3: Block diagram of a direct-modulation (polar) Tx front-end [79].

Direct-modulation transmitters can be implemented in different forms. Figure 2-3 illustrates one realization that supports most modulation schemes: a polar transmitter [79]. The complex modulation is separated into the phase and amplitude paths and applied directly at the frequency synthesizer and PA, respectively. The transmitter can be simplified if constant-envelope modulation such as FSK is used, as a conventional PA can be used without amplitude modulation. Similarly, if amplitude modulation such as on/off keying (OOK) is used, the phase of the carrier signal does not need to be locked by a phase-locked loop (PLL), and a free-running oscillator with duty-cycled frequency calibration would be sufficient [80].

An ultra-low-power direct-modulation OOK transmitter is demonstrated by [40]. The block diagram of the transmitter is shown in Figure 2-4. The 2GHz carrier signal is generated using a film bulk acoustic wave resonator (FBAR) oscillator without a PLL or a frequency locked loop (FLL), and the modulation is carried out by switching on and off the entire front-end. The output power is -3dBm while the power consumption is 2.15mW, resulting an overall power efficiency of 23%.

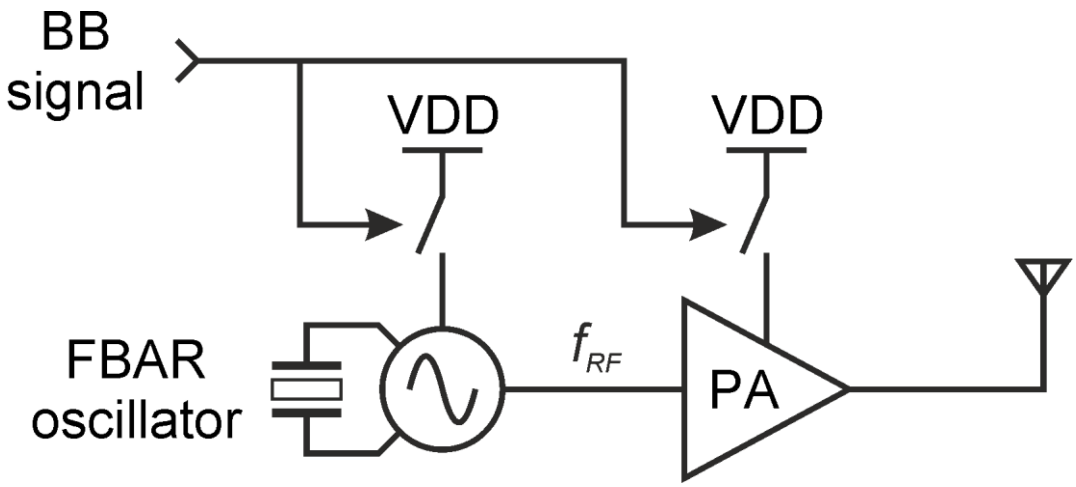


Figure 2-4: Block diagram of the direct-modulation OOK Tx in [40].

By comparing [78] and [40] it is clear that the direct-modulation Tx benefits from lower power consumption in stages preceding the PA (pre-PA). This is especially important for low-power transmitters, where the output power level (P_{out}) is low and the power drawn by the pre-PA ($P_{pre\text{-}PA}$) may be comparable to the PA power consumption (P_{PA}). The overall efficiency of a transmitter (η_{Tx}) is given by:

$$\eta_{Tx} = \frac{P_{out}}{P_{Tx}} = \frac{P_{out}}{P_{PA} + P_{pre-PA}} = \frac{1}{1/\eta_{PA} + P_{pre-PA}/P_{out}}, \tag{2.5}$$

where η_{PA} is the drain efficiency of the PA. To maximize η_{Tx}, not only should the PA efficiency be maximized, but also the pre-PA power should be kept at just a fraction of P_{out}, which is below 0dBm (1mW) as specified in Chapter 1. Therefore, the direct-modulation architecture is chosen in this work for its high overall power efficiency at low RF output levels.

Challenges still remain even for the direct-modulation Tx. The transmitter in [40] is only able to deliver OOK modulation at the resonance frequency of the FBAR oscillator, offering

little flexibility in frequency range and modulation schemes. These limitations will be addressed in the event-driven Tx designed in this work.

2.2.2 Receiver architectures

Just as the Tx counterpart, different Rx architectures can be chosen in nm-CMOS technologies. Conventional architectures such as super-heterodyne [81], low-IF [82], zero-IF [78], and sliding-IF [83] receivers offer reliable performance at the cost of complexity and power consumption. Due to the stringent power budget in event-driven applications (i.e., around 100 μW for receiver), other architectures must be investigated.

Firstly, common Rx architectures are analyzed to identify their limitations in power reduction. Among those architectures, the zero-IF receiver seems the best candidate for low-power applications due to its low complexity and high level of integration [77]. A block diagram of a zero-IF receiver is shown in Figure 2-5. The received RF signal is amplified by the low-noise amplifier (LNA), then downconverted to baseband via a pair of mixers driven by the quadrature LO signal. At the analog baseband, the low-pass filters (LPFs) perform channel selection, and the programmable gain amplifiers (PGAs) boost the signal level to the optimum input level of the ADCs. Demodulation can be carried out in the digital baseband.

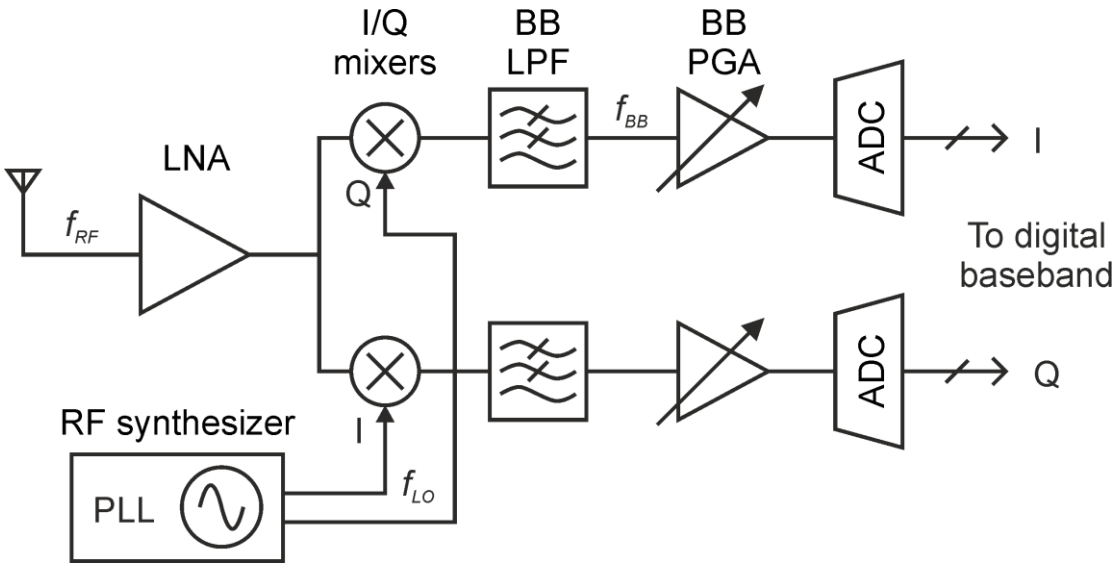


Figure 2-5: Block diagram of zero-IF receiver front-end.

Various techniques can be applied to reduce the power consumption of such receivers. The LNA can be removed entirely and passive mixers can be used as the input stage [84]. The baseband LPF and PGA are typically combined into a single block [85]. In the case of constant-envelope modulation, the PGA can be replaced by limiting amplifiers and demodulation can be carried out in the analog domain without ADCs [78]. Despite these efforts, the power consumption of such receivers is still well above 100 µW. The bottleneck in power reduction is the RF synthesizer, which generates the quadrature LO signal via a PLL. The lowest power consumption reported for an RF PLL is around 1mW [86], which is mainly consumed by the VCO and frequency dividers operating in the gigahertz range. For an RF oscillator alone, the power consumption is more than 100 µW due to the limited Q-factor of on-chip inductors [55].

The super regenerative principle is often utilized in ultra-low-power receivers to detect amplitude-modulated signals [40], [87]. The block diagram of a super regenerative receiver is shown in Figure 2-6. Compared to a zero-IF receiver, the super regenerative receiver requires no mixers, and a single-path analog baseband chain can be used instead of the quadrature baseband in zero-IF receivers. In addition, the demodulation can be carried out in the analog domain with a threshold detector without analog-to-digital conversion. These differences clearly reduce the power consumption; the receiver in [87] consumes 2.8mW with fully integrated signal chain and calibration circuits, while the receiver in [40] benefits from the FBAR-based super regenerative oscillator and consumes merely 450 µW.

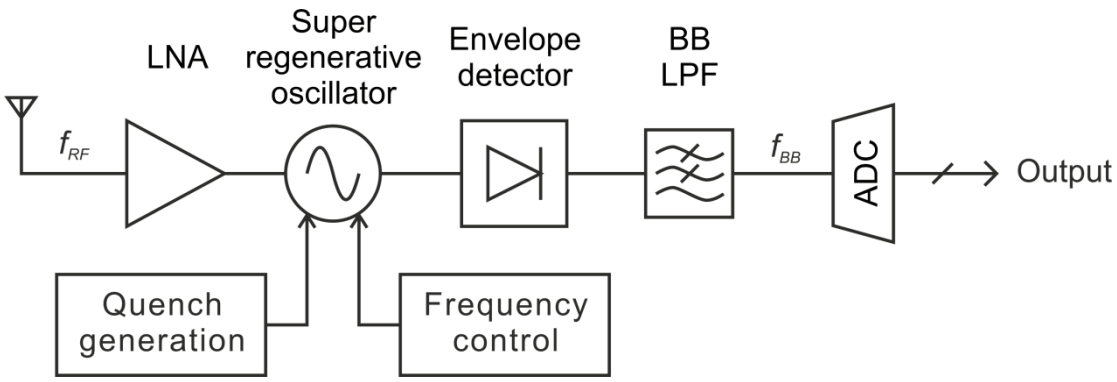


Figure 2-6: Block diagram of a super regenerative receiver front-end.

Typically, super regenerative receivers can only support amplitude based modulations such as OOK. These modulation schemes suffer from poor spectrum efficiency and require higher signal-to-noise ratio (SNR) during demodulation compared to phase modulations [88]. In addition, when strong interference is present, the super regenerative oscillator may be pulled to the interference frequency, and it downconverts the interferer instead of the desired signal. This implies poor interference rejection. Despite consuming relatively lower power than the zero-IF receiver, due to the presence of the RF super regenerative oscillator, it is difficult to achieve power consumption below 100μW in today's technology.

Another Rx architecture that achieves low power consumption is the envelope detection receiver. The block diagram of a generic envelope detection receiver is shown in Figure 2-7. The RF signal is downconverted by the envelope detector to baseband without the need for an LO signal. The baseband signal can be demodulated by comparing the baseband signal to a threshold voltage in the threshold detector. Due to the absence of RF synthesizers and local oscillators, the complexity and power consumption of envelope detection receivers is the lowest compared to other Rx architectures. The LNA preceding the envelope detector can be removed at the cost of sensitivity degradation. The envelope detector itself can be a passive circuit, so the static power consumption of such receivers can be kept below 100μW [43], [44], some even below 1μW [89], [90].

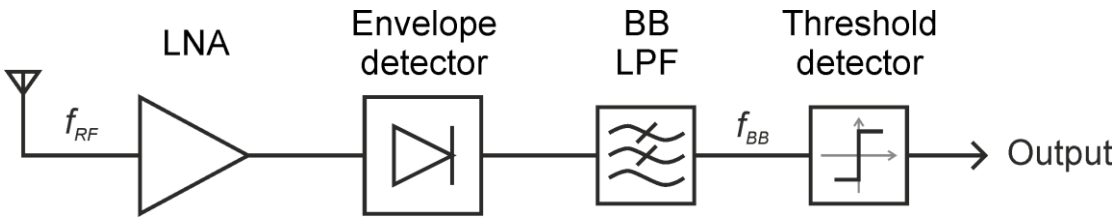


Figure 2-7: Block diagram of an envelope detection receiver.

Similar to super regenerative receivers, envelope detection receivers can only support amplitude based modulations. In addition, such receivers suffer from poor sensitivity due to the limited gain and poor noise performance of low-power RF amplifiers. As the envelope

detector is insensitive to the frequency and phase of the input signals, the receiver also suffers from poor interference rejection.

The various Rx architectures analyzed in this section feature different advantages and drawbacks. When the power budget is reduced, the overall performance and reliability degrade in one or several respects. For event-driven applications, the envelope detection receiver appears to be the only choice for achieving power consumption below 100 µW. Although this type of receivers is confined to amplitude modulation schemes with poor spectrum efficiency, it is still acceptable since the data rate is low and data are often transferred in bursts rather than continuously in event-driven applications. On the other hand, the limited performance in such receivers, especially the poor sensitivity and interference resilience, must be improved from the circuit and system level to meet the requirements of event-driven radios.

2.3 Summary

In this chapter, the technology platform for the event-driven radio was analyzed. The nm-CMOS technology adopted in this thesis features high performance active transistors and high quality passive components. Meanwhile, the high-performance and low-power digital circuits can be leveraged to assist the radio front-end via built-in self test and calibration techniques.

Low-power radio architectures were also surveyed. Based on the stringent power budget and requirements of generic event-driven applications, the direct-modulation transmitter and envelope detection receiver are chosen in this work. In the next chapter, two proof-of-concept radio circuits of these architectures are designed and implemented to verify the proposed architectures.

Chapter 3

Proof-of-Concept Circuits

It has been proposed in the last chapter that the direct-modulation transmitter and the envelope detection receiver are suitable for event-driven radios. To evaluate the performance of these proposals, two proof-of-concept radio front-ends are designed in a 90nm CMOS technology. This chapter is dedicated to the design, implementation and measurement of these circuits.

3.1 A 2.4GHz Direct-modulation OOK Transmitter with Digital Pulse-shaping

A direct-modulation transmitter front-end with low pre-PA power consumption and high overall efficiency is built to support OOK modulation at 2.4GHz [91]. It is designed for short-range wireless body-area network (WBAN) and wireless sensor network (WSN) applications which require low power dissipation (less than 5mW) and moderate output power (around 0dBm) [92], similar to the requirements of generic event-driven radios derived in section 1.3. In this section, the transmitter implementation and evaluation results are described.

3.1.1 Transmitter Architecture

A block diagram of the transmitter is shown in Figure 3-1. It consists of an RF voltage-controlled oscillator (VCO) and a digitally-controlled power amplifier (PA) for direct modulation. A local oscillator (LO) buffer is inserted between the PA and the VCO to isolate the oscillator from the dynamic input impedance of the PA. The LO buffer and the VCO are

carefully optimized for low power consumption to avoid degradation of the overall power efficiency.

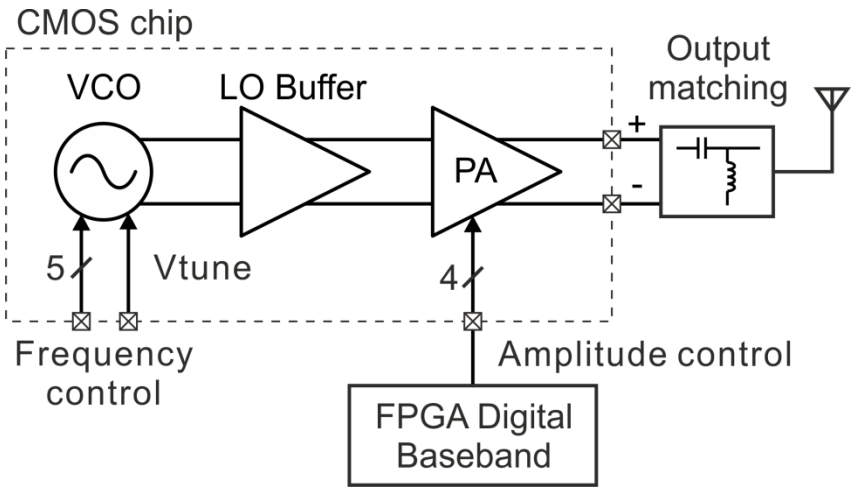


Figure 3-1: Block diagram of the proof-of-concept transmitter.

The transmitter needs to support data rates up to 10Mbps for data-intensive applications such as electroencephalography (EEG) [93]. As a trade-off between performance and power consumption, the VCO and the LO buffer stay on during transmission, while the PA, which can be switched on and off much faster than an LC oscillator, is modulated by the digital baseband (DBB) signal. This strategy also avoids the frequency transient that occurs during VCO start-up.

Unlike typical event-driven radios, the spectral efficiency of this transmitter (Tx) is still important due to its higher data rate. To improve the efficiency of OOK modulation, pulse-shaping is applied to the PA. The output amplitude of the PA is therefore programmed in 16 discrete steps via the 4-bit DBB signal. By applying gradual changes to the amplitude levels during bit transitions, the power spectrum of the Tx output can be concentrated near the carrier frequency, resulting in better spectral efficiency than with conventional OOK modulation.

3.1.2 Circuit Implementation

The transmitter is designed to operate from a 1V supply in a 90nm CMOS technology. The technology features 1 polysilicon and 9 metal layers for interconnection, including 2 thick (approximately 1µm) and 1 ultra-thick (approximately 3µm) metal layers at the top. Mixed-signal components, such as on-chip inductors and MIM capacitors, are available as well.

3.1.2.1 LC VCO Design

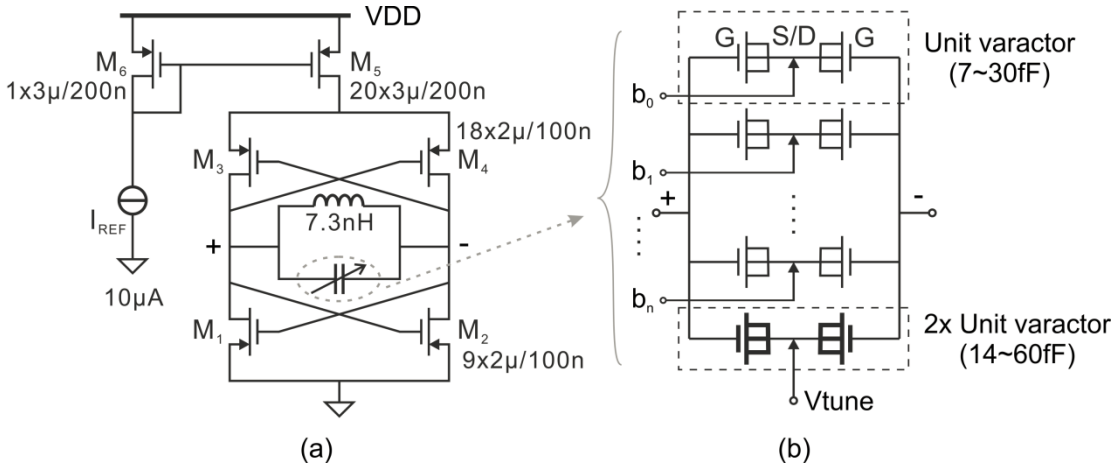


Figure 3-2: Schematic of the integrated 2.4GHz VCO (a) and illustration of the tuning capacitance (b).

The VCO generating the 2.4GHz carrier signal is completely integrated on-chip. The schematic of the VCO is shown in Figure 3-2. Complementary cross-coupled PMOS and NMOS transistors are adopted to double the negative output conductance in a given current consumption. This reduces the maximum output signal swing of the VCO compared to a single N- or PMOS cross-coupled pair. However, the minimum power consumption of the VCO is reduced by 50%, which is critical to improving the overall power efficiency. PMOS tail current source M5 is chosen for its low 1/f noise, which will be upconverted as close-in phase noise around the carrier [94]. The active transistors M_1-M_4 are biased in moderate-inversion to maximize their transconductance efficiency, while the tail current source is biased in

strong-inversion for low thermal noise. The VCO operates in the current-limited region where the active transistors stay in the saturation region for the optimum trade-off between phase noise and power consumption [95].

At 2.4GHz, the loss in the LC tank is dominated by the on-chip inductor. The parallel loss resistance (R_P) of the tank at resonance can be calculated as

$$R_P = 2\pi f_{res} \cdot L \cdot Q, \tag{3.1}$$

where f_{res} is the resonance frequency, L is the inductance and Q is the quality-factor of the tank. To start and maintain oscillation, the negative conductance of the cross-coupled pair must be higher than $1/R_P$. To minimize the required negative conductance, which is proportional to the current consumption of the oscillator, R_P should be maximized. This implies that the product between L and Q should be as high as possible [55]. As the inductance and Q-factor are both interdependent and frequency dependent, there is an optimal inductor in the given technology. However, in this work, the optimal inductance is higher than 10nH, and the tank capacitance must be lower than 0.44pF to oscillate at frequencies higher than 2.4GHz. Such capacitance will be contributed primarily by the device parasitics of the cross-coupled pair and the input capacitance of the following stage, and therefore little room is left for variable capacitance to realize frequency tuning. To cover the industrial, scientific and medical (ISM) frequency band from 2.4GHz to 2.5GHz with ±10% margin for process, voltage and temperature (PVT) variations, a frequency range from 2.16GHz to 2.75GHz (i.e., 24% referring to the center frequency) is required. As a trade-off between the frequency tuning range and tank loss, a 7.3nH symmetric spiral inductor is chosen. Thanks to the ultra-thick top metal layer and differential-mode operation [96], the Q-factor is 17 at 2.4GHz, resulting in 1.87kΩ R_P. The tank capacitance consists of an array of switched varactors in parallel with a pair of varactors controlled by an analog tuning voltage. This ensures a large tuning range while reducing the phase noise originating from the control voltage. The switched varactor array is implemented with 31 unit varactor pairs, each of which can be tuned between 7fF and 30fF (differential) with a minimal Q-factor of 65. Their tuning voltages are switched between supply and ground by 5 digital control bits, while the analog controlled pair is 2 unit varactor pairs connected in parallel

with their tuning port connected to an analog tuning voltage, Vtune. This combination provides redundancy against mismatch between the 31 digitally-controlled units and the analog-tuned units, such that any frequency spot within the tuning range can be covered. In the 90nm CMOS technology, the switched varactor bank occupies less area, and achieves approximately 50% higher tuning range than switched MIM banks with the same Q-factor since it does not suffer from the on-state resistance and off-state capacitance of the switches in the signal path.

3.1.2.2 Direct-modulating PA Design

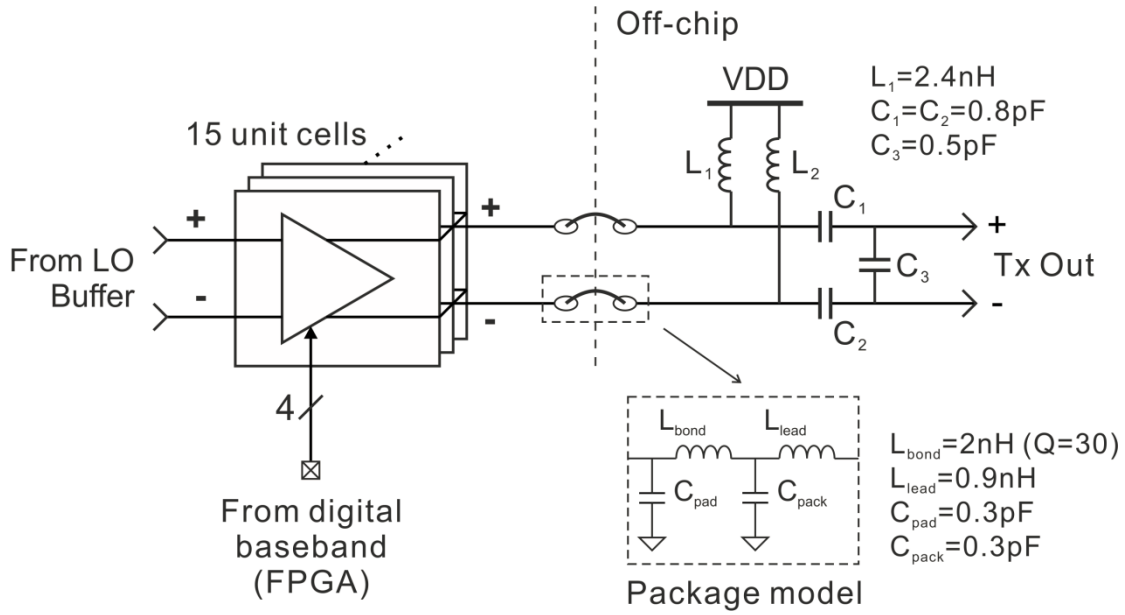
The proposed digitally-controlled PA is illustrated in Figure 3-3. The PA consists of 15 unit PA cells connected in parallel. Each unit cell is implemented as a pseudo-differential NMOS pair M_1 and M_2 (2 x 2μm wide by 100nm long fingers) with cascode transistors M_3 and M_4 (4 x 2μm wide by 100nm long fingers). The LO signal drives the input NMOS pairs with a fixed differential swing of 400mV, and the output of each unit cell is combined by summing RF currents in the output matching network.

The gates of M_3 and M_4 in the unit cells are connected to rail-to-rail amplitude control signals. When the control signal is high (V_{DD}), the cascode transistors are switched on, and M_1 and M_2 operate in saturation region. When the control signal is low (ground), the cascode transistors are switched off, and M_1 and M_2 operate in linear region with no RF current output. The amplitude control signals of the 15 unit cells are thermometer-coded from a 4-bit binary baseband signal, so that the total RF current can be programmed in 16 discrete steps, resulting in 16 output power levels for amplitude modulation, power control or pulse-shaping.

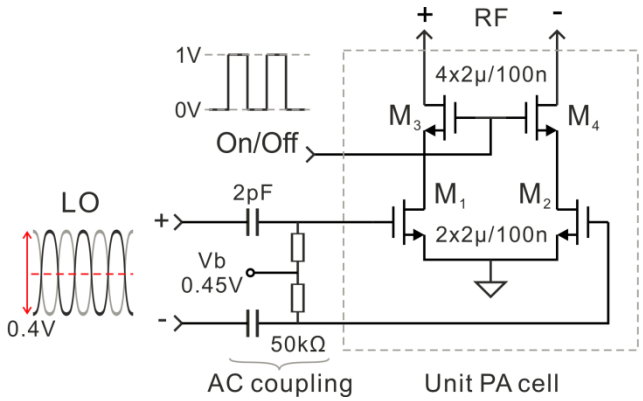
The biasing of the PA is optimized for overall power efficiency. If biased class-C, the power efficiency of the PA improves, but the input swing required is also higher and the power consumption of the LO buffer increases. Similarly, switching PAs, such as class-E and class-F, require a rail-to-rail square wave input, which leads to even higher power consumption of the LO buffer. For example, to drive a typical 100fF input capacitance of a PA at 2.4GHz, the power dissipated to charge and to discharge this capacitance (i.e., P_{cap}) between 0V and 1V is

$$P_{cap} = 100\,fF \times (1V)^2 \times 2.4GHz = 240\,\mu W\,, \tag{3.2}$$

while if the voltage swing across the capacitance is reduced by half, the power dissipation will decrease by 75% to 60 μW. On the other hand, when biased class-A, the poor efficiency of the PA (theoretical maximum of 50%) degrades the overall efficiency. As a result, the PA is biased class-AB as a trade-off between drain efficiency of the PA and pre-PA power consumption. The nominal differential input swing is 400mV, while the gate bias of M_1 and M_2 is 450mV.



(a) Block diagram



(b) unit cell schematic

Figure 3-3: Illustrations of the 4-bit digitally-controlled PA.

In class-AB, the output voltage can swing between 0V and $2V_{DD}$; however the transistors in the unit cells will be driven into linear region when the output voltage approaches zero,

which degrades both the linearity and the power efficiency of the PA. As a result, the output voltage is confined between 0.5V and 1.5V for power efficiency and linearity. If the impedance seen at the output of the unit cell is R_L, then power delivered to the load (P_{OUT}) under 1V differential swing is

$$P_{OUT} = \frac{(1V)^2}{2 \times R_L} = \frac{1}{2R_L}(W) . \tag{3.3}$$

To deliver 1mW power at the antenna, the optimal R_L should be 500Ω. In practice, due to the loss in the matching network, the power delivered by the PA unit cells is slightly higher than 1mW, and the optimal R_L is lower than 500Ω. An off-chip output matching network with 2 inductors and 3 capacitors is implemented to transform the 100Ω (differential) antenna impedance to the optimal impedance at the output of the unit cells. LC network acts as a capacitive transformer [97], while the high-Q (higher than 50) off-chip surface-mounted inductors and capacitors (SMD) minimize the power loss at the cost of board area and bill of materials. The inductors in the matching network also feed currents to the PA unit cells. Packaging parasitics such as the bondpad capacitance and bondwire inductance are absorbed into the matching network as shown in Figure 3-3.

3.1.2.3 LO Buffer Design

The schematic of the low-power LO buffer is shown in Figure 3-4. Similar to the VCO, the LO buffer also utilizes a complementary topology to maximize the transconductance for a given bias current. The ratio between the NMOS and PMOS transistors is 2, which makes their transconductances similar to minimize the distortion in the output LO signal. The PMOS transistors are biased via a current mirror, while the common-mode path of the NMOS transistors is a diode-connected transistor via feedback resistors R_1-R_2. The feedback resistors are chosen 120kΩ each, so that they do not load either the input or the output of the buffer.

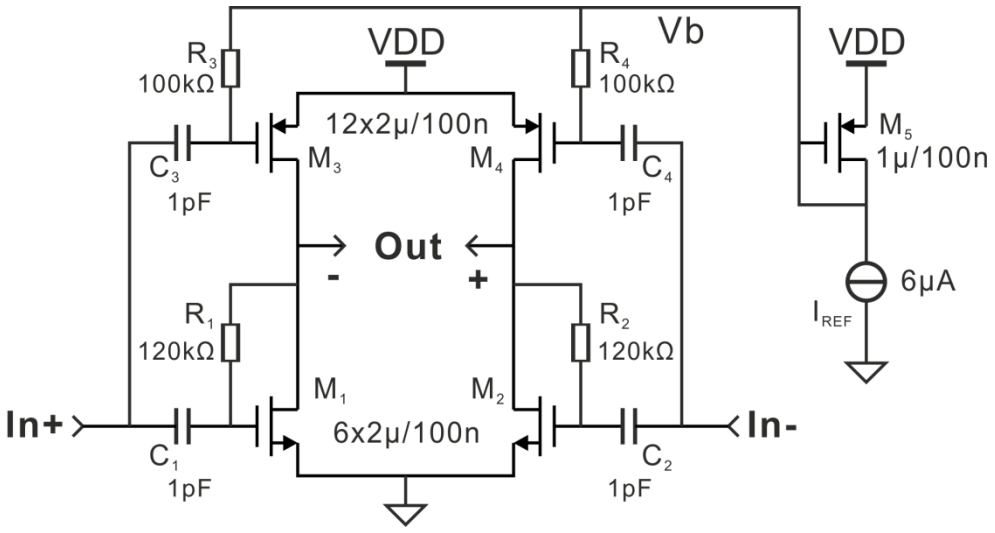


Figure 3-4: Schematic of the complementary LO buffer.

The active transistors M_1-M_4 are biased in weak inversion to reduce the power consumption of the buffer at the cost of large transistor size and high input and output capacitance. The input capacitance of the buffer is in parallel with the tank capacitance of the VCO, and therefore it can be tuned out by the inductance of the VCO. The output capacitance is in parallel with the PA input capacitance, which is approximately 10 times larger. Therefore, the power dissipated to charge and discharge the output capacitance does not dominate the overall power consumption of the LO buffer.

3.1.2.4 Transmitter Prototype

The fabricated Tx front-end chip is wire-bonded in a 56 pin, surface mounted quad flatpack no-lead package (QFN). The chip micrograph is shown in Figure 3-5. The active circuitry measures 0.564mm by 1.564mm excluding bondpads. Digital baseband logic is implemented in a Xilinx Virtex-5 FPGA platform to control the operation of the Tx front-end. The packaged chip and off-chip matching network are solder attached to a 4-layer printed circuit board (PCB) for evaluation.

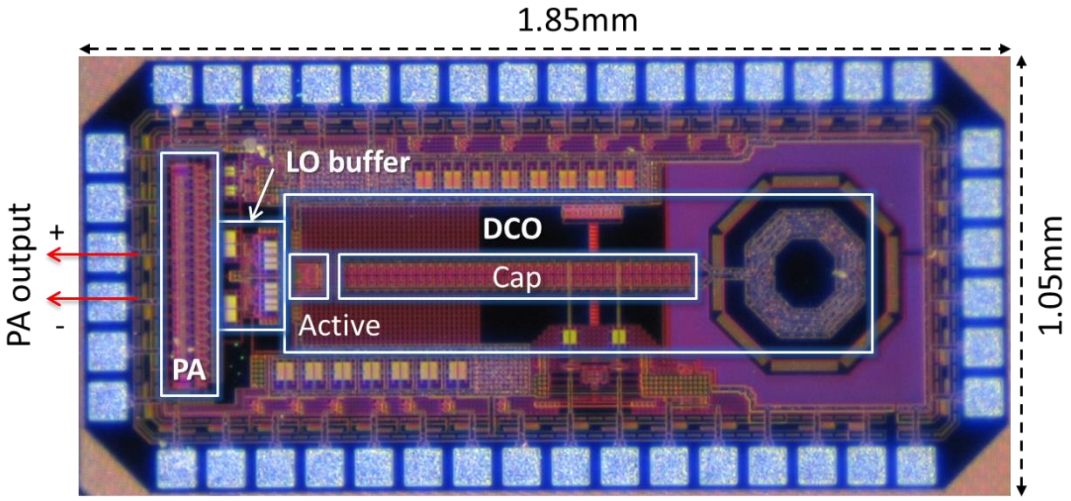


Figure 3-5: Chip micrograph of the proof-of-concept transmitter.

3.1.3 Evaluation Results

The VCO is able to oscillate with power consumption as low as 112 µW at 2.4GHz. The measured phase noise of the VCO is -109dBc/Hz at 1MHz offset from the carrier at this power consumption. During normal operation, the VCO consumes 250 µW, and its phase noise is -112dBc/Hz at the same offset frequency.

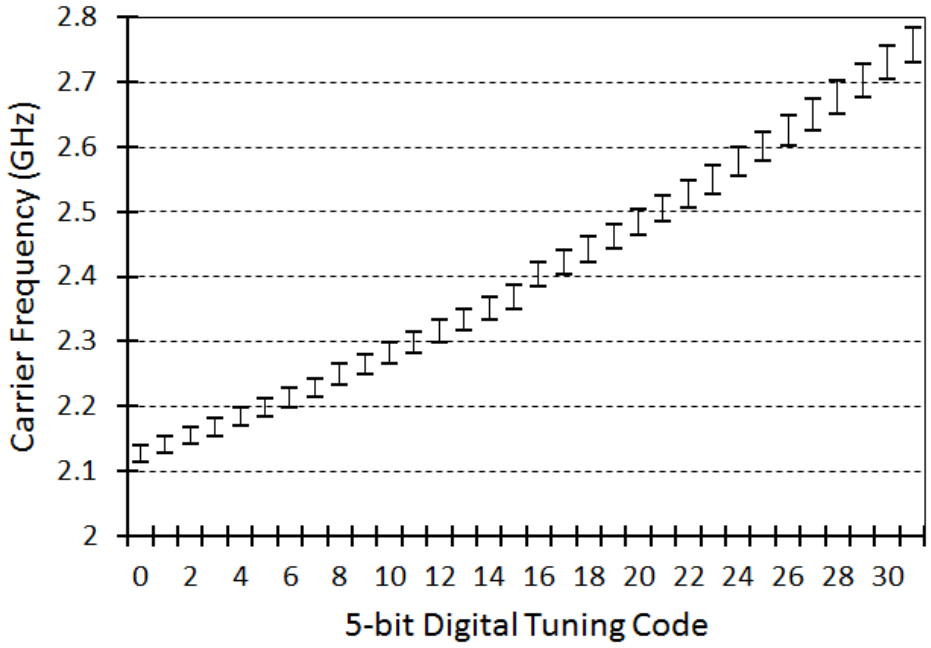


Figure 3-6: Measured tuning range of the VCO.

The VCO can be tuned between 2.11GHz and 2.8GHz, covering a range of 28% with respect to the center frequency 2.455GHz. All of the frequency spots are covered by the 5-bit digital coarse tuning and the analog fine tuning voltage. The analog tuning ranges under different digital tuning settings are plotted in Figure 3-6. It can be seen that the overlap between digital tuning codes 15 and 16 is the smallest, which is equivalent to large differential nonlinearity (DNL) in the capacitor bank. However, Monte Carlo simulation with up to 500 samples only shows a standard deviation of the capacitor steps up to 0.0016 LSB, which implies the measured mismatch may be attributed to poor matching in the layout instead of capacitance variation of intrinsic devices. The matching and the tuning overlap are improved in a later version by increasing the size of the analog tuning varactor (to cover larger rang by the analog fine tuning) and adopting a common-centroid varactor placement in the layout.

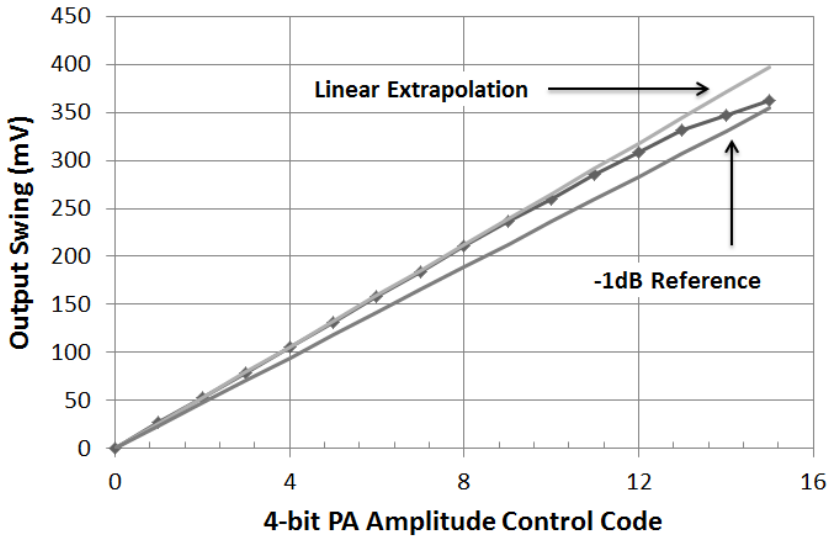


Figure 3-7: Tx output signal level at different amplitude control codes.

Figure 3-7 plots the measured 2.4GHz signal swing on a 50Ω termination for different amplitude control codes. As the code increases, more unit PA cells are activated, and the output signal level grows linearly. When the voltage swing at the PA unit cell outputs increases, the transistors may enter triode region and degrade the linearity. As explained in section 3.1.2.2, the optimal load impedance for this PA is chosen to ensure that the transistors stay in

saturation at the target output level (i.e., 0dBm). Therefore, a good linearity is achieved and the PA does not reach the 1dB compression point when all the unit cells are activated.

When 13 out of the 15 unit PA cells are on, the transmitter outputs 0dBm with 3.88mW power consumption at 1V VDD. The PA, LO buffer and VCO consume 3.14mW, 490 μW and 250 μW, respectively. The pre-PA stages contribute to only 19% of the overall power consumption, while the overall power efficiency of the transmitter (η_{TX}) is 25.8%. The overall efficiency is defined as

$$\eta_{TX} = \frac{P_{OUT}}{P_{DC}}, \tag{3.4}$$

where P_{OUT} and P_{DC} are the average RF output power and power consumption of the transmitter, respectively. When all the unit PA cells are on, η_{TX} increase to 32% with 1.2dBm output power.

OOK modulation is applied to the transmitter via the PA amplitude control signal. The baseband signal of alternating 0s and 1s is applied, and all the PA unit cells are switched on and off completely. Figure 3-8 shows the transient waveform of a 10Mbps OOK output. The rise- and fall-times of the carrier envelope are 20ns and 10ns, respectively. The maximum data rate of the transmitter is higher than 20Mbps.

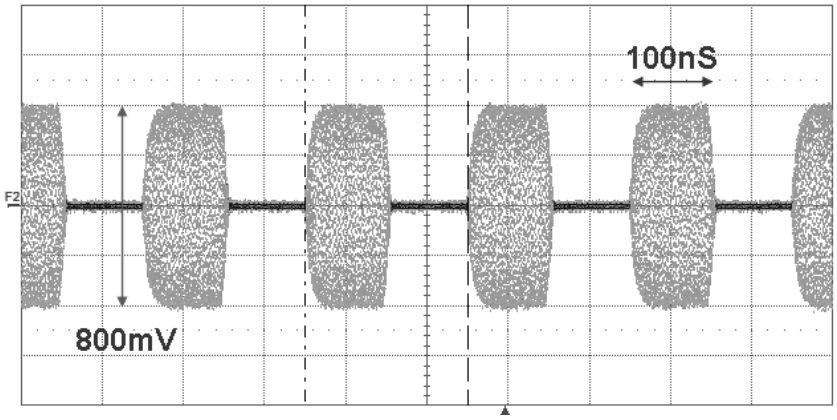


Figure 3-8: Tx output waveform at 10Mbps OOK modulation.

By gradually increasing the number of active PA cells within one bit period, the pulse of the Tx output can be shaped to improve the spectral efficiency of OOK modulation. Raised-cosine pulse-shaping with 8x oversampling and a roll-off factor of 0.2 is applied to a 3.125Mbps OOK impulse. The digital signal processing function for the pulse-shaping is im-

plemented on the FPGA platform, and the block diagram is shown in Figure 3-9. In the FPGA digital baseband module, the 3.125Mbps binary signal is firstly oversampled by a factor of 8 to 25Msps. Then a finite impulse response (FIR) digital filter convolves the oversampled binary bits with 6-bit, signed raised-cosine filter coefficients to generate the 4-bit unsigned output codes for the PA. The filter coefficients are carefully scaled to avoid overflow with all possible input data patterns. In addition, as the PA cannot handle negative amplitudes, the PA amplitude control signal is clipped to 0 when a negative value is generated by the FIR filter.

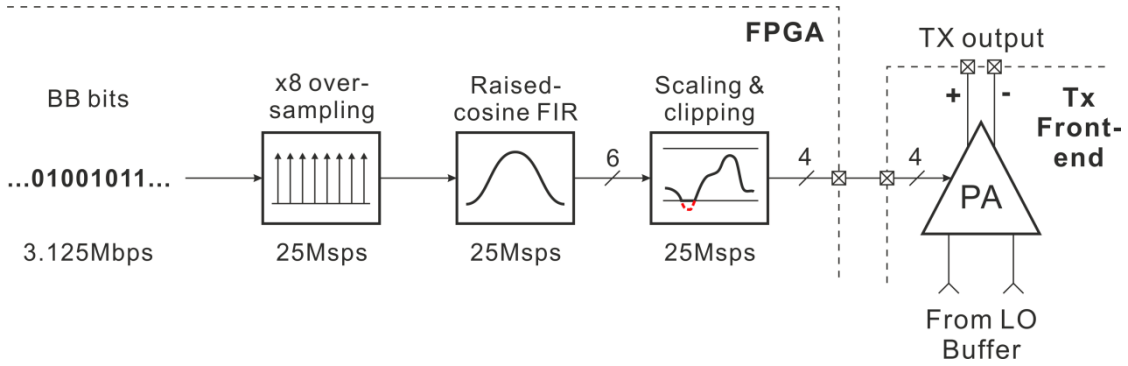
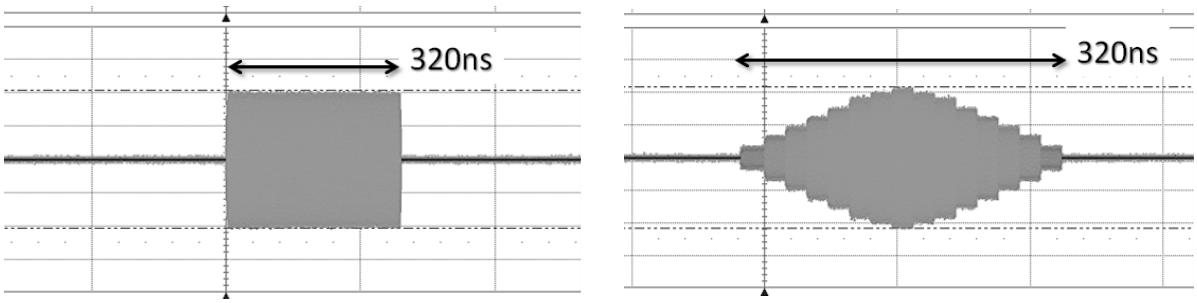


Figure 3-9: Tx pulse-shaping digital logic and interface to the Tx front-end.

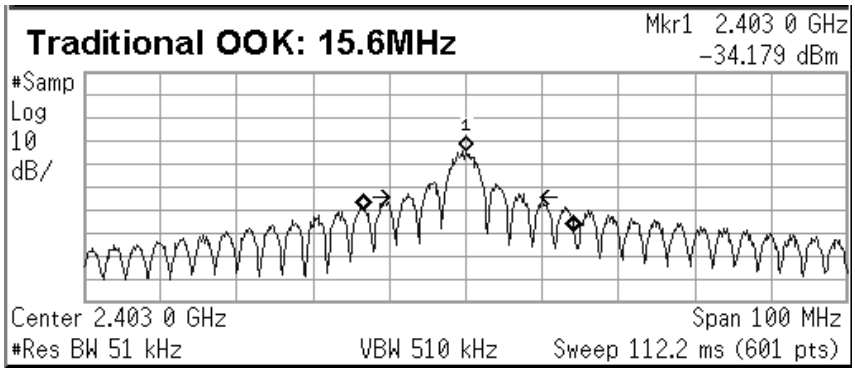


(a) Unshaped OOK pulse (b) Shaped OOK pulse

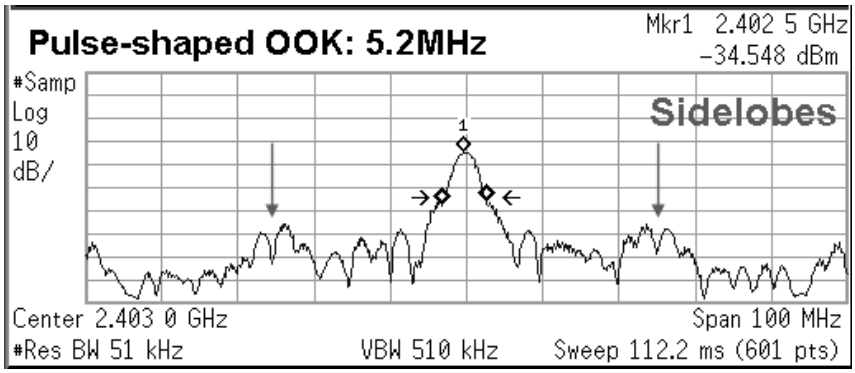
Figure 3-10: Measured Tx output of isolated OOK pulses at 3.125Mbps.

The resulting Tx output signal is shown in Figure 3-10(b), together with an unshaped OOK pulse in Figure 3-10(a). By comparing the spectrum of the Tx output signals in Figure 3-11, the advantage of pulse-shaping is shown clearly in the spectral efficiency: the -20dBc bandwidth of the unshaped and shaped OOK signals is 15.6MHz and 5.2MHz, respectively.

The side-lobes of the pulse-shaped OOK originate from the 25MHz oversampling clock, which are 32dB below the main-lobe.



(a) Unshaped OOK spectrum



(b) Shaped OOK spectrum

Figure 3-11: Measured Tx output spectrum of OOK pulses at 3.125Mbps.

When transmitting an OOK modulated signal with equal probability of 0 and 1, the transmitter consumes 2.31mW. The power consumption breakdown is shown in Figure 3-12. Most of the power is consumed by the PA, with 22% of total power delivered to the antenna. The pre-PA stages contribute only 32% of the overall power consumption, which is desired for an efficient low-power transmitter.

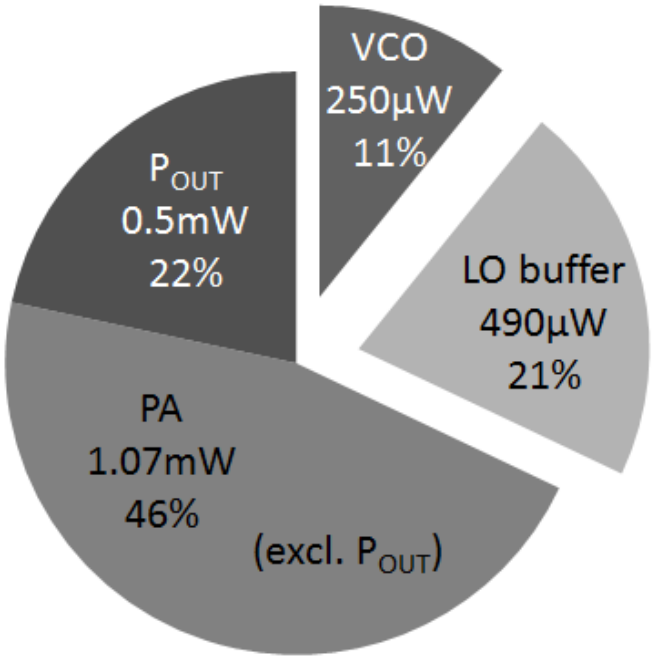


Figure 3-12: Power breakdown of the Tx front-end when transmitting OOK signals.

3.1.4 Summary

Table 3-1: Comparison to the state-of-the-art low-power OOK transmitters.

Reference	Freq. (GHz)	Pout (mW)	Peak η_{TX} (%)	Data rate (Mbps)
[51]	1.9	1.2	46	0.33
[98]	0.433	0.054	4.5	10
[39]	0.9	0.6	6.9	1
This work	**2.4**	**1**	**25.8**	**10**

The Tx front-end implemented in this section adopts the direct-modulation architecture to apply OOK modulation with low pre-PA power dissipation and high overall power efficiency. It delivers a 0dBm, 2.4GHz carrier signal at 25.8% overall efficiency. The comparison in Table 3-1 with other state-of-the-art examples shows that this proof-of-concept transmitter achieves one of the best overall power efficiencies among low-power OOK transmitters. While the efficiency in [51] is higher, this work realizes a much higher data rate thanks to the fast switching time of the PA. In addition, pulse-shaping is applied to the OOK transmitter

developed in this work to improve the spectral efficiency of the modulated signal, which is not implemented in other examples.

3.2 A 2.4GHz / 915MHz Wake-up Receiver Based on Synchronized-switching Envelope Detection

An envelope detection receiver front-end is designed as a wake-up receiver (WuRx) for wireless sensor network applications. It supports amplitude-based modulation schemes at the 2.4GHz, or 915MHz frequency bands and consumes 51 μW. A novel 1/f noise reduction technique, called synchronized-switching is proposed to improve the sensitivity of the receiver. In this section, the implementation and evaluation results of this proof-of-concept receiver are presented.

3.2.1 Receiver Architecture

The block diagram of the receiver front-end is shown in Figure 3-13. It consists of an input matching network, a low-noise amplifier (LNA), an envelope detector (ED), and a baseband (BB) amplifier. A synchronized-switching technique, which is similar to the chopper stabilization (CHS) technique used in analog signal processing [99], is proposed to suppress the DC offset and 1/f noise of the receiver. The reduction of low-frequency noise is as a major advantage for a WuRx, since its received signal is concentrated at low frequencies due to the low data rate [100], and the baseband signal-to-noise ratio (SNR) suffers from impairments due to 1/f noise and DC offsets.

The signals at nodes (a) to (g) in Figure 3-13 correspond to the subset (a) to (g) in the illustration in Figure 3-14. The proposed noise suppression technique adds choppers (mixers) at both the input and output of the receiver. However, any polarity change of the signal in the RF stage will not be detected after squaring by the ED. Therefore, the input chopper (an NMOS switch to ground) does not alternate the polarity of the RF signal, but switches the RF signal (pulse-shaping ignored for simplicity) at (a) on and off via the input synchro-

nized-switching (SS) clock (i.e., CLK_{RF} at (b)) at the frequency f_{SS}. The resulting signal is shown in Figure 3-14(c), which is amplified by the LNA and fed to the envelope detector. The envelope detector output follows the amplitude of its input signal at f_{SS} as shown in Figure 3-14(d). Frequency f_{SS} is chosen above the 1/f corner frequency, in this case 10MHz, so that the output signal of the detector is not corrupted by 1/f noise. The signal is amplified by the baseband (BB) stage, and the output of the BB amplifier is shown in Figure 3-14(e). The signal is then mixed with the output SS clock, i.e., CLK_{BB} at (f). At the same time, the DC offset and 1/f noise of the envelope detector and BB amplifiers are upconverted to f_{SS} and its higher harmonics, which is low-pass filtered at the chopper output as shown in Figure 3-14(g).

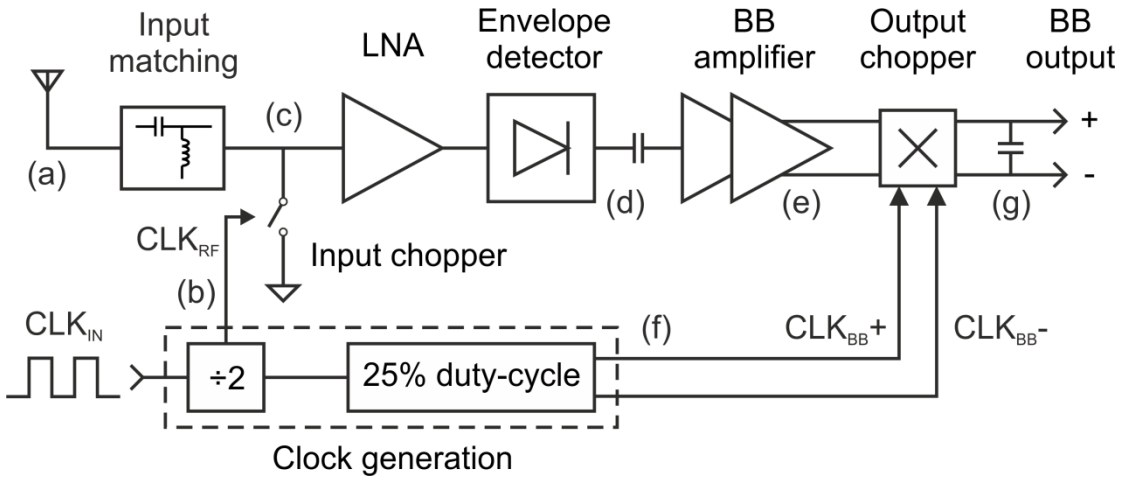


Figure 3-13: Block diagram of the proof-of-concept receiver.

Due to the limited bandwidth in the Rx signal chain, the signal is delayed between the input and output choppers. To compensate for the delay, the CLK_{BB} is delayed with respect to CLK_{RF} by 1/4 clock cycle. This is achieved by using 25% duty-cycle instead of 50% in CLK_{BB} as shown in Figure 3-14(f), to capture the peak of the BB amplifier output. The clock generation is realized by clock division and low complexity logic operations on the divided clock. Together with the passive input switch and output chopper, the synchronized-switching technique adds only negligible area and power overhead to a conventional envelope detection receiver.

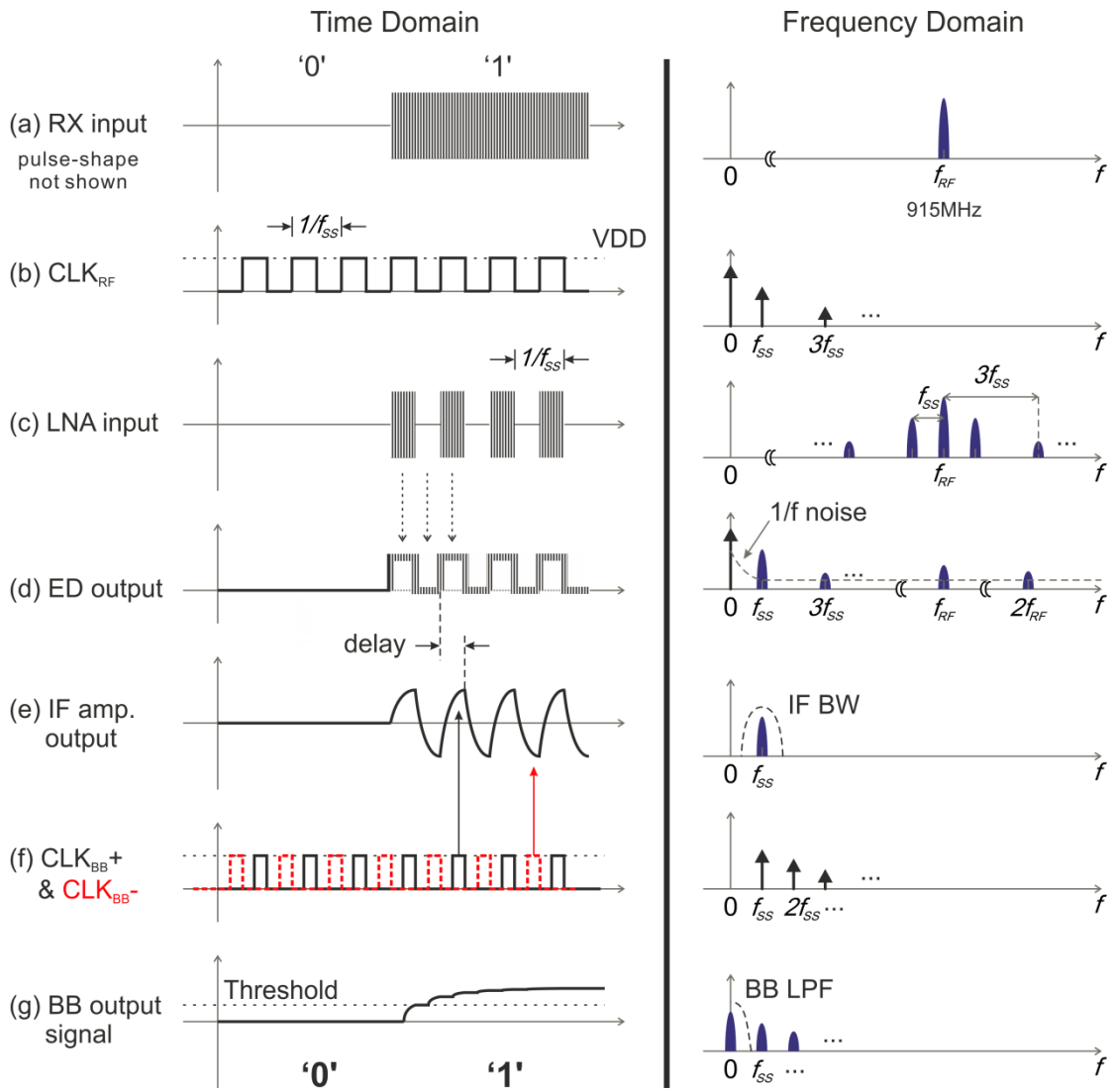


Figure 3-14: Illustration of synchronized-switching envelope detection.

The effect of the proposed technique is shown in Figure 3-15. The single-sideband noise figure (NF_{SSB}) of a typical envelope detection receiver is simulated on the circuit level. With synchronized-switching, the 1/f noise of the receiver is clearly suppressed. Below 1kHz, the noise figure improvement is higher than 20dB. The integrated noise between 1kHz and 100kHz is reduced by 18.7dB when the proposed technique is activated. Although the noise performance of a nonlinear envelope detection receiver cannot be fully characterized by its noise figure [43], the simulation verifies the suppression of 1/f noise by the synchro-nized-switching technique.

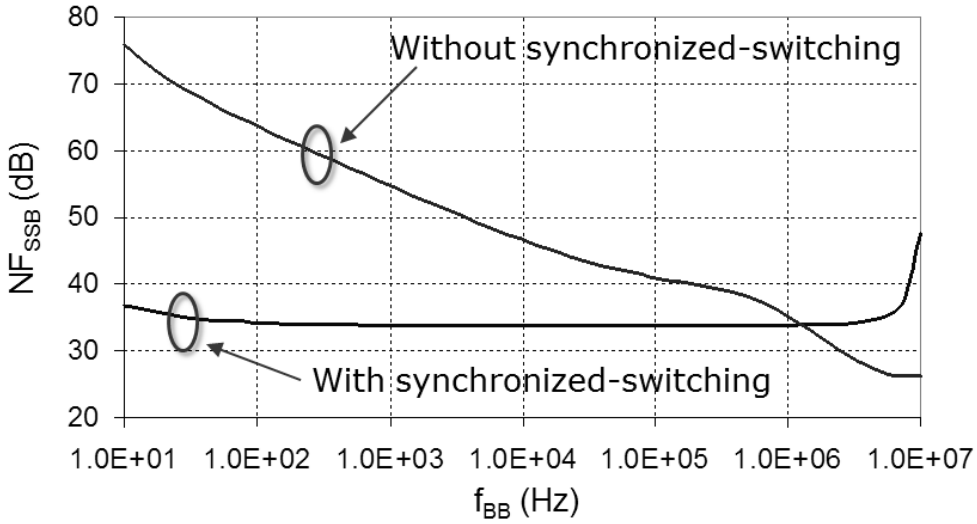


Figure 3-15: Effect of synchronized-switching operation on receiver noise.

3.2.2 Circuit Implementation

The receiver is designed in the same 90nm CMOS technology as the proof-of-concept transmitter. Although the nominal supply voltage in this technology is 1.2V, the analog front-end is designed to operate from 0.5V supply in order to achieve low power consumption.

3.2.2.1 RF Front-end

The RF front-end of the receiver consists of the LNA and the envelope detector. Typically, the sensitivity of envelope detection receivers is limited by the envelope detector [39], [43], [44]. Therefore, to improve Rx sensitivity, the gain of the LNA is maximized within the power budget.

The schematic of the RF front-end is shown in Figure 3-16. The LNA is implemented as an NMOS cascode amplifier with inductive load. The input matching is realized using a capacitive transformer with on-chip capacitors and an off-chip high-Q inductor. Parasitics from chip packaging is included in the matching network design. Capacitors C_1 and C_2 transform the 50Ω source impedance into 5kΩ to obtain 20dB passive voltage gain. Inductor L_1 resonates with the total capacitance at the input of the LNA at the carrier frequency, and its resistive loss dominates the real part (approximately 5kΩ) of the input impedance of the LNA.

The resonance frequency can be tuned via a tuning voltage applied to C_3 to correct the center frequency shift due to component variations. The DC bias of M_1 (i.e., $V_{B,LNA}$) is provided by a current mirror (not shown) via a 100kΩ resistor. Another varactor C_4 is added to the amplifier load to tune the output resonator (with the load inductor L_2) to the carrier frequency. Similar to L_1, L_2 is also an off-chip inductor with Q-factor higher than 50 to maximize the gain. By replacing L_1 and L_2 externally, the receiver is able to operate in different frequency bands, e.g. 915MHz or 2.4GHz ISM bands. The input SS grounding switch (M_4) is implemented as an NMOS transistor between the input of the LNA and ground. The LNA is designed with 26dB voltage gain, while consuming 54 μA excluding biasing.

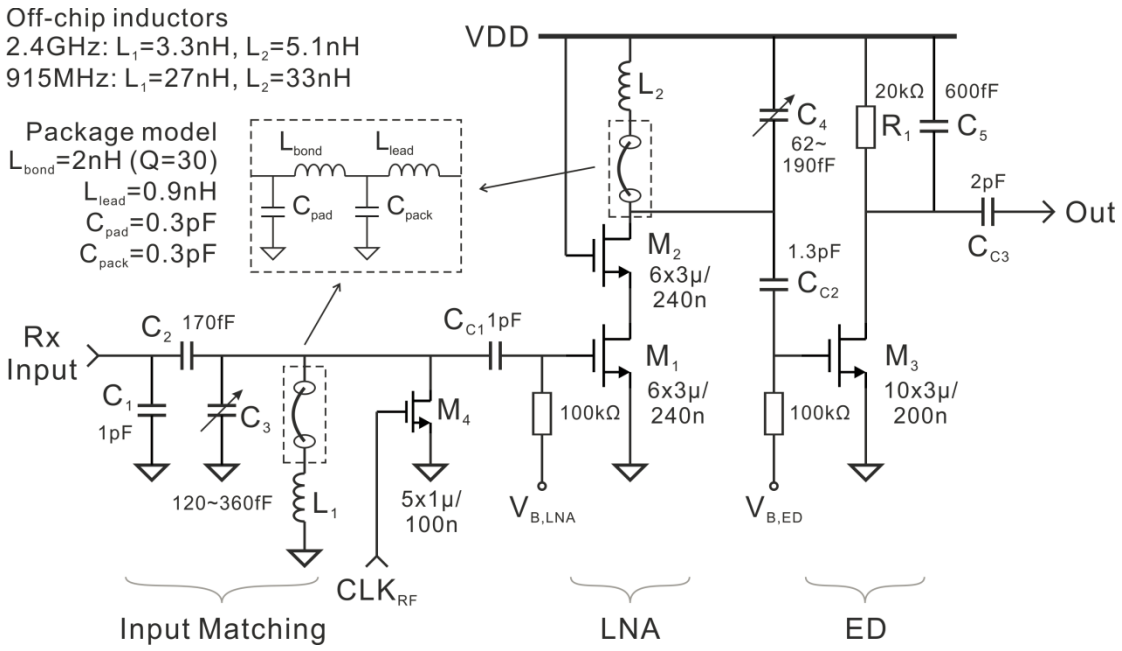


Figure 3-16: Schematic of the LNA and envelope detector (bias circuits not shown).

The envelope detector is implemented as a single NMOS transistor (M_3) with an RC load. The squaring operation is achieved using the 2nd-order nonlinearity of the NMOS transistor. The RF voltage at the output of the LNA is squared, and the resulting low-frequency component is proportional to the square of the input amplitude. Besides the 2nd-order term, there is also the linear term in the NMOS drain current at the carrier frequency, which is suppressed by the low-pass RC load. In conventional envelope detectors, the desired output signal resides at DC, and therefore it needs to be separated from the bias point using a duplicated

branch which provides a reference voltage [39], [43], [44]. In this work the desired output signal is moved up to f_{SS} by the synchronized-switching operation, so the signal is separated from DC simply by AC coupling at the envelope detector output. The envelope detector consumes 10 µA under 0.5V V_{DD}.

3.2.2.2 Analog Baseband

The analog baseband consists of a 2-stage amplifier that amplifies the output signal of the envelope detector at f_{SS}, and an output chopper that downconverts the signal back to DC. The input stage of the BB amplifier is shown in Figure 3-17. The input amplifier stage converts the single-ended input signal into differential format. It is implemented as an NMOS differential pair M_1 and M_2 biased in weak-inversion to increase the g_m efficiency to 24S/A. The load resistors R_L produce less noise than current source that gives larger gain. The programmable source degeneration resistor, R_{DEG1}, is used to adjust the gain. At 10 µW power consumption, the gain is -6dB and 14dB in low and high gain modes, respectively.

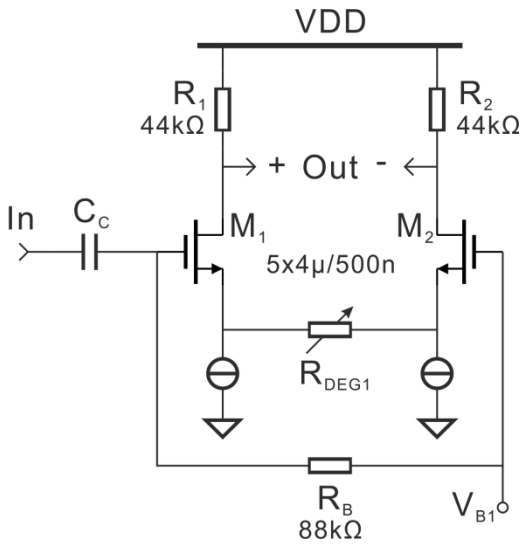
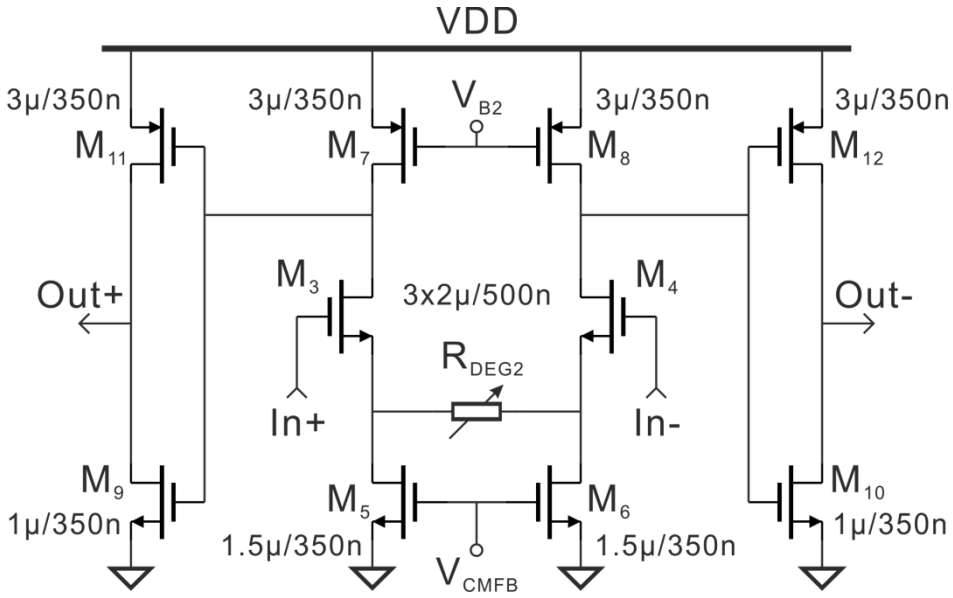
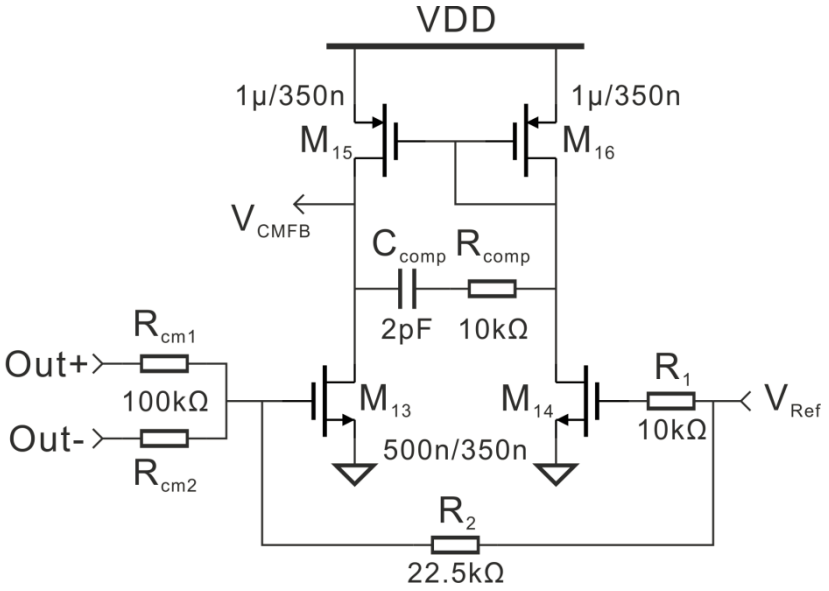


Figure 3-17: Input stage of the baseband amplifier.



(a) signal path



(b) common-mode feedback (CMFB)

Figure 3-18: Output stage of the baseband amplifier.

The output stage of the baseband amplifier is a 2-stage fully-differential amplifier shown in Figure 3-18(a). The 1st stage is NMOS differential pair M_3 and M_4 loaded by PMOS current sources M_7 and M_8. To fully utilize the voltage headroom, the 2nd stage is a push-pull output stage M_9-M_{12}, so that the output signal can swing from rail to rail. This amplifier is used in open-loop instead of the closed-loop configuration due to the limited power budget

and gain. On the other hand, frequency compensation is not required for differential mode operation. A common-mode feedback (CMFB) circuit shown in Figure 3-18(b) is used to set the output common-mode (CM) voltage to V_{Ref}, which is set to $V_{DD}/2$. Frequency compensation of the CMFB loop is achieved by capacitor C_{comp} and resistor R_{comp}. Two gain settings are available by programming the source degeneration resistance R_{DEG2}. At 11 µW power consumption, this output amplifier stage delivers up to 30dB gain.

AC coupling at the input of the BB amplifier (M_1) and the bandwidth of the amplifier result in a bandpass frequency response. The -3dB bandwidth is 1.5MHz and 30MHz, and the passband gain is 41dB in the maximum gain mode.

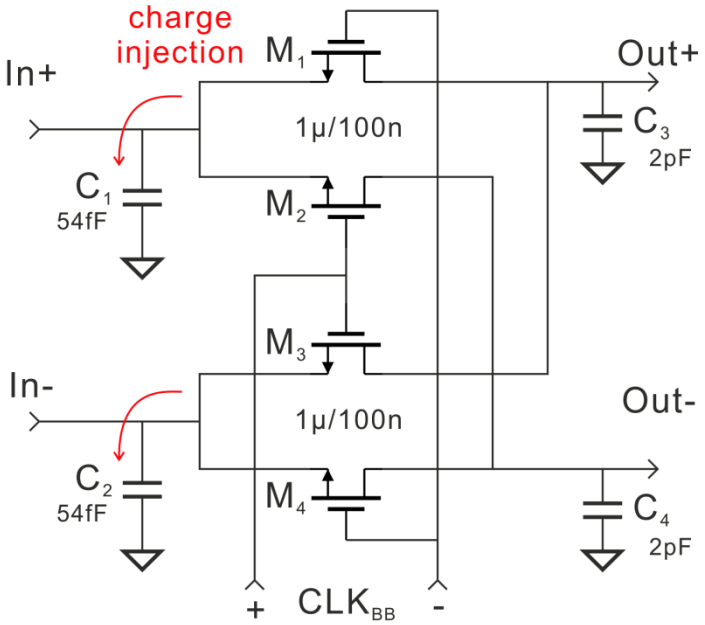


Figure 3-19: Schematic of the output chopper.

The schematic of the output chopper is shown in Figure 3-19. It consists of 4 NMOS switches and 4 capacitors. The switches form a Gilbert switching quad driven by CLK_{BB}+/-, so that the output signal of the BB amplifier is mixed with the 10MHz clock signal. The output of the chopper is sampled and held on capacitors C_3 and C_4, with bandwidth limited to 500kHz. The charge-injection effect of MOS switches [99] does not affect the differential signal. However, the common-mode voltage will be affected when M_1-M_4 are switched on and off. The charge injected to the output nodes of the chopper is absorbed by capacitor C_3

and C_4. However, at the input of the chopper, the injected charge sees high impedance from the output of the baseband amplifier, and large voltage spikes can be introduced. Capacitors C_1 and C_2 are added to reduce the impedance at f_{SS}, and to absorb the injected charge to reduce the perturbation to the input common-mode voltage [99].

Although other analog circuits are designed for 0.5V supply voltage, the synchronized-switching transistors, i.e., the NMOS grounding switch at the Rx input and the chopper at the output, are driven by 1V clock signals. This is to avoid performance degradation due to higher switch resistance when a 0.5V clock level is used. A dedicated 1V supply is provided for the clock generation circuits in this work. Clock-boosting techniques [56] could be adopted so that a 1V clock is generated from a single 0.5V supply.

3.2.2.3 Clock generation

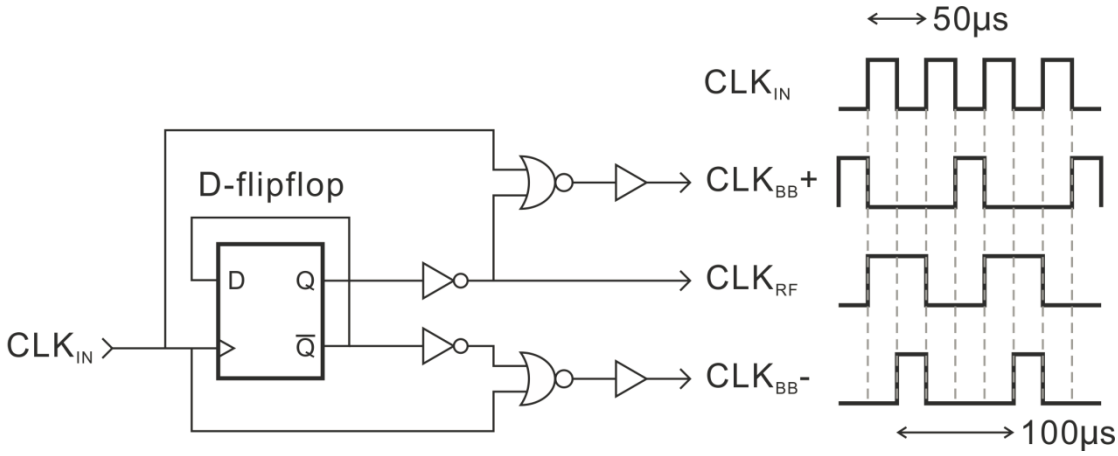


Figure 3-20: Block diagram of the clock generation module.

The clock generation circuit is illustrated in Figure 3-20. The synchronized-switching clocks CLK_{RF} and CLK_{BB} are derived from an external master clock (CLK_{IN}) at 20MHz. The master clock is divided by 2 using a standard-cell D-type flip-flop. The resulting 10MHz, 50% duty-cycled output clock is used as the input SS clock CLK_{RF}, while the 25% duty-cycled CLK_{BB}+/- is generated using the logic gates shown in Figure 3-20. The clock generation

module is designed for 1V supply voltage to provide 1V clock swing for the switches, and the power consumption is 3μW when it is active.

3.2.2.4 Receiver Prototype

The complete receiver front-end chip is shown in Figure 3-21. The active circuit area is 0.36mm^2 excluding bondpads. The chip is wire-bonded in a QFN56 package and attached to a 4-layer PCB together with the off-chip inductors for evaluation.

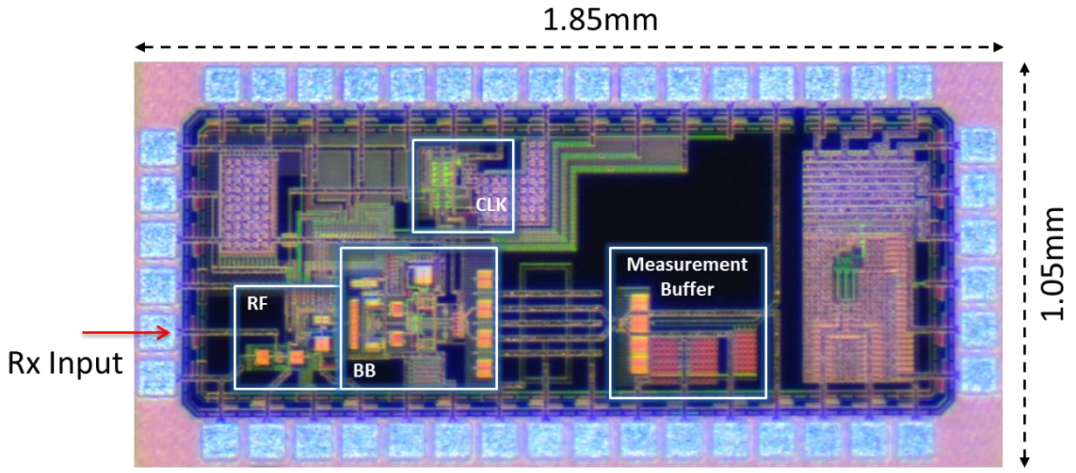


Figure 3-21: Chip micrograph of the proof-of-concept receiver.

3.2.3 Evaluation Results

The receiver is evaluated at the 915MHz and 2.4GHz bands using different off-chip inductors. To verify the suppression of low-frequency noise, a 915MHz OOK modulated signal at -80dBm is provided to the receiver, with variable modulation rate from 10Hz to 500kHz. The Rx output signal and noise level is plotted in Figure 3-22, where both the noise floor and the signal level are flat from 30Hz to 100kHz. The receiver DC offset is also reduced to less than 1mV in typical samples, versus tens of mV when the synchronized-switching operation is disabled.

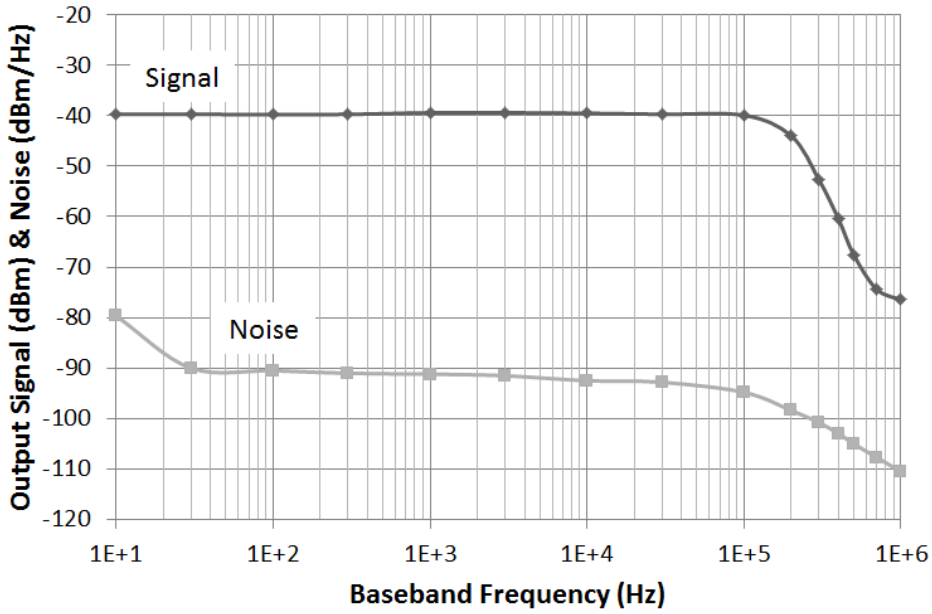


Figure 3-22: Measured output signal level and noise floor for a 915MHz receiver.

In this chip implementation, the output signal is not bandlimited to the signal bandwidth due to the lack of an explicit low-pass filter (LPF) at the output stage. To estimate the sensitivity that can be achieved when a LPF is added, it is assumed that the filter suppresses noise at frequencies higher than the modulation rate, i.e., 100kHz LPF bandwidth for 100kbps OOK modulation. Figure 3-23 shows the SNR for different carrier and data rate settings calculated based on measured output signal levels and noise floor. Demodulation of the OOK Rx signal requires an SNR higher than 11dB to achieve a bit-error-rate (BER) lower than 10^{-3} [88]. For 100kbps OOK, the 915MHz receiver sensitivity is -75dBm (SNR > 11dB) assuming the output is low-pass filtered with 100kHz bandwidth. If the data rate is reduced to 10kbps and noise beyond 10kHz is filtered, the sensitivity improves by another 5dB (instead of 10dB due to the quadratic input/output transfer of the detector, i.e., $V_{OUT} = k \cdot V_{IN}^2$). For the 2.4GHz receiver, the measured sensitivity based on the same assumption is -64dBm and -69dBm at 100kbps and 10kbps, respectively.

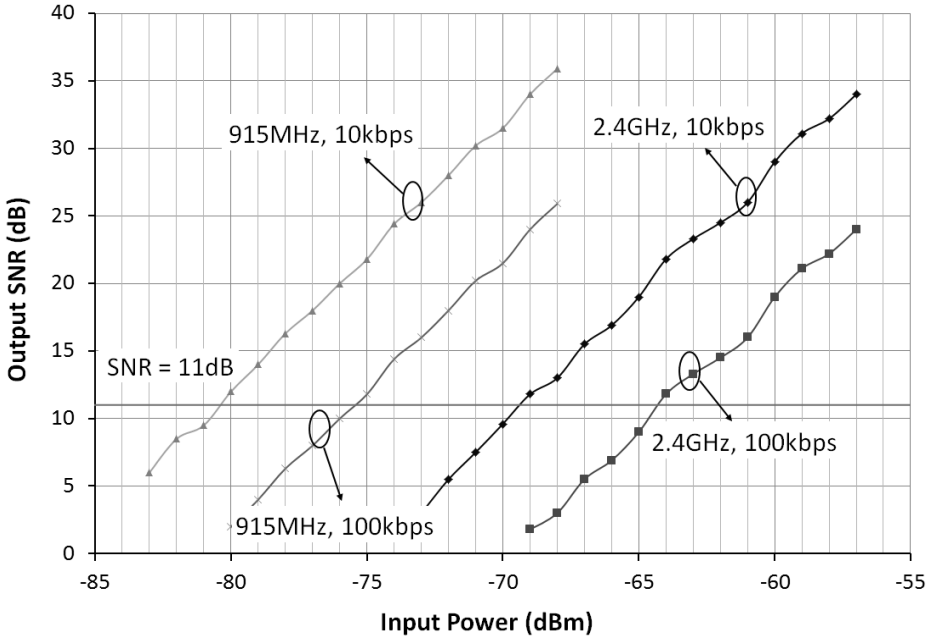
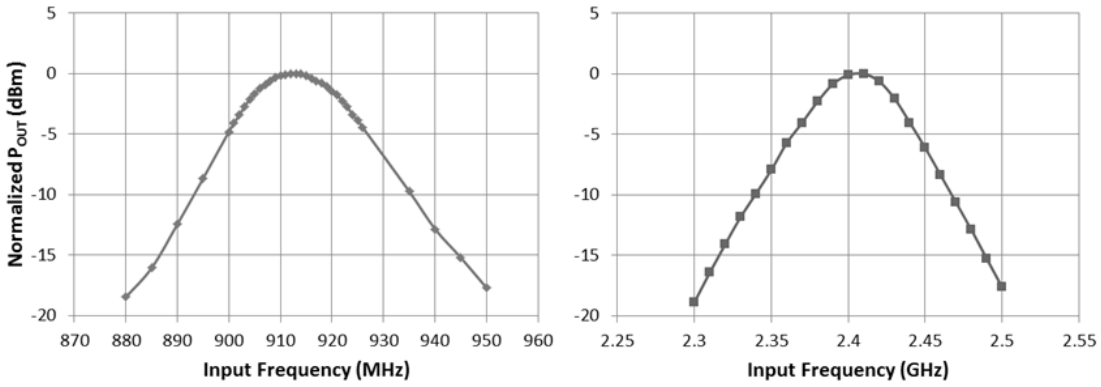


Figure 3-23: Measured output SNR for different carrier and data rate settings.

The measured frequency selectivity of the receiver is shown in Figure 3-24. The -3dB RF bandwidths are 21MHz and 59MHz for the 915MHz and 2.4GHz receivers, respectively. The -10dB RF bandwidths are 42MHz and 127MHz for the 915MHz and 2.4GHz receivers, respectively. While out-of-band interference can be filtered out, the receiver is still susceptible to in-band interference.



(a) (b)

Figure 3-24: Measured frequency selectivity of the receiver in (a) 915MHz and (b) 2.4GHz configurations.

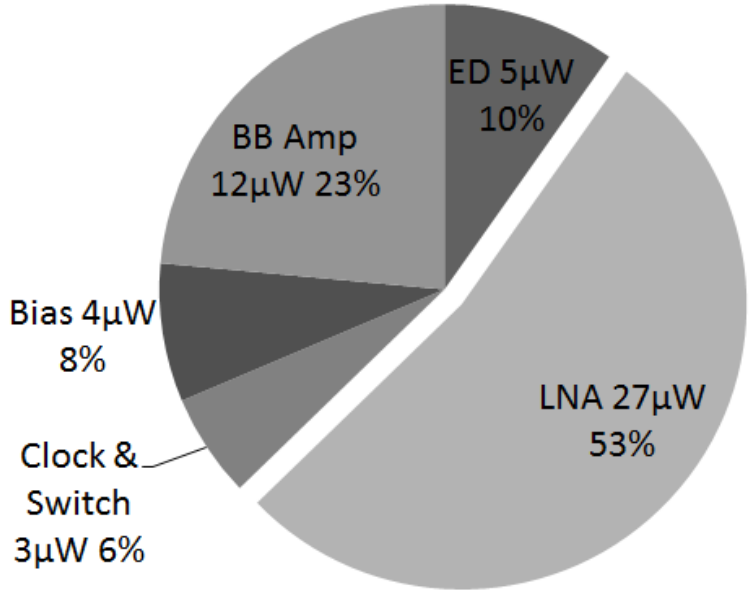


Figure 3-25: Power breakdown of the Rx front-end.

The power consumption breakdown of the receiver is shown in Figure 3-25. More than half of the power is consumed by the LNA, which is the circuit block operating at the highest frequency. The total power consumption of the Rx front-end from both the 1V supply for the clock generation circuits, and 0.5V supply for the rest of the receiver is 51 µW.

3.2.4 Summary

The proof-of-concept Rx front-end adopts the RF envelope detection to achieve the 50 µW power consumption required for a wake-up receiver. A novel synchronized-switching technique is implemented to enhance the receiver sensitivity for low-date operations, with little penalty in power consumption. Table 3-2 compares this work to state-of-the-art low-power OOK receiver implementations. This receiver achieves similar power consumption as [43]. The sensitivity at 900MHz is better than 2.4GHz due to higher RF gain available at lower frequencies. Compared to [44], which is also an envelope detection receiver, this receiver achieves better sensitivity at both 900MHz and 2.4GHz carrier frequencies with lower power consumption. The receiver in [39] which also operates at 900MHz consumes much higher power (500µW to 2.5mW), while its sensitivity is still much lower than this work even if it is

normalized to the same date rate (i.e., 100kbps). An ultra-wideband (UWB) receiver [47] is also listed for comparison. The UWB receiver operates at 4.35GHz carrier frequency, which allows full integration of the front-end components. At 2Mbps data rate, the UWB receiver achieves -76.5dBm sensitivity while consuming 750μW. If its power consumption scales linearly as the data rate, then it would consume 37.5μW at 100kbps, which is very competitive. However, as is analyzed in Chapter 1, such UWB receivers consume significantly higher power when listening to the channel and searching for wireless events. The use of high-Q surface-acoustic wave (SAW) and film bulk-acoustic wave (FBAR) filters and resonators in [39], [43], [44] helps the receivers to reject out-of-band interference. In this work, the selectivity is limited by the front-end bandwidth shown in Figure 3-24. The poor interference rejection of envelope detection receivers must be addressed in following chapters.

Table 3-2: State-of-the-art low-power OOK receiver comparison.

References	**Frequency (GHz)**	**Sensitivity (dBm)**	**P_{DC} (μW)**	**External Components**
[44]	1.9	-50 @ 100kbps	65	1 FBAR resonator
[39]	0.9	-37 to -65 @ 1Mbps	500 to 2500	2 Inductors & 1 SAW filter
[43]	2	-72 @ 100kbps	52	1 FBAR resonator
[47]	4.35	-76.5 @ 2Mbps	11560 (searching) 750 (2Mbps)	None
This work	0.9	-80 @ 10kbps -75 @ 100kbps	51	2 Inductors
	2.4	-69 @ 10kbps -64 @ 100kbps		

3.3 Conclusion

The proof-of-concept Tx and Rx circuits successfully verify the low power consumption and high efficiency of the direct-modulation transmitter and envelope detection receiver architectures proposed in the last chapter. However, several improvements are necessary for

event-driven radio applications. For the transmitter, the power consumption needs to be reduced below 1mW without compromising the power efficiency. Moreover, the absence of a PLL implies that the carrier frequency needs to be manually adjusted, which is impractical when a large number of radio nodes are deployed. The receiver is sensitive to input signals in a wide frequency range. This degrades its reliability when interferers are present at nearby frequencies. Further improvement of the sensitivity is also desired in order to reach an 80dB link budget with a Tx output level below 0dBm.

To achieve these improvements required by event-driven applications, circuit and system techniques will be investigated. A new generation of transceiver demonstrators will be built in subsequent chapters.

Chapter 4

Enhancement of the Envelope Detection Radio

To achieve the specifications desired for generic event-driven radio applications, the performance of the proof-of-concept transceiver circuits should be improved. In this chapter, the bottlenecks of the envelope detection radio are analyzed, and a novel 2-tone envelope detection scheme is proposed to enhance the sensitivity and selectivity of such radio transceivers.

4.1 Noise and Sensitivity of Envelope Detection Receivers

State-of-the-art envelope detection receivers [39], [43], [44] exhibit insufficient sensitivity for event-driven radio applications. The proof-of-concept receiver in Chapter 3, though achieving better sensitivity thanks to the synchronized-switching technique, still lacks several dB in sensitivity when paired with a transmitter consuming 1mW, or below. Furthermore, due to the nonlinear operation of the envelope detector, it is difficult to predict the Rx sensitivity. Although there have been several attempts to analyze the nonlinear noise characteristics of an envelope detector [101]–[103], little insight has been provided for optimizing the sensitivity to circuit designers.

In this section, the noise characteristics of the envelope detection receiver are analyzed and modeled, and sensitivity optimization guidelines are proposed. In addition, the synchronized-switching envelope detection technique is also investigated.

4.1.1 Nonlinear Noise Analysis

A generic envelope detection Rx front-end is illustrated in Figure 4-1. The envelope detector (ED) downconverts the RF signal by squaring. For an input signal of

$$S_{IN} = A(t)\cos\left(2\pi f_C t + \varphi_C\right), \tag{4.1}$$

the output of the squaring operation is

$$S_{OUT} = kS_{IN}^2 = kA^2(t)\frac{1+\cos\left(2\pi \cdot 2 f_C t + 2\varphi_C\right)}{2}, \tag{4.2}$$

where A(t) is the amplitude of the RF signal, f_C is the carrier frequency, φ_C is the carrier phase, and k is a scaling factor for the envelope detector, which is related to circuit and device parameters. The squaring operation generates a baseband (BB) component

$$S_{OUT,BB} = \frac{k}{2}A^2(t), \tag{4.3}$$

and also a high-frequency component at $2f_C$ which is removed by the low-pass filtering (LPF).

Front-end gain stages are often added to boost up the signal level, so that the output of the envelope detector is strong enough to overcome the baseband (BB) noise generated by the BB stages. However, RF amplifiers also add noise to the signal and degrade the signal-to-noise ratio (SNR) of the receiver. The impact of RF and BB noise sources will be analyzed separately.

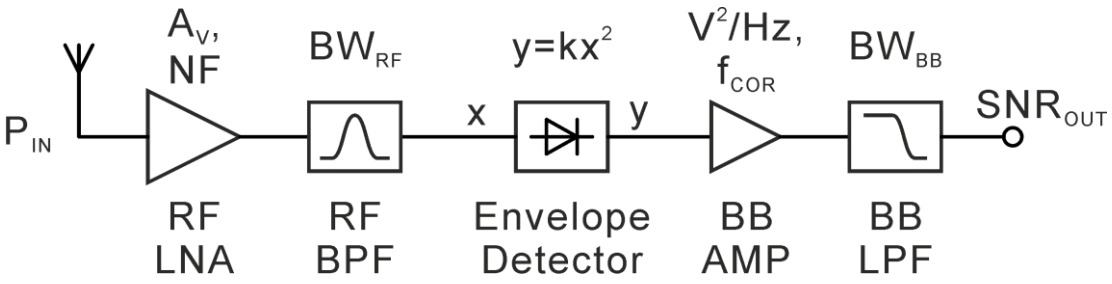


Figure 4-1: Block diagram of a generic envelope detection receiver front-end.

4.1.1.1 RF Front-end Noise

Noise in the RF front-end is generated by the low-noise amplifier (LNA) and the RF part of the envelope detector. It is assumed that the RF front-end is linear to simplify the nonlinear anal-

ysis, and that nonlinearity in the receiver chain is dominated by the squaring operation of the envelope detector. As a result, the impact of the RF front-end noise can be lumped into the noise factor of the front-end,

$$PSD_{ED,IN} = K_B T \cdot A_V^2 \cdot F_{FE}\,, \tag{4.4}$$

where $PSD_{ED,IN}$ (in mW/Hz) is the noise power spectral density (PSD) at the ED input, A_V is the voltage gain of the LNA, and F_{FE} is the front-end noise factor. The thermal noise floor is K_BT, which is equal to 3.981×10^{-18} mW/Hz, or -174dBm/Hz at room temperature. Typically, the impedance level is matched at the receiver input. In fact, impedance mismatch will be reflected in the noise factor F_{FE}, and the choice of gain quantities (e.g., voltage gain vs. power gain) has no impact on the following analysis since the signal and input equivalent noise undergo the same transfer in the RF front-end. In the following analysis, the on-chip impedance level is normalizes to 1Ω, so that the signal and noise power is written as the square of their voltages.

The envelope detector is in between the RF front-end and the baseband, and its noise sources are also divided in two parts, noise sources prior to self-mixing, which should be included in the calculation of RF front-end noise in (4.4), and noise sources after self-mixing, which should be included in the calculation of baseband noise in the next sub-section.

The noise at the ED input is centered at the carrier frequency with a bandwidth of BW_{RF}, which is determined by the bandpass response of the LNA. To simplify the calculation, the in-band noise is assumed to be white Gaussian noise, and the out-of-band noise is assumed to be zero (i.e., a brickwall approximation, which overestimates total noise), so that the total noise power at the ED input, $\sigma_{ED,IN}^2$, is

$$\sigma_{ED,IN}^2 = PSD_{ED,IN} \cdot BW_{RF}\,. \tag{4.5}$$

On the other hand, the signal power at the ED input, $S_{ED,IN}^2$, is

$$S_{ED,IN}^2 = P_{IN} \cdot A_V^2\,, \tag{4.6}$$

where P_{IN} is the RF input power, and $S_{ED,IN}$ is the signal voltage. The ED input in the voltage domain is given as

$$x = S_{ED,IN} + N_{ED,IN}, \tag{4.7}$$

where $N_{ED,IN}$ is the noise voltages, and it has zero mean and variance of $\sigma^2_{ED,IN}$. After squaring, the output noise is

$$y = kx^2 = k\left(S^2_{ED,IN} + 2S_{ED,IN}N_{ED,IN} + N^2_{ED,IN}\right). \tag{4.8}$$

The variance of the output noise in (4.8) is calculated by making use of the 1st, 2nd, 3rd and 4th central moments of Gaussian distribution, which are 0, σ^2, 0 and $3\sigma^4$, respectively [104]

$$\begin{aligned}
\sigma_y^2 &= E\left(y^2\right) - \left(E\left(y\right)\right)^2 \\
&= k^2 E\left(\left(S^2_{ED,IN} + 2S_{ED,IN}N_{ED,IN} + N^2_{ED,IN}\right)^2\right) - k^2\left(E\left(S^2_{ED,IN} + 2S_{ED,IN}N_{ED,IN} + N^2_{ED,IN}\right)\right)^2 \\
&= k^2\left(S^4_{ED,IN} + 6S^2_{ED,IN}E\left(N^2_{ED,IN}\right) + E\left(N^4_{ED,IN}\right)\right) - k^2\left(S^2_{ED,IN} + E\left(N^2_{ED,IN}\right)\right)^2 \\
&= 4k^2 S^2_{ED,IN}\sigma^2_{ED,IN} + 2k^2\sigma^4_{ED,IN}.
\end{aligned} \tag{4.9}$$

Since one-half of the signal and noise power resides at $2f_C$, and the other half resides at BB, the BB signal and noise power at the envelope detector output is

$$S^2_{ED,OUT} = k^2 S^4_{ED,IN} / 2, \tag{4.10}$$

and

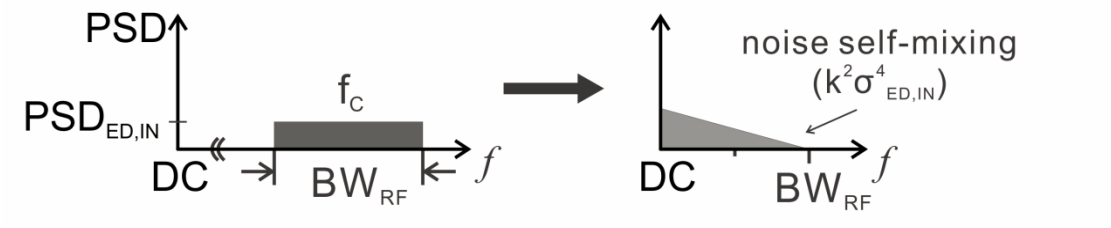
$$\sigma^2_{ED,OUT} = \sigma_y^2 / 2 = 2k^2 S^2_{ED,IN}\sigma^2_{ED,IN} + k^2\sigma^4_{ED,IN}, \tag{4.11}$$

respectively. The noise in (4.11) comes from two mechanisms: the mixing between the signal and noise, i.e., $2k^2 S^2_{ED,IN}\sigma^2_{ED,IN}$, and the self-mixing of noise, i.e., $k^2\sigma^4_{ED,IN}$. For the self-mixed noise, convolution of the band-pass filtered white noise spectrum results in a triangular shaped output PSD between DC and BW_{RF} as shown in Figure 4-2(a). For the noise generated by mixing with the input signal, the baseband noise spans uniformly from DC to $BW_{RF}/2$ as shown in Figure 4-2(b), because the input signal is located in the middle of BW_{RF}.

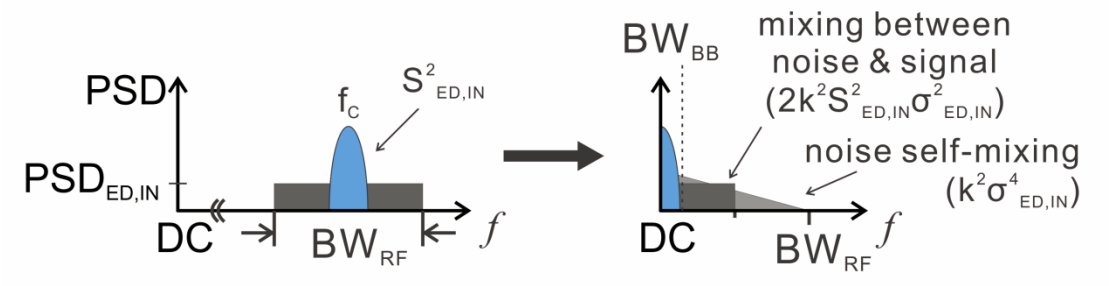
Therefore, the noise PSD at the ED output can be written as:

$$PSD_{ED,OUT} = \frac{2k^2 S^2_{ED,IN}\sigma^2_{ED,IN}}{BW_{RF}/2} + \frac{k^2\sigma^4_{ED,IN}\cdot 2\left(BW_{RF} - f\right)}{BW_{RF}\cdot BW_{RF}}, \tag{4.12}$$

where f is the baseband frequency in the range from DC to f=BW_{RF}.



(a) noise self-mixing



(b) mixing between noise and signal

Figure 4-2: Illustration of noise spectral distribution during envelope detection.

A low-pass filter (LPF) is usually adopted to suppress the noise power beyond the base-band signal bandwidth, i.e., BW_{BB}, so that the Rx output SNR is improved. For now we assume the baseband circuits are noiseless with a passband gain of 1, so the total noise power at the Rx output, σ_{OUT}^2, is

$$\sigma_{OUT}^2 = \int_0^{BW_{BB}} PSD_{ED,OUT}\,df \approx \left(4k^2 S_{ED,IN}^2 \sigma_{ED,IN}^2 + 2k^2 \sigma_{ED,IN}^4\right)\frac{BW_{BB}}{BW_{RF}}, \tag{4.13}$$

valid for BW_{BB} much smaller than BW_{RF}. Together with (4.10), the Rx output SNR is

$$SNR_{OUT} = \frac{S_{ED,OUT}^2}{\sigma_{OUT}^2} = \frac{S_{ED,IN}^4}{8S_{ED,IN}^2\sigma_{ED,IN}^2 + 4\sigma_{ED,IN}^4}\cdot\frac{BW_{RF}}{BW_{BB}}. \tag{4.14}$$

As it requires an SNR higher than 11dB (theoretically) to demodulate OOK signal with bit-error-rate (BER) lower than 10^{-3} [88], the minimal Rx input power to satisfy 11dB output SNR is defined as the sensitivity. By combining (4.4), (4.5), (4.6) and (4.14), the minimal detectable signal power (P_{MDS}, or the sensitivity) can be found as

$$P_{MDS} = 4SNR_{MIN}BW_{BB}F_{FE}K_BT + 2F_{FE}K_BT\sqrt{4BW_{BB}^2SNR_{MIN}^2 + BW_{RF}BW_{BB}SNR_{MIN}}. \tag{4.15}$$

Two scenarios are identified to evaluate various factors affecting Rx sensitivity in (4.15). The first scenario is when BW_{RF} is small, so that the output noise is dominated by the mixing between the signal and noise. Thus, the sensitivity of the receiver, $P_{MDS,SN}$ (in mW) is

$$P_{MDS,SN} = 8K_B T \cdot F_{FE} \cdot BW_{BB} \cdot SNR_{MIN} . \quad (4.16)$$

The second scenario is when BW_{RF} is large, so that the output noise is dominated by the self-mixed noise. Consequently, the sensitivity, $P_{MDS,N2}$ (in mW) of the receiver is

$$P_{MDS,N2} = 2K_B T \cdot F_{FE} \cdot \sqrt{BW_{RF} \cdot BW_{BB} \cdot SNR_{MIN}} . \quad (4.17)$$

The solution in (4.15) is plotted on Figure 4-3, together with the approximations of (4.16) and (4.17). The data rate is 10kbps, so a BW_{BB} of 10kHz is assumed. When BW_{RF} is large, the sensitivity matches the approximation in (4.17) as expected. When it decreases, the sensitivity improves by 5dB per decade until it reaches the lower limit given by (4.16). In addition, the sensitivity is linearly related to F_{FE} in both (4.16) and (4.17), which dictates that the sensitivity difference is equal to the difference between the NF curves.

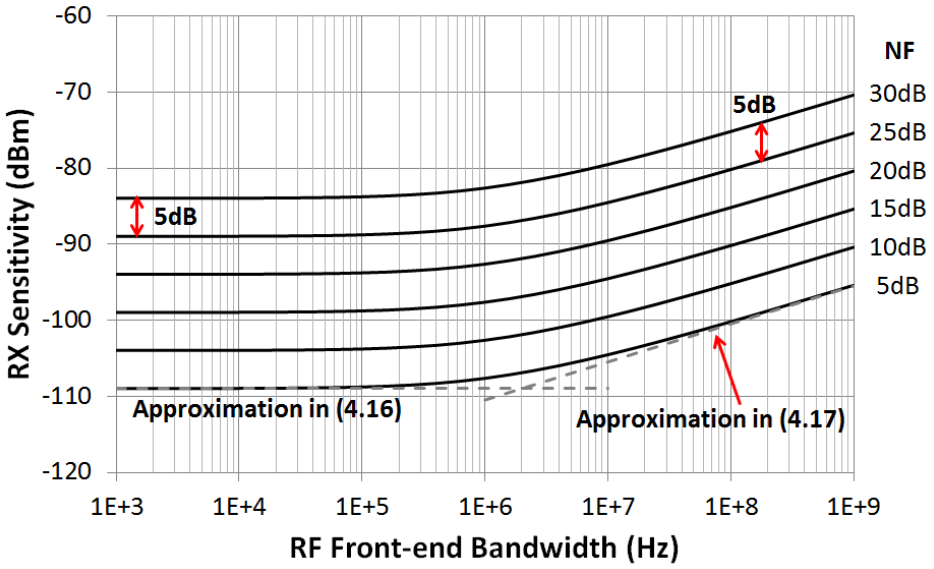


Figure 4-3: Rx sensitivity at 10kbps with different noise figure (NF) and RF bandwidth when limited by RF stage noise.

Since the noise and signal are both amplified by the RF front-end gain A_V, the Rx sensitivity is not directly related to A_V. The influence of A_V on the RF stage noise is already re-

flected by the total noise figure of the RF stage. However, as will be shown in the next sub-section, the gain of the RF front-end has a quadratic impact on the Rx sensitivity when baseband noise is dominant.

4.1.1.2 Baseband Noise

So far the baseband is assumed noiseless. In reality, the BB noise will also degrade the Rx sensitivity. To analyze the impact of the BB noise, the RF stages are now assumed noiseless. The root-mean-square (RMS) signal level at the input of the baseband stages, $V_{IN,BB}$, is

$$V_{IN,BB} = \frac{k}{2} \cdot \left(A_V \cdot V_{IN} \right)^2 = \frac{k}{2} \cdot A_V^2 \cdot \frac{P_{IN}}{10}, \tag{4.18}$$

where V_{IN} is the input voltage (in V_{rms}), which is translated from the input power P_{IN} (in mW) assuming 50Ω impedance at the Rx input. The baseband SNR can be calculated by comparing the signal-to-noise ratio

$$SNR_{BB} = \frac{V_{IN,BB}^2}{\overline{v_{n,eq}^2}} = \frac{k^2 A_V^4 P_{IN}^2}{400} \Big/ \overline{v_{n,eq}^2}. \tag{4.19}$$

where $\overline{v_{n,eq}^2}$ is the input-referred BB noise power in V^2, and it should also include the baseband noise of the envelope detector. The Rx sensitivity at a BER of 10^{-3} is limited by BB noise, $P_{MDS,BB}$ (in mW), and is found at the 11dB SNR level for OOK modulation

$$P_{MDS,BB} = \frac{20\sqrt{\overline{v_{n,eq}^2} \cdot SNR_{MIN}}}{kA_V^2} = \frac{71 \cdot \overline{v_{n,eq}}}{kA_V^2}. \tag{4.20}$$

It can be seen from (4.20) that the sensitivity $P_{MDS,BB}$ is proportional to the BB input-referred noise voltage $\overline{v_{n,eq}}$ when limited by the BB noise. It is inversely proportional to the scaling factor of the envelope detector, k, and the square of the front-end gain, A_V. Therefore, for a 10dB increase in A_V the sensitivity improves by 20dB.

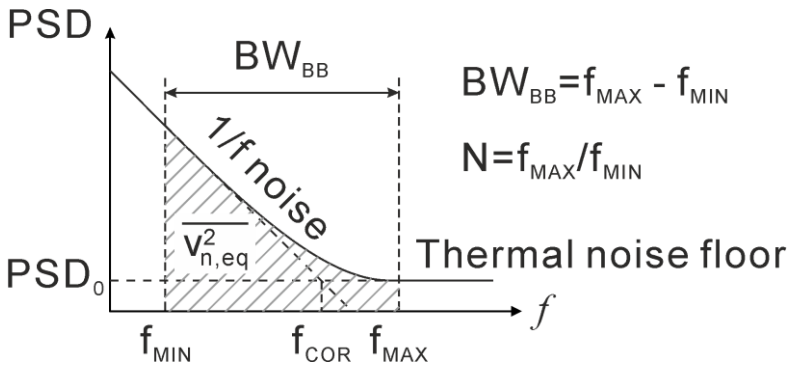


Figure 4-4: Typical power spectrum of the input-referred noise in baseband circuits.

The baseband noise consists of 1/f and thermal noise. The typical noise profile of baseband stages is illustrated in Figure 4-4. At frequencies below the 1/f noise corner (f_{COR}), the noise PSD is dominated by 1/f noise. At frequencies higher than f_{COR}, it is dominated by the thermal noise floor (PSD_0).

The noise power $\overline{v_{n,eq}^2}$ is obtained by integrating the noise PSD from the lowest (f_{MIN}) to the highest frequency of interest (f_{MAX}). Frequency f_{MIN} should not be zero, otherwise the integration is unbounded as the 1/f noise is undefined at DC. In general, f_{MIN} is determined by the duration of observation, and it depends on the data rate and packet length in radio applications, as well as how the demodulation is carried out (i.e., either with a fixed or a dynamic threshold). For example, assuming a simple OOK detector which compares the analog signal of duration Ts to a fixed threshold, then f_{MIN} is approximately the inverse of the signal duration (i.e., 1/Ts), since signal or noise at frequencies below 1/Ts cannot be observed within Ts. The data rate determines how fast the signal changes, which is proportional to f_{MAX}. For generic analysis, f_{MAX} is assumed to be N times f_{MIN}, (i.e., $f_{MAX} = N f_{MIN}$), so that the total noise bandwidth is

$$BW_{BB} = f_{MAX} - f_{MIN} = (N-1) f_{MIN} . \tag{4.21}$$

Within the noise bandwidth, the total thermal noise power is

$$\overline{v_{n,th}^2} = PSD_0 \cdot BW_{BB} , \tag{4.22}$$

and the total 1/f noise power is

$$\overline{v_{n,1/f}^2} = \int_{f_{MIN}}^{f_{MAX}} PSD_{1/f}\,df = PSD_0 \cdot f_{COR} \cdot \ln(N). \tag{4.23}$$

Thus the total input-referred power of the baseband noise is

$$\overline{v_{n,eq}^2} = PSD_0\left(BW_{BB} + f_{COR} \cdot \ln(N)\right) \tag{4.24}$$

The sensitivity given in (20) can be rewritten as

$$P_{MDS,BB} = \frac{71}{kA_V^2}\sqrt{PSD_0\left(BW_{BB} + f_{COR} \cdot \ln(N)\right)} = \overline{P_{MDS,BB}}\sqrt{1+\frac{f_{COR}}{BW_{BB}}\ln(N)} \tag{4.25}$$

where

$$\overline{P_{MDS,BB}} = \frac{71}{kA_V^2}\sqrt{PSD_0 \cdot BW_{BB}} \tag{4.26}$$

represents the sensitivity when 1/f noise is ignored.

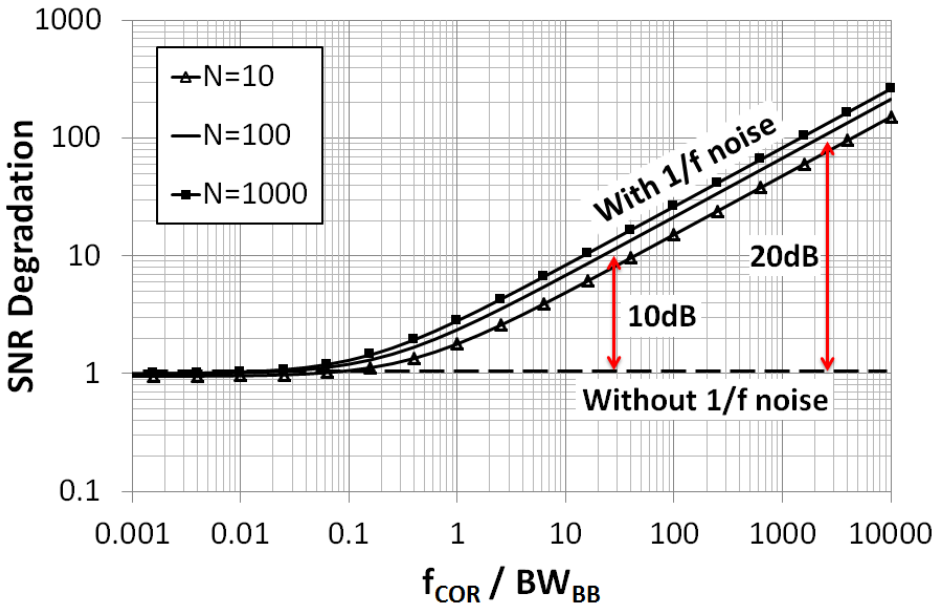


Figure 4-5: Rx sensitivity at different flicker noise corner frequency when RF noise is insignificant.

The normalized Rx sensitivity $P_{MDS,BB} / \overline{P_{MDS,BB}}$ is plotted as a function of f_{COR} normalized to BW_{BB} in Figure 4-5. As expected, the sensitivity decreases as f_{COR} increases. In nanometer CMOS technologies, the 1/f corner frequency of minimal-sized transistors can reach 10MHz, or beyond [61]. On the other hand, the data rate and hence BW_{BB} is lower than 100kbps for

event-driven radios. Consequently, the sensitivity degradation due to 1/f noise can be significant, e.g., up to 20dB as in Figure 4-5 if f_{COR} is above 10MHz and BW_{BB} is lower than 10kHz.

It is also shown in Figure 4-5 that the Rx sensitivity is a weak function of N. For a reasonable range of N (i.e., f_{MAX}/f_{MIN} = 10 to 1000), the 1/f noise has similar impact on the sensitivity.

4.1.2 Sensitivity Optimization

Several guidelines in the design of an envelope detection receiver may be formulated from the results of the foregoing noise analysis. Firstly, as shown in Figure 4-3, a narrowband RF front-end, such as the tuned RF amplifier used in the proof-of-concept receiver is preferred to a broadband front-end (e.g., the untuned amplifier used in [39]). At the same time, the RF front-end noise figure should be minimized within the available power budget.

In addition, the input-referred BB noise power should be minimized according to (4.20), so that a lower RF gain (A_V) is required for the desired sensitivity. As the RF amplifier is typically the most power hungry block in an envelope detection receiver, the reduction of its gain requirement can result in an overall power reduction.

Furthermore, as shown in Figure 4-5, 1/f noise degrades the sensitivity in low data rate receivers substantially. The sensitivity can be improved further if the 1/f noise is suppressed, as is the case in the synchronized-switching receiver.

With the help of the noise analysis, the dominant noise contributors in a receiver can be identified so that the Rx sensitivity can be optimized efficiently.

4.1.3 Synchronized-Switching Technique

To evaluate the sensitivity improvement from the synchronized-switching technique, the nonlinear noise analysis is expanded to the receiver model shown in Figure 4-6. The operation of this technique was described in Chapter 3, while its noise behavior is analyzed in this sub-section.

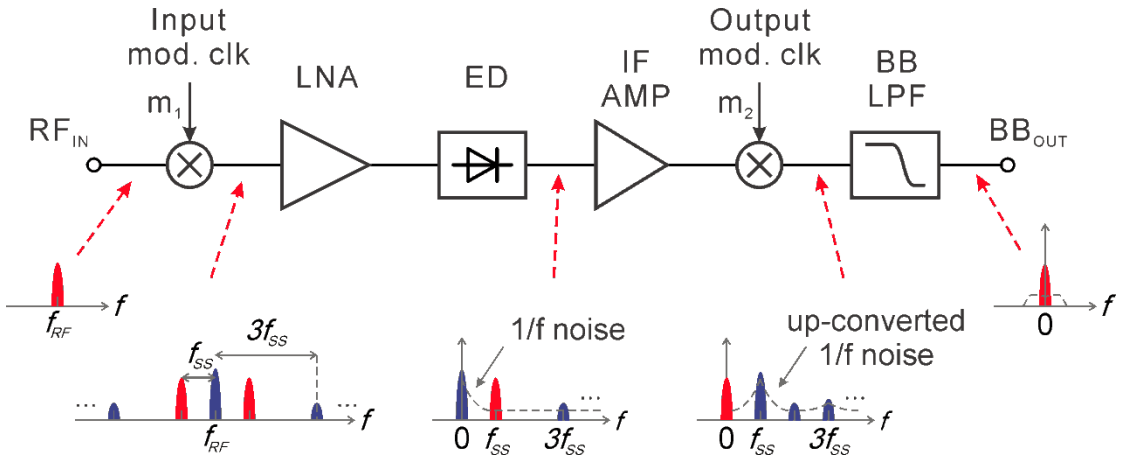


Figure 4-6: Modeling of a synchronized-switching envelope detection receiver.

The noise in the synchronized-switching Rx undergoes the same transformation as that in a conventional chopper-stabilized (CHS) amplifier. The synchronized-switching operation moves the 1/f noise out of the signal band so that the output noise floor of the receiver depends mainly on the *thermal* noise floor between DC and $f_{SS}/2$ [99]. On the other hand, the input chopper shorts the Rx input to ground for half of the time, so the signal power is reduced by 3dB. Meanwhile, thermal noise from the RF front-end and baseband stages remains constant. Therefore, to maintain the 11dB output SNR required for demodulation (BER of 10^{-3}), the receiver input signal needs to be 3dB higher than a conventional envelope detection receiver (assuming 1/f noise is negligible). Given these conditions, the sensitivity of a synchronized-switching receiver can be calculated using the equations derived in section 4.1.1, except that 1/f noise should be disregarded and 3dB penalty should be added to the resulting sensitivity. For example, if a conventional envelope detection receiver without 1/f noise can achieve a sensitivity of -80dBm, then when the synchronized-switching technique is applied, the receiver can achieve -77dBm sensitivity even when the 1/f noise if present.

4.2 Selectivity of Envelope Detection Receivers

Beside insufficient sensitivity, another critical drawback of the envelope detection receiver is poor interference rejection. In this section, the frequency selectivity of the envelope detection receiver is investigated.

To analyze the frequency selectivity of the envelope detection receiver mathematically, the receiver block diagram in Figure 4-1 can be reused. By following (4.1), (4.2) and (4.3), it can be seen that the frequency and phase information of the carrier, f_C and φ_C, respectively, are lost during envelope detection. If an interferer

$$I = A_I(t)\cdot\cos(2\pi f_I t + \varphi_I) \tag{4.27}$$

is present at the input of the envelope detector together with the desired signal described by

$$S = A_S(t)\cdot\cos(2\pi f_C t + \varphi_C), \tag{4.28}$$

the output becomes:

$$\begin{aligned} A_{OUT} &= k\cdot(S+I)^2 \\ &= k\cdot A_S^2(t)\cdot\frac{1+\cos(2\pi f_C t + 2\varphi_C)}{2} + k\cdot A_I^2(t)\cdot\frac{1+\cos(2\pi f_I t + 2\varphi_I)}{2} \\ &\quad +2k\cdot A_S(t)A_I(t)\cdot\frac{\cos[(2\pi f_C + 2\pi f_I)\cdot t + (\varphi_C+\varphi_I)]}{2} \\ &\quad +2k\cdot A_S(t)A_I(t)\cdot\frac{\cos[(2\pi f_C - 2\pi f_I)\cdot t + (\varphi_C-\varphi_I)]}{2}. \end{aligned} \tag{4.29}$$

The first 2 terms of (4.29) arise from self-mixing of the signals and interference, and the last 2 terms from intermodulation between the signal and interferer. After the LPF, the low-frequency components are

$$A_{OUT,BB} = \frac{k\cdot A_S^2(t)}{2} + \frac{k\cdot A_I^2(t)}{2} + 2k\cdot A_S(t)A_I(t)\cdot\frac{\cos(2\pi\Delta f t + \Delta\varphi)}{2} \tag{4.30}$$

where $\Delta f = f_C - f_I$ and $\Delta\varphi = \varphi_C - \varphi_I$. The first 2 terms in (4.30) both reside around DC, so they cannot be distinguished via frequency filtering. This can also be shown in the frequency domain in Figure 4-7, which illustrates this fundamental limitation of envelope detectors.

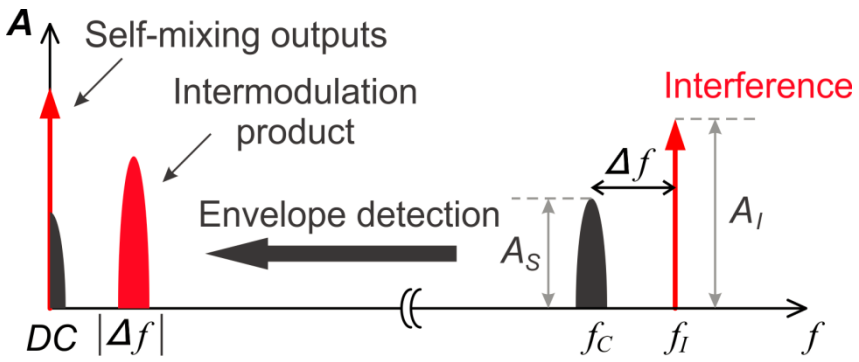


Figure 4-7: Simplified illustration of envelope detector frequency response.

To reject interference, high-Q RF prefiltering is typically adopted in such receivers [39], [43], [44]. However, the passband bandwidth of existing RF front-end filter technologies, e.g., LC, surface acoustic wave (SAW) and bulk acoustic wave (BAW) filters, is still much larger than the bandwidth of the desired signal. As a result, in-band interferers from either the same network or other systems will pass through the filter and corrupt reception of the desired signal. To enhance the resilience of the event-driven radio to in-band interference, a novel scheme is proposed for envelope detection receivers in the next section.

4.3 2-Tone Envelope Detection Scheme

From Figure 4-7 and (4.30) it can be seen that not all frequency and phase information is lost during envelope detection because Δf and $\Delta\varphi$ remain in the detector output. However, at the receiver, it is not possible to make use of Δf and $\Delta\varphi$ because the presence of the interference is uncertain, and also the interference frequency is unknown in general.

On the other hand, it is possible to create an intentional intermodulation component with known frequency and phase at the output of the envelope detector. It is achieved by sending two carrier tones with a predefined frequency offset via the transmitter. As shown in Figure 4-8, the desired signal is split into two parts centered at f_{C1} and f_{C2}. At the receiver, the input RF signal can be written as

$$S = A_S(t)\left[\cos(2\pi f_{C1}t+\varphi_1)+\cos(2\pi f_{C2}t+\varphi_2)\right], \tag{4.31}$$

assuming that the signal power is represented by 2 sinusoid carriers and that it is split equally between the two tones. These two tones will produce an intermodulation component at $f_{C1}-f_{C2}$, which can be taken as the desired output signal

$$A_{OUT,Desired}=k\cdot A_S^2(t)\cdot\cos\left(2\pi f_{IF}t+\varphi_{IF}\right), \tag{4.32}$$

where $f_{IF}=f_{C1}-F_{C2}$ and $\varphi_{IF}=\varphi_{C1}-\varphi_{C2}$, respectively.

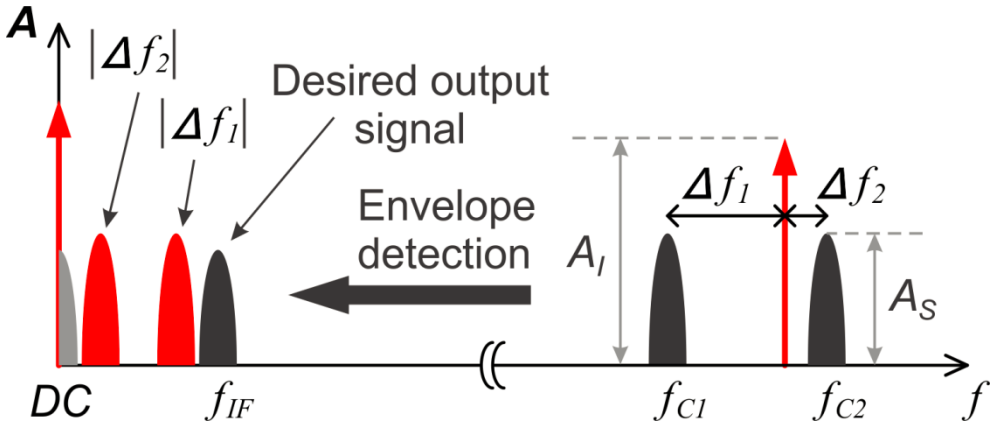


Figure 4-8: Simplified illustration of 2-tone envelope detection with an interferer.

When in-band interference exists together with the desired signal, it introduces unwanted components after envelope detection as shown in Figure 4-8. One of the unwanted components is located at DC, which is generated by the self-mixing of the interference. It is the same component as the second term in (4.30), i.e., $\frac{k\cdot A_I^2(t)}{2}$. As it is near DC instead of f_{IF}, it can be suppressed by filtering.

The other unwanted components originate from intermodulation between the interference and the desired signal. The interference is mixed with both carrier tones and generates multiple intermodulation components, including the most important ones illustrated in Figure 4-8

$$\begin{aligned}A_{OUT,Undesired}=&k\cdot A_S(t)A_I(t)\cdot\cos\left(2\pi\Delta f_1t+\Delta\varphi_1t\right)\\&+k\cdot A_S(t)A_I(t)\cdot\cos\left(2\pi\Delta f_2t+\Delta\varphi_2t\right)\end{aligned}, \tag{4.33}$$

where Δf_1, Δf_2 represent the differences in frequency between the two carrier tones and the interference, respectively, while $\Delta\varphi_1$, $\Delta\varphi_2$ are the corresponding phase differences.

When Δf_1 or Δf_2 is equal to $\pm f_{IF}$, the undesired intermodulation components could mask the

desired signal after envelope detection. By comparing (4.32) and (4.33), several scenarios can be identified as shown in Figure 4-9.

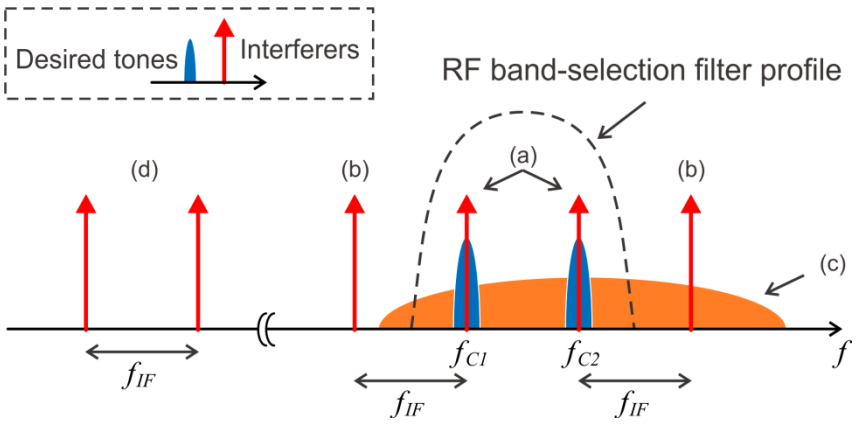


Figure 4-9: Interferers affecting the desired signal in 2-tone envelope detection.

The first scenario is illustrated in Figure 4-9(a), where the interferer is at the same frequency as one of the 2 desired carrier tones. Mathematically, $f_I = f_{C1}$ or $f_I = f_{C2}$, so that $\Delta f_2 = f_{IF}$ or $\Delta f_1 = -f_{IF}$.

The second scenario is illustrated in Figure 4-9(b), where the interferer is not overlapping with either desired carrier tone, but it is f_{IF} away from one or the other tone. In other words, $f_I = 2f_{C1} - f_{C2}$ or $f_I = 2f_{C2} - f_{C1}$, so that $\Delta f_1 = f_{IF}$ or $\Delta f_2 = -f_{IF}$.

The third scenario is shown in Figure 4-9(c), where the interferer has a bandwidth wider than $f_{IF}/2$. After squaring, its self-mixed component $\frac{k \cdot A_I^2(t)}{2}$ will span from DC to beyond f_{IF}. Consequently, the desired intermodulation signal is corrupted.

The last scenario is shown in Figure 4-9(d), where two or more narrowband interferers exist, and they are f_{IF} away from one another. After squaring, one of their intermodulation components is also located at f_{IF}, overlapping with the desired intermodulation signal.

If RF front-end prefiltering is present in the receiver, out-of-band interference can be suppressed. As shown in Figure 4-9, when a proper combination of RF front-end filter and 2-tone frequency plan is adopted, the interferers in the second and the last scenario lie outside of the RF bandwidth and thus are suppressed prior to envelope detection. The larger the frequency separation between the 2 carrier tones, the larger the RF filter bandwidth can be. If

the 2 carrier tones are sufficiently far apart, a low-Q RF filter can be used to reject the out-of-band interference. Such a filter may even be integrated on-chip with inductors and capacitors. However, a large 2-tone frequency separation leads to a higher intermodulation frequency f_{IF} after envelope detection, and thus increases the power consumption of the receiver. In addition, as both frequency tones need to be within the same band, there is an upper limit in the 2-tone separation imposed by regulations of wireless frequency spectrum. Therefore, the frequency plan of the 2-tone envelope detection scheme should be made based on a trade-off between interference rejection, system cost and power consumption.

In addition to improved interference rejection, the 2-tone envelope detection scheme features another advantage, sensitivity. Since the desired output signal of the envelope detector resides at f_{IF} instead of DC, the signal is not corrupted by 1/f or DC offset as long as f_{IF} is chosen above the 1/f noise corner frequency. As a result, the sensitivity of the receiver is also improved, as is the case of the synchronized-switching receiver.

4.4 Summary

The analysis of the envelope detection radio in this chapter identifies the sensitivity and selectivity limitation in event-driven radios. A novel envelope detection scheme (i.e., 2-tone envelope detection) is proposed to enhance the selectivity as well as the sensitivity of such receivers. In the following chapters, an ultra-low-power 2-tone transceiver is designed to benefit from the proposed scheme and fulfill the requirements of generic event-driven radio applications.

Chapter 5

2-Tone Direct-Modulation Transmitter

In order to benchmark the performance of the proposed 2-tone envelope detection scheme, an ultra-low-power transmitter front-end is designed in this chapter to deliver modulated 2-tone signals while fulfilling the requirements of generic event-driven radio applications. The measured data of the transmitter implementation is also presented.

5.1 Architecture

As is proposed in Chapter 2 and verified by the proof-of-concept transmitter, direct-modulation is the architecture of choice for event-driven radio transmitters. However, conventional transmitters are used for single-carrier modulation. In this section, an enhanced direct-modulation transmitter architecture is introduced, and a novel modulation scheme is proposed.

5.1.1 2-Tone Carrier Generation

Several approaches exist to generate two carrier tones. Two single-tone signals can be combined, as is illustrated in Figure 5-1. In such an implementation, two RF oscillators are required to generate two local oscillator (LO) signals. As the frequency separation between the two tones is used to distinguish the desired signal from interference, it needs to be precisely defined. As a result, two phase-locked loops (PLLs) sharing a common reference clock (CLK_{REF}) are required to regulate the operation of the two LOs. The second PLL in this architecture (compared to a conventional single-tone Tx) could double the power drawn by pre-PA stages. Fur-

thermore, since the frequencies of the two oscillators are closed to each other, they are subject to injection locking and pulling [105], [106] which will disrupt their frequency separation.

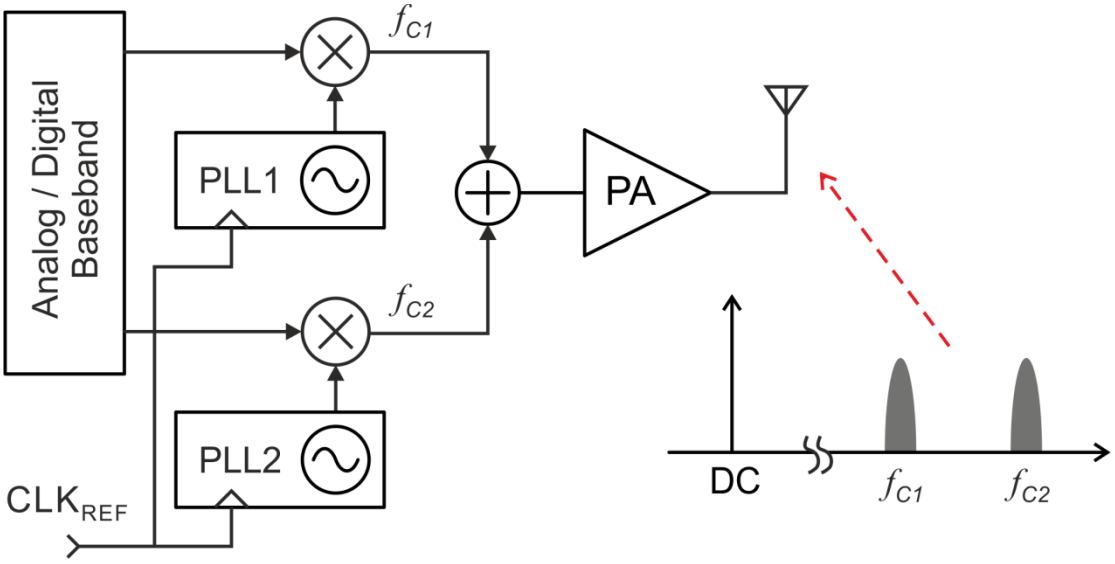


Figure 5-1: Generating a 2-tone signal by adding 2 single-tone carriers.

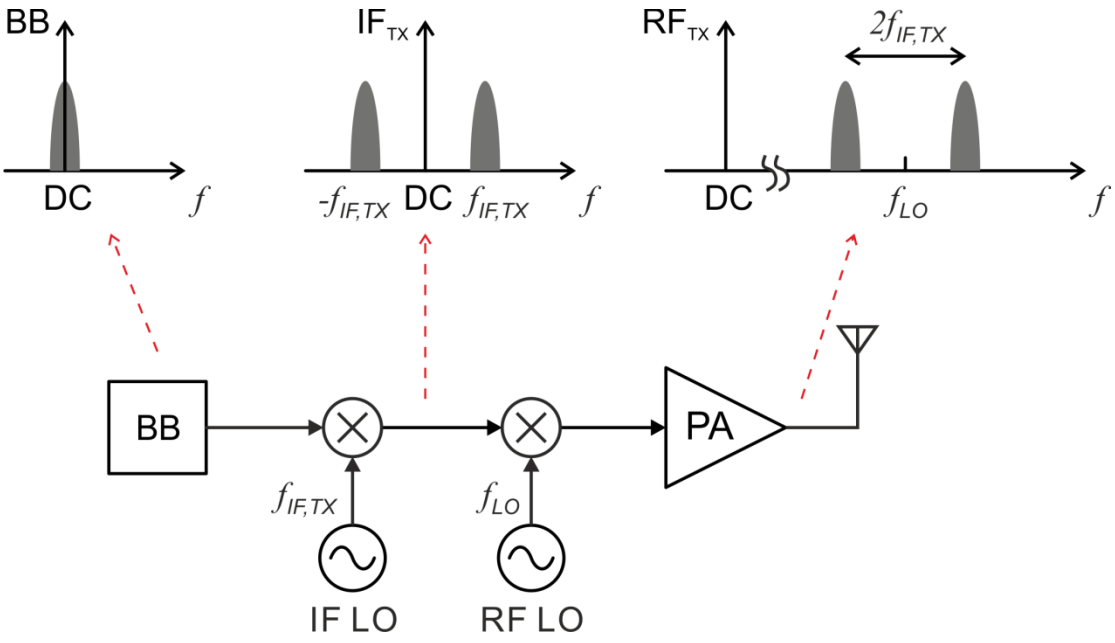


Figure 5-2: Generating 2-tone signals by 2-step upconversion.

To avoid LO pulling and reduce power consumption, it is desired to generate the 2-tone carrier from a single RF oscillator. A 2-step upconversion approach is proposed as shown in

Figure 5-2. The baseband (BB) information is firstly upconverted to an intermediate frequency (IF) using the IF oscillator at $f_{IF,TX}$. The resulting IF signal, IF_{TX}, can be described by

$$IF_{TX} = A_{IF,TX}(t)\cdot\cos\left(2\pi f_{IF,TX}(t)\cdot t+\varphi_{IF,TX}(t)\right), \tag{5.1}$$

where $A_{IF,TX}$ is the amplitude and $\varphi_{IF,TX}$ is the phase of the IF signal. Baseband information can be used to modulate the amplitude ($A_{IF,TX}$), frequency ($f_{IF,TX}$) or phase ($\varphi_{IF,TX}$) of the IF signal. The IF signal is then mixed with an RF oscillator at f_{LO} in the second stage. The IF signal is upconverted to both the upper- and lower-sideband of the LO frequency, and the output signal can be written as

$$\begin{aligned} RF_{TX} &= A_{IF,TX}(t)\times \\ &\{\cos[(2\pi f_{LO}+2\pi f_{IF,TX}(t))\cdot t+\varphi_{LO}+\varphi_{IF,TX}(t)] \\ &+\cos[(2\pi f_{LO}-2\pi f_{IF,TX}(t))\cdot t+\varphi_{LO}-\varphi_{IF,TX}(t)]\}, \end{aligned} \tag{5.2}$$

where φ_{LO} is the phase of the RF LO signal. The amplitude of the RF LO signal is assumed constant and is normalized for simplicity. The Tx output signal contains two modulated tones, one at

$$f_{C1} = f_{LO} - f_{IF,TX}, \tag{5.3}$$

and the other at

$$f_{C2} = f_{LO} + f_{IF,TX}. \tag{5.4}$$

The two carrier tones are separated by $2f_{IF,TX}$.

Typically, the frequency of the IF oscillator is below 50MHz to support 2-tone separation below 100MHz, while the RF oscillator is operating in the gigahertz range. As the frequencies of the two oscillators can be chosen far away from each other, injection locking or pulling is avoided [105], [106].

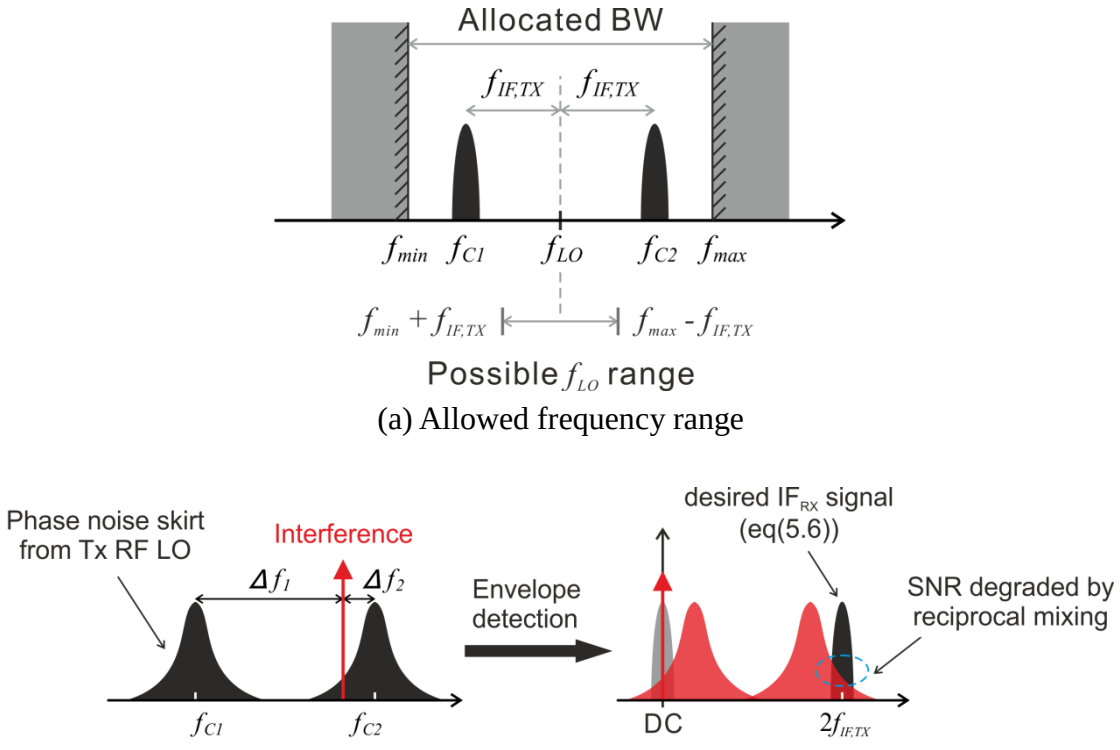
When the Tx output signal is squared by an envelope detector at the receiver, the detector output is (path loss and Rx gain ignored for simplicity)

$$\begin{aligned} ED_{RX} = RF_{TX}^2 = A_{IF,TX}^2(t)\times\Big\{1&+\frac{\cos\left[2\pi(2f_{LO}+2f_{IF,TX}(t))\cdot t+2\varphi_{LO}+2\varphi_{IF,TX}(t)\right]}{2} \\ &+\frac{\cos\left[2\pi(2f_{LO}-2f_{IF,TX}(t))\cdot t+2\varphi_{LO}-2\varphi_{IF,TX}(t)\right]}{2} \\ &+\cos\left[2\pi(2f_{LO})\cdot t+2\varphi_{LO}\right]+\cos\left[2\pi(2f_{IF,TX}(t))\cdot t+2\varphi_{IF,TX}(t)\right]\Big\}, \end{aligned} \tag{5.5}$$

which contains a baseband component, double-frequency components at $2f_{LO}+2f_{IF,TX}(t)$ and $2f_{LO}-2f_{IF,TX}(t)$, and intermodulation components at $2f_{LO}$ and $2f_{IF,TX}$. The last component at $2f_{IF,TX}$ is the desired signal

$$IF_{RX} = A^2_{IF,TX}(t)\cos\left[2\pi(2f_{IF,TX}(t))\cdot t + 2\varphi_{IF,TX}(t)\right], \tag{5.6}$$

while the other components are discarded by filtering. It can be seen that the frequency and phase of the Tx IF oscillator, i.e., $f_{IF,TX}$ and $\varphi_{IF,TX}$ are preserved in IF_{RX}, similar to the IF stage in a super-heterodyne transceiver. Therefore, similar requirements (i.e., low phase noise and high frequency accuracy) apply to the IF oscillator in the 2-tone transmitter as in a super-heterodyne transceiver. Crystal oscillators (XO) can be used to generate the IF oscillation signal directly for both the 2-tone transmitter and the 2-tone receiver (in the next chapter) with low power consumption [107].



(a) Allowed frequency range

(b) Impact of RF LO phase noise

Figure 5-3: Constraints of Tx RF local oscillator performance.

Although the frequency and phase of the RF oscillator in the transmitter, i.e., f_{LO} and φ_{LO}, are not present in (5.6), they are still subject to two constraints. Firstly, the 2 output tones

must stay within the allocated frequency range dictated by either regulations or the receiver front-end bandwidth. As illustrated in Figure 5-3(a), f_{LO} should stay between $f_{min} + f_{IF,TX}$ and $f_{max} - f_{IF,TX}$. The other constraint applies to the phase noise of the RF LO, as explained in Figure 5-3(b). The intermodulation between a potential interferer and the noisy sidebands of the 2-tone signal produces noise at the desired intermodulation frequency (i.e., $2f_{IF,TX}$) similar to the reciprocal mixing observed in a conventional receiver [108]. The signal-to-noise ratio (SNR) is therefore degraded after envelope detection. As a trade-off between performance and power consumption, the RF oscillator can be implemented as a voltage or digitally controlled oscillator periodically calibrated to ensure its frequency accuracy.

5.1.2 Digital-IF Transmitter

To reduce complexity in the pre-PA stage and benefit from the efficiency of the direct-modulation transmitter architecture in terms of power consumption, the first upconversion step of the proposed transmitter is moved to the digital domain (Digital IF), while the second upconversion step is carried out by a direct-modulation PA.

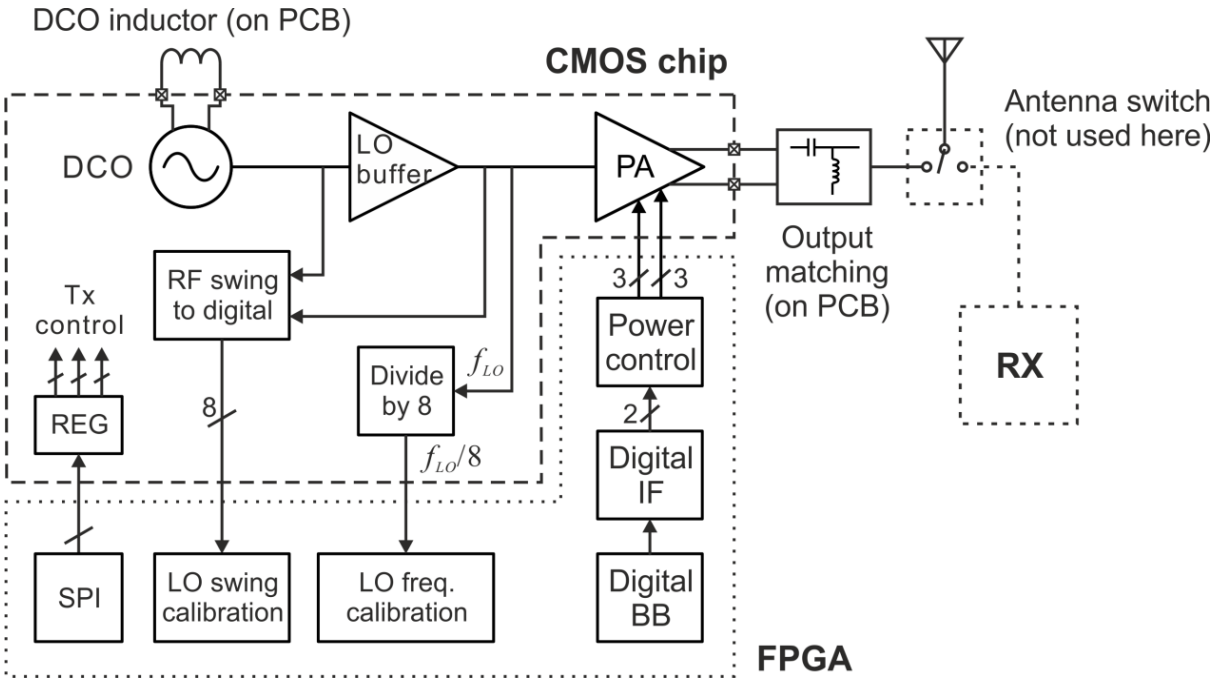


Figure 5-4: Block diagram of the digital-IF transmitter for 2-tone modulation.

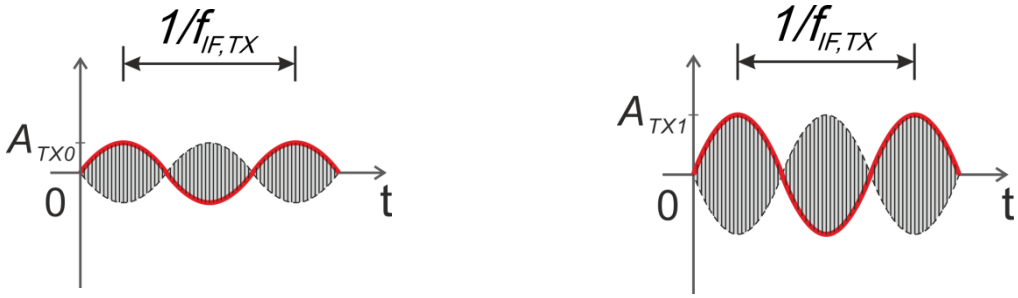
The block diagram of the digital-IF transmitter is shown in Figure 5-4. The digital baseband (BB) signal is upconverted to the intermediate frequency in the digital IF module, while a single-tone RF LO signal is generated by a digitally-controlled oscillator (DCO). The LO signal is amplitude and phase modulated by the digital IF signal in the PA, which is described in the next subsection. To reduce the dynamic loading effect of the PA on the LO, a buffer is inserted between the DCO and PA for isolation. In this work, the transmitter and the receiver are separated, and therefore an antenna switch is not necessary. When the receiver and transmitter are combined on one chip, an antenna switch or a shared input / output matching network is required to share one antenna between the transmitter and the receiver.

Two mixed-signal calibration loops, an LO frequency calibration loop and an LO swing calibration loop, monitor and correct the amplitude and frequency of the LO output on-chip. As discussed in Chapter 2, this contributes to further power reduction since the required performance of the analog circuits can be ensured without consuming unnecessary power.

5.1.3 2-Tone IF-PSK Modulation

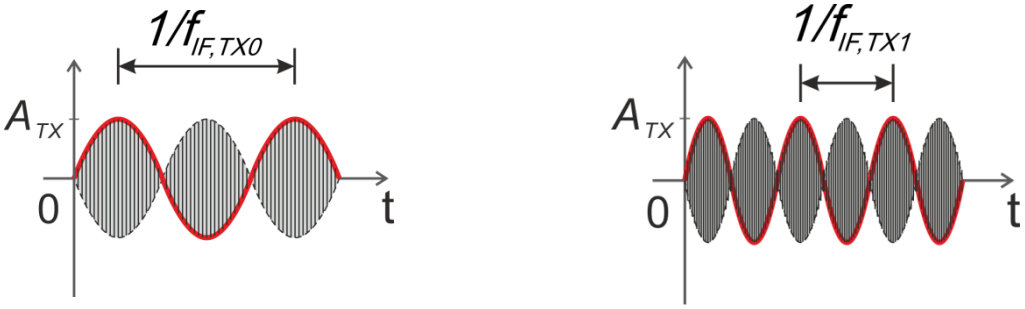
The baseband signal can modulate the amplitude, phase or frequency of the IF signal in the transmitter, which will be preserved after envelope detection according to (5.6). Figure 5-5 shows the Tx output waveform when the IF amplitude is modulated, with the IF signal overlaid (in red). The amplitude of the RF pulses represents either ‘0’ or ‘1’. Figure 5-6 shows the Tx output waveform and the IF signal when the IF frequency is modulated. The repetition rate of the RF pulses changes according to the baseband signal. In the case where the IF phase is modulated, as shown in Figure 5-7, the time delay of the RF pulses is controlled by the baseband signal.

The digital-IF transmitter proposed in section 5.1.2 is most suitable for the amplitude- and phase-shift-keying of the IF signal (i.e., IF-ASK and IF-PSK), as well as conventional OOK and ASK modulation. In this work, the use of IF-PSK is preferred over IF-ASK due to its better resilience to noise and immunity to threshold variation during demodulation [109].



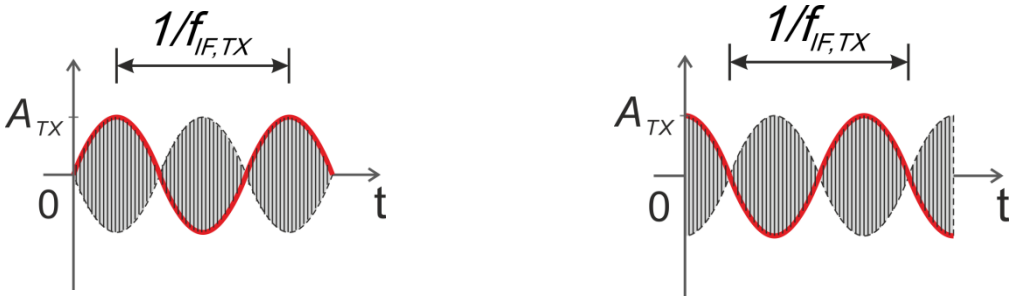
(a) transmitting '0' (b) transmitting '1'

Figure 5-5: Modulating IF amplitude in the transmitter.



(a) transmitting '0' (b) transmitting '1'

Figure 5-6: Modulating IF frequency in the transmitter.



(a) transmitting '0' (b) transmitting '1'

Figure 5-7: Modulating IF phase in the transmitter.

The IF-PSK modulation steps in the proposed transmitter are shown in Figure 5-8. In the digital IF module, a 3-level (-1, 0, 1) digital approximation is generated at $f_{IF,TX}$ with reference to an accurate input clock, which can be derived from a low-power crystal oscillator. Due to the nature of the digital signal, the spectra of the IF signal contain not only the fundamental

tone at $f_{IF,TX}$, but also odd-order harmonics at $3f_{IF,TX}$, $5f_{IF,TX}$, etc. The phase of the IF sine wave is determined by the baseband signal. When transmitting a '0', it has 0 °phase shift, and when transmitting a '1' it is phase shifted by 90 °. The digital IF signal is then multiplied by the single-tone LO signal in the PA. When the IF signal is '-1' the RF output has 180° carrier phase, and when the IF signal is '1' the RF output has 0° carrier phase. The output is switched off when the IF is '0'. The RF output of the transmitter contains frequency components at f_{LO} + $f_{IF,TX}$ and $f_{LO} - f_{IF,TX}$, so the frequency separation between the two tones is $2f_{IF,TX}$. The original carrier tone at f_{LO} diminishes due to frequency conversion, whereas higher-order harmonics from the digital IF signal are upconverted to $f_{LO} \pm 3f_{IF,TX}$, $f_{LO} \pm 5f_{IF,TX}$, and so on. However, these higher-order IF harmonics are pushed out of the RF Tx band by increasing the IF, and rejected by the bandpass response of the transmitter and/or the receiver.

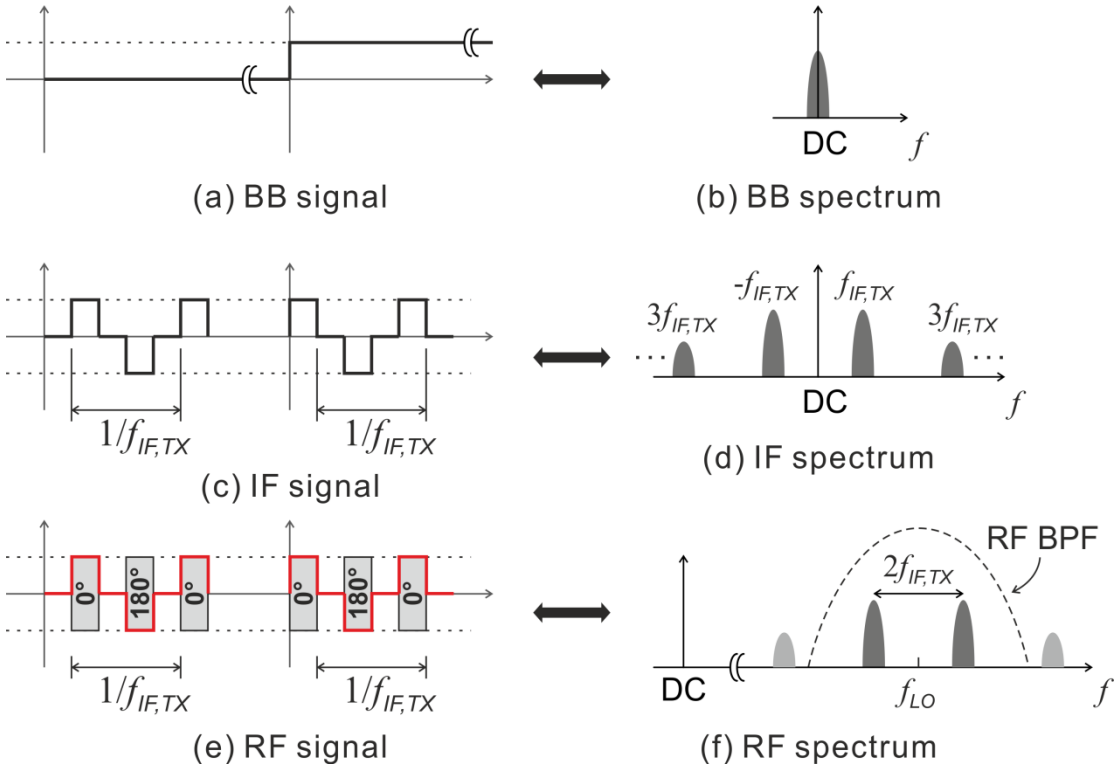


Figure 5-8: Illustration of the IF-PSK 2-tone modulation in the digital-IF transmitter.

Note that due to the squaring operation of the envelope detector in the receiver, the IF frequency and phase are doubled as shown in (5.6). For this reason, 90 °phase shift is used in the IF-PSK modulation, which after squaring results in 180 °phase shift in the receiver IF that

can be detected as conventional binary phase-shift keying (BPSK). If 180 ºphase-shift is used in the IF-PSK modulation, the receiver IF signal will have 360º phase shift between '0' and '1', which cannot be detected.

5.2 Front-End Circuit Design

The transmitter front-end is designed to fulfill the requirements of generic event-driven radio applications. It is intended to operate in the 915MHz ISM band as well as other sub-GHz license-free bands from 780MHz to 1GHz. All the circuit blocks are designed for 1V supply voltage.

5.2.1 Digitally-Controlled Oscillator

The design of the oscillator is carried out by Mr. Ao Ba from Delft University of Technology [110] under the supervision of the author of this work. As the frequency of this oscillator is calibrated periodically, the oscillator must maintain its frequency when the calibration circuits are switched off to ensure that the two RF tones stay within the target frequency range. A DCO is well-suited to this purpose; once calibrated, the digital frequency tuning signal can be stored in a digital register with negligible power consumption. By contrast, if a voltage controlled oscillator is used, the analog tuning voltage has to be maintained either by a digital-to-analog converter (DAC), or held on a large capacitor [87]. A DAC consumes extra power and introduces phase noise to the carrier signal, while the tuning voltage held on a large capacitor suffers from charge leakage of the capacitor as well as charge injection from duty-cycling switches.

Both ring and LC oscillators are considered for the RF oscillator block. Typically, LC oscillators achieve a better figure-of-merit (FoM) than ring oscillators at the cost of larger chip area or more external components [111], [112]. This work implements an LC oscillator with an off-chip inductor to lower power consumption, and achieve low phase noise and high frequency stability against supply and temperature variations.

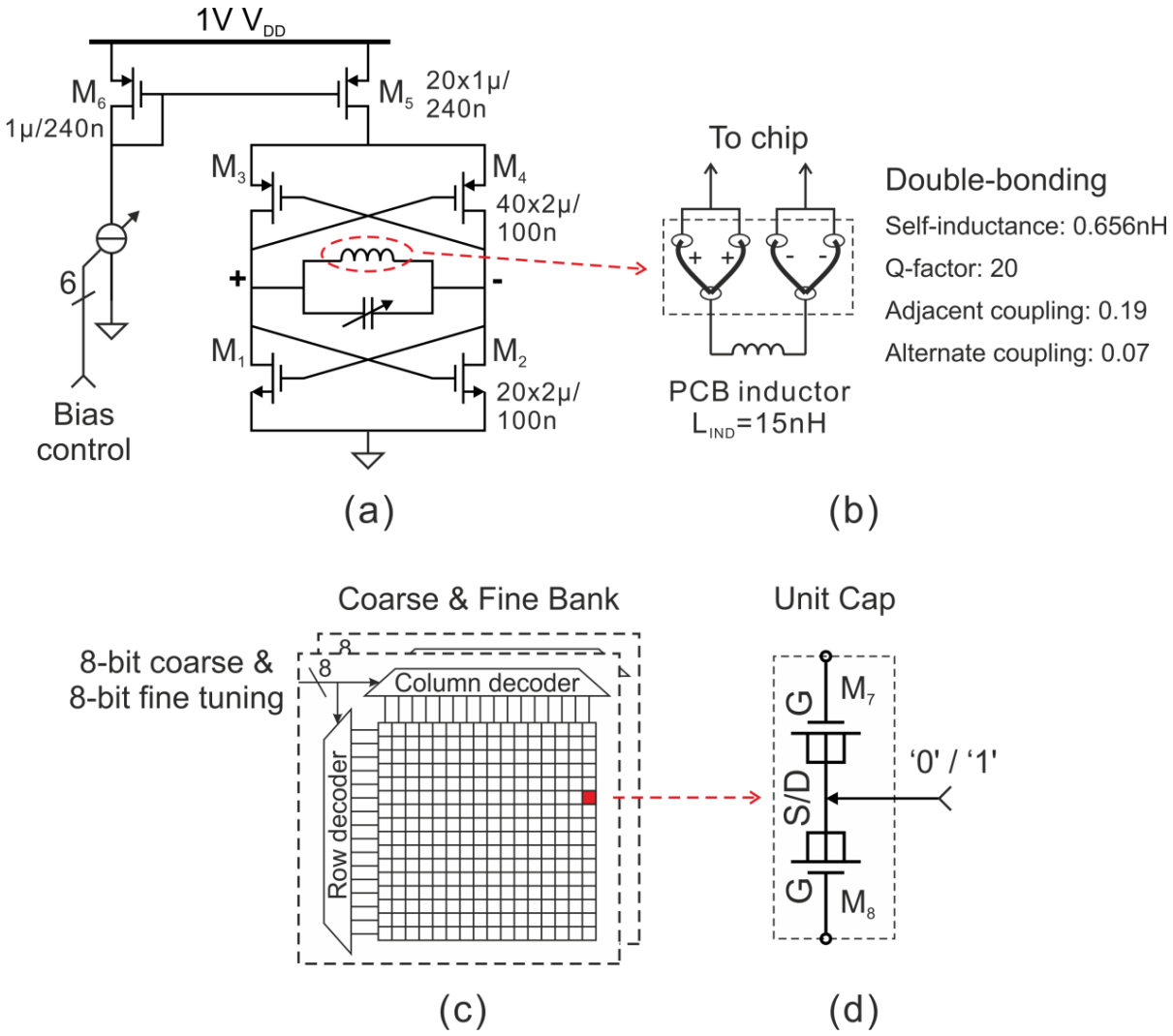


Figure 5-9: Schematic of the RF DCO and its tuning capacitors.

The topology and schematic of the DCO are shown in Figure 5-9. It adopts the complementary cross-coupled pair to achieve approximately 50% current reduction as compared to a single N- or PMOS cross-coupled pair. The cross-coupled transistors are biased in weak-inversion to maximize the transconductance efficiency G_M/I_D [55]. The increase in transistor size due to weak-inversion operation adds parasitic capacitance to the LC tank, and reduces frequency tuning range of the DCO. The optimal size of the cross-coupled transistors is chosen via circuit simulation as a trade-off between power consumption, frequency running range and phase noise. A PMOS tail current source is used to lower 1/f noise in the bias current and realize better phase noise performance [113]. The bias current is controlled by a 6-bit programmable current mirror so that the oscillation signal swing can be adjusted digitally.

The frequency tuning of the DCO is implemented using two digitally-controlled capacitor banks. One capacitor bank is for coarse tuning and the other is for fine tuning. Each of the capacitor banks is controlled by an 8-bit digital oscillator tuning word (OTW). The capacitors in both banks are unity-weighted, and the binary OTWs are thermometer-encoded to switch on and off the unit capacitors progressively. By doing so, frequency monotonicity is guaranteed within each tuning bank.

The coarse bank needs to provide a tuning range between 780MHz and 1GHz. Differential varactor pairs shown in Figure 5-9(d) are used as the unit capacitors. By switching their tuning voltage to ground or V_{DD}, the capacitance will vary between high and low states. On the other hand, the fine tuning bank should realize fine resolution. Small unit capacitances are required for fine frequency steps, which are implemented using small-sized (200nm by 200nm) NMOS transistors switched between depletion and inversion modes with capacitance steps on the order of 100aF.

A 15nH off-chip inductor with Q-factor of 65 is used in the tank. Double-bonding is used to reduce the bondwire inductance so that the LC tank inductance is dominated by the off-chip inductor. The package parasitic effects are modeled as shown in Figure 5-9(b) to ensure the frequency coverage. The tank impedance at resonance is around 5.6kΩ. If an on-chip inductor with a (typical) Q-factor around 13 at 1GHz were used instead, the tank impedance would be reduced to 1.1kΩ, and more power (approximately 5 times) would be required to start oscillation. Thanks to the high-Q off-chip inductor, the DCO is able to oscillate at just 55μW power consumption in simulation. The penalty of using an off-chip inductor is that both the form-factor and bill-of-materials of the radio will increase, as a trade-off for power efficiency.

5.2.2 Digitally-Controlled Power Amplifier

The block diagram and schematic of the PA are shown in Figure 5-10. It consists of an RF front-end, a binary-to-thermometer encoder, and a power control module. The 2-bit IF_B which represents '-1', '0' and '1' is converted to two 7-bit thermometer-coded signals (IF_T+ and IF_T-)

based on 8 power levels (3-bit) as shown in Table 5-1. To ensure equal delay and proper timing of IF_T+ and IF_T-, the encoder is integrated on-chip with the RF front-end, while the power control logic is implemented externally in a commercial FPGA platform.

Table 5-1: Generation of two 7-bit thermometer-coded IF_T+/-.

2-bit IF_B (-1, 0 and 1)	3-bit Power (0 to 7)	7-bit IF_T+	7-bit IF_T-
"10" (-1)	"000" (0)	"0000000"	"0000000"
	"001" (1)	"0000000"	"0000001"
	"010" (2)	"0000000"	"0000011"
	"011" (3)	"0000000"	"0000111"
	"100" (4)	"0000000"	"0001111"
	"101" (5)	"0000000"	"0011111"
	"110" (6)	"0000000"	"0111111"
	"111" (7)	"0000000"	"1111111"
"00" (0)	X	"0000000"	"0000000"
"01" (1)	"000" (0)	"0000000"	"0000000"
	"001" (1)	"0000001"	"0000000"
	"010" (2)	"0000011"	"0000000"
	"011" (3)	"0000111"	"0000000"
	"100" (4)	"0001111"	"0000000"
	"101" (5)	"0011111"	"0000000"
	"110" (6)	"0111111"	"0000000"
	"111" (7)	"1111111"	"0000000"

The RF front-end of the PA is composed of 7 identical units containing a pseudo-differential transconductor and a double-balanced Gilbert cell. The transconductor at the bottom of the PA unit converts the input LO voltage to current signals, and is biased in class-AB as a trade-off between the required input swing and power efficiency. The Gilbert cell mixes the LO current with the IF_T signals. When IF is '1' (i.e., IF_T+ = '1' and IF_T- = '0'), the positive and negative LO currents are switched to the positive and negative PA outputs, respectively. When IF is '-1' (i.e., IF_T+ = '0' and IF_T- = '1'), the LO currents are inverted, and when IF is '0' (i.e., both IF_T+ and IF_T- = '0'), the LO currents are switched off. To carry out IF-PSK modulation, the IF signal iterates through '0', '1', '0' and '-1' with its phase modu-

lated by the baseband data. For OOK modulation, the IF signal is either '0' or '1', while for BPSK modulation, the IF signal is given as '-1' or '1', corresponding to '0' or '1', respectively, in the baseband.

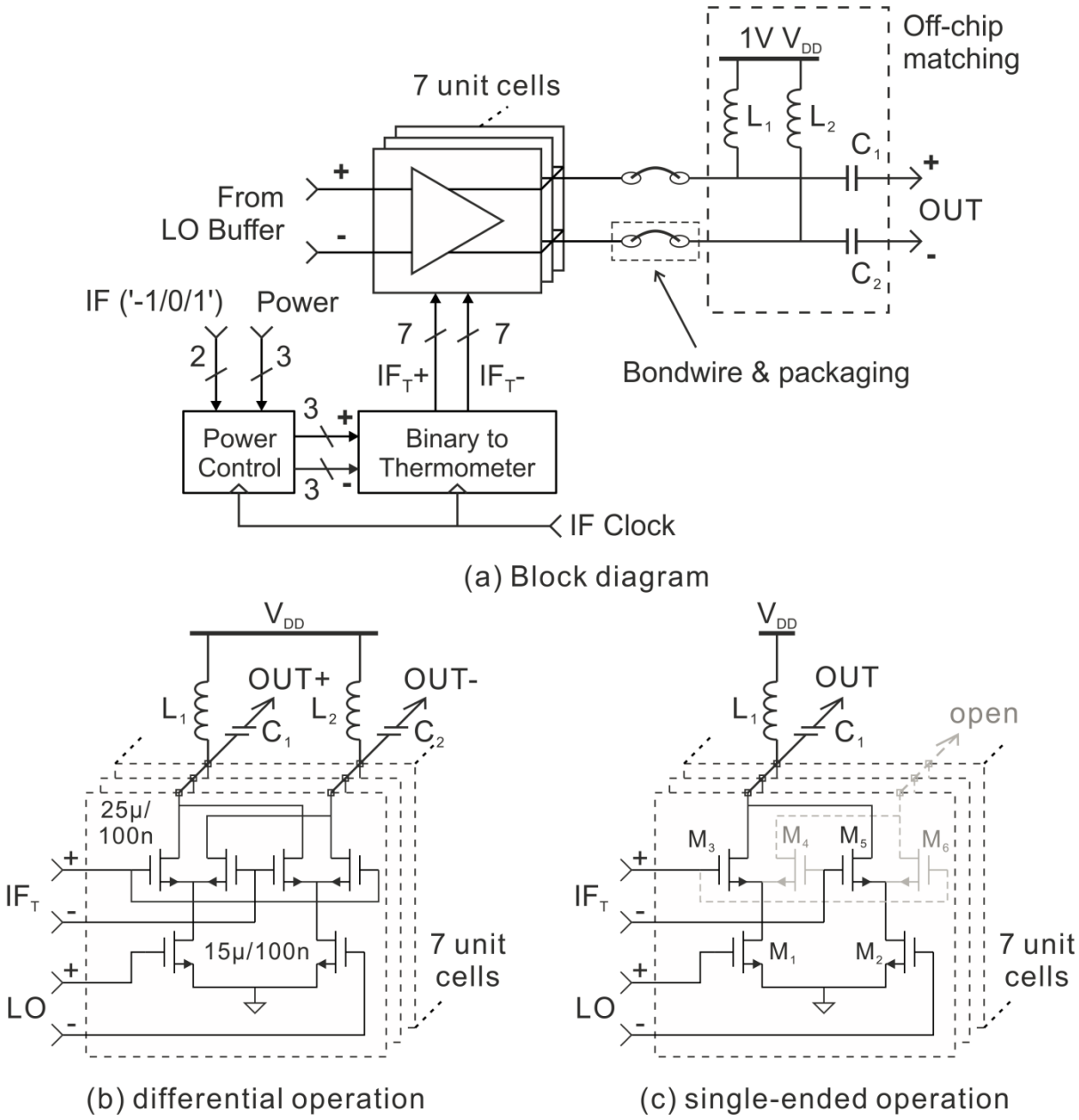


Figure 5-10: Block diagram and schematic of the PA.

The power control logic determines how many PA units are switched on, so that the amount of current reaching the PA outputs is adjusted in 8 discrete steps. The discrete output

levels can be also used for pulse-shaping, as described for the proof-of-concept transmitter in Chapter 3.

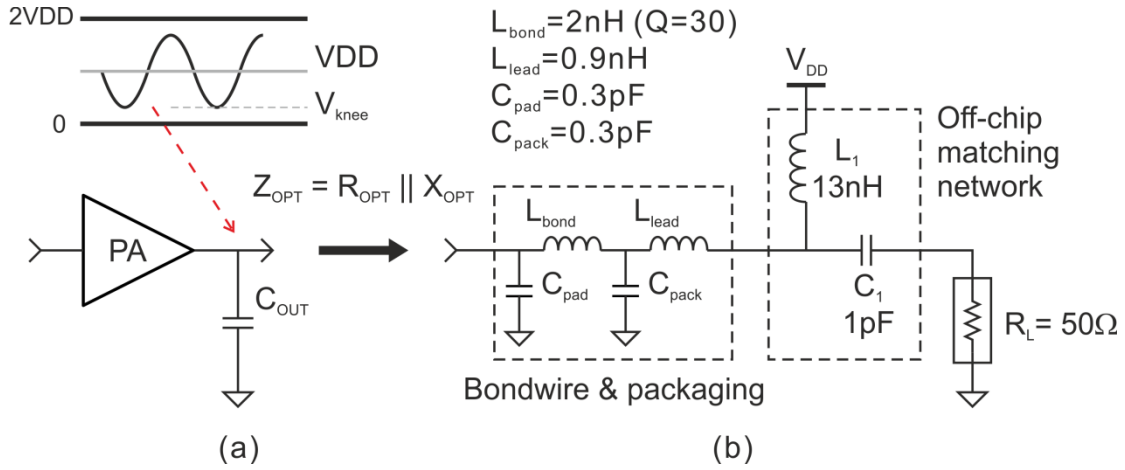


Figure 5-11: Output matching network of the PA (single-ended equivalent).

The output currents from the 7 PA units are summed at the matching network input. The matching network needs to be optimized so that the total capacitance at the outputs of the Gilbert cells (C_{OUT} in Figure 5-11) is tuned out to maximize the output voltage swing [114]. The optimal load impedance is the parallel combination of the optimal resistance ($R_{OPT,SE}$) and reactance ($X_{OPT,SE}$), which are given by

$$R_{OPT,SE} = \frac{(V_{DD} - V_{knee})^2}{2 \cdot P_{OUT,SE}} \tag{5.7}$$

and

$$X_{OPT,SE} = -\frac{1}{j\omega \cdot C_{OUT}}, \tag{5.8}$$

where ω is the radius carrier frequency, and V_{knee} is the minimal output voltage at the PA output when the transistors stay in saturation region. $P_{OUT,SE}$ is the peak output power for a single branch of the differential PA. If the target differential output level is 1mW, then $P_{OUT,SE}$ should be 0.5mW. For 1V V_{DD} and 0.29V knee voltage, the single-ended optimal load resistance is around 500Ω. An off-chip LC matching network together with the package parasitics shown in Figure 5-11 transforms the 50Ω termination into the desired load impedance for the PA at 915MHz.

One branch of the differential matching network can be disabled to allow a single-ended output. In that case, the PA delivers half of the maximum output power at the same power efficiency. This mode is illustrated in Figure 5-10(c) and it is used to expand the output power range of the transmitter to fulfill the event-driven radio requirements, while maintaining the PA drain efficiency. Since the peak-to-average power ratio (PAPR) of both OOK and IF-PSK is 3dB, the average output level of the transmitter is -3dBm and -6dBm in differential and single-end modes, respectively.

5.2.3 LO Buffer

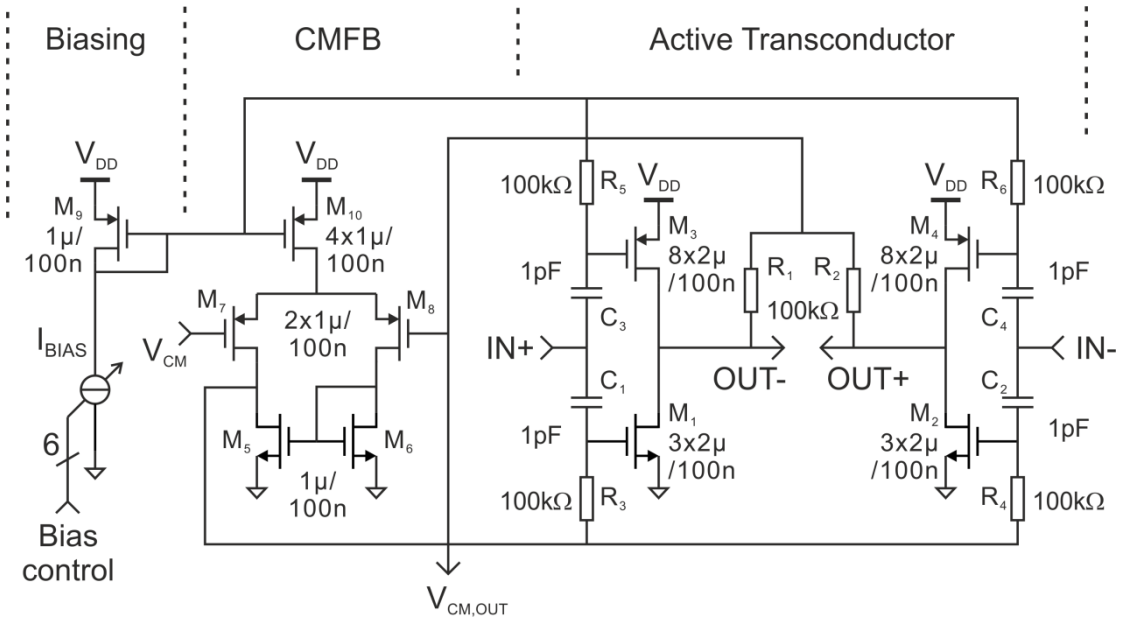


Figure 5-12: Schematic of the LO buffer.

The schematic of the LO buffer is shown in Figure 5-12. It consists of three parts: a programmable current mirror, a common-mode feedback (CMFB) circuit, and an active transconductor. The transconductor consists of a pair of complementary common-source P- and NMOS transistors, with gates AC-coupled to the DCO output. The output common-mode voltage ($V_{CM,OUT}$) is obtained via two 100kΩ resistors, and compared to the desired level (V_{CM}) in the CMFB circuitry. The CMFB loop gain ensures that the common-mode level at

the buffer output equals V_{CM} so that the PA can be DC-coupled to the buffer. This not only makes the layout more compact, but also reduces signal loss in AC coupling networks.

By increasing or decreasing reference current (I_{BIAS}) to the PMOS current mirror, the biasing point of the transconductor is moved toward either class-A or class-C, respectively. For a given input LO swing, the output LO amplitude increases or decreases accordingly. The reference current can be set via a 6-bit digital signal, which can either be programmed manually, or adjusted automatically via the LO swing calibration loop introduced in section 5.3.1.

5.2.4 RF Swing to Digital Converter

An RF swing to digital converter is designed to detect variations of the LO signal levels at the output of the DCO and at the input of the PA. A block diagram of the converter is shown in Figure 5-13. Firstly, two envelope detectors acquire the amplitude of the LO signals at the DCO output and PA input, respectively. Then, one of the amplitude signals is selected by an analog switch and converted into an 8-bit digital signal via a successive approximation register (SAR) ADC described in [115].

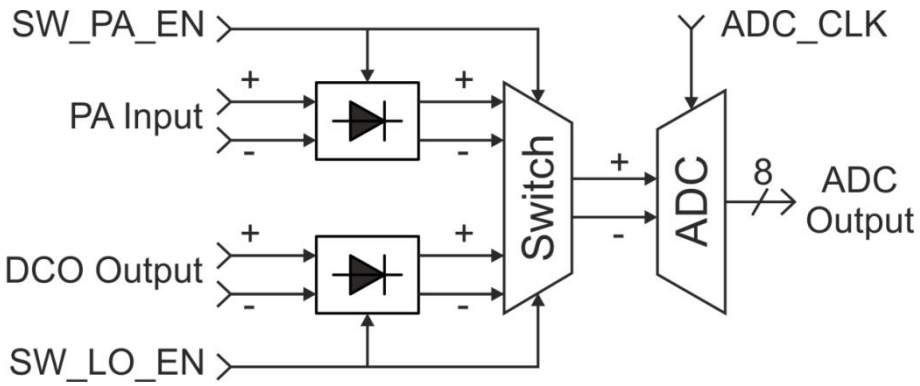


Figure 5-13: Block diagram of the RF swing to digital converter.

The schematic of the swing detector at the PA input is shown in Figure 5-14. The differential LO signal at the PA input is rectified by the NMOS pair M_1 and M_2 to the output node PA_SW+. A replica branch is added to generate a DC reference level at PA_SW- from the common-mode voltage of the LO buffer output ($V_{CM,OUT}$ in Figure 5-12). A similar block is used to detect the swing level at the DCO output.

The output of this converter is used to track variations of the LO swing at different stages of the transmitter. Although the process, voltage and temperature (PVT) variations in the converter itself may also affect the conversion output, its impact is smaller and also easier to predict than variations in the off-chip inductors and packaging parasitics. Therefore, the bias level of the DCO and the LO buffer should be calibrated based on the converter output so that the variation in LO swing is minimized, and the desired input swing is provided to the PA.

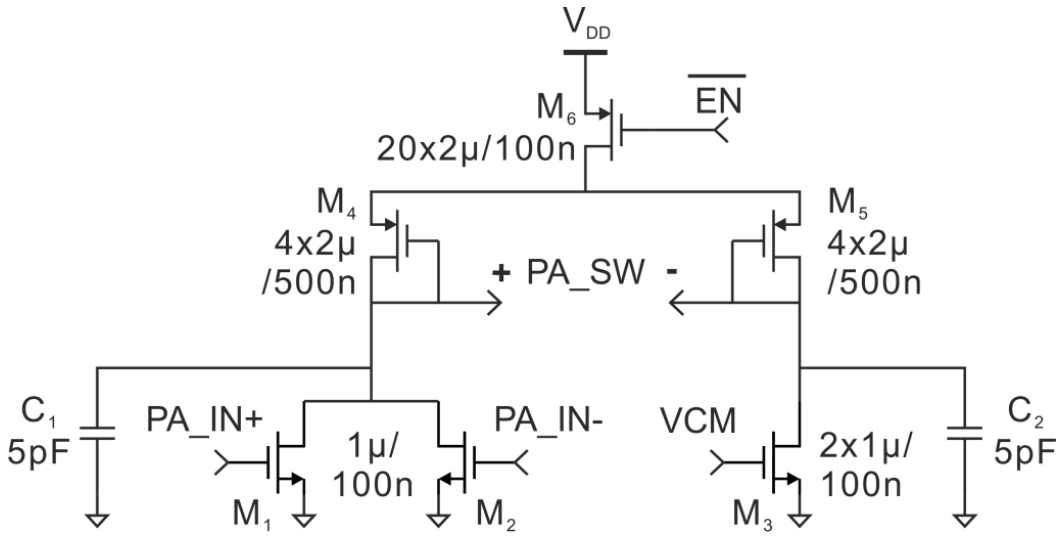


Figure 5-14: Swing detector at PA input.

The RF swing to digital converter consumes less than 30 µA during the calibration phase of the transmitter. The swing calibration algorithm implemented on the FPGA platform is described in section 5.3.1.

5.2.5 LO Frequency Divider

A divider scales the LO frequency by 1/8 for calibration. The block diagram and schematic of the divider is shown in Figure 5-15. It employs a 4-stage ring [116] to scale the LO frequency down to around 100MHz. The D flip-flop in the ring divider is realized with two inverters (INV_1 and INV_2) and two transmission gates (TG_1 and TG_2) driven by opposite clock phases [116]. The states of the flip-flop are stored in the device and parasitic capacitance (C_{par1} and

C_{par2}), and thus needs to be refreshed every RF clock cycle to counteract leakage. Due to the simple structure and low transistor count, this flip-flop reduces power consumption drastically.

Prior to the divider, the input signal from the LO buffer is amplified to full-swing by a rail-to-rail driver. Both the driver and the D flip-flops are designed with minimal gate length, which ensures low power consumption and a compact layout. For 915MHz input frequency, the power consumption of the complete divider is around 30μW in operation.

For an input LO frequency between 780MHz and 1GHz, the divider output clock is between 97.5MHz and 125MHz, which can be processed further by the LO frequency calibration loop implemented on the FPGA platform. The calibration algorithm is described in section 5.3.2.

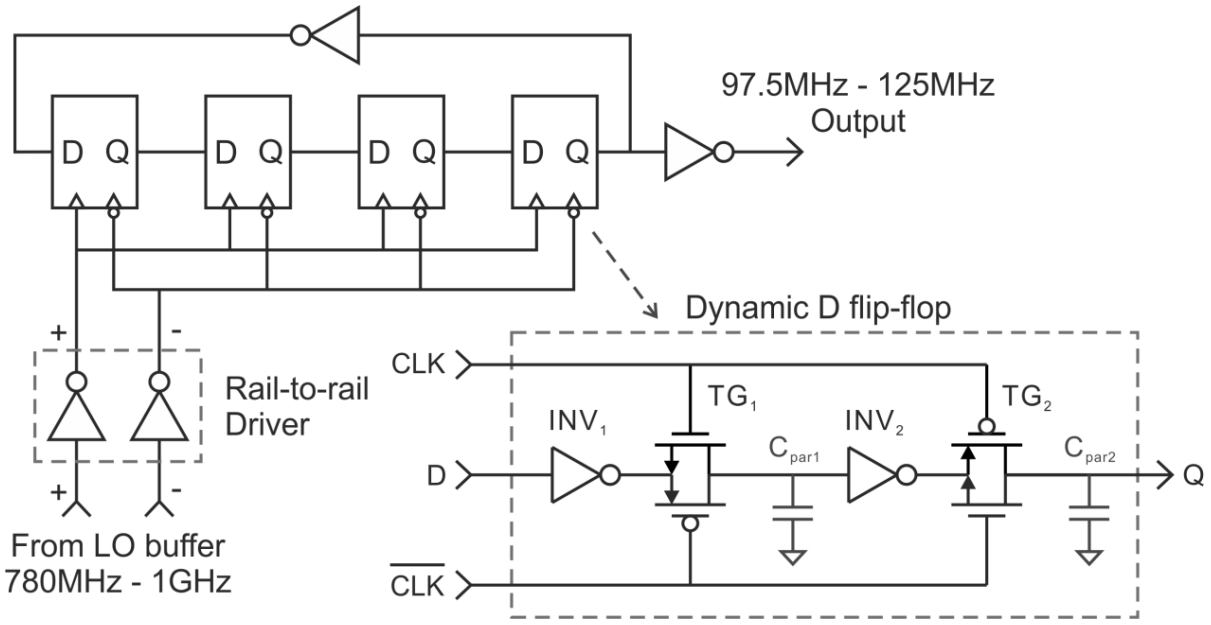


Figure 5-15: Dynamic LO frequency divider.

5.3 System Implementation

The event-driven transmitter front-end is manufactured in the same 90nm CMOS technology as the proof-of-concept circuits in Chapter 3. The digital baseband and IF modules, as well as the LO swing and frequency calibration algorithms are implemented in a Xilinx Virtex-5 FPGA

platform for flexibility. The digital logic on the FPGA can be combined with the analog front-end in a single IC, if desired.

The CMOS chip is wire-bonded in a quad flatpack no-lead (QFN) package with 48 pins. A serial peripheral interface (SPI) bus and internal digital registers are the digital interface designed to control the operation of the circuits. Figure 5-16 shows the chip micrograph, where the active circuitry occupies 0.71mm^2. The packaged chip is soldered to a 4-layer printed circuit board (PCB), together with the DCO inductor and the output matching network.

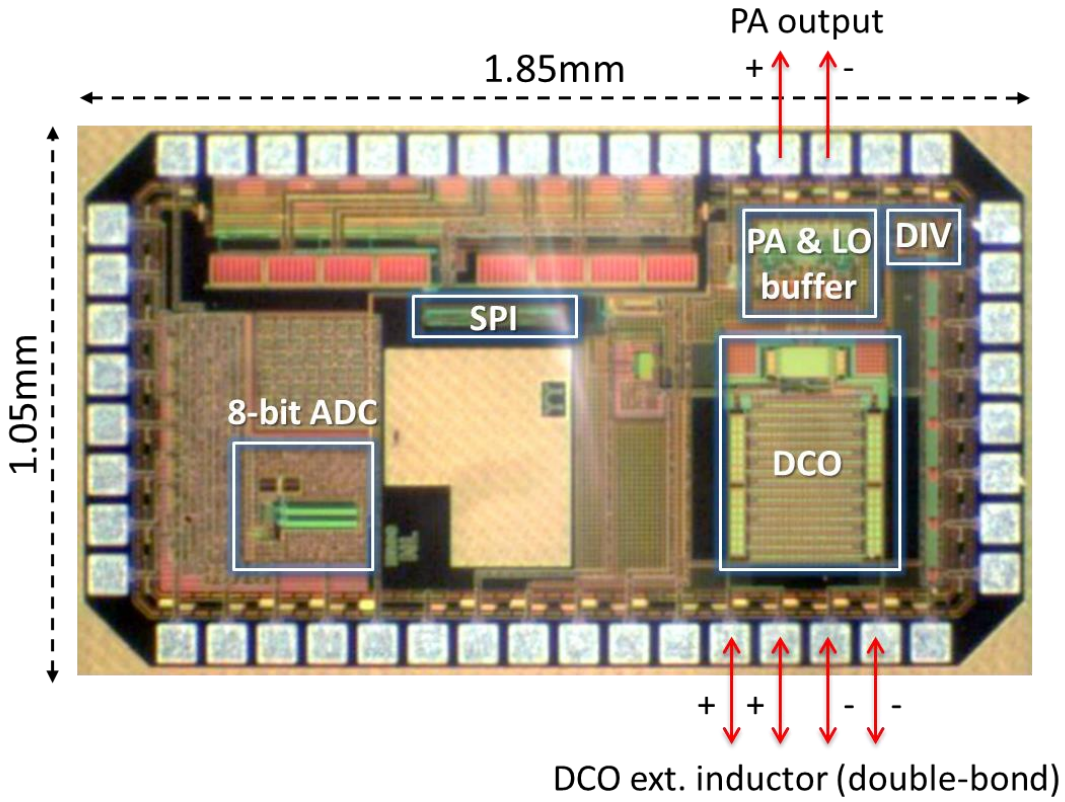


Figure 5-16: Chip micrograph of the 2-tone event-driven transmitter.

5.3.1 LO Swing Calibration Loop

The block diagram of the LO swing calibration loop is shown in Figure 5-17. The output of the on-chip RF swing to digital converter is fed to the calibration logic on the FPGA, which compares the detected swing to a target reference and searches for the correct biasing level for the DCO and LO buffer. A flow chart for the calibration algorithm is shown in Figure 5-18. The

DCO output swing is calibrated as the first step. A stepwise searching algorithm is adopted to increase the 6-bit DCO bias level from zero, until the target swing level is reached. Then the PA input swing is calibrated using the same algorithm so that the 6-bit bias level of the LO buffer is found and fixed.

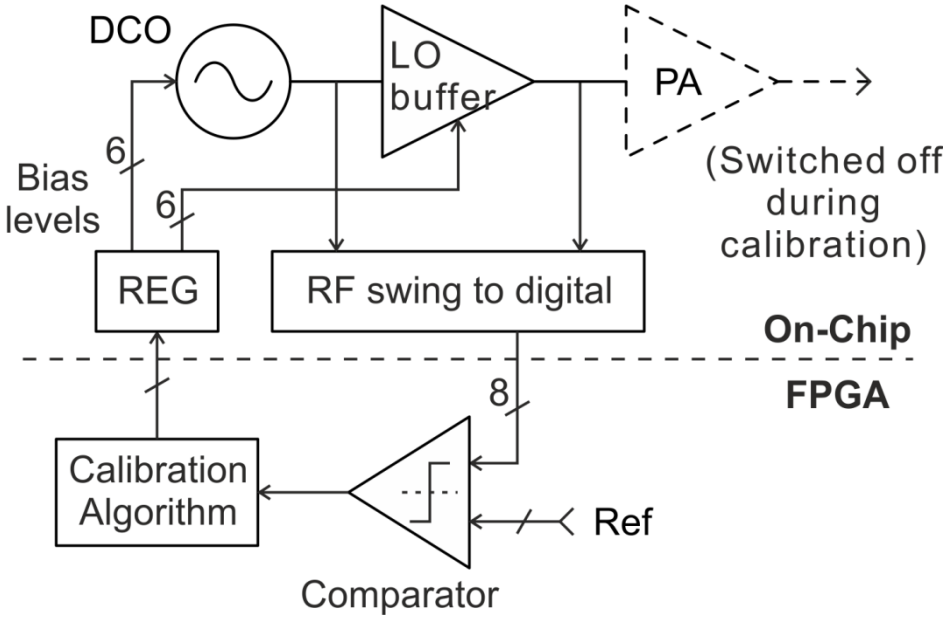


Figure 5-17: Block diagram of the LO swing calibration loop.

The calibration is carried out with the PA switched off. After calibration, the calibration loop is deactivated and bias settings are stored in the on-chip digital registers (REG).

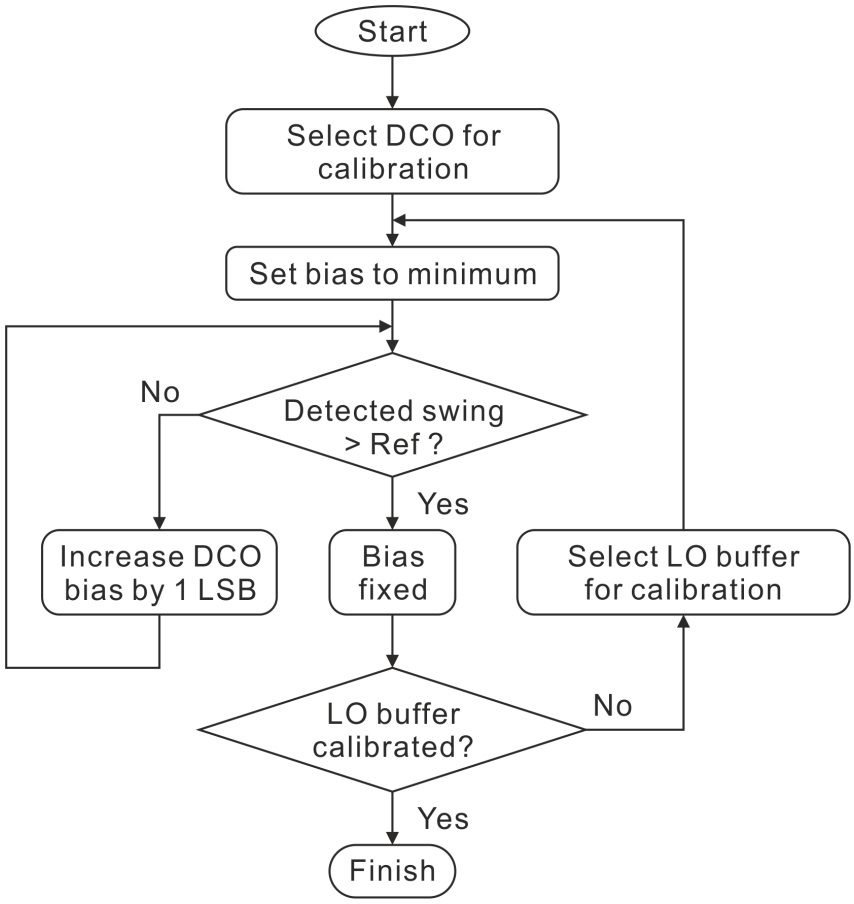


Figure 5-18: Flow chart of the LO swing calibration algorithm.

5.3.2 LO Frequency Calibration Loop

A block diagram of the LO frequency calibration loop is illustrated in Figure 5-19. The output clock of the on-chip LO frequency divider (i.e., CLK_V), is provided to a 13-bit clock counter. The counter accumulates the rising edge of CLK_V within each 32kHz reference clock period (i.e., CLK_{REF}) to estimate the LO frequency. The counter output is compared to a frequency control word (FCW), and a successive approximation register (SAR) searching algorithm is employed to find the coarse and fine oscillator tuning words (OTW).

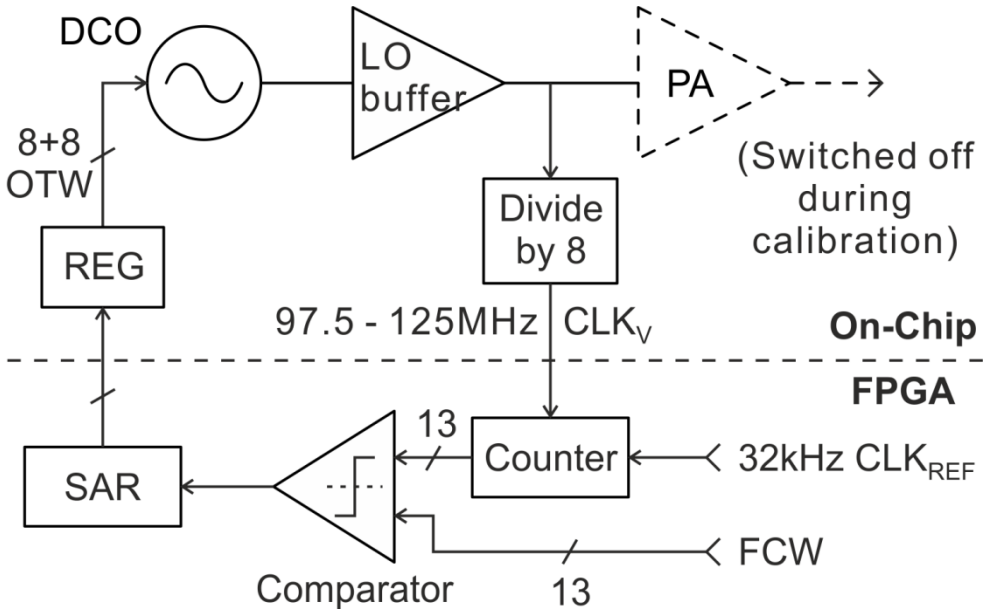


Figure 5-19: Block diagram of the carrier frequency calibration loop.

The timing of the frequency calibration operation is illustrated in Figure 5-20. As both the coarse and the fine OTW consist of 8 bits, it takes 16 iterations to complete the SAR search. Within each iteration, two reference clock cycles are required. The first cycle is used for counting, while the second cycle is used for updating the OTW, reset the counter, and settling of the DCO frequency. The coarse OTW is searched first, followed by the search of the fine OTW. In total, the calibration operation takes 32 reference clock cycles and lasts for 1ms. Once calibrated, the calibration loop including the on-chip divider is switched off, and the OTWs are stored in on-chip digital registers.

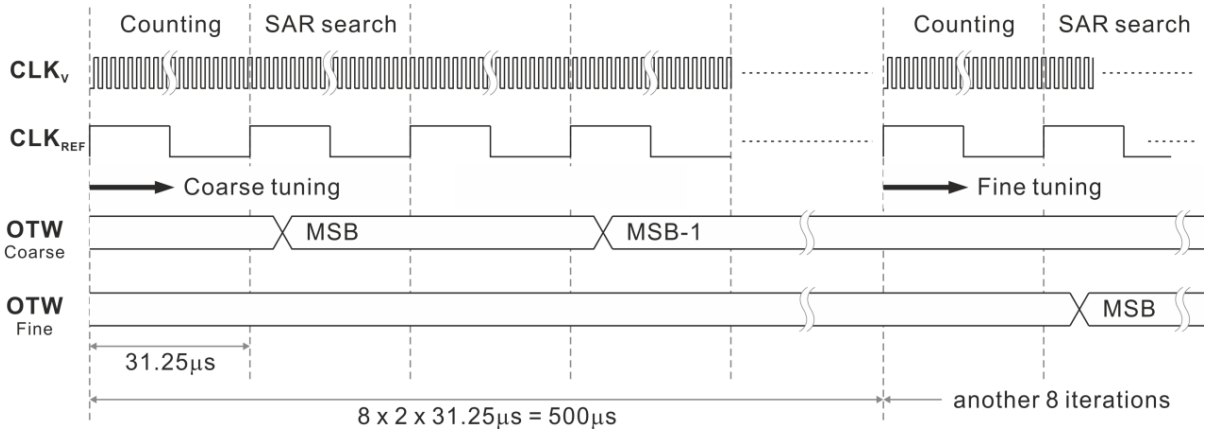


Figure 5-20: Timing diagram of the LO frequency calibration loop.

In order to obtain the desired LO frequency (i.e., f_{LO}), the FCW should be set as:

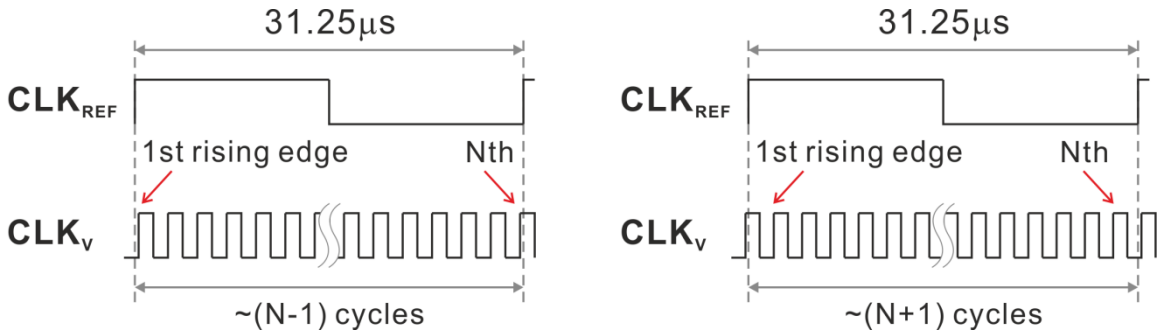
$$FCW = \left\lfloor \frac{f_C}{8 \times f_{REF}} + 0.5 \right\rfloor = \left\lfloor \frac{f_C}{8 \times 32kHz} + 0.5 \right\rfloor, \tag{5.9}$$

where f_{REF} is the reference frequency, in this case 32kHz. The floor operator (i.e. $\lfloor \bullet \rfloor$) and the addition of 0.5 round the FCW to the nearest integer, which is required due to the limited number of bits in the FCW and counter. This leads to a quantization error (i.e., ε_{FCW}) up to

$$\varepsilon_{FCW} = \pm 0.5 \times 8 \times f_{REF} = \pm 0.5 \times 8 \times 32kHz = \pm 128kHz . \tag{5.10}$$

On the other hand, since the counter is only capable to determine the integer number of CLK_V cycles in one reference cycle, another source of frequency error exists. Figure 5-21 illustrates the worst-case frequency errors due to integer resolution of the counter. Despite counting N rising edges, the number of CLK_V cycles within one reference clock cycle could range from N-1 to N+1. The frequency error (i.e., ε_{CNT}) corresponding to this ±1 cycle uncertainty is:

$$\varepsilon_{CNT} = \pm 1 \times 8 \times f_{REF} = \pm 1 \times 8 \times 32kHz = \pm 256kHz . \tag{5.11}$$



(a) N-1 cycles with N rising edge (b) N+1 cycles with N rising edge

Figure 5-21: Frequency error due to counter operation.

In addition, the oscillation frequency can deviate from the desired value by the DCO fine-tune resolution after the last SAR search operation. In the worst case, it is given by

$$\varepsilon_{DCO} = \pm f_{RES,DCO} , \tag{5.12}$$

where ε_{DCO} is the frequency error and $f_{RES,DCO}$ is the tuning resolution of the DCO fine bank, which is below 50kHz from simulation.

The total frequency error (i.e., ε_{LO}) after calibration is the summation of ε_{FCW}, ε_{CNT} and ε_{DCO} (assuming that they are uncorrelated) is given by

$$\varepsilon_{LO} = \varepsilon_{FCW} + \varepsilon_{CNT} + \varepsilon_{DCO} = \pm 128kHz \pm 256kHz \pm f_{RES,DCO} \leq 434kHz\,. \quad (5.13)$$

The LO frequency error ε_{LO} should be smaller than the allowed f_{LO} range illustrated in Figure 5-3 via system level frequency planning. As an example, if the entire 26MHz (902MHz – 928MHz) ISM band is available for the transmitter, and the 2-tone separation is chosen as 8MHz, the allowed LO frequency range is 26MHz – 8MHz = 18MHz. This is much larger than the LO frequency error given in (5.13). Since ε_{FCW} and ε_{CNT} are proportional to f_{REF}, it is possible to reduce the frequency error further by using a lower reference frequency, at the cost of longer calibration time (32 reference cycles).

5.4 Evaluation Results

The evaluation of the event-driven transmitter covers the DCO performance, the power efficiency of PA and transmitter, the quality of the modulated output signal, as well as power consumption analysis.

5.4.1 DCO performance and calibration

With a 15nH (nominal) inductor, the DCO can be tuned from 780MHz to 1GHz. Between the coarse and fine tuning steps, overlapping frequency ranges exist as shown in Figure 5-22. Despite uncertainty in the off-chip inductor (15nH ±5%), the measured deviation in frequency range among 5 measured samples is less than 2%. The fine resolution is 17kHz at 900MHz, and below 27kHz across the entire range.

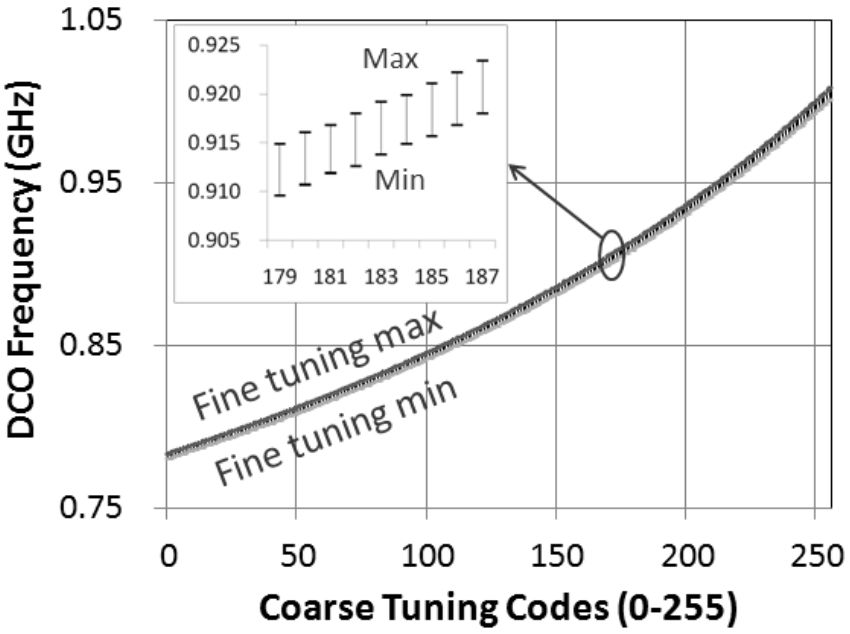


Figure 5-22: Measured DCO frequency tuning range.

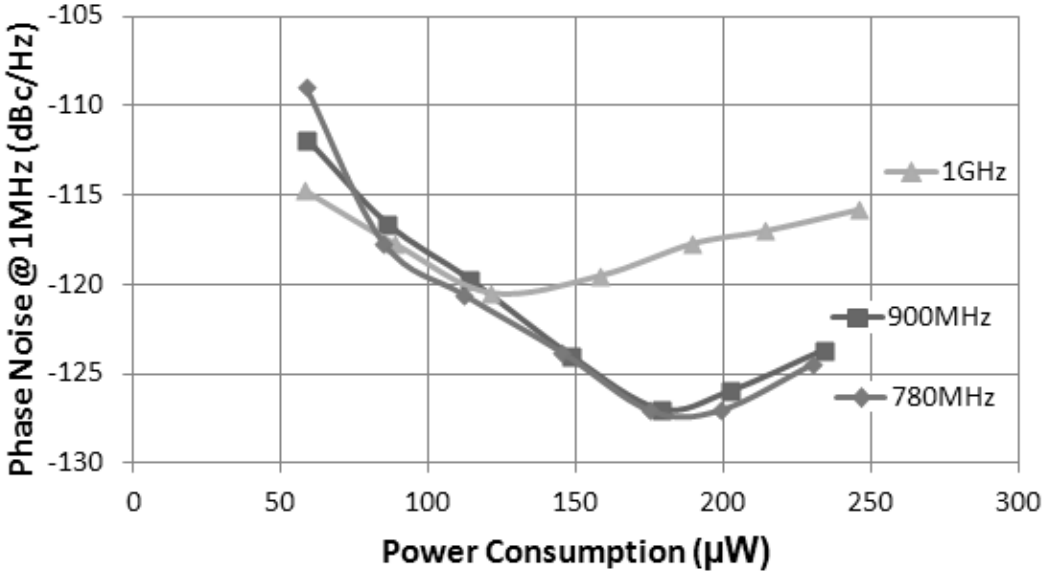
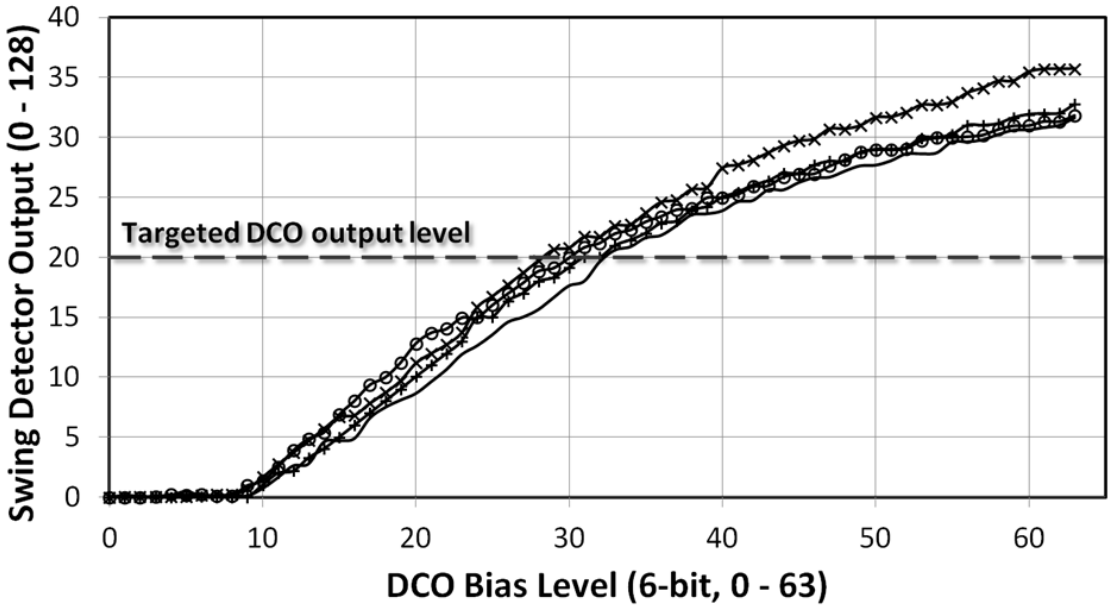
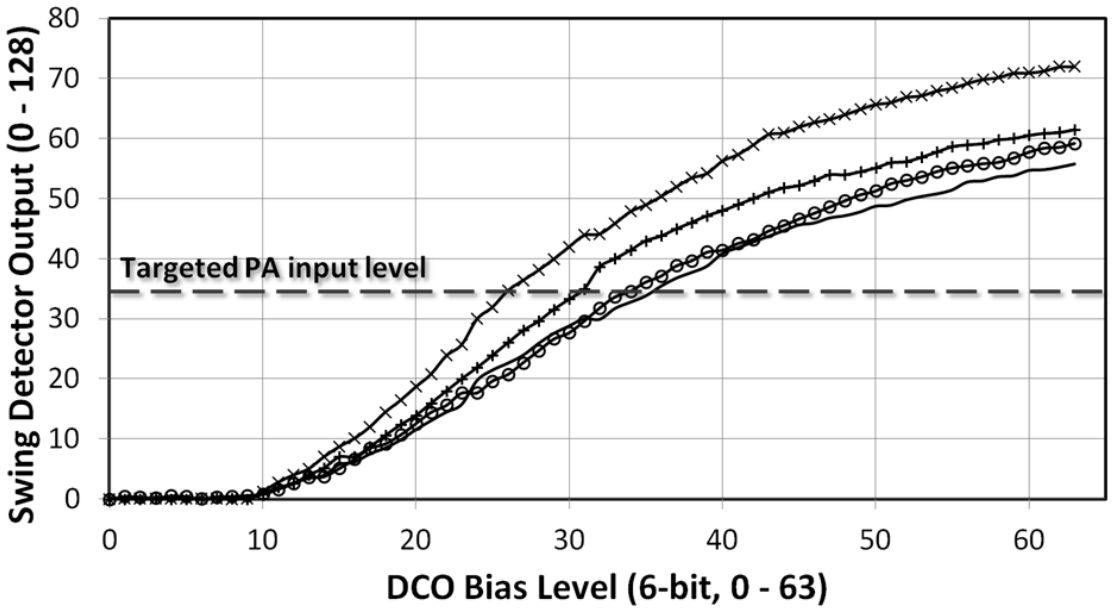


Figure 5-23: Measured DCO phase noise at different output frequencies.

Figure 5-23 shows the DCO phase noise at 1MHz offset when tuned to different center frequencies and at different power levels. The phase noise can be optimized below -120dBc/Hz by adjusting the bias current. Nominally, the DCO is biased at 150μA and achieves -124dBc/Hz at 1MHz away from the 900MHz center frequency.



(a) Detected DCO output swing



(b) Detected PA input swing

Figure 5-24: Measured output of the RF swing to digital converter with DCO bias level swept in 4 test chips.

The RF swing to digital converter is verified by testing multiple chips. Figure 5-24(a) shows the detected DCO output swing when the DCO bias level is swept from minimum to maximum. The four samples measured show relatively good convergence. Figure 5-24(b)

shows the converter output for the PA input swing with the DCO bias level swept. The signal levels in the 4 test chips show larger variation. Post layout Monte Carlo simulation of 100 samples shows a standard deviation of ±10% in the LO buffer gain referring to the average, which is in accordance with the measured data. The variation is caused by the transistor mismatch between the biasing current mirror (M_9 in Figure 5-12) and its corresponding active transistors (M_3 and M_4 in Figure 5-12). Thanks to the swing calibration loop, such gain variations can be calibrated.

Two mixed-signal calibration loops are also verified in the measurements. As the bias level of the DCO and LO buffer may shift the LO frequency slightly, the LO swing calibration loop is activated first. After the DCO and the LO buffer are biased correctly, the frequency calibration loop is enabled to adjust the LO frequency within ±411kHz (DCO fine tune resolution better than 27kHz). The calibration loops are then switched off, and the transmitter is ready to deliver output signal.

5.4.2 Power efficiency

The output power level of the PA is up to 0dBm when the differential output is taken. In such a case, the PA consumes 2.35mW with a drain efficiency of 42.5%. Together with 300μW pre-PA power consumption (including biasing, DCO and LO buffer), the global power efficiency of the Tx front-end is 37.7%. As shown in Figure 5-25, when the number of active PA units is reduced from 7 to 1, both the output power and power efficiency decrease. When delivering a 2-tone IF-PSK or a conventional OOK modulated signal, the maximum output power becomes -3dBm, with 33.9% global efficiency. When a single-ended output stage is used, the transmitter delivers up to -6dBm average output level with 893μW power consumption, resulting in 28.1% global efficiency.

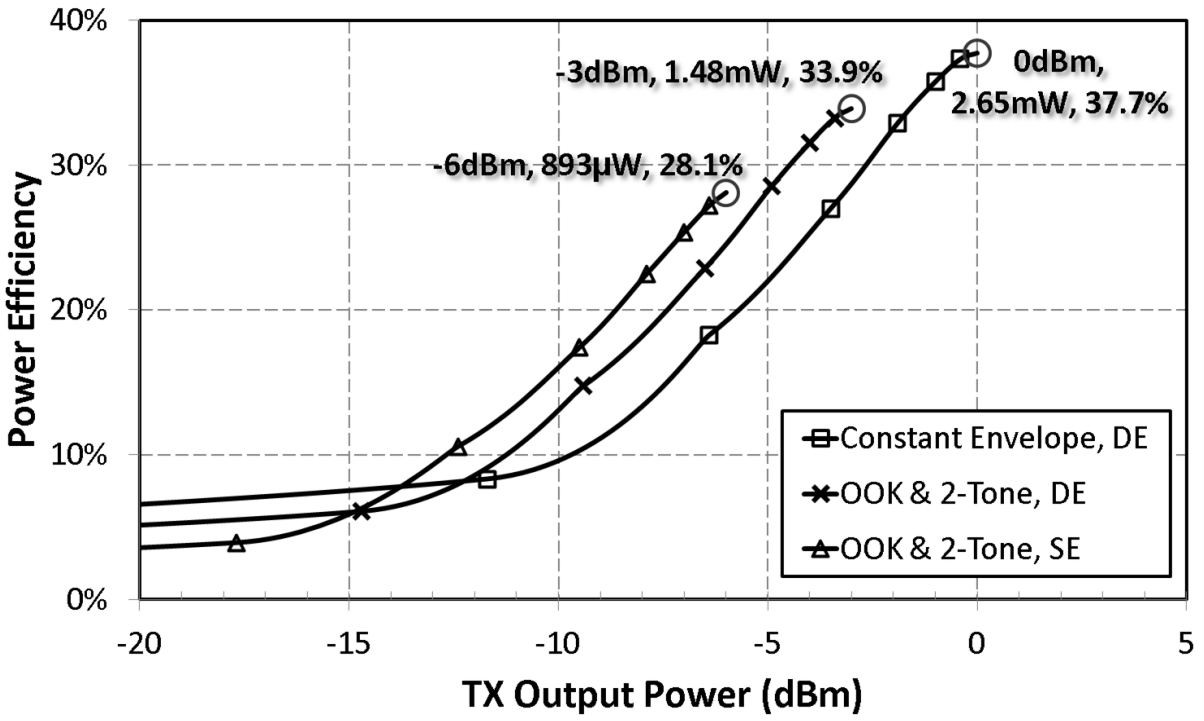


Figure 5-25: Measured global power efficiency at different output levels (differential / single-ended).

5.4.3 Tx modulation

The 2-tone IF-PSK modulated signal is shown in Figure 5-26 with 10kbps data rate and 8MHz 2-tone separation around the 916MHz center frequency. Data rates up to 1Mbps can be supported in IF-PSK mode, which is sufficient for generic event-driven applications. Sidelobes can be observed together with the 2 desired tones in the output spectrum shown in Figure 5-27. This is expected due to the digitized IF signal that modulates the LO signal. The sidelobes are only suppressed to a limited extent by the output matching network (Q-factor below 20). For higher suppression, a high-Q surface-acoustic wave (SAW) filter can be used at the cost of an output power loss of approximately 3dB [117]. In fact, as will be described in the next chapter, the event-driven receiver will be equipped with a SAW filter, so no SAW filter is required for the transmitter. When the transmitter operates in single-end output mode, the mismatch in the front-end circuitry will introduce a leakage tone at the 916MHz LO frequency, 23dB below the main tones.

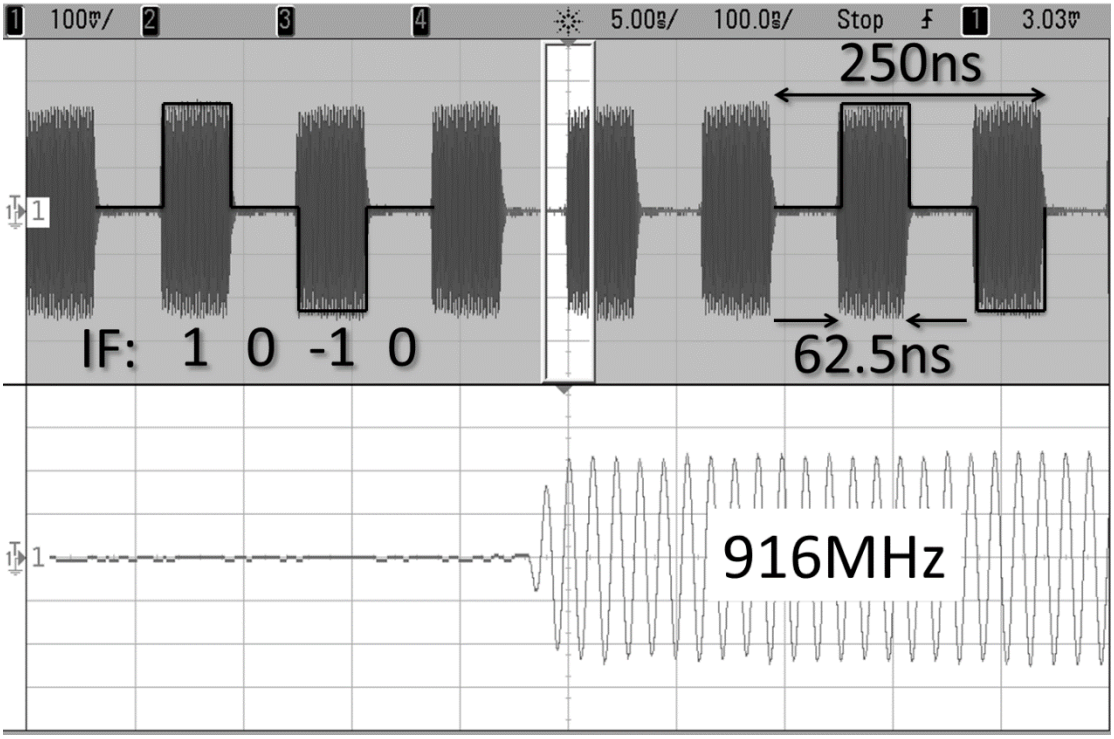


Figure 5-26: 2-tone output signal waveform with 8MHz tone spacing around 916MHz.

In both OOK and BPSK mode, the transmitter supports data rates up to 10Mbps. Figure 5-28 and Figure 5-29 show the Tx output waveform in OOK and BPSK modes, respectively. Note that the transition between '0' and '1' in OOK and BPSK modes is approximately 3ns and 4ns, respectively, much less than the 100ns bit duration of 10Mbps signals.

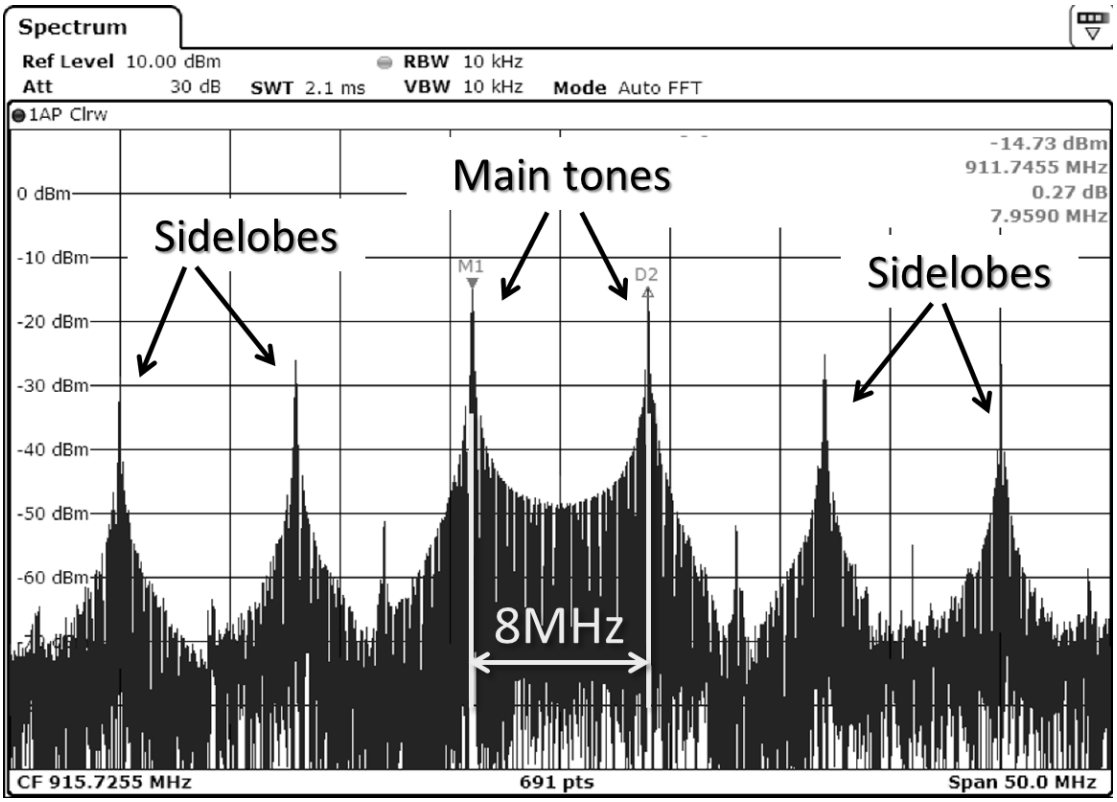


Figure 5-27: 2-tone output signal spectrum with 8MHz tone spacing around 916MHz.

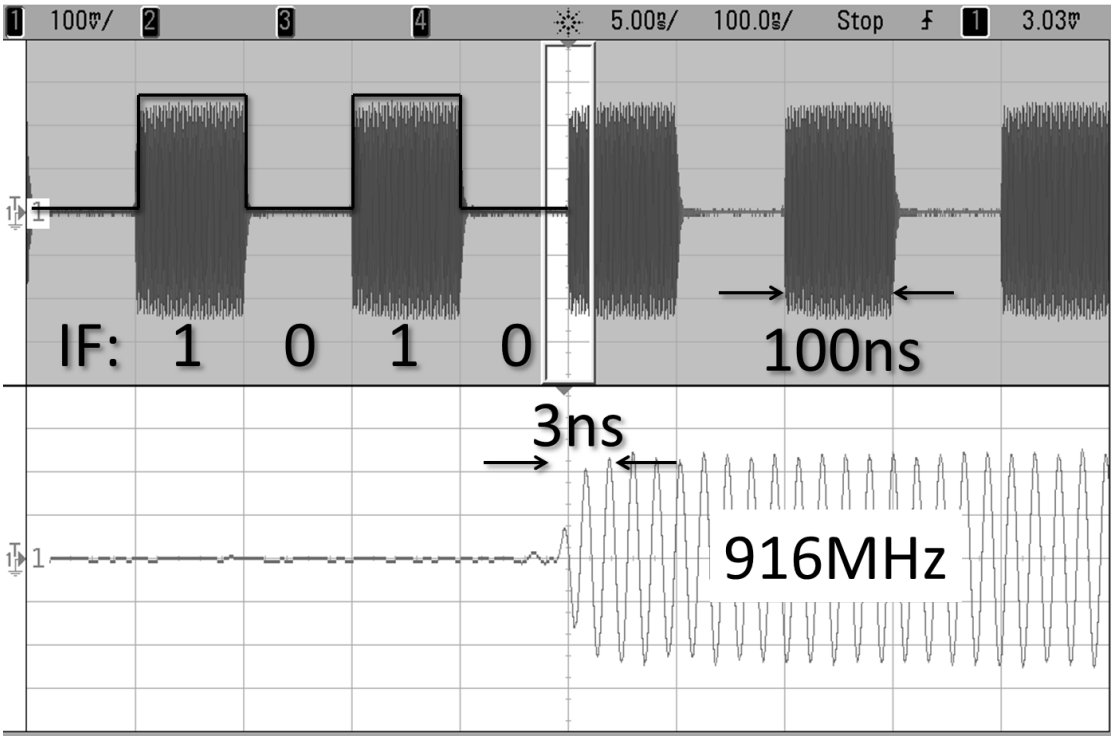


Figure 5-28: 10Mbps OOK output waveform at 916MHz.

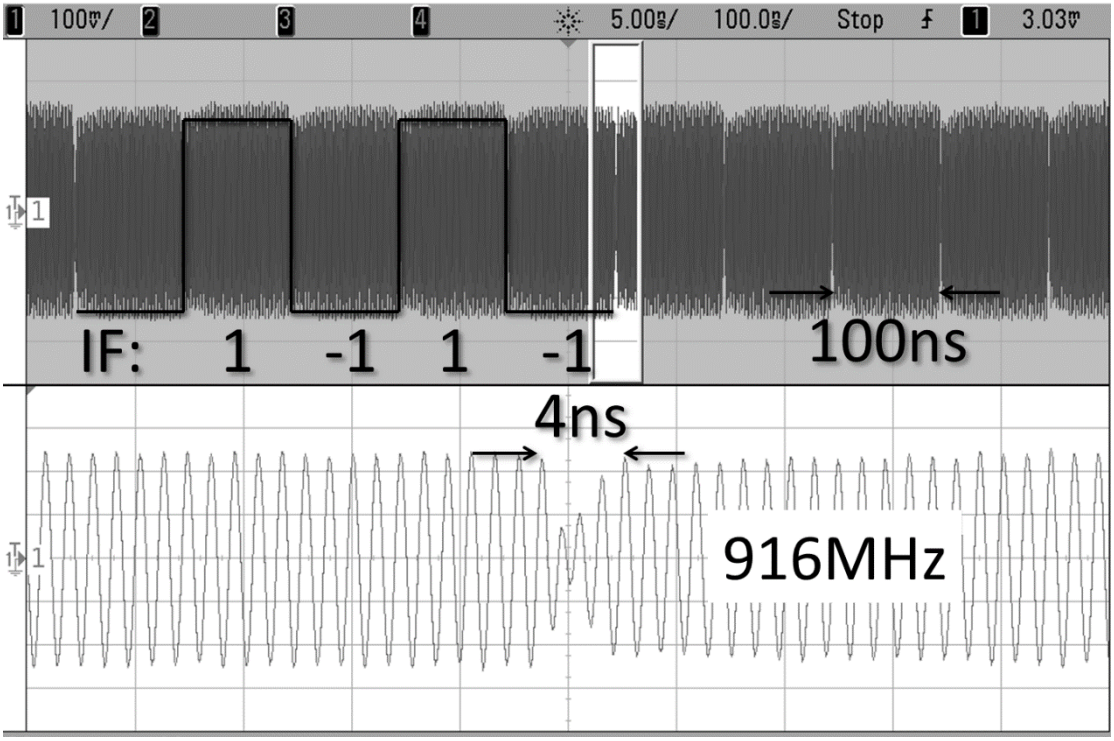


Figure 5-29: 10Mbps BPSK output waveform at 916MHz.

5.4.4 Power consumption analysis

A power consumption breakdown of the event-driven transmitter front-end is shown in Figure 5-30. The transmitter operates in 2-tone IF-PSK or OOK modes, with -6dBm single-ended output power on average. The total power consumption is 893 μW, 28.1% of which is delivered to the 50Ω load.

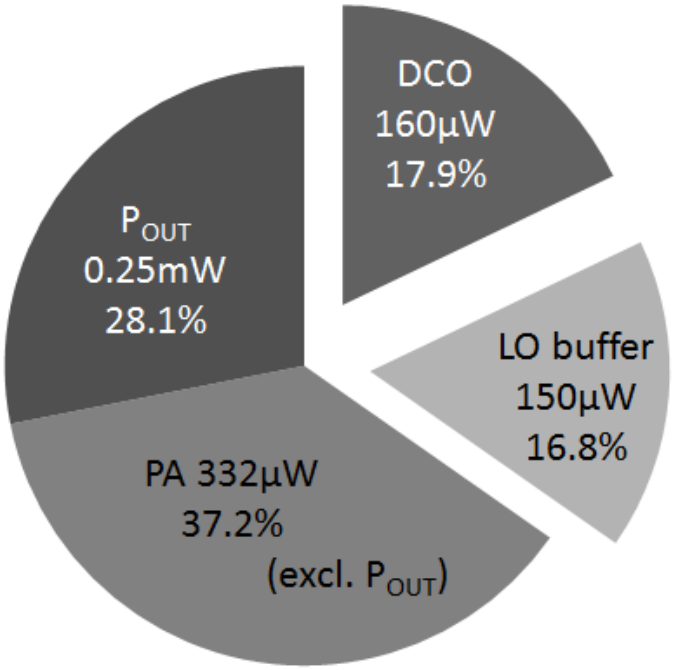


Figure 5-30: Power consumption breakdown of the Tx front-end at -6dBm output level (single-ended output).

5.5 Conclusions

An ultra-low-power Tx front-end is implemented to carry out the 2-tone signaling scheme proposed in Chapter 4. The digital-IF architecture only requires a carrier DCO, LO buffer and a digital controlled PA in the analog front-end, while modulation is applied directly to the PA. Two mixed-signal calibration loops are implemented to ensure the performance regardless of on-chip PVT variations or off-chip component tolerance. Several modulation schemes are supported, including the 2-tone IF-PSK modulation, OOK and BPSK modulation, with output power from -6dBm to 0dBm. The Tx front-end consumes as little as 893µW when activated, fulfilling the power budget desired for generic event-driven radio applications.

In Figure 5-31, the event-driven transmitter is compared with other state-of-the-art low-power transmitters surveyed in Figure 1-6. Compared to others, this transmitter achieves state-of-the-art low power consumption while maintaining a high overall efficiency of 28.1%. Most importantly, this transmitter supports the 2-tone IF-PSK modulation without increasing

complexity or power consumption, which will enhance the sensitivity and selectivity of a 2-tone envelope detection receiver.

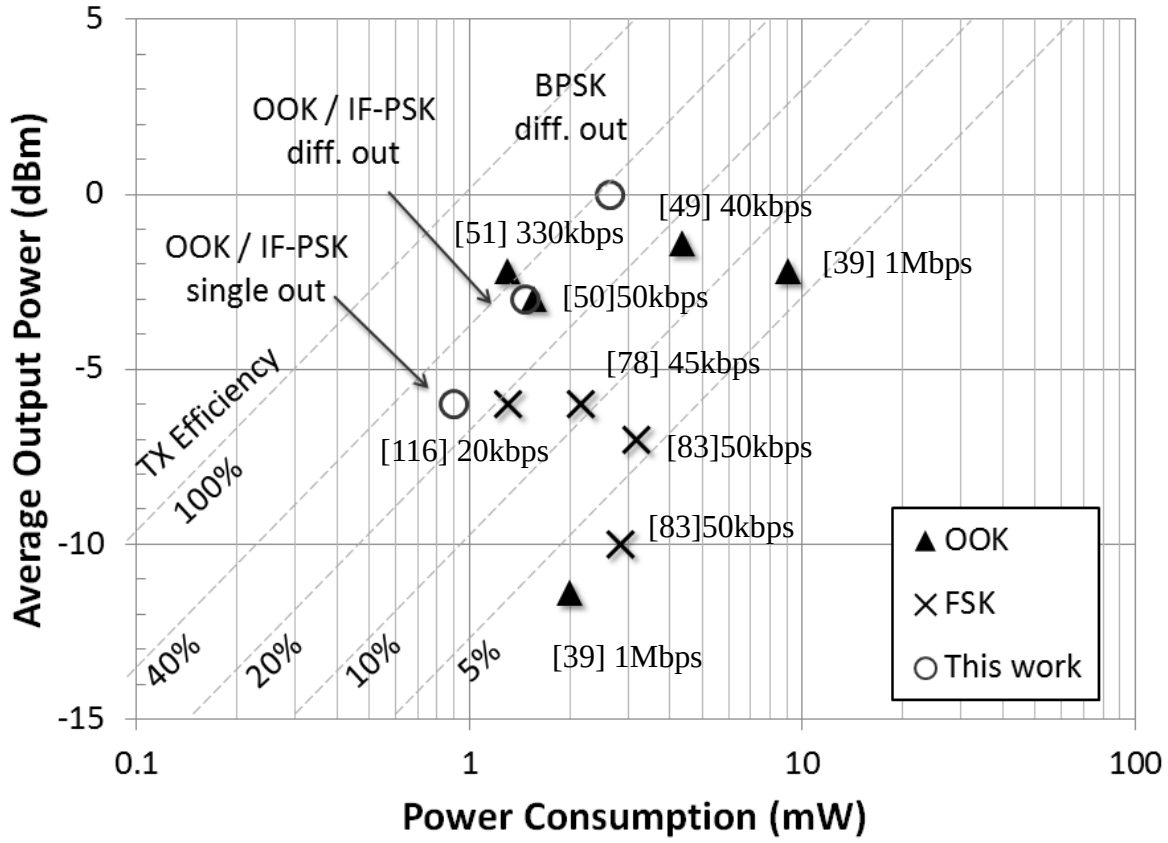


Figure 5-31: Comparison to state-of-the-art ultra-low-power transmitters.

In the next chapter, the event-driven receiver is implemented to realize the enhancements from the 2-tone envelope detection scheme.

Chapter 6

2-Tone Envelope Detection Receiver

In this chapter, the design of a 2-tone envelope detection receiver is presented. In section 6.1, the front-end architecture and demodulation method for a 2-tone IF-PSK signal is proposed. In section 6.2, the front-end circuit blocks are described, followed by the system-level implementation detailed in section 6.3. In section 6.4, the receiver chip is evaluated, and conclusions are drawn in section 6.5.

6.1 Architecture

To detect and demodulate 2-tone IF-PSK modulated signals described in Chapter 5, a novel receiver architecture based on envelope detection is required. In this section, a low-power receiver front-end and a low-complexity IF-PSK demodulation method are presented.

6.1.1 2-Tone Envelope Detection Receiver Front-End

The receiver front-end needs to accomplish several tasks before the 2-tone IF-PSK signal can be demodulated. Firstly, it needs to pre-filter the input RF signal to reject out-of-band interferers, and then square the RF signal to generate the intermodulation signal. Then the intermodulation signal should be downconverted to the baseband, while interference and noise at other frequencies should be suppressed. Lastly, the analog signal needs to be digitized for processing by the digital baseband (DBB).

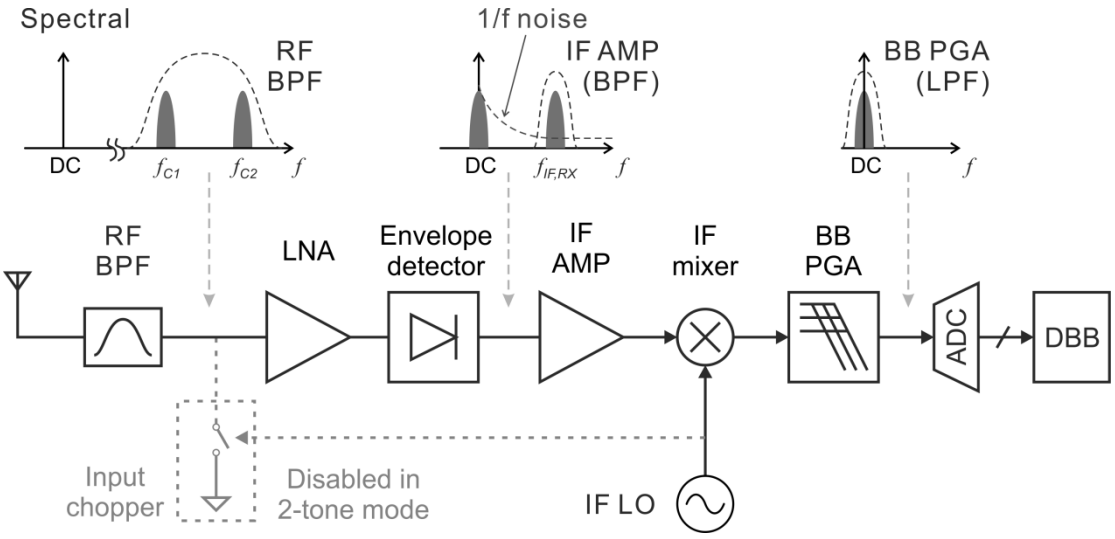


Figure 6-1: Architecture of the proposed 2-tone envelope detection receiver.

The block diagram of the proposed receiver front-end is shown in Figure 6-1. An RF band-pass filter (BPF), either inherent in the response of the input matching network and LNA or implemented using a high-Q resonator, suppresses out-of-band interference. The desired 2-tone signal located at f_{C1} and f_{C2} is amplified by the LNA. An envelope detector squares the LNA output signal, generating frequency components around DC and at the intermediate frequency (i.e., $f_{IF,RX} = |f_{C2} - f_{C1}|$). An intermediate frequency amplifier (IF AMP), which also serves as a band-pass filter, amplifies the signal component at $f_{IF,RX}$ and attenuates the DC and high frequency components. An IF mixer driven by an IF local oscillator (LO) downconverts the signal from $f_{IF,RX}$ to DC, and a programmable gain amplifier (PGA) low-pass filters the baseband signal with variable gain. An analog-to-digital converter (ADC) digitizes the analog baseband signal so that further signal processing and demodulation can be carried out in a digital baseband (DBB) module.

The proposed architecture features an IF stage composed of an amplifier and a mixer. As the intermediate frequency is much lower than the carrier frequency (e.g., by a factor of 1/100 if 9MHz 2-tone separation is used in a 900MHz radio) the added power consumption from the IF stage is insignificant in the total power dissipation. Hence, the proposed receiver can potentially achieve power efficiency similar to a conventional envelope detection receiver.

The proposed receiver can also support single-tone OOK modulation by using a grounding chopper at the LNA input. Driven by the IF LO signal, the chopper shorts the input signal to ground periodically, and the receiver operates in synchronized-switching mode (as presented in Chapter 3). Note that the receiver still benefits from 1/f noise suppression in the 2-tone mode, as long as the intermediate frequency (i.e., $f_{IF,RX}$) is chosen higher than the 1/f corner frequency.

6.1.2 2-Tone IF-PSK Demodulation

The IF-PSK modulated 2-tone signal at different stages of the receiver is illustrated in Figure 6-2. After the front-end filter and LNA, the envelope of the RF signal is a sinusoid at frequency $f_{IF,TX}$, which is one half of the 2-tone separation according to section 5.1.1. There is 90 °phase difference in the carrier envelope between '0' and '1' symbols. After envelope detection, the intermodulation component is obtained. The DC component is removed by the IF AMP. The intermodulation frequency is equal to the 2-tone separation, i.e., $f_{IF,RX} = 2f_{IF,TX}$. Due to the frequency doubling at the receiver, the phase difference in the IF signal between '0' and '1' is 180 °. In other words, the desired signal in the receiver IF stage is binary PSK (BPSK) modulated, which becomes clear after the DC and high frequency signals are suppressed by the IF AMP.

To demodulate the BPSK modulated signal at the receiver IF, quadrature downconversion is required so that the IF phase can be mapped to in-phase (I) and quadrature (Q) components on the constellation for later demodulation. In this case, the analog baseband of the receiver needs to be implemented as shown in Figure 6-3. Two IF mixers, two BB PGAs and two ADCs are required, in addition to quadrature IF LO signals.

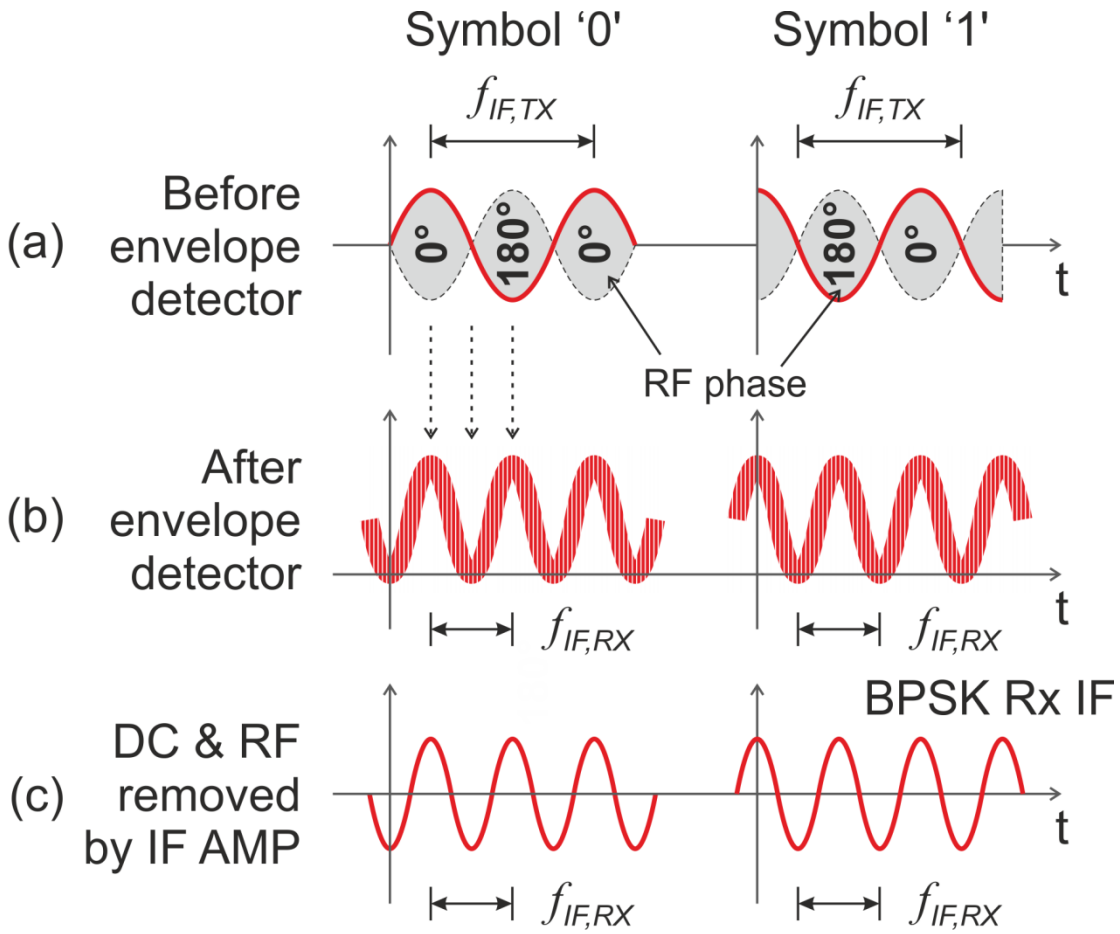


Figure 6-2: Illustration of the downconversion steps in the receiver.

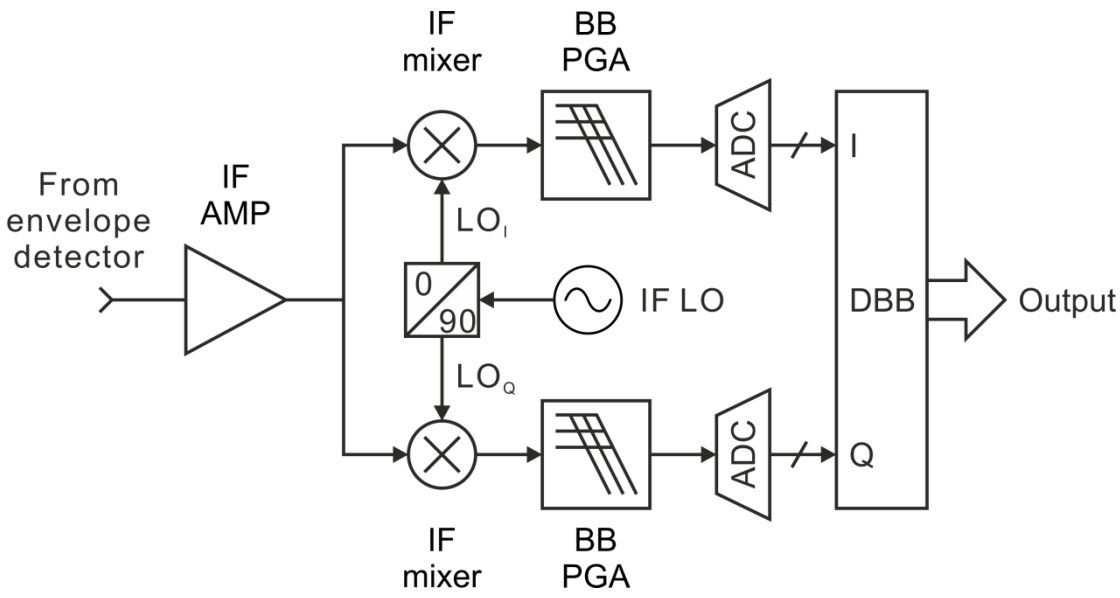


Figure 6-3: Quadrature analog baseband for PSK signals.

To minimize power consumption and reduce chip area, an alternative implementation is proposed to avoid using quadrature signals in the analog baseband. The single-phase analog baseband proposal is shown in Figure 6-4, where the IF signal is not downconverted to DC, but rather to another (lower) IF which can still accommodated by the BB PGA and ADC. The low-IF signal is then downconverted to baseband using a complex numerically-controlled oscillator (NCO), two multipliers and two digital LPFs. The resulting digital I/Q signal can be used for BPSK demodulation, which will be described in section 6.3.

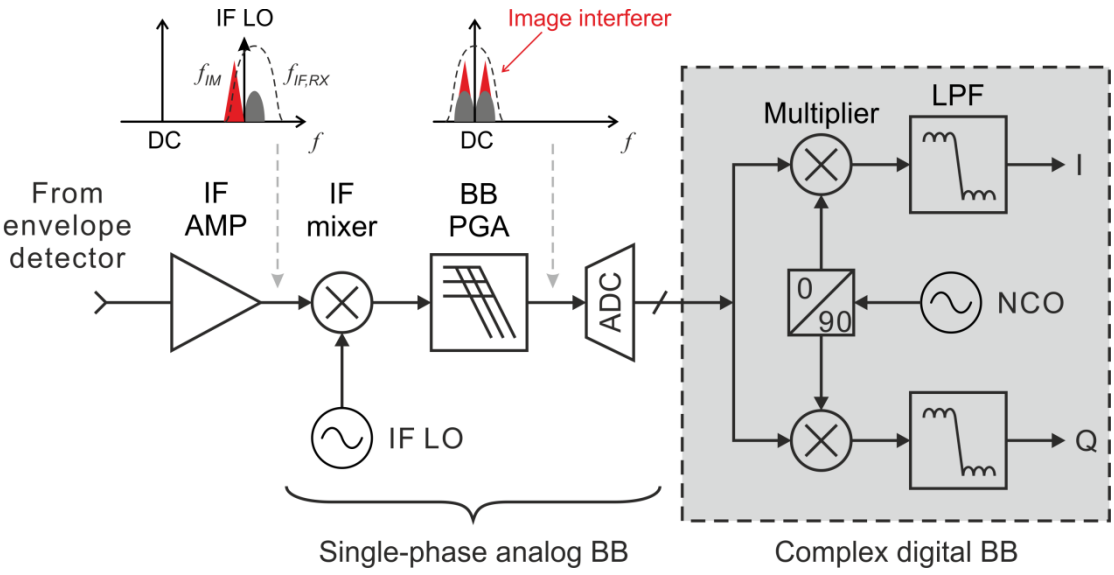


Figure 6-4: Single-phase analog baseband using low-IF and digital downconversion.

Similar to super-heterodyne and low-IF receivers, the proposed single-path analog baseband suffers from potential interference at the image frequency [77]. In this work, the low-IF output (f_{LIF}) of the analog baseband is:

$$f_{LIF} = f_{IF,RX} - f_{IF,LO}\,, \tag{6.1}$$

where $f_{IF,LO}$ is the frequency of the IF LO. As the IF LO is single-phase, interference at the image frequency (f_{IM}) will also be downconverted to f_{LIF}, and can no longer be separated from the desired signal. The image frequency is given by:

$$f_{IM} = f_{IF,LO} - f_{LIF} = f_{IF,RX} - 2f_{LIF}\,, \tag{6.2}$$

which is $2f_{LIF}$ away from the desired signal at the IF mixer input. In this work, the minimal f_{LIF} is chosen to minimize the bandwidth of the BB LPF and the sampling rate of the ADC. The minimal f_{LIF} is determined by the IF signal bandwidth (BW_{IF}):

$$f_{LIF} = BW_{IF} / 2. \tag{6.3}$$

As a result, the image is just adjacent to the desired signal at the IF mixer input, and it cannot be suppressed by the band-pass filtering of the IF AMP. The "dead zones" due to image interference occupy the same bandwidth as the desired 2-tone signal. For a 100kbps IF-PSK modulated signal, each carrier tone occupies roughly 200kHz bandwidth [88]. The two 200kHz dead zones are relatively small compared to the overall frequency band (e.g., 26MHz in the 915MH ISM band).

6.2 Front-End Circuit Design

Similar to the 2-tone transmitter, the event-driven receiver should operate in the 915MHz ISM band, as well as other sub-GHz license-free bands from 780MHz to 1GHz. The design considerations of the Rx front-end are detailed in this section.

6.2.1 Power-Efficient Multi-Stage LNA

According to the sensitivity analysis in Chapter 4, a high-gain, narrowband amplifier is desirable in envelope detection receivers. The noise figure of the amplifier should also be minimized with the available power budget. To maximize amplifier gain over power consumption (i.e., A_V/P_{DC}), iterative (cascaded) amplifier stages can be used [118]. To illustrate this, the gain of an amplifier stage (A_V) is assumed linearly proportional to its current consumption (I_{DC}) as a first-order approximation

$$A_V = k \cdot I_{DC}, \tag{6.4}$$

where k is a constant. For a multi-stage cascaded amplifier, the total gain is

$$A_{Total} = A_V^N = \left(k \cdot I_{DC}\right)^N = \left(\frac{k \cdot I_{Total}}{N}\right)^N. \tag{6.5}$$

For a desired gain (A_{Total}), the total current consumption (I_{Total}) can be minimized by finding the optimal number of stages:

$$N_{OPT} = N\left|\left(\frac{d(I_{Total})}{d(N)} = 0\right) = \ln\left(A_{Total}\right).\right. \tag{6.6}$$

The optimal gain per stage is *e* (Euler's number), or $20\log_{10}(2.7) = 8.7$dB. In this work, the gain of each amplifier stage is approximately 10dB, because the gain of an amplifier increases sub-linearly as its bias current is increased.

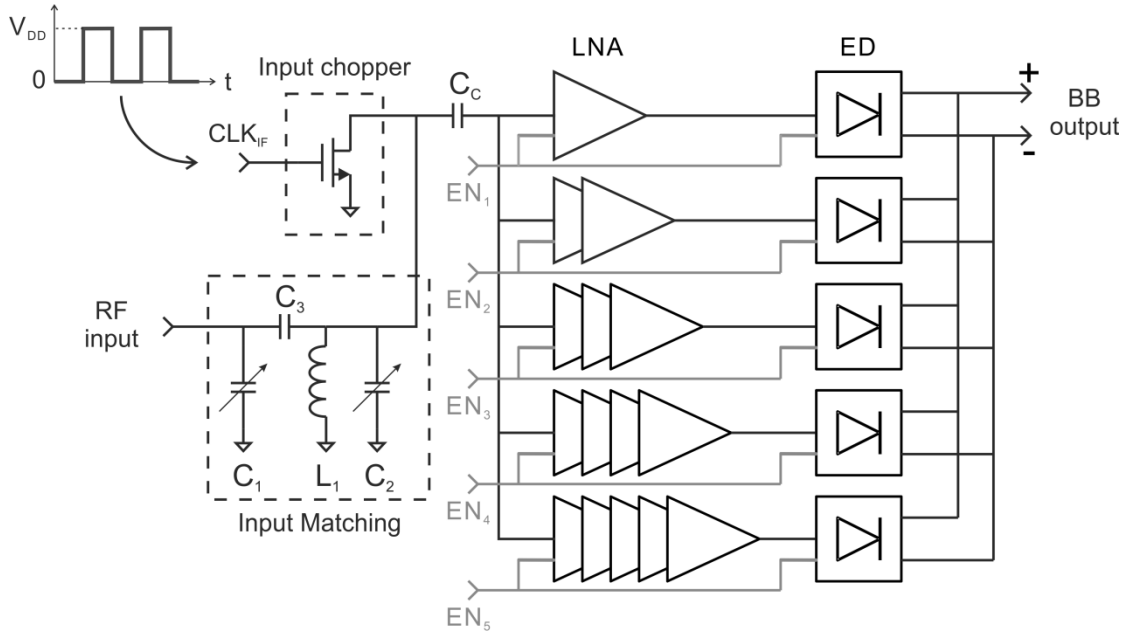


Figure 6-5: Block diagram of the programmable RF front-end.

To accommodate input level from -90dBm to -30dBm, the signal range in the RF front-end is 60dB. Furthermore, due to the squaring operation of the envelope detector ($y=kx^2$), the signal range is doubled to 120dB at the baseband. Such a large dynamic range will result in compression in this low-power, low-voltage receiver. In order to reduce the dynamic range, 5 signal paths with different numbers of cascaded amplifier stages (i.e., from 1 to 5) are implemented as the LNA, as shown in Figure 6-5. By choosing a signal path appropriate for the input signal level, the dynamic ranges of the RF and baseband signals are reduced to 10dB and 20dB, respectively. In addition, the power consumption of the LNA is scaled as the input level varies, because only one of the 5 signal chains is activated.

The input matching network is implemented on-chip with a programmable LC network. As shown in Figure 6-5, C_1 and C_3 form a capacitive transformer together with L_1 and C_2 [44]. It converts the 50Ω antenna impedance to match the input impedance of the LNA in the desired frequency band. The impedance transformation ratio is programmed by C_1, which is a digitally-controlled capacitor bank with 4 control bits. The resonant frequency of the network is adjusted by C_2, another 4-bit capacitor bank. By adjusting C_1 and C_2, input matching can be achieved from 750MHz to 1GHz.

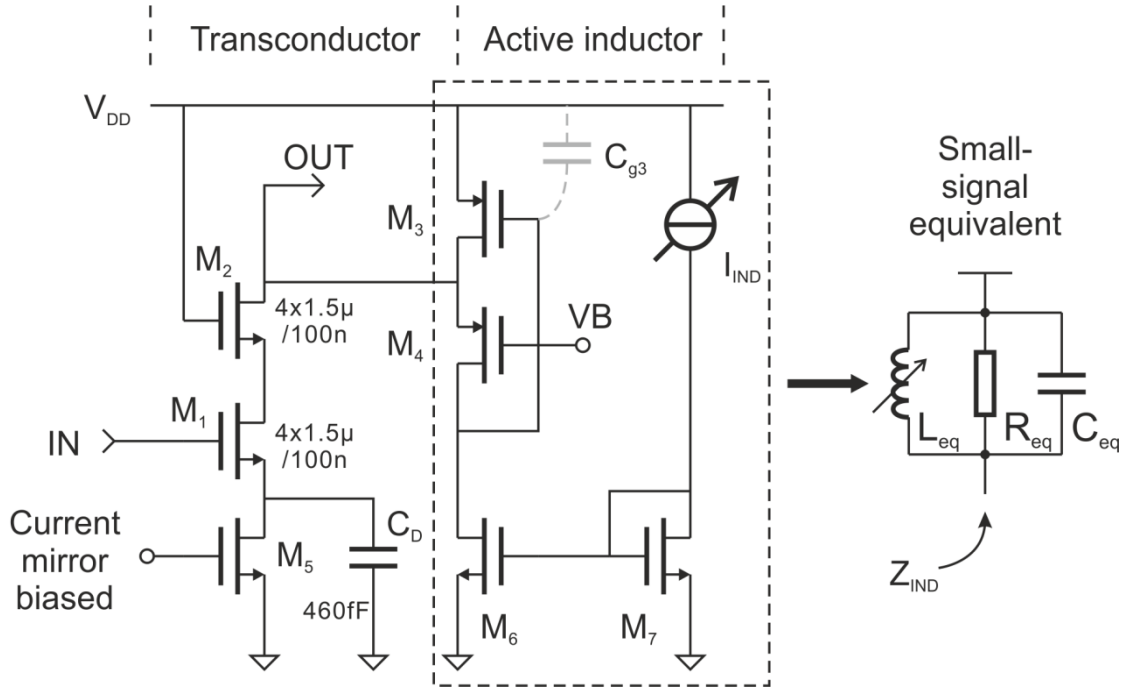


Figure 6-6: Schematic of a single LNA stage.

The schematic of a single amplifier stage is shown in Figure 6-6. The cascode stage is chosen for its high input and output impedances, as well as voltage gain. It also offers better reverse isolation than a common-source stage to avoid instability in the multi-stage amplifier. The driving transistor, M_1, is biased by NMOS current source, M_5. An on-chip decoupling capacitor of 0.5pF, C_D, is connected between ground and source of M_1 to lower the impedance at the source of M_1. As the bias current is determined by the current of M_5 instead of the gate voltage of M_1, several amplifier stages can be DC-coupled in cascade, eliminating the need for large (in size and value) AC coupling capacitors. Signal loss due to the substrate

parasitic capacitance of AC coupling capacitors is thus avoided, so that better power efficiency can be achieved.

A resonant load is implemented for each unit amplifier to a realize band-pass response centered at the carrier frequency. On-chip active inductors are adopted in the load to resonate with device (M2, M3 and M4) and parasitic capacitance at the output node. Unlike on-chip spiral inductors, an active inductor can be implemented with much smaller chip area since only MOS transistors are needed. This is especially beneficial in this work as a large number of inductors are needed for the 15 amplifier units. The drawbacks of active inductors are poor noise and linearity compared to passive inductors, which are addressed later.

As shown in Figure 6-6, the inductive load is realized with M_3 and M_4 as two transconductors. The small-signal equivalent circuit of the active inductor is the RLC network shown in Figure 6-6. The equivalent inductance [44] is $L_{eq} = \frac{C_{g3}}{g_{m4} g_{m3}}$, where g_{m3} and g_{m4} are the transconductance of M_3 and M_4, respectively, and C_{g3} is the total capacitance at the gate of M_3, contributed mainly by the gate-source capacitance of M_3. The equivalent parallel resistance is $R_{eq} = 1/g_{m4}$, and the equivalent parallel capacitance is $C_{eq} = C_{s4}$, where C_{s4} is the total capacitance at the source of M_4. It is dominated by C_{gs4}, the gate-source capacitance of M_4. The self-resonant frequency of the active inductor is thus

$$f_{res} = \frac{1}{2\pi\sqrt{L_{eq} C_{eq}}} = \sqrt{\frac{g_{m3}}{2\pi C_{g3}} \cdot \frac{g_{m4}}{2\pi C_{s4}}} \le \sqrt{f_{T3} \cdot f_{T4}}\,, \tag{6.7}$$

where f_{T3} and f_{T4} are the transit frequencies of M_3 and M_4, respectively. The minimum gate length is chosen for M_3 and M_4 and they are biased to give transit frequencies of 5.7GHz and 8.5GHz, respectively. Similarly, the minimum gate length is chosen for M_1 and M_2 to reduce the capacitance at the output node of the unit amplifier.

The Q-factor of the active inductor is given by:

$$Q = \frac{R_{eq}}{\mathrm{Im}\left[L_{eq}\right]} = \frac{1/g_{m4}}{2\pi f \cdot C_{g3}/\left(g_{m3} g_{m4}\right)} = \frac{g_{m3}}{2\pi C_{g3} \cdot f} \le \frac{f_{T3}}{f}\,. \tag{6.8}$$

It can be seen that the Q-factor decreases as frequency increases. At 915MHz, the Q is below 6.23 due to the 5.7GHz transit frequency of M_3. Furthermore, the 3dB bandwidth (i.e., f_{BW}) of the active inductor load is:

$$f_{BW} = f_C / Q \geq 915MHz / 6.23 = 147MHz, \tag{6.9}$$

which is wider than the 915MHz ISM band (902 – 928MHz).

A programmable current source is used to provide bias current for M_3 and M_4 so that the inductance and the center frequency of the amplifier can be adjusted via g_{m3} and g_{m4}. At resonance, the LC tank impedance is equal to R_{eq}. Therefore, the passband voltage gain of the amplifier is

$$G_{unit} = g_{m1} \cdot |Z_{IND}| = \frac{g_{m1}}{g_{m4}}, \tag{6.10}$$

where g_{m1} is the transconductance of M_1. To the first order, the gain of the unit cell is proportional to the bias current of the transconductor and the active inductor. To find out the actual gain of the amplifier, circuit simulation is needed. In each stage of the cascaded amplifier, M_1 is biased at 14μA, while the bias current of M_4 can be adjusted from 750nA to 3μA to tune the resonance frequency. An exception is made for the first stage, where the bias for M_1 is doubled to reduce the noise figure of the amplifier from 20dB to 17dB.

Figure 6-7 plots the simulated gain of each amplifier unit (including layout parasitics) with the 14μA nominal bias. The center frequency of each amplifier unit can be tuned from 710MHz to 1.1GHz, which is double the target frequency range (780MHz to 950MHz), leaving sufficient margin for all process corners, supply voltages between 0.9V and 1.1V and temperatures between -27˚C and 100˚C according to corner simulations. The 3-dB bandwidth is at least 300MHz when tuned to different frequencies. The passband gain varies between 13dB and 8dB with 14μA nominal current consumption when the center frequency is tuned from low to high. At higher frequencies, the passband gain is reduced since g_{m4} in (6.10) is increased at higher bias current in M_4.

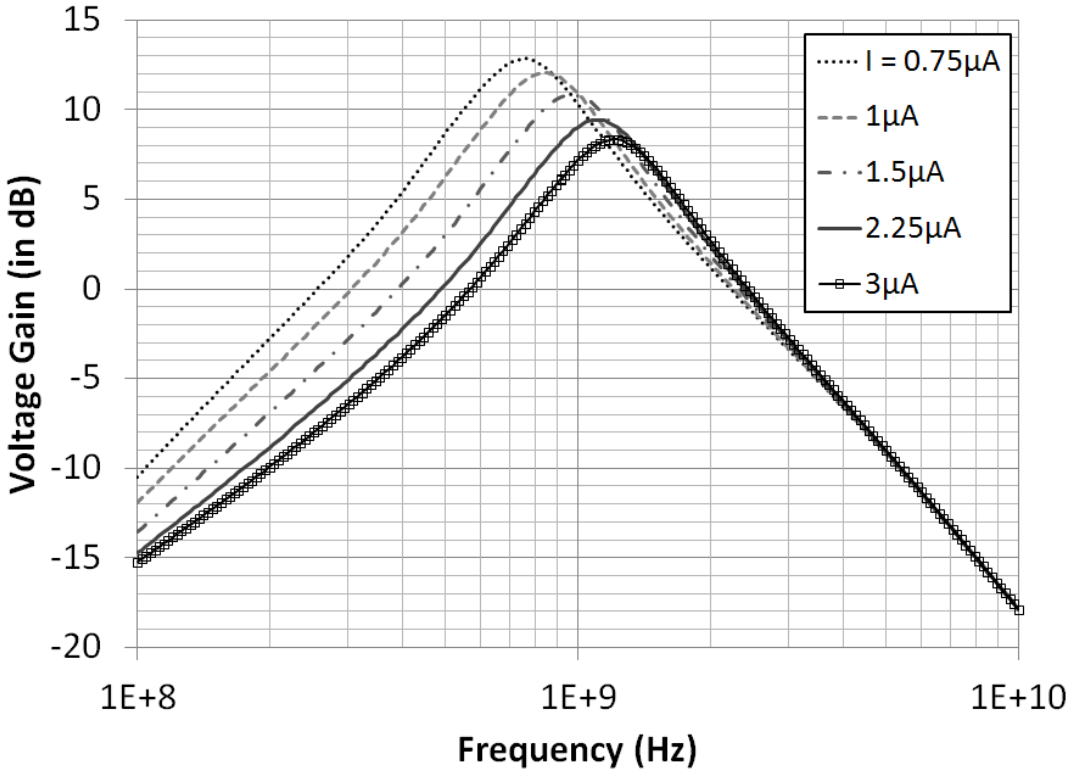


Figure 6-7: Simulated gain of an amplifier unit at different bias currents for the active inductor.

Since the active inductor requires approximately 200mV headroom, the output swing of the amplifier is limited compared to amplifiers with a passive inductor as the load. The output 1dB compression point of the unit amplifier is simulated to be 224mV peak-to-peak. The 5 gain settings must be utilized to extend the dynamic range of the RF front-end and avoid compression due to a strong desired signal or in-band interference. The automatic gain control (AGC) mechanism of this receiver is introduced in section 6.3.1.

The 5 RF signal paths achieve cascaded gains ranging from 23dB to 67dB (including 13dB passive voltage gain from the matching network) at corresponding bias current levels between 30 and 113µA. When tuned to 900MHz, the total simulated noise figure is between 16.7dB (maximum gain) and 17dB (minimum gain) for five signal paths, as the noise of each signal path is dominated by its input stage. The active inductor in the 1st stage contributes to 53% of the total noise, which is a combined result of low g_{m1} (below 0.5mS), shot noise in the transistors biased in weak-inversion, and low Q-factor of the active inductor. If better

sensitivity is required, more bias current can be added to increase g_{m1} at the cost of power consumption. Alternatively, an off-chip, high-Q inductor can be used instead of the active inductor for lower noise and higher gain, but with the penalty of system size and cost.

When operating in the synchronized-switching mode, the NMOS grounding switch at the amplifier input is driven by the CLK_{IF} signal. The CLK_{IF} with 50% duty-cycle is derived from the IF LO signal. In the 2-tone mode, the NMOS switch is kept open and does not affect the input signal.

6.2.2 Envelope Detector

The envelope detector is realized using the 2nd-order non-linearity of an NMOS transistor as shown in Figure 6-8. The single-ended output of the LNA is AC-coupled to the common-source NMOS transistor M_1. Biased in weak-inversion, the drain current of M_1 is exponentially related to the input voltage:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{V_{IN}+V_{Bias}}{nV_T}\right) = I_{Bias} \exp\left(\frac{V_{IN}}{nV_T}\right) = I_{Bias} + I_{Bias}\frac{V_{IN}}{nV_T} + \frac{I_{Bias}}{2}\left(\frac{V_{IN}}{nV_T}\right)^2 + \cdots, \tag{6.11}$$

where I_0 is the technology current [53] (similar to the saturation current in bipolar technologies), n is the subthreshold slope factor (typically between 1.3 and 1.4 in bulk CMOS biased in moderate inversion [53]), V_T is the thermal voltage, (26mV at room temperature), V_{Bias} is the DC bias voltage of M_1, and I_{Bias} is the DC bias current, which is equal to $I_0 \frac{W}{L} \exp\left(\frac{V_{Bias}}{nV_T}\right)$. The 2nd-order term in (6.11), i.e., $\frac{I_{Bias}}{2}\left(\frac{V_{IN}}{nV_T}\right)^2$, generates the baseband and intermodulation components from the square of the input signal, V_{IN}. The NMOS transistor M_3 is identical to M_1 to generate a replica reference (I_{Bias}), which is subtracted from (6.11) if the output of the envelope detector is taken differentially:

$$V_{OUT} = V_{OUT+} - V_{OUT-} = I_{Bias}R_L + \frac{I_{Bias}R_L}{2}\left(\frac{V_{IN}}{nV_T}\right)^2 - I_{Bias}R_L = \frac{I_{Bias}R_L}{2}\left(\frac{V_{IN}}{nV_T}\right)^2. \tag{6.12}$$

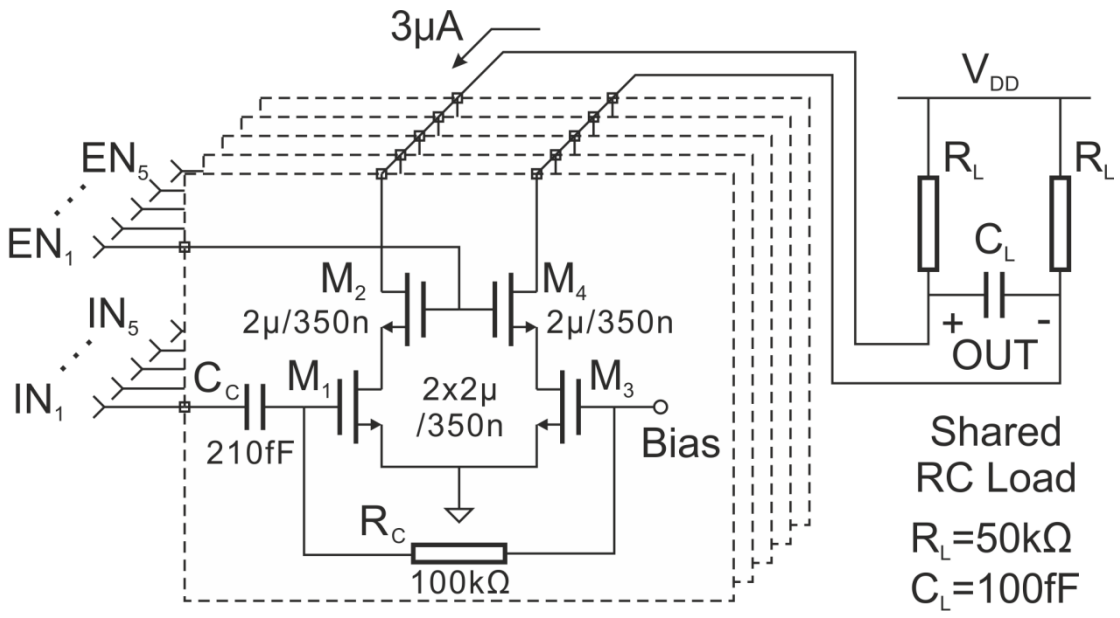


Figure 6-8: Schematic of the envelope detector (5 detector circuits in parallel with individual enable lines).

As shown in Figure 6-5, each LNA path is connected to one envelope detector. A pair of cascode transistors (i.e., M_2 and M_4 in Figure 6-8) connect M_1 and M_3 to the RC load shared by the five signal paths. One of the five signal paths is selected when the enable signal (i.e., $EN_1 \ldots EN_5$) at the cascode gates is switched to V_{DD}. When enabled, the envelope detector consumes 6μW.

6.2.3 IF and BB Stages

The IF AMP is shown in Figure 6-9. The input stage is a differential pair of NMOS transistors, with g_m programmed via the source-degeneration resistor, R_{DEG}. To realize a band-pass response, an active inductor is adopted for the load. Following the same analysis as in the LNA, the small-signal equivalent inductance is $\frac{C_F}{g_{m2}g_F}$, where C_F is the feedback capacitor, g_{m2} is the transconductance of M_2, and g_F is the feedback transconductance. The feedback transconductance is implemented with M_4 and M_5 as cascaded source followers, and g_F is approximately equal to the transconductance of M_5 (i.e., g_{m5}). Together with the load capacitance C_L, the load impedance of the filter peaks at $\frac{1}{2\pi\sqrt{\frac{C_F C_L}{g_{m5}g_{m2}}}}$, which is tuned to the receiver IF fre-

quency ($f_{IF,RX}$ = 8MHz, equal to the 2-tone separation). By programming R_{DEG}, the passband gain ranges from 15.5dB to 27.5dB with 7μA current consumption.

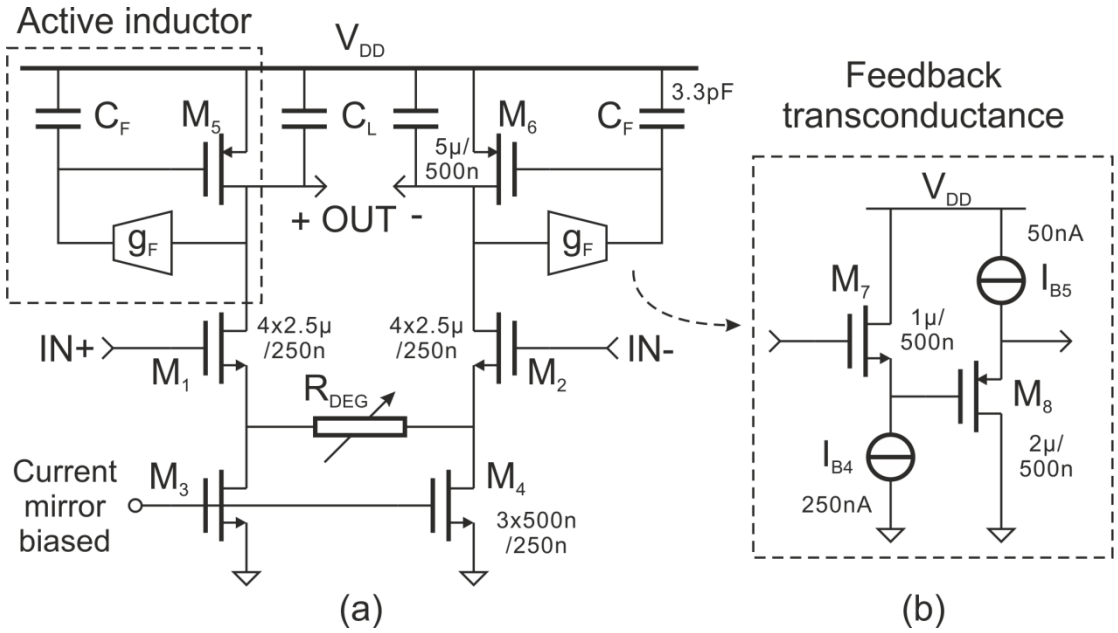


Figure 6-9: Schematic of the IF AMP.

The block diagram of the IF mixer and BB PGA is shown in Figure 6-10. The output of the IF AMP is downconverted to baseband via the IF mixer, and then low-pass filtered by the BB PGA. The BB PGA is implemented using two OPAMPs with programmable RC feedback networks. The gain of the amplifier can be set between 0 and 22dB by programming R_1, and its bandwidth can be adjusted between 10kHz and 100kHz by programming C_1 and C_2. To limit the chip area, a low-pass bandwidth below 10kHz is not implemented in the BB PGA. A digital LPF is used in the DBB to further limit the bandwidth of 1kbps signals. Each OPAMP consumes 7.5μA, resulting in 15μW total power consumption at 1V V_{DD}.

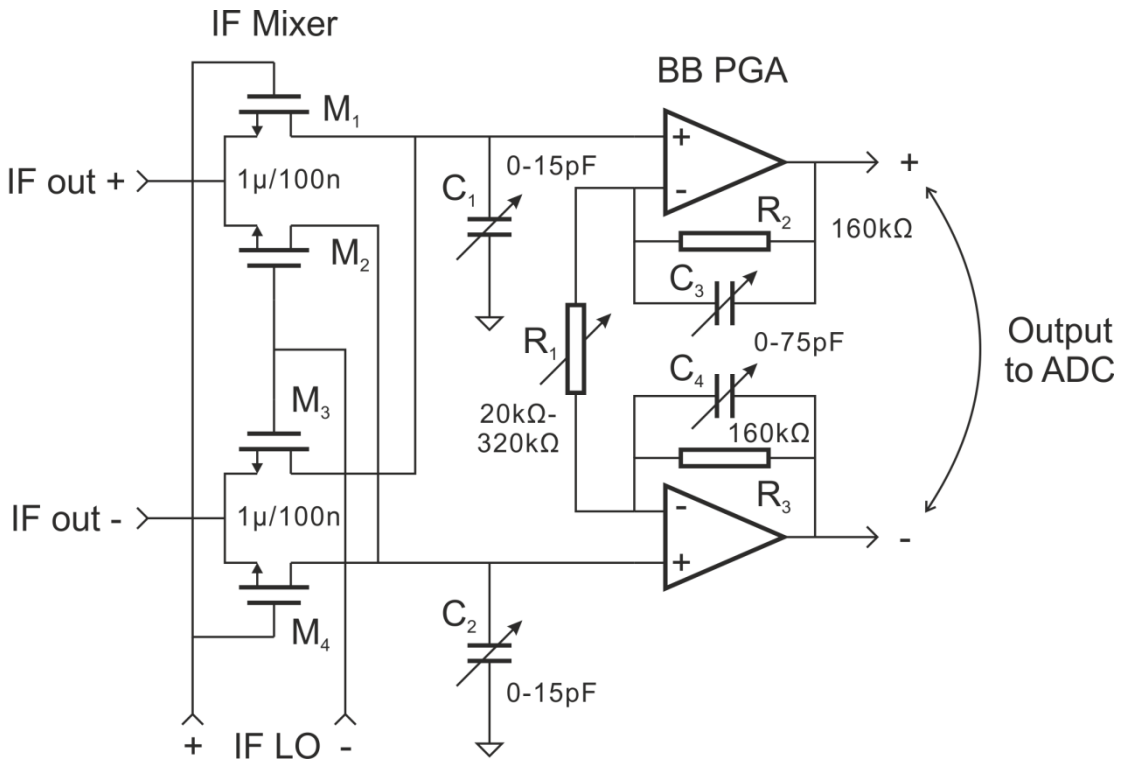


Figure 6-10: Block diagram of the IF mixer and BB PGA.

6.2.4 Analog-to-Digital Converter

An 8-bit successive-approximation register (SAR) ADC [115] is designed by Dr. Pieter Harpe from Eindhoven University of Technology and integrated with the receiver front-end to digitize the analog baseband signal for the DBB. The block diagram of the ADC is shown in Figure 6-11. The ADC is based on the charge redistribution principle, where a custom-designed switched-capacitor network implements the sample and hold (S/H), the feedback DAC and the summation node. Based on the output of the comparator, the asynchronous control logic performs an 8-bit binary-search to determine the digital output code. It achieves one of the best Walden figure-of-merit (FoM_W) [119] of 12fJ/conversion-step, which is calculated as:

$$FoM_W = \frac{P_{DC}}{2^{ENOB} \cdot \min\left(f_S, 2ERBW\right)}, \tag{6.12}$$

where P_{DC} is the power consumption, ENOB is the effective number of bits, f_S is the sampling frequency, and ERBW is the effective resolution bandwidth.

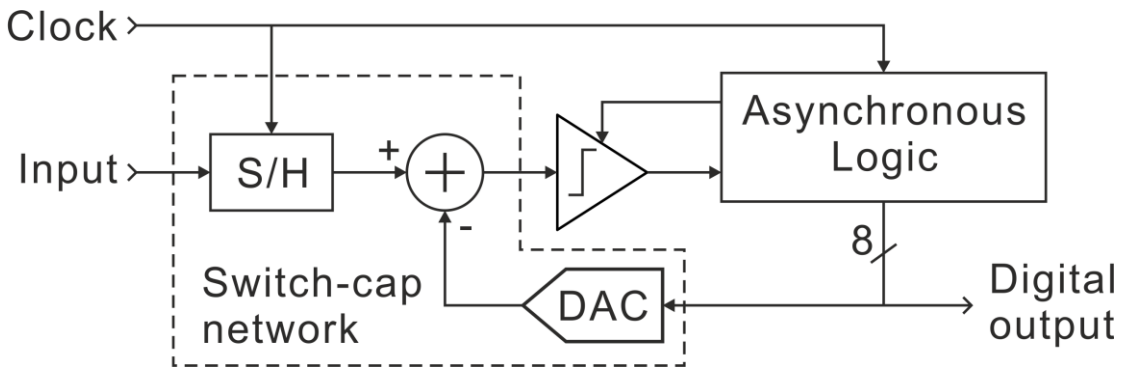


Figure 6-11: Block diagram of the 8-bit SAR ADC [115].

The ADC is able to operate up to 10MS/s, while in the receiver its sampling rate is fixed at 800kS/s for different data rates. At 800kS/s, the ADC consumes 2.1 μA under 1V power supply.

6.2.5 Receiver Sensitivity Estimation

The nonlinear noise analysis carried out in Chapter 4 is applied to this receiver to predict its RF sensitivity based on simulated parameters. The simulated receiver front-end parameters are shown in Table 6-1. The bandwidth of the BB PGA is set to 10kHz to receive a 10kbps OOK modulated signal. By referring to Figure 4-3, it can be seen that the self-mixed noise dominates the RF stage noise in this receiver as the LNA bandwidth is around 100MHz. Therefore, the impact of noise from the RF stages should be calculated using (4.17):

$$\begin{aligned} P_{MDS,N2} &= 2K_B T \cdot F_{FE} \cdot \sqrt{BW_{RF} \cdot BW_{BB} \cdot SNR_{MIN}} \\ &= 2 \times 3.981 \times 10^{-18} \times 50.1 \times \sqrt{100 \times 10^6 \cdot 10 \times 10^3 \cdot 12.6} \\ &= 1.416 \times 10^{-9} (mW) \\ &= -88.5 (dBm) \end{aligned} \quad (6.13)$$

Due to the synchronized-switching operation, there will be a 3dB sensitivity penalty compared to a conventional envelope detection receiver. As a result, when the baseband noise is ignored, the receiver should achieve -85.5dBm sensitivity for all RF gain settings in synchronized-switching mode.

To assess the impact of baseband noise, (4.26) is used:

$$P_{MDS,BB} = \frac{20\sqrt{v_{n,eq}^2 \cdot SNR_{MIN}}}{kA_V^2} = \frac{71\sqrt{PSD_0 \cdot BW_{BB}}}{kA_V^2}$$
$$= \frac{71\sqrt{6.63\times10^{-14}\times10\times10^3}}{27.7\times A_V^2} \qquad (6.14)$$
$$= \begin{cases} -64(dBm), & \text{for 1X LNA gain path;} \\ -75(dBm), & \text{for 2X LNA gain path;} \\ -86(dBm), & \text{for 3X LNA gain path;} \\ -97(dBm), & \text{for 4X LNA gain path;} \\ -108(dBm), & \text{for 5X LNA gain path.} \end{cases}$$

Thanks to the synchronized-switching operation, 1/f noise can be ignored, but 3dB penalty should be added to the sensitivity found in (6.14). When all noise sources in the receiver are taken into account, the estimated sensitivities for 10kbps OOK reception in synchronized-switching mode are listed in Table 6-2. Note that the estimation does not yet include the loss (around 2 to 3dB) from the surface acoustic wave (SAW) preselect filter at the receiver input.

Table 6-1: Simulated front-end parameters at 10kbps

LNA gain path		1X	2X	3X	4X	5X
LNA gain (dB)	A_V	23	34	45	56	67
LNA noise figure (dB)	NF_{FE}	17				
LNA noise factor	F_{FE}	50.1				
LNA bandwidth (Hz)	BW_{RF}	100M				
Envelope detector scaling factor (V^{-1})	k	27.7				
Baseband thermal noise floor (V^2/Hz)	PSD_0	6.63×10^{-14}				
Baseband bandwidth (Hz)	BW_{BB}	10k				

Table 6-2: Sensitivity prediction for synchronized-switching OOK reception (without SAW preselect filter loss).

LNA gain path		1X	2X	3X	4X	5X
Sensitivity at different data rates (dBm)	1kbps	-66	-76.8	-86.5	-89.9	-90.5
	10kbps	-61	-71.8	-81.1	-84.9	-85.5
	100kbps	-56	66.8	-76.1	-79.9	-80.5

The sensitivity estimation for 10kbps can be readily extended to other data rates. Note that the sensitivity ($P_{MDS,RF}$ or $P_{MDS,BB}$) is proportional to the square root of baseband bandwidth (BW_{BB}) in both (6.13) and (6.14). Consequently, for each factor of 10 scaling of data rate (assuming BW_{BB} scales accordingly), the sensitivity should be scaled by 5dB. The resulting sensitivity predictions for different data rates are also listed in Table 6-2. Though the LNA gain path with 5 cascaded amplifiers brings virtually no sensitivity improvement compared to the path with 4 cascaded amplifiers, it is still implemented as a reference to verify the sensitivity estimation.

6.3 System Implementation

The event-driven receiver front-end is implemented in the same 90nm CMOS technology as the transmitter front-end in Chapter 5. The digital baseband for both 2-tone and conventional OOK modes is implemented in a commercial FPGA platform for flexibility.

The CMOS chip is wire-bonded to a quad flatpack no-lead (QFN) package with 56 pins. A serial peripheral interface (SPI) bus and internal digital registers are integrated as the digital interface to control the operation of the receiver. Figure 6-12 shows the chip micrograph, where the active circuitry occupies 1.27mm^2. On the printed circuit board (PCB) where the packaged chip is mounted, an external SAW filter can be connected to the RF input to suppress out-of-band interference.

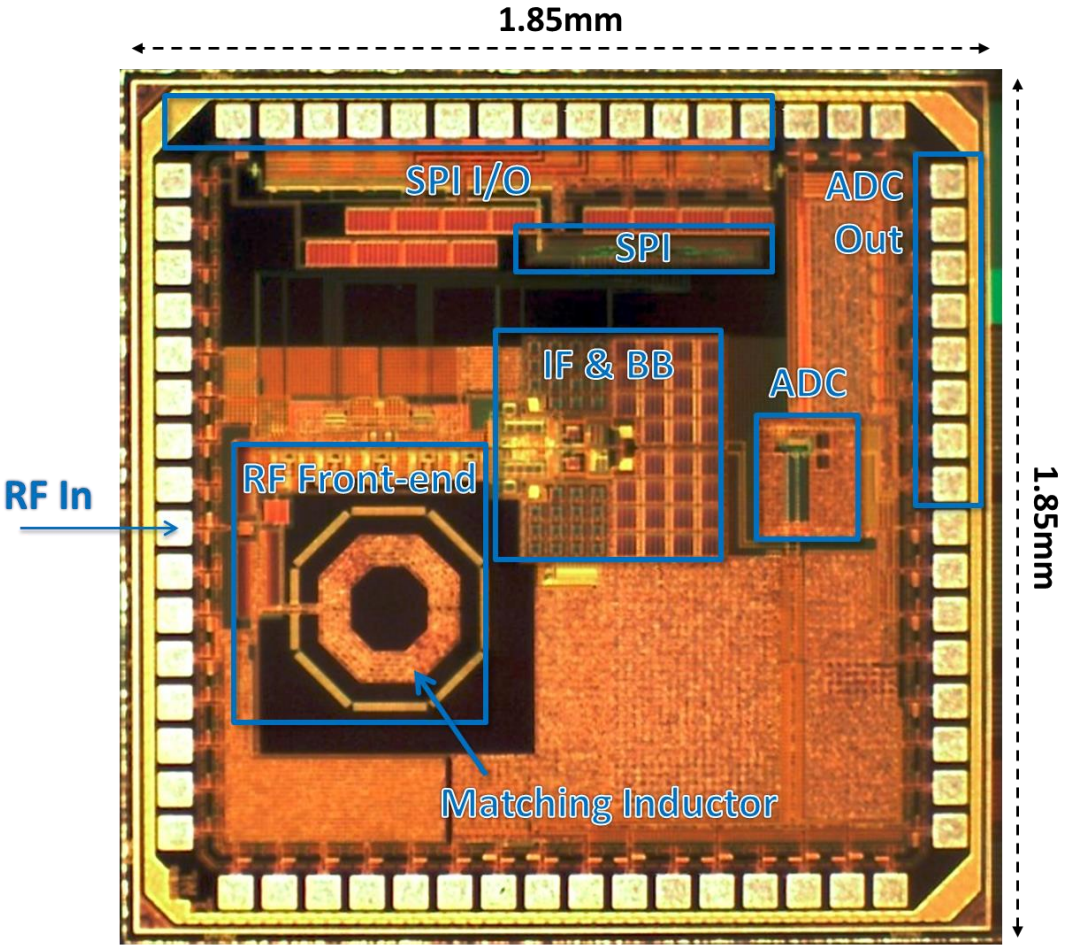


Figure 6-12: Chip micrograph of the 2-tone event-driven receiver front-end.

6.3.1 Digital Baseband in 2-tone Mode

When operating in the 2-tone mode, the output signal of the ADC is at low-IF instead of DC, as discussed in section 6.1.2. For different data rates, the choices of low-IF and BB PGA cut-off frequency (f_C), as well as ADC sampling rate (f_S) are listed in Table 6-3. For 10kbps and 100kbps reception, the low-IF is chosen at 5kHz and 50kHz, while the BB PGA f_C is set to 10kHz and 100kHz, respectively. For 1kbps data rate, as the minimal f_C of the BB PGA is 10kHz, the 5kHz low-IF is maintained. To reduce the complexity in clock generation and DBB design, the ADC f_S is fixed at 800kS/s for all data rates, so that the over-sampling ratio (OSR) is 800, 80 and 8 for 1kbps, 10kbps and 100kbps, respectively. The lowest OSR of 8 is already sufficient to capture the baseband symbols accurately.

Table 6-3: 2-tone baseband parameters for different data rate.

Data rate (kbps)	Low-IF (kHz)	BB PGA f_C (kHz)	ADC f_S (kSps)	ADC OSR
1	5	10	800	800
10	5	10	800	80
100	50	100	800	8

Prior to 2-tone IF-PSK demodulation, the digital baseband needs to downconvert the low-IF signal to DC, and reduce the OSR to 1. In addition, the received signal strength indication (RSSI) needs to be obtained, so that the LNA and BB PGA gains can be set accordingly. Figure 6-13 shows the 2-tone receiver DBB implemented on FPGA. The ADC samples are downconverted to DC, and low-pass filtered using a finite impulse response (FIR) filter. The FIR filter cuts the noise and interference at frequencies beyond the signal bandwidth, while it also reduces the OSR to 8 by down-sampling the 1kbps and 10kbps signals. The resulting I/Q digital baseband signal is provided to a decimation and RSSI estimation module, which reduces the OSR to 1 for demodulation, and provide RSSI for automatic gain control (AGC) of the Rx front-end.

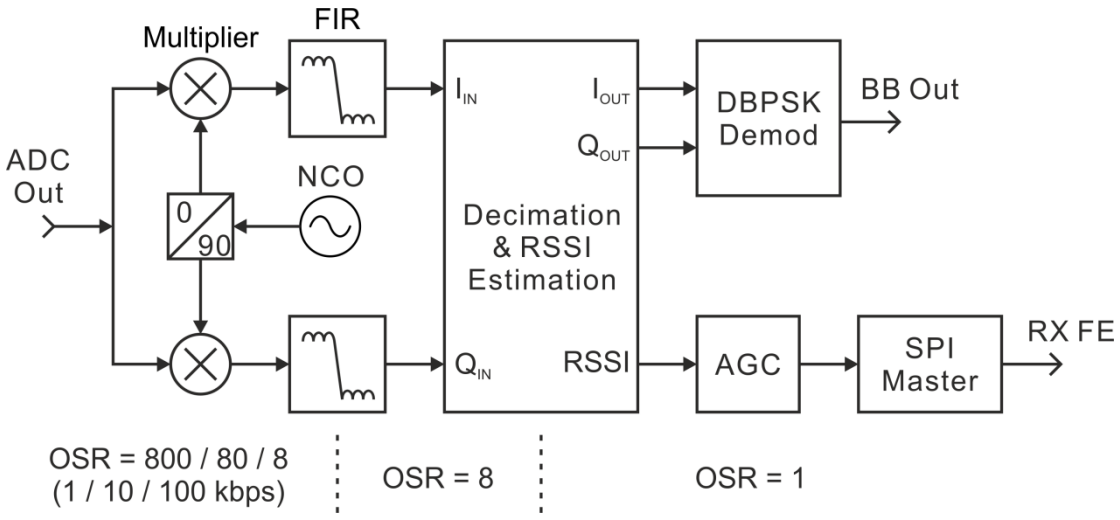


Figure 6-13: Block diagram of the Rx digital baseband for 2-tone IF-PSK reception.

The operation of the decimation and RSSI estimation module is shown in Figure 6-14. The oversampled I_{IN} and Q_{IN} signals are firstly delayed by N samples, where N can be con-

trolled from 0 to 7. The resulting signals are provided to a delay and RSSI estimator in both the in-phase and the quadrature signal paths. Meanwhile, a down-sampling block takes one sample out of each 8 I or Q samples at a predefined position, in this case the 4th sample. The delay estimator calculates the time delay of the ADC samples in both paths, and the path with the stronger signal (i.e., larger RSSI) is used to control the delay-line. The delay control block compares the estimated delay with a setpoint, and adjusts the variable delay so that the 4th sample is the optimal sample after settling.

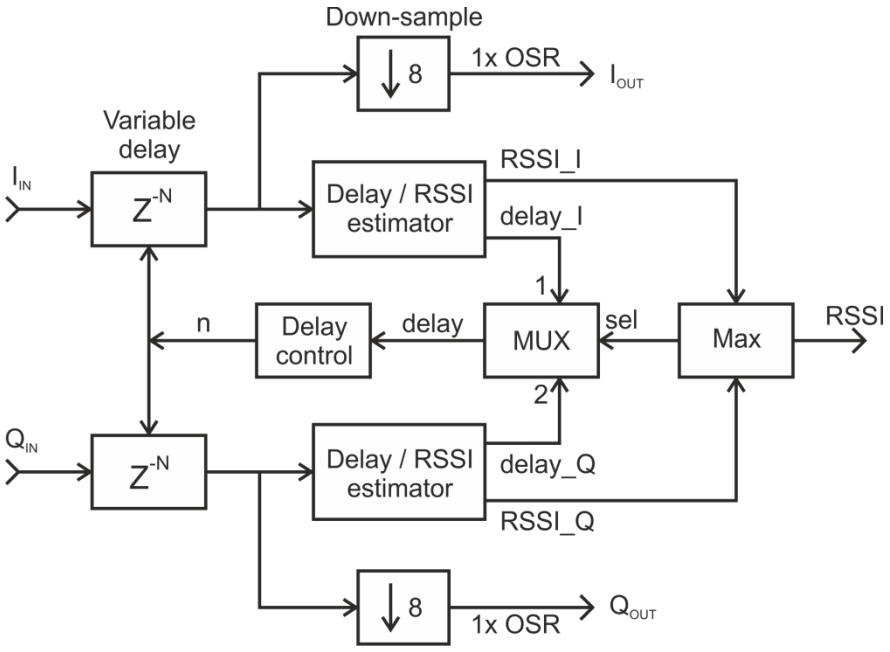


Figure 6-14: Block diagram of the decimation and RSSI estimation module in 2-tone mode.

The operation of the delay / RSSI estimator is shown in Figure 6-15. It takes snapshots of 16 consecutive samples (i.e., 2 bit-periods) with 8 samples (1 bit) of overlap to estimate the signal delay and RSSI. The RSSI is computed as the difference between the maximal and minimal levels in one snapshot. The positions of the minimal and maximal samples are also taken, and their median is calculated as the delay. Since accurate estimations require zero-crossing of samples, snapshots without zero-crossing are disregarded, and the previous estimation is maintained.

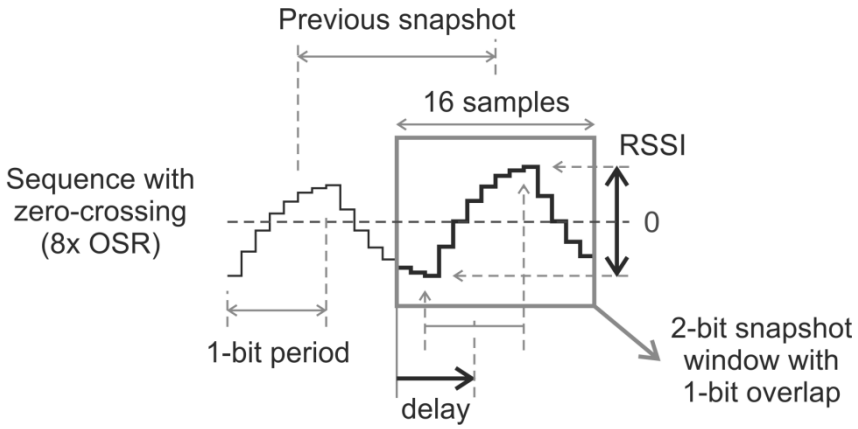


Figure 6-15: Snapshot Delay / RSSI estimation in 2-tone mode.

The larger RSSI readout from the I/Q paths is compared to the desired signal level (RSSI setpoint) in the automatic gain control (AGC) block, which adjusts the front-end gain accordingly. The baseband gain is adjusted in 6dB steps in the BB PGA, while the RF gain is adjusted in 10dB / step, which is equivalent to 20dB / step at the IF and BB stages due to squaring.

The down-sampled I_{OUT} and Q_{OUT} signals are used for demodulation. Since the Rx IF and BB signal is BPSK modulated, the demodulator has to cope with phase ambiguity due to an arbitrary phase-shift between the transmitter and receiver [88]. To solve this problem without using complex algorithms, differential encoding is adopted in the transmitter, so that the baseband information is presented in the phase change between symbols, instead of their arbitrary phase. In addition, differential BPSK (DBPSK) greatly simplifies the demodulator implementation, since a non-coherent demodulator shown in Figure 6-16 can be used without recovering the phase of the carrier [88]. Furthermore, the non-coherent DBPSK demodulator is resilient to the carrier frequency offset (in this receiver the IF LO offset); thus there is no need to estimate, track or compensate the phase rotation in the Rx DBB.

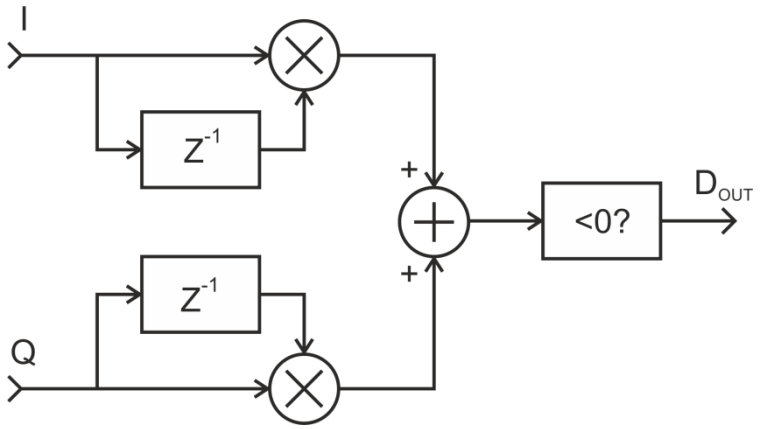


Figure 6-16: Non-coherent DBPSK demodulator in the Rx DBB.

6.3.2 Digital Baseband in OOK Mode

The block diagram of the proposed OOK DBB is shown in Figure 6-17. Similar to the 2-tone DBB, the ADC sampling rate is fixed at 800kS/s for all data rates. The samples are low-pass filtered using an FIR, which also down-samples the 1kbps and 10kbps signals to reduce the OSR to 8. After filtering, the samples pass through a variable delay-line, which is controlled by the estimated delay from a delay / RSSI estimator. The output of the delay is down-sampled to OSR = 1 and compared to a threshold for OOK demodulation. The delay / RSSI estimator shown in Figure 6-18 is similar to the one used in the 2-tone DBB. In addition to calculating the RSSI and delay for each snapshot of two consecutive bits, the mean value of the samples is also calculated. The mean is provided to a moving average (MA) block which generates the de-modulation threshold. The AGC module functions the same way as in the 2-tone DBB.

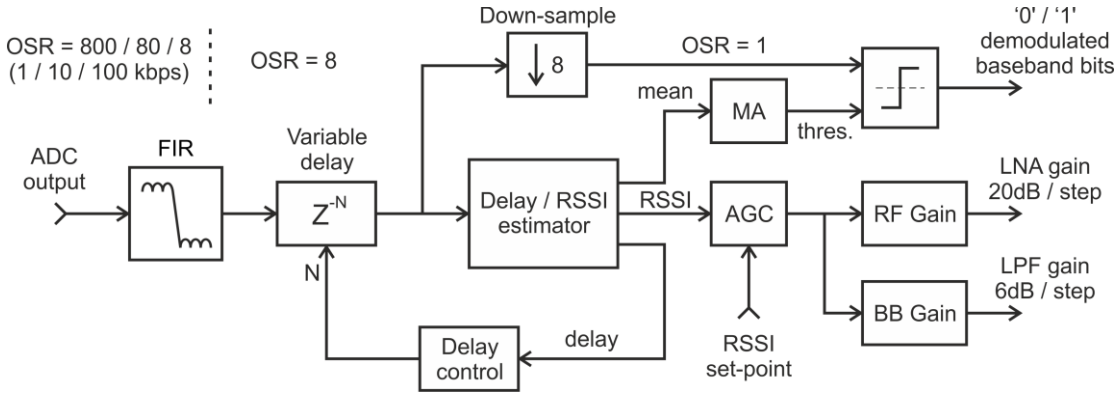


Figure 6-17: Block diagram of Rx digital baseband in OOK mode.

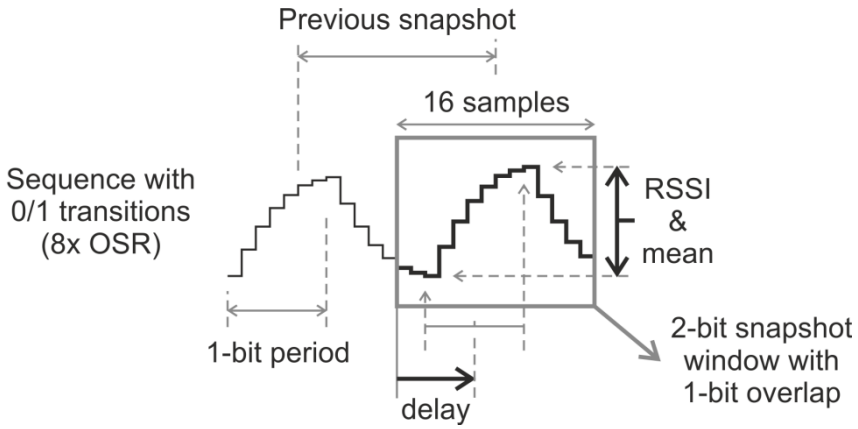


Figure 6-18: Snapshot delay / RSSI estimation in OOK mode.

Similar to the 2-tone DBB, the operation of the RSSI / delay estimator relies on transitions between 0 and 1 in the baseband data. As the mean and threshold is dependent on the signal amplitude, demodulation is only possible after the AGC loop settles. Consequently, a preamble sequence of alternating 0s and 1s is required so that the AGC, threshold, and delay control loop can converge before any random payload is demodulated. Note that this restriction does not apply to the 2-tone receiver, since the DBPSK demodulator shown in Figure 6-16 does not dependent on the amplitude of the I/Q baseband signal. This is another benefit of the 2-tone IF-PSK modulation over the conventional OOK modulation.

6.4 Evaluation Results

The evaluation of the event-driven receiver focuses on the sensitivity and selectivity of the receiver, which is presented in this section.

6.4.1 Input matching

To measure the input matching network, the receiver input is connected directly to a network analyzer without a SAW preselect filter mounted. The receiver is operating in the 2-tone mode so that the input synchronized-switching switch is not operating. The center frequency of the matching network can be programmed from 780MHz to 950MHz without external matching components. As show in Figure 6-19, better than -20dB S_{11} can be achieved in each band of

interest. Among 10 measured samples from the same wafer, the digital control signals for the matching network do not need to be readjusted to achieve the same S_{11}.

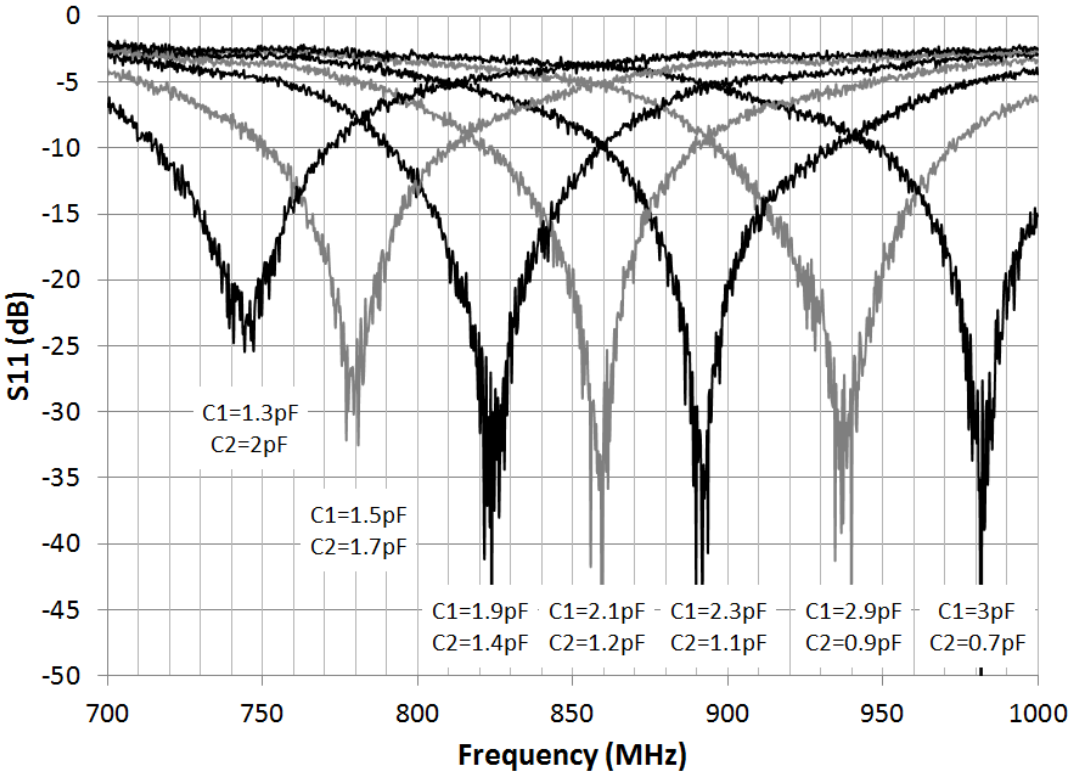


Figure 6-19: Measured input return loss under different settings.

6.4.2 Sensitivity

The sensitivity of the receiver is measured at different carrier frequencies without the SAW preselect filter, which represents the intrinsic performance of the receiver. Firstly, performance at 915MHz carrier frequency is measured. An OOK signal modulated by alternating 0s and 1s is provided to the receiver to measure the sensitivity in the synchronized-switching mode. Different RF signal chains of 1 to 5 LNA stages (1X AMP to 5X AMP) are used in the measurement, and the sensitivity measured at 10^{-3} bit-error-rate (BER) is listed in Table 6-4. The sensitivity improves as the data rate reduces, or when more gain stages are cascaded as predicted in section 6.2.5. Sensitivity up to -89.5dBm is achieved at 1kbps with 4X AMP RF chain. For 10kbps and 100kbps, the highest sensitivity is -86.5dBm and -81.5dBm, achieved with 5X and 4X AMP RF chains, respectively. The power consumption of the receiver front-end at

different sensitivity levels is also listed in Table 6-4. The receiver dissipates from 63.5μW to 146μW depending on the number of active LNA stages. The power consumption of the IF LO, which is not included on-chip, can be as low as 10μW if a crystal oscillator is integrated together with the front-end [107].

Table 6-4: Measured sensitivity and power consumption at different data rates.

Data rate (kbps)	**Measured Sensitivity**				
	1X AMP	2X AMP	3X AMP	4X AMP	5X AMP
1	-64.5	-70	-80.5	-89.5	-89
10	-61	-68.5	-79.5	-86	-86.5
100	-55.5	-62	-74	-81.5	-81.5
Power consumption* (μW)	63.5	83.5	102	121	146

* including on-chip Rx front-end, excluding DBB and IF LO generation.

The measured sensitivity at 10kbps is plotted together with the prediction from Table 6-2 in Figure 6-20. The receiver is also simulated using Cadence® SpectreRF™ periodic steady state (PSS) and periodic noise (Pnoise) analyses. In such simulations, noise is regarded as a small signal so noise self-mixing cannot be captured. Since the noise self-mixing during envelope detection dominates the RF front-end noise level, the simulation does not predict the sensitivity accurately in the high gain modes. By contrast, the measured sensitivities are close to the prediction from Table 6-2. The mismatch in the low-gain modes may be attributed to the RF gain variation between simulation and implementation. Post-layout Monte Carlo simulation using 100 samples shows a standard-deviation in LNA gain of 1.8dB, which translates to 3.6dB sensitivity deviation when the Rx sensitivity is limited by the baseband noise (i.e., RF chains with 1 to 3 stage LNA cascaded) according to (6.14). The standard-deviation for LNA noise figure is 0.73dB, which results in 0.73dB sensitivity deviation when the Rx sensitivity is limited by the RF noise (i.e., RF chains with 4 and 5 stage LNA cascaded) according to (6.13).

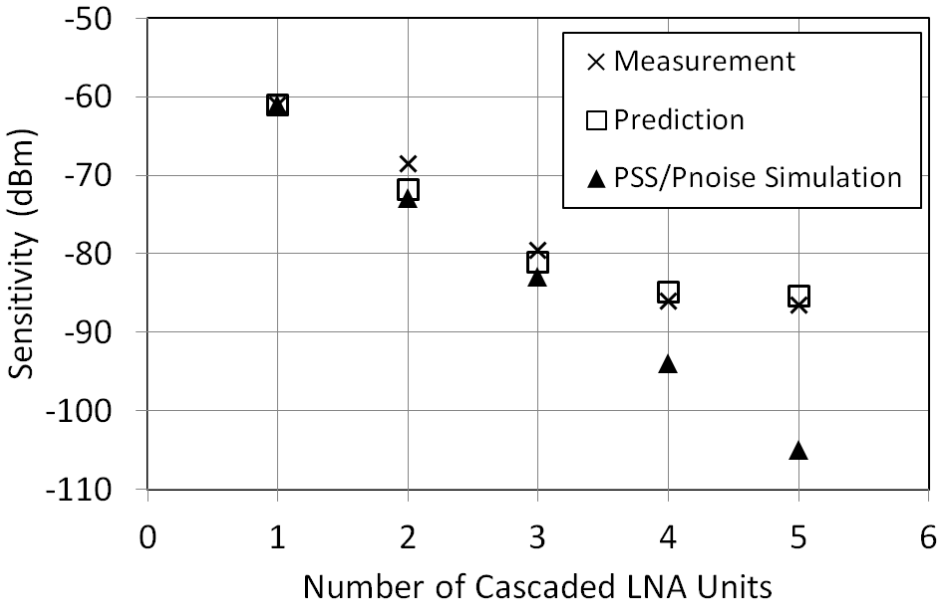


Figure 6-20: Comparison of measured, predicted and simulated sensitivity at 10kbps.

By comparing Table 6-4 and Table 6-2, it can be seen that the measured sensitivity at 1kbps is poorer than prediction, especially with low RF gain paths. It was discovered that the quantization noise floor of the ADC becomes the limiting factor when the input signal is weak and the Rx gain is low (less than 4 LNA stages in the RF front-end). To overcome this problem and to achieve scalable sensitivity at different data rates, the baseband stages should be redesigned with higher gain, which would not increase the overall power consumption significantly due to the low baseband frequency (i.e., less than 1MHz).

The receiver was also programmed to other carrier bands, including 780MHz, 868MHz and 950MHz. Similar sensitivities have been measured, except for the 950MHz band, where approximately 1dB degradation is observed. When operating in the 2-tone mode, the measured receiver sensitivities are similar to the OOK mode.

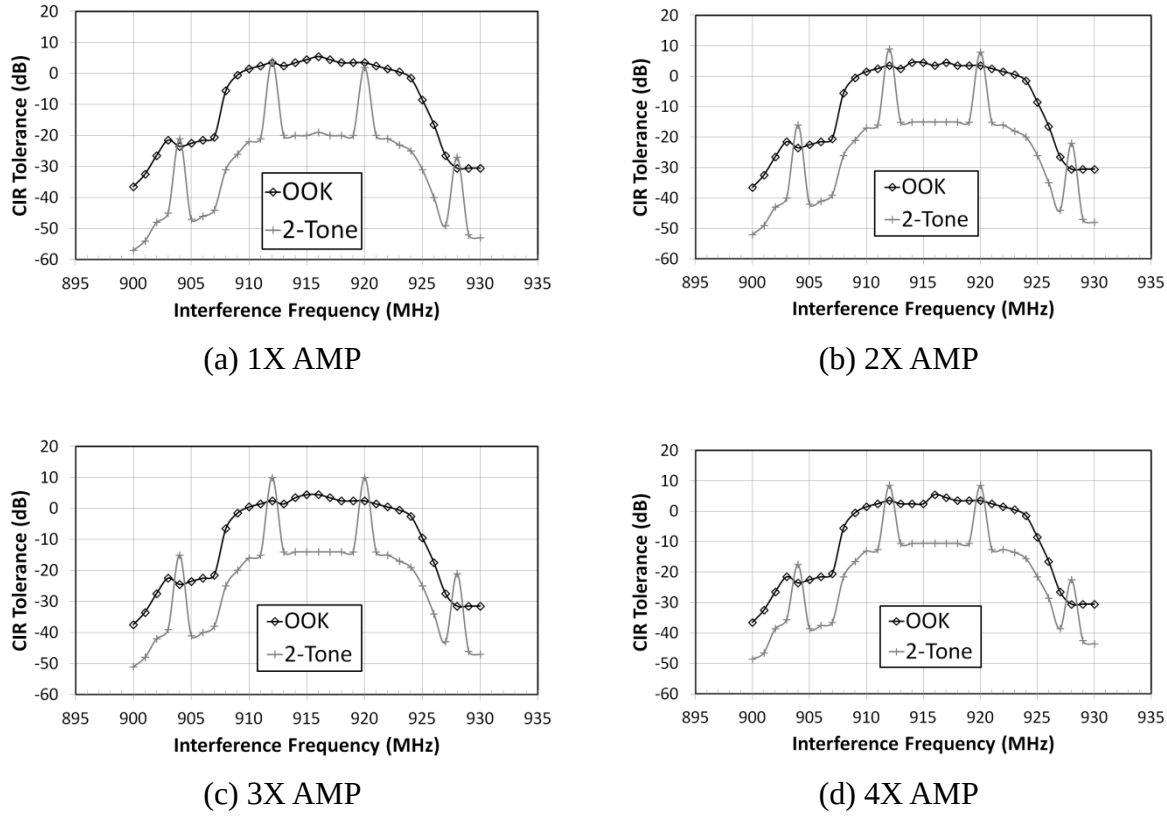
When a SAW filter is mounted at the receiver input to improve out-of-band interference rejection, the measured Rx sensitivities are degraded by around 3dB compared to the intrinsic Rx sensitivities shown in Table 6-4 due to the filter insertion loss.

6.4.3 Interference rejection

The receive selectivity is measured in the 915MHz band with a SAW preselect filter [117] mounted to reject out-of-band interference in both the OOK and the 2-tone mode. The 2-tone event-driven transmitter designed in Chapter 5 is connected to the receiver via a programmable attenuator. The input signal to the receiver is 3dB above the sensitivity level in each gain modes (between -58dBm and -83dBm, 3dB higher than Table 6-4 due to SAW filter loss), and the data rate is 10kbps. In the OOK mode, the desired signal is centered at 915MHz, while in the 2-tone mode, the two carrier tones are located at 912MHz and 920MHz. A randomized OOK interferer at 10kbps is added in-band. The selectivity is measured at different RF signal paths and plotted in Figure 6-21. For the OOK mode, the selectivity follows the frequency response of the SAW filter, and in the passband of the SAW filter the desired signal needs to be several dB higher than the interferer to ensure a BER below 10^{-3}. Better in-band interference rejection is achieved in the 2-tone mode. At minimum gain, the receiver tolerates -19dB in-band carrier-to-interference ratio (CIR) in the 2-tone mode, while conventional OOK requires up to 5.5dB CIR. At the highest sensitivity levels (i.e. 4 LNA stages cascaded), 16dB improvement is obtained from the 2-tone mode over the OOK mode. A comparison of the in-band interference rejection between the OOK and the 2-tone mode is summarized in Table 6-5.

Table 6-5: Measured in-band interference tolerance at different RF signal paths (10kbps data rate)

Cascaded LNA Stages	**In-band CIR Tolerance (dB)**		**Improvement (dB)**
	OOK	2-tone	
1X AMP	5.5	-19	24.5
2X AMP	4.5	-15	19.6
3X AMP	4.5	-14	18.5
4X AMP	5.5	-10.5	16



(a) 1X AMP (b) 2X AMP

(c) 3X AMP (d) 4X AMP

Figure 6-21: Measured interference tolerance at different LNA gain settings (10kbps data rate).

As expected, when the interferer is 8MHz (Δf) away from either carrier tones (i.e., 904/912/920/928MHz), the interference has a more significant impact in 2-tone mode. To alleviate this problem, the 2 carrier tones can be shifted by controlling the Tx DCO to avoid interferers at particular frequencies such as this.

It is also shown in Table 6-5 that as the RF gain increases, the interference rejection in the 2-tone mode degrades gradually. This is due to the fact that the linearity of the RF LNA is poor due to the use of multiple amplifier stages and the active inductor load. The strong interference incurs gain compression in the RF amplifiers [108], which reduces the level of the desired signal and degrades the SNR at the receiver baseband. If better interference rejection is required, the linearity of the RF front-end should be improved, which can be achieved in different ways. For example, a higher supply voltage can be used so that the headroom for signal swing increases. On the other hand, the active inductors can be replaced by passive

inductors at the later amplifier stages to accommodate larger signal swing without using a higher supply voltage. However, compromises in higher power consumption, larger chip area, or higher cost should be expected.

6.4.4 Power consumption analysis

Figure 6-22 shows the power consumption breakdown of the event-driven receiver front-end with the 4X AMP signal path. It supports both 2-tone IF-PSK and OOK modes, and achieves -89.5dBm sensitivity at 1kbps while dissipating 121 µW. The power consumption scales dynamically with the input signal level from as low as 63.5 µW via the AGC loop. As expected, the majority of the power is spent on the RF front-end, including 74% in the RF amplifiers and 5% in the envelope detector. This front-end needs to achieve high gain and low noise to meet the sensitivity requirements of generic event-driven applications, and therefore demands the most power.

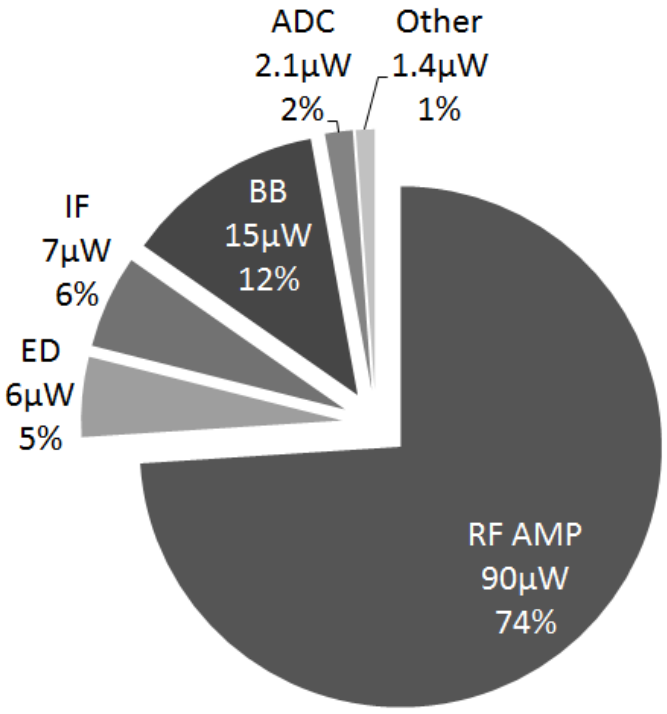


Figure 6-22: Power consumption breakdown of the Rx front-end with 4-stage cascaded LNA (excluding IF LO and DBB).

6.5 Conclusion

An ultra-low-power event-driven Rx front-end is designed to support the proposed 2-tone modulation scheme proposed in Chapter 5. The implemented receiver maintains the low-complexity and power consumption of conventional envelope detection receivers, while achieving up to 282 times (24.5dB) better in-band interference rejection. The receiver front-end dissipates from 63.5 µW to 121 µW depending on the input signal level, with the highest sensitivity of -86dBm at 10kbps (-89.5dBm and -81.5dBm at 1kbps and 100kbps, respectively). In addition, a low-complexity digital baseband has been proposed and implemented on an FPGA platform to demodulate 2-tone IF-PSK modulated signal with differential encoding.

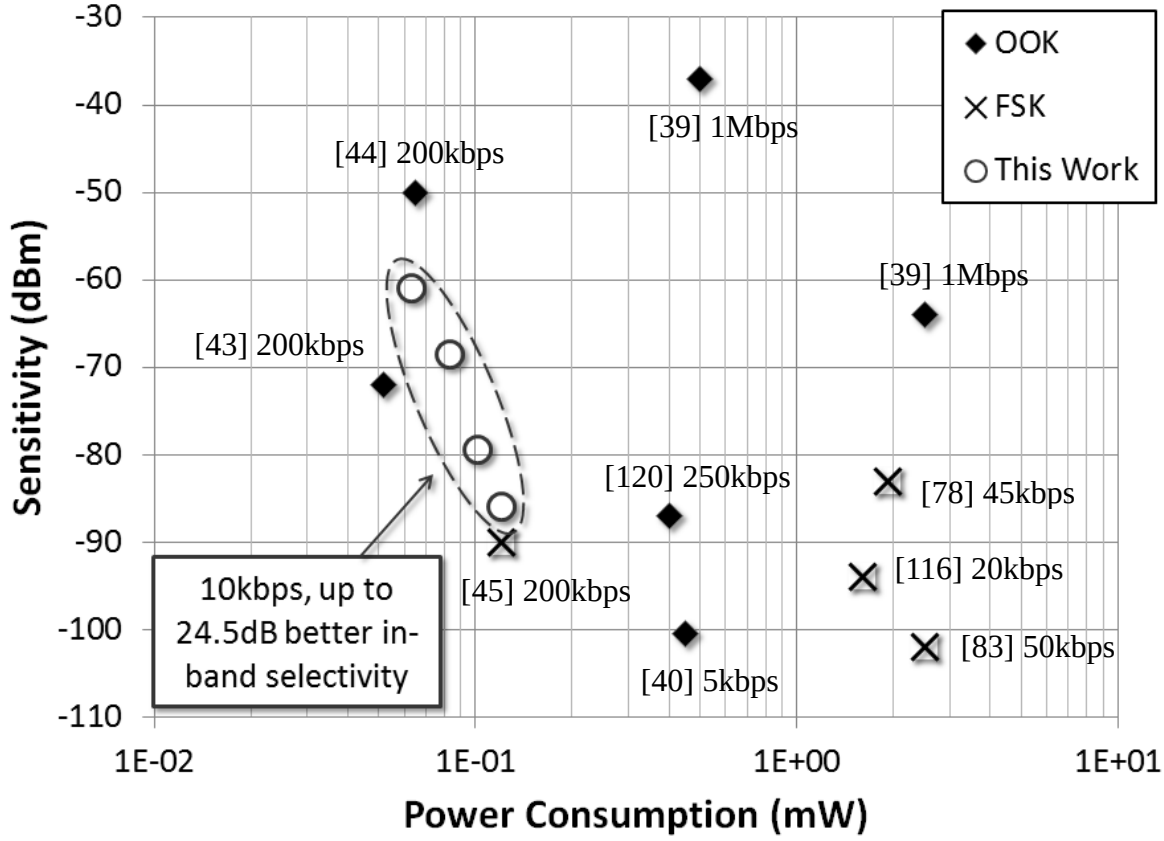


Figure 6-23: Comparison to state-of-the-art ultra-low-power receivers.

In Figure 6-23, the 2-tone envelope detection receiver is compared with the state-of-the-art low-power receivers surveyed in Figure 1-7. This receiver achieves the state-of-the-art power consumption and sensitivity, which are also scalable for various event-driven radio applications. When the data rate of this receiver is increased to 100kbps, its sensitivity will be degraded by approximately 5dB. On the other hand, for applications requiring lower data rate, this receiver can operate at 1kbps with up to -89.5dBm sensitivity. Most importantly, the receiver verifies the proposed 2-tone envelope detection scheme, which is capable of rejecting in-band interference. By contrast, all state-of-the-art OOK receivers targeting similar performance and power budget lack in-band frequency selectivity, making them vulnerable to interference in practical applications.

Chapter 7

Conclusions and Recommendations

In the final chapter of this thesis, the scope and depth of the research work is revisited, and its scientific contributions are highlighted. Suggestions for future research in the area of event-driven radio research are outlined.

7.1 Summary

The notion of ubiquitous communication, sensing and signal processing promises mankind a wonderful future of better life quality, productivity and security. Among various technological challenges, this work has focused on ultra-low-power event-driven radio, which serves as an autonomous wireless communication interface for applications such as healthcare, information and entertainment, industrial and home automation, as well as environment monitoring.

The thesis started with the definition and analysis of wireless event-driven applications, and then the available technology platforms and state-of-the-art in radio transceivers were reviewed in the first two chapters. The most difficult challenges recognized are: 1) to realize a radio transceiver with a power budget around 100μW while 2) achieving sufficient performance for practical application scenarios, including a link budget of more than 80dB, data rates up to 100kbps, and the ability to reject both out-of-band and in-band interferers.

Two proof-of-concept radio front-ends were designed in Chapter 3 to verify the architectural choice of the direct-modulation transmitter and the envelope detection receiver. The Tx front-end delivers pulse-shaped OOK output at -3dBm, while dissipating 2.31mW. The Rx

front-end achieves -80dBm sensitivity at 51 μW thanks to the proposed synchronized switching technique.

In Chapter 4, the sensitivity and selectivity of envelope detection radios were analyzed, aiming at improving the performance of the radios. A novel 2-tone signaling technique was proposed to reject in-band interference in envelope detection radios. In Chapter 5 and Chapter 6, a prototype radio transmitter and receiver were designed to benchmark the performance of 2-tone envelope detection in practice. The digital-IF, direct-modulation transmitter carries out the 2-tone IF-PSK modulation with -6dBm output power while consuming 893 μW. The 2-tone envelope detection receiver realized up to 282 times improvement in interference rejection while dissipating between 63.5 μW and 121 μW. A link budget of over 80dB is realized by this transceiver pair, which translates to a link span up to 30 meters in indoor environments and 100 meters outdoors. The challenges in performance and power consumption identified at the beginning of this thesis have been addressed by these circuits.

7.2 List of Contributions

The theoretical analysis, circuit and system design, as well as the transceiver implementations presented in this thesis have advanced the state-of-the-art substantially in multiple aspects. The most significant scientific contributions of this work are summarized as follows:

1. The synchronized-switching envelope detection technique proposed and implemented in Chapter 3 improves the sensitivity of envelope detection receivers by suppressing 1/f noise. Such enhancement can extend the range of a low-power radio with little penalty in power consumption, chip area or complexity.
2. The 2-tone envelope detection technique proposed in Chapter 4 introduced in-band frequency selectivity for envelope detection receivers for the first time. It is a completely new signaling technique which greatly improves the robustness of envelope

detection radios in practical environments. As verified by the prototype radios described in Chapter 5 and 6, the proposed technique can be implemented using low-complexity and low-power circuits.

3. Despite being widely used in ultra-low-power radios, the sensitivity of envelope detection receivers has been difficult to simulate or predict due to the nonlinear operation of the detector. The system-level analysis carried out in Chapter 4 started from the circuit design point of view, and provided an analytical model that predicts the sensitivity of such receivers. The synchronized-switching envelope detection receiver was also analyzed, and the sensitivity predictions matched the measurement results in Chapter 6.
4. Again in Chapter 4, guidelines for optimizing receiver sensitivity have been obtained based on the insight from a system-level noise analysis.
5. Radio front-ends and low-complexity digital baseband for 2-tone IF-PSK modulation and demodulation have been proposed and verified in Chapter 5 and 6 of this study. The comprehensive scope puts this work apart from recent and ongoing research works in the same field [8], [45], [90], [120], [121], which focus only in the radio front-end design.
6. Overall, this thesis has confirmed the feasibility of ultra-low-power, autonomous and robust event-driven radios in CMOS technologies by following a systematic approach, devising innovative architectures, and optimizing circuit performance.

7.3 Recommendations for Future Work

Based on this work, several related areas of research in this emerging field can be explored in future.

The transmitter and receiver front-ends presented in this thesis can be integrated together with the digital baseband (currently on FPGA) onto a single CMOS chip. Single-chip integration should also consider the inclusion of the off-chip matching network and the DCO inductor used in the transmitter. This may introduce loss of performance or increase of power consumption, which might be compensated by newer circuit techniques or more advanced technologies. The system-on-chip integration of event-driven radios can effectively reduce the size, weight and cost of the event-driven nodes, paving the way for mass application in various markets.

The transceiver performance in this work can be further improved, or the power consumption can be reduced to support a wider range of applications. This can be done if several circuit blocks are redesigned. In the receiver, the noise figure and the linearity of the RF front-end can be improved to boost the sensitivity and interference rejection. For the transmitter, the LO buffer between the DCO and PA can be removed to improve the power efficiency, although frequency accuracy and stability may be affected. As derived in Chapter 5, the 2-tone IF-PSK modulation should be tolerant to such degradation. In addition, the output level of the transmitter can be lowered further if shorter range communication is sufficient, to reduce the Tx power dissipation.

A proof-of-concept, autonomous, event-driven platform can be designed incorporating the sensing, signal processing, radio communication and energy-harvesting modules, similar to [122]. The autonomous operation of the event-driven nodes with the help of energy-harvesting technology can emphasize the power efficiency of the event-driven radio.

The circuits implemented in this work are fabricated in typical process corner and verified for nominal conditions of supply voltage and temperature. Due to the variety of potential applications, an improved event-driven radio should be reliable under all possible circum-

stances, for example, under varying ambient temperature and humidity when the wireless network is deployed outdoors, as well as for all process corners to ensure high yield in production. Therefore, a redesign should ensure sufficient margin for PVT variations, however, with a possible penalty in power consumption. Alternatively, the built-in self-test and calibration principles adopted in this work (i.e., the Tx LO swing and frequency calibration) can be extended to other parts of the radio to ensure the required level of performance across a wide range of operating conditions without increasing the power consumption.

Apart from addressing these technical challenges, the support from industrial standards is also a key factor in the development of wireless event-driven applications. Although several new IEEE standards have been defined for low-power, short-range wireless communication, for example IEEE802.15.4 WPAN (for wireless personal area network) [123] and its variants, IEEE802.15.4g-SUN (for smart utility network) [124] and IEEE802.15.4k-LECIM (for low energy, critical infrastructure monitoring networks) [125], none of them is tailored to event-driven applications with an extremely low power budget imposed by energy-harvesting sources. New standards should be defined for such applications so that devices from different manufacturers can operate together, with quality of service ensured. Comprehensive system-level studies should also be carried out to combine the latest research achievements on different layers, such as the physical, data link and network layers, into successful standards.

Bibliography

[1] "nRF905 Single chip 433/868/915MHz Transceiver Product Specification." Nordic Semiconductor, 2008.

[2] "nRF24L01+ Single Chip 2.4GHz Transceiver Product Specification v1.0." Nordic Semiconductor, 2008.

[3] "CC2500 Low-Cost Low-Power 2.4 GHz RF Transceiver." Texas Instruments, 2009.

[4] "CC1101 Low-Power Sub-1 GHz RF Transceiver." Texas Instruments, 2013.

[5] P. Ross, "Managing care through the air [remote health monitoring]," *IEEE Spectrum*, vol. 41, no. 12, pp. 26–31, Dec-2004.

[6] R. Fensli, E. Gunnarson, and O. Hejlesen, "A wireless ECG system for continuous event recording and communication to a clinical alarm station.," in *Proceedings of 26th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (IEMBS)*, 2004, vol. 3, pp. 2208–11.

[7] C. V Pollack, "Wireless cardiac event alert monitoring is feasible and effective in the emergency department and adjacent waiting areas.," *Critical pathways in cardiology*, vol. 8, no. 1, pp. 7–11, Mar-2009.

[8] N. Pletcher, "Ultra-low power wake-up receivers for wireless sensor networks," University of California, Berkeley, Berkeley, 2008.

[9] E. Jovanov and A. Milenkovic, "Body Area Networks for ubiquitous healthcare applications: opportunities and challenges.," *Journal of medical systems*, vol. 35, no. 5, pp. 1245–54, Oct-2011.

[10] Y. Li, Z. Wang, and Y. Song, "Wireless Sensor Network Design for Wildfire Monitoring," in *Proceedings of 6th World Congress on Intelligent Control and Automation*, 2006, pp. 109–113.

[11] D. M. Doolin and N. Sitar, "Wireless sensors for wildfire monitoring," in *Smart Structures and Materials: Sensors and Smart Structures Technologies for Civil, Mechanical, and Aerospace Systems*, 2005, vol. 5765, pp. 477–484.

[12] G. Werner-Allen, K. Lorincz, M. Ruiz, O. Marcillo, J. Johnson, J. Lees, and M. Welsh, "Deploying a wireless sensor network on an active volcano," *IEEE Internet Computing*, vol. 10, no. 2, pp. 18–25, Mar-2006.

[13] H. Dubois-Ferriere, R. Meier, L. Fabre, and P. Metrailler, "TinyNode: a comprehensive platform for wireless sensor network applications," in *Proceedings of 5th International Conference on Information Processing in Sensor Networks*, 2006, pp. 358–365.

[14] C. C. Enz, A. El-Hoiydi, J.-D. Decotignie, and V. Peiris, "WiseNET: an ultralow-power wireless sensor network solution," *Computer*, vol. 37, no. 8, pp. 62–70, Aug-2004.

[15] E. Le Roux, N. Scolari, B. Banerjee, C. Arm, P. Volet, D. Sigg, P. Heim, J.-F. Perotto, F. Kaess, N. Raemy, A. Vouilloz, D. Ruffieux, M. Contaldo, F. Giroud, D. Severac, M. Morgan, S. Gyger, C. Monneron, T.-C. Le, C. Henzelin, and V. Peiris, "A 1V RF SoC with an 863-to-928MHz 400kb/s radio and a 32b Dual-MAC DSP core for Wireless Sensor and Body Networks," in *Proceedings of IEEE International Solid-State Circuits Conference (ISSCC)*, 2010, pp. 464–465.

[16] J. P. Carmo, P. M. Mendes, C. Couto, and J. H. Correia, "A 2.4-GHz CMOS Short-Range Wireless-Sensor-Network Interface for Automotive Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 5, pp. 1764–1771, May-2010.

[17] M. Gorlatova, P. Kinget, I. Kymissis, D. Rubenstein, X. Wang, and G. Zussman, "Energy harvesting active networked tags (EnHANTs) for ubiquitous object networking," *IEEE Wireless Communications*, vol. 17, no. 6, pp. 18–25, Dec. 2010.

[18] M. Shen and H. Tenhunen, "Cost and performance analysis for mixed-signal system implementation: system-on-chip or system-on-package?," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 25, no. 4, pp. 262–272, Oct-2002.

[19] R. R. Tummala and V. K. Madisetti, "System on chip or system on package?," *IEEE Design & Test of Computers*, vol. 16, no. 2, pp. 48–56, 1999.

[20] A. Fontanelli, "System-in-Package Technology: Opportunities and Challenges," in *Proceedings of 9th International Symposium on Quality Electronic Design (ISQED)*, 2008, pp. 589–593.

[21] K. Yadav, I. Kymissis, and P. R. Kinget, "A 4.4μW Wake-Up Receiver Using Ultrasound Data," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 3, pp. 649–660, Mar. 2013.

[22] H. Ishihara, T. Umeda, K. Ohno, S. Iwata, F. Moritsuka, T. Itakura, M. Ishibe, K. Hijikata, and Y. Maki, "A 130μA wake-up receiver SoC in 0.13μm CMOS for reducing standby power of an electric appliance controlled by an infrared remote controller," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2011, pp. 226–228.

[23] B. Otis and J. Rabaey, *Ultra-Low Power Wireless Technologies for Sensor Networks (Integrated Circuits and Systems)*. Springer, 2007.

[24] M. A. Ingram, L. Thanayankizil, and J. W. Jung, "Perspectives on Energy-Harvesting Wireless Sensor Networks," *Globalization of Mobile and Wireless Communications*, Springer Netherlands, Dordrecht, pp. 249–274, 2011.

[25] M. Gorlatova, A. Wallwater, and G. Zussman, "Networking low-power energy harvesting devices: Measurements and algorithms," *2011 Proceedings IEEE INFOCOM*, pp. 1602–1610, Apr. 2011.

[26] J. Kao, S. Narendra, and A. Chandrakasan, "Subthreshold leakage modeling and reduction techniques [IC CAD tools]," in *IEEE/ACM International Conference on Computer Aided Design, 2002. ICCAD 2002.*, pp. 141–148.

[27] A. A. P. Chandrakasan, R. Min, M. Bhardwaj, S.-H. H. Cho, and A. Wang, "Power aware wireless microsensor systems," in *Proceedings of the 28th European Solid-State Circuits Conference (ESSCIRC)*, 2002, pp. 47–54.

[28] E. Lin, "A comprehensive study of power-efficient rendezvous schemes for wireless sensor networks," University of California, Berkeley, 2005.

[29] Y. Ou, "Sleeping Strategies for Wireless Sensor Networks," University of Rochester, 2011.

[30] Y. Zhang, L. Huang, G. Dolmans, and H. de Groot, "An analytical model for energy efficiency analysis of different wakeup radio schemes," in *IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, 2009, pp. 1148–1152.

[31] V. Jelicic, M. Magno, D. Brunelli, V. Bilas, and L. Benini, "Analytic comparison of wake-up receivers for WSNs and benefits over the wake-on radio scheme," *Proceedings of the 7th ACM workshop on Performance monitoring and measurement of heterogeneous wireless and wired networks - PM2HW2N*, ACM Press, New York, New York, USA, p. 99, 2012.

[32] Y. Zhang, A. Breeschoten, X. Huang, N. Kiyani, A. Ba, P. Harpe, K. Imamura, R. de Francisco, V. Pop, G. Dolmans, and H. de Groot, "Improving energy-efficiency in

building automation with event-driven radio," in *International Conference on Wireless Communications and Signal Processing (WCSP)*, 2011, pp. 1–5.

[33] I. Mampentzidou, E. Karapistoli, and A. a. Economides, "Basic guidelines for deploying Wireless Sensor Networks in agriculture," in *International Congress on Ultra Modern Telecommunications and Control Systems*, 2012, pp. 864–869.

[34] R. Beckwith, D. Teibel, and P. Bowen, "Unwired wine: sensor networks in vineyards," in *Proceedings of IEEE Sensors*, 2004, pp. 561–564.

[35] Y. Zhang and G. Dolmans, "Wake-up radio assisted energy-aware multi-hop relaying for low power communications," *IEEE Wireless Communications and Networking Conference (WCNC)*, pp. 2498–2503, Apr. 2012.

[36] S. Ergen and P. Varaiya, "On multi-hop routing for energy efficiency," *IEEE Communications Letters*, vol. 9, no. 10, pp. 880–881, Oct. 2005.

[37] "ISM 868 MHz Ceramic Antenna W3013 Datasheet." Pulse Electronics Corporation.

[38] S. Y. Seidel and T. S. Rappaport, "914 MHz path loss prediction models for indoor wireless communications in multifloored buildings," *IEEE Transactions on Antennas and Propagation*, vol. 40, no. 2, pp. 207–217, 1992.

[39] D. C. Daly and A. P. Chandrakasan, "An Energy-Efficient OOK Transceiver for Wireless Sensor Networks," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, May 2007.

[40] B. Otis, Y. H. Chee, and J. Rabaey, "A 400μW-RX, 1.6mW-TX superregenerative transceiver for wireless sensor networks," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2005, vol. 36, no. 3, pp. 396–398.

[41] Y. Chee, "Ultra low power transmitters for wireless sensor networks," University of California, Berkeley, 2006.

[42] Y.-H. Liu, "Design of 400-MHz energy-efficient RF transceivers for bio-medical implantable applications," National Taiwan University, 2009.

[43] N. M. Pletcher, S. Gambini, S. Member, and J. Rabaey, "A 52μW Wake-Up Receiver With -72 dBm Sensitivity Using an Uncertain-IF Architecture," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.

[44] N. Pletcher, S. Gambini, and J. Rabaey, "A 65 μW, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," in *IEEE Custom Integrated Circuits Conference*, 2007, pp. 539–542.

[45] J. Pandey, J. Shi, and B. Otis, "A 120μW MICS/ISM-band FSK receiver with a 44μW low-power mode based on injection-locking and 9x frequency multiplication," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2011, vol. 61, no. 10, pp. 460–462.

[46] D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, Z. N. Aldworth, T. L. Daniel, J. Voldman, J. G. Hildebrand, and A. P. Chandrakasan, "A Pulsed UWB Receiver SoC for Insect Motion Control," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 153–166, Jan. 2010.

[47] B. Vigraham and P. Kinget, "A self-duty-cycled and synchronized UWB receiver SoC consuming 375pJ/b for −76.5dBm sensitivity at 2Mb/s," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 444–445.

[48] M. Crepaldi, C. Li, J. R. Fernandes, and P. R. Kinget, "An Ultra-Wideband Impulse-Radio Transceiver Chipset Using Synchronized-OOK Modulation," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2284–2299, Oct. 2011.

[49] B. P. P. Otis, Y. H. H. Chee, R. Lu, N. M. M. Pletcher, and J. M. M. Rabaey, "An ultra-low power MEMS-based two-channel transceiver for wireless sensor networks," in *Symposium on VLSI Circuits Digest of Technical Papers IEEE*, 2004, pp. 20–23.

[50] Y. Chee, A. M. Niknejad, and J. M. Rabaey, "An Ultra-Low-Power Injection Locked Transmitter for Wireless Sensor Networks," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1740–1748, Aug. 2006.

[51] Y. Chee, A. Niknejad, and J. Rabaey, "A 46% Efficient 0.8dBm Transmitter for Wireless Sensor Networks," in *Symposium on VLSI Circuits Digest of Technical Papers*, 2006, pp. 43–44.

[52] P. R. Kinget, "Designing analog and RF circuits for ultra-low supply voltages," *ESSCIRC 2007 - 33rd European Solid-State Circuits Conference*, pp. 58–67, Sep. 2007.

[53] D. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*. Wiley-Interscience, 2008, p. 632.

[54] E. A. Vittoz, "Weak inversion for ultra low-power and very low-voltage circuits," in *2009 IEEE Asian Solid-State Circuits Conference*, 2009, pp. 129–132.

[55] N. Pletcher and J. Rabaey, "A 100 μW, 1.9GHz oscillator with fully digital frequency tuning," in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC)*, 2005, pp. 387–390.

[56] K. Bult, “Analog design in deep sub-micron CMOS,” in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC)*, 2000, pp. 126–132.

[57] P. R. Kinget, “Device mismatch and tradeoffs in the design of analog circuits,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1212–1224, Jun. 2005.

[58] M. J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, “Transistor matching in analog CMOS applications,” in *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, pp. 915–918.

[59] C.-H. Jan, M. Agostinelli, H. Deshpande, M. A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, H. Lakdawala, J. Lin, Y.-L. Lu, S. Mudanai, J. Park, A. Rahman, J. Rizk, W.-K. Shin, K. Soumyanath, H. Tashiro, C. Tsai, P. VanDerVoorn, J.-Y. Yeh, and P. Bai, “RF CMOS technology scaling in High-k/metal gate era for RF SoC (system-on-chip) applications,” in *2010 International Electron Devices Meeting*, 2010, pp. 27.2.1–27.2.4.

[60] C. H. Diaz, D. D. Tang, and J. Sun, “CMOS technology for MS/RF SoC,” *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 557–566, Mar. 2003.

[61] R. Brederlow, “Low Frequency Noise Considerations for CMOS Analog Circuit Design,” in *AIP Conference Proceedings*, 2005, vol. 780, no. 1, pp. 703–708.

[62] P. Andreani and S. Mattisson, “On the use of MOS varactors in RF VCOs,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, Jun. 2000.

[63] T. Soorapanth, C. P. C. Yue, D. K. Shaeffer, T. I. Lee, and S. S. Wong, “Analysis and optimization of accumulation-mode varactor for RF ICs,” in *1998 Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No.98CH36215)*, 1998, pp. 32–33.

[64] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, “CMOS mixers and polyphase filters for large image rejection,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, Jun. 2001.

[65] K. F. Smith, “A digital-trim controlled on-chip RC oscillator,” in *Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems. MWSCAS 2001 (Cat. No.01CH37257)*, 2001, vol. 2, pp. 882–885.

[66] J. R. LONG, “Passive Components for Silicon RF and MMIC Design,” *IEICE TRANSACTIONS on Electronics*, vol. E86–C, no. 6. The Institute of Electronics, Information and Communication Engineers, pp. 1022–1031, 01-Jun-2003.

[67] J. R. Long, “Monolithic transformers for silicon RF IC design,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[68] R. Staszewski, K. Muhammad, and D. Leipold, "Digital Signal Processing for RF at 45-nm CMOS and Beyond," in *IEEE Custom Integrated Circuits Conference 2006*, 2006, pp. 517–522.

[69] M. M. Frank, "High-k / metal gate innovations enabling continued CMOS scaling," in *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2011, pp. 25–33.

[70] M. Powell, S.-H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-Vdd: a circuit technique to reduce leakage in deep-submicron cache memories," in *Low Power Electronics and Design, 2000. ISLPED '00. Proceedings of the 2000 International Symposium on*, 2000, pp. 90–95.

[71] R. B. Staszewski, J. Wallberg, S. Rezeq, O. Eliezer, S. Vemulapalli, R. Staszewski, N. Barton, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and GSM/edge transmitter in 90nm CMOS," in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, 2005, vol. 51, no. 11, pp. 316–318.

[72] R. B. Staszewski, K. Muhammad, D. Leipold, C. Hung, Y. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, P. T. Balsara, and S. Member, "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[73] R. B. Staszewski, I. Bashir, and O. Eliezer, "RF Built-in Self Test of a Wireless Transmitter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 2, pp. 186–190, Feb. 2007.

[74] S. Bou-Sleiman and M. Ismail, *Built-in-Self-Test and Digital Self-Calibration for RF SoCs*. Springer, 2011, p. 106.

[75] J. Mehta, R. B. Staszewski, O. Eliezer, S. Rezeq, K. Waheed, M. Entezari, G. Feygin, S. Vemulapalli, V. Zoicas, C.-M. Hung, N. Barton, I. Bashir, K. Maggio, M. Frechette, M.-C. Lee, J. Wallberg, P. Cruise, and N. Yanduru, "A 0.8mm^2 all-digital SAW-less polar transmitter in 65nm EDGE SoC," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 58–59.

[76] C. Tsang, Y. Chiu, J. Vanderhaegen, S. Hoyos, C. Chen, R. Brodersen, and B. Nikolic, "Background ADC calibration in digital domain," in *2008 IEEE Custom Integrated Circuits Conference*, 2008, pp. 301–304.

[77] P.-I. Mak, S.-P. U, and R. Martins, "Transceiver architecture selection: Review, state-of-the-art survey and case study," *IEEE Circuits and Systems Magazine*, vol. 7, no. 2, pp. 6–25, 2007.

[78] R. van Langevelde, M. van Elzakker, D. van Goor, H. Termeer, J. Moss, and a. J. Davie, "An ultra-low-power 868/915 MHz RF transceiver for wireless sensor network applications," *2009 IEEE Radio Frequency Integrated Circuits Symposium*, pp. 113–116, Jun. 2009.

[79] Y. Liu, X. Huang, M. Vidojkovic, G. Dolmans, and H. de Groot, "An energy-efficient polar transmitter for IEEE 802.15.6 body area networks: system requirements and circuit designs," *IEEE Communications Magazine*, vol. 50, no. 10, pp. 118–127, Oct. 2012.

[80] J. L. Bohorquez, J. L. Dawson, and A. P. Chandrakasan, "A 350μW CMOS MSK transmitter and 400μW OOK super-regenerative receiver for Medical Implant Communications," in *IEEE Symposium on VLSI Circuits*, 2008, pp. 32–33.

[81] G. Chien, Y. A. Hsu, and L. Tse, "A 2.4GHz CMOS transceiver and baseband processor chipset for 802.11b wireless LAN application," in *2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC.*, 2003, vol. 1, pp. 358–499.

[82] P. Choi, H. C. Park, S. Kim, S. M. S. S. Park, I. Nam, T. W. Kim, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, K. Lee, and S. Member, "An experimental coin-sized radio for extremely low-power wpan (IEEE 802.15.4) application at 2.4 ghz," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2258–2268, Dec. 2003.

[83] A. C. W. Wong, G. Kathiresan, C. K. T. Chan, O. Eljamaly, O. Omeni, D. McDonagh, A. J. Burdett, and C. Toumazou, "A 1 V Wireless Transceiver for an Ultra-Low-Power SoC for Biotelemetry Applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1511–1521, Jul. 2008.

[84] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.

[85] Y.-H. Liu, X. Huang, M. Vidojkovic, A. Ba, P. Harpe, G. Dolmans, and H. de Groot, "A 1.9nJ/b 2.4GHz multistandard (Bluetooth Low Energy/Zigbee/IEEE802.15.6) transceiver for personal/body-area networks," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 446–447.

[86] D. Park, "A 2.5-GHz 860μW charge-recycling fractional-N frequency synthesizer in 130nm CMOS," in *IEEE Symposium on VLSI Circuits*, 2008, pp. 88–89.

[87] J.-Y. Chen, M. P. Flynn, and J. P. Hayes, "A Fully Integrated Auto-Calibrated Super-Regenerative Receiver in 0.13µm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1976–1985, Sep. 2007.

[88] L. W. Couch, *Digital and Analog Communication Systems*, 6th Editio. Prentice Hall, 2001.

[89] S. von der Mark, R. Kamp, M. Huber, and G. Boeck, "Three stage wakeup scheme for sensor networks," in *SBMO/IEEE MTT-S International Conference on Microwave and Optoelectronics, 2005.*, 2005, pp. 205–208.

[90] N. E. Roberts and D. D. Wentzloff, "A 98nW wake-up radio for wireless body area networks," in *IEEE Radio Frequency Integrated Circuits Symposium*, 2012, pp. 373–376.

[91] X. Huang, P. Harpe, X. Wang, G. Dolmans, and H. de Groot, "A 0dBm 10Mbps 2.4GHz ultra-low power ASK/OOK transmitter with digital pulse-shaping," in *IEEE Radio Frequency Integrated Circuits Symposium*, 2010, pp. 263–266.

[92] M. Vidojkovic, X. Huang, P. Harpe, S. Rampu, C. Zhou, L. Huang, J. van de Molengraft, K. Imamura, B. Busze, F. Bouwens, M. Konijnenburg, J. Santana, A. Breeschoten, J. Huisken, K. Philips, G. Dolmans, and H. de Groot, "A 2.4 GHz ULP OOK Single-Chip Transceiver for Healthcare Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 6, pp. 523–534, Dec. 2011.

[93] J. P. Carmo, N. Sé. Dias, H. R. Silva, P. M. Mendes, C. Couto, and J. H. Correia, "A 2.4-GHz Low-Power/Low-Voltage Wireless Plug-and-Play Module for EEG Applications," *IEEE Sensors Journal*, vol. 7, no. 11, pp. 1524–1531, Nov. 2007.

[94] D. J. Young, S. J. Mallin, and M. Cross, "2 GHz CMOS Voltage-Controlled Oscillator with Optimal Design of Phase Noise and Power Dissipation," *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 131–134, Jun. 2007.

[95] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[96] T. S. D. Cheung and J. R. Long, "Shielded Passive Devices for Silicon-Based Monolithic Microwave and Millimeter-Wave Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006.

[97] Y. H. Chee, J. Rabaey, and A. M. Niknejad, "A class A/B low power amplifier for wireless sensor networks," in *IEEE International Symposium on Circuits and Systems*, 2004, pp. IV–409–12.

[98] M. K. Raja, "A 52 pJ/bit OOK transmitter with adaptable data rate," in *IEEE Asian Solid-State Circuits Conference (ASSCC)*, 2008, pp. 341–344.

[99] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[100] J. M. Rabaey, J. Ammer, T. Karalar, B. Otis, M. Sheets, and T. Tuan, "PicoRadios for wireless sensor networks: the next challenge in ultra-low power design," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2002, vol. 1, pp. 200–201.

[101] M. Kac and A. J. F. Siegert, "On the Theory of Noise in Radio Receivers with Square Law Detectors," *Journal of Applied Physics*, vol. 18, no. 4, p. 383, 1947.

[102] I. T. Monroy, "On analytical expressions for the distribution of the filtered output of square envelope receivers with signal and colored Gaussian noise input," *IEEE Transactions on Communications*, vol. 49, no. 1, pp. 19–23, 2001.

[103] C. Helstrom, "Distribution of the filtered output of a quadratic rectifier computed by numerical contour integration," *IEEE Transactions on Information Theory*, vol. 32, no. 4, pp. 450–463, Jul. 1986.

[104] W. Feller, *An introduction to probability theory and its applications*, Volume 2. Wiley, 1966.

[105] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[106] R. Adler, "A study of locking phenomena in oscillators," *Proceedings of the IEEE*, vol. 61, no. 10, pp. 1380–1385, 1973.

[107] E. A. Vittoz, M. G. R. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: theory and application," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 3, pp. 774–783, Jun. 1988.

[108] B. Razavi, *RF Microelectronics*. Prentice Hall, 1997, p. 352.

[109] M. Schwartz, W. R. Bennett, and S. Stein, "Communication Systems and Techniques," *IEEE Communications Magazine*, vol. 34, no. 5, p. 9, May 1996.

[110] A. Ba, "Ultra-low-power Digitally-controlled Oscillator for Event-driven Transmitter," Delft University of Technology, 2011.

[111] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, Jun. 2001.

[112] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.

[113] A. Jerng and C. G. Sodini, "The impact of device type and sizing on phase noise mechanisms," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 360–369, Feb. 2005.

[114] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS Broadband Power Amplifier With a Transformer-Based High-Order Output Matching Network," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.

[115] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26μW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[116] A. Molnar, B. Lu, S. Lanzisera, B. W. Cook, and K. S. J. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference (CICC)*, 2004, pp. 401–404.

[117] "B3718 SAW RF filter - Short range device," *EPCOS Datasheet*. EPCOS, 2009.

[118] J. D. Meindl and P. H. Hudson, "Low power linear circuits," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, vol. IX, no. 2, pp. 112–113, Dec. 1966.

[119] B. Murmann, "ADC Performance Survey 1997-2013," 2013. [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

[120] S. Drago, D. M. W. Leenaerts, F. Sebastiano, L. J. Breems, K. A. A. Makinwa, and B. Nauta, "A 2.4GHz 830pJ/bit duty-cycled wake-up receiver with −82dBm sensitivity for crystal-less wireless sensor nodes," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2010, pp. 224–225.

[121] J. Pandey and B. P. Otis, "A Sub-100 μW MICS/ISM Band Transmitter Based on Injection-Locking and Frequency Multiplication," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1049–1058, May 2011.

[122] R. Shad, B. P. Otis, Y. Chee, J. M. Rabaey, and P. Wright, "A 1.9GHz RF Transmit Beacon using Environmentally Scavenged Energy."

[123] “802.15.4-2003 - IEEE Standard for Information Technology - Telecommunications and Information Exchange Between Systems - Local and Metropolitan Area Networks Specific Requirements Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) ,” 2003.

[124] “IEEE Standard for Local and metropolitan area networks--Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs) Amendment 3: Physical Layer (PHY) Specifications for Low-Data-Rate, Wireless, Smart Metering Utility Networks.” pp. 1–252, 2012.

[125] “IEEE Standard for Local and metropolitan area networks Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs)Amendment 5: Physical Layer Specifications for Low Energy, Critical Infrastructure Monitoring Networks.” 2013.

List of Publications

Journal Papers

X. Huang, A. Ba, P. Harpe, G. Dolmans, H. de Groot, J.R. Long, "A 915 MHz, Ultra-Low Power 2-Tone Transceiver with Enhanced Interference Resilience," *IEEE Journal of Solid-State Circuits,* vol.47, no.12, pp.3197-3207, Dec. 2012.

X. Huang, P. Harpe, G. Dolmans, H. de Groot, J.R. Long, "A 780MHz to 950MHz, 64μW to 146μW Power-Scalable Synchronized-Switching OOK Receiver for Wireless Event-Driven Applications," accepted by *IEEE Journal of Solid-State Circuits,* Feb. 2014.

X. Huang, G. Dolmans, H. de Groot, J.R. Long, "Noise and Sensitivity in RF Envelope Detection Receivers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.60, no.10, pp.637-641, Oct. 2013.

M. Vidojkovic, **X. Huang**, P. Harpe, S. Rampu, C. Zhou, L. Huang, J. van de Molengraft, K. Imamura, B. Busze, F. Bouwens, M. Konijnenburg, J. Santana, A. Breeschoten, J. Huisken, K. Philips, G. Dolmans, H. de Groot, "A 2.4 GHz ULP OOK Single-Chip Transceiver for Healthcare Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol.5, no.6, pp.523-534, Dec. 2011.

Conference Papers

X. Huang, S. Rampu, X. Wang, G. Dolmans, H. de Groot, "A 2.4GHz/915MHz 51μW Wake-Up Receiver with Offset and Noise Suppression," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* pp.222-223, 7-11 Feb. 2010.

M. Vidojkovic, **X. Huang**, P. Harpe, S. Rampu, C. Zhou, L. Huang, K. Imamura, B. Busze, F. Bouwens, M. Konijnenburg, J. Santana, A. Breeschoten, J. Huisken, G. Dolmans, H. de Groot, "A 2.4 GHz ULP OOK Single-Chip Transceiver for Healthcare Applications", *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* pp.458-459 Feb. 2011.

X. Huang, P. Harpe, X. Wang, G. Dolmans, H. de Groot, "A 0dBm 10Mbps 2.4GHz Ultra-Low Power ASK/OOK Transmitter with Digital Pulse-Shaping," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* pp.263-266, 23-25 May 2010.

X. Huang, P. Harpe, G. Dolmans, H. de Groot, "A 915MHz Ultra-Low Power Wake-Up Receiver with Scalable Performance and Power Consumption," *IEEE European Solid-State Circuit Conference (ESSCIRC),* pp.543-546, 12-16 Sept. 2011.

X. Huang, A. Ba, P. Harpe, G. Dolmans, H. de Groot, J.R. Long, "A 915MHz 120μW-RX/900μW-TX Envelope-Detection Transceiver with 20dB In-Band Interference Tolerance," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* pp.454-456, 19-23 Feb. 2012.

Y. Zhang, A. Breeschoten, **X. Huang**, N. Kiyani, A. Ba, P. Harpe, K. Imamura, R. De Francisco, V. Pop, G. Dolmans, H. de Groot, "Improving Energy-Efficiency in Building Automation with Event-Driven Radio," *International Conference on Wireless Communications and Signal Processing (WCSP),* 9-11 Nov. 2011.

N. Kiyani, Y. Zhang, P. Harpe, **X. Huang**, G. Dolmans, "Performance Analysis and Measurement Results of An Ultra-Low Power Wakeup Radio in the Presence of Interference," *URSI General Assembly and Scientific Symposium,* 13-20 Aug. 2011.

Book Chapters

G. Dolmans, F. Bouwens, A. Breeschoten, B. Busze, P. Harpe, L. Huang, **X. Huang**, M.

Konijnenburg, V. Pop, M. Vidojkovic, “Ultra Low-Power Wireless Body-Area Sensor Networks,” book chapter in *Analog Circuit Design*, pp.145-162, 2012,Springer Netherlands.

Other Papers

Y-H. Liu, **X. Huang**, M. Vidojkovic, G. Dolmans, H. de Groot, "An Energy-Efficient Polar Transmitter for IEEE 802.15.6 Body Area Networks: System Requirements and Circuit Designs," *IEEE Communications Magazine,* vol.50, no.10, pp.118-127, October 2012.

M. Vidojkovic, **X. Huang**, X. Wang, C. Zhou, A. Ba, M. Lont, Y-H. Liu, P. Harpe, M. Ding, B. Busze, N. Kiyani, K. Kanda, S. Masui, K. Philips, H. de Groot, “A 0.33nJ/b IEEE802.15.6/Proprietary-MICS/ISM-Band Transceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications,” *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* Feb. 2014.

Y-H. Liu, **X. Huang**, M. Vidojkovic, A. Ba, P. Harpe, G. Dolmans, H. de Groot, "A 1.9nJ/b 2.4GHz Multistandard (Bluetooth Low Energy/Zigbee/IEEE802.15.6) Transceiver for Personal/Body-Area Networks," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* pp.446-447, 17-21 Feb. 2013.

Y-H. Liu, **X. Huang**, M. Vidojkovic, K. Imamura, P. Harpe, G. Dolmans, H. de Groot, "A 2.7nJ/b Multi-standard 2.3/2.4GHz Polar Transmitter for Wireless Sensor Networks," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* pp.448-450, 19-23 Feb. 2012.

X. Wang, Y. Yu, B. Busze, H. Pflug, A. Young, **X. Huang**, C. Zhou, M. Konijnenburg, K. Philips, H. de Groot, "A Meter-Range UWB Transceiver Chipset for Around-the-Head Audio Streaming," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* pp.450-452, 19-23 Feb. 2012.

M. Vidojkovic, Y-H. Liu, **X. Huang**, K. Imamura, G. Dolmans, H. de Groot, "A Fully Integrated 1.7–2.5GHz 1mW Fractional-N PLL for WBAN and WSN Applications," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp.185-188, 17-19 June 2012.

P. Harpe, **X. Huang**, X. Wang, G. Dolmans, H. de Groot, "A 0.37μW 4bit 1MS/s SAR ADC for Ultra-Low Energy Radios," *International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, 25-28 April 2011.

M. Notten, H. Veenstra, **X. Huang**, J.B. Mills, "A 60GHz LC-VCO Module Using Flip-Chip on A Laminate Substrate," *European Microwave Integrated Circuits Conference (EuMIC)*, pp.415-418, 28-29 Sept. 2009.

H. Veenstra, M. Notten, **X. Huang**, J.R. Long, "60GHz Quadrature Doppler Radar Transceiver in A 0.25μm SiGe BiCMOS Technology," *IEEE European Solid-State Circuit Conference (ESSCIRC)*, pp.246-249, 15-19 Sept. 2008.

Acknowledgements

It was a tough journey carrying out this PhD study while having another job. This dissertation would not have been completed with the generous support from my supervisors, colleagues, friends and family. Hereby, I would like to express my thankfulness to everyone who has helped me on the way to the completion.

My first and foremost gratitude belongs to my promoter and academic advisor, Prof. John R. Long. Your guidance started during my Master's study, both in the classrooms where you taught the course of RFIC design, and on one-to-one basis when I was working on my Master project in Philips Research. You seldom gave direct answers to my questions, but instead inspired me to think. I learned from you the prudent attitude toward research, logical way of thinking, and the courage to tackle complex problems. These are the best qualities a professor could offer to his/her students, which make them independent and responsible thinkers, capable of pushing forward the scientific and technical frontiers. When I had the idea of working on a PhD, I immediately came to you since I knew there would be a lot more things I could learn from you. It did not just stop at the academic level. I had to work hard on your jokes since your sense of humor can only be understood by intelligent people. In addition, your whereabouts is always a mystery since you left Delft, but I am grateful that you make a lot of efforts coming back and support me remotely till the completion of this thesis.

I am also indebted to my manger in imec – Holst Centre, Dr. Guido Dolmans. It was your initiative to start the wake-up receiver project, which later evolved to the event-driven radio. Since I joined imec in 2008, you gave me a lot of trust and freedom to explore and realize my ideas, and to build up the foundation of this thesis. When I proposed to start a PhD, you supported me as much as you could, and eventually I became the first person in imec – Holst Centre to carry out an on-job PhD. You also helped me translate the summary of this dissertation into Dutch, which I hope is also very meaningful to you.

I am grateful to the management of imec - Holst Centre which offered me the option of an on-job PhD. Beside Guido, the support also comes from my other manager Dr. Kathleen Philips, the program director Harmke de Groot, the HR director Marij Heil and many others. The support from Kathleen is crucial in keeping my PhD going forward during heavy work-loads and continuous deadlines. She also encouraged me to carry on and pushed me for results when I felt stuck.

I would like to thank Prof. Robert Bogdan Staszewski in TU Delft as well. Although we did not collaborate on this PhD thesis, we do work together on other projects in imec, and I can often get inspiration from our conversations. In fact, before you came to Delft, I had some ideas about digital-RF and found your papers and patents. It was a great news that you came to Delft, so I can learn more from you in future collaborations.

My appreciation also goes to my doctoral examination committee members, Prof. Long, Prof. Staszewski, and Dr. Dolmans, as well as Prof. Nauta and Prof. Baltus who I frequently came across in conferences, and Prof. Enz and Prof. Kinget who have to travel to the Netherlands from abroad, and the reserved member Prof. Makinwa who taught me during my Master's study. Thanks for reviewing my PhD thesis and the insightful comments on making it better.

I thank my previous supervisor in Philips Research, Dr. Hugo Veenstra, who not only guided me through my Master's project, but also provided me with tips and advises on managing an on-job PhD based on his first-hand experience.

There are so many colleagues and friends to whom I feel grateful. Dr. Pieter Harpe from Technology University of Eindhoven and Ao Ba from imec were part of the event-driven radio project, and I am proud to have their circuits in my chips. Jac Romme and Steffie van de Vorstenbosch helped me proofread the Dutch translation of the summary. Mark Stoopman, my colleague in both imec and TU Delft, did an excellent job on translating my propositions into Dutch. My colleagues in the Ultra-Low Power Wireless group of imec helped me a lot both on my job and on my life. I enjoyed the tennis drills and football games in High Tech Campus with Kanda-san, Songbo, Kezheng, Ming, Jac, Ruben, Stefano and others. I had a lot

of technical discussions, food, drinks, parties and fun with my friends Duan Zhao, Hao Gao, Yu Pu, Bo Liu, Wei Tong, Yongjia Li, Yao Liu, Xun Luo, and many others I forget to mention.

My peers from Fudan University deserve special mentioning. Yi Zhao and Wanghua Wu came to the Netherlands via the same program as me, and later carried out PhD study in the same group. There were moments of difficulties during these years, but we supported one another both at work and in daily life, so the transition and the stay in the Netherlands were rather pleasant.

During the 8-year stay in the Netherlands, I am mostly in debt to my family in China. My parents love me so much, but I only went back to them once a year. No matter what I do or where I am, their unconditional love and support make me feel safe and secure. I am eternally grateful, and I wish that someday I could pay them back. Special thanks to my mother, a wise, kind and resilient woman, who has a profound influence on my character.

To my girlfriend, Xiaofan Deng, thank you so much for your support and understanding during this whole process. It was you who encouraged me to pursue the PhD, and it was your love and trust that allows me to achieve higher. You have made my life wonderful. You also made a lot of sacrifices for bearing my long working hours, sharing my frustrations, and being away from your parents, to whom I am also grateful. You designed the cover of this thesis, which I think is a perfect finishing touch on this chapter of my life. I am looking forward to the next life adventure with you!

Xiongchuan Huang

March 2014, Rotterdam

Curriculum Vitae

Xiongchuan Huang was born on January 30, 1984 in Mianyang, Sichuan, China. He received the B.Sc. degree in Microelectronics from Fudan University, Shanghai, China in 2005. In 2006, he came to the Netherlands and started his Master of Science study in Delft University of Technology, where he received M.Sc. degree in Microelectronics with distinction (cum laude) in 2008.

In 2007, he worked in Philips Research, Eindhoven, the Netherlands, on a 60GHz radar receiver design on BiCMOS technology as his master thesis. From 2008 on, he has been working in imec – Holst Centre in Eindhoven where he is now a senior researcher. Since 2011 on, he has been working part-time in Delft University of Technology as a PhD researcher. His research interests are ultra-low power circuit and system design for radio communications.