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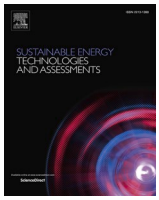

Two-stage active power curtailment-based islanding detection technique for photovoltaic-based microgrids with zero non-detection zone

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ABSTRACT

Effective islanding detection is mandatory for distributed generations (DGs) to avoid equipment damage and ensure the safety of network personnel. This paper proposes a fast, accurate, power quality-friendly, and practical two-stage active power curtailment (APC)-based islanding detection technique (IDT) for photovoltaic (PV)-rich microgrids. In the first stage, a periodic small disturbance is injected into the maximum power point tracking (MPPT) algorithm to slightly curtail the DG's active power, causing a small mismatch even on a balanced island. During islanding, the introduced active power mismatch shifts output voltage, triggering the second stage disturbance to the MPPT algorithm. Hence, the output voltage drops further, resulting in islanding detection. A real-time digital simulation (RTDS) using the modified IEEE 13-node system corroborates the successful detection of all stringent cases in less than 1.2 s with no false tripping for non-islanding disturbances. This zero non-detection zone (NDZ) is achieved by curtailing less than 1 % of the DG's available output. This technique is a practical solution for microgrids with high penetration of photovoltaic generators (PVGs) due to its simple structure and straightforward threshold determination, irrespective of the microgrid structure. The fast detection time allows the DG to seamlessly transition to the standalone microgrid.

Introduction

Nowadays, microgrids represent a large share of renewable energy sources worldwide, offering many techno-socio-economic-environmental opportunities and advantages [1]. Among all renewable resources, photovoltaic generators (PVGs) have been steadily installed due to their simple implementation, low maintenance cost, peak load shaving, and modularity. Despite these advances, the growing integration of PVGs on the distribution networks poses a few technical challenges, such as unintentional islanding [2]. A microgrid gets islanded when energized PVGs and local loads are electrically disconnected from the upstream network [3]. This situation may cause power quality (PQ) disturbances, a safety hazard for the network personnel, and equipment damage due to the out-of-phase reclosing [4]. All these consequences can occur for all grid-connected PVGs, regardless of the size, location, and technology. Several standards have proposed the post-islanding protection and control actions that should be taken to avert such consequences. To this end, IEEE Std. 1547–2018 recommends 2 s as the maximum islanding detection time for ceasing DGs' output power [5]. Further, this recently updated standard recommends a seamless transition from grid-connected to the controlled islanded mode. Thus, the DG would supply the critical loads of the autonomous microgrid after islanding detection and properly switching to grid-forming mode to regulate voltage and frequency [6]. This seamless transition to the controlled islanding process requires fast islanding detection without destabilizing the DGs [7]. Hence, developing a fast and reliable methodology for detecting the islanding operation of PVGs has drawn the attention of many researchers.

Various islanding detection techniques (IDTs), categorized into remote and local, have been developed for grid-connected PVGs. Remote schemes exploit a telecommunication channel between the upstream substation and DGs [8,9]. Islanding is identified when this link is lost due to a circuit breaker (CB) opening. These fast and reliable IDTs can be applied to synchronous-based and inverter-interfaced DG technologies. However, the expensive telecommunication infrastructures are still challenging for small-scale DG units, e.g., residential and commercial grid-connected PVGs.

On the other hand, local IDTs, including passive, active, and hybrid, are based on measuring magnitudes at the point of common coupling (PCC). As shown in Fig. 1 for a PV-based microgrid, the upstream grid compensates for the power mismatch between generation and load

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Nomenclature

Abbreviations

APC	Active power curtailment
CB	Circuit breaker
DG	Distributed generation
IDT	Islanding detection technique
MPPT	Maximum power point tracking
NDZ	Non-detection zone
OC	Open-circuit
PCC	Point of common coupling
PQ	Power quality
PVG	Photovoltaic generator
RoCoF	Rate of change of frequency
RTDS	Real-time digital simulator
SFS	Sandia frequency shift
THD	Total harmonic distortion
VSI	Voltage source inverter

Units

I_{DG}	DG output current (pu)
I_{MPP}	PV array MPP current (A)
I_{NEW}	Post-disturbance PV array current (A)
k_1	Ratio of V_{OC} to V_{MPP}
k_2	Ratio of ΔV_{PV} to V_{MPP}
P_L^{po}	Post-islanding load active power (kW)
P_L^{pr}	Pre-islanding load active power (kW)
R	Local load resistive model (Ω)
R_P	Parallel resistance of PV module model (Ω)
R_S	Series resistance of PV module model (Ω)
T	Time period of the injected disturbance (s)
t_{APC}	Time duration of the injected disturbance (s)
Th_1	Voltage threshold of the first stage (%)
Th_2	Voltage threshold of the second stage (%)
P_L	Local load active power (kW)
P_{MPP}	PV array MPP power (kW)
P_{NEW}	Post-disturbance PV array power (kW)
P_{DG}	DG active power output (kW)
Q_f	Load quality factor
Q_L	Load reactive power (kvar)
V_{MPP}	PV array MPP voltage (V)
V_{NEW}	Post-disturbance PV array voltage (V)
V_{OC}	PV array OC voltage (V)
$V_{PV,ref}$	Reference of PV array voltage (V)
V_{PCC}	PCC voltage (pu)
ΔP	Active power mismatch of an island (kW)
ΔQ	Reactive power mismatch of an island (kvar)
ΔV_{PCC}	PCC voltage variation after islanding (%)
ΔV_{PV}	PV array voltage shift (V)

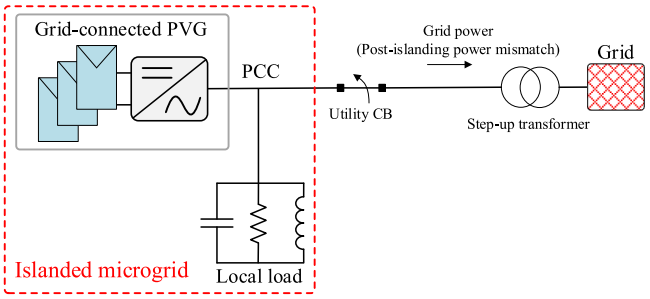

Fig. 1. Islanding event description of a PV-based microgrid.

during normal operation. When the utility CB opens, the grid's exchanged power with the microgrid terminates, shifting the local variables to new operating points. Therefore, the islanding condition is recognized in passive IDTs when the measured signal(s) deviates from the preset threshold(s). Banu et al. employed several passive relays, including under/over voltage, under/over frequency, rate of change of frequency (RoCoF), and DC link voltage, for detecting the islanding operation of grid-tied PVGs [10]. The combined method identifies the most critical islanding scenarios; however, deploying several relays increases the complexity and costs of the method. The rate of change of impedance at PCC has been estimated by differential equations and the least square error technique [11]. While this index is low in grid-connected mode, it increases sharply after islanding inception. The simulations highlight the small non-detection zone (NDZ) of the presented method, i.e., undetected islanding operating points in terms of active and reactive power mismatches. A similar idea has been adopted by Bharti et al., wherein superimposed positive and negative sequence impedances at the PCC have been compared with predefined thresholds [12]. The MATLAB/Simulink-based simulations underscore its timely and precise islanding detection for synchronous- and inverter-based DGs. The appropriate tuning of the two thresholds necessitates impedance data of the local load and upstream network, which vary significantly in real-time. Another impedance-based passive scheme has exploited two phasor measurement units at the upstream substation and PVG terminal [13]. Xing and Mu defined an impedance term containing voltage and current variation of both phasor measurement units, distinguishing islanding and internal faults in the presence of multi-PVGs. In another study, Wang et al. demonstrated that the large impedance angle at PCC becomes small or even negative after island formation. The main challenge of this IDT is to set the threshold for impedance angle, which depends on the load power factor and DG distance from PCC [14]. Despite simple implementation, classical/modern passive IDTs suffer from a moderate/small NDZ. Furthermore, setting the threshold at a small level would wrongly trigger the method in non-islanding disturbances, while some islanding events may remain undetected for a large threshold. Hence, threshold determination is another challenge that should be fulfilled as a compromise between minimum NDZ and false tripping in non-islanding transients.

Passive-based pattern recognition approaches have recently been developed to classify islanding and non-islanding events after sufficient training [15]. Chen et al. have applied differential Entropy and a well-trained support vector machine to the DGs' instantaneous active and reactive powers [16]. After islanding inception, the measured differential Entropy shifts markedly within two different timeframes, detecting the islanding event. The real-time digital simulation (RTDS)-based studies indicated the successful detection of all 240 islanding cases for a large microgrid. In [17], five features were initially extracted from the PCC voltage and then fed into a deep neural network for training. The MATLAB/Simulink-based simulations endorse $>$ 99 % islanding classification accuracy of the presented method if it is well-trained, e.g., using at least 200 datasets. Although the pattern recognition IDTs have improved the classical passive IDTs from the NDZ and speed perspectives, they suffer from high dependency on the structure and parameters of the studied case, e.g., input variables for training, number of layers, and number of neurons in [17]. Hence, time-consuming tests should be repeated when the microgrid parameter/structure changes, for example, adding or removing a DG.

To grapple with the shortcomings of passive IDTs, the injection of a controlled disturbance into the inverter-interfaced DG's control loop has been adopted in active schemes [18–20]. Hereby, the local variable

deviation is enlarged/expedited in islanding scenarios. Conversely, the effect of the injected disturbance is negligible in grid-connected mode as the upstream network strictly controls the PCC. Absolute negative voltage feedback has been inserted into the reference current of the voltage source inverter (VSI) [21]. This disturbance reduces the PVG's active power output in islanding operation, drifting the PCC voltage beyond the under-voltage setting. This methodology detects all islanding scenarios within ~ 0.8 s at the expense of destabilizing the PVG. Hence, the PVG cannot support the isolated microgrid after islanding detection. Gulipalli et al. have integrated an exponential term into the conventional active phase shift IDT [22]. The experimental results imply the method's reduced NDZ compared to the active phase shift scheme. Negative sequence current injection into the DC/AC converter of the VSI has been established by Shamseh et al. [23]. When the grid is out of service, this variable increases the negative sequence voltage at PCC. This positive feedback enlarges the negative sequence current; thus, this process repeats until the negative sequence voltage exceeds a predefined threshold. The threshold and parameters of the disturbance are determined through numerous simulations to ensure minimum NDZ. Similarly, a frequency deviation feedback has been injected into the reactive power control loop of inverter-interfaced DGs [24]. Besides the reduced NDZ and detection time, the PQ issue and lack of detection in multiple-DG scenarios are the main demerits of the presented IDT. Generally speaking, active IDTs move forward by diminishing the NDZ and detection time; however, the imposed disturbance enlarges the harmonics/subharmonics of the output current, showing PQ difficulties. Further, since the DG is destabilized for islanding detection purposes, it cannot supply the critical loads of the islanded microgrid in autonomous mode, as recommended by IEEE Std. 1547-2018 [5].

Finally, passive and active IDTs are applied in hybrid schemes to reduce the NDZ and the adverse effect of the disturbance on PQ [25]. In this regard, an active disturbance is injected when a passive criterion is stimulated. PCC voltage, frequency, and their derivative terms have been adopted by Serrano-Fontova et al. [26]. Through the measured indicators, a three-phase RC load is connected at the PCC to augment the variation of frequency and RoCoF. The simulations show negligible NDZ without maloperation in non-islanding transients. Similarly, the connection of parallel capacitance was used in [27] to introduce an additional power imbalance in suspicious events, shifting RoCoF out of predefined limits. In [28], RoCoF and sandia frequency shift (SFS) were combined. The proposed maximum likelihood approach indicates faster and higher accuracy in the RoCoF estimation process than the phase-locked-loop-based approach. The impact of the reactive power injection on the ratio of voltage total harmonic distortion (THD) to the current's one has been established as an islanding detection index [29]. The experimental tests reveal that while the RoCoF criterion cannot solely identify islanding events with small power mismatches, the imposed reactive power augments the power imbalance, eliminating the NDZ. These hybrid IDTs enhance the NDZ and speed of existing frequency/RoCoF relays. Nevertheless, their demerits are complexity, high cost, and the transients caused every time islanding is suspected, and dependency of the thresholds on the size of the connected load of the test case.

According to the IEEE Std. 1547-2018, an IDT can be commercialized when it passes all islanding requirements, especially the zero NDZ capability [5]. Therefore, solar inverter manufacturers mainly exploit active and hybrid methodologies, e.g., active frequency drift and small reactive power injection [30] and two RoCoF settings [31]. In addition, fast detection, simple structure, low PQ degradation, and self-standing settings tuning are other paramount features considered in the assessment of IDTs [32]. Therefore, developing a new IDT for PV-rich microgrids to enhance the currently available methodologies and address the features above is still of interest. To this end, this paper proposes a two-stage active power curtailment (APC)-based IDT for microgrids with high PVG penetration. In the first stage of this methodology, a periodic small disturbance is injected into the maximum power point tracking (MPPT) algorithm to curtail the active power output. This creates an active power mismatch between generation and demand, even on a perfectly balanced island. This PVG active power curtailment reduces the PCC voltage in islanding conditions, triggering the second stage disturbance into the MPPT algorithm. As a result, the PCC voltage drops further, and islanding is identified.

In addition to eliminating the NDZ, the proposed active IDT provides the following advantages:

- Accurate detection in less than 1.2 s, which is below the maximum permissible time mandated in [5].
- Straightforward threshold determination, irrespective of the microgrid's characteristics.
- Cost-effective integration into the existing VSIs due to its simple and inexpensive structure.
- Negligible adverse effect on PQ as the proposed disturbance does not enlarge harmonics/subharmonics.
- Facilitating the seamless transition to the controlled autonomous microgrid after islanding detection due to the fast maximum power point (MPP) restoration.
- Wide range of applications, as it can be implemented into all PV module and inverter technologies.

The rest of the paper is organized as follows. The next section elaborates on the proposed two-stage APC-based technique and selection criteria for threshold determination. The outstanding performance of the proposed method is then demonstrated, where various islanding and non-islanding scenarios are simulated in the RSCAD platform. Afterwards, the numerous advances of this IDT are highlighted through an in-depth comparison with a few existing solutions reported recently for PV-based microgrids. The next section analytically discusses the proposed method's negligible effect on PVG yield. Finally, concluding remarks and future works are discussed.

Description of the proposed technique

The main idea of the proposed two-stage IDT is to temporarily disturb the active power balance between the PVG and the load in the microgrid. This intentional active power mismatch is introduced by a change in the PV array reference voltage, resulting in an APC at the AC side. This methodology has been widely adopted in standalone microgrids where this curtailment regulates over frequency/voltage [33]. In the first stage, this power mismatch is used to identify suspicious islanding events, even for an island with zero power imbalance. In the second stage, a larger disturbance augments the existing active power mismatch to decline the voltage further for islanding detection purposes. The structure of the proposed IDT and analytical expressions for thresholds determination are presented as follows.

Methodology description

According to Fig. 1, the relation between PCC voltage (V_{PCC}) and active power in the normal operation can be expressed as follows:

$$P_L^{pr} = P_{DG} - \Delta P = \frac{V_{PCC}^2}{R} \tag{1}$$

where, P_L^{pr}, P_{DG}, and ΔP represent the pre-islanding active power of local load, DG, and grid, respectively. Also, R is the resistance part of the parallel RLC local load model, as defined in IEEE Std. 1547-2018 [5]. After island formation, the exchanged power with the grid is stopped, causing a mismatch between generation and load. Thus, the PCC voltage shifts to a new operating point to satisfy $P_{DG} = P_L^{po}$:

$$P_L^{po} = P_{DG} = \frac{(V_{PCC} + \Delta V_{PCC})^2}{R} \tag{2}$$

where, ΔV_{PCC} and P_L^{po} are the PCC voltage change and load's active power after the islanding occurrence. By combining the recent expressions, the relation between power imbalance and PCC voltage variation is yielded:

$$\frac{\Delta P}{P_{DG}} = 1 - \left(\frac{V_{PCC}}{V_{PCC} + \Delta V_{PCC}}\right)^2 \quad (3)$$

According to this term, the range of active power mismatches that post-islanding PCC voltage leaves the standard limits can be defined. For V_{PCC}=1 pu, for example, the post-islanding voltage remains inside the standard 0.88–1.10 pu range for $-29.13\,\% < \Delta P/P_{DG} < 17.36\,\%$ [5]; thus, when $\Delta P/P_{DG}$ is out of this range, the conventional voltage relay cannot detect islanding, suffering from a large NDZ.

The proposed IDT is structured to first identify the suspicious islanding events. In this regard, the absolute PCC voltage variation ($|\Delta V_{PCC}|$) is measured and compared with a preset threshold (Th_1). When $|\Delta V_{PCC}| \geq Th_1$, a suspicious event is classified. The absolute deviation is considered since the V_{PCC} can rise or drop after island formation. Furthermore, the PCC voltage measurement to compute $|\Delta V_{PCC}|$ is performed at the grid frequency, 50 Hz, in this paper.

Similar to the presented explanation for the voltage relay, the first stage cannot identify suspicious cases with $|\Delta V_{PCC}| < Th_1$. Hence, a temporary APC is introduced to shift the voltage, i.e., $\Delta P = \Delta P_{DG}$. To this end, the PVG active power curtails periodically by deviating its operating point from the MPP, as shown in the PV array power vs. voltage profile in Fig. 2 (a). In VSI, the MPPT algorithm is employed on the DC/DC converter to fully utilize the available power of the PV array, i.e., ensuring MPP operation. In this IDT, a small periodic disturbance is injected into the PV array voltage reference ($V_{PV,ref}$) in the MPPT algorithm:

$$V_{PV,ref} = V_{MPP} + \Delta V_{PV}^1 \quad (4)$$

The employed first stage disturbance voltage (ΔV_{PV}^1) shifts the PV array operating point to the right-hand side of MPP. Hence, the PVG active power is reduced, adding the required active power mismatch to satisfy $|\Delta V_{PCC}| \geq Th_1$ condition. Therefore, all critical islanding events, even the balanced ones, are identified as suspicious. When the first stage stimulates the second disturbance into the MPPT algorithm, the PV array operating point moves further to the right-hand side:

$$V_{PV,ref} = V_{MPP} + \Delta V_{PV}^2 \quad (5)$$

where, ΔV_{PV}^2 is the PV array voltage disturbance in the second stage and $\Delta V_{PV}^2 > \Delta V_{PV}^1$. The PVG active power curtails further, reducing the PCC voltage. Thus, the method detects the islanding events when the $|\Delta V_{PCC}|$ becomes larger than the predefined second threshold (Th_2). This also deactivates the periodic injection of the first stage disturbance.

According to the level of $\Delta P/P_{DG}$ in Eq. (3), three islanding scenarios can occur in the proposed IDT:

Large $\Delta P/P_{DG}$: Due to the significant active power mismatch, the PCC voltage leaves the standard range, and islanding is classified without further action.

Small $\Delta P/P_{DG}$: In the second scenario, the PCC voltage remains within the standard limits while its variation is greater than Th_1, $|\Delta V_{PCC}| \geq Th_1$ (Fig. 2 (b)). The existing active power mismatch meets the first stage condition, and this event is categorized as suspicious. Hence, the second disturbance is injected into the MPPT algorithm; either the first disturbance is injected or not. The active power of the PVG drops so that the PCC voltage is reduced. Thus, islanding is classified due to the simultaneous active power drop and $|\Delta V_{PCC}| \geq Th_2$. Note that when the PVG is connected to the grid, the effect of the imposed voltage disturbance is negligible.

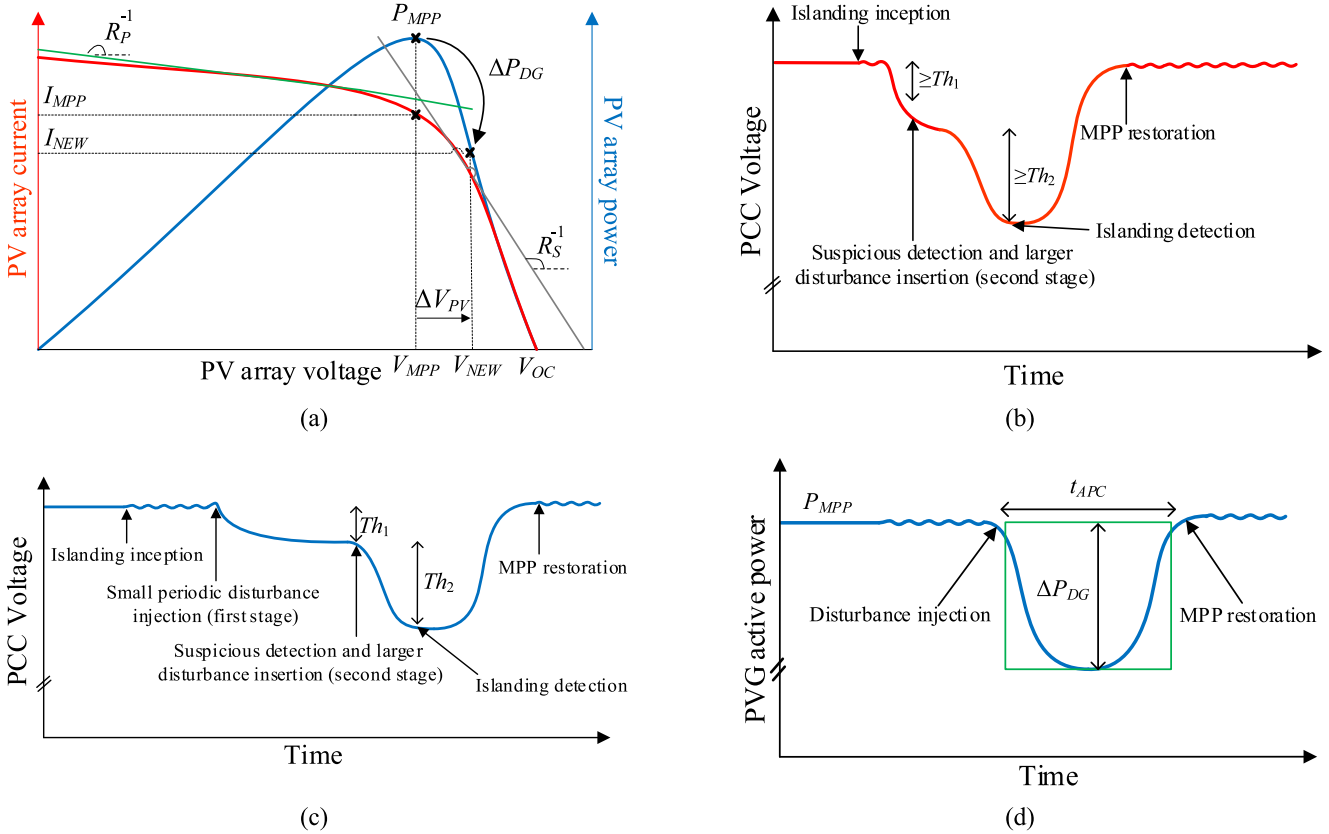

Fig. 2. Principle of the proposed method: a) PV array power vs. voltage characteristics, b) Performance in an island with small ΔP ($Th_1 \leq |\Delta V_{PCC}| < Th_2$), c) Performance in an island with zero/negligible ΔP ($|\Delta V_{PCC}| < Th_1$), d) Power estimation for determining the energy loss during curtailment.

Negligible/Zero $\Delta P/P_{DG}$: As illustrated in Fig. 2 (c), the last islanding scenario occurs with a slight PCC voltage change, $|\Delta V_{PCC}|< Th_1$. To classify such scenarios as suspicious, an active power mismatch is created by the disturbance injection of the first stage, described earlier. The created active power mismatch changes the PCC voltage so that a suspicious event is recognized. Therefore, the second disturbance is initiated and deviates the PV array voltage reference even more from the MPP, similar to the previous scenario. This curtails the PVG active power and reduces PCC voltage so that $|\Delta V_{PCC}|\geq Th_2$, hence classifying the islanding operation correctly.

Since the PCC voltage drops during short-circuit faults, an additional condition is established to discriminate such events and islanding. Similar to [21], a short-circuit fault is identified when PVG current output (I_{DG}) in each phase exceeds a threshold. As demonstrated later in non-islanding studies, this condition reliably distinguishes fault scenarios from islanding. It is worth saying that the user can freely choose the threshold for discriminating those events. As the current of grid-following solar inverters is usually limited to approximately the nominal value, it is set at 110 % in this paper.

The straightforward flowchart and inexpensive realization of the proposed method are depicted in Fig. 3. In Fig. 3 (b), the time delay to compute $|\Delta V_{PCC}|$ is set according to the system frequency, 20 ms in the studied system with 50 Hz. Furthermore, the disturbances are injected for 0.2 s to ensure MPP deviation without reducing the PVG active power output for a long time. In addition to the simple structure, this method only curtails the active power output, i.e., reducing the amplitude of the output current. Since it does not inject harmonic/sub-harmonic content, the PQ barely deteriorates. Also, the MPP is restored after islanding detection, as displayed in Fig. 2 (b) and (c). This provides a chance for PVG to contribute its maximum power to support the critical loads of the autonomous island. Finally, the method can be implemented into any PV module and inverter technologies, supporting a wide range of applications.

Thresholds determination

In the presented method, the PV array voltage disturbances (ΔV_{PV}^1 and ΔV_{PV}^2) should be accurately selected to meet the required APC for reliable detection of the suspicious and islanding events in the first and second stages, $|\Delta V_{PCC}|\geq Th_1$ and $|\Delta V_{PCC}|\geq Th_2$, respectively. In this

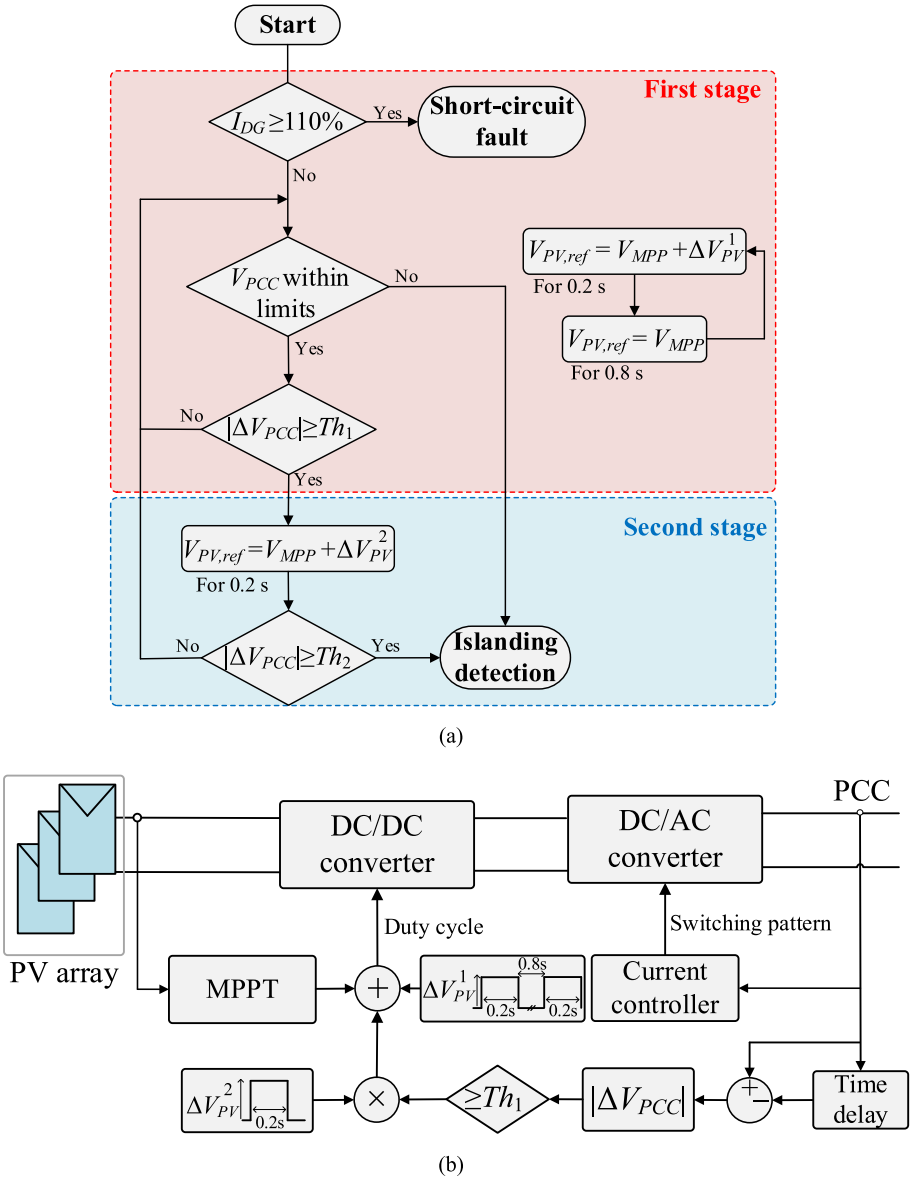

Fig. 3. Proposed methodology: a) Flowchart, b) Realization in existing VSI.

regard, the PV module current vs. voltage is considered in Fig. 2 (a). According to the well-known single-diode model of the PV module, the right- and left-hand sides of MPP can be modeled through two resistances: series (R_S) and parallel (R_P) [34]. Based on R_S, the relation of the open-circuit (OC), MPP, and new PV array's operating points can be expressed as:

$$R_S = \frac{V_{OC} - V_{MPP}}{0 - I_{MPP}} = \frac{V_{OC} - V_{NEW}}{0 - I_{NEW}} \tag{6}$$

where, the subscript "NEW" refers to the PV module operating point after disturbance injection, either in the first or second stage. By assuming $V_{OC}=k_1 \times V_{MPP}$ and $\Delta V_{PV}=k_2 \times V_{MPP}$, Eq. (7) can be simplified as follows:

$$\frac{(k_1 - 1)\, V_{MPP}}{I_{MPP}} = \frac{(k_1 - k_2 - 1)\, V_{MPP}}{I_{NEW}} \tag{7}$$

The current and power of the PV array after disturbance injection, I_{NEW} and P_{NEW}, can be expressed as follows:

$$I_{NEW} = I_{MPP} \frac{(k_1 - k_2 - 1)}{(k_1 - 1)} \tag{8}$$

$$\begin{aligned} P_{NEW} &= V_{NEW} I_{MPP} \frac{(k_1 - k_2 - 1)}{(k_1 - 1)} = (1 + k_2) V_{MPP} I_{MPP} \frac{(k_1 - k_2 - 1)}{(k_1 - 1)} \\ &= P_{MPP} \frac{(k_1 - k_2 - 1)(1 + k_2)}{(k_1 - 1)} \end{aligned} \tag{9}$$

This expression provides P_{NEW} for various PV array voltage disturbances (k_2). Also, k_1, which lies within the 1.2–1.3 range, can be found in the PV module datasheet presented by the vendor [35]. The relative active power curtailment ($\Delta P_{DG}/P_{MPP}$), applied in the two stages, can be finally computed as follows:

$$\frac{\Delta P_{DG}}{P_{MPP}} = \frac{P_{NEW} - P_{MPP}}{P_{MPP}} = \frac{(k_1 k_2 - 2k_2 - k_2^2)}{(k_1 - 1)} \tag{10}$$

By considering $\Delta P=\Delta P_{DG}$, Eqs. (3) and (10) quantify the required ΔV_{PV}^1 so that the $|\Delta V_{PCC}|$ surpasses the first threshold of the proposed IDT. It is worth pointing out that Eq. (3) is valid for two operating points in islanding operation when ΔP_{DG} substitutes ΔP. Thus, a similar approach can be used to define ΔV_{PV}^2. Also, when the microgrid includes other DG technologies, the PCC voltage shift caused by the PVG's active power curtailment may not surpass the preset threshold. Therefore, the injected disturbance to the PV array voltage should contain a margin to ensure that $|\Delta V_{PCC}|$ surpasses the corresponding threshold.

In this study, Th_1 and Th_2 are set at 2 % and 5 %, respectively. Hence, the $\Delta P/P_{DG} \geq -4.12$ % ensures PCC voltage drop by 2 % according to Eq. (3), i.e., a suspicious incident is detected by $|\Delta V_{PCC}| \geq 2\%$. Similarly, islanding events are classified when $\Delta P/P_{DG} \geq$-10.80 %, ensuring that the proposed imbalance causes $|\Delta V_{PCC}| \geq 5\%$. As demonstrated later, $k_2 = 2.1$ % and $k_2 = 3.8$ % selection ensure that the mentioned criterion is effective for suspicious and islanding detection in the first and second stages, respectively.

Real-time digital simulation results

The performance of the proposed IDT is assessed under various islanding and non-islanding scenarios for the modified IEEE 13-bus system, illustrated in Fig. 4. This multi-node test system is used in this paper to study several multi-PVG islanding and non-islanding events. Two PVGs with 300 kW and 100 kW nominal active power are simulated in real-time. An accurate single-diode model is exploited for the 400 W monocrystalline PV module of two PVGs, with V_{OC}=37.1 V, I_{SC}=13.7 A, V_{MPP}=30.7 V, and I_{MPP}=13.0 at the standard test condition with 1000 W/m^2 solar irradiance and 25 °C solar cell temperature [35]. Boost and buck-boost converters are integrated into the DC stage of the PVG_1 and PVG_2, respectively. The converter of PVG_1 exploits the perturb and observe MPPT technique, whilst the second one is equipped with incremental conductance, both working at 0.1 kHz frequency. These selections demonstrate the method's effectiveness, disregarding the DC/DC converter topology and MPPT algorithm. The DC power is converted to AC through a pulse width modulation in the DC/AC converter with a 2 kHz frequency. The PVGs are set to work at a unity power factor.

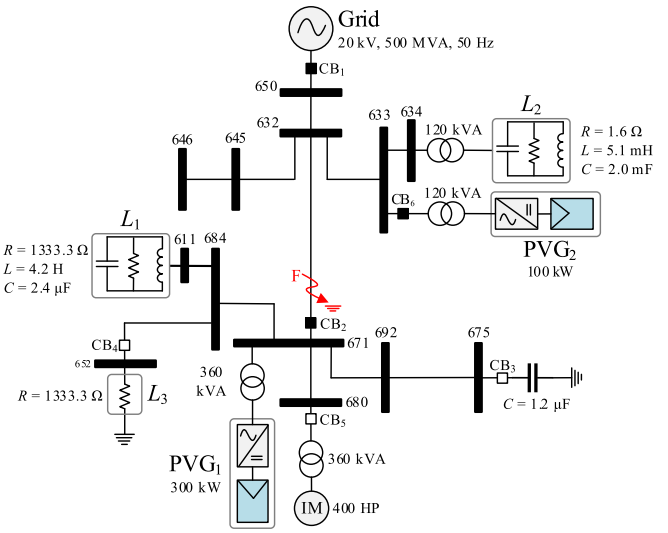

Fig. 4. Schematic of the studied microgrid, modified IEEE 13-bus system.

According to the employed PV module, $k_1 = V_{OC}/V_{MPP}$=1.21; hence, Eq. (10) can be used to obtain k_2 for $\Delta P/P_{DG}$=−4.12 % and −10.80 %. Two real roots for each equation are found; positive and negative, implying the right- and left-hand side of MPP. The one with positive k_2 is selected as the new PV array voltage is greater than the MPP one ($V_{NEW}>V_{MPP}$). Therefore, k_2 is 1.1 % and 2.8 % for $\Delta P/P_{DG}$=−4.12 % and −10.80 %, respectively. Considering a 1 % margin, the disturbance of the first and second stages is set at 2.1 % and 3.8 %. These selections ensure the PCC voltage change by more than 2 % and 5 % to fulfill the detection of the suspicious and islanding events in the first and second stages, respectively.

Two constant impedance loads are pinned at the first and second PCCs at 20 and 0.4 kV, respectively. These loads are tuned to simulate different active/reactive power mismatches and quality factors (Q_f), according to IEEE Std. 1547.1–2020 [36]. Also, the case study system considers a pure resistive load 3 (L_3), a capacitor bank, and an induction motor (IM) to simulate non-islanding disturbances. It is worth noting that PVGs, second load (L_2), and IM are connected to a 20 kV grid through 20/0.4 kV Dy11 transformers. Other industrial loads and capacitor banks are connected directly to the 20 kV distribution network.

Islanding events

Table 1 presents the islanding and non-islanding scenarios for the test system. According to IEEE Std. 1547.1–2020 [36], which defines the requirements and test procedures for verifying compliance with IEEE Std. 1547–2018 [5], the proposed IDT must be evaluated under negligible/zero power mismatches, less than 2 % and 5 % for active and reactive power, respectively. In addition, two cases with small active power mismatches are simulated. Hereby, the performance of the presented technique is studied when the second stage disturbance is stimulated without the necessity of the first stage disturbance. Finally, the effectiveness of the proposed IDT under multi-DG and various load quality factors is analyzed.

Regarding the detection time, the worst case occurs when the islanding incepts just after the first disturbance injection. Since this disturbance is periodically triggered for 0.2 s within a 1 s period, all

Table 1
Results for various islanding and non-islanding scenarios.

Islanding scenarios				
Case no.	**Test Description**	P_L+jQ_L (kW, kVAr)	ΔP+$j\Delta Q$ (%)	**Detection time (ms)**
1	Single-PVG islanding by opening CB_2 (P_{DG1} = 300 kW; Q_{DG1} = 0 kVAr)	285 + j0	+5 + j0	**340**
2		294 + j0	+2 + j0	**1191**
3		300 + j6	0 + j2	**1063**
4		300 + j0	0	**1062**
5		300-j6	0-j2	**1196**
6		306 + j0	−2 + j0	**1053**
7		315 + j0	−5 + j0	**377**
8	Various Q_fs by opening CB_2 (P_{DG1} = 300 kW; Q_{DG1} = 0 kVAr)	300 + j0 (Q_f = 1.0)	0	**1071**
9		300 + j0 (Q_f = 2.5)		**1065**
10		300 + j0 (Q_f = 4.0)		**1082**
11		300 + j0 (Q_f = 8.0)		**1101**
12	Multi-PVG by opening CB_1 (P_{DG1} = 300 kW; Q_{DG1} = 0 kVAr; P_{DG2} = 100 kW; Q_{DG2} = 0 kVAr)	294 + j0; 98 + j0	+2 + j0	**1042; 1033**
13		300 + j6; 100 + j2	0 + j2	**1030; 1030**
14		300 + 0j; 100 + j0	0	**1071;1087**
15		300-j6; 100-j2	0-j2	**1036; 1036**
16		306 + 0j; 102 + 0j	−2 + j0	**1033; 1027**

Non-islanding disturbances				
Case no.	**Test Description**	**Maximum $\lvert\Delta V_{PCC}\rvert$**		**Method triggers?**
		[1.0, 1.2] s* (%)	**>1.2 s** (%)**	
17	150 kVAr capacitor connection by closing CB_3	2.4	0.2	**No**
18	300 kW third load connection by closing CB_4	0.8	0.1	**No**
19	DG_2 trip by opening CB_6	2.6	0.2	**No**
20	400 HP IM start by closing CB_5***	2.3	0.2	**No**
21	Single-phase-ground fault (0.1 Ω resistance)	97.0	0.5	**No**
22	Single-phase-ground fault (10 Ω resistance)	13.7	0.4	**No**
23	Three-phase-ground fault (0.1 Ω resistance)	95.5	0.6	**No**
24	Three-phase-ground fault (10 Ω resistance)	13.7	0.4	**No**

* During non-islanding event/first stage disturbance; ** During second stage disturbance injection.
*** Stator impedance = 0.042 + j0.087 pu, Rotor impedance = 0.050 + j0.066 pu, Magnetizing reactance = 2.974 pu

islanding cases are simulated at t = 0.3 s to this end.

As the initial study, Cases 1–7 with small and negligible active or reactive power mismatches and Q_f = 1 in a single-PVG island are examined. These power imbalances are simulated by adjusting the RLC parameters of the first load (L_1). The results of these scenarios, including a reference of V_{PV} ($V_{PV,ref1}$) and P_{DG1} (for Case 4), and the PCC voltage of all cases are illustrated in Fig. 5 (a) and (b), respectively.

The outputs endorse the above theoretical explanation about the relationship between active power mismatch and PCC voltage. According to Eq. (3), the ΔV_{PCC} is 2.6 % and −2.4 % in Cases 1 and 7, with +5 % and −5 % active power mismatches, respectively. The second stage disturbance causes a V_{PCC} drop of more than 5 % in 340 ms and 377 ms. Thus, the second disturbance is activated before the first stage disturbance injection. In other cases, with a negligible/zero $\Delta P/P_{DG}$, however, the PCC voltage variation is smaller than Th_1 = 2 %. The suspicious event is thereby identified using the first stage disturbance during t = [1, 1.2] s. When a suspicious event is recognized, either by injection of the first disturbance or not, the PVG active power curtailment in the second stage reduces the PCC voltage for all cases so that $|\Delta V_{PCC}| \geq 5$ %. Therefore, the islanding condition is identified within ~ 1.2 s, and the NDZ is fully eliminated.

In the literature, the performance of IDT for various quality factors has been studied. Therefore, the tests are extended in Cases 8–11 for Q_f = 1.0, 2.5, 4.0, and 8.0 with zero power mismatch. The results in Fig. 5 (c) corroborate the successful islanding detection of these cases within 1.1 s. Similar to Case 4 with ΔP=0, this IDT identifies suspicious events by the imposed small disturbance in the first stage. Afterwards, the second stage injected disturbance reduces the PCC voltage so that the islanding detection threshold (Th_2) is surpassed.

Typically, commercial and power plant PV projects are composed of several parallel VSIs connected to the same/nearby PCC(s). The interaction between the VSIs' control is crucial in this situation, especially for active and hybrid IDTs. The imposed disturbance may counteract the imbalance introduced by other DGs, missing islanding events, e.g., the voltage positive feedback in [37]. The performance of the proposed IDT is therefore evaluated in such multi-PV scenarios. In Cases 12–16 of Table 1, 0 % and ± 2 % active power imbalances are simulated by adjusting L_1 and L_2. The voltage at the output terminal of PVG_1 and PVG_2 for Cases 12, 14, and 16 is illustrated in Fig. 5 (d). What stands out from the outputs is that after island formation at t = 0.3 s, both PVGs' active power is curtailed when the suspicious islanding event is classified. The voltage at both PVGs' terminal drops and islanding is identified by $|\Delta V_{PCC}| \geq Th_2$ criterion within ~ 1.1 s.

Non-islanding scenarios

In addition to an accurate detection of islanding events, the proposed method should not exhibit false operation in non-islanding disturbances. Thus, several non-islanding circumstances are simulated in real-time, as shown in Table 1. These events are simulated at t = 1 s by opening/closing the corresponding CB.

Cases 17–20 investigate four types of non-islanding events that can cause a voltage deviation. Cases 17 and 18 explore the effect of switching a capacitor and a resistive load, respectively. The impact of PVG active power curtailment on V_{PCC} is expected to be negligible under these circumstances as the grid controls the PCC. This behavior is readily seen in the V_{PCC} variation in Fig. 6 (a) and maximum $|\Delta V_{PCC}|$ in Table 1, computed during the first and second disturbance injections.

In addition, single/three-phase-ground short-circuit faults with different fault resistance values are simulated in the distribution line, close to bus 671 (Fig. 4). The fault is initiated at t = 1 s and cleared after 0.15 s. The outputs in Fig. 6 (b) for Case 22 indicate a notable V_{PCC} change during the fault occurrence. Nevertheless, the current of the faulty phase(s) in Fig. 6 (b) surpasses the established condition, and such events are classified as faults.

From the outputs, it is evident that the proposed IDT successfully

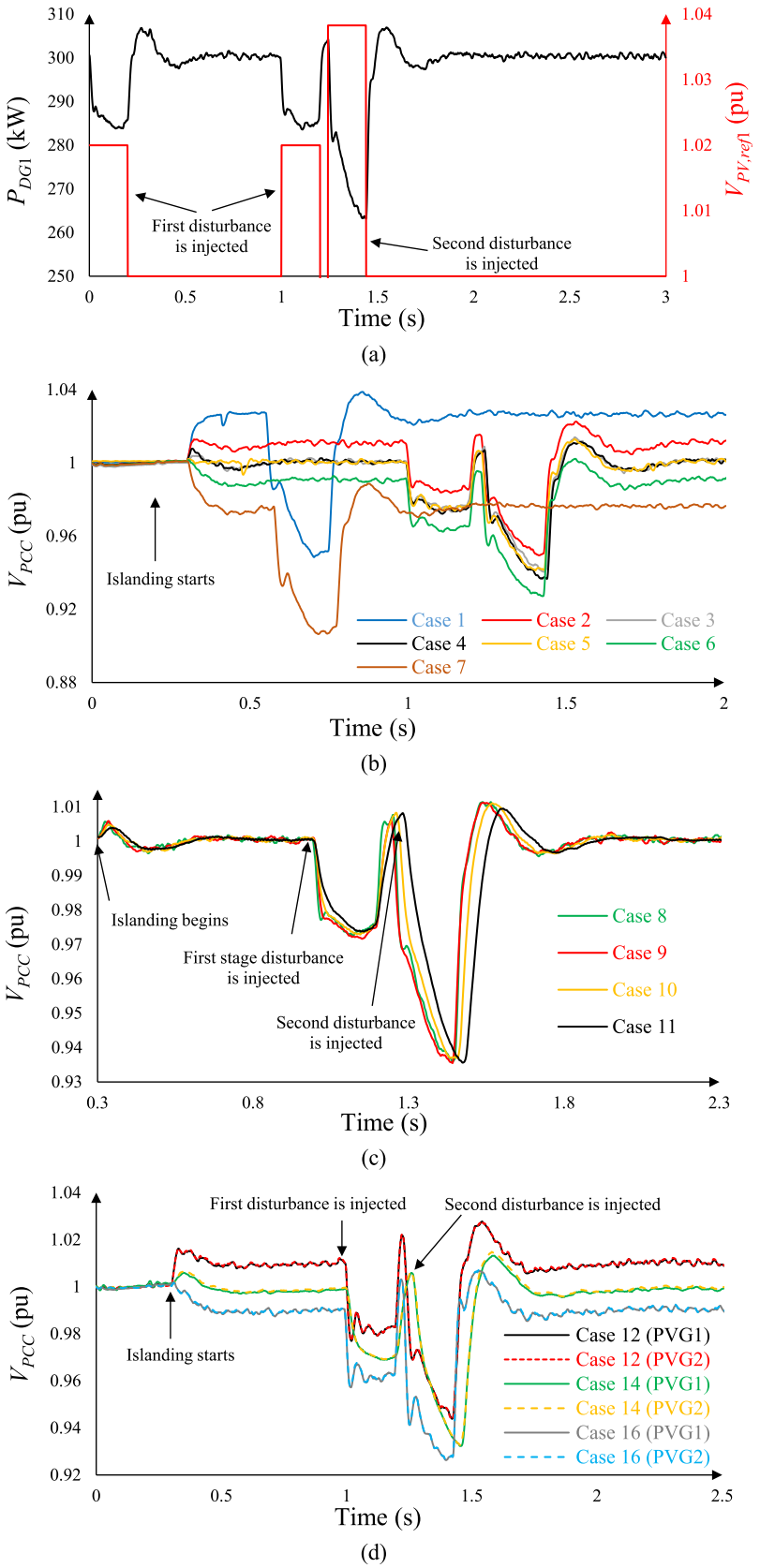

Fig. 5. Performance of the proposed IDT: a) In a balanced island (Case 4), b) Various active power mismatches (Cases 1–7), c) Various load quality factors of a balanced island (Cases 8–11), d) Multi-PVG cases with zero/small active power mismatches.

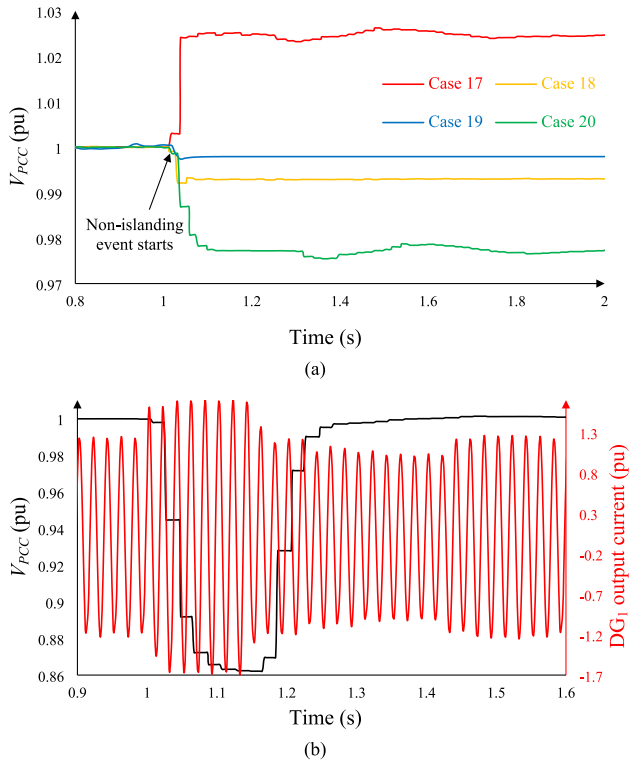

Fig. 6. Performance of the proposed IDT in non-islanding disturbances: a) PCC voltage, b) Outputs of Case 22 fault.

detects all islanding events for both single and multi-PVG cases. For a zero/very small power imbalance, the detection time is at most 1.196 s. Since the suspicious events are identified before injecting the first stage disturbance, the detection time decreases to less than 0.4 s for scenarios with larger imbalances, e.g., Cases 1 and 7.

Comparison with existing methods for PV-based microgrids

This section highlights the overall outstanding performance of the proposed active IDT through a comparison with recently published IDTs. As summarized in Table 2, paramount features are analyzed, including NDZ, detection time, PQ degradation, thresholds determination, structure complexity, and the ability to seamlessly transition to a standalone mode as voltage and frequency do not fall significantly [32].

Based on the comparison, it is found that:

- Unlike most classical methods (e.g., multiple relays [10], rate of change of superimposed impedance [11], and impedance angle [14]) and modern local IDTs (e.g., improved active phase shift [18], positive feedback of negative sequence current injection [23], and switching of capacitor [26] and inductor [27]), the proposed disturbance in the first stage eliminates the NDZ. Thus, it can be commercialized in practice, according to [5].
- Zero NDZ is fulfilled here at the cost of a longer detection time. Although this time is greater than most local IDTs, it is lower than the maximum allowable time suggested by [5].
- Contrary to most phase shift [22,23] and frequency shift [24] active methods, the proposed IDT does not inject a signal that constantly causes power quality issues.
- Most modern IDTs still suffer from moderate/high threshold dependency on the studied DG/microgrid. Conversely, the threshold settings of the presented method only rely on the V_{OC}/V_{MPP} ratio, irrespective of the microgrid characteristics. This feature ensures reliable performance, even when the microgrid parameters/structure change.
- Most local-based techniques with more complex strategies and higher implementation costs are presented to mitigate the NDZ and detection time (e.g., machine learning-based IDTs [15,16]), while these goals are achieved in the proposed method with a simple and inexpensive structure.
- Finally, some IDTs introduce active/reactive power imbalances by adding passive elements [26,27] or altering the available power from the primary source for islanding detection purposes [20,21], thus causing the disconnection of the microgrid for under/over voltage/frequency. However, as shown in the analysis, this method recovers the MPP in 200 ms after islanding detection, facilitating the stable operation of the autonomous microgrid.

Discussions

The proposed IDT is structured to curtail the PVG active power output for successful suspicious and islanding detections in the first and second stages. Nonetheless, this zero NDZ is achieved at the cost of a drop in efficiency. In this part, the effect of imposed disturbances on the efficiency of the PVG is analytically assessed.

Table 2
Comparison with existing islanding detection techniques developed for PV systems.

Methodology		NDZ	Detection time	PQ deg.	Threshold dependency	Cost and complexity	Seamless transition
Remote	Communication-based [8,9]	Zero	Low	Zero	None	High	Yes
Passive	Five relays combination [10]	Zero	Medium	Zero	High	High	Yes
	Rate of change of impedance [11]	Small	Low	Zero	High	Medium	Yes
	Superimposed positive and negative impedances [12]	Small	Low	Zero	High	Medium	Yes
	Phasor measurement units for impedance-based index [13]	Small	Low	Zero	High	High	Yes
	Impedance angle [14]	Small	Low	Zero	High	Medium	Yes
	Pattern recognition [15–17]	Zero/ Small	Low	Zero	High	High	Yes
Active	Absolute negative voltage [21]	Zero	Medium	Small	Medium	Medium	No
	Improved active phase shift [22]	Small	Low	Medium	Medium	High	No
	Negative sequence current injection [23]	Small	Low	Medium	High	Medium	No
	d-axis current injection [20]	Small	Low	Medium	Medium	Medium	No
	Frequency feedback into the injected reactive power disturbance [24]	Small	Low	Medium	Medium	Medium	No
Hybrid	RC load connection [26]	Small	Low	Small	High	Medium	Yes
	Rate of change of voltage and power [25]	Small	Low	Small	Medium	Medium	Yes
	Parallel capacitor switching [27]	Small	Low	Small	High	Medium	Yes
	RoCoF and SFS [28]	Small	Low	Medium	Medium	Medium	No
	THD and absolute frequency deviation [29]	Small	Low	Small	High	Medium	Yes
Active	Proposed technique	Zero	Medium	Small	Low	Low	Yes

According to Fig. 2 (d), the loss of efficiency due to the employed APC in both stages can be expressed as:

$$Loss\ of\ Efficiency = \frac{\Delta P_{DG}}{P_{MPP}} \times \frac{t_{APC}}{T} = \frac{(k_1 k_2 - 2k_2 - k_2^2)}{(k_1 - 1)} \times \frac{t_{APC}}{T} \quad (11)$$

Here, Fig. 2 (d) shows the shape of the curtailed active power. This APC over time is estimated by a rectangle, displayed by solid green lines. Also, t_{APC} and T denote the time duration of APC and its period, 0.2 s and 1 s for the first stage. The selected disturbance of the first stage for the studied PV module (i.e., $k_2 = 2.1$ %) leads to $\Delta P_{DG}/P_{MPP} = -8.1$ %. The efficiency drop caused by the first stage is 1.62 % under $t_{APC} = 0.2$ s and $T = 1$ s, implying a slight effect of the imposed periodical disturbance on the PVG efficiency.

Similarly, the efficiency drop in the second stage can be quantified by Eq. (11), $\Delta P_{DG}/P_{MPP} = -15.0$ % under $k_2 = 3.8$ %. The disturbance is triggered in this stage when the event is suspected. Therefore, T depends on the time interval between two suspicious events. For example, when the second stage disturbance is triggered every minute, the efficiency drop is 15.0 %×(0.2 s ÷ 60 s) = 0.05 %. Hence, the effect of this disturbance would be even slighter than the first stage as it is solely activated during suspicious events.

Conclusion and future works

This paper proposes a two-stage methodology for detecting the islanding operation of PV-rich microgrids. The proposed method is simple and offers zero NDZ with a fast decision-making process. Both stages of this active power curtailment-based technique include a disturbance injection into the MPPT algorithm. These disturbances reduce the PVG active power output, enlarging the microgrid's mismatch between generation and demand, even on a perfectly balanced island. Therefore, the first stage identifies the suspicious islanding events in small power mismatch scenarios, while the second stage is designed to classify islanding conditions with a greater PCC voltage drop.

The successful performance of the proposed technique is demonstrated by using a modified version of the IEEE 13-bus system with 100 kW and 300 kW PVGs implemented in an RTDS. The capacitor bank, induction motor, and additional load are modeled and switched ON to simulate non-islanding disturbances. The results endorse an adequate operation during such events without causing undesired tripping. Despite the slight effect on PVG's efficiency (less than 1 % decrease), it is found that:

- The method classifies precisely all islanding (within 1.2 s) and non-islanding scenarios.
- Contrary to most active and hybrid IDTs, this method does not enlarge harmonics/subharmonics amplitude; hence, its adverse effect on the PQ is negligible.
- The proposed method enhances the presently available IDTs for microgrids with large penetration of PV units, enabling them to transition to the autonomous mode once islanded has been identified.
- The proposed IDT's structure is simple, and its thresholds are analytically set without necessitating microgrid data. This outstanding overall performance and straightforward realization make the proposed IDT an efficient solution for PV-based microgrids.

In future works, the proposed methodology can be realized by considering non-uniform solar radiation and grid-forming VSIs. The analytical expressions are based on uniform received irradiance and do not cover the partial shading conditions. Thus, this IDT can be fostered to consider the PV systems with likely partial shading occurrence. The latter can also be addressed by substituting the VSIs operating as grid-following in the studied microgrid for VSIs operating in grid-forming ones.

Since the proposed method reduces slightly the PVG efficiency, an economic analysis can be conducted as future research to quantify the financial impact. In this regard, the cost of reduced energy by APC can be determined in net metering or feed-in tariff policy, i.e., calculating the loss of revenue generated by the proposed APC on the PVG. On the other hand, since the NDZ is eliminated, it is proven that the PVG can operate safely and identify all islanding scenarios. Therefore, the cost of NDZ elimination can also be determined by considering the probability of occurrence of both islanding and non-islanding events, as listed in Table 1. As a future study, this interesting analysis reveals the method's advantages from the economic perspective.

CRediT authorship contribution statement

Reza Bakhshi-Jafarabadi: Writing – original draft, Validation, Methodology, Conceptualization. **Alexandre Serrano Fontova:** Writing – original draft, Validation, Methodology. **Marjan Popov:** Writing – review & editing, Supervision, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

References

[1] Kiehbadroudinezhad M, Hosseinzadeh-Bandbafha H, Rosen MA, Kumar Gupta V, Peng W, Tabatabaei M, et al. The role of energy security and resilience in the sustainability of green microgrids: Paving the way to sustainable and clean production. Sustain. Energy Technol. Assessm. 2023;60. Doi: 10.1016/j.seta.2023.103485.
[2] Kataray T, Nitesh B, Yarram B, Sinha S, Cuce E, Shaik S, et al. Integration of smart grid with renewable energy sources: Opportunities and challenges – A comprehensive review. Sustain. Energy Technol. Assessm. 2023;58. Doi: 10.1016/j.seta.2023.103363.
[3] Bakhshi-Jafarabadi R, Sadeh J, Serrano-Fontova A, Rakhshani E. Review on islanding detection methods for grid-connected photovoltaic systems, existing limitations and future insights. IET Renewable Power Generation 2022;16. Doi: 10.1049/rpg2.12554.
[4] Serrano-Fontova A, Casals Torrens P, Bosch R. Power quality disturbances assessment during unintentional islanding scenarios. a contribution to voltage sag studies. Energies (Basel) 2019;12. Doi: 10.3390/en12163198.
[5] Association IS. IEEE Std. 1547-2018. Standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces. 2018.
[6] Rodríguez-Amenedo JL, Gómez SA, Zubiaga M, Izurza-Moreno P, Arza J, Fernández JD. Grid-forming control of voltage source converters based on the virtual-flux orientation. IEEE Access 2023;11:10254–74. https://doi.org/10.1109/ACCESS.2023.3240516.
[7] Fazal S, Enamul Haque M, Taufiqul Arif M, Gargoom A, Oo AMT. Grid integration impacts and control strategies for renewable based microgrid. Sustainable Energy Technol Assess 2023;56:103069. https://doi.org/10.1016/J.SETA.2023.103069.
[8] Poluektov A, Pinomaa A, Romanenko A, Ahola J, Kosonen A. Sensitivity analysis of a PLC-based DSSS anti-islanding system in power distribution grids. International J Elect Power Energy Syst 2019;113. Doi: 10.1016/j.ijepes.2019.06.022.
[9] Bayrak G, Kabalci E. Implementation of a new remote islanding detection method for wind-solar hybrid power plants. Renew Sustain Energy Rev 2016; 58. Doi: 10.1016/j.rser.2015.12.227.
[10] Banu IV, Barkat F, Istrate M, Guerrero JM, Culea G, Livinti P, et al. Passive anti-islanding protection for three-phase grid-connected photovoltaic power systems. Int J Electr Power Energy Syst 2023;148. Doi: 10.1016/j.ijepes.2023.108946.
[11] Tadikonda N, Kumar J, Mahanty RN. A technique for detection of islanding in a microgrid on the basis of rate of change of superimposed impedance (ROCSI). Electric Power Syst Res 2022;206. Doi: 10.1016/j.epsr.2022.107838.
[12] Bharti IP, Singh NK, Gupta OH, Singh AK. Unplanned islanding detection of renewable energy sources using sequence impedance with zero NDZ. Electr Eng 2024. https://doi.org/10.1007/s00202-023-02176-9.
[13] Xing J, Mu L. A novel islanding detection method for distributed PV system based on μpMUs. IEEE Trans Smart Grid 2023;14. Doi: 10.1109/TSG.2023.3236790.

[14] Wang C, Xu H, Yang F, Yang Z, Chen H, Chen Y, et al. Measurement of impedance angle for anti-islanding protection in multi-source distribution network. Energy Rep 2024;11:3022–36. https://doi.org/10.1016/j.egyr.2024.02.048.
[15] Nsaif YM, Hossain Lipu MS, Hussain A, Ayob A, Yusof Y. Island detection for grid connected photovoltaic distributed generations via integrated signal processing and machine learning approach. Int J Elect Power Energy Syst 2023;154. Doi: 10.1016/j.ijepes.2023.109468.
[16] Chen L, Dong X, Wang B, Shang L, Liu C. An edge computing-oriented islanding detection using differential Entropy and multi-support vector machines. IEEE Trans Smart Grid 2023. https://doi.org/10.1109/TSG.2023.3288361.
[17] Hussain A, Mirza S, Kim CH. Islanding detection and classification of non-islanding disturbance in multi-distributed generation power system using deep neural networks. Elect Power Syst Res 2023; 224. Doi: 10.1016/j.epsr.2023.109807.
[18] Chen H, Ye J. An improved active phase-shift islanding detection method based on fuzzy adaptive PID algorithm. Int J Power Energy Syst 2023;43. Doi: 10.2316/J.2023.203-0464.
[19] Mostaro M, Monteiro HLM, Dias FM, Silva LRM, Duque CA. Islanding detection based on impedance estimation using small signal injection. Int J Elect Power Energy Syst 2022; 139. Doi: 10.1016/j.ijepes.2022.107983.
[20] Hasanisadi M, Khoei M, Tahami F. An improved active islanding detection method for grid-connected solar inverters with a wide range of load conditions and reactive power. Electric Power Syst Res 2023;224. Doi: 10.1016/j.epsr.2023.109714.
[21] Bakhshi-Jafarabadi R, Sadeh J. New voltage feedback-based islanding detection method for grid-connected photovoltaic systems of microgrid with zero non-detection zone. IET Renew Power Generat 2020;14. Doi: 10.1049/iet-rpg.2019.1174.
[22] Gulipalli SC, Chou PH, Chen YM, Liu TI, Chu CC. Frequency-locked loop based new automatic phase-shift method for active islanding detection of three-phase microgrid. IEEE Trans Ind Appl 2023;59. Doi: 10.1109/TIA.2023.3281537.
[23] Shamseh MB, Inzunza R, Ambo T. A novel islanding detection technique based on positive-feedback negative sequence current injection. IEEE Trans Power Electron 2022;37. Doi: 10.1109/TPEL.2022.3146342.
[24] Peng T, Bai C, Song X, Duan S. An islanding detection method based on the reactive power disturbance for multiple inverter-based DG systems. IEEE Trans Ind Electron 2024;71:3253–63. https://doi.org/10.1109/TIE.2023.3274875.
[25] Seyedi M, Taher SA, Ganji B, Guerrero J. A hybrid islanding detection method based on the rates of changes in voltage and active power for the multi-Inverter systems. IEEE Trans Smart Grid 2021;12. Doi: 10.1109/TSG.2021.3061567.
[26] Serrano-Fontova A, Martinez JA, Casals-Torrens P, Bosch R. A robust islanding detection method with zero-non-detection zone for distribution systems with DG. Int J Electr Power Energy Syst 2021; 133. Doi: 10.1016/j.ijepes.2021.107247.
[27] Rostami A, Jalilian A, Zabihi S, Olamaei J, Pouresmaeil E. Islanding detection of distributed generation based on parallel inductive impedance switching. IEEE Syst J 2020;14:813–23. https://doi.org/10.1109/JSYST.2019.2923289.
[28] Biyya I, Oubrahim Z, Abbou A. Fast hybrid islanding detection for DGs with inverters using maximum likelihood-based ROCOF and SFS. Comput Electr Eng 2024;116:109176. https://doi.org/10.1016/j.compeleceng.2024.109176.
[29] Patekar RS, Panigrahi BK. A novel two-stage hybrid anti-islanding protection scheme and non-detection zones analysis of inverter-based generations. IEEE J Emerg Select Top Indust Electron 2024:1–12. https://doi.org/10.1109/JESTIE.2024.3381007.
[30] Operating instructions for Fronius Tauro 50-3/Eco 100-3 2024. www.fronius.com/~/downloads/Solar%20Energy/Operating%20Instructions/42,0426,0307,EN.pdf (accessed February 12, 2024).
[31] Manual of Kaco blueplanet 87–165 TL3 2024. www.kaco-newenergy.com/downloads (accessed February 12, 2024).
[32] Datta A, Ray A, Mukherjee D, Saha H. Selection of islanding detection methods based on multi-criteria decision analysis for grid-connected photovoltaic system applications. Sustain Energy Technol Assessm 2014;7. Doi: 10.1016/j.seta.2014.04.003.
[33] Zepter JM, Engelhardt J, Ledro M, Gabderakhmanova T, Marinelli M. Experimental assessment of active power control of distributed generation units. Sustainable Energy Technol Assess 2023;60:103500. https://doi.org/10.1016/J.SETA.2023.103500.
[34] Deotti LMP, da Silva IC. A survey on the parameter extraction problem of the photovoltaic single diode model from a current–voltage curve. Solar Energy 2023; 263. Doi: 10.1016/j.solener.2023.111930.
[35] BLK MG11S solar module datasheet n.d. www.q-cells.co.uk/private-customers/solar-panels (accessed February 18, 2024).
[36] IEEE Std. 1547.1-2020. IEEE standard conformance test procedures for equipment interconnecting distributed energy resources with electric power systems and associated interfaces. 2020.
[37] Samui A, Samantaray SR. An active islanding detection scheme for inverter-based DG with frequency dependent ZIP–Exponential static load model. Int J Electr Power Energy Syst 2016;78:41–50. https://doi.org/10.1016/j.ijepes.2015.11.054.