Power Supply for Multiple Pickup IPT System in Lighting Applications

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Challenge the future

Power Supply for Multiple Pickup IPT System in Lighting Applications

by

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ABSTRACT

Inductive power transfer (IPT) has become a hot topic and is supposed to have a wide range of application in the future. This thesis focuses on the IPT system with multiple pickups in the lighting application. A multiple pickup system can power more than one pickup at the same time and the power consumption varies with a different number of pickups connecting in the circuit. A problem with the multiple pickup system is that at light load the power supply consumes a large amount of reactive power for a small active power demand. The aim of the design is to build a power supply with a constant current output. The designed circuit is supposed to reduce the reactive power demand and keep zero voltage switching (ZVS) in all range of load.

This thesis selects the half bridge inverter and LCL-T network as the topology. The characteristic of the LCL-T network is first analyzed under first harmonic approximation. The trade off between the constant current output, reactive power demand, and ZVS is interpreted. The system is proposed to work at a higher frequency for a light load. In addition, the effects of higher order harmonics on the switching current and apparent power are also given in the form of calculations. Subsequently, the parameters in the topology of the half bridge inverter and LCL-T network are determined. The control circuit is built to realize automatic frequency switching according to the load condition. The next step is to simulate the designed circuit in LTspice and construct it in the lab. The result of simulation and experiment verifies that the reactive power demand is reduced with a higher frequency at light load. Constant current output and ZVS are ensured at the same time in all range of load. But the efficiency of the system does not show a clear improvement since the loss is dominated by the cable loss, which is determined by the requirement of cable current and the pickup design.

Keywords: inductive power transfer, LCL-T network, constant current output, apparent power reduction, zero voltage switching

PREFACE

It is an unforgettable experience to do my master thesis in Philips Lighting. I would like to express my sincere gratitude to the people who gave their assistance during the thesis.

First, I would like to thank D. Pardijs for offering me this opportunity to do my work in Philips Lighting. I would also like to thank Dr. B. Ackermann for supervising. Dr. B. Ackermann gave me endless academic assistance during the whole work and was patient for each of my question. Without his supervision and experienced guidance, it would be impossible for me to finish this thesis.

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I would like to offer my deepest gratitude to my parents and my girlfriend. I am so grateful that my parents could support my decisions without any hesitation. Jie, it was nice to have you around for the two years in the Netherlands. The Netherlands is our lucky land.

Thank you all!

Donghao Wu
Eindhoven, September 2017

CONTENTS

1

INTRODUCTION

1.1. INDUCTIVE POWER TRANSFER SYSTEMS

Inductive power transfer (IPT) systems [1] transfer electrical power without physical contact between source and load by first converting electrical energy to magnetic energy and then back to electrical energy. The IPT systems have some apparent advantages over traditional ways of charging. They have higher security performance because there is no naked conductor exposed to the outside. This is preferable in many harsh situations, such as the underwater and humid environment. They are more user-friendly. The charging process is simplified and does not need connectors. It also simplifies the way of system installation. This provides extra value for the situation that time of installation and repair is limited, such as tunnel lights and signal lights in the airport.

1.1.1. PRINCIPLE

The fundamental operating principle derives from Faraday's law. Power is transferred between changing magnetic field and alternating current, similar as a transformer. As shown in Fig. 1.1, AC current in the transmitter coil generates a time-varying magnetic field, which induces an alternating voltage in the receiver coil. The block diagram of an IPT system is depicted in Fig. 1.2. The power factor corrector (PFC) takes power from AC mains and provides a constant dc voltage at the output. The switched mode power supply inverts the constant DC voltage to alternating current, which is injected to the compensation circuit and primary coil. At the coupled coils, power transfers wirelessly from a primary coil to secondary coil taking the changing magnetic field as a medium. At last, power flows to the load at the secondary side. There may be secondary compensation and rectifier present before the load.

1.1.2. CLASSIFICATION

The classification of IPT systems can be based on the pickup number and the degree of coupling. A single pickup IPT system has one secondary winding. The power transfers between primary winding and secondary winding. A multiple pickup IPT system has multiple secondary windings and the primary winding is always in the form of a cable or track. The degree of coupling describes how strong it is between primary winding and secondary winding(s). Fig. 1.3 depicts the classification of IPT systems.
Fig. 1.4(a) is an example of a strong coupling single pickup IPT system [2]. It is a tight mounting rotatable transformer with $100\mu m$ air gap and introduced as a novel power supply for robot system. It is used to replace movable cables. Fig. 1.4(b) is a schematic of wireless charging mobile phone [3]. The magnitude of air gap is in the order of millimeters.

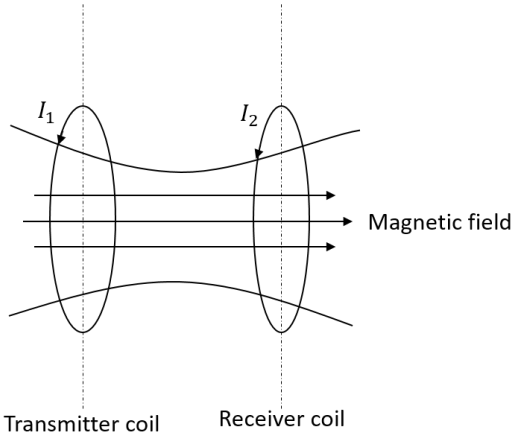


Figure 1.1: Energy transfers between coils

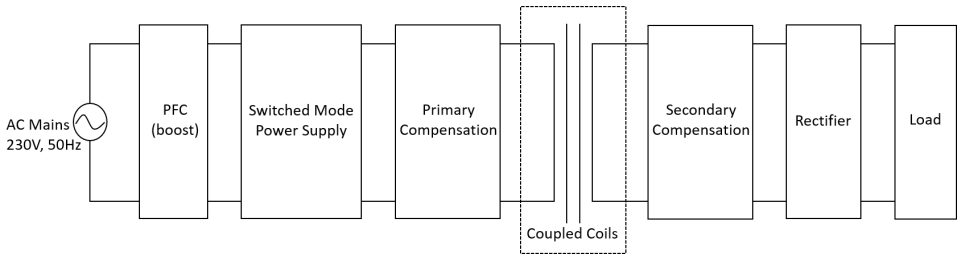


Figure 1.2: A block diagram of IPT system

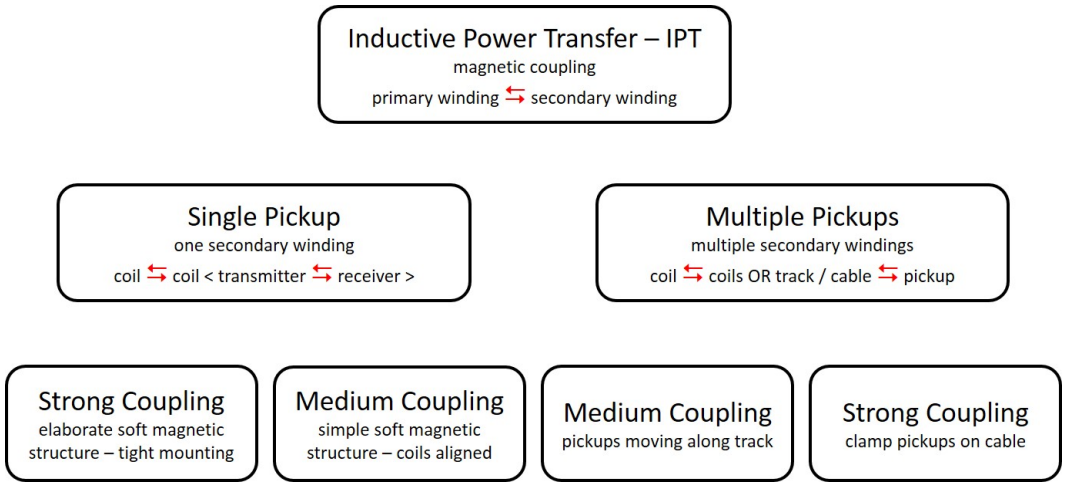
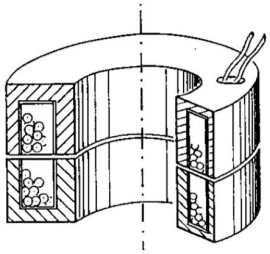
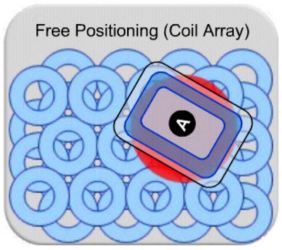


Figure 1.3: The classification of IPT systems



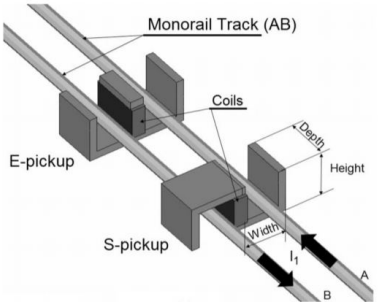
(a) Rotatable transformer in robot system [2]



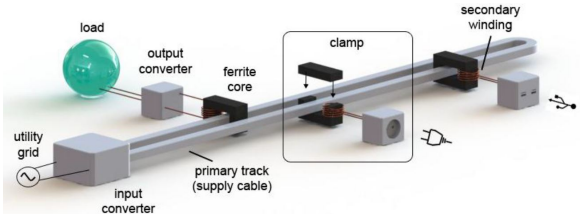
(b) Wireless charging Phone [3]

Figure 1.4: Examples of single pickup systems

For multiple pickup IPT systems, there are two common types: monorail with movable pickup and long cable with clamped pickup. Fig. 1.5(a) is the monorail type. It is widely used in the IPT system of automated guided vehicles in industrial plant [4]. Fig. 1.5(b) is an example of clamped pickup used in IPT residential system [5]. The pickup is clamped to the cable tightly. Clamped pickups are proposed for lighting applications and will be discussed in more details in chapter 1.2.1. The coupling in the clamped pickup is relatively stronger than in movable pickup.



(a) Monorail IPT system [4]



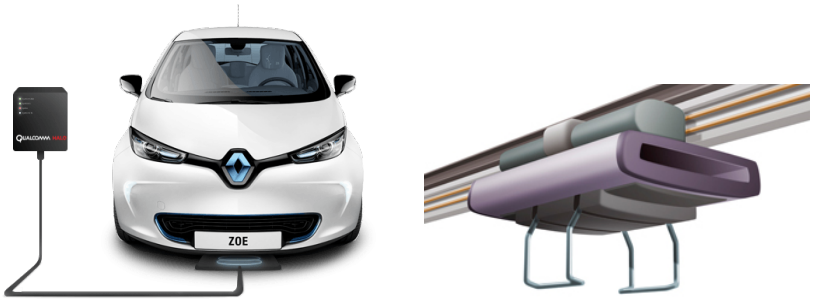
(b) E-Snake inductive system concept [5]

Figure 1.5: Example of multiple pickup system

There are already numerous applications in the market:

- Single pickup system
  - Qualcomm Halo for electric vehicles charging
  - Samsung wireless charger for smartphones
- Multiple pickup system
  - Clamped pickup systems: 3i-Innovation, Isotera, Greengage Lighting, Transfotec
  - Movable pickup systems: Vahle, Daifuku, SEW Eurodrive, Conductix

The Qualcomm Halo [6] declares that it delivers high energy-transfer efficiency higher than 90% and high power – 3.3 kW and 6.6 kW - even if pads are misaligned. Vahle and Daifuku [7] provide IPT system used for transport system in industrial plants.



(a) Qualcomm Halo [6]

(b) Daifuku's noncontact power supply [7]

Figure 1.6: Applications of IPT system

1.1.3. OTHER WIRELESS POWER TRANSFER SYSTEMS

Besides inductive power transfer, there are other wireless power transfer technologies. They can be categorized as following based on their working principle:

- Capacitive power transfer (CPT)
  In CPT system, power transfers wirelessly between electrodes of capacitor through the electrical field between capacitor electrodes. A block diagram of a CPT system is depicted in Fig. 1.7. A high frequency voltage applied to the transmitting plate can generate an oscillating electric field, which will induce an alternating voltage on the receiving plate. In CPT systems, the electrical field is largely confined between the plates of the capacitor, so there are less interferences compared to IPT system [1]. However, electric fields can interact with most materials and are dangerous for materials near the capacitor plates. CPT has high efficiency only if the distance between the electrodes is very small. This makes CPT mostly used in small sized applications, such as biomedical applications.

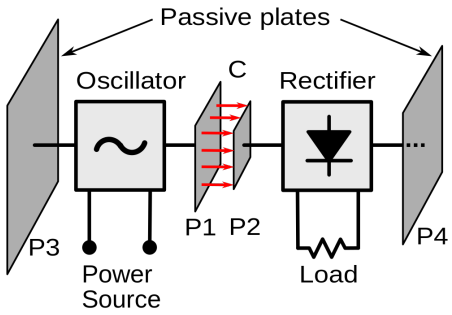


Figure 1.7: A block diagram of CPT system [8]

- Far field wireless power transfer
  IPT and CPT systems are both near-field techniques. Far field techniques use electromagnetic waves to transfer the power, which can be transferred over multiple kilometer ranges. Two main far field techniques are microwave power transmission (MPT) and laser. A proposed application for MPT system is to orbit solar power from solar power satellites to earth and spacecrafts [9]. Lasers were explored in military weapons and aerospace applications.

1.1.4. WIRELESS POWER TRANSFER STANDARDS

There are mainly three standards used in wireless power transfer worldwide. They are Qi, A4WP and PMA.

The Qi is the first introduced open standard developed by the Wireless Power Consortium. The Qi standard is based on inductive power transfer. At first, it specifies the standard for low power smaller than 5W and typically serves for mobile phones. There are already more than 100 mobile phones which can be charged with Qi standard. In the latest version in 2015, the power range is extended and high power specification is also delivered for the power up to 1kW. PMA is a standard based on inductive power transfer similar to Qi but is introduced by different companies alliance.

A4WP is an abbreviation of Alliance for Wireless Power, which is another standard formed by Samsung and Qualcomm to compete with Qi standard. A4WP is based on resonant power transfer, which is slightly different from inductive power transfer. The IPT system requires the distance between the transmitter and the receiver in the magnitude of centimeters and also requires good alignment condition. This limits its application scenario. The idea of resonant power transfer derives from the phenomenon that the coupling is enhanced when the secondary side of the loosely coupled coil resonates [10]. It is utilized at much higher frequency (typically 6.78MHz) than IPT. The benefit is that it allows a larger distance (2m in the experiment of MIT [11]) and misalignment between the transmitter and the receiver. But usually IPT will have higher efficiency than resonant power transfer.

1.1.5. WIRELESS POWER IN THE FUTURE

Wireless power transfer has been an attractive concept since it is created by Nicola Tesla in the 20th century. Nowadays, as Wi-Fi, bluetooth become popular, there is no need to use cable to communicate information. Power cable is the last cable to be cut for complete wireless freedom. The technology of wireless power transfer at present stage is still limited by efficiency and distance. Numerous companies are committed to overcoming the drawbacks and popularizing the technology. Fig. 1.8 is a concept of residential wireless power by Energous, where all the devices in the living room can be charged without wires.

Figure 1.8: A residential wireless power concept by Energous [12]

1.2. MULTIPLE PICKUP IPT SYSTEM

Multiple pickup IPT systems provide power to more than one pickup. The power of a multiple pickup system can range from several watts, like low voltage sensors, to several kilowatts. A schematic of multiple pickup system is shown in Fig. 1.9. Different from a basic IPT system with a single pickup, the primary side of the coupling coil in a multiple pickup system is a long cable, where multiple pickups are coupled.

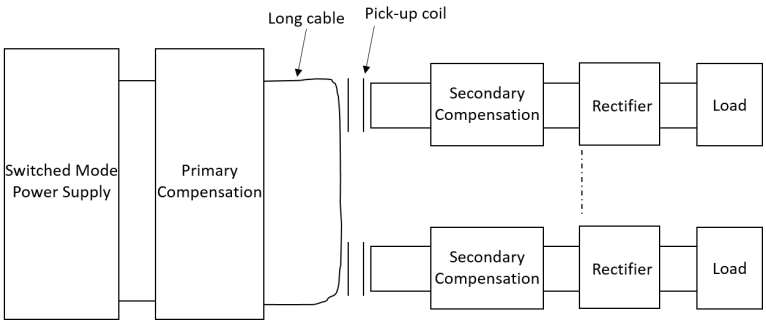


Figure 1.9: Block diagram of a multiple pickup IPT system

During operation, the number of powered pickups is variable. One fundamental requirement is that the power delivered to each powered pickup should not be influenced by the number of powered pickups. This means that the cable current I_{cable} should be constant during operation.

1.2.1. MULTIPLE PICKUP IPT SYSTEM IN LIGHTING APPLICATIONS

There are commercially available products of IPT system in lighting applications. Most of them use clamped pickup. 3i-Innovation provides inductively powered LED lighting used in airport guidance systems and road traffic [13]. Greengage Lighting provides induction powered lighting used in farming, which has fully dimmable light for smooth light transitions [14]. Isotera and Transfotec have contactless LED for various situations [15][16]. A comparison of specification of these commercial products is listed in table 1.1. Fig. 1.10 depicts the product of Isotera, a multiple pickup IPT system with clamped pickups.

Table 1.1: A comparison of commercial induction lighting system [14] [15] [16]

Company	Power Supply	Power (W)	Frequency (kHz)	Efficiency, η
Isotera	PH200 PFC	200	50	96%
Isotera	PH500 PFC	500	50	95%
Greengage	Power Hub	200	\	> 95%
Transfotec	LMPS-DC350	35	16	\
Transfotec	LMPS-750	75	16	\

1.2.2. PICKUP CHARACTERISTICS

In the lab of Philips Lighting, there are built lighting pickups for IPT system, as shown in Fig. 1.11. The pickup has a cylindrical external housing and can be rotated into the concrete. Fig. 1.12 provides the section view of the pickup. In test, they are powered with a commercial broadband amplifier and are proved to be functional. The topology of pickup in lab is depicted in Fig. 1.13. It consists of a transformer, a rectifier, a lamp module and a voltage con-

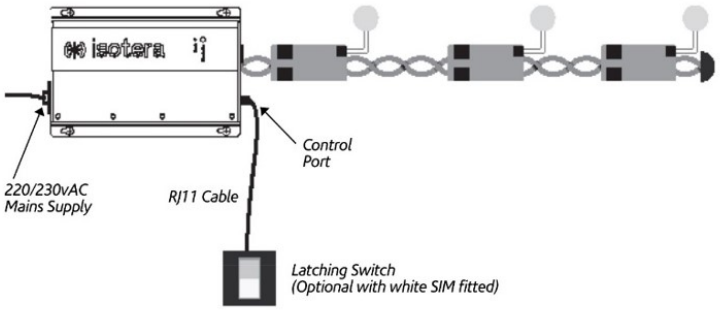
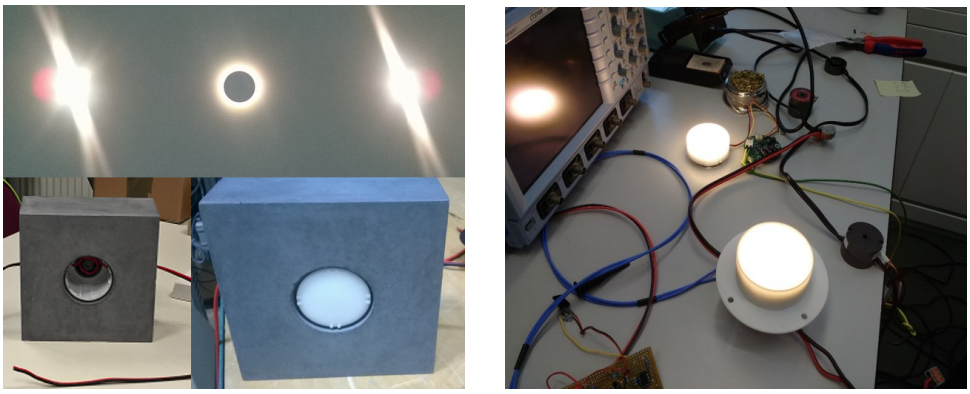


Figure 1.10: Isotera IPT system [15]

troller. The used lamp module is called Blue Parrot Module [17]. When pickup is switched off, the load resistor is short circuit. Related parameters are listed in table 1.2.



(a) Pickup embedded in concrete (b) Pickup and cable

Figure 1.11: IPT Pickup in Philips lighting lab

1.2.3. SYSTEM TOPOLOGY

In this thesis, a power supply is supposed to build to power the pickups. The power supply shall include blocks of switched mode power supply and primary compensation in Fig. 1.2. It has DC voltage input and AC current output to the cable. System topology is shown in Fig. 1.14. Half bridge inverter and LCL-T resonant tank are selected as topologies.

Half bridge inverter is selected qualitatively over various inverters [20]: full bridge inverter, class E inverter, etc. The input of inverter is after the PFC so input voltage is normally around $400V$. Voltage stress on the switch of class E inverter will be $\approx 3.5 \times 400V = 1400V$, which is apparently too large. And the power supply is supposed to power 20 pickups. Total power consumption is around $20 \times 5W = 100W$. For this medium power level, half bridge inverter is suitable.

While there are already controllers on the load side, a complicated control circuit is avoided in power supply in order to avoid that the whole system becomes too complicated. LCL-T network is a simple circuit that can act as a constant current source without extra control circuit [21] [22]. The principle is depicted in Fig. 1.15. According to Thevenin theorem, an ideal voltage source series with an impedance can be transferred to an ideal current source in parallel with the same impedance. When the operating frequency equals the resonant

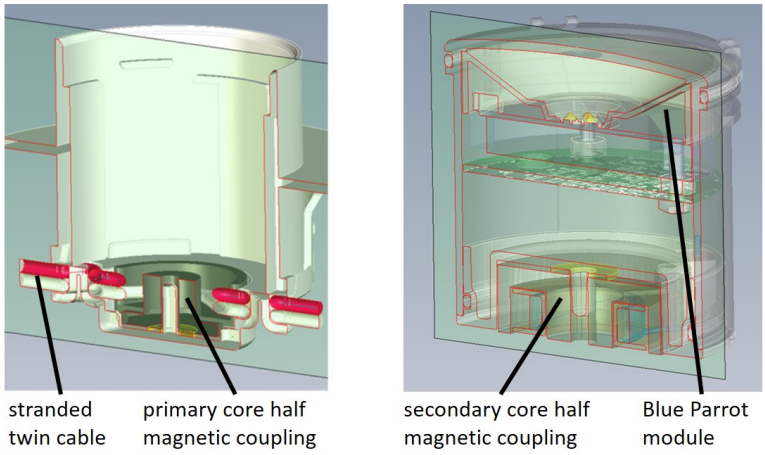


Figure 1.12: Section view of pickup

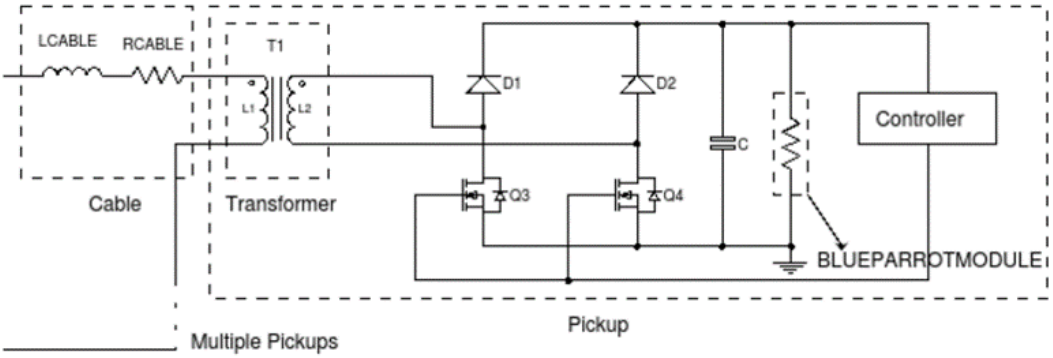


Figure 1.13: Pickup topology in Philips Lighting lab

Table 1.2: Parameters of Pickup in lab

Blue Parrot Module [17]	**Transformer [18]**
P=5W	Core: 3C90, P42/29
$V_{module} = 22V \pm 10\%$	$l_{airgap} = 0.05mm \sim 1mm$
Cable [19]	$N_1 = 1\ or\ 2\ or\ 3$
$l_{cable} = 40m$	$N_2 = 15$
$R_{wire,50kHz} = 25m\Omega/m$	
$L_{wire,50kHz} = 0.7\mu H/m$	

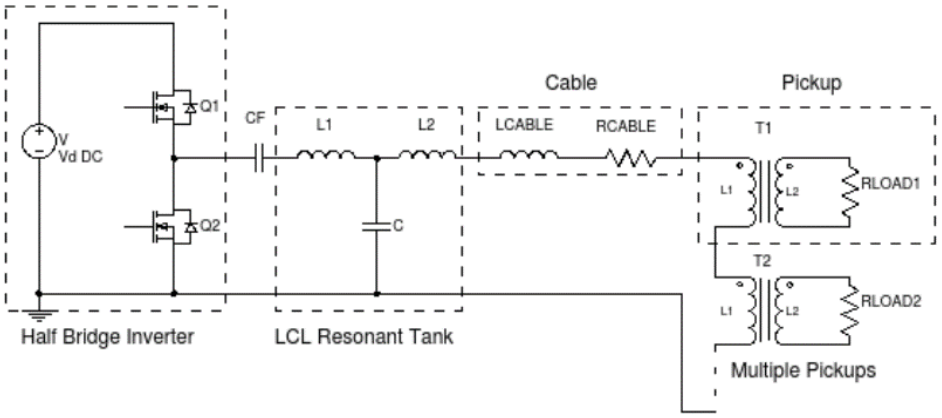


Figure 1.14: System topology of the multiple pickup IPT system

frequency of L_1 and C, current flowing out from parallel L_1 is the same as current flowing into C. So then the LCL-T network has a constant current output.

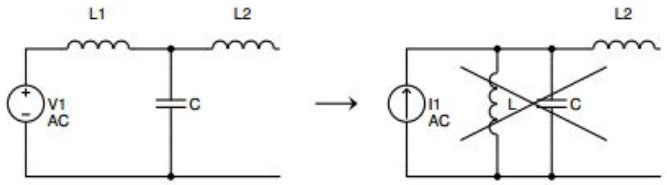


Figure 1.15: Principle of LCL as current source

There is some research of applying LCL-T to IPT system [23] [24]. LCL-T acts as an improvement of parallel compensation on primary side and the aim of application is to enhance the inverter power delivery capability. Operation frequency equals resonant frequency of L_2 and C, where L_2 is the inductance of primary coil. Thus C can fully compensate the primary coil. This is different from [21] [22], where operation frequency equals the resonant frequency of L_1 and C. L_1 is selected to meet power demand from load side. The constant current output is achieved by extra control circuit [24]. Some research also investigates other characteristic of LCL-T network. LCL-T can be used to obtain a high voltage gain when the load is represented as a resistor in parallel with a capacitor [25]. Paper [26] shows that, comparing to the conventional PRC, LCL-T network has better performance in high dynamic control characteristics and reduces component stresses. Analysis of high order harmonics is also proposed for LCL-T network with a simplified circuit [27].

1.2.4. RESEARCH GOAL

The goal of this thesis is to design a constant current source for IPT system and the design will be validated by pickups in Philips Lighting lab. When analyzing LCL-T resonant converters, the load is normally represented as a resistor and L_2 is set as L_1 to make apparent power small [21][22]. This selection is not applicable for this thesis, considering the particularity of multiple pickup IPT system:

- While there are multiple pickups, the reflected reactance from pickups is comparable to L_2 in LCL-T network and varies during operation.
- It is a long cable system, thus the inductance of the cable will be influenced by practical installation.

The main challenge is that load resistance and reactance varies during operation, which results in resonant frequency of circuit variable and low efficiency at light load. To design a constant current source for the whole load range, the following steps are formulated:

1. Chapter 2: Analysis of the parameters in LCL-T network

   In this step, how LCL-T parameters influence the circuit performance are investigated, including ZVS, output current variation, power factor, etc.

2. Chapter 3: Design of the half bridge inverter and LCL-T network

   The half bridge inverter and LCL-T network are designed based on the load of resistors and inductors. A control circuit is also proposed to switch the operation frequency automatically.

3. Chapter 4: Simulation and experiment

   The circuits are simulated separately as the control circuit and the half bridge circuit in the LTspice. A modification based on the high order harmonics is also proposed according to the simulation. In the experiment part, the circuit is constructed and tested with the load represented by resistors and inductors. Then, the IPT pickups in lab will be used to test the constructed circuit.

4. Chapter 5: Conclusion and Future work

   In the final chapter, the conclusion of the whole work is drawn and how future work can be proceeded is described.

2

ANALYSIS OF LCL-T NETWORK

2.1. INTRODUCTION

As has been mentioned in chapter 1, an LCL-T network is selected as resonant tank in the system, due to its constant current output characteristic. Fig. 2.1 shows the LCL-T network used in previous papers.

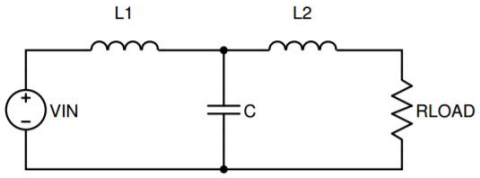


Figure 2.1: Equivalent LCL-T network discussed in previous papers [21][22][28][29][30][31]

The two inductors L_1, L_2 are equal and the operating frequency ω is $1/\sqrt{L_1 C}$.

$$L_1 = L_2 \tag{2.1}$$

$$\omega = \frac{1}{\sqrt{L_1 C}} \tag{2.2}$$

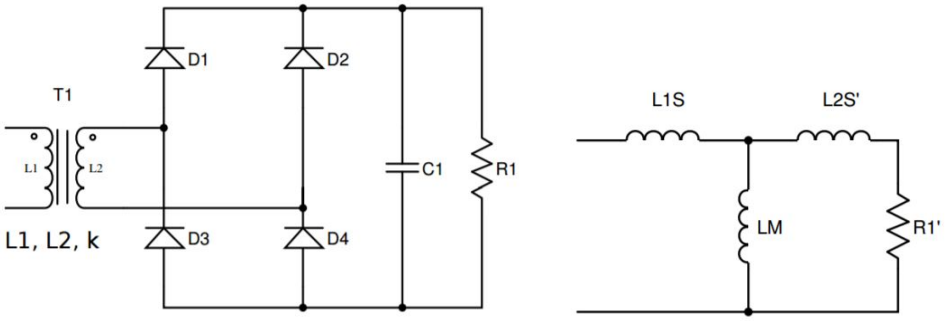
Thus the current through the load will be:

$$I_{load} = \frac{V_{in}}{j\omega L_1} \tag{2.3}$$

It fulfills the requirement that the load, which are pickups in our system, have no influence on the current through them. Besides, the whole circuit will have a resistive input impedance Z_{in} and the apparent power is minimized.

$$\begin{aligned} Z_{in} &= j\omega L_1 + \frac{(j\omega L_2 + R_{load})\frac{1}{j\omega C}}{j\omega L_2 + R_{load} + \frac{1}{j\omega C}} \\ &= \frac{L_1/C}{R_{load}} \end{aligned} \tag{2.4}$$

However, the limitation of above discussion is that the load is simplified as a resistor, which is not accurate in an IPT system. A typical load circuit in an IPT system is depicted in Fig. 2.2(a). It consists of a loosely coupled transformer, a rectifier, a capacitor filter and a load



(a) Load circuit (b) Equivalent load circuit

Figure 2.2: A typical load circuit in IPT system

resistor. The equivalent circuit is depicted in Fig. 2.2(b). Considering the equivalent relation of transformer and rectifier [32], parameters can be calculated as following:

$$L_{1s} = (1-k)L_1 \tag{2.5}$$

$$L_m = kL_1 \tag{2.6}$$

$$L'_{2s} = (\frac{N_1}{N_2})^2 (1-k)L_2 \tag{2.7}$$

$$R'_1 = (\frac{N_1}{N_2})^2 \frac{8}{\pi^2} R_1 \tag{2.8}$$

The equivalent impedance of load is:

$$\begin{aligned} Z_{load} &= j\omega L_{1s} + \frac{j\omega L_m (j\omega L'_{2s} + R'_1)}{j\omega L'_{2s} + R'_1 + j\omega L_m} \\ &= \frac{\omega^2 R'_1 L_m^2}{R_1'^2 + \omega^2 (L_m + L'_{2s})^2} + j\omega [L_{1s} + \frac{L_m (R_1'^2 + \omega^2 L'_{2s}(L_m + L'_{2s}))}{R_1'^2 + \omega^2 (L_m + L'_{2s})^2}] \end{aligned} \tag{2.9}$$

Both the real part and image part of Z_{load} are positive. Thus, in an IPT system, it is more suitable to represent the pickup as a resistor in series with an inductor instead of only a resistor. In an IPT system, compensation is a common way to make the load less inductive and various forms of compensation have been proposed [4]. Series compensation and parallel compensation are the most common. However, for a multiple pickup system, a solution on the power supply side is preferred, instead of the compensation in pickups, which means a large number of extra components. The discussion in the following sections of this chapter will be based on Fig. 2.3. N is the number of pickups.

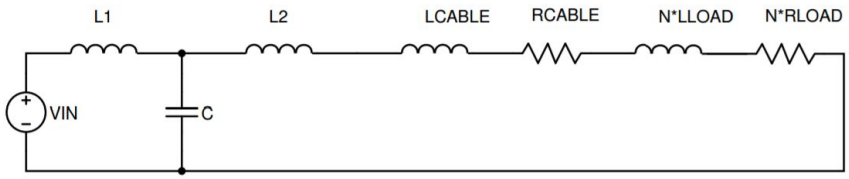


Figure 2.3: LCL-T network and inductive load

2.2. FIRST HARMONIC ANALYSIS

In this section, an LCL-T network with inductive load will be investigated using first harmonic approximation [32]. To analyze the LCL-T network generally, parameters are defined to describe the relation between components in the network and target functions are defined to describe the characteristics of the network.

2.2.1. NETWORK GENERALIZATION

The combination of inductors on the right branch of the LCL-T network is defined as:

$$L_{cm} = L_2 + L_{cable} + N * L_{load} \tag{2.10}$$

The ratio of inductors is defined as:

$$k = \frac{L_{cm}}{L_1} \tag{2.11}$$

The resonant frequency and the normalized switching frequency are defined as:

$$\omega_0 = \frac{1}{\sqrt{L_1 C}} \tag{2.12}$$

$$\omega_n = \frac{\omega}{\omega_0} \tag{2.13}$$

The combination of resistors on the right branch of the LCL-T network is defined as:

$$R_{cm} = R_{cable} + N * R_{load} \tag{2.14}$$

The characteristic impedance Z_n and Q value of the resonant network are defined as:

$$Z_n = \sqrt{\frac{L_1}{C}} \tag{2.15}$$

$$Q = \frac{\omega_0 L_1}{R_{cm}} \tag{2.16}$$

The LCL-T network is redrawn in Fig. 2.4. k, ω_n, Q can be used to describe the relation between L_1, L_{cm}, C, R_{cm}. While L_{cm}, R_{cm} include the inductive and resistive part of load respectively, the variation of k, Q can represent the variation of the load, in other words, different number of on-state pickups.

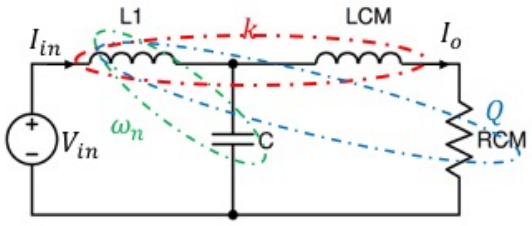


Figure 2.4: LCL-T network with defined parameters

2.2.2. TARGET FUNCTION DEFINITION

- Constant current output H

As stated in chapter 1, one basic requirement for the LCL-T network in our system is to have a constant current output. Normalized current output is used and this characteristic is defined as:

$$H = \frac{|I_o|}{(V_d/Z_n)} \tag{2.17}$$

where V_d is the input voltage of the half bridge inverter. It can be written using only k, ω_n, Q:

$$H(k,\omega_n,Q) = \frac{|I_o|}{(V_d/Z_n)} = \frac{2}{\pi|j\omega_n - jk\omega_n^3 - \frac{\omega_n^2}{Q} + j\omega_n k + \frac{1}{Q}|} \tag{2.18}$$

As k, Q varies, the smaller the variation of H, the better the constant current output characteristic of the LCL-T network.

- Apparent power $\frac{kVA}{kW}$

  During system operation, the number of on-state pickups is allowed to vary from 0 to 21. While each pickup can be equivalent to a resistor in series with an inductor, the variation of number of on-state pickups results in the resonant frequency of the system changing. Reactive power could be large especially when the system is at light load. To describe how much reactive power is in the system, $\frac{kVA}{kW}$ is defined as:

$$\frac{kVA}{kW} = \frac{|V_{in}||I_{in}|}{|V_o||I_o|} \tag{2.19}$$

  where $|V_o||I_o|$ is the power consumed by the load resistor, $|V_{in}|$ and $|I_{in}|$ are amplitude of voltage and current at the output of inverter. It can also be represented by k, ω_n, Q:

$$\frac{kVA}{kW}(k,\omega_n,Q) = |(1 - k\omega_n^2 + \frac{j\omega_n}{Q}) \times (j\omega_n Q - jk\omega_n^3 Q - \omega_n^2 + j\omega_n kQ + 1)| \tag{2.20}$$

  $\frac{kVA}{kW}$ closer to 1, indicating that reactive power in the system is small.

- Phase angle ϕ

  While half bridge is selected as the inverter before LCL-T network, in order to maintain ZVS across both switches, midpoint voltage V_{in} must lead output current I_{in} during each switching cycle. Only then the anti-parallel diode of off-state mosfet can be conducted before that mosfet turns on and the midpoint voltage can turn to the opposite rail voltage during dead time. This requires that the input impedance Z_{in} is inductive.

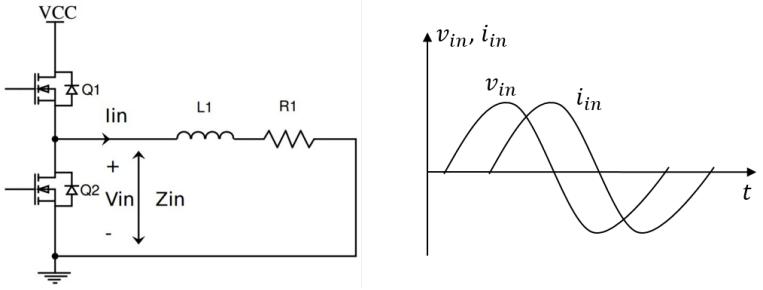


Figure 2.5: ZVS in half bridge inverter

The phase angle of input impedance is defined as:

$$\phi = arctan(\frac{imag(Zin)}{real(Zin)}) \tag{2.21}$$

where input impedance can be written based on k, ω_n, Q:

$$Z_{in} = Q \times R \times \frac{(1-\omega_n^2)(1+j\omega_n kQ) + j\omega_n Q}{Q(1-\omega_n^2 k) + j\omega_n} \tag{2.22}$$

So representation of ϕ by k, ω_n, Q:

$$\phi(\omega_n, k, Q) = arctan[\frac{\omega_n}{Q} \times (Q^2 \times (1-\omega_n^2 k)(1+k(1-\omega_n^2)) - (1-\omega_n^2))] \tag{2.23}$$

As k, Q varies, ϕ should be kept positive.

2.2.3. K, Q RANGE DISCUSSION

As stated in the last paragraph of section 2.2.1, the variation of k and Q represents the change of load during operation. Few points about the range of k are worth noting before discussion about target functions, which could help to avoid unnecessary discussion.

- Eqn. (2.4) gives an expression of input impedance of LCL-T network when $L_1 = L_2$. If $L_1 < L_2$, Z_{in} will become:

$$\begin{aligned} Z_{in} &= j\omega L_1 + \frac{(j\omega L_2 + R_{load})\frac{1}{j\omega C}}{j\omega L_2 + R_{load} + \frac{1}{j\omega C}} \\ &= \frac{L_1/C}{R_{load} + j(\omega L_2 - \frac{1}{\omega C})} \\ &= \frac{L_1/C(R_{load} - j(\omega L_2 - \frac{1}{\omega C}))}{R_{load}^2 + (\omega L_2 - \frac{1}{\omega C})^2} \end{aligned} \tag{2.24}$$

  while $L_1 < L_2$, then $\omega L_2 > \frac{1}{\omega C}$ and imaginary part of Z_{in} becomes negative. This is not allowed for ZVS. Thus the range of k can be limited no larger than 1 during following discussion.

- As shown in Fig. 2.6, in this system, turning on/off the pickup is realized by bridgeless PFC circuit. When the pickup is on-state, the two mosfets in the lower branches are off and it works as a rectifier. To turn off the pickup, the two mosfets are on and makes the load resistor short circuit.

  Fig. 2.7 is the equivalent load circuit, containing load resistor and transformer. While L_{1s} does not change no matter the pickup is on or off, the part in dashed box can be used to compare the equivalent impedance of pickup in on-state and off-state:

$$Z_{dash}(R) = \frac{j\omega L_m(j\omega L_{s2} + R)}{j\omega L_m + j\omega L_{s2} + R} \tag{2.25}$$

$$imag(Z_{dash}(R)) = \omega \frac{L_m R^2 + \omega^2 L_{s2} L_m (L_{s2} + L_m)}{R^2 + \omega^2 (L_{s2} + L_m)^2} \tag{2.26}$$

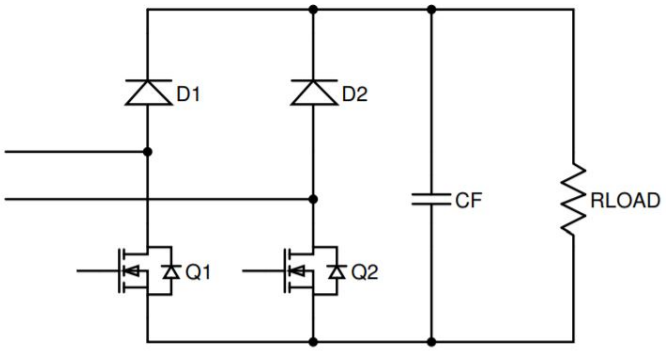


Figure 2.6: Turning on/off the pickup by bridgeless PFC

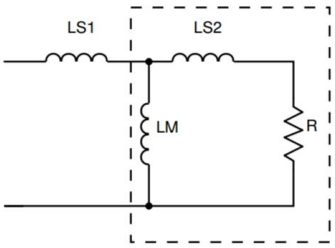


Figure 2.7: Comparison of pickup impedance (including transformer) in on-state and off-state

After mathematical derivation, it can be proven that the imaginary part of pickup impedance is smaller in off-state than in on-state:

$$imag(Z_{dash}(R)) = \omega \frac{L_m R^2 + \omega^2 L_{s2} L_m (L_{s2} + L_m) + L_m \omega^2 (L_{s2} + L_m)^2 - L_m \omega^2 (L_{s2} + L_m)^2}{R^2 + \omega^2 (L_{s2} + L_m)^2} \tag{2.27}$$

$$= \omega (L_m - \frac{\omega^2 L_m^2 (L_{s2} + L_m)}{R^2 + \omega^2 (L_{s2} + L_m)^2}) \tag{2.28}$$

The obvious conclusion is that as R goes lower, $imag(Z_{dash}(R))$ becomes smaller. The system has highest inductive load and resistive load when every pickup is in on-state and has lowest inductive load and resistive load when every pickup is in off-state.

2.2.4. TARGET FUNCTION ANALYSIS

How the target function $H, \frac{kVA}{kW}, \phi$ are influenced by k, ω_n, Q will be elaborated. Eqn. (2.18), (2.20), (2.23) are the expressions of $H, \frac{kVA}{kW}, \phi$ based on k, ω_n, Q.

1. Constant current output H

   Fig. 2.8 depicts target function H(k, ω_n, Q). While normalized current output H is a function of three variables, it is impossible to plot all the variables in consecutive dimensions in a 2-D graph. The function is plotted over ω_n in the range of 0.8 to 1 with $k = 0.8, 0.9, 1$ and $Q = 0.1, 1, 10, 40$.

   What can be observed is that all the curves converge at one point when $\omega_n = 1$. This means when $\omega_n = 1$ normalized current output H is the same for all the curves and the current I_o through L_{cm} and R_{cm} (in Fig. 2.4) is constant no matter how L_{cm} and R_{cm} change. $\omega_n = 1$ is a perfect choice to fulfill the requirement of constant current output.

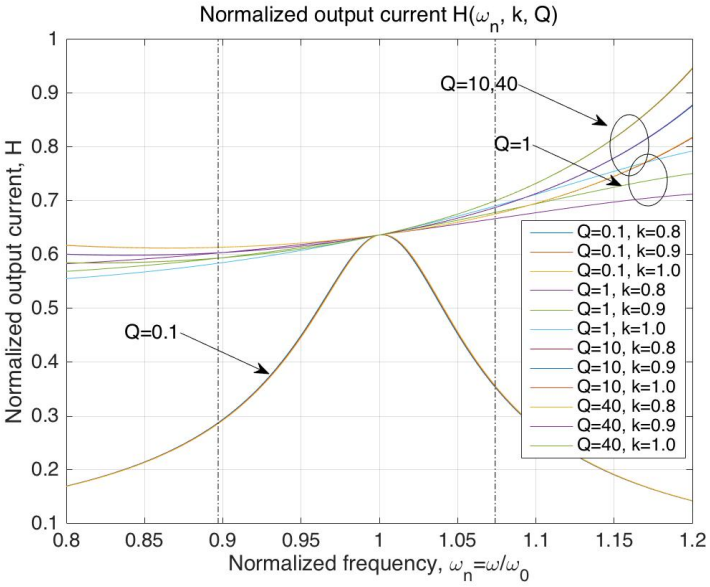


Figure 2.8: Target Function H(k, ω_n, Q)

For the curves $Q = 0.1$, normalized current output H is sensitive to the frequency variation and has a relatively large deviation from other curves, comparing to the deviation between others. For the curves $Q = 1, 10, 40$, at some frequencies, like $\omega_n = 1.05$, normalized current output H changes in a very small range. After traversing all the data, it is found out that between $\omega_n = 0.897$ and $\omega_n = 1.074$ the difference in normalized output current H is less than 5% at the same ω_n for $Q = 1, 10, 40$.

2. Apparent power $\frac{kVA}{kW}$

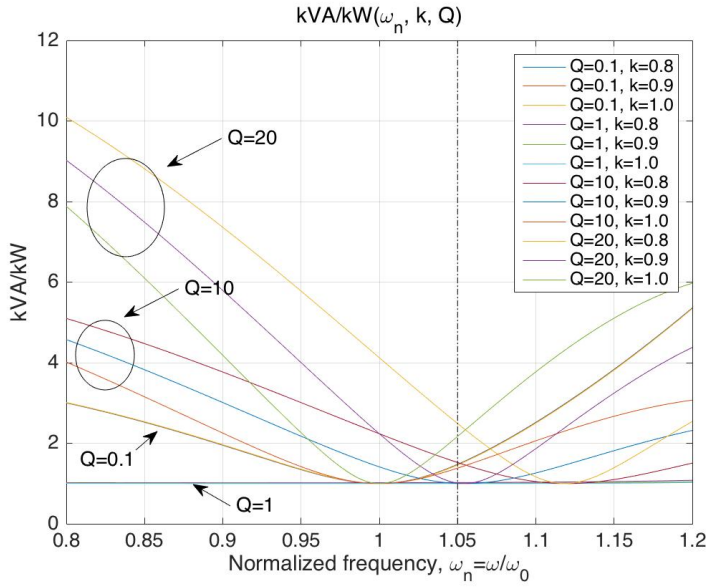


Figure 2.9: Target Function $\frac{kVA}{kW}(k, \omega_n, Q)$

Fig. 2.9 depicts target function $\frac{kVA}{kW}(k, \omega_n, Q)$. When $\omega_n < 1$, for all the curves except $Q = 1$, the more ω_n deviates from 1, the larger $\frac{kVA}{kW}$ is. But when $\omega_n > 1$, as ω_n becomes larger, $\frac{kVA}{kW}$ first is smaller and then gradually larger. Based on Fig. 2.9, it can be inferred

that $\omega_n = 1$ is not the best case to minimize the overall $\frac{kVA}{kW}$ for the whole load range. In other words, there is a normalized frequency ω_n higher than 1 that can make overall $\frac{kVA}{kW}$ minimum. The value of this normalized frequency depends on k and Q.

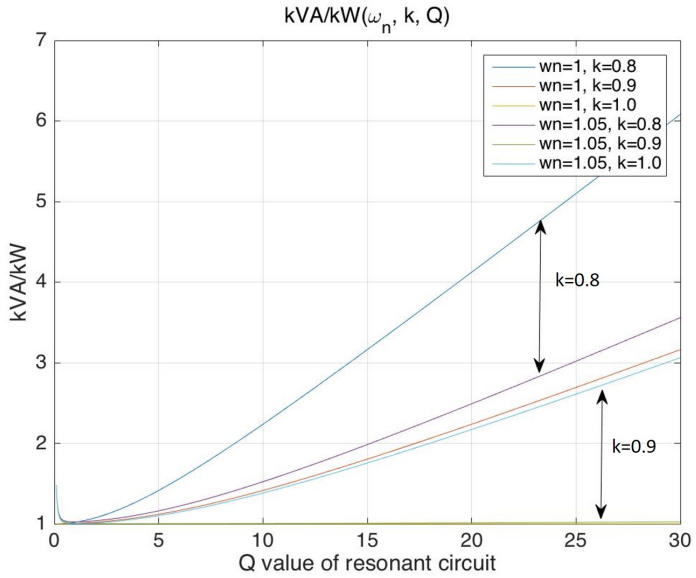


Figure 2.10: Target Function $\frac{kVA}{kW}(k, \omega_n, Q)$ with x axis of Q

To verify that a higher normalized frequency ω_n helps to reduce overall $\frac{kVA}{kW}$, Fig. 2.10 depicts how $\frac{kVA}{kW}$ changes over Q. The dark blue curve is $\frac{kVA}{kW}$ with $\omega_n = 1, k = 0.8$. The purple curve is $\frac{kVA}{kW}$ with $\omega_n = 1.05, k = 0.8$. It can be found that as Q increases, the purple curve is apparently smaller than the dark blue curve and the difference becomes larger and larger. The same trend can be found when comparing $\frac{kVA}{kW}$ with $\omega_n = 1, k = 0.9$ and $\frac{kVA}{kW}$ with $\omega_n = 1.05, k = 0.9$. There is a special curve: $\frac{kVA}{kW}$ with $\omega_n = 1, k = 1$, which does not change with Q. This has been explained in section 2.1.

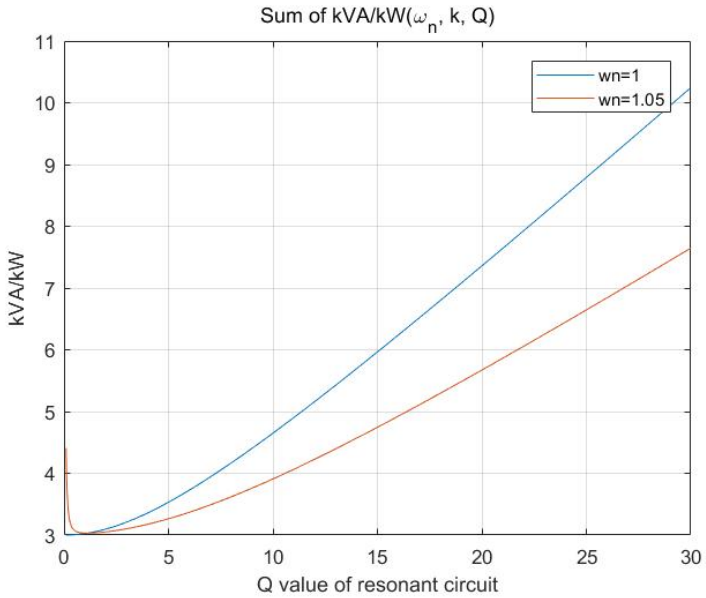


Figure 2.11: Sum of $\frac{kVA}{kW}(k, \omega_n, Q)$ from Fig. 2.10 having the same k on the x axis of Q

Fig. 2.11 shows a more clear conclusion by plotting the sum of curves in Fig. 2.10 having the same k. A higher normalized frequency ω_n can reduce reactive power in the system, especially at light load (large Q).

3. Phase angle ϕ

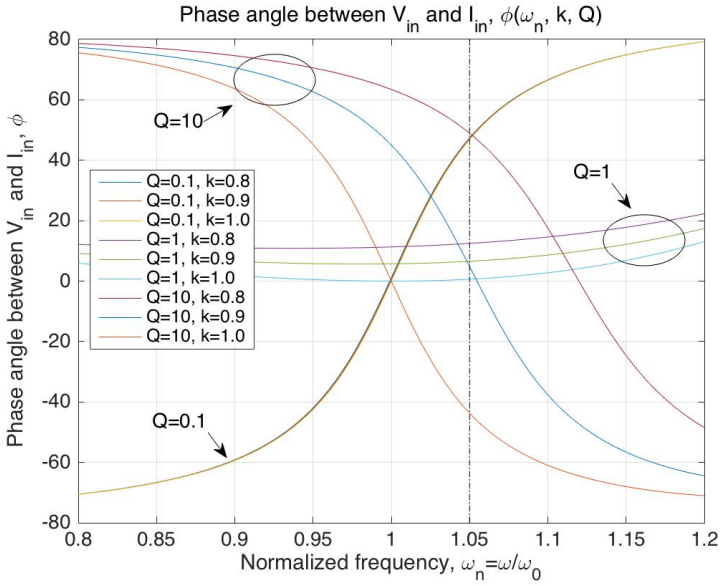


Figure 2.12: Target function $\phi(k, \omega_n, Q)$

Fig. 2.12 depicts phase angle $\phi(k, \omega_n, Q)$. As stated in section 2.2.2, phase angle ϕ should be kept positive as k, Q vary. In Fig. 2.12, the curves with $Q = 1$ can keep positive for whole range of ω_n. The curves with $Q = 0.1$ or $Q = 10$ have some part falling in a negative range. In last paragraph, a conclusion is given that higher normalized frequency ω_n helps to reduce overall reactive power in the circuit. But as Fig. 2.12 shows it may destroy zero voltage switching under certain load condition ($Q = 10$).

2.2.5. ZVS CONDITION ANALYSIS

This section aims to find out the situation of (k, ω_n, Q) when the loss of ZVS happens. Whether ZVS is lost is based on phase angle ϕ. Eqn. (2.23). To keep ZVS, Eqn. (2.23) should be larger than zero and can be rewritten as:

$$\phi = arctan[\frac{\omega_n}{Q} \times (Q^2 \times (1 - \omega_n^2 k)(1 + k(1 - \omega_n^2)) - (1 - \omega_n^2))] > 0 \tag{2.29}$$

This is equivalent to:

$$(\omega_n^2 k - 1)(1 + k(1 - \omega_n^2)) < \frac{\omega_n^2 - 1}{Q^2} \tag{2.30}$$

Section 2.2.3 has stated that k should not be larger than 1. According to Eqn. (2.16), Q obviously is larger than 0. Considering the variation of output current I_o, ω_n should be in the range of 1 to 1.074. The range of (k, ω_n, Q) is discussed here to simplify Eqn. (2.30) one step further:

$$Q = \begin{cases} \text{Any value} > 0, & \text{if } k < \frac{1}{\omega_n^2} \\ < \sqrt{\frac{\omega_n^2 - 1}{(\omega_n^2 k - 1)(1 + k(1 - \omega_n^2))}}, & \text{if } k > \frac{1}{\omega_n^2} \end{cases} \tag{2.31}$$

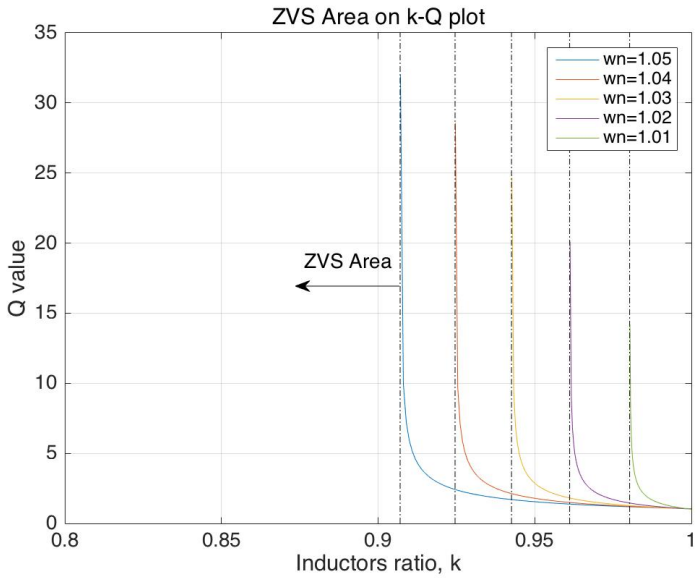
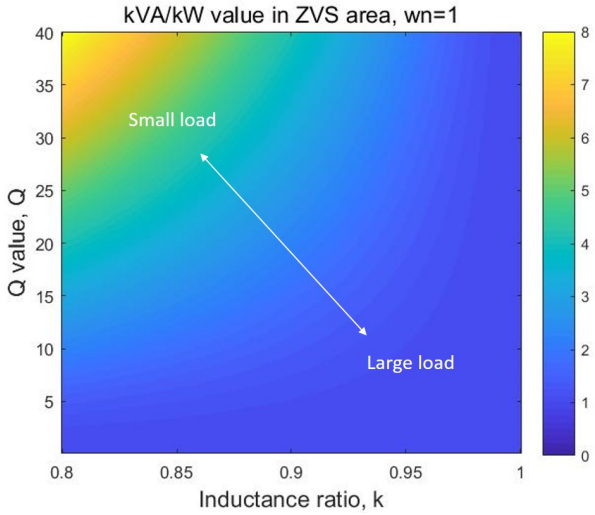
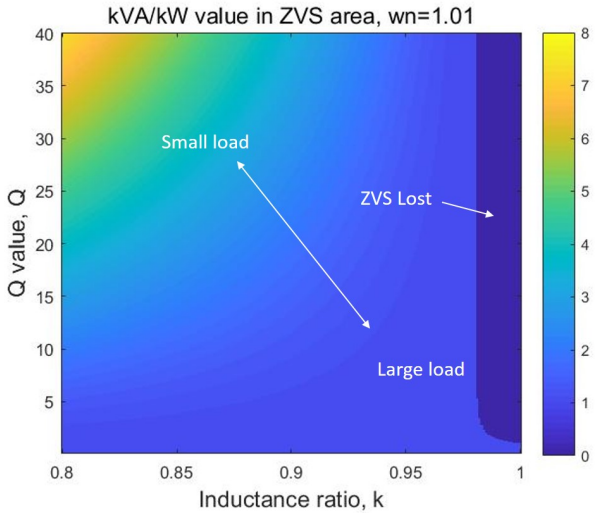


Figure 2.13: ZVS area on $k-Q$ plot

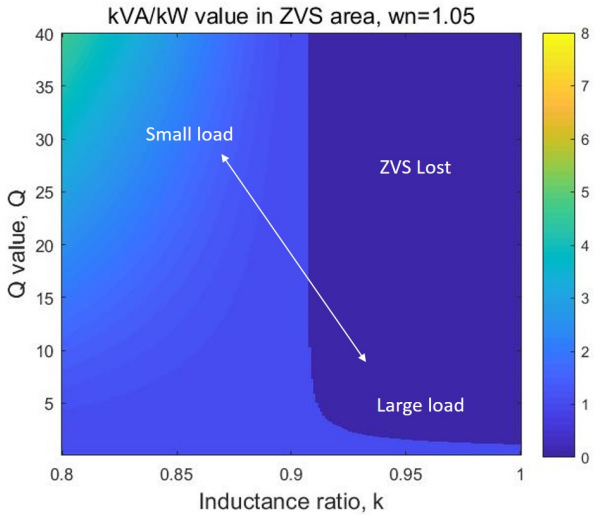
Fig. 2.13 plots the border of ZVS area on $k-Q$ dimensions based on Eqn. (2.31). Five curves represent borders under different system frequencies. If k and Q of the circuit falls on the left side of the curve with corresponding system frequency, then phase angle is positive and ZVS can be realized. In Fig. 2.13, $\omega_n = 1.05$ shows the smallest ZVS area on the plot and $\omega_n = 1.01$ shows the largest ZVS area.
Fig. 2.14 use colormap to show how $\frac{kVA}{kW}$ distribute on $k-Q$ dimensions under different system frequencies. The dark blue area in Fig. 2.14(b) and Fig. 2.14(c) are ZVS lost area. Comparing the three graphs, as frequency ω_n increases, dark blue area grows and yellow area decreases, which means ZVS lost area gets larger and overall $\frac{kVA}{kW}$ gets smaller. There is a trade off between ZVS area and overall $\frac{kVA}{kW}$.
As stated in section 2.1, the load can be equivalent to a resistor in series with an inductor. When the load is turned off, both the resistor and inductor get smaller. This means full load condition correspond to large k small Q and light load condition corresponds to large Q small k. As the system operates from a full load to no load condition, the load curve on $k-Q$ graph should move from right bottom corner to left upper corner.



(a) $\frac{kVA}{kW}$ on $k-Q$ under $\omega_n = 1$



(b) $\frac{kVA}{kW}$ on $k-Q$ under $\omega_n = 1.01$



(c) $\frac{kVA}{kW}$ on $k-Q$ under $\omega_n = 1.05$

Figure 2.14: $\frac{kVA}{kW}$ comparison on $k-Q$ plot under different system frequencies

2.2.6. SIMULATION VERIFICATION

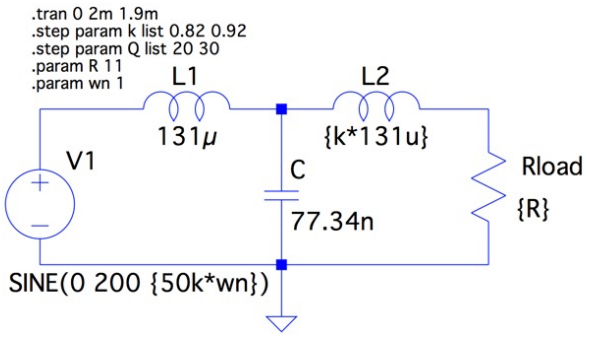


Figure 2.15: LTspice model of LCL-T Network

This section will use simulation to verify the conclusion of the previous section. Fig. 2.15 shows a LCL-T network built in LTspice. The source voltage is an ideal sine wave with $50kHz$ and $200V$ amplitude. $L_1 = 131\mu H$ and $C = 77.34nF$ are resonant at $50kHz$.

The current through the resistor is plotted in Fig. 2.16 under four different k, Q combination: $k = 0.82$ $Q = 20, k = 0.92$ $Q = 20, k = 0.82$ $Q = 30, k = 0.92$ $Q = 30$. The normalized frequency ω_n is set as 1.05. It proves the variation of output current is limited when system operates at 1.05 times the resonant frequency of L_1 and C.

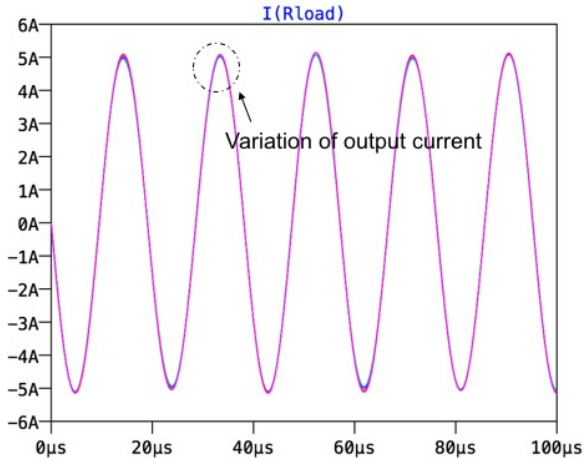


Figure 2.16: Output current under different k, Q when $\omega_n = 1.05$ in LTspice

How $\frac{kVA}{kW}$ changes with ω_n is plotted in Fig. 2.17. Two curves represent $k = 0.82, Q = 30$ and $k = 0.92, Q = 20$, respectively. Both of them prove that as frequency slightly goes higher, $\frac{kVA}{kW}$ decreases. The reduction is more obviously under $k = 0.82, Q = 30$, which represents a light load condition comparing to the other curve. It is worth noting that when $k = 0.92, Q = 20, \omega_n = 1.05$, the system can not realize ZVS, which conforms to the content shown in Fig. 2.13.

The simulation result verifies the analysis of LCL-T network in first harmonic approximation.

2.3. HIGH ORDER HARMONICS ANALYSIS

2.3.1. LCL SIMPLIFICATION IN HIGH ORDER HARMONICS

The output voltage of the half bridge inverter is a square wave and can be replaced by a Fourier series expansion:

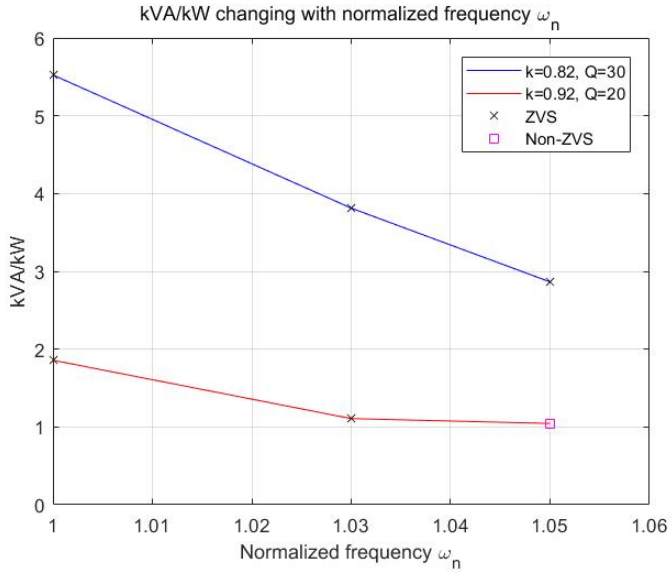


Figure 2.17: $\frac{kVA}{kW}$ changing with normalized frequency ω_n in simulation

$$V_{inv}(t) = \frac{4V_{sq}}{\pi} \sum_{n=1,3,5...}^{+\infty} \frac{sin(n\omega t)}{n} \tag{2.32}$$

V_{sq} is the amplitude of the square wave voltage, ω is the frequency of square wave and n corresponds to the order of harmonics. A simplification will be introduced for LCL network under high order harmonics, which is depicted in Fig. 2.18. The method was first introduced in [27].

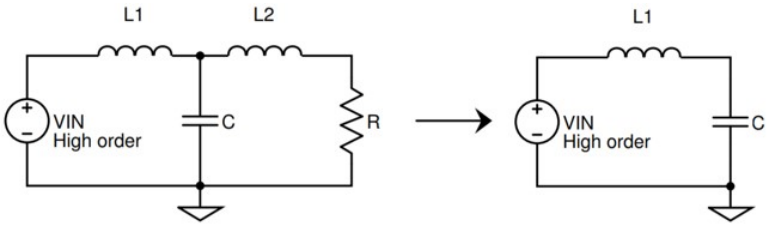


Figure 2.18: LCL-T simplification in high order harmonics analysis

As harmonics order increases, the impedance of L_2 increases and impedance of C decreases. For instance, comparing to fundamental, impedance of L_2 is 3 times higher and impedance of C is 3 times smaller in 3rd order harmonics. While L_2 is parallel to C, the total impedance mainly depends on C in high order harmonics. Thus the LCL-T network can be simplified to a LC circuit when analyzing in high order harmonics. The LCL network of three passive components is simplified to a LC network of two passive components under high order harmonics, which greatly reduces computational effort. High order harmonics have no influence on real power consumption, since high order harmonics current does not flow through the load resistor.

While the high order harmonic exists, the inverter output current deviates from ideal sine wave. As shown in Fig. 2.5, to achieve ZVS in half bridge inverter, inverter output voltage must lead inverter output current, so that the anti-parallel diode of off-state mosfet can be conducting before that mosfet turns on. The size of inverter output current at switching

instant is a key to realize ZVS. It must be large enough to remove the charge in the output capacitor of off-state mosfet during the dead time. The inverter output current at switching instant will be calculated precisely in section 2.3.2.
Besides switching current, the other impact of high order harmonics is that they provide extra reactive power in the circuit. This will be calculated in section 2.3.3.

2.3.2. SWITCHING CURRENT CALCULATION

SWITCHING CURRENT IN FIRST HARMONICS ANALYSIS

Switching current will firstly be calculated in first harmonics analysis. Fig. 2.19 shows a LCL-T network with sine wave voltage source.

$$V(t) = \frac{4V_{sq}}{\pi} sin(\omega t) \tag{2.33}$$

$$\omega = \frac{1}{\sqrt{L_1 C}} \tag{2.34}$$

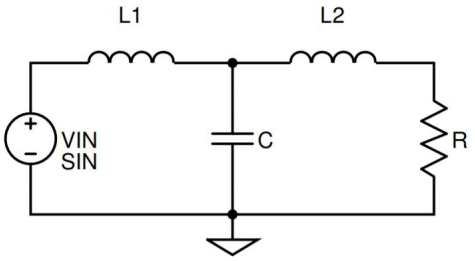


Figure 2.19: LCL-T with sine wave source

Total circuit impedance:

$$\begin{aligned} Z &= j\omega L_1 + \frac{(j\omega L_2 + R)\frac{1}{j\omega C}}{j\omega L_2 + R + \frac{1}{j\omega C}} \\ &= \frac{L_1/C}{j\omega L_2 + R + \frac{1}{j\omega C}} \\ &= \frac{L_1/C}{R^2 + (\omega L_2 - \frac{1}{\omega C})^2}(R - j(\omega L_2 - \frac{1}{\omega C})) \end{aligned} \tag{2.35}$$

Phase angle:

$$\phi(Z) = arctan(-\frac{\omega L_2 - \frac{1}{\omega C}}{R}) \tag{2.36}$$

Amplitude:

$$|Z| = \frac{L_1/C}{\sqrt{R^2 + (\omega L_2 - \frac{1}{\omega C})^2}} \tag{2.37}$$

Inverter output current:

$$I_{inv,1}(t) = \frac{V_{inv,1}}{|Z|} sin(\omega t - \phi(Z)) \tag{2.38}$$
$$= \frac{V_{inv,1}}{L_1/C} \sqrt{R^2 + (\omega L_2 - \frac{1}{\omega C})^2} sin(\omega t - arctan(-\frac{\omega L_2 - \frac{1}{\omega C}}{R}))$$

At switching constant t=0:

$$I_{inv,1,t=0} = \frac{V_{inv,1}}{L_1/C} \sqrt{R^2 + (\omega L_2 - \frac{1}{\omega C})^2} \times (-\frac{\frac{1}{\omega C} - \omega L_2}{\sqrt{R^2 + (\omega L_2 - \frac{1}{\omega C})^2}}) \tag{2.39}$$
$$= \frac{V_{inv,1}}{L_1/C} (\omega(L_2 - L_1))$$
$$= \frac{4V_{sq}}{\pi\omega L_1} (\frac{L_2}{L_1} - 1)$$

SWITCHING CURRENT IN HIGH ORDER HARMONICS ANALYSIS

This part will analyze the switching current in high order harmonics analysis.
Total impedance after simplification in Fig. 2.18:

$$Z_n = jn\omega L_1 + \frac{1}{jn\omega C} \tag{2.40}$$

Inverter output current in n order harmonics:

$$I_{inv,n}(t) = \frac{V_{inv,n}}{\omega L_1 (n - \frac{1}{n})} sin(n\omega t - \frac{\pi}{2}) \tag{2.41}$$

At switching instant, t=0:

$$I_{inv,high} = \sum_{n=3,5,...}^{+\infty} I_{n,t=0} = -\frac{1}{\omega L_1} \sum_{n=3,5,...}^{+\infty} \frac{V_{inv,n}}{n - \frac{1}{n}} \tag{2.42}$$
$$= -\frac{4V_{sq}}{\pi\omega L_1} \lim_{n \to +\infty} \frac{1}{2} \times (\frac{1}{2} - \frac{1}{4} + \frac{1}{4} - \frac{1}{6} + ... - \frac{1}{n+1})$$
$$= -\frac{4V_{sq}}{\pi\omega L_1} \times \frac{1}{4}$$

The combination of inverter output current at switching constant in first harmonics and high order harmonics:

$$I_{inv} = I_{inv,1} + I_{inv,high} \tag{2.43}$$
$$= \frac{4V_{sq}}{\pi\omega L_1} (\frac{L_2}{L_1} - 1.25)$$

SIMULATION VERIFICATION

The simulation circuit in Fig. 2.20 is used to verify the switching current calculation. A pulse voltage source is used to represent square wave voltage. Fig. 2.21(a) is the inverter output for $k = 0.92, Q = 20, \omega_n = 1$. Based on (2.43), switching current should be:

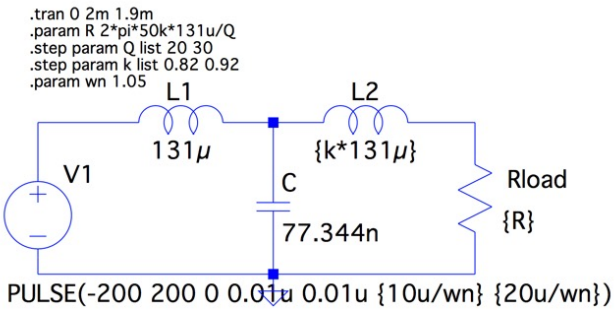


Figure 2.20: LTspice model of LCL-T network with square wave source

$$I_{inv} = \frac{4V_{sq}}{\pi\omega L_1}(\frac{L_2}{L_1} - 1.25) = -2.04A \tag{2.44}$$

Fig. 2.21(b) is the inverter output for $k = 0.82, Q = 20, \omega_n = 1$. Based on (2.43), switching current should be -2.66A. In simulation, the switching current is 2.14A and 2.75A, respectively. The error is 4.7% and 3.3%.
Besides switching current, in Fig. 2.22, the current through the load I_o is also checked in simulation under $k = 0.82$ $Q = 20, k = 0.92$ $Q = 20, k = 0.82$ $Q = 30, k = 0.92$ $Q = 30$ when $\omega_n = 1.05$. The characteristic of limited current variation is kept when taking high order harmonics into account. The reason is most of high order harmonics current flows through C rather than L_2 while impedance of C is at least 9 times smaller than L_2. Thus the influence of high order harmonics on the current through load I_o is not obvious.

2.3.3. REACTIVE POWER CALCULATION

From Fig. 2.18, high order harmonic current mainly flows through L_1 and C. Since they are not resonant in high order harmonics, they produce extra reactive power. The total reactive power at inverter output can be obtained by first calculating the apparent power.
Apparent power S_{inv}:

$$S_{inv} = V_{inv,rms} \times I_{inv,rms} \tag{2.45}$$

Reactive power Q_{inv}:

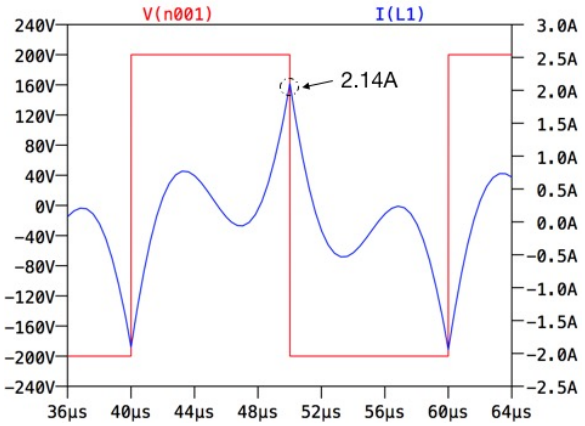
$$Q_{inv} = \sqrt{S_{inv}^2 - P_{inv}^2} \tag{2.46}$$

Eqn. 2.38 and Eqn. 2.41 give the expressions of inverter output current under first harmonic and high order harmonics. In order not to make the calculation too cumbersome, only third harmonics is taken into account. The apparent power can be calculated:

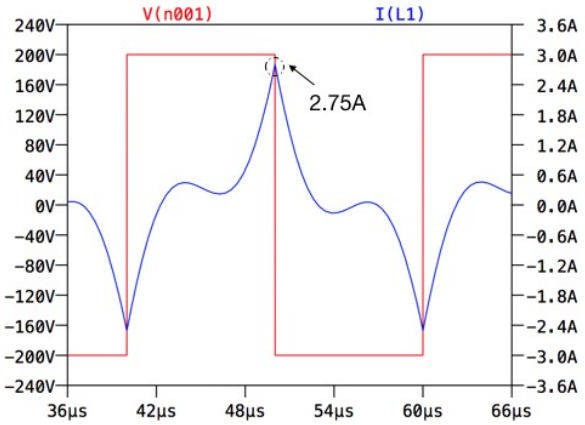
$$V_{inv,rms} = V_{sq} \tag{2.47}$$

$$I_{inv,rms} = \sqrt{\frac{1}{T_1}\int_0^{T_1}(I_{inv,1}(t) + I_{inv,3}(t))^2 dt} \tag{2.48}$$

$$\begin{aligned} I_{inv,3} &= \frac{V_{inv,3}}{\omega L_1(3-\frac{1}{3})} sin(n\omega t - \frac{\pi}{2}) \\ &= \frac{V_{inv,1}}{8\omega L_1} sin(3\omega t - \frac{\pi}{2}) \end{aligned} \tag{2.49}$$



(a) $k = 0.92, Q = 20, \omega_n = 1$



(b) $k = 0.82, Q = 30, \omega_n = 1$

Figure 2.21: Inverter output waveform in simulation

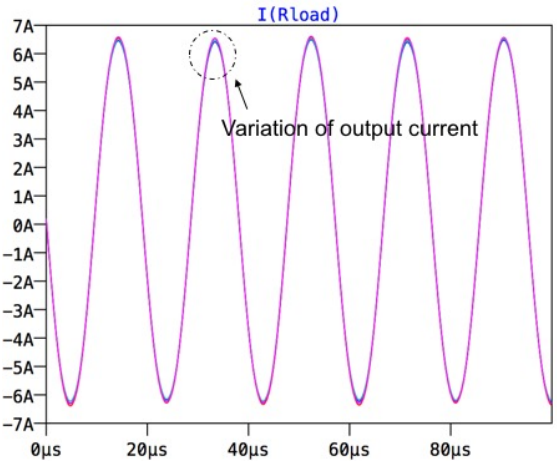


Figure 2.22: Current through load I_o under different load(k, Q) when ω_n = 1.05 and square wave input

Eqn. (2.38) and Eqn. (2.49) are brought into Eqn. (2.48):

$$I_{inv,rms} = \frac{V_{sq}}{\pi}\sqrt{\frac{8}{|Z|^2} + \frac{1}{8\omega^2 L_1^2}} \tag{2.50}$$

$$S_{inv} = \frac{V_{sq}^2}{\pi} \times \sqrt{\frac{8}{|Z|^2} + \frac{1}{8\omega^2 {L_1}^2}} \tag{2.51}$$

The apparent power for first harmonic is:

$$\begin{aligned} S_{inv,1} &= V_{inv,1,rms} \times I_{inv,1,rms} \\ &= \frac{8V_{sq}^2}{\pi^2|Z|} \end{aligned} \tag{2.52}$$

Apparently $S_{inv,1}$ is smaller than S_{inv}. While $V_{inv,rms}$ is just $\frac{V_d}{2}$, the accuracy of calculated apparent power S_{inv} simply depends on $I_{inv,rms}$. The precision of calculated $I_{inv,rms}$ is checked by using the same LTspice model in Fig. 2.20. As shown in table 2.1, the error is aroung 5% and considering only third order harmonic is sufficient to get an accurate result of $I_{inv,rms}$.

Table 2.1: $I_{inv,rms}$ comparison between Eqn. (2.50) and LTspice model

	Calculation(A)	LTspice(A)	Error(%)
$k = 0.82, Q = 30$	0.969	1.01	4.1
$k = 0.92, Q = 20$	0.685	0.727	5.7

2.4. CHAPTER SUMMARY

In this chapter, LCL network is analyzed in a general way under first harmonic and also high order harmonics. The following conclusions are drawn:

- In first order harmonic analysis, operating at higher frequency has a benefit of lower reactive power in the circuit. And the characteristic of constant current output is maintained at the same time. To keep ZVS for the whole load range, the system is proposed to operate at two different frequency depending on the load condition, high frequency at light load and low frequency at large load.
- High order harmonics have influence on inverter output current and cannot affect the current through the load. Mathematical equations are deduced to calculate inverter output current at switching instant and the reactive power provided by high order harmonics. The precision of both of them are verified with simulation.

3

POWER SUPPLY DESIGN WITH RL LOAD

3.1. INTRODUCTION

This chapter describes the design of the power supply with the load of equivalent inductors and resistors for a multiple pickup system in this chapter. It is required to meet power demand and guarantee ZVS. Based on the analysis of chapter 2, the power supply will work at two different frequencies depending on load condition to reduce reactive power in the circuit at light load. The specification of the system will be first introduced. And then the LCL network, control circuit and half bridge will be designed in turn.

3.2. SPECIFICATION

As stated in section 2.1, without compensation, the pickup can be equivalent to an inductor in series with a resistor. Before the design, the equivalent inductor and resistor of a pickup need to be determined. In Fig. 1.13, the pickup is consisted of a Blue Parrot module, a transformer, a rectifier and a voltage controller. Table 1.2 depicts the parameters of the pickup. According to table 1.2, the equivalent load resistor of the Blue Parrot module is:

$$R_{module} = \frac{V_{module}^2}{P} = 96.8\Omega \tag{3.1}$$

The equivalent ac resistance for the rectifier is given as [32]:

$$R_{rec} = \frac{8}{\pi^2} R_{module} = 78.5\Omega \tag{3.2}$$

In the table 1.2, the air gap distance of the transformer $l_{air\ gap}$ is in a range of $0.05mm$ to $1mm$. The air gap distance is limited by mechanical reasons. The number of the primary turns N_1 can be 1 or 3. So the parameters of the transformer will also be measured with the same core and cable under air gap distance of $0.05mm$, $0.5mm$ and $1mm$ and the number of primary turns of 1 or 3. $L_{eq(on)}$ and $R_{eq(on)}$ are the equivalent inductor and resistor when the load resistor is connected. $L_{eq(off)}$ and $R_{eq(off)}$ are the equivalent inductor and resistor when the load resistor is short-circuited.
Considering the magnitude of L_{eq} and R_{eq} shown in table 3.1 and table 3.2, the power supply will be designed based on each pickup represented as a $1\mu H$ inductor in series with a 0.5Ω

Table 3.1: Equivalent inductor and resistor of pickup, $N_1 = 1, N_2 = 15$, at 50kHz

	$L_{eq(on)}, \mu H$	$R_{eq(on)}, \Omega$	$L_{eq(off)}, \mu H$	$R_{eq(off)}, \Omega$
$l_{air\ gap} = 0.05mm$	1.10	0.260	0.470	0.024
$l_{air\ gap} = 0.50mm$	0.79	0.053	0.471	0.024
$l_{air\ gap} = 1mm$	0.65	0.031	0.470	0.022

Table 3.2: Equivalent inductor and resistor of pickup, $N_1 = 3, N_2 = 15$, at 50kHz

	$L_{eq(on)}, \mu H$	$R_{eq(on)}, \Omega$	$L_{eq(off)}, \mu H$	$R_{eq(off)}, \Omega$
$l_{air\ gap} = 0.05mm$	6.87	1.90	1.08	0.058
$l_{air\ gap} = 0.50mm$	3.92	0.32	1.09	0.058
$l_{air\ gap} = 1mm$	2.64	0.148	1.11	0.059

resistor. The specification of the system is listed in table 3.3 and depicted including the power supply topology in Fig. 3.1. The system frequency is selected to be $50kHz$ for high load and another slightly higher frequency for low load. This selection is based on the common frequency of similar commercial products in the markt, shown in table 1.1. The number of on-state pickups varies in the range of 0 to 20. Each pickup consumes 5W power when they are turned on.

Table 3.3: System specification

Power Supply	$V_d = 320V$, $f = 50kHz, > 50kHz$
Pickups	$R = 0.5\Omega$, $L = 1\mu H$, $N = 20$, $P = 5W/pickup$
Cable	$R_{cable} = 1\Omega$, $L_{cable} = 30\mu H$

3.3. LCL NETWORK DESIGN

This section determines the parameters of the LCL network. Chapter 2 shows that when taking higher frequency at light load, the system can have the benefit of lower reactive power and keep the characteristic of constant current output. This section also determines how the frequency should switch as the number of pickups changes.
While each pickup consumes $5W$, the current through pickups is

$$I_{load} = \sqrt{\frac{P}{R}} = 3.16A \tag{3.3}$$

The input voltage to half bridge inverter is $320V$, so the amplitude of the square wave voltage and the amplitude of the first harmonic are

$$V_{sq} = \frac{V_d}{2} = 160V \tag{3.4}$$

$$V_{inv,1} = \frac{4V_{sq}}{\pi} = 203.7V \tag{3.5}$$

The LCL network can have a constant current output when L_1 and C are resonant at system

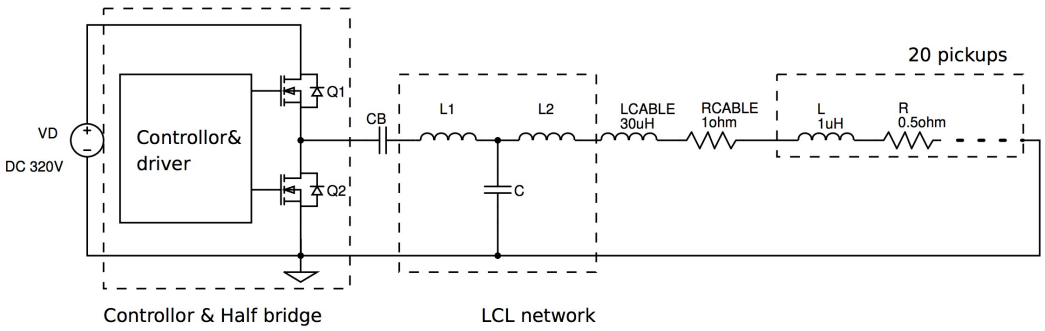


Figure 3.1: Power supply topology with the specification

frequency $f = 50kHz$. So L_1 and C are calculated by

$$L_1 = \frac{V_{inv,1}}{\sqrt{2}\omega I_{load}} = 145.1\mu H \tag{3.6}$$

$$C = \frac{1}{\omega^2 L_1} = 69.8nF \tag{3.7}$$

Eqn. (2.4) shows that when the inductor on the right branch of LCL equals the inductor on the left branch of LCL, the total impedance is resistive. Besides that, section 2.2.3 proves that the right branch inductor should not be larger than the left branch inductor to avoid the total impedance being capacitive. The sum of inductors on the right branch in Fig. 3.1 should be equal to L_1 at full load.

$$L_2 = L_1 - L_{cable} - 20 \times L = 95.1\mu H \tag{3.8}$$

The range of inductors ratio k and Q value are determined:

$$k : \frac{L_{cable} + L_2}{L_1} \sim \frac{L_{cable} + L_2 + 20 * L}{L_1} \rightarrow 0.862 \sim 1 \tag{3.9}$$

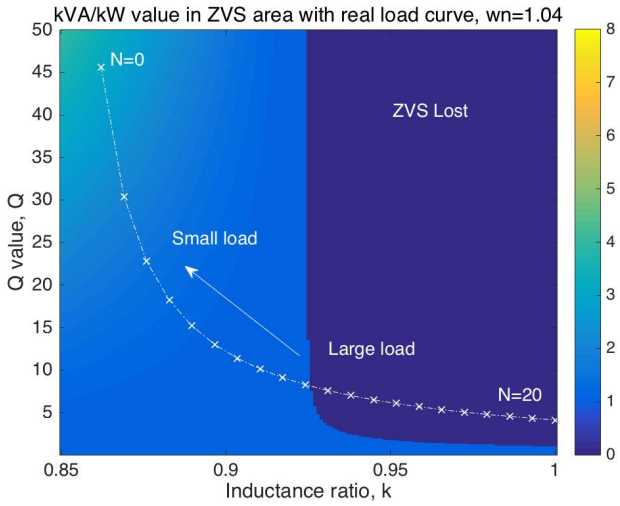
$$Q : \frac{\omega L_1}{R_{cable}} \sim \frac{\omega L_1}{R_{cable} + 20 * R} \rightarrow 45.58 \sim 4.14 \tag{3.10}$$

Similarl to Fig. 2.14, how k, Q change with different load is plotted on a $\frac{kVA}{kW}$ colormap with k, Q axis in Fig. 3.2. Since in Fig. 3.2(b) the major part of the load curve falls on the ZVS lost area, $\omega_n = 1.04$ is a better choice considering the whole load range. When $N < 10$, $\omega_n = 1.04$. When $N \geqslant 10$, $\omega_n = 1$.

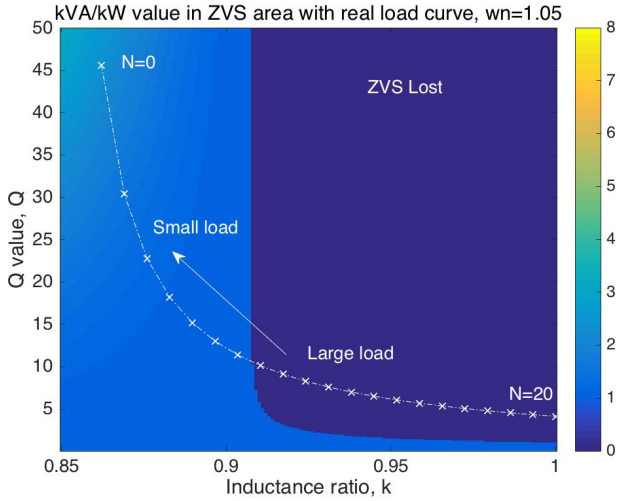
3.4. HALF BRIDGE INVERTER DESIGN

From table 3.3, the half bridge inverter is supposed to generate a $50kHz$ (or $1.04 * 50kHz$) square wave voltage with $\pm 160V$ amplitude. The frequency switching will be introduced in the next section. This section determines the parameters of driver IC and MOSFET. $IR2153D$ is used for driver IC and $IRF740LC$ is selected as MOSFET in the half bridge.

The $IR2153D$ is a high voltage half bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer [33]. Fig. 3.3 is a typical connection of IR2153D. The frequency is configured with a single resistor and timing capacitor connected to the R_T pin and C_T pin [34], determined by Eqn. (3.11) where the 75Ω term accounts for resistance of the R_T pin. The output square wave has a 50% duty cycle and $1.2\mu s$ fixed dead time, which are determined internally by the $IR2153D$. To generate a frequency of $50kHz$, $R = 1449\Omega$ and $C = 10nF$ are selected.



(a) $\frac{kVA}{kW}$ on $k-Q$ under $\omega_n = 1.04$



(b) $\frac{kVA}{kW}$ on $k-Q$ under $\omega_n = 1.05$

Figure 3.2: $\frac{kVA}{kW}$ with $k-Q$ axis under different frequencies, $\omega_n = 1.04, 1.05$

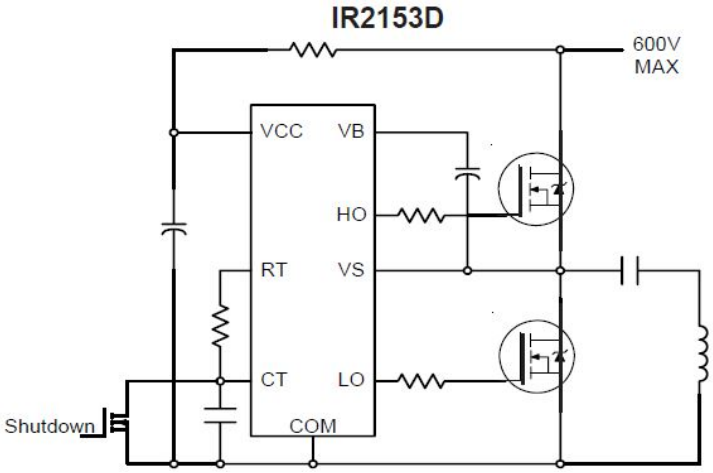


Figure 3.3: A typical connection of IR2153D [33]

$$f = \frac{1}{1.38(R+75)C} \tag{3.11}$$

$$R = 1449\Omega, C = 10nF \tag{3.12}$$

The $IRF740LC$ is a low charge N-channel Power MOSFET achieving significantly lower gate charge over conventional MOSFETs [35]. It is tolerant for maximum drain-source voltage of $400V$. Fig. 3.4 depicts how capacitances of $IRF740LC$ vary with drain-source voltage V_{ds}. During the turn-on procedure, the total amount of charge to be released in the output capacitance of $IRF740LC$ is calculated in Eqn. (3.13).

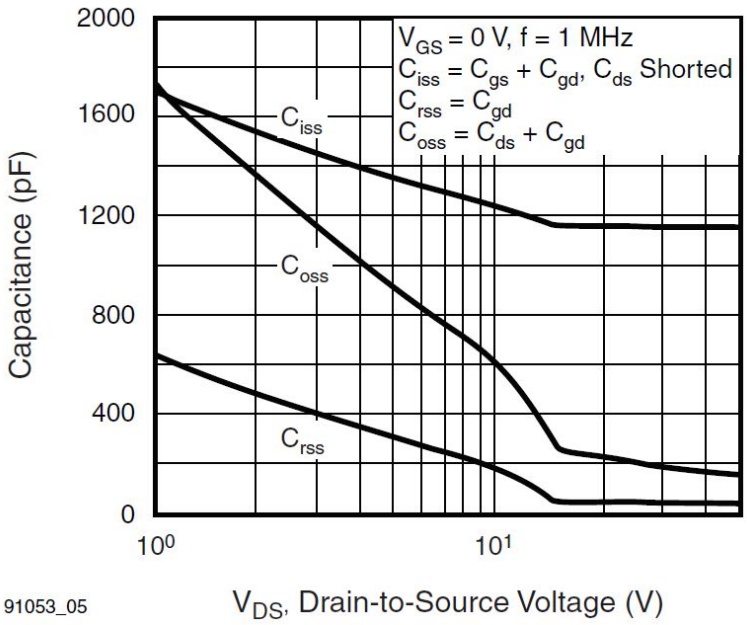


Figure 3.4: Typical capacitance vs. drain-to-source voltage of $IRF740LC$ [35]

$$Q_{output} = \int_0^{V_d} C_{oss} dV_{ds} \tag{3.13}$$

Since C_{oss} changes with different V_{ds} and the relation is not a simple function, the C_{oss} curve in Fig. 3.4 is digitized to 70 ~ 80 points and shown in Fig. 3.5. When $V_{ds} > 50V$, the slope of the $C_{oss} - V_{ds}$ curve is very small and C_{oss} is considered to be constant. Eqn. (3.13) is rewritten as Eqn. (3.14). A similar procedure can be done for the reverse transfer capacitance C_{rss}. The digitized curve is shown in Fig. 3.5 and the result is in Eqn. (3.15).

$$Q_{oss} = \sum_{n=1}^{30} \frac{C_{oss,n} + C_{oss,n+1}}{2} \times (V_{ds,n+1} - V_{ds,n}) + C_{oss,31} \times (320V - 50V) \tag{3.14}$$

$$= 73.58nC$$

$$Q_{rss} = 20.37nC \tag{3.15}$$

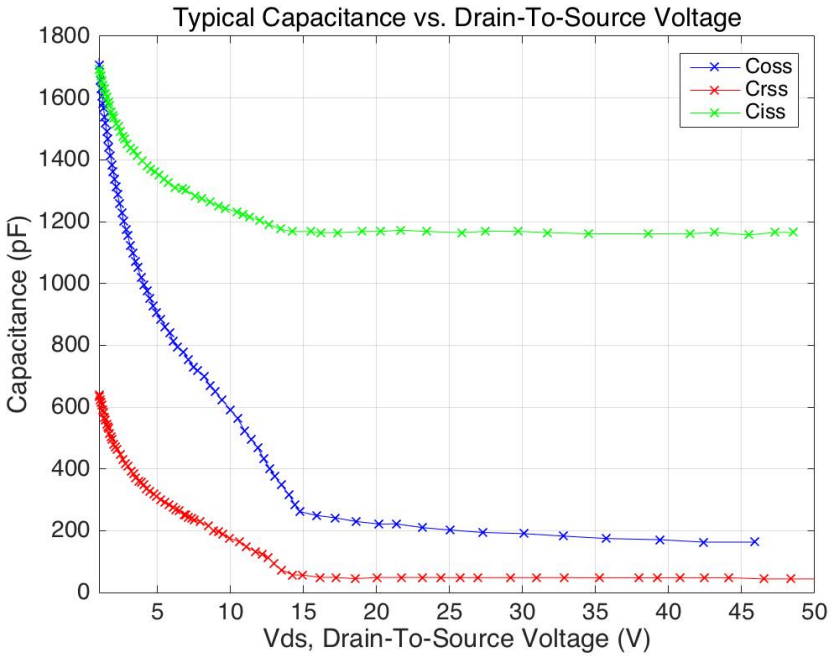


Figure 3.5: Digitized capacitance curve of *IRF*740*LC*

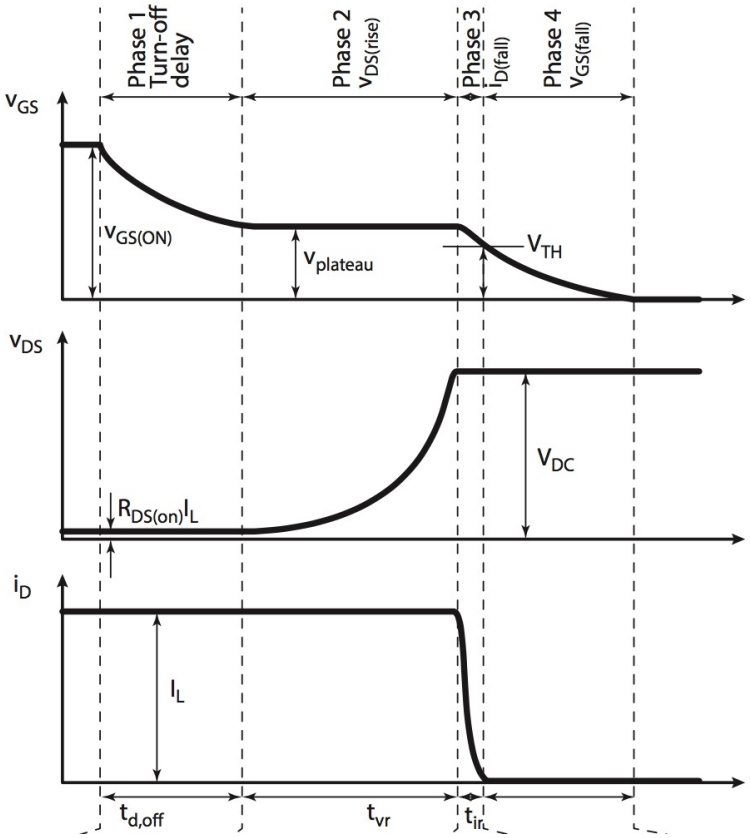


Figure 3.6: Turn-off procedure of MOSFET [36]

3.4.1. DEAD TIME MATCHING

While $IR2153D$ is a driver IC with fixed deadtime of $1.2\mu s$, it is necessary to check if $1.2\mu s$ is long enough to satisfy ZVS with the MOSFET $IRF740LC$ and the load mentioned in previous sections. Fig. 3.6 is the waveform and stage of a general MOSFET when it is turning off.
In the first phase, the gate drive voltage steps down to 0 and the gate-source voltage V_{gs} starts to decrease. This phase stops when V_{gs} decreases to the plateau voltage $V_{plateau}$. The duration time is calculated by:

$$t_{d,off} = R_G C_{iss0} ln(\frac{V_{GS(on)}}{V_{plateau}}) \tag{3.16}$$

In the second phase, V_{gs} remains at the plateau voltage and the drain-source voltage V_{ds} starts to rise until it reaches the DC bus voltage. The duration time is:

$$t_{vr} = \frac{Q_{rss} R_G}{V_{plateau}} \tag{3.17}$$

In the third phase, the load current starts to transfer from the MOSFET to the freewheeling diode and V_{ds} decreases from $V_{plateau}$ to V_{TH}. The duration time is:

$$t_{if} = R_G C_{iss,full} ln(\frac{V_{plateau}}{V_{TH}}) \tag{3.18}$$

At the end of phase 3, there is no load current conducting through the MOSFET. In phase 4, only V_{gs} discharges from V_{TH} to zero. The sum of phase 1 to 3, $t_{outgoing}$, is the time needed for gate capacitance discharging to below threshold voltage V_{TH}. At the end of phase 3, the outgoing MOSFET is fully turned off.

$$t_{outgoing} = t_{d,off} + t_{vr} + t_{if} \tag{3.19}$$

ZVS requires that the output capacitance C_{oss} of the incoming MOSFET is fully discharged before its gate drive voltage steps up. After the outgoing MOSFET fully turning off, all the load current conducts through the freewheeling diode of incoming MOSFET, discharging the C_{oss}. With conservative estimation, the time needed for C_{oss} fully discharging is given by:

$$t_{dis} = \frac{Q_{oss}}{I_{inv}} \tag{3.20}$$

where I_{inv} is the inverter output current at the switching instant.
With above analysis, for a half bridge inverter, ZVS turn-on is achieved only if, within the available dead time T_{dt} [37]:

- The gate capacitance of the outgoing MOSFET is discharged to below V_{th}, and
- The output capacitance of the incoming MOSFET is fully discharged.

Table 3.4: Parameters in Eqn. (3.16) to Eqn. (3.20) [35]

C_{iss0}	$C_{iss,full}$	$V_{GS(on)}$	$V_{plateau}$	V_{TH}	Q_{oss}	Q_{rss}
$1.7nF$	$1.15nF$	$12V$	$6.8V$	$3V$	$73.58nC$	$20.37nC$

Table 3.4 lists the parameters in Eqn. (3.16) to Eqn. (3.20) based on the datasheet of $IRF740LC$ [35]. C_{iss0} is the input capacitance C_{iss} when V_{ds} is zero. $C_{iss,full}$ is the C_{iss} when V_{ds} is $320V$. Inside $IR2153D$ there is a zener diode between V_{cc} pin and COM pin, which has a clamp voltage of $15.6V$. $V_{GS(on)}$ cannot be larger too much than that value and is set as $12V$. The inverter output current at the switching instant I_{inv} can be calculated using Eqn. (2.43). At full load condition, there is the smallest switching current for the whole load range.

$$I_{inv} = \frac{4V_{sq}}{\pi\omega L_1}\left(\frac{L_2 + L_{cable} + 20 \times L}{L_1} - 1.25\right) = -1.117A \tag{3.21}$$

If $R_G = 4.7\Omega$ and $V_{GS(on)} = 12V$, the transition time for outgoing MOSFET and incoming MOSFET are calculated as:

$$t_{outgoing} = 4.7 \times 1.7 \times ln(\frac{15}{6.8}) + \frac{20.37 \times 4.7}{6.8} + 4.7 \times 1.15 \times ln(\frac{6.8}{3})ns = 23.04ns \tag{3.22}$$

$$t_{dis} = \frac{73.58nC}{1.117A} = 65.87ns \tag{3.23}$$

$$t_{dt} = 1.2\mu s > t_{outgoing} + t_{dis} = 88.91ns \tag{3.24}$$

The fixed dead time of $IR2153D$ is much larger than the time needed to discharge gate capacitance of outgoing MOSFET and output capacitance of incoming MOSFET. Thus ZVS is assured.

3.4.2. BOOTSTRAP CIRCUIT

Bootstrap gate drive circuit is one of the most widely used methods to supply power to the high-side MOSFET. Fig. 3.7 is the topology of the bootstrap circuit. It utilizes the characteristic that capacitor voltage cannot change instantaneously. When the low side MOSFET is conducting and the high side MOSFET is off, V_s is pulled down to zero and V_{DD} charges the bootstrap capacitor C_{BOOT} through bootstrap resistor R_{BOOT} and bootstrap diode D_{BOOT}. In Fig. 3.7, the charging current is shown as a red line. When the high side MOSFET is conducting and low side is off, C_{BOOT} discharges in the blue dashed line and provides gate driver voltage to the high side MOSFET. While $IR2153D$ already integrates D_{BOOT} internally, only C_{BOOT} needs to be selected.

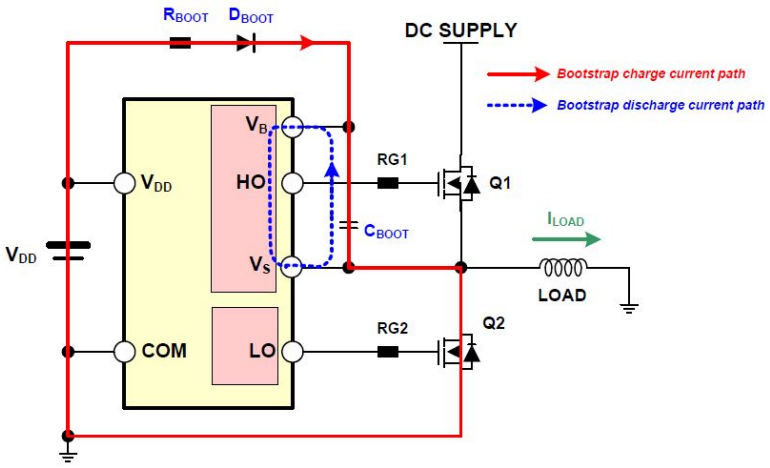


Figure 3.7: Bootstrap power supply circuit [38]

Bootstrap capacitor C_{BOOT} selection has to consider the maximum voltage drop when the high-side switch is in on state. While the datasheet of $IRF740LC$ does not provide a clear

value of the minimum gate drive voltage, with a test of $IRF740$, it is found that $\Delta V_{BOOT} = 1V$ is acceptable for $V_{GS(on)} = 12V$. The relation between C_{BOOT} and ΔV_{BOOT} is

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{BOOT}} \tag{3.25}$$

where Q_{total} is the total amount of the charge supplied by the C_{BOOT}. The main part of Q_{total} is the gate charge Q_{gate}. The maximum gate charge of $IRF740LC$ is $39nC$ [35].

$$C_{BOOT} \approx \frac{Q_{gate}}{\Delta V_{BOOT}} = \frac{39nC}{1V} = 39nF \tag{3.26}$$

With a conservative consideration, $C_{BOOT} = 68nF$ is selected.

3.5. CONTROL CIRCUIT DESIGN

3.5.1. DOUBLE FREQUENCY DRIVE USING IR2153D

In section 3.3, it is stated that the system will operate at $50kHz$ when the number of on-state pickups $N \geq 10$ and at $1.04 \times 50kHz$ when $N < 10$. This will reduce reactive power in the circuit and maintain ZVS at the same time. The aim of the control circuit is to make the system frequency switching happen automatically. Fig. 3.8 introduces how to switch the system frequency with an auxiliary capacitor C_2, which is controlled by a small-signal transistor Q_1. When the transistor is in off-state, there is no current flowing in the $C_2 - Q_1(D_1)$ branch and C_2 is out of the circuit. The frequency is high and is given by:

$$f_1 = \frac{1}{1.38(R_1 + 75)C_1} \tag{3.27}$$

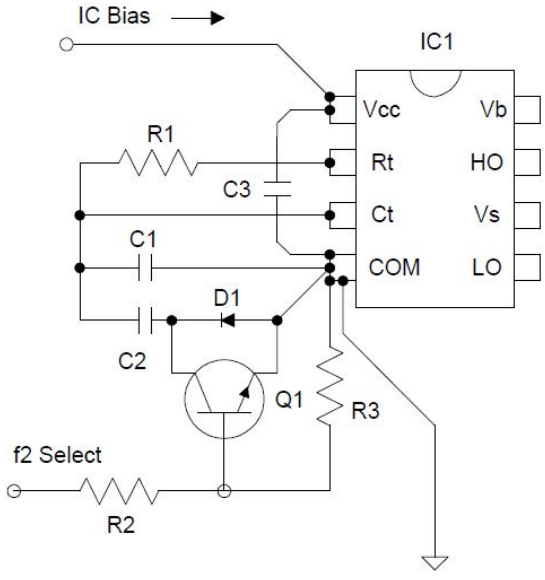


Figure 3.8: Parallel capacitor switch [34]

When the transistor is in on-state, the $Q_1(D_1)$ provides a path for C_2 to charge and discharge. The auxiliary capacitor C_2 is in parallel with C_1. The frequency is lower and is given by:

$$f_2 \approx \frac{1}{1.38(R_1 + 75)(C_1 + C_2)} \tag{3.28}$$

Because $f_1 = 1.04 * f_2$, the relation between C_1 and C_2 is deducted by:

$$\frac{C_2}{C_1} = \frac{1.38(R_1 + 75)}{1.38(R_1 + 75)} \times 1.04 - 1 = 0.04 \tag{3.29}$$

$$C_2 = 0.04 \times C_1 = 0.4nF \tag{3.30}$$

Because the total capacitance becomes larger ($10nF \rightarrow 10.4nF$), R_1 needs to be revised:

$$R_1 = \frac{1}{1.38 \times 10.4nF \times 50kHz} - 75 = 1318.5\Omega \tag{3.31}$$

3.5.2. CONTROL LOGIC AND TOPOLOGY

The next stage is to design the circuit which is able to give the signal to switch the transistor Q_1 based on load condition. The signal must be able to represent how many pickups are in the on-state. Because the current through cable and pickups is constant AC current, it is clear that the amplitude of AC voltage on the fixed point on the cable is proportional to the number of pickups in on-state. The signal flows as shown in Fig. 3.9. The voltage on the connection point between cable and LCL network is selected. The DC voltage signal $V_{check,dc}$ to Q_1 is positive proportional to the number of on-state pickups.

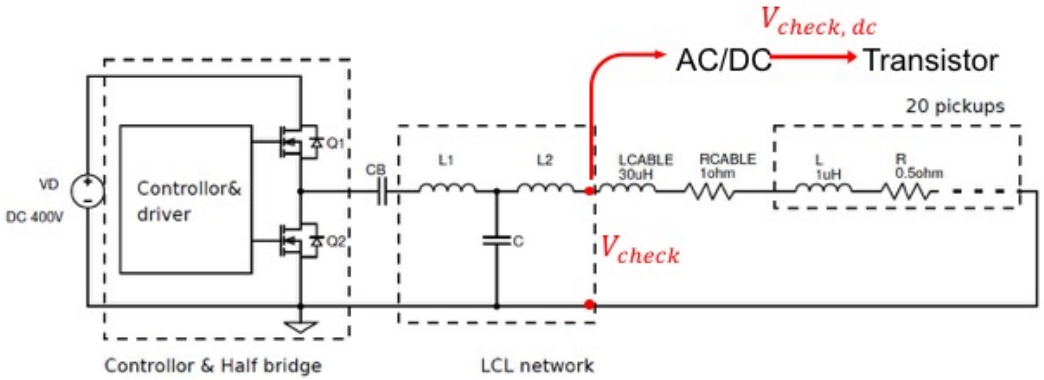
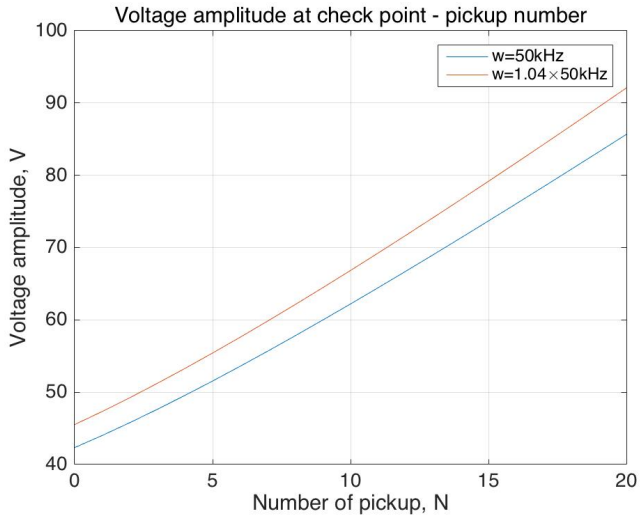


Figure 3.9: Schematic to switch Q_1

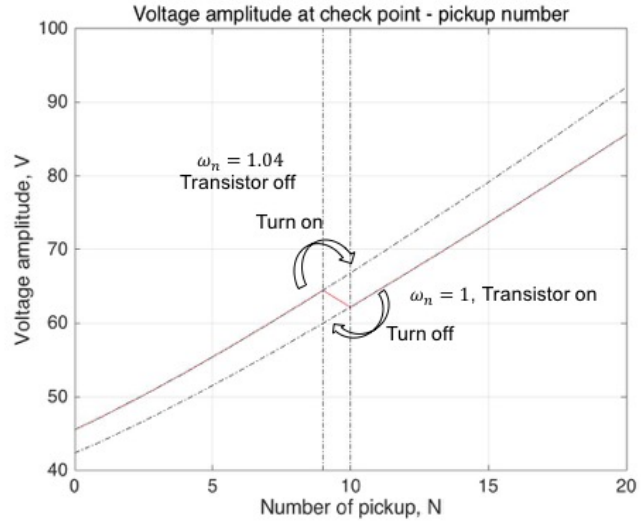
Fig. 3.10(a) depicts how the ac voltage amplitude at the check point $V_{check,ac}$ changes with number of on-state pickups. The blue line is when frequency is $50kHz$ and the red line corresponds to $1.04 \times 50kHz$. Fig. 3.10(b) shows the voltage when the system operates at $50kHz$ when $N \geq 10$ and at $1.04 \times 50kHz$ when $N < 10$. For the overall trend, $V_{check,ac}$ goes higher as more pickups are in on-state. But it is worth noting that $V_{check,ac}$ for $\omega_n = 1.04, N = 9$ is higher than for $\omega_n = 1, N = 10$. This means that the transistor Q_1 can not be turned on/off depending on a single voltage level and needs to be turned on/off at different signal voltages. The ac voltage amplitude of the two switching points are:

$$V_{check,ac(at\ \omega_n=1.04,N=9)} = 64.47V, V_{check,ac(at\ \omega_n=1,N=10)} = 62.21V \tag{3.32}$$

When the number of on-state pickups decreases, the transistor turns off at $V_{\omega_n=1,N=10} = 62.21V$. When the number of on-state pickups increases, the transistor turns on at $V_{\omega_n=1.04,N=9} = 64.47V$. This automatic frequency conversion is realized by the topology in Fig. 3.11. The ac voltage signal $V_{check,ac}$ inputs to the diode D. After the single diode D and filter capacitor C_{filter}, the ac voltage signal $V_{check,ac}$ transfers to the dc voltage signal $V_{check,dc}$. The trig pin and thrs



(a) $V_{check,ac}$ changing under different ω_n



(b) $V_{check,ac}$ changing with automatic frequency switching

Figure 3.10: Check point ac voltage amplitude changing with number of on-state pickups

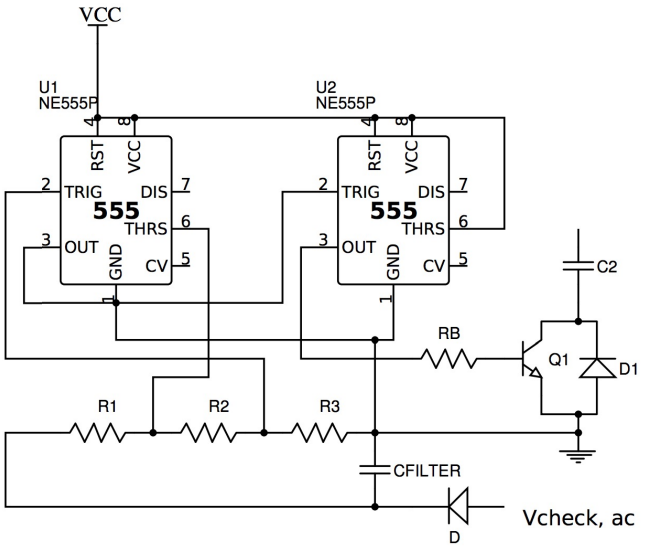


Figure 3.11: Control circuit for frequency conversion

pin of the left 555 chip are connected with the voltage divider circuit. The voltage inputs are given by:

$$V_{trig} = V_{23} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{check,dc} \tag{3.33}$$

$$V_{thrs} = V_{12} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{check,dc} \tag{3.34}$$

For the 555 chip, when V_{trig} is lower than $\frac{1}{3}V_{cc}$, the out pin steps up and when V_{thrs} is higher than $\frac{2}{3}V_{cc}$, the out pin steps down. Thus if R_1, R_2, R_3 values are set to satisfy:

$$V_{12(at\ \omega_n=1.04,N=9)} = \frac{2}{3}V_{cc} \tag{3.35}$$

$$V_{23(at\ \omega_n=1,N=10)} = \frac{1}{3}V_{cc} \tag{3.36}$$

The out pin of left 555 chip turns from low to high at $V_{check,ac(at\ \omega_n=1,N=10)} = 62.21V$ and turns from high to low at $V_{check,ac(at\ \omega_n=1.04,N=9)} = 64.47V$. The right 555 chip serves as a signal inverter. So the transistor turns on at $V_{check,ac(at\ \omega_n=1.04,N=9)} = 64.47V$ and turns off at $V_{check,ac(at\ \omega_n=1,N=10)} = 62.21V$.

Here only one diode serves as half wave rectifier for AC/DC signal conversion. The full wave rectifier topology is not used because of the problem of ground point. Fig. 3.12 shows the half-wave rectifier replaced by a full-wave rectifier. AC voltage signal is injected to point A and B. DC voltage signal is obtained at point C and D. V_{12} and V_{23} connect with $thrs$ pin and $trig$ pin seperately. However, the ground of 555 chip is the same as point B, the voltage V_{12} and V_{23} to 555 chip are acutally not DC voltage. Thus the full-wave rectifier can not be used.

Fig. 3.13 shows the input to the half-wave rectifier and output after the filter capacitor. The capacitor charges and discharges in each period and there is ripple in output DC voltage. The ripple depends on how quickly the capacitor discharges, which is represented as RC time constant. If $RC \gg T_{period}$, the capacitor discharges very slowly and there is

$$V_{check,dc} = V_{check,ac,amplitude} \tag{3.37}$$

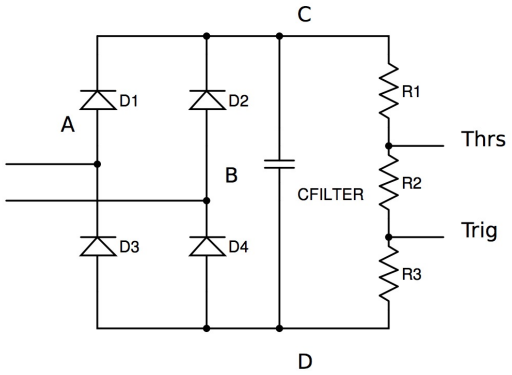


Figure 3.12: Problem of using full-wave rectifier in control circuit

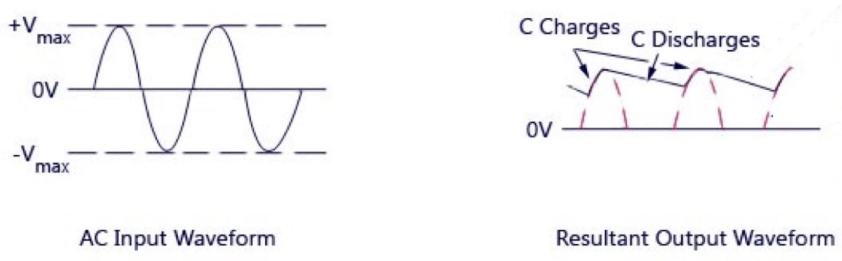


Figure 3.13: Half-wave rectifier with filter capacitor

V_{cc} is $12V$, the same as $V_{GS(on)}$. With the combination from Eqn. (3.33) to Eqn. (3.37), the resistors in voltage divider circuit are calculated by:

$$\frac{R_2+R_3}{R_1+R_2+R_3} \times V_{check,ac(at\ \omega_n=1.04,N=9)} = \frac{2}{3}V_{cc} \tag{3.38}$$

$$\frac{R_3}{R_1+R_2+R_3} \times V_{check,ac(at\ \omega_n=1,N=10)} = \frac{1}{3}V_{cc} \tag{3.39}$$

$$R_1 = 13.6226R_3, R_2 = 0.9299R_3 \tag{3.40}$$

If $R_3 = 10k\Omega$,

$$R_1 = 136.23k\Omega, R_2 = 9.3k\Omega, R_3 = 10k\Omega \tag{3.41}$$

The filter capacitor needs to be

$$C_{filter} \gg \frac{T_{period}}{R_1+R_2+R_3} = 0.13nF \tag{3.42}$$

Another point worth noting is that V_{trig} and V_{thrs} can not be larger than V_{cc}, or the 555 chip will be broken. The maximum V_{trig} and V_{thrs} are at full load.

$$V_{trig,max} < V_{thrs,max} = \frac{R_2+R_3}{R_1+R_2+R_3} \times V_{check,ac(at\ \omega_n=1,N=20)} = 10.632V < V_{cc} \tag{3.43}$$

3.5.3. TRANSISTOR AS A SWITCH

The transistor Q_1 in Fig. 3.11 operates as 'ON/OFF' type solid state switch. The operation areas for a transistor as switch is depicted in Fig. 3.14: saturation region and cut-off region.

Saturation region represents transistor fully-on and cut-off region represents transistor fully-off. In the cut-off region, because there is no base current I_b, the current through the collector I_c is zero. The switch is off. In saturation region, the maximum amount of base current is applied, thus maximum collector current is allowed to flow with minimized collector-emitter voltage drop. The switch operates in on-state.

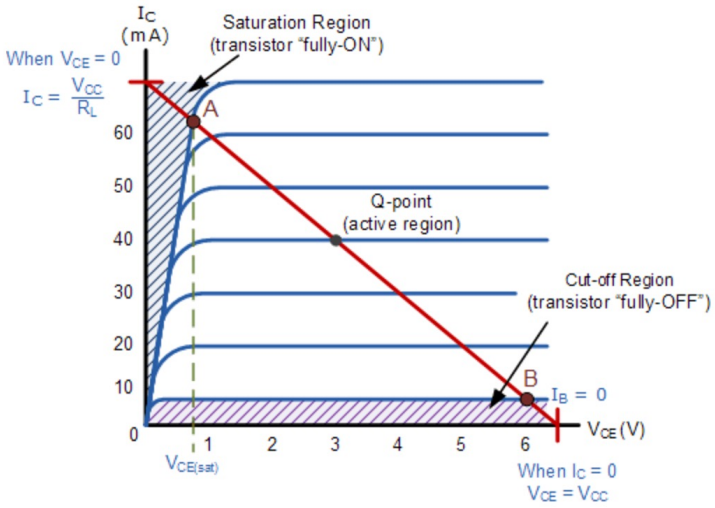


Figure 3.14: Operation areas for a transistor switch [39]

$BSX20$ is selected as the type of the transistor. In the datasheet [40], for the test condition of

$$I_c = 10mA, I_B = 1mA \tag{3.44}$$

the base-emitter saturation voltage

$$V_{BE,sat} = 0.7V \sim 0.85V \tag{3.45}$$

While for the IR2153D the previous design is

$$V_{cc} = 12V, R = 1318.5\Omega, C = 10.4nF \text{ or } 10nF \tag{3.46}$$

the charging and discharging current flowing through the collector

$$I_C < \frac{1}{3}\frac{V_{cc}}{R} = 3.04mA < 10mA \tag{3.47}$$

This means when $V_{BE} = 0.85V, I_B = 1mA$, the transistor $BSX20$ can act as an on-state switch. The bipolar resistor R_B will be

$$R_B = \frac{V_{out,555} - V_{BE,sat}}{I_B} = 11.15k\Omega \tag{3.48}$$

3.6. CHAPTER SUMMARY

This chapter provides a procedure of the power supply design based on the analysis of LCL network in chapter 2. The LCL network, the half bridge inverter and the control circuit are

designed one by one in this chapter. The LCL network is calculated based on the power demand from the load. The half bridge inverter is determined to supply the power and ensure ZVS. The control circuit is designed to switch the frequency according to the load condition. The following points have been determined:

- The topology to realize frequency switching is determined.
- The size of driver IC, MOSFET and transistor are selected.
- The value of passive components are calculated.

4

SIMULATION AND EXPERIMENT VALIDATION

4.1. INTRODUCTION

This chapter simulates the designed circuit from chapter 3 and validates it in the experiment. Since there is no LTspice model of driver IC $IR2153D$, the simulation is divided into two parts: the control circuit and the half bridge inverter. The simulation result is first depicted and then the analysis is given. The modification of the circuit will be proposed based on the analysis.
A prototype circuit is constructed after the simulation. The parameters of the setup are first introduced. After that experimental results are depicted and analyzed. Futhermore, a lighting pickup is also integrated into the circuit and measured.

4.2. SIMULATION

4.2.1. CONTROL CIRCUIT SIMULATION

A simulation model of the control circuit is built in LTspice as shown in Fig. 4.1. The LTspice model of $BSX20$ is from [41]. The output of the right 555 timer provides the base-emitter voltage to the transistor Q_1. A voltage source V_{test} and a resistor R_{test} are in series with the transistor Q_1 to check if Q_1 is conducted or not. The result is depicted in Fig. 4.2. The blue curve corresponds to the signal voltage connected to the dividers (R_1, R_2, R_3). It is set to fall and rise between $75V$ and $55V$. The red curve is the base-emmitter voltage V_{BE} at the transistor Q_1. V_{BE} steps down and up at different signal voltage and controls the current through Q_1 (the green curve $I_c(Q_1)$ in Fig. 4.2).

4.2.2. HALF BRIDGE SIMULATION

The half bridge inverter is built in Fig. 4.3. The model of $IRF740LC$ is defined based on the code given on [42]. While there is no LTspice model of $IR2153D$, the parameters of $IR2153D$ are typed in voltage sources which are placed at the gate of $IRF740LC$.
For $50kHz$ frequency generation:

$$t_{on} = 8.8\mu s, t_{period} = 20\mu s, t_{rise} = 80ns, t_{fall} = 45ns, V_{on} = 12V \tag{4.1}$$

For $52kHz$ frequency generation:

$$t_{on} = 8.41\mu s, t_{period} = 19.23\mu s, t_{rise} = 80ns, t_{fall} = 45ns, V_{on} = 12V \tag{4.2}$$

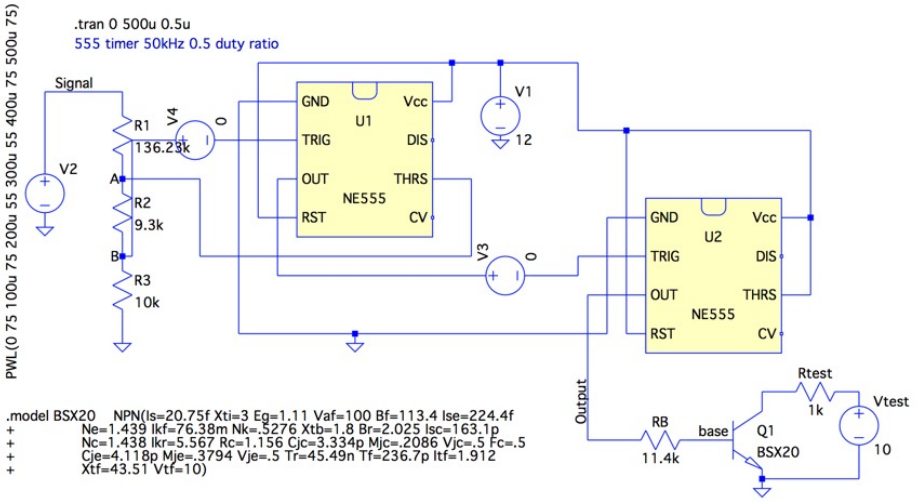


Figure 4.1: Simulation verification of the control circuit

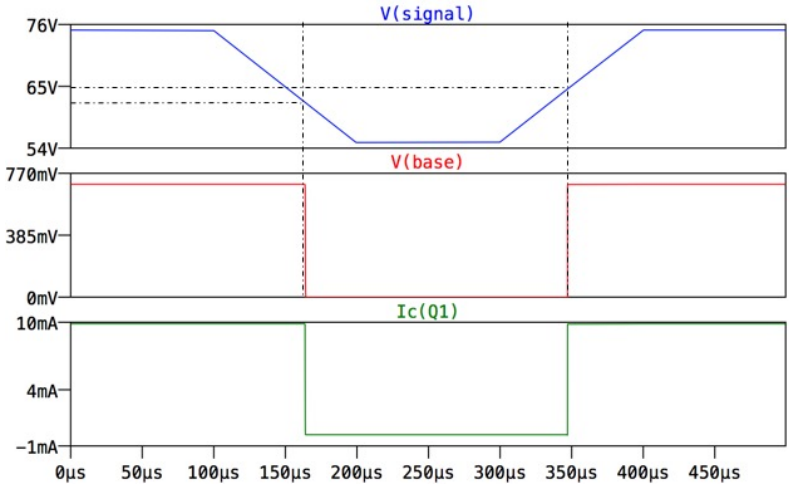


Figure 4.2: Simulation result of the control circuit

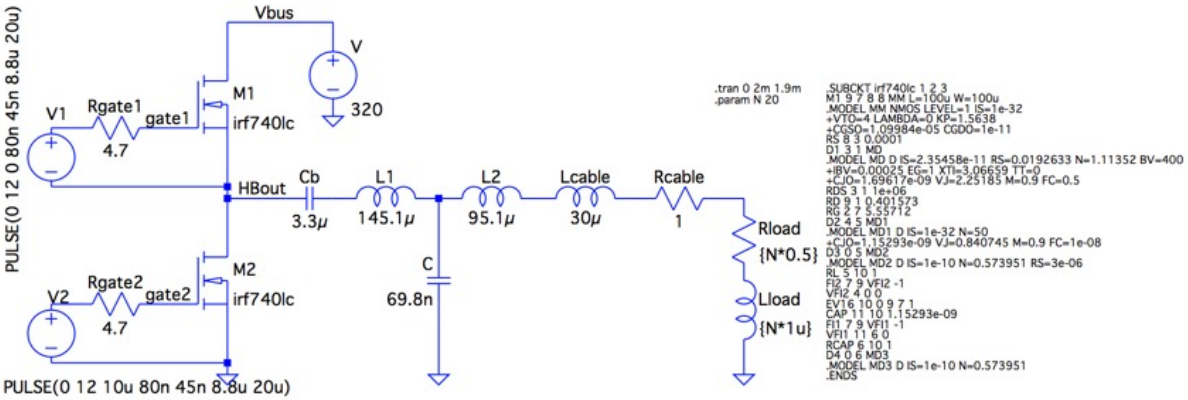


Figure 4.3: Simulation of half bridge inverter

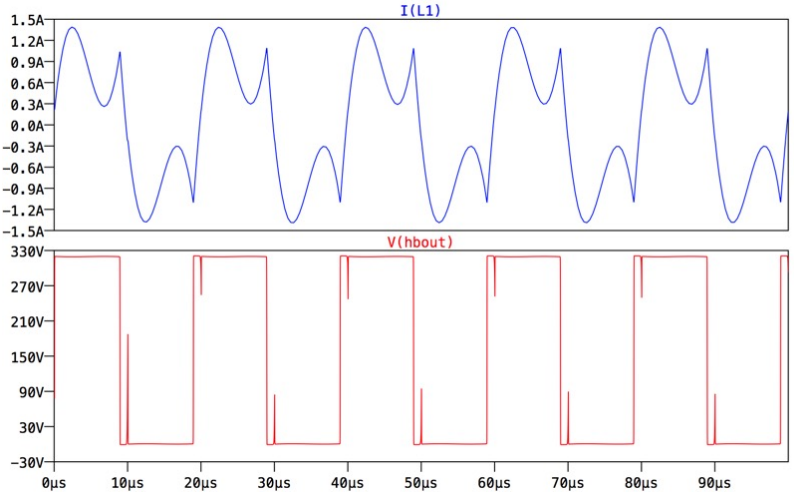


Figure 4.4: Inverter output voltage and current at $N = 20$

The output voltage and current of the inverter for $N = 20$ are shown in Fig. 4.4. The blue curve is the current through the inductor L_1. The red curve is the voltage at point $HBout$. There are unexpected peaks in the waveform of V_{HBout}.

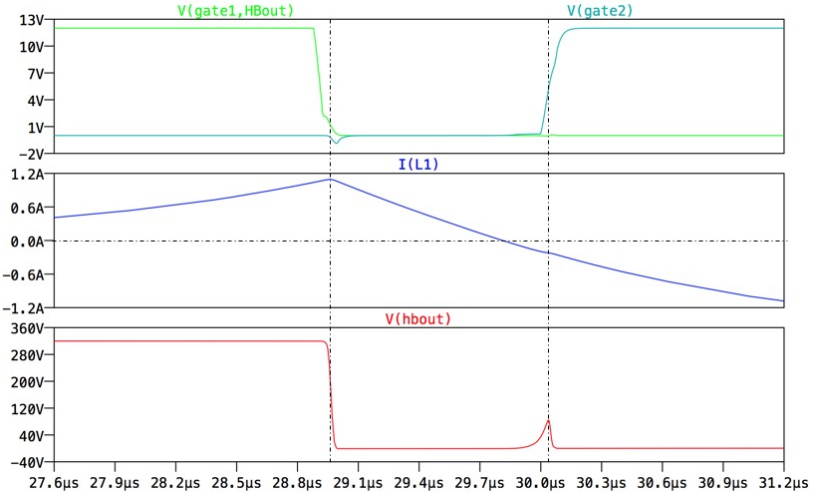


Figure 4.5: Output waveform at switching instant at $N = 20$ (up MOSFET turning off and down MOSFET turning on)

An expansion of the waveforms at switching instant (up MOSFET turning off and down MOSFET turning on) is shown in Fig. 4.5. The green and blue-green curves are the gate-source voltage at the MOSFETs. Time between the two vertical dash lines is the dead time between the two MOSFETs switching. When the MOSFET on the up branch turns off, the output current flows switching from the up MOSFET to the freewheeling diode of the down MOSFET and discharges the output capacitance of the down MOSFET. However, the direction of output current flowing changes during the dead time before the down MOSFET turning on, which is shown in the middle graph in Fig. 4.5. The output current flows switching from the freewheeling diode of the down MOSFET to the freewheeling diode of the up MOSFET. After the output capacitance of up MOSFET discharges, the voltage at the middle point of two MOSFETs the rising again. In Fig. 4.5, what has to be noticed is that the voltage across the drain and source of down MOSFET is not zero when it turns on. ZVS at turning on is lost

because of the peaks in the output voltage.
The solution is to reduce L_2. According to Eqn. (2.43), a smaller L_2 can increase the magnitude of inverter current (the calculated I_{inv} is negative) at switching instant, thus inverter current is prevented from changing direction during dead time. After several attempts in the simulation, the value of L_2 is reduced to:

$$L_2 = 95.1\mu H \rightarrow L_2 = 90\mu H \tag{4.3}$$

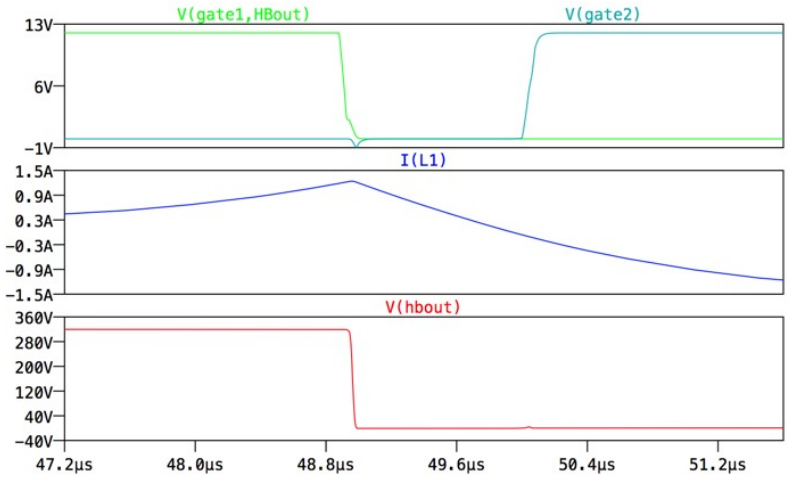


Figure 4.6: Output waveform at switching instant at $N = 20$ with $L_2 = 90\mu H$ (up MOSFET turning off and down MOSFET turning on)

Waveforms in Fig. 4.6 are plotted under $L_2 = 90\mu H$ and there is no voltage peak in V_{inv}. ZVS is realized. According to section 3.3, $50kHz$ is the operation frequency for $N = 10 \sim 20$ and $52kHz$ is the operation frequency for $N = 0 \sim 9$. With the revised L_2, there are no voltage peaks appearing in dead time and ZVS is implemented under all load conditions. The rms

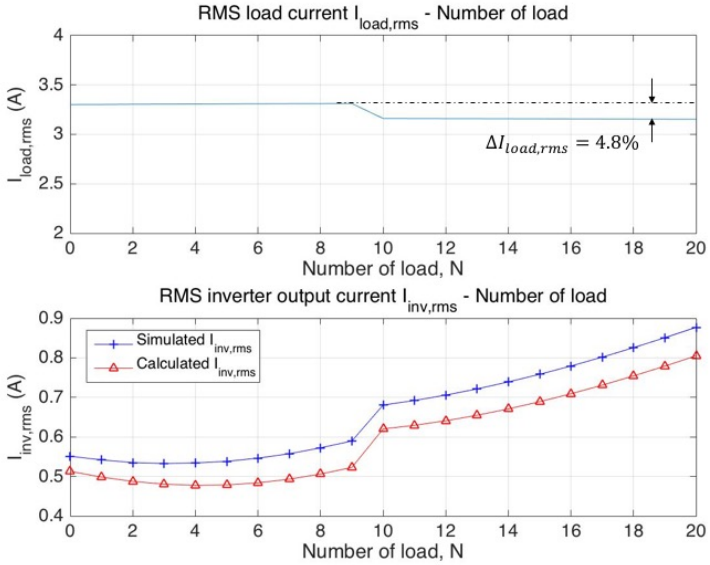


Figure 4.7: RMS value of load current and inverter output current

value of load current and inverter output current are depicted in Fig. 4.7. The maximum

load current variation during the load range is $\Delta I_{load,rms} = 4.8\%$, which is allowed for the load. In Fig. 4.7, the overall trend of rms inverter output current is increasing as the load number increases. There is a sudden change of $I_{inv,rms}$ at $N = 9$ and $N = 10$, which indicates that $I_{inv,rms}$ has a step down when frequency switches from $50kHz$ to $52kHz$. The calculated $I_{inv,rms}$ are also plotted based on Eqn. (2.50). The error could result from dead time and the ignorance of higher (> 3) order harmonics.
Fig. 4.8 depicts the power variation curves. The real power P received by each load under $52kHz$ is slightly higher than under $50kHz$ due to the relatively higher $I_{load,rms}$ shown in Fig. 4.7. The curve of apparent power S corresponds to $I_{inv,rms}$. Fig. 4.9 shows a comparison of the ratio of apparent power and real power S/P at the inverter output when there is frequency switching and there isn't frequency switching. When $N < 10$, power ratio S/P operating at $52kHz$ (red curve with triangle) is clearly smaller than operating at $50kHz$ (blue curve with cross).

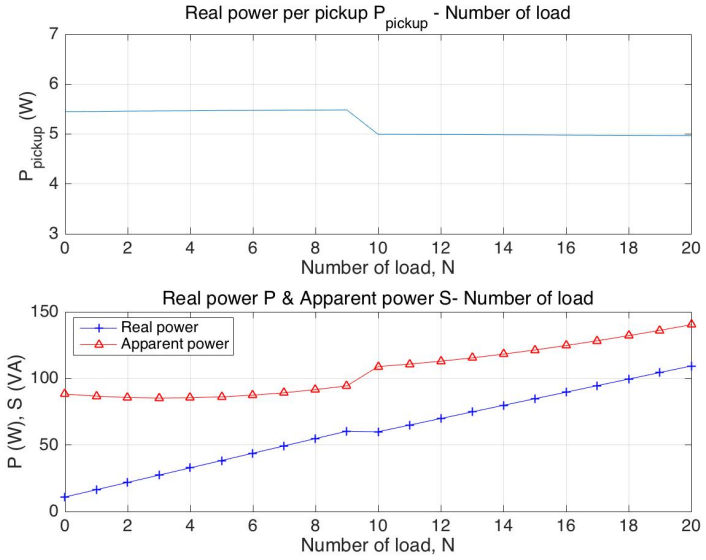


Figure 4.8: Real power and apparent power consumed by the circuit

In conclusion, the simulation result proves that with the given circuit design and the control strategy of switching to even higher frequency for smaller number of load:

- The load current varies within 4.8%, which is acceptable for the pickups.
- ZVS is maintained under all load condition.
- Apparent power has a certain reduction, compared to constant frequency operation.

4.2.3. HIGH ORDER HARMONICS MODIFICATION

In the previous design process, a necessary condition to realize ZVS is that, under first harmonic analysis (FHA), the phase angle of input impedance (at the output of inverter) must be larger than zero so the inverter output current can first discharge the output capacitance before the MOSFET turns on. Fig. 3.2(a) shows that if $\omega_n = 1.04$, the higher frequency $1.04 \times 50kHz$ can only serve for $N = 0 \sim 9$.
However, this is too conservative when taking the high order harmonics into account. Eqn. (2.39) and Eqn. (2.43) give the inverter output current at the switching instant under only FHA and including high order harmonics. A waveform comparison of them is plotted in Fig.

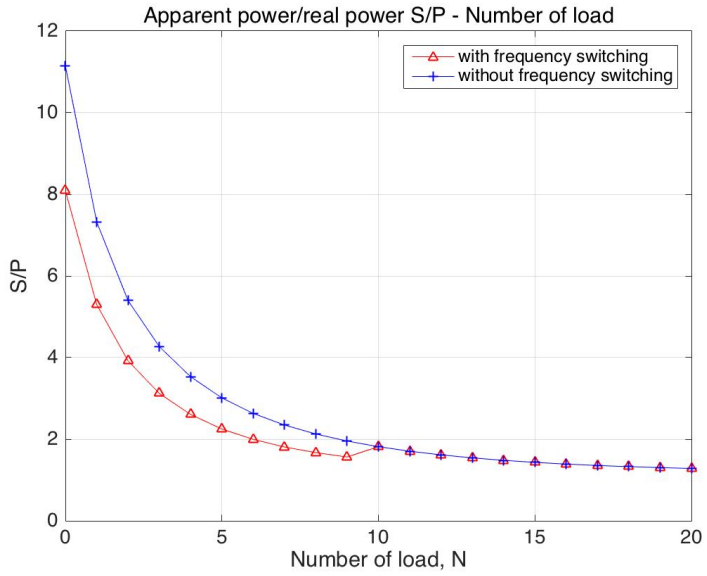


Figure 4.9: Apparent power dividied by real power with/without frequency switching

4.10 under the same load condition. The vertical dash dot line represents the switching instant of up MOSFET turning off and down MOSFET turning on. The red curve is under only FHA and the blue curve is under FHA plus high order harmonics. It clearly can be seen from the figure that the blue curve has a larger value than the red curve at the instant of vertical dash dot line. As indicated by Eqn. (2.39) and Eqn. (2.43), for both conditions, the current at the switching instant gets higher when the load becomes smaller and gets smaller when the load becomes larger, which are shown in Fig. 4.10 with arrows.

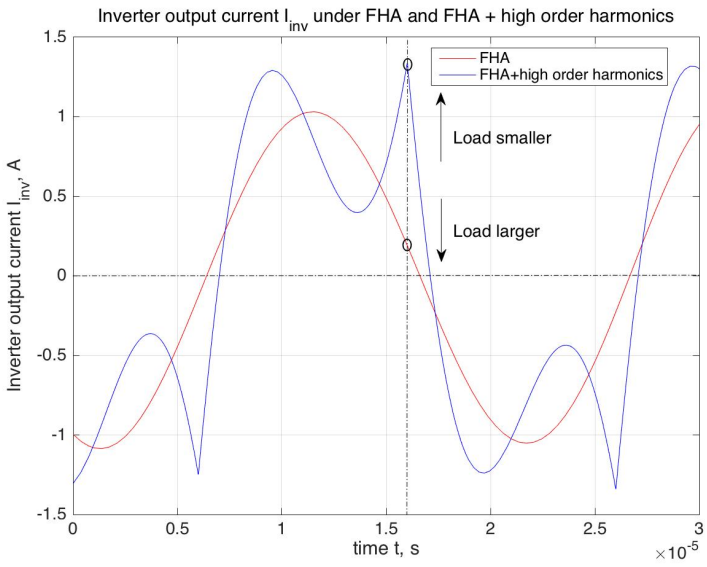


Figure 4.10: A comparison of inverter output current at switching instant between under FHA and under FHA+high order harmonics

At the switching instant of up MOSFET turning off and down MOSFET turning on, if $N \geq 10$ and the frequency is $1.04 \times 50kHz$, the inverter output current is negative and leads the output voltage under FHA. But with a combination of high order harmonics the inverter output

current at that moment can still be positive. There is a potential to enlarge the working area of the higher frequency of $1.04 \times 50kHz$. It must be taken care that Eqn. (2.43) can not be directly used to estimate the working area due to the existence of the dead time, because the current falls during the dead time. The appropriate range needs to be determined in the simulation. Fig. 4.11 is the attempt to find the range in simulation. The waveforms are plotted under $\omega_n = 1.04$ and $N = 9 \sim 13$. The red curve and blue-green curve are the gate-source voltage at the MOSFETs. The green curve is the output voltage of the inverter and the blue curve is the current at the output of inverter. There is a small voltage peak in inverter output voltage when $N = 13$. As N decreases, the voltage peak disappears. Therefore, the frequency switching point is for $N \geq 13$, $f = 50kHz$ and for $N < 13$, $f = 1.04 \times 50kHz$.

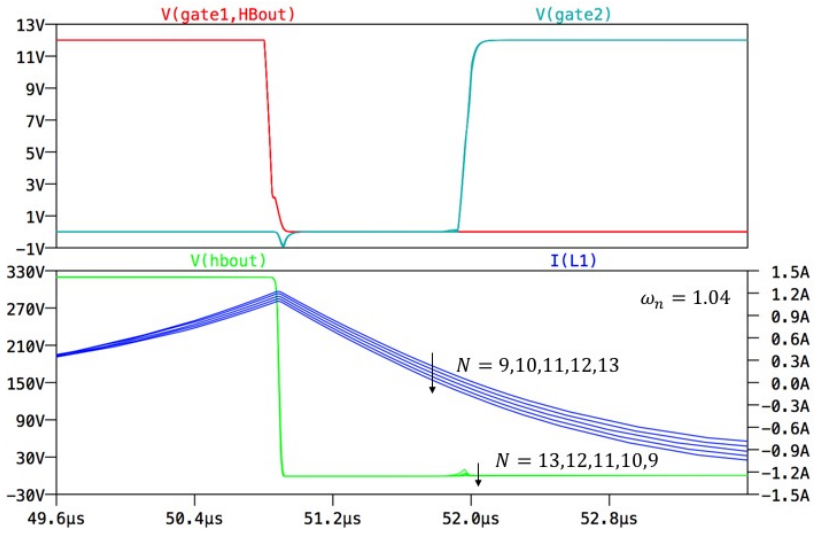


Figure 4.11: The attempt to find appropriate range of the working area of $1.04 \times 50kHz$

4.2.4. SIMULATION CONCLUSION

So far the simulation result of the proposed circuit is given. The simulation of control circuit shows a result consistent with the design. The external capacitor can be connected or disconnected to the driver IC according to the load condition. In the simulation of the half bridge inverter, the ZVS is damaged according to the design in chapter 3 because of the long dead time. While the dead time is fixed by the driver IC and can not be revised, the solution is to increase the inverter output current at the switching off instant to prevent the current changing direction during the dead time. So the inductor L_2 is reduced. Furthermore, improved modeling utilizing the high order harmonics is discussed. A larger working area of the higher frequency is defined based on the simulation. The experiment will be introduced in the following sections.

4.3. EXPERIMENT

4.3.1. EXPERIMENT SETUP

According to the schematic in Fig. 4.12 and parameters in Table. 4.1, the circuit is constructed as shown in Fig. 4.13. $C_6 = 1\mu H$ in Fig. 4.12 is a capacitor parallel to the MOSFETs and stabilizes V_d. C_4 in Fig. 4.12 is a capacitor series connected at the output of the inverter to filter the ouput DC component and here a big capacitor of $4.7\mu F$ is used to minimized its influence on the AC component. R_{L_1} and R_{L_2} are the resistance of the inductors L_1 and L_2. The number of loads in on-state is adjusted by manual switches, which are the red objects shown

in Fig. 4.13(b). Fig. 4.14 is the $k-Q$ curve of the 0 ~ 20 loads for the constructed circuit.

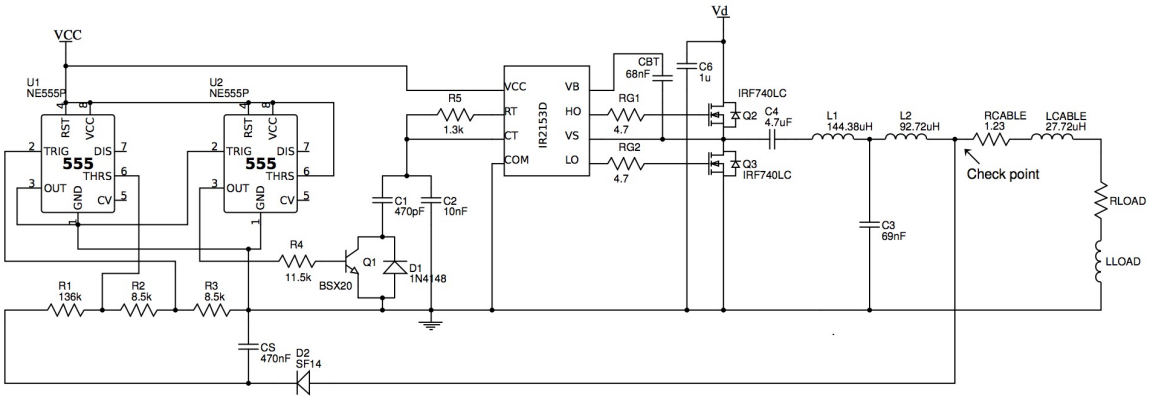


Figure 4.12: The complete schematic of power supply and load

Table 4.1: Experiment parameters

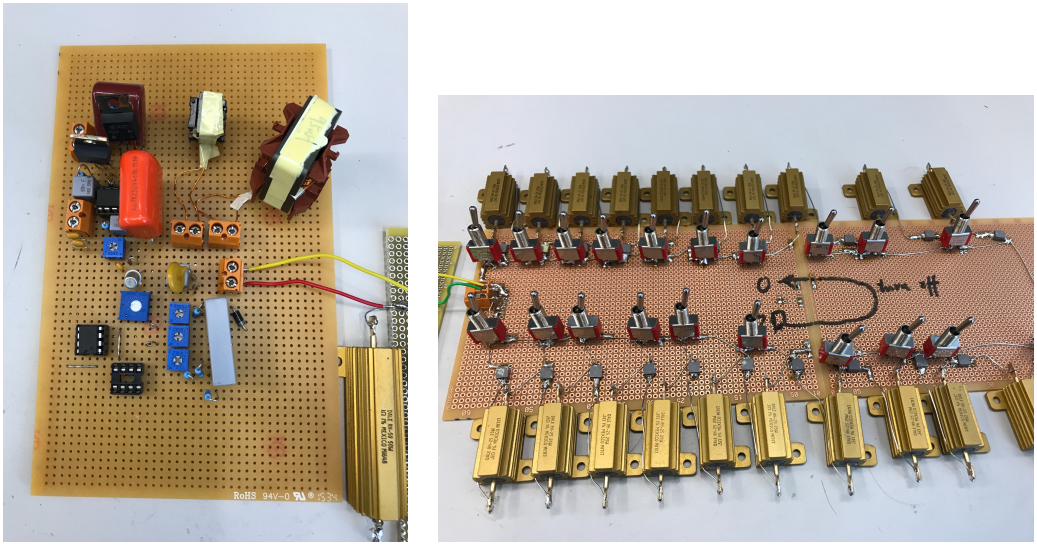
Parameter	Value	Parameter	Value
V_d	$320V$	L_{cable}	$27.73\mu H$
L_1	$144.38\mu H$	R_{cable}	1.23Ω
L_2	$92.72\mu H$	$L_{N=20}$	$22.95\mu H$
C	$69nF$	$R_{N=20}$	10.39Ω
R_{L_1}	0.61Ω	f_1	$50.04kHz$
R_{L_2}	0.19Ω	f_2	$52.40kHz$

4.3.2. EXPERIMENT WITH RL LOADS

The built setup in Fig. 4.13 is powered with $12V$ to the driver and control circuit and then added $V_d = 320V$ to the half bridge. If the sequence of turning on is opposite, the circuit will get burned. Data and graphs are first recorded with automatic frequency switching, $50.4kHz$ for $N = 13 \sim 20$ and $52.4kHz$ for $N = 0 \sim 12$. Afterwards the measurement is done with constant frequency operation to make a comparison.

Fig. 4.15 shows the waveforms of inverter output voltage V_{inv} (red), inverter output current I_{inv} (green), gate source voltage of the up branch MOSFET V_{gate1} (blue) and gate source voltage of the down branch MOSFET V_{gate2} (yellow) at $N = 20, f = 50.03kHz$. There is no obvious ripple in the waveforms of the half bridge output voltage and current. A negative voltage appears in the waveform of V_{gate1}. This is because during the commutation, the inductive parasitic elements of the two MOSFETs will drag the central point voltage of the half bridge below ground. Fig. 4.16 shows the waveforms of the ac and dc voltage at the check point V_{check} (red, blue) and the load current I_{load} (green). The waveform of ac voltage at the check point $V_{check\ ac}$ is not distorted by the control circuit. The waveform of dc voltage at the check point $V_{check\ dc}$ is close to the maximum vaule of $V_{check\ ac}$ due to the large smoothing capacitor. In Fig. 4.16, at $N = 20$, $V_{check\ dc} = 88.6V$ and the amplitude of $V_{check\ ac}$ is $175.2V$. A voltage divider consisting of higher resistors (ten times of the existed) is also tried in the experiment. With the higher resistors, voltage at the trig and thres pin to 555 is sensitive to the ripples in the control circuit because the current flowing in the voltage divider is only $\sim 10\mu A$.

Fig. 4.17 shows the waveforms at $N = 14, f = 52.40kHz$, which is considered to be not allowed



(a) The power supply (b) The load of resistors and inductors

Figure 4.13: The power supply with the load of resistors and inductors

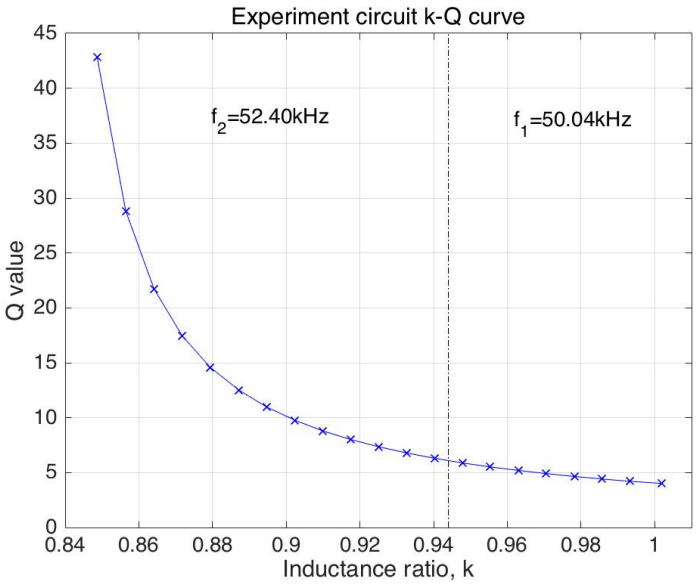


Figure 4.14: $k-Q$ curve of experiment circuit for $0 \sim 20$ load

Figure 4.15: The waveform of $V_{inv}(red), I_{inv}(green), V_{gate1}(blue)$ and $V_{gate2}(yellow)$ at $N = 20$

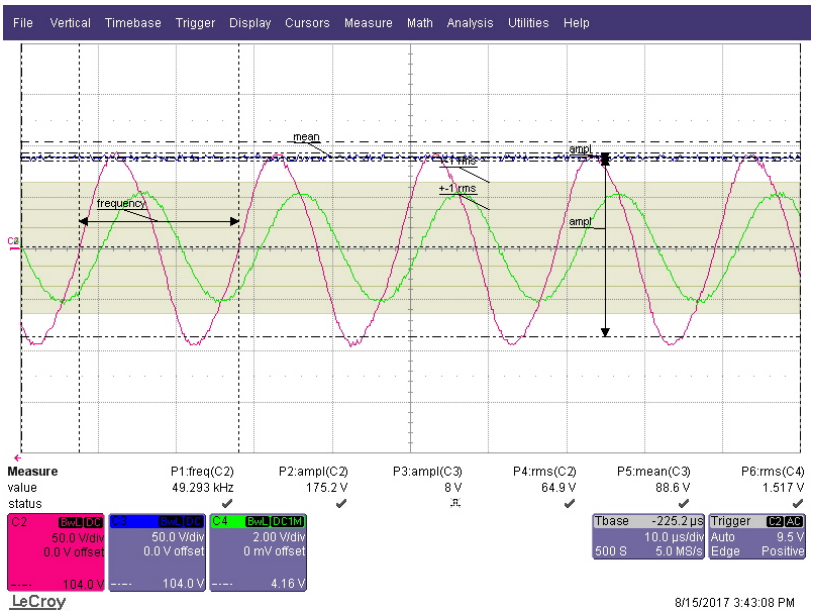


Figure 4.16: The waveform of $V_{check\ ac}(red)$, $I_{load}(green)$ and $V_{check\ dc}(blue)$ at $N = 20$

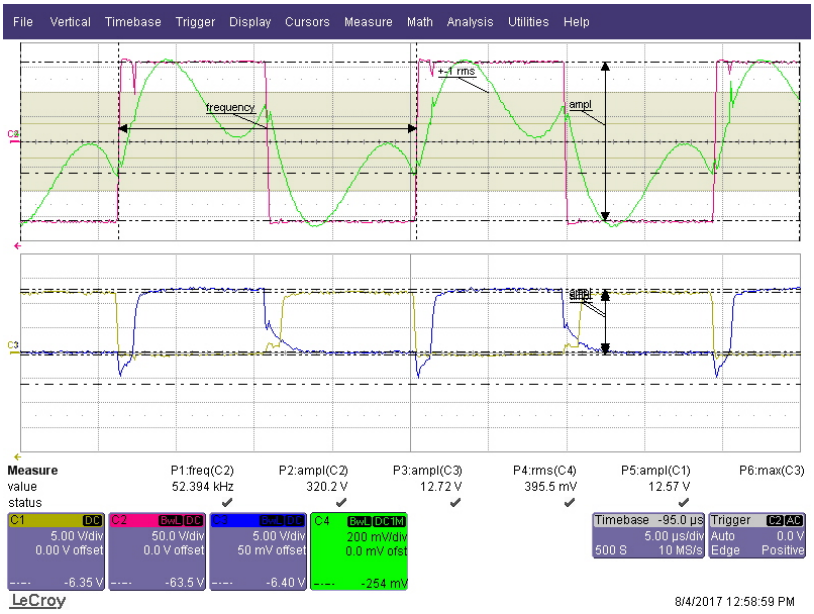


Figure 4.17: The waveform of $V_{inv}(red), I_{inv}(green), V_{gate1}(blue)$ and $V_{gate2}(yellow)$ at $N = 14$

in the design (should be at $50.04kHz$) because of the voltage peaks in the inverter output voltage. The experiment verifies the border of the operating frequency in the design.

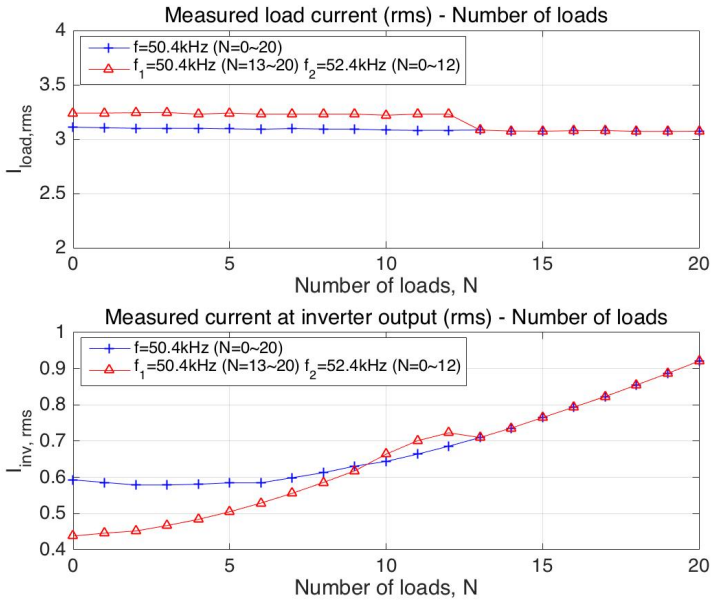


Figure 4.18: Measured load current and measured inverter output current

Fig. 4.18 shows the measured rms value of the load current $I_{load,rms}$ and the inverter output current $I_{inv,rms}$ for different number of loads in the experiment. The blue curve corresponds to the circuit working at the same frequency $f = 50.4kHz$ for the whole load range. The red curve corresponds to the circuit working at $f = 50.4kHz$ for $N = 13 \sim 20$ and at $f = 52.4kHz$ for $N = 0 \sim 12$. In the above graph, the load current $I_{load,rms}$ at $N = 0 \sim 12, f = 52.4kHz$ is around $3.23A$ and $I_{load,rms}$ at $N = 13 \sim 20, f = 50.4kHz$ is around $3.07A$. The difference is 5%. The small variation of load current ensures that the real power received by each load has only a small

change. In the below graph, when the load $N < 8$, the inverter output current $I_{inv,rms}$ has a clear reduction at $f = 52.4kHz$ compared to $f = 50.4kHz$. For $N = 10 \sim 12$, $I_{inv,rms}$ at $52.4kHz$ is even higher than $I_{inv,rms}$ at $50.4kHz$. There are several reasons that could lead to this:

1. A trimmer resistor is selected as the timing resistor in the driver IC $IR2153D$. The value of that resistor could have minor deviation from the designed value as the number of load changes, which causes frequency fluctuations and leads to the change of inverter output current.

2. There are ripples in the voltage divider of the control circuit. Since $V_{check,ac(at\omega_n=1.04,N=9)}$ and $V_{check,ac(at\omega_n=1,N=10)}$ has only a difference of $2V$, the ripples could lead the bipolar transistor in on-state (then the lower operation frequency) when the number of load is just below 12 (like 11, 10 and 9), which does not meet the expectation.

Therefore, for a lower $I_{inv,rms}$ in the constructed circuit, frequency $52.4kHz$ should be only for $N = 0 \sim 8$. But the overall trend of I_{inv} is the same as the design.

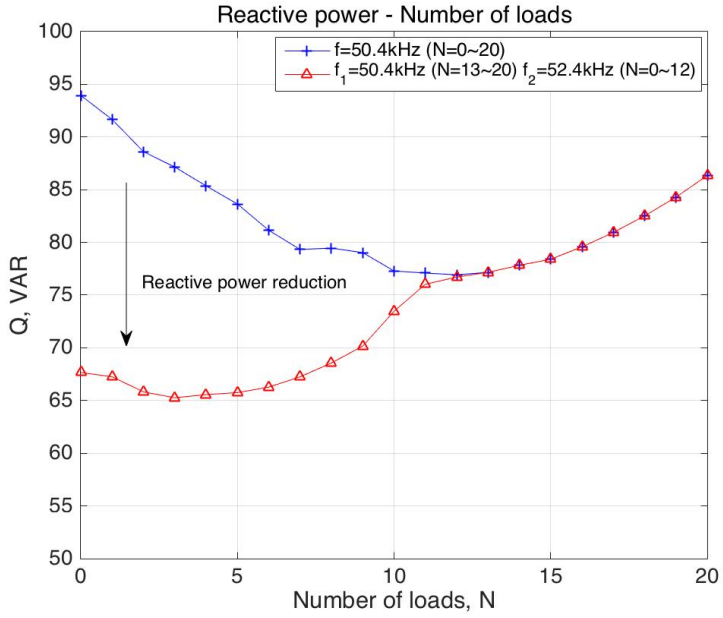


Figure 4.19: Measured reactive power at the output of the inverter

Fig. 4.19 depicts the reactive power measured at the output of the inverter. The red curve represents the power supply operating with automatic frequency switching. The blue curve represents the power supply with constant frequency operation. As the number of loads N decreases, the reduction of reactive power by the higher frequency is more obvious. When the load $N < 3$, $Q_{52.4kHz}$ is only $\frac{3}{4}$ of $Q_{50.4kHz}$.
$\frac{kVA}{kW}$, the ratio between apparent power and real power at the output of the inverter, is the goal function used in chapter 2 to describe how much apparent power is needed for the specific real power demand. In the analysis of chapter 2, the losses in the passive components are not taken into account. Hence Fig. 4.20 shows the ratio between the apparent power at the output of inverter and the real power received by the load. As the number of load gets smaller, the needed apparent power for unit real power consumption increases, but the higher frequency can give improvement. When $N = 1$, at $50.4kHz$, it needs $16.5VA$ for unit real power consumption, but only $11.6VA$ at $52.4kHz$.

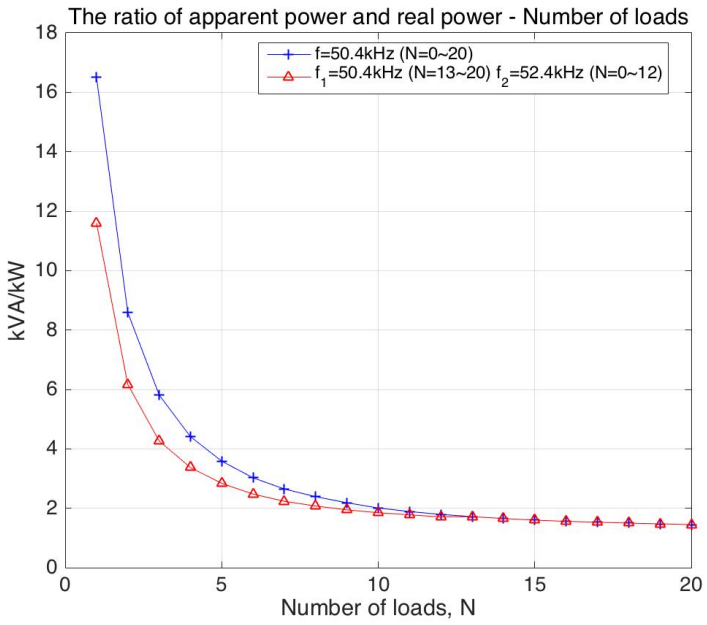


Figure 4.20: The ratio between apparent power at the output of the inverter and the real power consumed by the load

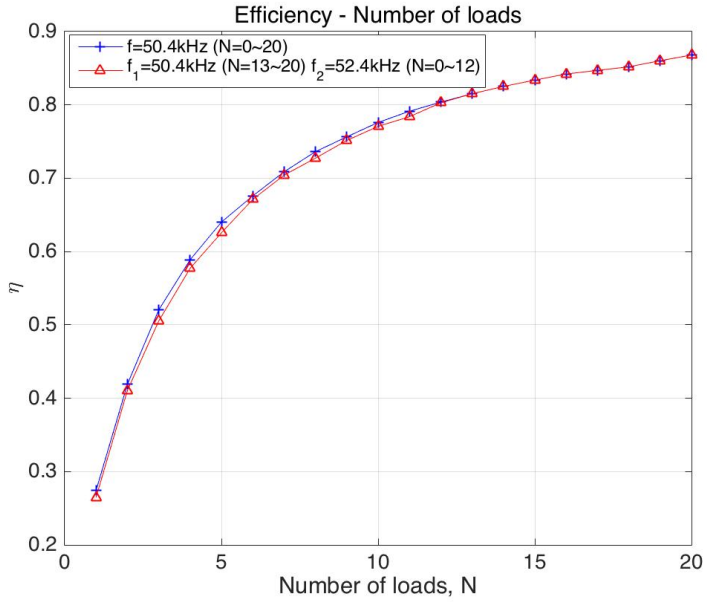


Figure 4.21: Efficiency of the power supply in the experiment

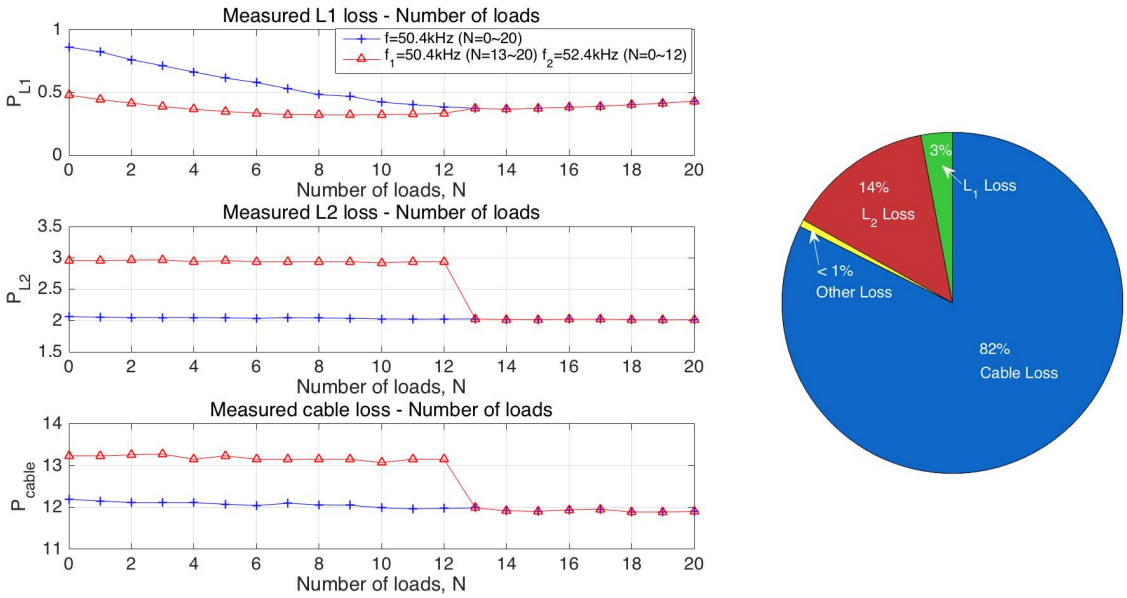


Figure 4.22: Measured Losses (left) and losses distribution at $N = 20,\ f = 50.4kHz$ (right)

Fig. 4.21 is the efficiency of the power supply. And the same as previous graphs, the red curve represents the operation with automatic frequency switching and the blue curve represents the constant frequency operation. Although in Fig. 4.19 the reactive power is reduced a lot under automatic frequency switching, the efficiency actually does not have apparent difference.

Fig. 4.22 shows the measured losses changing with different number of loads and how they distribute at $N = 20,\ f = 50.4kHz$, which explains the reason that the efficiency does not have clear difference. The losses in the circuit mainly consist of inductor L_1 loss, inductor L_2 loss and cable loss. The losses in the MOSFET and capacitors are much more smaller than these three. The left graph shows that P_{L1} decreases with the automatic frequency switching at the light load but P_{L2} and P_{cable} get even higher. The right graph in Fig. 4.22 shows that the cable loss is the largest loss, which takes a part of 82% at $N = 20,\ f = 50.4kHz$, and inductor L_2 loss is the second, which is 14% at $N = 20,\ f = 50.4kHz$. With the automatic frequency switching, $I_{inv,rms}$ has a clear reduction at light load and this helps to reduce $P_{L1,loss}$ and $P_{loss,MOSFET}$. However, these two losses are not the main loss in the circuit. The two main losses P_{L2} and P_{cable} are even higher with the control. Thus automatic frequency control does not help to increase the efficiency.

4.3.3. EXPERIMENT WITH LIGHTING PICKUP

Since the whole circuit design aims to power the lighting pickup, a lighting pickup is integrated into the load. The parameters of the pickup and the measured value are depicted in table 4.2. Fig. 4.23 shows the powered lighting pickup and Fig. 4.24 shows the waveforms of the voltage drop on the lighting pickup V_{pickup} (red) and the current through it I_{pickup} (green). The pickup can be lighted up with the constructed circuit but it needs a detailed design in the future to make it working efficiently.

Table 4.2: Parameters of the integrated lighting pickup

Parameter	Value	Parameter	Value
N_1	2	U_{rms}	$3.49V$
N_2	15	I_{rms}	$3.09A$
l_{air}	$0.2mm$	P	$4.06W$
		S	$10.83VA$

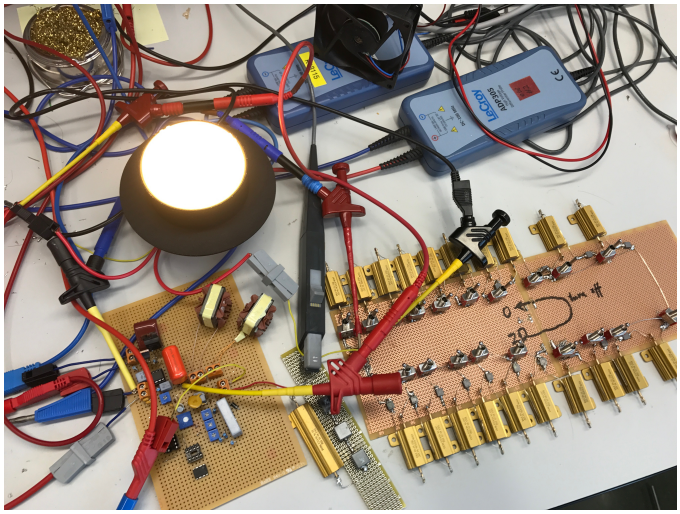


Figure 4.23: The integrated lighting pickup

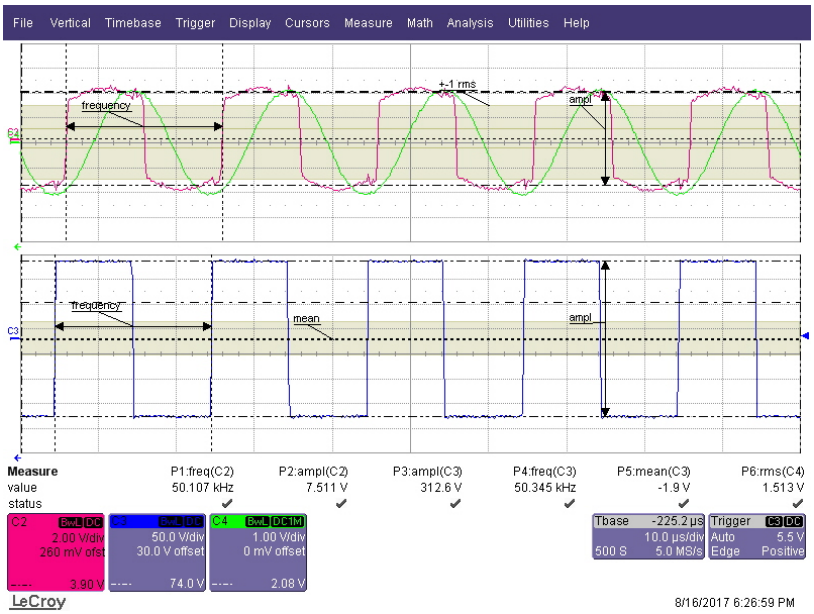


Figure 4.24: The waveforms of V_{pickup} (red), I_{pickup} (green) and V_{inv} (blue)

4.3.4. EXPERIMENT CONCLUSION

The information of the experiment and the measured result are introduced after the simulation. The constructed power supply is first connected with the RL load. The measured power and current correspond to the design and simulation result. The inverter output current is reduced with the automatic frequency switching and a smaller apparent power is needed at the inverter to provide the same real power to the load. Although the reactive power shows an obvious reduction, the overall system efficiency does not have a clear improvement. The reason is that the main losses in the circuit are the cable loss and L_2 loss. To improve the efficiency, the most straightforward way is to design a pickup which needs a smaller cable current.

5

CONCLUSION AND FUTURE WORK

5.1. CONCLUSION

In recent years, wireless power transfer has become a hot topic. There are already many products, standards and academic research in this area. More and more people assume that in the future wireless power transfer will have a huge impact on our lives. This report focuses on an application of wireless power transfer, the inductive power transfer (IPT) with multiple pickups in a lighting application.

The goal of this thesis is to design a power supply for the multiple pickup system. At the first step, half bridge and LCL-T network are selected as the topology since they constitute a structure of the current source without complicated control. Different from previous papers about LCL-T network as a current source, this thesis takes into account the effect of the variation of the load inductor. Since the resonant frequency of the system changes according to the load, the starting point of the design is to build a current source with the smaller apparent power required at partial load and ensure ZVS during the whole load range.

The characteristic of the LCL-T network is first analyzed in chapter 2. In the analysis, functions are defined to describe the output current, apparent power, and phase angle of total impedance. The result of the analysis is that with a higher frequency at partial load, the required reactive power can be reduced a lot and the constant current output is ensured at the same time. To guarantee ZVS, the power supply is supposed to work at one frequency for a large load and at the other higher frequency at lower load. The effect of high order harmonics on the switching current and reactive power are taken into account.

In the circuit design procedure, IRF740LC and IR2153D are selected as the MOSFETs and driver IC. Two 555 timers are combined to realize the automatic frequency switching. Parameters of the passive components in the circuit are determined.

In the simulation, the result is consistent with the design. The apparent power demand is reduced with the higher frequency at partial load and the constant current output and ZVS are ensured during the whole load range. According to the result of the simulation, a modification is proposed that the working area of the higher operating frequency can be enlarged considering the effect of high order harmonics on the switching current.

In the experiment, a setup is constructed. The reduction of apparent power demand is realized. Constant current output and ZVS are verified. However, the efficiency of the whole circuit does not show a clear improvement with the automatic frequency switching. This results from that the main loss is dominated by the cable loss. Since the current in the cable is

required to be constant to provide constant power to pickups, there is no space to reduce the cable loss from the power supply side. To reduce the cable loss, a cable with smaller resistance and a lower current demand from the pickup are preferred.

5.2. FUTURE WORK

In this thesis, the power supply consisting of half bridge inverter and the LCL-T network is investigated. To construct the whole IPT system, the next step is the pickup design. The pickup should require a low current in the cable to enhance the efficiency of the system. In addition, what worth noting is the maximum voltage in the cable when designing the pickup for a lower cable current because lower current means higher voltage. The limitation of the maximum voltage in the cable should be taken into consideration. The power supply consisting of the half bridge inverter and the LCL-T network will be revised according to the designed pickup parameters in a later step. According to the effort in the design of power supply in this report, there are a few points that could be useful for the pickup design and the revised design of power supply:

- Compensation (or partly compensation) can be used to in the pickup design to reduce the apparent power in the pickup and reduce the cable current.
- A driver IC with adjustable dead time is recommended. $1.2\mu s$ is too long for the constructed circuit.
- Digital control should be applied in the circuit, which is more convenient to control the frequency and set the dead time comparing to analog control.

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