IC-Compatible Two-Level Bulk Micromachining Process Module for RF Silicon Technology

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***Abstract*—This paper presents a novel two-level silicon bulk micromachining for integration of radio-frequency (RF) devices. The RF devices are fabricated at the frontside of Si (100) wafers using conventional integrated circuit (IC) technology. A post-processing module is applied from the wafer backside with precise alignment to the frontside. This module can provide a blanket ground plane at an optimum position beneath the wafer surface, a frontside contact from the wafer surface to that ground plane, and trenches to suppress crosstalk through the conductive silicon by adding two mask levels. An extension to four masks allows for an integration of large passive components beneath circuitry for a much reduced chip area, lowering chip size and cost. The feasibility of the novel post-process module is demonstrated through the fabrication of microstrip transmission lines, conductor-backed spiral inductors, trench-barriers against crosstalk through the conductive silicon substrate, and high-quality subsurface spiral inductors.**

***Index Terms*—Crosstalk, lithography, microstrip, microwave devices, RF transceiver, silicon micromachining, spiral inductor, three-dimensional integration.**

I. Introduction

THE STRONGLY emerging wireless communications market calls for a higher integration level of radio-frequency (RF) components in order to be able to reduce cost and form factor. Access to such highly integrated and ultimately single-chip transceiver solutions gives promise to widen the existing markets and also open up new product areas. The enormous market volume in RF technologies today, however, tends to hinder the transition from conventional planar integrated structures to more advanced RF structures. Such innovative features may be of advantage, and in cases indispensable, to further pursue high-level integration of RF functions as the operating frequencies move upwards. Planar silicon technology has several shortcomings with respect to the integration of RF transceivers. If one compares a conventional RF transceiver in hybrid technology to a monolithic silicon transceiver, one can identify several bottlenecks:

1) microstrip transmission-lines are widely used on printed circuit board (PCB) in hybrid systems, but microstrips are not yet available in advanced silicon technology;
2) integrated spiral inductors are typically built over moderately doped silicon to minimize substrate losses. Only planar contacts, laterally spaced from the inductor, can be provided to bias the conductive silicon substrate. This may lead to inconsistent inductor characteristics, depending on the impedance terminations [2];
3) crosstalk through the conductive silicon substrate is a serious concern, and at frequencies beyond 1 GHz even conventional silicon-on-insulator (SOI) does not provide a solution [3];
4) inductors and microstrip transmission lines, in particular, occupy large areas, which is not a major issue on PCB. In silicon technology, however, chip area is very costly and large integrated passive components lead to high cost and limit the form factor.

These issues are illustrated in Fig. 1(a)–(d).

These bottlenecks have been addressed in various ways by research groups. The main feature that is missing in silicon technology to enable microstrip integration, as requested in 1), is a via-contact through the silicon substrate to a metallized ground plane at the wafer backside, while choosing an optimum wafer thickness [Fig. 1(a)]. Several groups have proposed wafer thinning to a substrate thickness of 100–200 μm, which would allow for through-wafer vias, but would raise serious concerns about wafer handling and stability during the manufacturing process [4], [5]. The significance of a well-defined ground under a spiral inductor coil on silicon substrates in 2) has not been widely recognized yet. The lack will likely lead to a challenge in future RF circuit design, where the effect of a substrate contact on a nearby inductor will have to be taken into account [Fig. 1(b)]. Crosstalk, identified in 3) as a major issue, may be suppressed to some extend by using high-resistivity SOI (HRS-SOI) wafers [Fig. 1(c)]. Even though such substrates likely lead to reduced crosstalk and to reduced substrate losses in inductors, they are not yet available in 8-in wafer diameter, which is the standard today. Another concern with SOI is the poor thermal conductivity of the buried oxide layer, which will become particularly crucial with the integration of transmitter power amplifiers. Silicon-on-sapphire (SOS), in contrast, provides excellent crosstalk isolation and thermal conductivity as well, but still owes prove of large-scale manufacturability, even though this technology has been around for a long time [6]. The concern of large-area consumption of on-chip passives [Fig. 1(d)], as mentioned in 4), has been addressed by approaches to built passives as part of the chip package. This concept is mainly of interest at lower gigahertz-frequencies, where, e.g., inductor values are large and the impedances of the interconnects to those passives in the package play a relatively small role. At high-gigahertz frequencies the implementation

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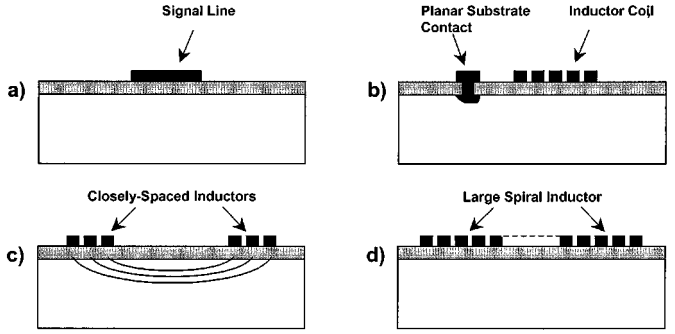

Fig. 1. Nonoptimized RF structures in bulk silicon: (a) signal line without RF ground; (b) spiral inductor with nearby planar ground contact; (c) adjacent components coupled by RF crosstalk through the conductive Si substrate; and (d) large passives, e.g., spiral inductors, consuming excessive chip area.

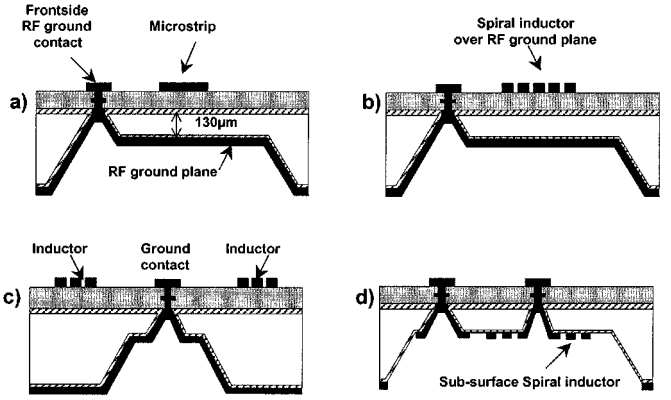

Fig. 2. Cross section of microwave structures that can be realized using the micromachining post-process module: (a) microstrip with micromachined ground plane, (b) integrated conductor-backed spiral inductor, (c) trench isolation structure using two inductors to sense crosstalk, and (d) inductor fabricated at the bottom of the etched cavity at the backside of the wafer.

of the RF passives in the package is likely not a realistic option, because relatively small inductance and capacitance values, of similar order as the interconnect parasitics, are needed. In addition, the issue of testing a transceiver that includes off-chip passives prior to the packaging presents a big problem.

For these reasons it appears to be advantageous, to modify silicon technologies in a way, that the issues 1)–4) are properly addressed. Given the large product volumes in wireless communications today, it is easily understandable, that silicon manufacturers tend to refrain from any major modification of their fabrication processes. The introduction of SiGe technology, just by adding a SiGe-base layer to the bipolar transistor structure in bipolar or BiCMOS processes, for instance, has taken ten years to arrive at large capacity manufacturing [7].

In this paper, we describe a novel post-process module that allows one to add the features required in 1)–4) to any silicon fabrication process without any need for modification and without any perturbation of that process. The results presented here are based on conference publications at ESSDERC'2000 and IEDM'2000 [8], [9]. In Section II, we explain the basic concept of the post-process module. A detailed description of the process flow of the module is given in Section III. In Section IV, the electrical results obtained by using various test structures are presented and discussed, and conclusions follow in Section V.

II. The Post Process Module

The concept of post-processing is frequently used in microsystem technology, where in many areas the product volume is too small to justify a dedicated fabrication process [10]. RF applications point to the other extreme, with a similar conclusion though. The extremely high production volume in communications technology today makes the chip manufacturers very cautious in modifying their fabrication processes, as already mentioned above. This provides an opportunity to use post-processing concepts in order to add the desired RF features to a silicon fabrication process without an interference with the integrated circuit (IC) processing. The advantage is, that such a post-process module can be developed independently and added to the IC fabrication process as high-volume throughput capability has been established.

The illustrations in Fig. 2 show how the components at the wafer frontside, as depicted in Fig. 1, can be enhanced by etching and metallizing the wafer backside. In Fig. 2(a), it is illustrated, how a two-step silicon etching process and a blanket backside metallization can add the desired ground plane to the structure shown in Fig. 1(a). Such a spaced ground plane would also be useful to define a uniform ground underneath the spiral coil of the inductor in Fig. 1(b), as shown in Fig. 2(b). The deep cavities and the vias to the frontside in Fig. 2(a) and (b) can be combined to form a trench through the entire silicon substrate [Fig. 2(c)], eliminating the crosstalk through the conductive silicon [Fig. 1(c)]. Finally, such post-processing could be enhanced with patterning of the backside metal, so that the large chip area occupied by the spiral inductors in a RF circuit [Fig. 1(d)] can effectively be reduced by placing many, if not all, inductors beneath the frontside circuitry [Fig. 2(d)]. Prior work has shown, that such stacking of spiral inductors and circuits is not possible in conventional silicon process technologies [11].

A post-process module applied to high-performance RF-IC technology has to meet certain criteria. First, the total thermal budget has to be very low so that the characteristics of the present active devices are not altered. Second, the wafer frontside has to be protected during post-processing and third, features on the wafer backside have to be sufficiently well aligned to the features at the frontside. Finally, the wafers have to maintain a mechanical stability and handling comparable to bulk silicon wafers to ensure manufacturability. This last issue becomes particularly apparent in some existing post-process approaches to RF applications. The local etching of the bulk silicon had previously been applied either from the wafer backside or through windows from the wafer frontside to remove bulk silicon under the spiral coil of an inductor in order to reduce the losses of that RF component [12], [13]. Those approaches, though effective in improving the inductor quality factor (Q), raise concerns about the stability of the wafers in a manufacturing environment, because the inductors are built on very thin membranes. In the post-processing module, presented here, wafer stability and handling have been achieved by keeping silicon membranes very thick. Sufficient

spacing of signal lines at the frontside to ground planes spaced 100–200 μm away, however, is required to minimize eddy current effects [14]. The fact, that the full wafer thickness is maintained for a considerable fraction of the chip, provides such a micromachined wafer with stiffness similar to that of a solid wafer [15], [16].

III. Fabrication Process

A novel micromachining process has been developed at the DIMES silicon facility for the post-process module. Only process steps using standard IC equipment have been employed. The process starts with the fabrication of the devices at the wafer frontside. Silicon 4-in p-type (100) wafers with a thickness of 525 μm and resistivities of 15 Ω-cm or 3000 Ω-cm were used. A 500-nm thick low-stress low-pressure chemical vapor deposition (LPCVD) silicon nitride layer is deposited on both sides of the wafers. This layer acts as a masking layer for the backside etching and, at the same time, as an etch-stop layer during the final through-wafer silicon etch in KOH from the backside. A 1.5-μm thick silicon oxide is deposited by plasma-enhanced chemical vapor deposition technique (PECVD) onto the frontside of the wafer. This layer is needed to isolate the metal lines from the substrate, i.e., as field dielectric layer. Contact holes are opened in this oxide (stopping on the underlying nitride) by plasma etching. The first metal layer, Al/1%–Si, is then deposited by sputtering and is patterned subsequently. Another isolation layer, a PECVD oxide, is deposited and via-holes are opened, again by dry etching. A second metal layer is deposited and patterned. The inter-metal oxide is 2 μm thick and the two metal layers are 2 μm and 4 μm thick, respectively. At this point the frontside processing is completed, and the wafers are ready for the post-process bulk micromachining. The flow of the post-process module is schematically shown in Fig. 3.

A. Blanket Metal Process

For structures like trenches to reduce crosstalk and RF devices with a blanket metal ground plane, as depicted in Fig. 2(a)–(c), only two extra masks are required. An EV-420 contact aligner, that is capable of front-to-backside optical alignment with an accuracy of $\sim$1 μm, is used. The first mask, used to define the ground plane area, is patterned on the LPCVD silicon nitride layer [Fig. 3(a)]. After the dry etching of the exposed nitride layer, the wafers are immersed in a 33 wt.% KOH solution at 85 °C. Under these conditions the etch-rate of silicon is about 1.4 μm/min. A special holder is used to protect the frontside metal structures from being attacked by the KOH solution. The silicon etching is stopped (time stop) when the ground plane is at the pre-defined distance (generally 130 μm) from the front surface [Fig. 3(b)]. A 500-nm thick PECVD is then deposited as a masking layer for the next etching step. In order to transfer patterns to the bottom of the deep-etched cavities (down to 400 μm) a new lithographic process has been developed. A thick positive photoresist, AZ4562, with modified coating and soft bake process is sufficient to obtain a good coverage and uniformity over the deep cavities. The second mask used to define the wafer-through vias or the isolation

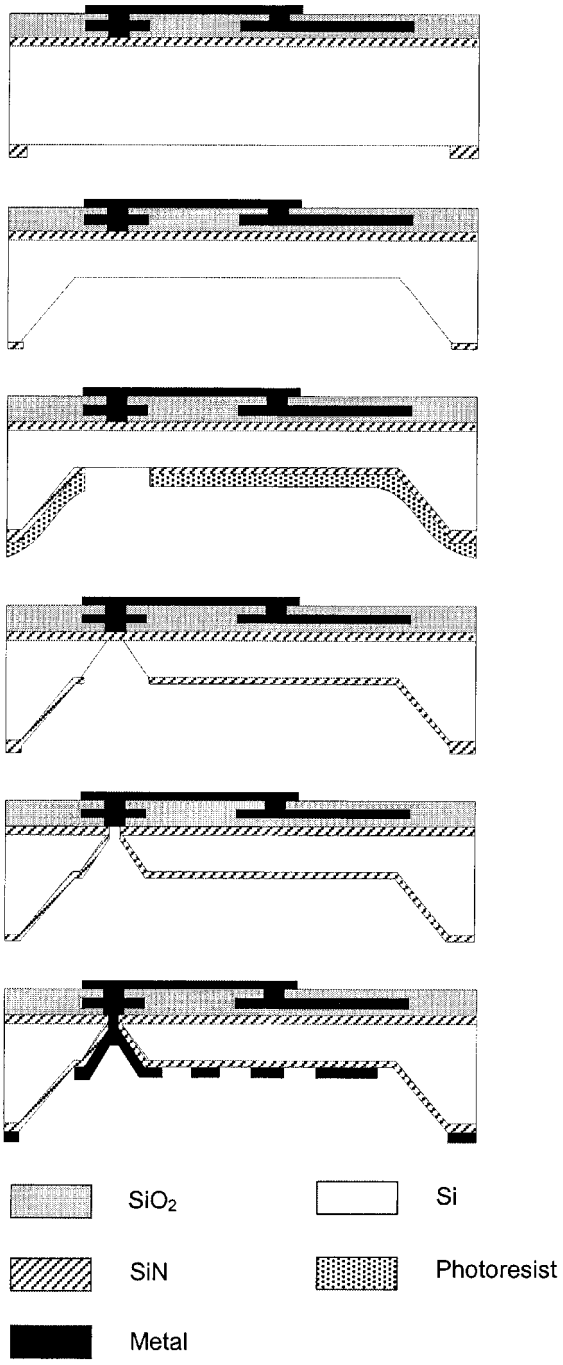

Fig. 3. Process flow of the micromachining post-process module.

trenches is exposed and the nitride-masking layer in the opened windows is removed by plasma etching [Fig. 3(c)]. The bulk silicon etching in the KOH solution is resumed until the silicon nitride layer on the frontside is reached [Fig. 3(d)]. Nitride removal by a maskless dry etching step followed by sputtering of 2–4 μm Al/1%–Si will complete the process for structures using a blanket metallization on the wafer backside.

Microstructures that were realized using this process are shown in Figs. 4 and 5. The pattern transfer process in the deeply etched grooves, trenches, or cavities presented the major challenge. The resolution of the pattern transfer process in deep cavities is affected by several parameters, such as

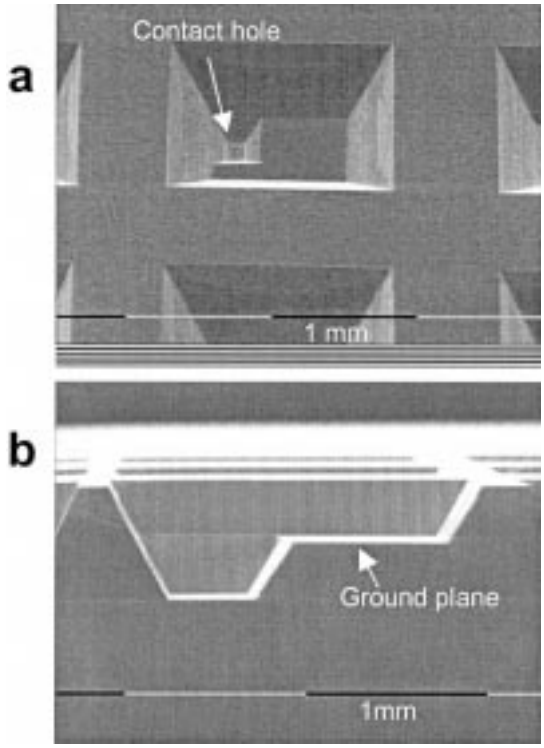

Fig. 4. SEM images of micromachined structures: (a) top view and (b) cross section (magnification 39× and 49×, respectively).

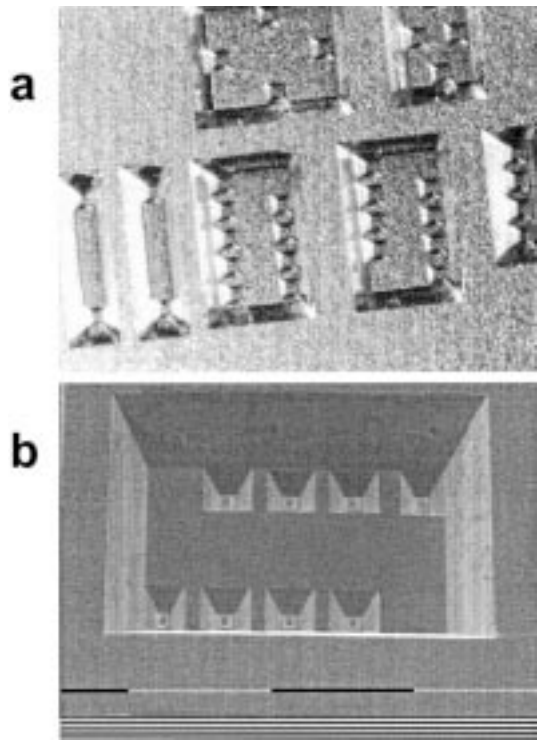

Fig. 5. Backside of a wafer after the final metallization step: (a) optical image showing several two-level micromachined structures with blanket metal and (b) SEM image (magnification 39×) of one such structure with 8-wafer-through contact holes.

resist thickness variation, size and shape of the cavities, etc. Several tests were carried out to investigate these effects and to search for the optimum process parameters. As indicated by the result shown in Fig. 5, the uniformity is sufficient to insure a successful pattern transfer to the wafer and to form several contact holes within the same cavity. The close-up of such a structure [see Fig. 5(b)] clearly shows that even the structures placed very close to the cavity side walls and quite closely spaced could be well patterned.

B. Patterned Backside Metal

In order to fabricate a spiral inductor at the bottom of a cavity a few more steps and two additional masks are required after the second bulk silicon etch-step is performed [Fig. 3(d)]. First, a 500-nm thick PECVD silicon nitride layer that will act as insulation layer is deposited in the etched cavities. Contact windows to the frontside are opened [Fig. 3(e)] by dry etching. The Al/1%–Si layer is sputtered over the cavities. Dry etching of the metal and an alloy step complete the device fabrication [Fig. 3(f)].

The two additional masks used for these structures contain patterns that have to be transferred at the bottom of and across deep (wafer thickness) cavities. Special care has to be taken with the lithographic process and slightly different conditions are used for each mask step. The high-viscosity, high-transparency positive photoresist AZ4562 has been chosen as a suitable resist for this purpose. The coating is carried out in a Convac spin coater that allows modification of the spinning program. The wafers are placed in the HMDS vapor-priming chamber for 10 min. Then the resist coating is applied with a spinning speed of 500 r/min for 4 s and 3500 r/min for 36 s. The soft bake takes place at 95 °C for 3 min. This coating program results in a good step coverage and reasonable thickness uniformity over the deep cavities [16].

The effect of dimension and shape of the cavities on the resist uniformity has also been investigated. Better results are obtained for the larger rectangles or square cavities. The average resist thickness at the bottom of 400-μm cavities obtained by this coating process is about 5 μm. The pattern is then transferred to the resist coated cavities by an EV-420 contact aligner in the soft contact mode. The gap between the mask and the photoresist layer is basically the depth of the etched cavities. This means that higher exposure energy is needed to expose the photoresist. An exposure energy of 375 mJ/cm2 is used to open etch windows and contact windows [Fig. 3(c) and (e)] and a somewhat lower value to pattern the metal [Fig. 3(f)]. After exposure, a development step is carried out in a solution of AZ400K and DI water (1 : 4). In order to open the small contact holes in the small cavities, as depicted in Fig. 3(e), the exposure and development step is applied twice. This is necessary as the resist in these small and deep cavities is thicker than at the ground plane area and this approach is preferred to an increase in energy dose as this would result in resolution loss. The exposure energy depends also on the pattern design. For example, the mask for patterning the metal layer [Fig. 3(f)] has more open areas than the one used for the small contact openings [Fig. 3(e)]. For this reason there is no need to increase the exposure time for the metal patterning.

Another aspect that has to be considered in this pattern transfer process is the loss of resolution. The loss of resolution is caused by the diffraction at feature edges on the mask when

using the proximity mode [17]. When the distance between the mask and the resist is about 400–500 μm (the depth of etched cavities), the dimensions of patterned structures can differ from their value at the layout level. This loss of resolution has to be taken into account when designing structures to be patterned in and across deep cavities. The loss of resolution can deform the shape of small patterned structures. Our previous experiments have shown that rounding of the corners takes place, for which smaller squares will be rounded when patterned at the bottom of 300–400 μm deep cavities. However, as the average dimensions of the structures required for the integration of RF components are often in the order of tens of micrometers, the loss of resolution is still acceptable for several types of structures. Moreover, once the photoresist coating process is optimized for uniformity and reproducibility, the loss of resolution can be partly compensated while designing the mask. In order to increase the density of these contact holes and reduce the size of the structures, a better resolution in the lithography process is required. Increased resist uniformity over the wafer, independently of the shape and position of the cavities, is necessary. The potential of a new coating technique, i.e., photoresist spray coating [18], is currently being evaluated.

In spite of the current limitation, the developed process is suitable to realize several microwave components. A typical example is the integration of a spiral inductor at the bottom of a cavity [as illustrated in Fig. 2(d)]. In conventional Si processes, spiral inductors with a typical size of about $200 \times 200\ \mu\text{m}^2$ have to be placed side by side with the active devices. The integration of inductors at the backside of the wafer is very attractive as this can substantially decrease the circuit density. SEM images of such a spiral inductor after resist exposure and development and after aluminum etching are depicted in Fig. 6(a) and (b), respectively. The inductor is integrated at the bottom of a 390-μm-deep cavity and contacts are brought to the frontside via two through-wafer holes.

The quality factor of this inductor can be improved if one can reduce the effect of the parasitic capacitance of the entirely metallized vias. Thus the patterning of metal lines across the vias is a very attractive prospect [19]. Fig. 7 shows an example of patterned metal lines running from the backside to the frontside of the wafer across the two-level micromachined cavities. These preliminary results are rather promising and can be extended to other application areas, such as integration of high-density three-dimensional interconnection structures.

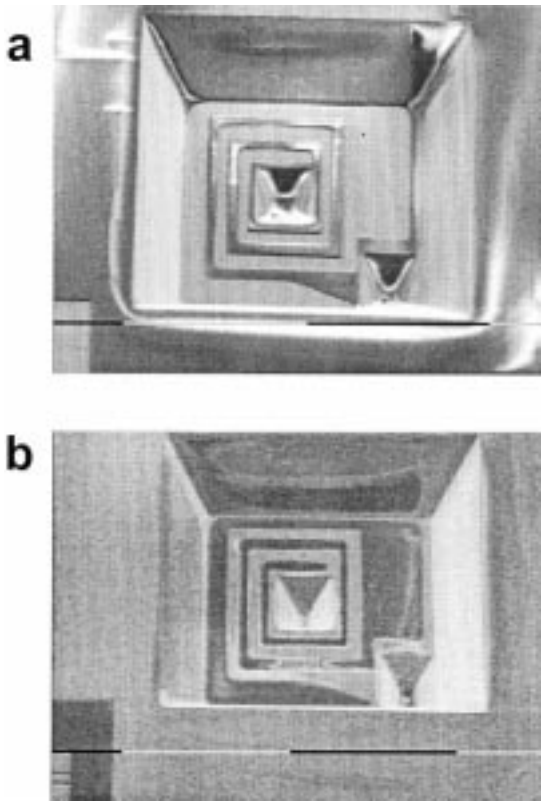

Fig. 6. SEM images of a spiral inductor at the bottom of a 390-μm-deep cavity (magnification $\times$44): (a) after resist exposure and development and (b) after Al dry etching.

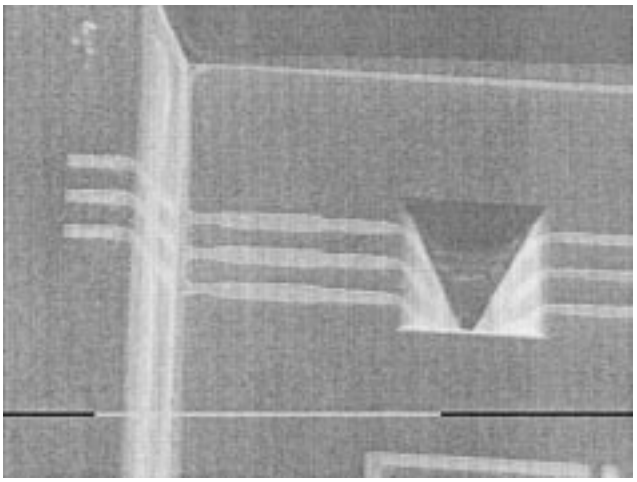

Fig. 7. Patterned metal lines (Al) running over and across the etched cavities (magnification $\times$72).

IV. Characterization of the Post-Process Module

For the electrical characterization of the post-processed RF features, shown in Fig. 2(a)–(d), special test structures were fabricated:

A. Microstrip Transmission Lines

A 30-μm wide signal line was fabricated at the top metal layer over a blanket ground plane, which was positioned at 130-μm distance beneath the surface, to form a microstrip [Fig. 2(a)]. For comparison, the same signal line was also built without that ground plane, i.e., over nonmicromachined bulk silicon. The ground plane resulted from a 4-μm thick aluminum deposition over the micromachined wafer backside. The contact to that ground plane was brought to the wafer surface by a via-contact, as described earlier in Section III. HRS substrates were used in this experiment. Both lines were characterized by S-parameter measurements, carried out by using an HP8110 network analyzer up to 40 GHz. The parasitics of the contact pads were not de-embedded. The reflection ($S11$) and the insertion loss ($S21$) of 1-mm long lines are shown in Fig. 8. The characteristic impedances of both lines were determined as $\sim$45 Ω. The insertion loss of the microstrip was considerably smaller than that of the

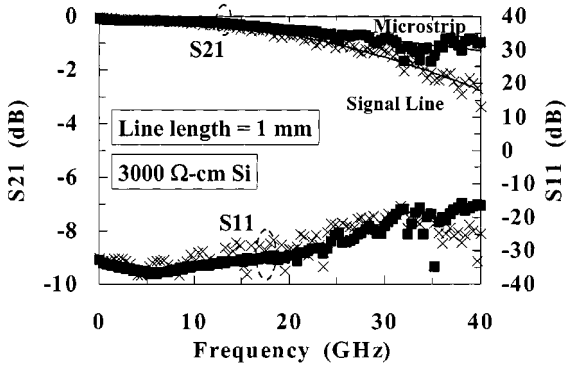

Fig. 8. Measured insertion loss (S_{21}) and reflection coefficient (S_{11}) of an integrated microstrip and a signal line.

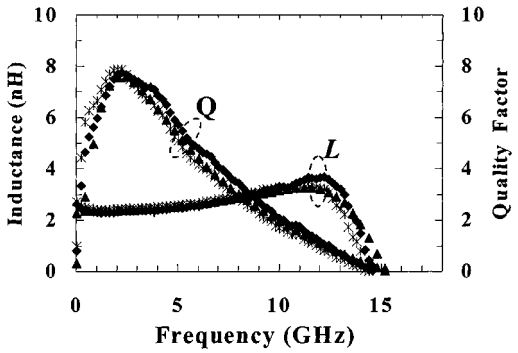

Fig. 9. Measured inductance (L) and quality factor (Q) of a four-turn spiral inductor with an area of 226×226 μm^2 extracted from one-port and both two-port reflection parameters.

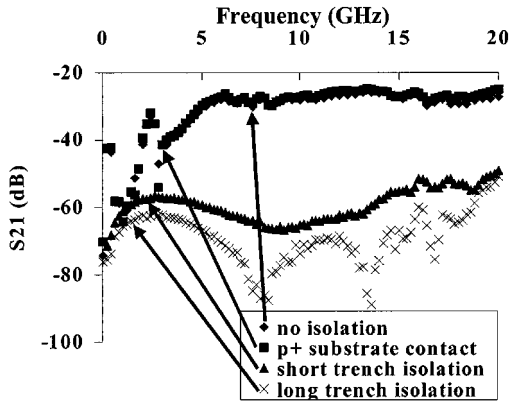

Fig. 10. Measured insertion loss (S_{21}) for the different isolation structures.

signal line without a ground plane ("signal line"). At a frequency of 17 GHz, the insertion loss was as low as 3 dB/cm, which compares well with state-of-the-art results on HRS wafers, on which the signal line is isolated from the substrate by an oxide [20].

B. Conductor-Backed Inductors

Test inductors with a ground plane underneath were built [Fig. 2(b)]. That ground plane was fabricated in the same way as that of the microstrip, discussed above. It had been shown in earlier work, that an inductor without a ground plane can exhibit an "electrical asymmetry," if a planar substrate contact is placed in close vicinity to the inductor coil. The effect can be particularly severe, if a ring of substrate contacts, a so-called "halo contact" surrounds the spiral coil [2]. The result of the effect is, that its characteristics will depend on the impedance terminations. It also means, that the same inductor tested in one-port and two-port test configurations will show different characteristics. This results in the dilemma, that a lumped-element model derived from a particular test site will not reproduce accurately well in all possible circuit implementations. We therefore tested a 2.5-nH inductor with an underlying ground plane, an area of 226×226 μm^2, four turns, and conductor width and space of 13 μm each, in one-port and two-port configurations. After measuring the S-parameters up to 15 GHz and converting to Z-parameters, the inductances and quality-factors were computed as functions of frequency. The inductances were derived as $L = (\mathrm{im}(Z_{11}))/\omega$, $L = (\mathrm{im}(Z_{11} - 50\ \Omega))/\omega$, and $L = \mathrm{im}(Z_{22} - 50\ \Omega)/\omega$ and the quality-factors as $Q = \mathrm{im}(Z_{11})/\mathrm{re}(Z_{11})$, $Q = (\mathrm{im}(Z_{11}) - 50\ \Omega))/(\mathrm{re}(Z_{11}) - 50\ \Omega))$, and $Q = (\mathrm{im}(Z_{22}) - 50\ \Omega))/(\mathrm{re}(Z_{22}) - 50\ \Omega$ for the one-port test and the two-port tests, respectively. Fig. 9 shows all measurement results in overlay. Very minor discrepancies were observed, demonstrating the effect of a uniformly defined ground potential under the spiral coil. The fact, that the inductances were 2.5 nH, as targeted from design, shows that eddy currents in the ground plane were negligible. That was a result of sufficient ground plane spacing of 130 μm [14].

C. Crosstalk Isolation

For the verification of crosstalk through the conductive silicon substrate laterally spaced spiral inductors were connected to a two-port test structure. The insertion loss has been used as an indication of crosstalk. The crosstalk has of course two components, i.e., electromagnetic coupling of the coils and capacitive coupling through the silicon substrate. Four different test cases were considered. The silicon substrate resistivity was 15 Ω-cm in this experiment. First, the test structure was placed on a solid and floating silicon substrate to provide a control [Fig. 1(c)]. Second, a substrate contact ring was formed around one of the inductors to form a guard ring [3]. The third test structure had a short trench barrier of 330 μm in length between the coils [Fig. 2(c)]. For the fourth structure that trench had a length of 1.6 mm. The insertion losses measured for the four test structures are shown in Fig. 10 up to 20 GHz. Obviously, the guard ring did not provide an improvement compared to the control structure for frequencies above 3 GHz [3]. But the short trench barrier already resulted in an improvement of the crosstalk isolation by more than 30 dB. For the long trench the measurement was limited by the noise floor of the test system, and one only can estimate that this crosstalk barrier provides an improvement of the isolation by >40 dB. It is obvious, that trenches etched from the wafer backside up to the frontside provide very effective crosstalk barriers and may thus be desirable additions to RF silicon technologies.

D. Subsurface Spiral Inductors

Two experiments were carried out to demonstrate the feasibility of inductor integration underneath circuitry. First, test inductors were fabricated at a distance of 130 μm beneath the chip surface by using the post-process module with four mask

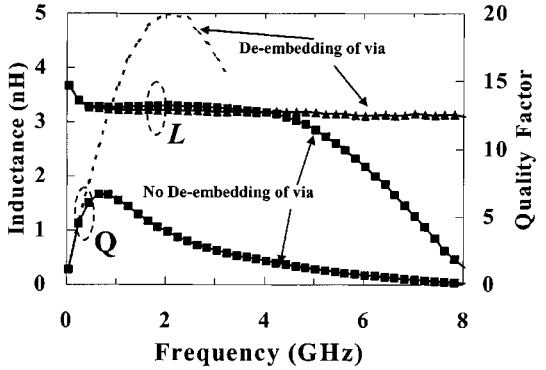

Fig. 11. Measured inductance (L) and quality factor (Q) of a two-turn inductor fabricated with a structure as in Fig. 2(d), with or without deembeding of the parasitic capacitance of via-cone and frontside pad.

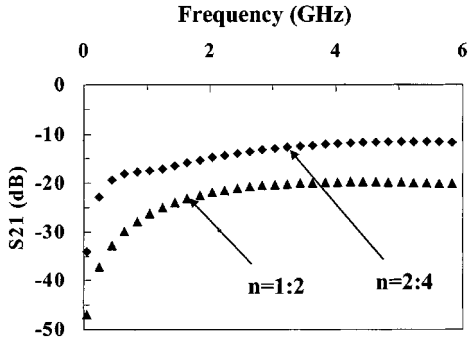

Fig. 12. Measured insertion loss (S_{21}) for two stacked coil pairs (turn ratios 1 : 2 and 2 : 4).

levels, as described in Section III-B. The purpose of that experiment was to show, that those components can be integrated and, that the quality is not sacrificed in comparison to inductors positioned at the chip surface. In a second experiment one inductor coil was spaced from the wafer surface and a second coil was positioned at the chip surface with maximum overlap of the buried coil. This structure thus formed a transformer, which represents the worst-case for coupling between components at the surface and buried components.

Both structures were fabricated in a 15 Ω-cm silicon substrate. The subsurface test inductor occupied a total area (A) of 970×780 μm^2, had a conductor width (W) and space (S) of 90 μm and 40 μm, respectively, and two turns ($n = 2$). The resulting inductance was 3.4 nH. For simplicity reasons, this inductor was built with a via to the chip frontside that was fully metallized (Fig. 6). The frequency-dependent inductance and quality-factor were derived from S-parameter measurements, as described in Section IV-B. The measurement results are shown in Fig. 11 for two cases, de-embedding of the probe pads only and de-embedding of probe pads and via. It becomes obvious, that for this relatively small inductor the fully-metallized vias have a significant impact on the inductor-Q. This is due to the large parasitic via capacitance as well as eddy current effects in the metallized center area of the spiral coil [21]. Without an inclusion of the via parasitic effects $Q_{\max} = 20$ was determined for this 3.4 nH inductor. This high $Q_{\max}$-value results to a large extend from the thick backside metallization of 2 μm, but is certainly affected considerably by the de-embedding of the large via parasitic. The conclusion thus is that subsurface high-Q inductors can be integrated by using the post-process module, provided that the via-capacitance can be reduced. Otherwise, this process may best applicable to large inductors (>10 nH). One way to reduce the parasitic capacitance of the via would be to use a lithographically defined metal line through the via instead of fully metallizing it (Fig. 7; Section III-B). This, however, still limits the compactness of the spiral coil of the inductor, since a hollow coil design is required. Most effective would be to use an anisotropic dry etching of the via to reduce the surface area [5]. For the given spacing of the inductor coil from the chip surface an about ten-fold reduction of the via parasitic capacitance can be expected. It should be noted here, that the inductor coil was fabricated by using conventional contact printing. The consequence of this approach was that the features printed had to be large. With a more sophisticated lithographic exposure it can be expected, that conductor width and space can be more comparable to structures built at the wafer frontside.

For the verification of the isolation between features at the frontside and buried features, two transformer structures were built. The first transformer had two turns at the frontside ($A = 580 \times 550$ μm^2, $W = 50$ μm, $S = 40$ μm, $n = 2$) and one turn in the buried coil ($A = 610 \times 510$ μm^2, $W = 70$ μm, $S = 20$ μm, $n = 1$), thus called 1 : 2 transformer. The second transformer had four turns at the frontside ($A = 935 \times 940$ μm^2, $W = 50$ μm, $S = 50$ μm, $n = 4$) and two turns in the buried coil ($A = 970 \times 780$ μm^2, $W = 90$ μm, $S = 40$ μm, $n = 2$), thus called 2 : 4 transformer. The insertion losses of the two transformers were measured both to be less than -10 dB (see Fig. 12). This appeared to be good evidence of sufficient isolation of this worst-case coupling between frontside and subsurface features. The isolation between circuitry and subsurface inductors is likely considerably better, but this needs ultimately to be demonstrated. The trend in those two test results, however, shows, that the isolation is better for smaller areas and fewer numbers of turns of the stacked coils. For very large subsurface inductors the distance to the chip surface may therefore have to be somewhat increased.

V. Conclusion

A novel micromachining post-process module for RF silicon technologies has been presented. The module provides several unique feature that are not available in conventional silicon IC processes:

1) low-loss microstrip transmission lines can be integrated;
2) conductor-backed inductors with characteristics independent of the position of substrate contacts in the circuit layout are feasible;
3) trench barriers between circuits and circuit sections become available to reduce on-chip crosstalk;
4) subsurface passive components can be employed to considerably reduce chip area and thus cost.

The post-process module is designed as a complement to any RF silicon technology without interfering with the IC processing or perturbing any of the active device characteristics. It is, however,

most effective at moderate silicon substrate resistivities (>10 Ω-cm), except for the crosstalk trench barrier becoming most effective at high silicon conductivities, such as epi substrates for CMOS. At the given status, solely techniques compatible with IC processing have been employed, making the module naturally migratable to current silicon manufacturing facilities. The module is believed to be a considerable enhancement of current IC processes without adding excessively to the total fabrication cost of a silicon RF chip.

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