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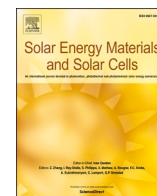
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Optimization of interface properties in *p*-type poly-SiO_x passivating contacts through intrinsic buffer layer modification

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ABSTRACT

Polycrystalline silicon (poly-Si) carrier-selective passivating contacts (CSPCs), featuring high photoconversion efficiency (PCE) and cost-effectiveness, have emerged as a promising approach for high-efficiency crystalline silicon (c-Si) solar cells. To minimize parasitic absorption losses induced by doped poly-Si window layers, wide bandgap oxygen-alloyed poly-Si (poly-SiO_x) layers are developed. However, challenges persist in achieving excellent surface passivation for boron-doped poly-SiO_x contact stacks, likely caused by boron diffusion during annealing and the reduced doping concentration resulting from lower crystallinity as oxygen content increases. In this study, we investigate the impact on the passivating contact structure and solar cell performance of a 10-nm thick intrinsic hydrogenated amorphous silicon buffer layer with varying oxygen content (a-Si (O_x):H) deposited by plasma-enhanced chemical vapor deposition (PECVD), and placed between the tunneling silicon oxide (SiO_x) and the poly-SiO_x (*p*⁺). After the hydrogenation step, we obtain both high passivation quality with implied open circuit voltage (*iV*_{oc}) of 728.3 mV and low contact resistivity (*ρ*_c) of 59.18 mΩ cm² on polished surface for oxygen-free a-Si:H buffer layer. These improvements can be attributed to the appropriate thickness of the tunnel oxide and confirmed by transmission electron microscopy (TEM) images, to higher crystallinity of the buffer layer, which facilitates more efficient doping in the buffer layer. This is evidenced by energy dispersive X-ray spectroscopy (EDX), and X-ray photoelectron spectroscopy (XPS) results. At the device level, a front-side textured, rear-side flat, rear junction poly-SiO_x/poly-SiO_x solar cell on n-type c-Si wafer, an efficiency improvement can be observed from 3.55 % without a PECVD buffer layer to 18.9 % with an oxygen-free a-Si:H PECVD buffer layer. The impact of the buffer layer crystallinity on cell performance is further demonstrated by deploying a 10-nm thick LPCVD buffer layer, which facilitates an efficiency of 21.15 % for the same device structure.

1. Introduction

In recent years, Tunnel Oxide Passivating Contact (TOPCon) technology, consisting of a heavily doped polycrystalline silicon (poly-Si) and an ultrathin tunneling silicon oxide (SiO_x) layer, has come to dominate c-Si solar cells market due to its significant advantages of high photoconversion efficiency (PCE) and cost-effectiveness in mass production [1,2]. Many numerical simulations suggest that TOPCon solar cells with outstanding passivation and contact quality can reach an efficiency of up to 28.7 % [3–6], which makes TOPCon technology one of the leading candidates for approaching the theoretical efficiency limit of crystalline silicon (c-Si) solar cells of 29.4 % [3–6]. To date, the highest

efficiency values of 26.89 % and 26.1 % were reported for c-Si solar cells utilizing such contacts with a front/back-contacted (FBC) design [7] and an interdigitated back contact (IBC) design [8], respectively.

However, a significant challenge still open in the TOPCon technology is the use of narrow band gap of poly-Si (~1.12 eV) [9,10], which leads to substantial parasitic absorption losses when used as window layers of solar cells [11,12]. To tackle this challenge, researchers have explored alternative materials with improved transparency by incorporating carbon [13,14], nitrogen [15], or oxygen [16,17] into poly-Si via plasma-enhanced chemical vapor deposition (PECVD). Among various poly-Si alloys, using CO₂ to fabricate the poly-SiO_x presents several advantages, including enhanced safety, cost-effectiveness [12],

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tuneability of optical properties [18] and ease of processing in both FBC and IBC configurations [17]. In addition, poly-SiO_x-based FBC solar cells exhibit significant advantages in tandem cell applications [16,19]. The reduced refractive index of poly-SiO_x [12,18,20] minimizes reflection losses at the transparent conductive oxide (TCO)/poly-SiO_x interface [19], improving light coupling into the bottom cell. Additionally, the lower extinction coefficient significantly reduces parasitic absorption [12,18,20], especially for long-wavelength, allowing more photons to reach the active layers in the tandem architecture. Furthermore, the tunable refractive index of poly-SiO_x by tailoring different oxygen content can minimize the reflection at the TCO/poly-SiO_x/c-Si interfaces to the greatest extent. These optical and structural advantages make poly-SiO_x a highly promising material for next-generation tandem photovoltaics. Therefore, poly-SiO_x passivating contact stacks will be further investigated in this work.

Compared to electron-collecting poly-Si (n^+) contact stacks, poly-Si (p^+) ones have yet to achieve optimal surface passivation and minimal contact resistivity (ρ_c). From a chemical passivation perspective, this performance gap is attributed to the formation of trap defects, boron-induced oxygen vacancy states, and pinholes formed during the high annealing temperature, all of which significantly compromise the quality of surface passivation [21–26]. In addition, the low doping level of poly-Si (p^+) constrains the effect of field-effect passivation [27]. Especially for the case with increased oxygen concentration in poly-SiO_x materials, the reduction in crystallinity leads to less efficient doping in poly-SiO_x, thereby significantly limiting the achievement of high field-effect passivation [17,28,29]. Similar to surface passivation, ρ_c performance is also dramatically restricted by both low doping concentration [30] and high trap densities [21,29]. The defect-induced increase of ρ_c can be explained by Fermi-level pinning formed by O-related donor-like surface states in tunnel SiO_x layer [21,29], which subsequently leads to an inverted surface electric field, hindering hole transport [21]. To minimize these problems, many efforts have been devoted to optimizing the interfaces of the stack by inserting a thin intrinsic hydrogenated amorphous silicon (a-Si:H(i)) buffer layer between the hole transport layer and the SiO_x layer [14,29,31–35]. Nogay et al. [14] reported that the incorporation of intrinsic buffer layer between poly-SiC_x (p^+) and SiO_x can boost the passivation quality by suppressing the reaction of SiO_x with carbon and impeding the accumulation of boron dopants around the SiO_x layer. Moreover, excellent passivation quality with the implied open circuit voltage (iV_{oc}) of 709 mV and low contact resistivity with ρ_c of 0.5 mΩ cm² by inserting an intrinsic buffer layer between poly-SiO_x (p^+) and SiO_x layer are achieved in Yang's work [34]. However, comprehensive studies on the interface optimization between poly-SiO_x (p^+) and SiO_x are rarely mentioned.

In this contribution, we apply a thin intrinsic buffer layer with tailored oxygen content between the tunneling SiO_x and the a-SiO_x (p^+) layers deposited by PECVD. Detailed analyses are performed focusing on interfacial microstructural properties of passivating contact stacks employing various buffer layers, using as main approaches transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS). Afterwards, we explore the influence of different buffer layer on passivation quality and contact property. Accordingly, the performance of FBC solar cells is evaluated and compared with that of similar solar cells endowed with high-crystallinity a-Si LPCVD buffer layer [36].

2. Experimental section

2.1. Fabrication and characterization of p -type poly-SiO_x/SiO_x/c-Si passivating contact

Symmetrical lifetime samples were prepared using n -type, double-side polished FZ c-Si wafers with (100) orientation and a resistivity between 1 and 5 Ω cm. These wafers had initially a thickness of 280 ± 20 μm. The samples underwent a standard cleaning process consisting of 10-min-long bath in 99 % HNO₃ at room temperature to remove organic

contaminants, followed by a 10-min-long bath in 69.5 % HNO₃ at 110 °C to eliminate metal impurities. Subsequently, a 0.55 % HF dip was used to remove any native SiO_x layer formed during the previous cleaning steps. Then, for the fabrication of the poly-SiO_x passivating contact stack, a tunneling SiO_x layer was first thermally grown on both sides of the wafer at 650 °C, with an oxidation time of 3 min and a gas mixture ratio of N₂ to O₂ at 10:1. In later sections, we refer to this tunneling layer to as t-SiO_x. Then, a stack of 10-nm thick intrinsic hydrogenated a-Si (O_x):H, 25-nm thick p -type a-SiO_x:H, and 2-nm thick p -type a-Si:H films were sequentially deposited by PECVD at 216 °C, using SiH₄, CO₂, H₂, and B₂H₆ (2 % in H₂ carrier gas) as gas precursors. Detailed deposition parameters are shown in Table S1. The intrinsic a-Si(O_x):H buffer layer was deposited using a conventional radio frequency (RF, 13.56 MHz), while the p -type a-SiO_x:H and the a-Si:H films were deposited with a very-high-frequency (VHF, 40.68 MHz). CO₂ was used as the oxygen source in the p -type a-SiO_x layer as well as for tailoring the oxygen content of the intrinsic a-Si(O_x):H. For all the doped a-SiO_x:H layers, the same CO₂ gas flow ratio, $R_{CO_2} = f[CO_2]/(f[CO_2] + f[SiH_4])$, was used. In contrast, different R_{CO_2} values ranging from 0 to 0.43 were employed for the a-SiO_x:H buffer layer. A similar structure without a buffer layer was also fabricated to act as a reference group. All samples were then loaded in a tube furnace at room temperature, which was subsequently heated up to 925 °C at a rate of 10 °C/min. The samples were held at 925 °C for 30 min, followed by passive cooling to room temperature. The entire annealing process was performed in a pure N₂ atmosphere. To further enhance the surface passivation, the high temperature annealed samples were capped with a 75-nm thick SiN_x layer formed by PECVD on both sides, subsequently performing a forming gas annealing (FGA) process at 400 °C for 30 min in a 10 % H₂ in N₂ atmosphere. After these high temperature annealing steps, the purpose of the top p -type poly-Si layer is clearly to act as a physical barrier, protecting the p -type poly-SiO_x from the damage otherwise inflicted by the HF solution used to remove the SiN_x capping layer.

For the passivation quality of the developed poly-SiO_x passivating contacts, the effective minority carrier lifetime (τ_{eff}) as a function of carrier injection intensity was measured by a Sinton WCT-120 lifetime tester applying the transient measurement mode [37], from which the iV_{oc} is extracted. The dark I - V characteristic was employed to determine the total resistance of poly-SiO_x (p^+) contact stacks [38], which consists of the resistance contributions from the c-Si bulk to the poly-SiO_x stacks, from the poly-SiO_x stacks to the Ag layer, as well as the internal resistance within the c-Si bulk, poly-SiO_x stacks and Ag layer. A schematic representation of the sample structure is illustrated in Fig. S1. The final contact resistance was derived by subtracting the resistance of the c-Si substrate and layers from the total resistance measured in the samples. It is noteworthy that the resistance of the layers can be considered negligible due to the reduced thickness of the poly-SiO_x stacks and the high conductivity of the Ag. To uncover the chemical composition of poly-SiO_x stacks, a depth profile analysis with a ThermoFisher K-Alpha XPS was conducted from the surface to the interface of n -type c-Si/SiO_x over etching times ranging from 0 to 680 s [39]. High resolution transmission electron microscopy (HR-TEM) coupled with energy dispersive X-ray spectroscopy (EDX) was employed to comprehensively evaluate the microstructure properties and compositional distribution of the contact stack in lamellas extracted from representative solar cells.

2.2. Fabrication and characterization of solar cell

The poly-SiO_x stacks were integrated into n -type monofacial rear junction FBC solar cells with dimensions of 2 cm × 2 cm. The cell structure is depicted in Fig. 1(a). It features an n -type poly-SiO_x stack on the textured front side and a p -type poly-SiO_x stack on the flat rear side. The fabrication sequence is illustrated in Fig. 1(b). Firstly, the wafers were single-side-textured to get random pyramids using a mixed solution of tetramethyl ammonium hydroxide (TMAH) and Alkatec additives at 85 °C for 15 min. Following standard cleaning procedures as

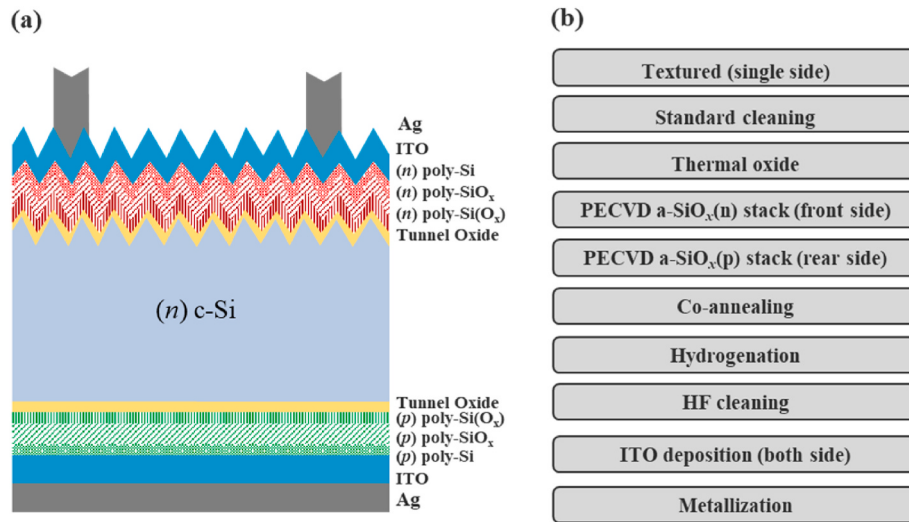


Fig. 1. (a) Schematic cross-section view, and (b) detailed fabrication process flow of the FBC solar cells. The deposited layers in both *n*-type and *p*-type stacks become poly-crystalline after the co-annealing step.

previously described, a t-SiO_x layer was then thermally grown on both sides of the wafer. Subsequently, *n*-type a-SiO_x stack was deposited on the front side, while *p*-type a-SiO_x stack was applied to the rear side. Similar to the *p*-type stack, also the *n*-type stack comprised an intrinsic buffer layer, *n*-type a-SiO_x layer, and *n*-type a-Si protective layer. For the final cell fabrication, we employed a fixed *n*-type buffer layer with $R_{CO_2} = 0$. For the *p*-type stack, we selected the $R_{CO_2} = 0$ case and the reference group (without buffer layer) for comparison. Similar to preparation of poly-SiO_x stacks, subsequently the samples will undergo high-temperature crystallization and hydrogenation processes via coating by PECVD SiN_x. Prior to the metallization process, the SiN_x layers were removed from the wafer surfaces using a HF solution. Following that, 75-nm and 150-nm thick indium tin oxide (ITO) layers were deposited via sputtering on the front side and the rear side, respectively. Finally, the formation of metal electrodes was carried out using screen printing technique.

The final performance of the solar cells was evaluated using an AAA-rated Wacom WXS-90S-L2 solar simulator under standard test conditions and calibrated with reference solar cells validated at Fraunhofer ISE CalLab.

3. Results and discussion

3.1. Microstructural properties and elemental composition of passivating contact stacks

The structural evolution and elemental composition analysis of the layers were evaluated by TEM. Fig. 2(a–c) show cross-sectional HR-TEM images of poly-SiO_x/SiO_x/c-Si structures for the reference sample without a buffer layer and samples with R_{CO_2} values of 0 and 0.27, respectively. As detailed in the experimental section, the reference stack (Fig. 2(a)) should include the following layers from bottom to top: c-Si bulk, t-SiO_x, poly-SiO_x, poly-Si, borosilicate glass (BSG), and the SiN_x residual layer. In contrast, in Fig. 2(b) (c), in addition to the aforementioned layers, a buffer layer is also supposed to be present between the t-SiO_x and poly-SiO_x layers. Moreover, corresponding scanning TEM (STEM) high-angle annular dark field (HAADF) images, combined with EDX elemental maps and line profiles, are presented separately, as shown in Fig. 2(d–f).

Fig. 2(a) clearly illustrates the presence of a t-SiO_x layer between the a-Si phase and the poly-SiO_x layer, further substantiated by the elemental analysis presented in Fig. 2(d). Additionally, analogous oxide layers with increased thickness are also observed in Fig. 2(b)(c),

corresponding to R_{CO_2} values of 0 and 0.27, respectively. The reasons for these variations in the oxide layer will be explained in detail in Section 3.3. Furthermore, due to the fusion of the buffer layer and the poly-SiO_x layer during subsequent high-temperature annealing complicates the ability to distinguish the boundary between these two layers. However, it's clear that both groups exhibit two individual sublayers between t-SiO_x and poly-Si layer: the top sublayer is more amorphous, while the bottom sublayer exhibits higher crystallinity. This phenomenon is not consistent with our previous findings, where the poly-SiO_x material comprised nanometer-scale silicon crystals that were predominantly in contact with each other and surrounded by amorphous structure [17]. In addition, interestingly, the buffer layer also appears to influence the crystallinity of the poly-SiO_x layer, as evidenced by the increase in the proportion of the amorphous phase with higher R_{CO_2} values. Further investigation is required to fully understand the underlying mechanisms of these structural variations. In contrast, the analysis of other layers can be distinctly performed based on their structure characteristics and elemental composition.

Notably, the boundaries between the poly-Si and BSG layers are less sharp in the reference group, where an a-Si phase is observed beneath the t-SiO_x layer. Instead, sharper interfaces are seen in the groups with a buffer layer with no amorphization under the tunneling oxide. The formation of such an amorphous layer has also been reported in Y. Lin et al. research on poly-SiC_x CSPCs [13], where it is hypothesized that this layer may result from the combined influence of high residual stress, high temperatures, and the introduction of C-based impurities [40,41]. We speculate in our study, as CO₂ was employed as an oxygen source, which inherently contains element C, that the observed phenomenon may primarily be attributed to the incorporation of C impurities. Nonetheless, further investigation is essential to substantiate this hypothesis.

Fig. 2(d–f) display STEM HAADF images combined with EDX elemental maps and line profiles for the reference sample and samples with R_{CO_2} values of 0 and 0.27, respectively. The HAADF images confirm the presence and arrangement of the identified layers as illustrated in Fig. 2(a–c). Each sample shows a sharp and well-preserved c-Si (a-Si)/SiO_x interface, with the SiO_x layer distinctly resolved in the EDX maps. The line profiles reveal variations in elemental composition across the layers, clearly describing the SiO_x layer and the distribution of boron within the poly-SiO_x layers, where a qualitative analysis of boron was conducted from the EDX results [42]. The line profiles indicate that boron content in the whole stack layers increases with decreasing R_{CO_2} value. Notably, in the reference group, the boron concentration is

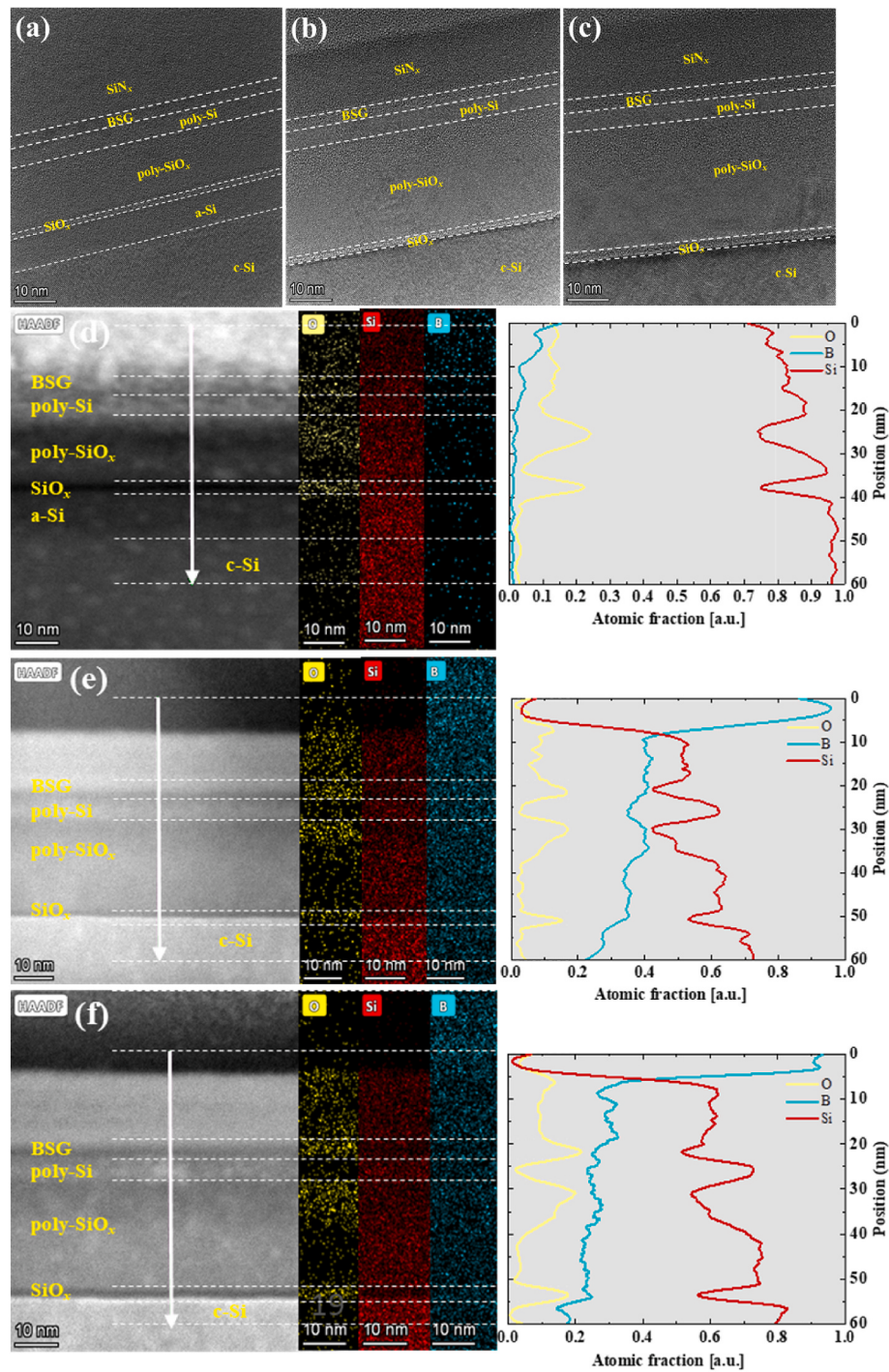


Fig. 2. Microstructural properties and elemental analysis of *p*-type poly-SiO_x/SiO_x/c-Si structures without and with a buffer layer between poly-SiO_x and SiO_x layers. Cross-sectional HR-TEM images and the corresponding EDX map together with the EDX line scan of Si, O and B elements of samples (a)(d) without a buffer layer, (b) (e) with $R_{\text{CO}_2} = 0$ and (c)(f) with $R_{\text{CO}_2} = 0.27$ buffer layer.

dramatically lower, which is consistent with our passivation results discussed in Section 3.5. We speculate that the buffer layer enhances the crystallinity of the entire poly-SiO_x stack, thereby facilitating the confinement of boron atoms within the poly-SiO_x material due to the different diffusivity of boron in materials with varying crystallinity during high-temperature annealing [43–48].

To further examine the chemical composition across the film, samples with different buffer layers were measured by XPS after specific etching periods as shown in Fig. 3. The atomic percentages through the film are plotted as a function of the etching time. All three figures show

high atomic percentages of N before 200 s etching time, which is consistent with TEM results that there are SiN_x residuals on the top surface of samples. The presence of three oxygen peaks in the XPS results indicates that our material has three distinct phases. The first oxygen peak corresponds to the BSG phase. The second oxygen peak signifies the poly-SiO_x material phase. The third oxygen peak represents the t-SiO_x. These observations are in line with the elemental line profile obtained from TEM analysis. For the analysis of B, similar to TEM, we can also perform some qualitative analyses. In comparison to samples without a buffer layer, those with a buffer layer exhibit higher and more stable

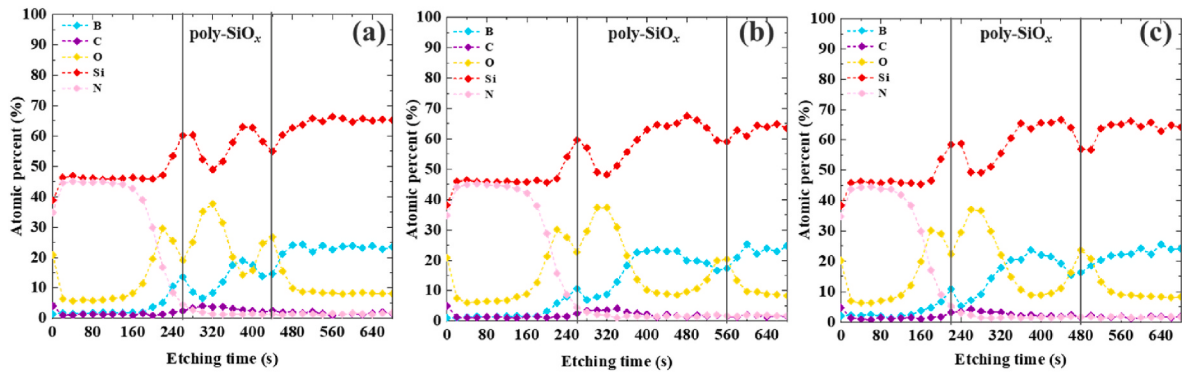


Fig. 3. XPS depth atomic percentage profile of poly-SiO_x passivating contact stacks with different buffer layer: (a) without a buffer layer, (b) with $R_{CO_2} = 0$, (c) $R_{CO_2} = 0.27$ buffer layer.

boron concentrations within the poly-SiO_x layers, which align with our findings derived from EDX analysis. Thus, the presence of the buffer layer plays a critical role in controlling boron distribution by enhancing crystallinity of poly-SiO_x stack layer.

3.2. Microstructural properties of the buffer layer

To analyze the microstructural properties of different buffer layers after the annealing process, HR-TEM images and corresponding fast Fourier transform (FFT) patterns of the buffer layers are presented in Fig. 4. As discussed in Section 3.1, the boundary between the buffer layer and poly-SiO_x becomes challenging to define after annealing. Consequently, we have chosen to compare the bottom region between the poly-Si layer and the t-SiO_x layer, as indicated between the white dashed line and the tunneling oxide layer. For a comprehensive analysis, the diffraction analysis was performed on two regions for each sample group: the regions are indicated by the yellow and green dashed rectangles. The HR-TEM image shows largely disordered structures, and the FFT patterns are almost completely diffuse with hardly any diffraction spots from Fig. 4(a), indicating that both regions in this sample are predominantly amorphous. The crystallinity of the buffer layer is found to improve as R_{CO_2} decreases observed in Fig. 4(b)(c). In particular, the sample with $R_{CO_2} = 0$ exhibits more visible crystalline structures in the HR-TEM images and more clear diffraction spots in the FFT patterns, indicating a significantly higher degree of crystallinity compared to the sample with $R_{CO_2} = 0.27$ [49]. These findings are consistent with the previous TEM and XPS analysis results.

3.3. Thickness analysis of tunnel oxide

Further TEM analyses were conducted on the reference sample as well as on samples having $R_{CO_2} = 0$ and 0.27 values after the annealing process. The results are presented in Fig. 2, where the interface t-SiO_x layer can be easily distinguished as a clear amorphous phase strip, as further illustrated in Fig. 5(a1-c1) with low magnification. To obtain more accurate thickness information of tunnel oxide, microscopically zoomed HR-TEM images of poly-SiO_x/SiO_x/c-Si interfaces are shown in Fig. 5(a–c). The interface tunnel oxide layer exhibits a uniform thickness across all samples, which can be attributed to the thermally grown oxides showing a higher tolerance to high annealing temperature [50]. Fig. 5(d–f) displays the thickness distribution of the tunnel oxide layers, which were derived from lamellar structures extracted from solar cells, with 100 points distributed across the entire lamellar structure for each sample. From the results, a very narrow thickness distribution can be observed for each sample, which indicates a good uniformity of the oxide layer. The average thickness in the reference group is 1.01 nm, which is approximately 0.5 nm less than the original thickness of 1.5 nm immediately after thermal growth. This reduction can be attributed to ion bombardment during the PECVD process [51,52], as well as the direct contact of boron atoms, which has resulted in an increased trap density within the tunnel oxide layer and facilitated boron penetration [24,51,53]. In contrast to the sample with $R_{CO_2} = 0$ which exhibits an average tunnel oxide thickness of 1.52 nm, the sample with $R_{CO_2} = 0.27$ shows an average 2.14-nm thick t-SiO_x layer. This can be explained by a contribution from the deposited doped poly-SiO_x layer. The effects of

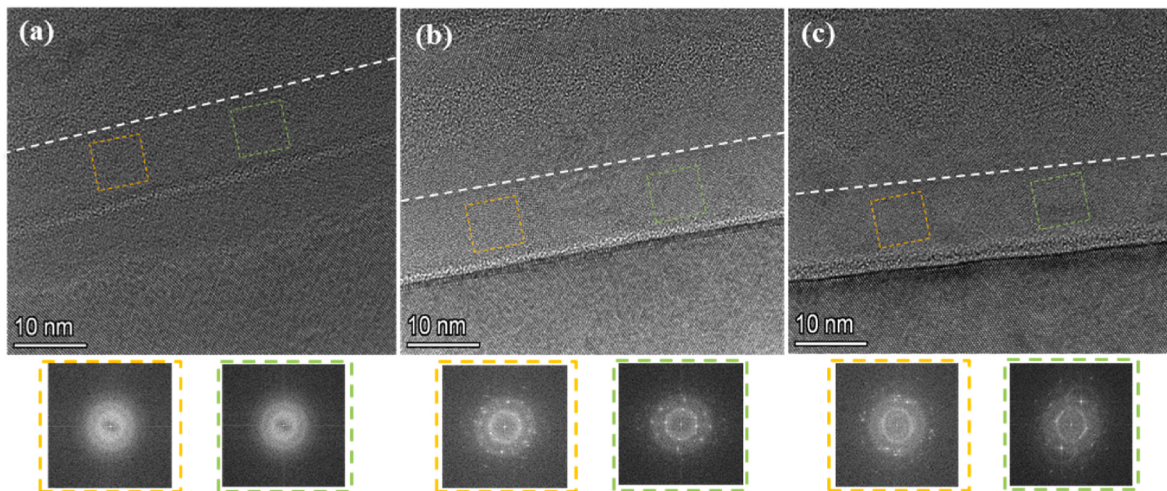


Fig. 4. HR-TEM micrographs and their corresponding fast Fourier transform (FFT) patterns of different buffer layers: (a) no buffer layer, (b) buffer layer with $R_{CO_2} = 0$, and (c) buffer layer with $R_{CO_2} = 0.27$.

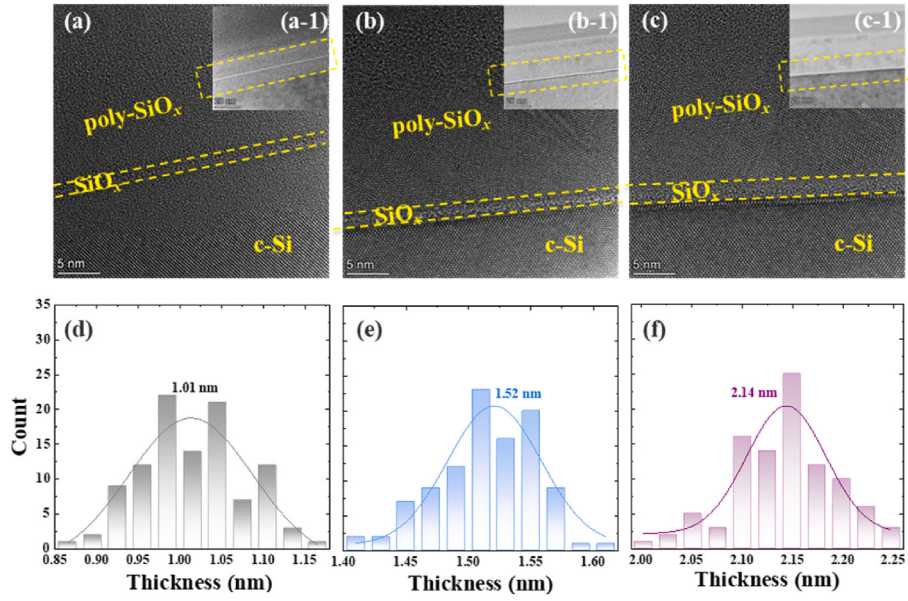


Fig. 5. HR-TEM images of poly-SiO_x stacks with varying buffer layers, along with the thickness distribution of the tunneling oxide: (a), (a-1), and (d) represent the samples without a buffer layer; (b), (b-1), and (e) correspond to samples with an $R_{CO_2} = 0$ buffer layer; (c), (c-1), and (f) show the samples with an $R_{CO_2} = 0.27$ buffer layer.

buffer layer on the thickness of t-SiO_x have not been explored in the works of Yang et al. and Nogay et al. However, it is widely recognized that the thickness of t-SiO_x plays a critical role in determining the carrier selectivity of passivating contact. Therefore, this section provides

valuable insights and cautionary guidance to researchers working in this field, emphasizing the importance of considering this factor in their studies.

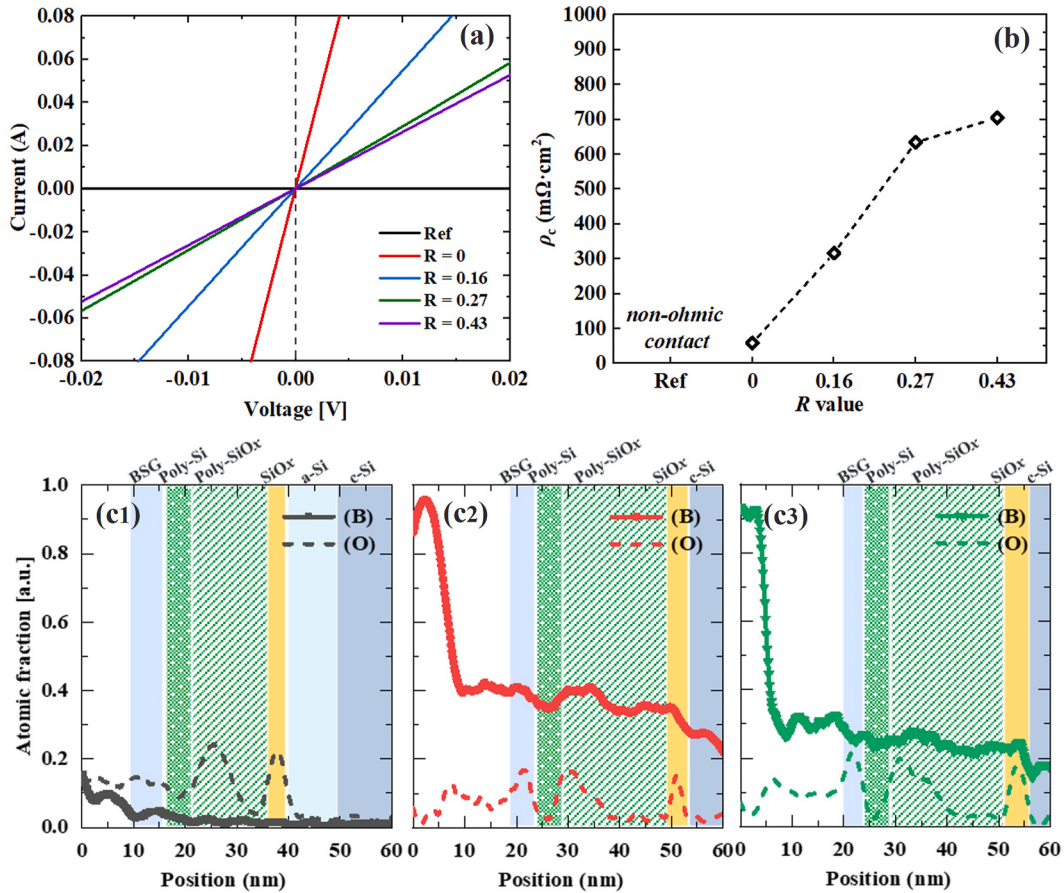


Fig. 6. (a) Dark I - V characteristics, (b) corresponding ρ_c values, and (c) EDX profiles: (c1) no buffer layer, (c2) buffer layer with $R_{CO_2} = 0$, and (c3) buffer layer with $R_{CO_2} = 0.27$.

3.4. Electrical properties

The ρ_c of samples with different buffer layers and without a buffer layer was investigated, and results are plotted in Fig. 6(a–b). The contacts with buffer layers exhibit ohmic contact behavior, with the extracted ρ_c demonstrating a significant variation depending on the value of R_{CO_2} . Specifically, ρ_c increases as R_{CO_2} rises. Optimal contact results were achieved for $R_{CO_2} = 0$. In addition, when R_{CO_2} exceeds 0, ρ_c increases significantly, reaching values greater than $300 \text{ m}\Omega \text{ cm}^2$, which are insufficient for high-efficiency FBC solar cells. In contrast, the sample without a buffer layer exhibits non-ohmic contact behavior, consistent with the elemental analysis from XPS and TEM, which indicates a low concentration of boron dopants throughout the entire stack. Additionally, EDX profiles from Fig. 2 were rearranged to display only atomic fraction of boron element for the samples without and with buffer layer, see Fig. 6(c). Considering the nominal thickness of the layers composing the stacks (as visible in TEM cross sections of Fig. 2), it is clear that the sample without a buffer layer has a lower boron atomic fraction, which can be attributed to the lower crystallinity of the entire stack. The reduced crystallinity leads to a diminished ability to confine boron atoms within the poly-SiO_x material due to the varying diffusivity of boron in materials with different crystallinities during high-temperature annealing [43–48]. Subsequently, comparing the groups with a buffer layer, the higher boron atomic fraction count is obtained when $R_{CO_2} = 0$ with respect to $R_{CO_2} = 0.27$. In ρ_c results we note that the $R_{CO_2} = 0.16$ value acts a threshold between higher and lower values. A possible explanation is that the relationship between doping and oxygen content is not linear, and when the oxygen content increases beyond a certain threshold, its effect on crystallinity or doping becomes minimal [28]. The analysis of the results in this section reveals that different buffer layers have a significant impact on electrical performance, which in turn affects the FF. This influence can be connected to the crystallinity of buffer layer discussed in section 3.2. A higher crystallinity in the buffer layer leads to better doping and, consequently, improved contact performance. However, this result and conclusion have not been extensively analyzed or reported in the relevant literature.

3.5. Passivation quality

We comprehensively investigated the passivation performance, after crystallization and hydrogenation annealing, of samples with double-side symmetrical poly-SiO_x structure integrating different buffer layer. Fig. 7(a) depicts the impact of various R_{CO_2} on passivation quality. A significant deterioration in passivation performance was observed for the reference sample compared to the samples with a buffer layer. On the one hand, this is expected, as we observed from TEM measurements

that an a-Si appears between t-SiO_x and c-Si substrate in the absence of buffer layer, which will lead to a low boron concentration within the c-Si wafer resulting in decreased field-effect passivation [54]. On the other hand, the deterioration of passivation quality can be ascribed to the break-up of the tunneling oxide layers, which experienced a thickness reduction from 1.5 to 1.01 nm, as observed in Fig. 5, due to ion bombardment during the PECVD process and increased trap density caused by boron penetration [55]. Then, when it comes to the groups with buffer layer, the passivation quality gradually improves as the oxygen content decreases, which can be attributed to a better field-effect passivation, in turn activated by a proper activation of dopants in the stack as well as a slight diffusion into the c-Si wafer [54]. However, as the thickness of t-SiO_x increases from 1.5 nm to 2.14 nm for increasing R_{CO_2} from 0 to 0.27, which can be explained by a contribution from the doped deposited poly-SiO_x layer [56], the diffusion of dopants into the wafer is hindered, resulting in lower-quality field-effect passivation [54]. Ultimately, further increasing the oxygen content to $R_{CO_2} = 0.43$, as a thicker oxide layer is expected, much poorer field effect passivation results in lower passivation quality than the case with buffer layer and $R_{CO_2} = 0$. After hydrogenation, the optimal passivation results with an iV_{oc} of 728.3 mV can be achieved under $R_{CO_2} = 0$ condition for double-side-flat *p*-type poly-SiO_x stack. These findings underscore the critical role of intrinsic a-Si buffer layer in promoting excellent passivation quality for *p*-type poly-SiO_x passivating contacts.

To further assess the passivation properties, the τ_{eff} values versus injection intensity are plotted for samples with different R_{CO_2} after the crystallization annealing at 925 °C for 30 min, as presented in Fig. 7(b). The observed curves exhibit a trend similar to that of the iV_{oc} . Overall, carrier lifetime increases with decreasing R_{CO_2} . Especially, the difference in lifetime for different R_{CO_2} is much more pronounced at excess minority carrier densities below $3 \times 10^{15} \text{ cm}^{-3}$, indicating a more significant presence of Shockley-Read-Hall (SRH) recombination in the samples with higher R_{CO_2} [57,58]. The sample without buffer layer shows a notably lower effective carrier lifetime of 0.84 ms. Firstly, the emergence of the amorphous silicon phase will lead to an increase in bulk SRH recombination. Secondly, the thinning of the tunneling oxide layer results in higher surface SRH recombination due to insufficient chemical passivation. Furthermore, the incorporation of oxygen will increase the risk of forming B-O complexes as interface defects [57]. When such defects cannot be effectively passivated, the τ_{eff} is adversely affected.

3.6. Cell results

To investigate the influence of the buffer layer's potential at the device level, solar cells were fabricated using both the optimal buffer

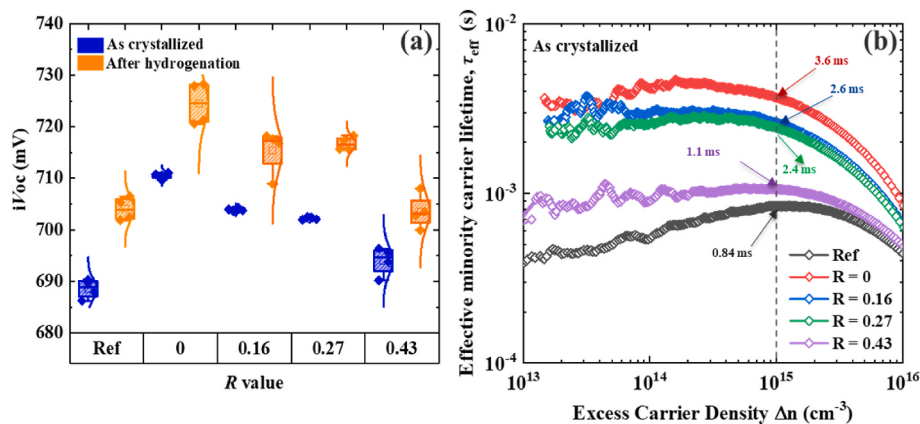


Fig. 7. Evaluation of passivation quality of *p*-type poly-SiO_x/SiO_x/c-Si structures without and with a buffer layer between poly-SiO_x and SiO_x layers: (a) iV_{oc} as crystallized (blue) and after hydrogenation (orange), evaluated $\Delta n = 10^{15} \text{ cm}^{-3}$; and (b) effective minority carrier lifetime curves of samples as crystallized with buffer layer showing different R_{CO_2} values. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

layer condition with $R_{\text{CO}_2} = 0$ and without any buffer layer as a reference. The comparison of the best J - V curves and the average FF for five samples under each condition is illustrated in Fig. 8, while additional detailed electrical parameters are presented in Fig. S2. The FBC solar cells with $R_{\text{CO}_2} = 0$ demonstrate an optimal efficiency of 18.9 % with an open-circuit voltage (V_{oc}) of 677 mV, a short-circuit current density (J_{sc}) of 35.6 mA/cm², and an FF of 78.4 %. By contrast, the cells without a buffer layer exhibit a significantly lower efficiency of 3.55 %, with a notably low FF of 17.4 %. The significant improvement in FF with the buffer layer can be primarily attributed to the significantly reduced ρ_c . The lower ρ_c reduces the barrier for hole transport, facilitating more efficient charge carrier movement, which in turn positively influences the J_{sc} . Additionally, we also observe an increase in V_{oc} when compared to cells without a buffer layer, which is consistent with passivation results, suggesting that the buffer layer effectively reduces recombination losses.

According to these findings, the presence of a buffer layer is crucial for achieving high-performance solar cells. In this study, we only investigate the impact of PECVD-deposited buffer layers with varying oxygen content on device performance to promote, in future developments, a lean flow chart fully based on PECVD technique, including the tunneling oxide [59]. However, as discussed in previous sections, the crystallinity of the buffer layer significantly affects the final device performance. In this respect, due to the minimal hydrogen content, LPCVD-based silicon thin films can achieve higher crystallinity [60] and be less absorptive [18] after high-temperature annealing than PECVD-based ones [60]. To corroborate this statement and building up on our previous experience, when we included LPCVD buffer layer into our poly-SiO_x stacks [16], we also newly fabricated solar cells as in Fig. 1 (a) but endowed with 10-nm thick LPCVD buffer layer. As shown in Fig. S3, we achieved an efficiency of 21.15 %, which not only increases our previous performance [16] but also corresponds to a $J_{\text{sc}} = 39.62$ mA/cm², underlining the optical potential of poly-SiO_x-based CSPCs endowed with a dense buffer layer. Detailed mechanistic analysis of the improvement in device performance will be explored further.

4. Conclusions

In this work, we investigate the impact, as function of oxygen content R_{CO_2} of a thin intrinsic buffer layer placed between the t-SiO_x and the poly-SiO_x (p^+) layers on the performance of passivating contacts in c-Si solar cells. Cross-sectional HR-TEM micrographs reveal that the crystallinity of poly-SiO_x stacks is significantly influenced by both the presence and composition of the buffer layer. In the absence of a buffer layer, a dramatic reduction in crystallinity within the poly-SiO_x stacks is observed, accompanied by the emergence of an a-Si phase between the t-

SiO_x layer and the c-Si substrate. Furthermore, in the presence of a buffer layer, the crystallinity of the layers progressively increases as the oxygen content decreases, which subsequently affects the boron doping concentration within the poly-SiO_x, as evidenced by XPS results. Additionally, the thickness of the t-SiO_x is also influenced by the buffer layer, specifically, the thickness of t-SiO_x increases with higher oxygen content in the buffer layer. In contrast, the thinnest t-SiO_x is obtained in the case without buffer layer. These structural modifications directly influence the passivation quality and contact properties, thereby impacting overall device performance. Through these analyses, our findings provide a deeper and broader understanding of the role of the buffer layer in p -type poly-SiO_x passivating contacts, laying a foundational basis for future research.

Notably, the p -type sample with an $R_{\text{CO}_2} = 0$ buffer layer shows significant improvements in surface passivation and contact properties with iV_{oc} of 728.3 mV and ρ_c of 59.18 mΩ cm² after hydrogenation. At device level, the best cell with an V_{oc} of 677 mV, FF of 78.4 %, J_{sc} of 35.6 mA/cm², and an efficiency of 18.9 %, are obtained with an $R_{\text{CO}_2} = 0$ buffer layer. To further demonstrate the necessity of a buffer layer showing higher crystallinity, we employed an LPCVD buffer layer, achieving an efficiency of 21.15 %. These findings highlight the potential of high-crystallinity buffer layers to enhance solar cell performance, suggesting a promising avenue for further efficiency improvements.

CRediT authorship contribution statement

Yingwen Zhao: Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Paul Procel Moya:** Writing – review & editing, Methodology. **Yifeng Zhao:** Writing – review & editing, Validation, Methodology. **Zhirong Yao:** Writing – review & editing. **Jin Yan:** Formal analysis. **Hiroki Nakajima:** Writing – review & editing. **Engin Özkol:** Writing – review & editing. **Miro Zeman:** Writing – review & editing, Funding acquisition. **Luana Mazzarella:** Writing – review & editing, Supervision, Methodology, Conceptualization. **Olindo Isabella:** Writing – review & editing, Validation, Supervision, Project administration, Methodology, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Zhirong Yao reports financial support was provided by The Topsector Energie of the Dutch Ministry of Economic Affairs. Yingwen Zhao reports financial support was provided by China Scholarship Council (CSC NO. 202208320029). If there are other authors, they declare that they

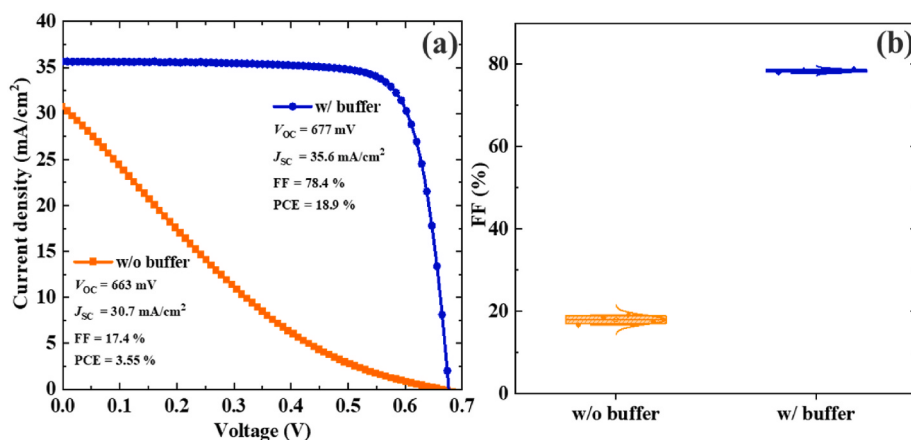


Fig. 8. (a) J - V characteristics of best solar cells without (orange) or with (blue) a buffer layer; (b) average FF calculated from five cells of each type. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.solmat.2025.113418>.

Data availability

Data will be made available on request.

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