Reducing Switching Artifacts in Chopper Amplifiers

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Reducing Switching Artifacts in Chopper Amplifiers

Yoshinori Kusuda

Reducing Switching Artifacts in Chopper Amplifiers

Proefschrift

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To my wife Kyoko and children Ryoko, Yukinori, and Kazunori

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Chapter 1

Introduction

This thesis describes the theory, design, and implementation of chopper amplifiers in CMOS integrated circuits (ICs). As the name implies, such amplifiers employ chopping to achieve low offset and low 1/*f* noise. Chopping is a circuit technique that involves up-modulating amplifier offset and low frequency noise to higher frequencies, and which therefore can achieve microvolt-level offset with very low temperature drift. On the other hand, it causes switching artifacts such as AC ripple and glitches at the amplifier's output, which usually need to be attenuated by low-pass filtering, thus decreasing the usable signal bandwidth. As a result, the use of chopper amplifiers has mainly been limited to low frequency applications. This thesis explores advanced circuit techniques to reduce such switching artifacts without decreasing the usable signal bandwidth, thus enabling the use of chopper amplifiers in a broader range of applications.

This chapter introduces the main objectives of this work. After a review of the key requirements of amplifiers in signal chains, the offset and low frequency noise behavior of a basic CMOS amplifier are described. Next, the chopping technique is presented, followed by a description of its traditional use in low frequency applications. Some newer applications are then described, which also require low offset and 1/*f* noise, but in which signal frequencies are too high for switching artifacts to be reduced by low-pass filtering. Lastly, the challenges associated with reducing switching artifacts in such applications are discussed.

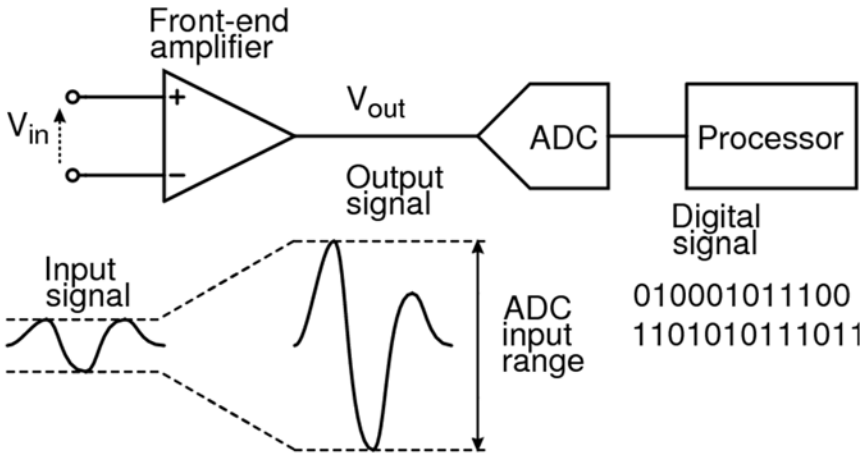

Figure 1-1: Precision data acquisition signal chain

1.1 Precision Data Acquisition Signal Chain

In today's digital signal processing era, analog signals from the real world are ubiquitously acquired and converted into digital signals for use in factories, test equipment, and healthcare systems. The new Internet of Things (IoT) era will lead to the acquisition of even more analog signals in vehicles, buildings, and even homes [1,2]. As a result, manufacturers will need to develop a wide variety of data acquisition signal chains in less time and at lower cost. Those with a resolution of 16 bits or higher are classified as precision data acquisition signal chains typically intended for physical signals, such as light, sound, temperature, pressure, magnetic field, and force. Such signals have relatively low frequency spectra ranging from DC to a few kilohertz or at most up to a few hundred kilohertz.

Figure 1-1 shows an example of a precision data acquisition signal chain consisting of a front-end amplifier, an analog-to-digital converter (ADC), and a digital processor [3]. The amplitude of the input signal V_{in} is often smaller than the full scale input range of the ADC. Therefore, the front-end amplifier must amplify V_{in} and produce an output V_{out} with an amplitude large enough to utilize the full range of the ADC. The amplifier's input errors may dominate the overall system performance, since they are added before the signals are amplified. For instance, when the front-end amplifier is configured for a gain of 100 and its output is applied to a 16-bit

ADC with a 5V full scale input, an input error of only 0.76μV corresponds to one LSB error in the resulting digital output. The offset and noise of the front-end amplifier must therefore be lower than this in order to maintain true 16-bit performance.

Other common requirements of a front-end amplifier are a wide input range and high common-mode rejection ratio (CMRR). This is because in certain applications, the input signals may be associated with common-mode noise and disturbances. Some applications, e.g. bridge readout, require the amplification of millivolt-level differential signals, while rejecting a few volts of common-mode noise. Additionally, the amplifier's input bias current should be low enough for applications where the input signal sources have high impedances. On top of all these requirements, cost and power efficiency are also important nowadays, especially since ADCs and digital processors have become cheaper and more power efficient thanks to the steady scaling of CMOS technology. In summary, front-end amplifiers are key elements of precision data acquisition signal chains, and can dominate their overall performance and cost.

1.2 CMOS Operational Amplifiers

1.2.1 Functionality

A front-end amplifier can be integrated on a single chip with an ADC, or can be realized off-chip with the help of a monolithic instrumentation amplifier (IA) or an operational amplifier (op-amp). While the first two options often result in a more compact subsystem and/or optimized performance, monolithic op-amp based implementations offer design flexibility. By modifying their feedback networks, such op-amps can realize different closed-loop transfer functions and accept various types of input signals, such as single-ended or differential, voltages or currents etc. [4]. This thesis presents original op-amp designs implemented as monolithic ICs. However, most of the theory and techniques presented are also applicable to IAs and other integrated amplifiers.

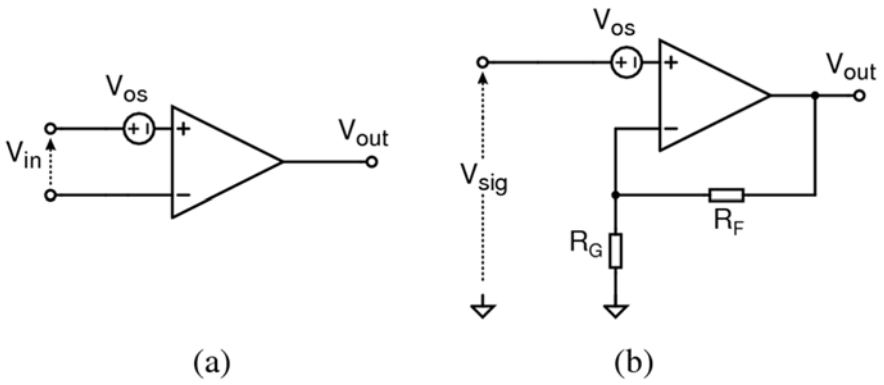

Figure 1-2: (a) Symbol of an op-amp; (b) closed-loop amplifier using an op-amp

Figure 1-2 (a) shows the symbol of an op-amp that amplifies a small differential input voltage V_{in} with a high open-loop gain A_{OL} [5-7]. This produces an output voltage V_{out} equal to:

$$V_{out} = A_{OL}(V_{in} - V_{os}), \qquad (1\text{-}1)$$

where V_{os} is the input offset voltage. In fact, as shown in Figure 1-2 (b), an op-amp is usually configured as a closed-loop amplifier with an input signal V_{sig}. The output voltage V_{out} and closed-loop gain A_{CL} are determined by external gain-setting resistors R_G and R_F, and is given by:

$$V_{out} \equiv A_{CL}\,(V_{sig} - V_{os}) \qquad (1\text{-}2)$$

$$A_{CL} = \frac{1}{1+\varepsilon}\left(1 + \frac{R_F}{R_G}\right) \qquad (1\text{-}3)$$

$$\varepsilon = \frac{1}{A_{OL}}\left(1 + \frac{R_F}{R_G}\right), \qquad (1\text{-}4)$$

where ε is a gain error due to an insufficient amount of A_{OL}. Additionally, V_{os} is superimposed onto V_{sig} and thus also degrades the precision. Therefore, op-amps should provide a sufficiently high open-loop gain and low offset to minimize the overall error. Those providing more than 100dB A_{OL} and less than 100µV V_{os} are classified as precision op-amps [8].

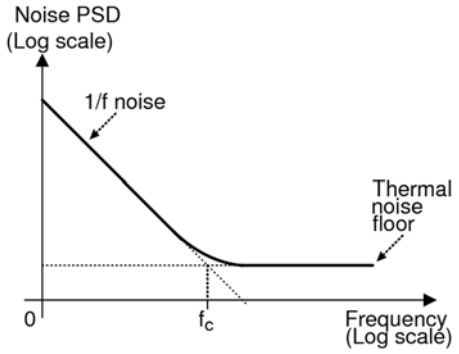

Figure 1-3: Noise PSD of a typical CMOS op-amp

1.2.2 Offset and Noise

Offset is a deterministic DC error and is usually the result of the systematic and random device mismatch that occurs during IC fabrication. The amount of device mismatch depends on device size and process technology. Since individual op-amps will then have unique offsets, only the standard deviation and maximum value of this offset can be specified for a given design. Typical CMOS op-amps have maximum offsets in the order of a few millivolts to tens of millivolts [9]. Offset can change with temperature and the input common-mode voltage; these changes are expressed by offset drift and CMRR specifications.

Noise, on the other hand, is completely due to random processes. It can be modeled as a zero-mean random error signal that is superimposed on an input signal. Figure 1-3 shows the noise power spectral density (PSD) of a typical CMOS op-amp. At higher frequencies it is flat and dominated by thermal noise. This can be reduced by increasing the amplifier's input transconductance at the cost of current consumption. To evaluate the power efficiency of an amplifier, the noise efficiency factor (NEF) is defined as:

$$NEF = v_{n,rms}\sqrt{\frac{I_{tot}}{4kTV_t}\cdot\frac{1}{BW\cdot\pi/2}}, \qquad (1\text{-}5)$$

where $v_{n,rms}$ is the total integrated RMS noise over frequency, I_{tot} is the current consumption, V_t is the thermal voltage equal to kT/q, and $BW\bullet\pi/2$ is the noise bandwidth of the amplifier [10]. When $v_{n,rms}$ is dominated by thermal noise, and is band-limited by a first order low-pass filtering, this equation can be simplified to:

$$NEF = e_n \sqrt{\frac{I_{tot}}{4kTV_t}}, \qquad (1\text{-}6)$$

where e_n is the input noise PSD. A differential pair realized by two bipolar transistors with no 1/*f* noise has an NEF of unity. On the other hand, a CMOS op-amp usually has a higher NEF due to various factors: the presence of more than one dominant noise source in its input stage; the current consumption of the subsequent gain stages; and the fact that for the same current the thermal noise of a MOS transistor is higher than that of a bipolar transistor. At lower frequencies, the noise PSD is dominated by 1/*f* noise, which increases as the frequency decreases [5]. The amount of 1/*f* noise and hence the corner frequency f_c depend on the device size and the process technology. Typical CMOS op-amps have corner frequencies in the range of a few kilohertz to tens of kilohertz.

1.2.3 Summary

CMOS op-amps suffer from considerable offset and 1/*f* noise which dominates their overall error in low frequency applications. Although such errors can be reduced by increasing device sizes, this will increase chip area and hence production cost. Offset can also be reduced by post-production trimming. However, this will usually not compensate well for offset drift over temperature. For these reasons, most precision op-amps have been realized in bipolar processes which offer lower offset and 1/*f* noise than CMOS processes. On the other hand, CMOS op-amps have a number of advantages, and thus are gaining popularity. First, most precision ADCs and digital processors are realized in CMOS processes, and so can be co-integrated with CMOS op-amps. Second, CMOS wafers are cheaper than bipolar or JFET ones. Third, digital logic and analog switches can be easily implemented in CMOS processes, enabling the use of various dynamic error correction techniques. Specifically, dynamic offset cancellation techniques such as auto-zeroing and chopping, can reduce offset and offset drift to levels significantly lower than those of trimmed bipolar op-amps [11]. Thus, chopper and auto-zero op-amps in CMOS processes have successfully served applications requiring microvolt-level offset, very low temperature drift, and/or low 1/*f* noise [11].

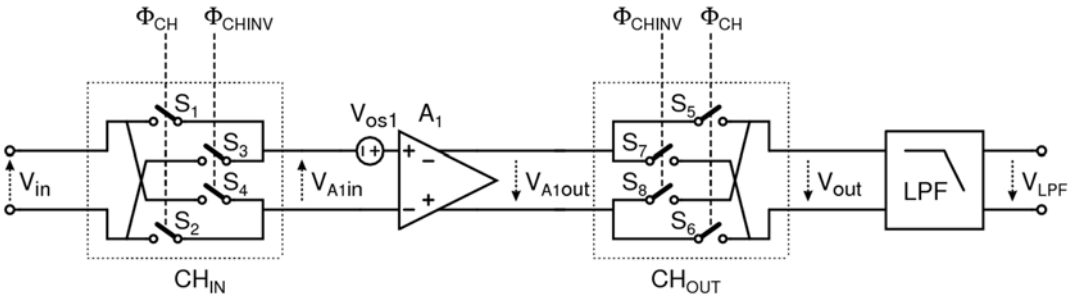

Figure 1-4: Functional diagram of chopping

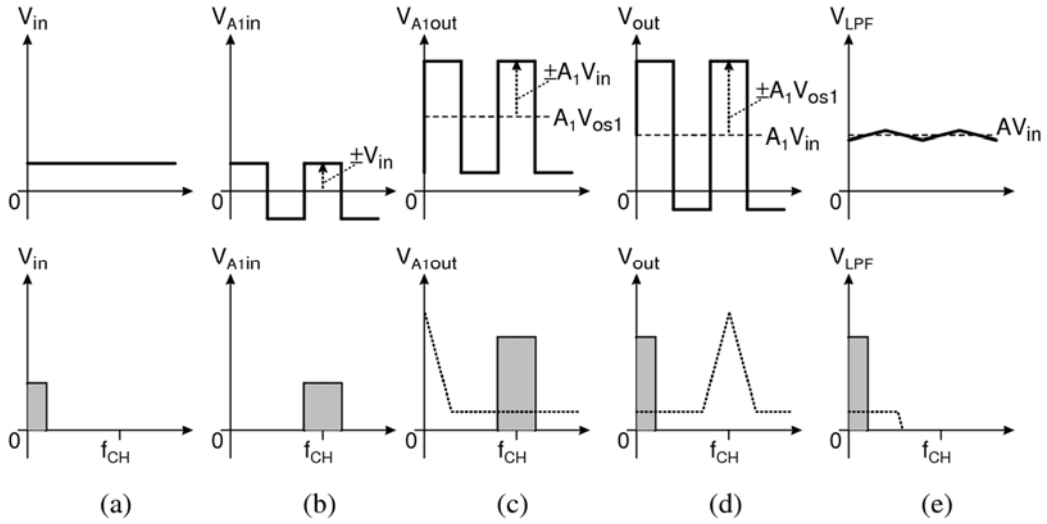

Figure 1-5: Signal, offset, and noise in the time and frequency domains

1.3 Chopping Principle

Chopping is a frequency modulation technique that is used to separate undesired offset and low frequency noise from low frequency signals [12]. Figure 1-4 shows a functional diagram of a chopper amplifier, consisting of an input chopper CH_{IN}, an amplifier A_1, an output chopper CH_{OUT}, and a low-pass filter (LPF). Additionally, A_1 is associated with an undesired input offset V_{os1}. The modulation is performed by CH_{IN} and CH_{OUT}, each of which consists of four switches $S_{1\text{-}4}$ and $S_{5\text{-}8}$, respectively. These switches are driven by complementary clocks Φ_{CH} and Φ_{CHINV} operating at a chopping frequency f_{CH}.

Figure 1-5 shows the signal, offset, and noise in the time and frequency domains to

illustrate how they are modulated. A low frequency input signal V_{in}, shown in Figure 1-5 (a), is first up-modulated to f_{CH} by CH_{IN} (Figure 1-5 (b)). Next, A_1 amplifies the up-modulated signal along with the offset and noise (Figure 1-5 (c)). This up-modulated signal and the thermal noise around f_{CH} are then down-modulated back to baseband by CH_{OUT}. Meanwhile, CH_{OUT} up-modulates the offset and the low frequency noise to f_{CH}, and thus produces switching artifacts (Figure 1-5 (d)). The LPF attenuates the switching artifacts, so that in the low frequency signal only the thermal noise floor interferes (Figure 1-5 (e)). However, the cutoff frequency of the LPF needs to be set lower than f_{CH}, which limits the usable signal bandwidth.

1.4 Traditional Applications of Chopper Op-Amps

As explained in the previous section, chopping up-modulates low frequency errors and produces switching artifacts. Thus, this technique has traditionally been used in low frequency applications, where offset and 1/*f* noise must be low, but in which high frequency noise can be attenuated by low-pass filters. This section reviews traditional applications of chopper op-amps along with the required performance.

1.4.1 Sensor Signal Conditioning

Sensors convert physical signals, such as light, sound, temperature, pressure, magnetic field, force, into electrical signals [13]. These electrical signals can be in the form of voltages, currents, resistances, or other quantities that are often quite small. Therefore, a front-end amplifier is required to produce a voltage output with an amplitude that is compatible with the full scale input of the ADC. Figure 1-6 shows a circuit diagram consisting of an op-amp and two gain setting resistors R_F, to amplify a bridge sensor signal [13]. The physical signal of interest is converted into a resistance change ΔR in a resistive sensor R_S. Consequently, the front-end amplifier produces an output voltage V_{out} given by:

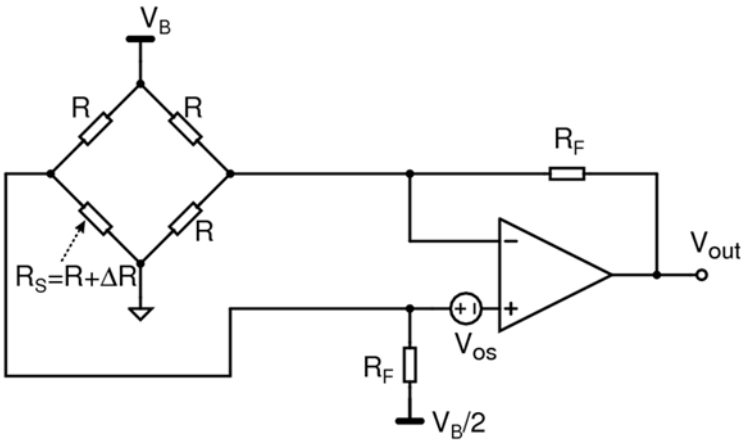

Figure 1-6: Bridge sensor and the front-end amplifier

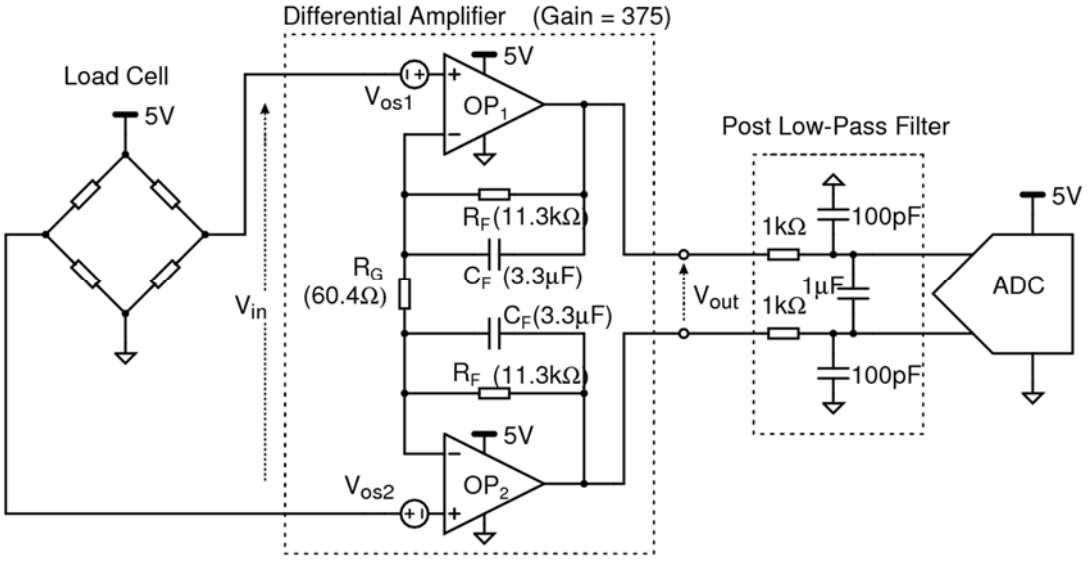

Figure 1-7: Load cell data acquisition signal chain

Table 1-1: System specification of Figure 1-7

	Op-amp error		ADC error	Total error
	1x op-amp Input referred	2x op-amp Output referred		
Offset	0.3 μV	159 μV	3 μV	273 LSB
Offset drift	2 nV/°C	1.0 μV/°C	0.01 μV/°C	1.8 LSB/°C
Noise PSD	5.6 nV/√Hz	3.0 μV/√Hz	-	-
Noise BW	-	6.7 Hz	-	-
RMS Noise	-	8.1 μVrms	1.1 μVrms	13.6 LSB,rms

$$V_{out} \approx \left(1 + \frac{R_F}{2R}\right) \cdot \left(\frac{\Delta R \cdot V_B}{2} + V_{os}\right) + \frac{V_B}{2}, \qquad (1\text{-}7)$$

where V_B is an excitation voltage for the bridge, and V_{os} is an input offset voltage of the op-amp. The input signal $\Delta R \bullet V_B/2$ is often at the millivolt-level. Therefore, the op-amp must have a microvolt-level input offset, and provide a closed-loop gain ($1+R_F/2R$), possibly of a few hundred or higher. Additionally, the offset must be stable with the changes in temperature or the input common-mode voltage that occur in many applications. Moreover, the $1/f$ noise should also be low, since signal frequencies are typically well below one kilohertz.

Figure 1-7 shows a specific example of a sensor data acquisition signal chain, consisting of a bridge load cell, a front-end differential amplifier, and a differential ADC [14]. The amplifier is configured for a gain of 375, with two op-amps $OP_{1,2}$ and gain settling resistors R_G and R_F. Additionally, $OP_{1,2}$ are chopper op-amps that have a 0.3μV typical offset, 2nV/°C offset drift, and 5.6nV/√Hz noise PSD [15]. The noise bandwidth is set to 6.7Hz with two feedback capacitors C_F and a low-pass filter. This filter attenuates the switching artifacts of the chopping at 200kHz by a factor of 90dB. The ADC has a 24-bit resolution with a 10V differential full scale input and a 0.6μV LSB [16]. Table 1-1 lists the error contributions of the op-amps and the ADC, as well as the resulting total error. It can be seen that due to their high gain, the op-amps dominate the total error.

1.4.2 Current Sensing

Another application example is in supply current sensing, the block diagram of which is shown in Figure 1-8 [17]. The goal is to monitor a load current I_{load} drawn from a DC power supply V_{SY}. A difference amplifier is realized by an op-amp and four resistors to amplify the voltage drop across a sense resistor R_{sense}. A relatively low voltage drop is preferred, in order not to affect the load. Therefore, the op-amp should have a low input offset to sense this low voltage drop. In this example, R_{sense} is placed between the load and the ground, setting the input common-mode voltage of the difference amplifier near the ground. In another example, R_{sense} can be placed between V_{SY} and the load, setting the input common-mode voltage near V_{SY}.

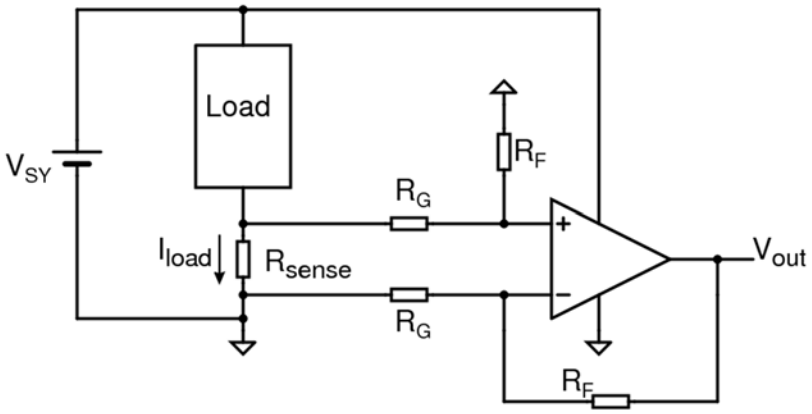

Figure 1-8: Current sensing amplifier for DC supply

Therefore, op-amps for this application should have wide input common-mode voltage ranges (ideally rail-to-rail).

1.4.3 Summary

In sensor signal acquisition and DC supply current sensing applications, the input signals are quite small, with signal frequencies usually well below one kilohertz, thus amplifiers with high closed-loop gains are necessary. However, low-pass filters with low cutoff frequencies can be readily applied to attenuate the switching artifacts of chopping. These filters also limit the noise bandwidth, so that a relatively high thermal noise PSD is tolerable. Lastly, input source impedances are typically lower than a few kΩ, so that nano-Ampere level input bias currents are also tolerable.

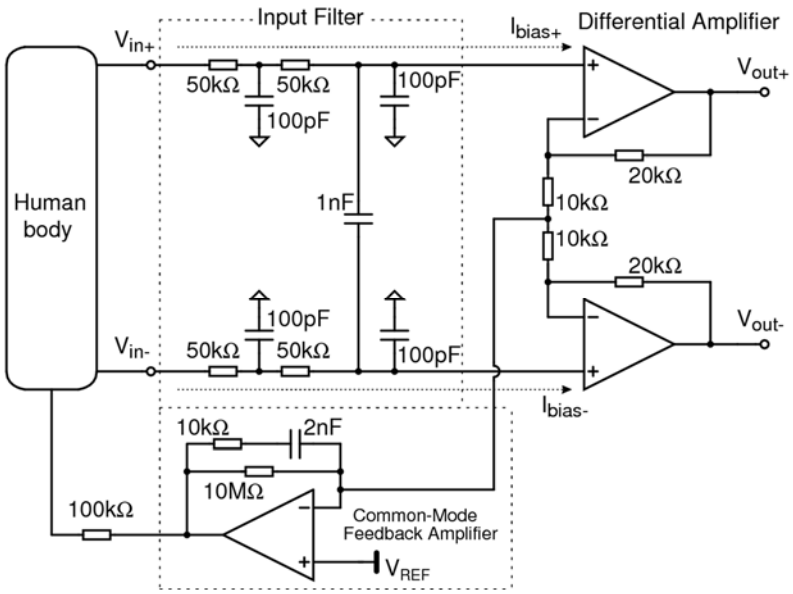

Figure 1-9: ECG front-end circuit

1.5 Newer Applications of Chopper Op-Amps

As discussed in the previous section, chopper op-amps mainly serve applications where signal frequencies and signal source impedances are relatively low. However, a broader range of applications could be served, if the switching artifacts of chopping could be pushed to higher frequencies and/or if their magnitudes could be reduced. This section introduces some new applications that have previously been served by precision bipolar or JFET op-amps. It also discusses the extra requirements that chopper op-amps will have to meet to serve these applications, which form the main motivation for the work in this thesis.

1.5.1 Biomedical Sensing Front-End

Biomedical sensing systems such as Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) require front-end differential amplifiers to boost the tiny voltages picked up by electrodes on the patient's skin [18, 19]. Figure 1-9 shows the block diagram of a typical front-end, consisting of a common-mode feedback amplifier, an input filter, and a

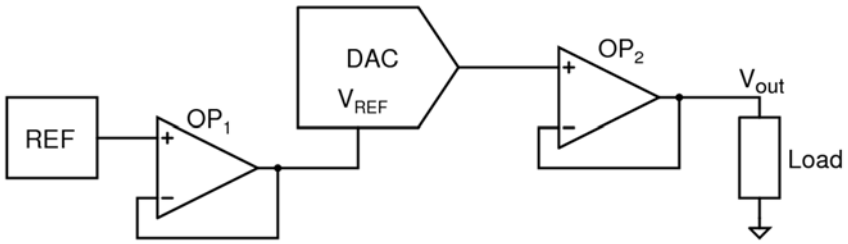

Figure 1-10: Precision DAC configuration

differential amplifier. Since the bandwidth of these biomedical signals is about 200Hz, chopper op-amps with low 1/*f* noise are preferred, and an external low-pass filter can be applied to attenuate the switching artifacts at the chopping frequency. However, as will be explained later, due to their input switching, chopper op-amps have input bias currents I_{bias+} and I_{bias-}. In conjunction with the 100kΩ input filter resistors required for patient isolation, this can cause significant errors. For instance, a 1nA bias current mismatch will cause a 100µV differential input offset. To avoid such large errors, the input bias currents should be at the 100pA level or lower. Moreover, for portable and wearable applications, each op-amp should have a low power consumption under 100 microwatts, and fit into a small package such as SC-70. Furthermore, a wide supply voltage range including 1.8V is preferred in order to share the supply voltage with other components such as ADCs and digital processors.

1.5.2 Reference and DAC Buffers

Precision op-amps are often used to buffer voltage references and DACs. Figure 1-10 shows an example of a precision DAC configuration, consisting of a reference, a reference buffer OP_1, a DAC, and a DAC output buffer OP_2 [20]. DACs and ADCs often generate kickback on their reference pins, so that the buffers need to quickly recover and provide stable voltages. Similarly, ADCs often generate kickback on their input pins due to the sampling action of their input circuitry. The DAC output buffer OP_2 needs to provide wide input and output ranges, and to drive resistive and/or capacitive loads. As a result, any switching artifacts should be small and outside the signal band. This particular DAC is capable of generating a 2MHz output signal, so that the switching artifacts should be above a few Megahertz. Additionally, OP_1 and OP_2 should be stable and perform well in a unity gain configuration.

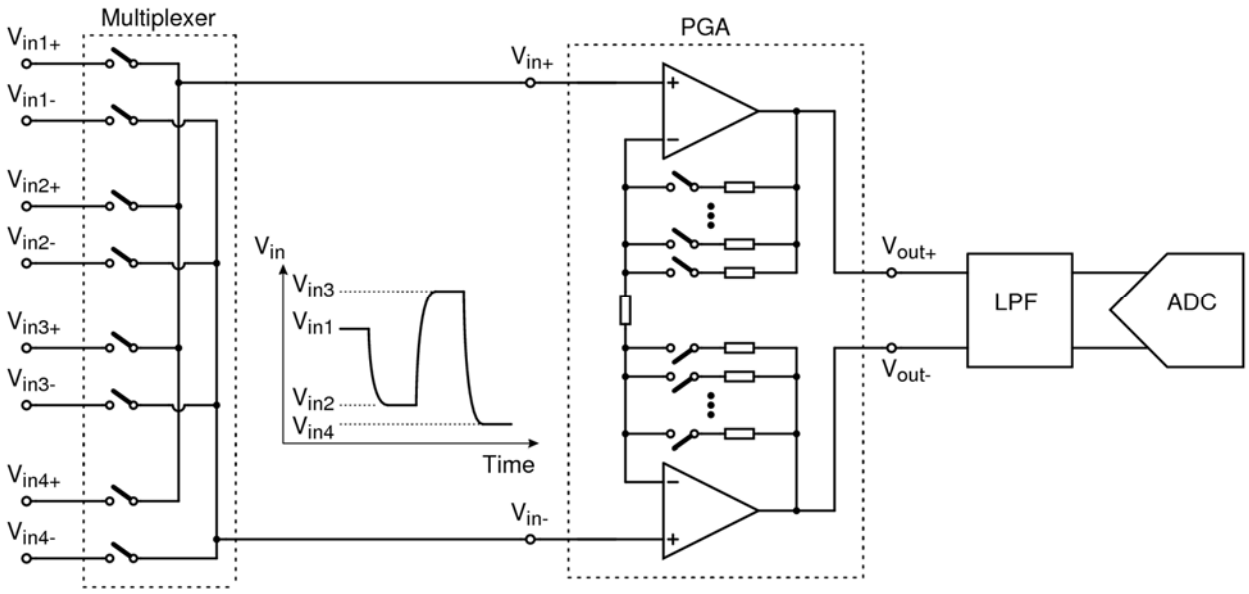

Figure 1-11: Process control signal acquisition chain with input multiplexer

1.5.3 Process Control Data Acquisition Signal Chain

Process control data acquisition signal chains are used in many locations such as automated factories, oil refineries, aerospace systems, as well as in medical equipment [21]. Figure 1-11 shows a typical block diagram consisting of a multiplexer, a programmable gain amplifier (PGA), a low-pass filter (LPF), and an ADC. The PGA consists of two op-amps and resistors, and has a selectable gain, typically ranging from one to ten. Each of the differential input signals $V_{in1\text{-}4}$ would represent physical signals, e.g. pressure, temperature, flow, etc., with frequencies typically below one kilohertz. However, when the multiplexer switches, the differential input of the PGA V_{in} quickly changes. This change can be as large as the full scale input of the ADC, and the allowed settling time may be only in the order of a few microseconds. Therefore, the closed-loop bandwidth of the PGA and the cutoff frequency of the LPF must be in the order of a few hundred kilohertz or higher. Any switching artifacts should then be minimized and be located above the Megahertz range. Additionally, the input signals may be at various common-mode levels with large common-mode noise, after being transmitted through a harsh environment. Therefore, the op-amp should also have a wide input common-mode voltage range, possibly up to ±10V, along with a high AC CMRR.

1.6 Challenges

The previous sections discussed traditional applications of chopper op-amps, as well as some newer ones. To justify their development costs, chopper op-amp designs should cover as many of these applications as possible. This is especially true for a stand-alone op-amp IC or an op-amp IP core intended for use in a variety of other ICs. Such a chopper op-amp should have small switching artifacts located at higher frequencies, while achieving low offset and low $1/f$ noise. Additionally, a low noise PSD, wide supply range, and wide common-mode voltage range will allow the op-amp to be used in a broader range of applications.

The chopping frequency should be set high enough to extend the usable signal bandwidth and to cover the newer applications. However, apart from the traditional op-amp design trade-offs between noise PSD, current consumption, and die area, chopper op-amp design also involves specific trade-offs between noise PSD, chopping frequency, and residual offset, caused by the switching artifacts.

1.7 Organization of the Thesis

This thesis presents circuit techniques that reduce the switching artifacts in chopper amplifiers, so as to achieve the levels of performance described in the previous section. Some of the proposed techniques can push the noise spectra peak to higher frequencies and reduce their magnitude, without significantly increasing the residual offset. Consequently, the proposed chopper op-amps offer wider usable signal bandwidths as well as superb DC performance, and therefore can be implemented in a broader range of applications.

Chapter 2 reviews three offset cancellation techniques—trimming, auto-zeroing, and chopping—including their advantages and disadvantages. In the review of the chopping technique, various switching artifacts are explained, including up-modulated ripple, output glitches, residual offset and input bias current, and gain reduction due to dynamic switching conductance. Next, Chapter 3 reviews some previous techniques that reduce some of these

switching artifacts.

Some original contributions are presented in Chapters 4, 5 and 6. Each chapter presents an individual design project, along with the proposed techniques, the overall op-amp design, and the measurement results. In Chapter 4, a local feedback technique, called auto-correction feedback (ACFB) is proposed to reduce the up-modulated ripple. This technique is implemented in a low power chopper op-amp design that draws 13μA from a 1.8 to 5.5V supply, to serve low power applications.

Chapter 5 presents a chopper op-amp that achieves a 5.6nV/√Hz noise PSD and a 0.5μV maximum offset, to serve applications requiring very small low frequency error. In order to mitigate the trade-off between the noise PSD and the residual offset, an adaptive clock boosting technique is employed in the input chopper. This minimizes its charge injection and keeps it constant over the amplifier's rail-to-rail input common-mode voltage range.

Chapter 6 presents a chopper op-amp, which operates from a 4.5-60V supply, and is intended to serve industrial applications that require wide supply and input common-mode voltage ranges as well as wide usable signal bandwidth. Two techniques are proposed to locate switching artifacts at higher frequencies and to reduce their magnitude. First, this op-amp employs six parallel input stages driven by 800kHz interleaved clocks, so as to locate the majority of the switching energy at 4.8MHz. Second, the input chopper incorporates a charge mismatch compensation circuit to reduce the maximum input bias current from 1.5nA to 150pA at post-production trimming. The thesis ends with Chapter 7, in which its original contributions are reviewed and the performance of the various designs is compared with the state-of-the-art.

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Chapter 2

Offset Cancellation Techniques

This chapter reviews offset cancellation techniques for amplifiers. First to be reviewed is offset trimming, in which offset is measured and then corrected at post-production test. Since the correction is performed only once, offset drift over time and temperature usually remains uncorrected. Next, after an explanation of the properties of MOS switches, a review is presented of dynamic offset cancellation techniques, such as auto-zeroing and chopping. Unlike offset trimming, these techniques periodically correct offset, and thus reduce offset drift and $1/f$ noise. However, as will be discussed, these techniques also have drawbacks, which include various residual DC and AC errors.

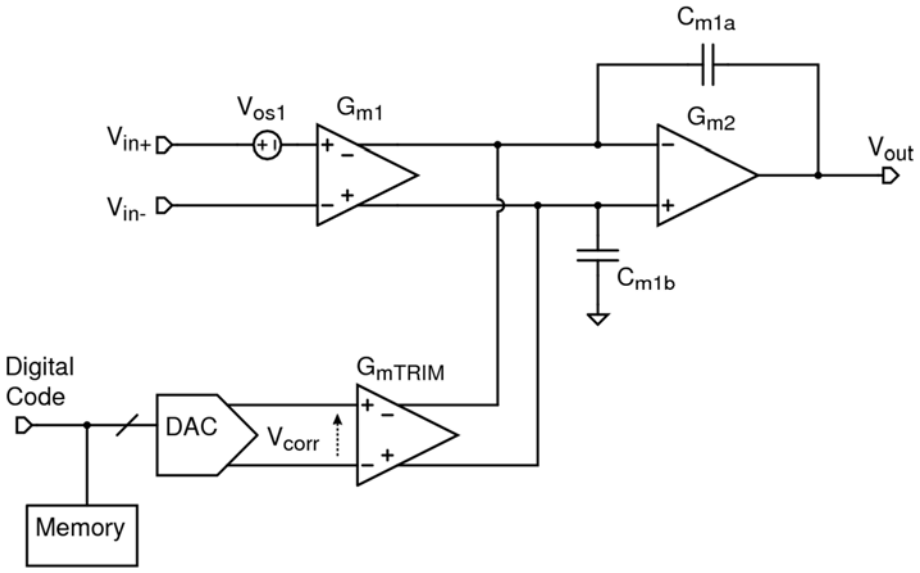

Figure 2-1: An offset trimmed op-amp

2.1 Offset Trimming

Offset trimming involves measuring the offset and then subtracting the resulting value thereafter [1,2]. Figure 2-1 shows an offset trimming implementation with a two stage op-amp. The signal path consists of input and output transconductors G_{m1} and G_{m2}, and frequency compensation capacitors C_{m1a} and C_{m1b}. Additionally, a trimming transconductor G_{mTRIM} and a DAC are implemented to subtract out an initial offset V_{os1}. At post-production test, first the correction voltage V_{corr} is set to zero, and then V_{os1} is measured externally. Next, V_{corr} is adjusted to:

$$V_{corr} = -\frac{G_{m1}}{G_{Trim}} V_{os1}, \quad (2\text{-}1)$$

through the DAC, so that G_{mTRIM} cancels the offset current of G_{m1}. Then, the corresponding digital code is stored in on-chip memory, so that V_{os1} remains corrected thereafter.

However, CMOS input differential pairs have uncorrelated absolute offset and offset drift [3]. Thus, trimming the absolute offset at one temperature does not decrease the offset drift. For this reason, most trimmed CMOS op-amps have a maximum offset drift greater than a few

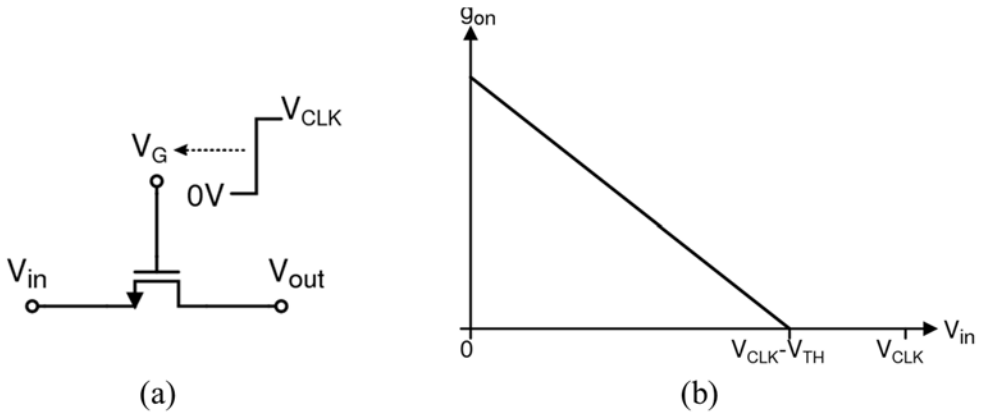

Figure 2-2: (a) An NMOS switch and (b) the on-conductance versus input voltage

µV/°C [4]. In 2011, Bolatkale reported a MOS-input op-amp achieving a 0.33µV/°C maximum offset drift by biasing the input stage at two different currents, while trimming at one temperature [3]. However, the second gain stage uses complementary bipolar devices which are not available in every CMOS process. In 2013, another MOS-input op-amp achieving a 0.8µV/°C maximum offset drift was reported [5], where its offset is corrected at the ambient temperature by a first DAC, and then its offset drift over temperature is corrected at a higher temperature by a second DAC. However, this method requires offset measurements at two different temperatures for each op-amp unit, and thus increases production cost. Bipolar input differential pairs have correlated absolute offset and offset drift, and therefore can achieve lower offset drift. For instance, the one reported in [6] achieves a 0.25µV/°C maximum offset drift. Nevertheless, as discussed in Section 1.4.1, this level of offset drift is still insufficient in some sensor applications, which require offset drifts below 0.1 µV/°C. Additionally, bipolar op-amps are ruled out in some applications due to their high input bias current (several nano-Amperes) and high manufacturing cost.

2.2 MOS Switches

2.2.1 Realization and On-Resistance

This section explains the properties of the MOS switches that are used in the dynamic offset cancellation techniques. They can be realized by either NMOS or PMOS switches, or a

combination of both (CMOS switches), depending on the targeted input voltage range [7]. Figure 2-2 (a) shows an NMOS switch with input, output, and gate terminals V_{IN}, V_{OUT}, and V_G. By driving V_G low to 0V, the switch turns off to isolate the two terminals V_{IN} and V_{OUT}. On the other hand, by driving V_G high to V_{CLK}, the switch turns on to connect the two terminals. When V_{OUT} is slightly larger or equal to V_{IN}, the on-conductance g_{on} between the two terminals is given by:

$$g_{on} = \beta \frac{W}{L}\left(V_{CLK} - V_{TH} - V_{IN}\right), \qquad (2\text{-}2)$$

where β is the transconductance parameter, V_{TH} is the threshold voltage, and W and L are the channel width and length of the NMOS, respectively [7]. As suggested by this equation, g_{on} is proportional to both W and the overdrive voltage $V_{CLK} - V_{TH} - V_{IN}$, and thus varies with V_{IN} as plotted in Figure 2-2 (b). For a targeted range of V_{IN}, the switch must be made sufficiently wide to achieve the desired on-resistance and hence the thermal noise.

2.2.2 Charge Injection

The amount of channel charge injection $q_{ch,inj}$ and clock feedthrough $q_{clk,inj}$ are proportional to the width [7]. They are given by:

$$q_{ch,inj} = WL \cdot C_{ox}\left(V_{CLK} - V_{TH} - V_{IN}\right) \qquad (2\text{-}3)$$

$$q_{clk,inj} = 2W \cdot C_{ov} \cdot V_{CLK}, \qquad (2\text{-}4)$$

where C_{ox} is the gate oxide capacitance per unit area, and C_{ov} is the gate overlap capacitance per unit of width. According to the two equations above, $q_{ch,inj}$ also increases with the overdrive voltage $V_{CLK} - V_{TH} - V_{IN}$, while $q_{clk,inj}$ increases with the clock swing V_{CLK}. Therefore, the resulting errors can depend on the supply voltage and the input voltage, which degrade the PSRR and the CMRR. This thesis uses the term *charge injection* to refer to the combination of a channel charge injection and clock feedthrough. When V_G rises, it generates a positive charge injection $q_{ch,inj} + q_{clk,inj}$ that splits into the V_{IN} and V_{OUT} terminals. When V_G drops, it generates the same amount of charge injection but with opposite polarity.

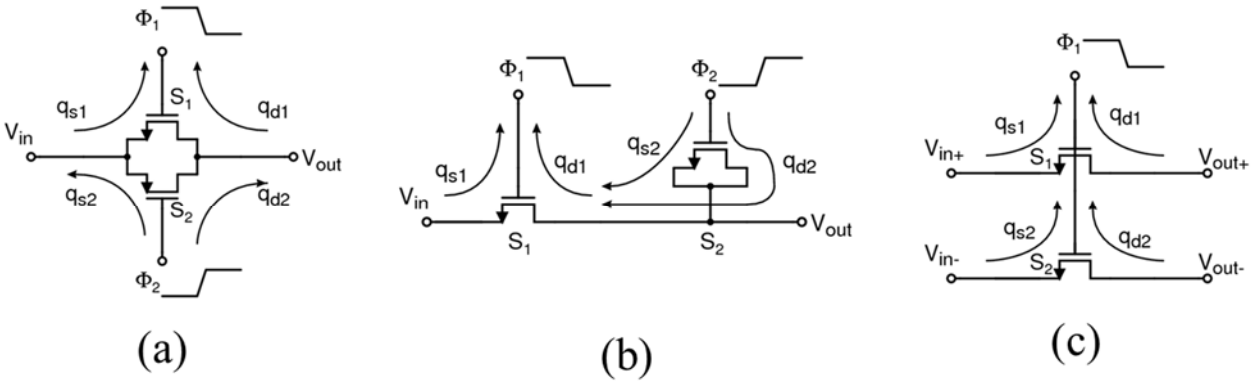

Figure 2-3: Cancellation of charge injection by (a) complementary switch, (b) dummy switch, and (c) differential circuitry

2.2.3 Cancellation of Charge Injection

To cancel the charge injection of an NMOS switch S_1, a PMOS switch S_2 can be added as shown in Figure 2-3 (a). S_1 and S_2 are driven by two complementary clocks Φ_1 and Φ_2, respectively. As a result, the switches generate charge injection of opposite polarity that cancel each other out. However, this cancellation scheme only works when V_{IN} is exactly half of V_{CLK}. Otherwise, the two switches have unequal overdrive voltages, and thus generate unequal amounts of channel charge injection.

Another way to cancel charge injection is to add an NMOS dummy switch S_2 as shown in Figure 2-3 (b). S_2 is half the size of S_1, so that its charge injections q_{s2} and q_{d2} cancel that of S_1 (q_{d1}) at the V_{OUT} node. However, the V_{IN} and V_{OUT} nodes are often driven by unequal impedances. In this case, the overall charge injection of S_1 is unequally split between these nodes, making this cancellation scheme ineffective.

The most effective solution is to use differential circuitry as shown in Figure 2-3 (c). Two NMOS switches S_1 and S_2 are driven by a single clock Φ_1, generating a nearly equal amount of charge injection. As long as the impedances are balanced differentially, the charge injection mismatch is only due to coupling capacitance mismatch, which is in the order of 1% to 10%.

As will be explained later, charge injection causes DC residual offset and transient glitches

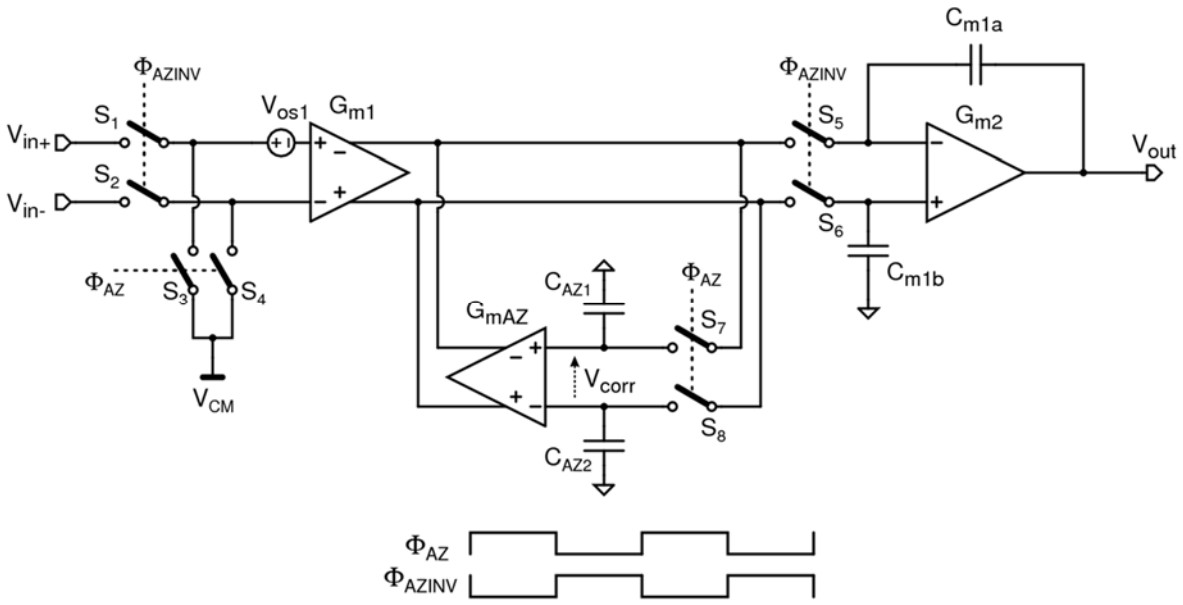

Figure 2-4: An auto-zero op-amp

in either chopper or auto-zero amplifiers. The residual offset is proportional to the amount of charge injection mismatch between differential switches. On the other hand, the magnitude of the glitches mainly depends on the absolute amount of charge injection. Therefore, both the mismatch and the absolute amount of charge injection should be minimized, while meeting the targeted on-resistance, and hence the thermal noise PSD.

2.3 Auto-Zeroing

Auto-zeroing is one of the two dynamic offset cancellation techniques available. Unlike offset trimming, it periodically measures and corrects offset, and thus reduces the offset drift and 1/*f* noise as well [7,8].

2.3.1 Principle

A block diagram of a two stage, auto-zeroed op-amp is shown in Figure 2-4. The signal path consists of input and output transconductors G_{m1} and G_{m2}. Additionally, it implements switches $S_{1\text{-}8}$, sampling capacitors $C_{AZ1,2}$, and an auto-zeroing transconductor G_{mAZ}, to measure, sample, and cancel an input offset of G_{m1} (V_{os1}). Switches $S_{1\text{-}8}$ are driven by complementary clocks Φ_{AZ} and Φ_{AZINV}, operating at the auto-zeroing frequency f_{AZ}. The op-amp is in the auto-zero phase when Φ_{AZ} is high, and is in the amplification phase when Φ_{AZINV} is high. In the auto-zero phase, the differential inputs of G_{m1} are shorted to a common-mode voltage V_{CM}, and the outputs are connected to the inputs of G_{mAZ} to form a local auto-zeroing feedback loop. Assuming the loop gain is infinite, the offset correction voltage V_{corr} is adjusted to:

$$V_{corr} = -\frac{G_{m1}}{G_{mAZ}} V_{os1}, \qquad (2\text{-}5)$$

so that G_{mAZ} cancels V_{os1}. When Φ_{AZ} drops, V_{corr} is sampled by $C_{AZ1,2}$. Next, when the amplification phase begins, the differential inputs and outputs of G_{m1} are connected to the signal path, so that the op-amp can amplify the input signals. The resulting offset is zero in principle, since V_{os1} is still cancelled by G_{mAZ} with the sampled V_{corr} in the previous auto-zero phase.

2.3.2 Residual Offset

In the circuit of Figure 2-4, residual offset is the result of several imperfections [7]. First, the

auto-zeroing feedback has a finite loop gain A_{vAZ}, resulting in an error voltage. Second, G_{mAZ} also has an input offset V_{osAZ}. Third, sampling switches S_7 and S_8 generate charge injections q_7 and q_8, when turning off. Their charge injection mismatch $\Delta q_{AZ8,7} = q_{AZ8} - q_{AZ7}$ then flows into $C_{AZ1,2}$, and produces another error voltage. As a result, the correction voltage V_{corr} includes the combined error voltage $V_{correrr}$ equaling:

$$V_{correrr} = \frac{1}{A_{vAZ}} \left(\frac{G_{m1}}{G_{mAZ}} V_{os1} \pm V_{osAZ} \right) \pm \frac{\Delta q_{8,7}}{C_{AZ1,2}} . \qquad (2\text{-}6)$$

By multiplying this error by G_{mAZ}/G_{m1}, the residual input offset $V_{os,res}$ obtained is:

$$V_{os,res} = \frac{1}{A_{vAZ}} \left(V_{os1} \pm \frac{G_{mAZ}}{G_{m1}} V_{osAZ} \right) \pm \frac{G_{mAZ}}{G_{m1}} \cdot \frac{\Delta q_{8,7}}{C_{AZ1,2}} . \qquad (2\text{-}7)$$

To minimize this residual offset, the auto-zeroing loop gain A_{zAZ} should be increased by using a cascoded topology. Additionally, $C_{AZ1,2}$ should be increased, and G_{mAZ} should be reduced with respect to G_{m1}. However, the tail current of G_{mAZ} must cover the maximum offset current of G_{m1}. Therefore, the transconductance should be reduced by employing long channel MOS devices or resistor degeneration. For instance, with A_{vAZ} = 80dB, a 10mV initial offset results in a 1µV residual offset. Additionally, with $C_{AZ1,2}$ = 10pF and G_{mAZ}/G_{m1} = 0.1, a 1fC charge injection mismatch will produce a 10µV residual offset.

2.3.3 Broadband Noise Folding

This subsection discusses the resulting noise PSD after auto-zeroing. The low frequency noise component of G_{m1} is also sampled by $C_{AZ1,2}$ along with the offset, and thus is cancelled thereafter. On the other hand, the high frequency noise component changes quickly after being sampled, and thus is not effectively cancelled. Moreover, at the offset sampling, the noise PSD above $f_{AZ}/2$ is folded back to the baseband frequencies between DC and $f_{AZ}/2$, as illustrated in Figure 2-5 [8,9]. The noise folding factor n_{fold} is defined as the ratio between the auto-zeroing loop bandwidth $f_{AZ,BW}$ and f_{AZ}, and is given by:

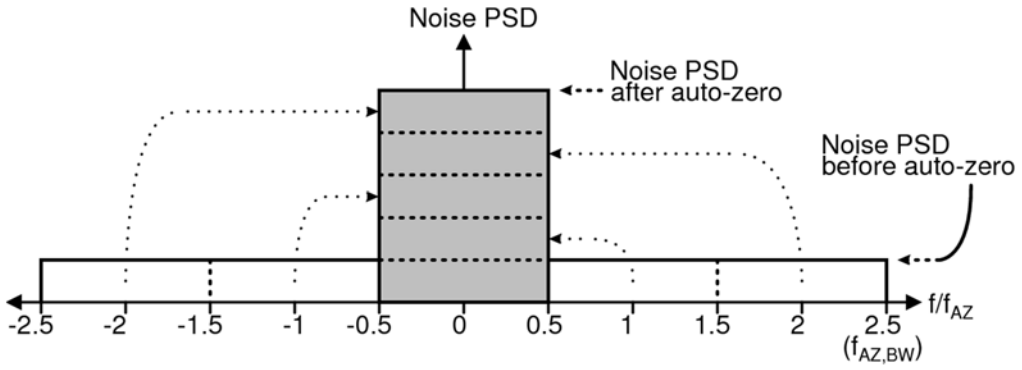

Figure 2-5: Noise folding upon auto-zero sampling

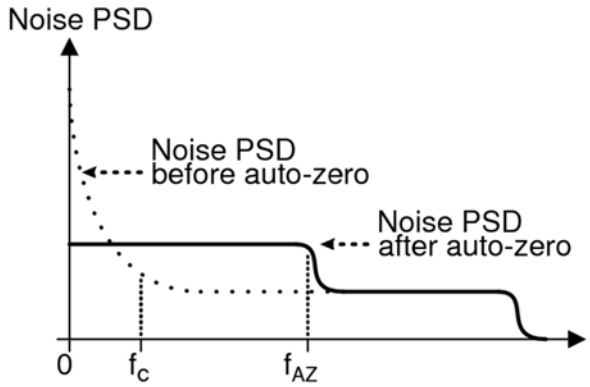

Figure 2-6: Noise PSDs before and after auto-zeroing

$$n_{fold} \equiv \frac{2 f_{AZ,BW}}{f_{AZ}} = \frac{2}{f_{AZ}} \frac{G_{mAZ}}{2\pi C_{AZ\,1,2}}. \qquad (2\text{-}8)$$

The larger n_{fold} is, the larger the resulting noise PSD is. Usually, this factor is greater than unity, since $f_{AZ,BW}$ is set higher than f_{AZ} to allow the auto-zeroing loop to settle within one auto-zero phase.

Figure 2-6 shows the typical noise PSDs before and after auto-zeroing. The $1/f$ noise is effectively reduced to a negligible level by setting f_{AZ} well above its corner frequency f_c. However, below $f_{AZ}/2$ the noise PSD is higher than the initial thermal noise floor due to the noise folding. In [10], a slow auto-zeroing loop is proposed to reduce n_{fold} below unity. Even so, the resulting noise PSD still exceeds the initial thermal noise floor by a factor of $\sqrt{2}$. Noise folding is one drawback that degrades the NEF of an auto-zeroed op-amp.

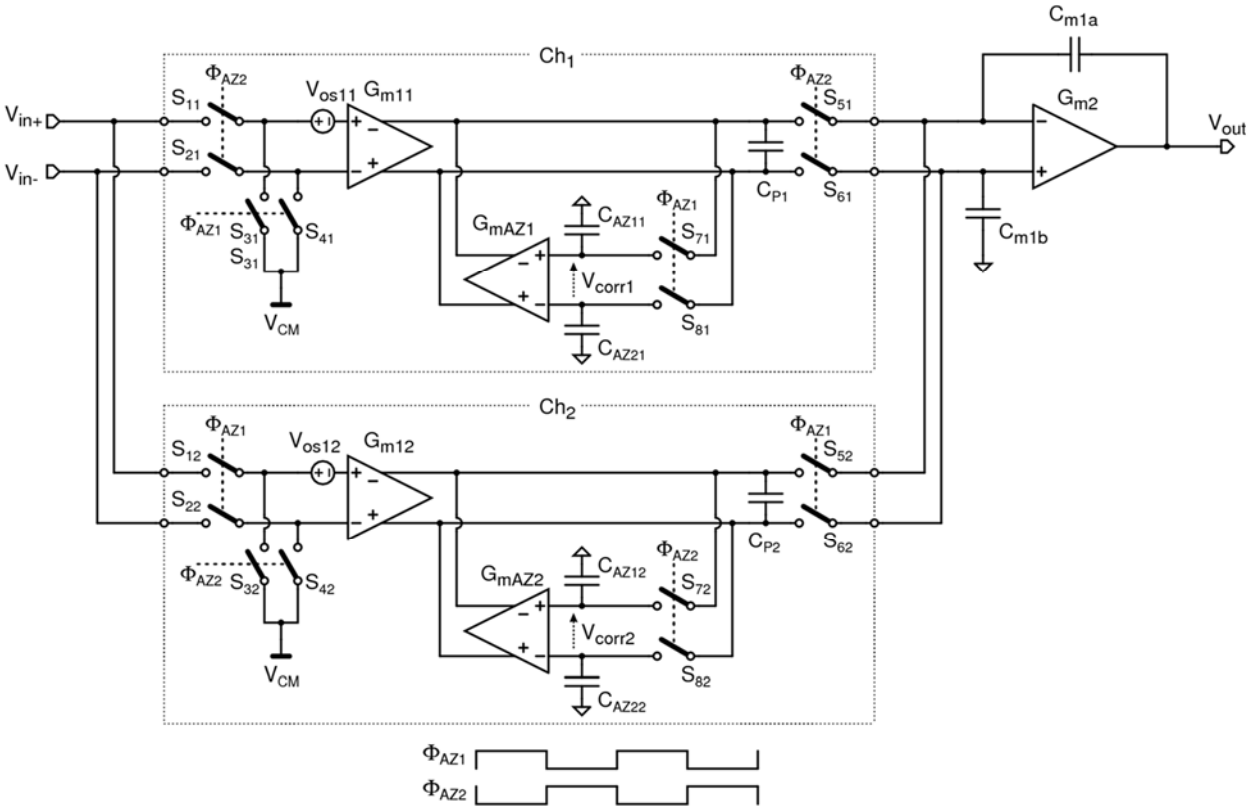

Figure 2-7: A ping-pong auto-zero op-amp

2.3.4 Ping-Pong Auto-Zeroing

Another drawback of an auto-zeroed op-amp is that it is unable to amplify signals during the auto-zero phase. This is unacceptable in many applications where input signals need to be continuously amplified. This problem can be solved by operating two identical input channels complementarily (ping-pong) [11]. Figure 2-7 shows the circuit diagram, consisting of two parallel input channels Ch_1 and Ch_2 followed by an output transconductor G_{m2}. Each channel consists of the same circuit shown in Figure 2-4, and is driven by complementary clocks Φ_{AZ1} and Φ_{AZ2}. When Φ_{AZ1} is high, Ch_1 is in the auto-zero phase while Ch_2 is in the amplification phase. In contrast, when Φ_{AZ2} is high instead, the phases are reversed. Consequently, the input signal is always amplified by either channel. However, the additional input channel consumes extra current and die area.

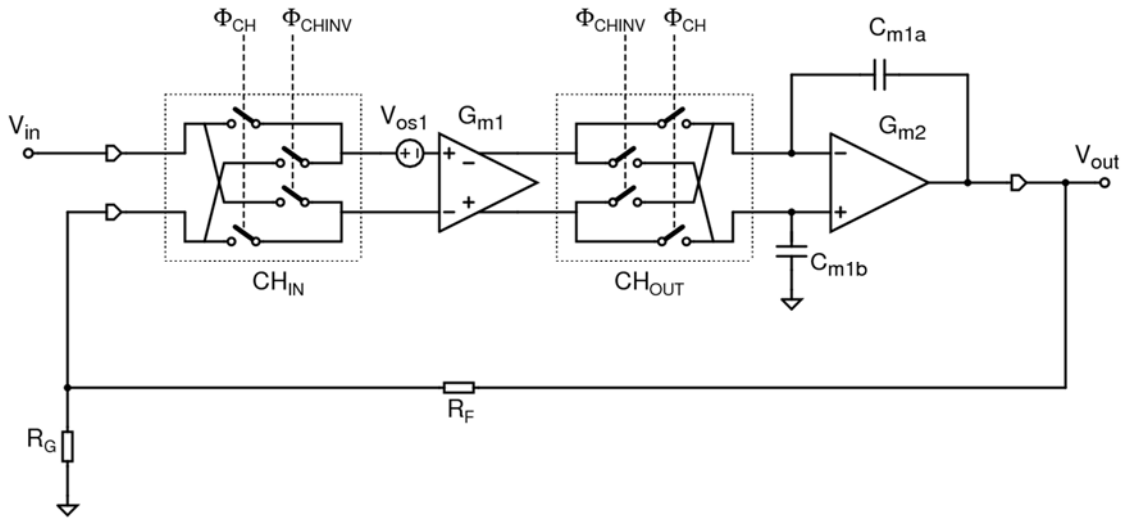

Figure 2-8: Chopper op-amp in a closed-loop

2.4 Chopping

Chopping is the other dynamic offset cancellation technique. While auto-zeroing samples and cancels offset, chopping modulates the input signal and the offset to separate them from each other in the frequency domain [8]. Since chopping neither involves sampling nor introduces noise folding, the resulting noise PSD is only slightly higher than the initial thermal noise floor [8]. Moreover, the signals are continuously amplified without requiring ping-ponging of the two channels. Therefore, chopping can achieve low offset and low noise PSD in a more power efficient manner than auto-zeroing. Since the basic principles of chopping were already presented in Chapter 1, this section will go on to discuss the various AC and DC errors caused by switching artifacts.

2.4.1 Up-Modulated Ripple

Figure 2-8 shows a two stage chopper op-amp with external gain setting resistors R_F and R_G. As explained in Section 1.3, the initial offset of G_{m1} (V_{os1}) is up-modulated and becomes output

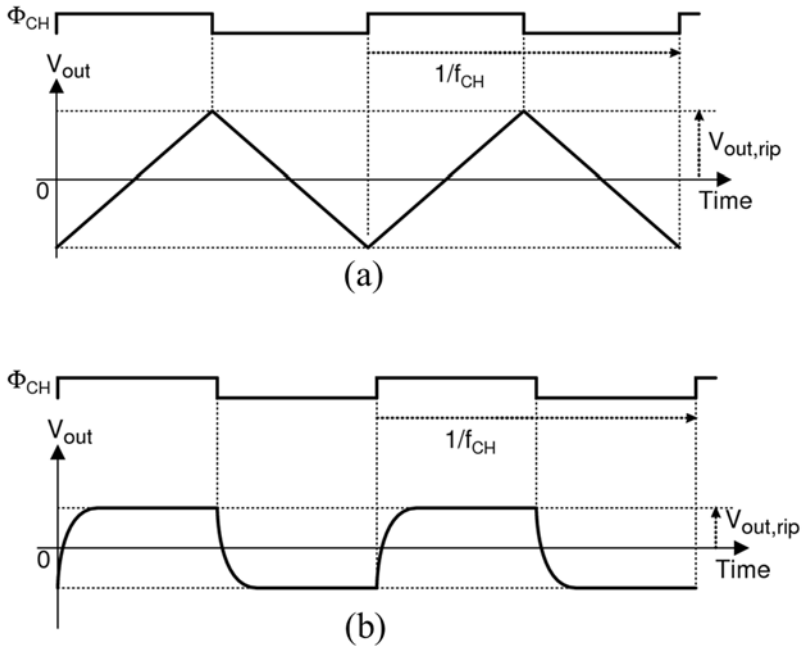

Figure 2-9: Output ripple (a) without feedback effect and (b) with feedback effect

ripple [12]. The amplitude of this ripple is affected by the closed-loop gain A_{CL} and the closed-loop bandwidth f_{CL} given by:

$$A_{CL} \approx 1 + \frac{R_F}{R_G} \qquad (2\text{-}9)$$

$$f_{CL} = \frac{1}{A_{CL}} \frac{G_{m1}}{2\pi C_{m1a,b}}. \qquad (2\text{-}10)$$

When the chopping frequency f_{CH} is well above f_{CL}, the ripple is produced in an open-loop manner with no feedback effect: V_{os1} is converted into a current by G_{m1}, up-modulated by CHOUT, and integrated over $C_{m1a,b}$. This results in a triangular output ripple as shown in Figure 2-9 (a); the peak amplitude $V_{out,rip}$ is given by:

$$V_{out,rip} = \frac{G_{m1}}{4 f_{CH} C_{m1a,b}} V_{os1}. \qquad (2\text{-}11)$$

On the other hand, when f_{CH} is well below f_{CL}, the output ripple is produced in a closed-loop

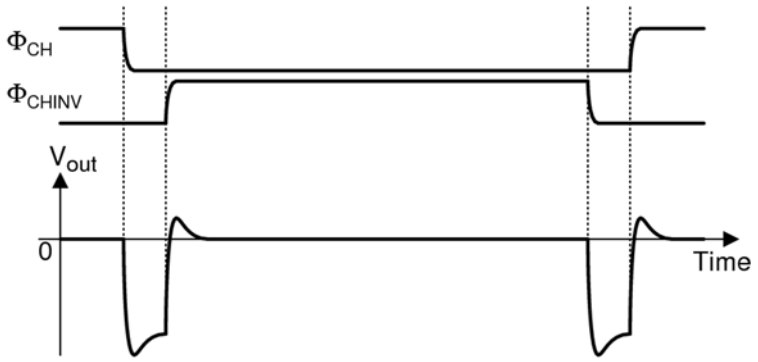

Figure 2-10: Output glitch due to input charge injection

manner with the feedback effect. Thus, it settles to two constant voltages after every clock transition, as shown in Figure 2-9 (b). The amplitude $V_{out,rip}$ is then given by:

$$V_{out,rip} = A_{CL} V_{os1} . \qquad (2\text{-}12)$$

For instance, with G_{m1} = 100µS, V_{os1} = 1mV, f_{CH} = 100kHz, $C_{m1a,b}$ = 10pF, and A_{CL} = 100, $V_{out,rip}$ is 25mV according to (2-11). When A_{CL} is reduced to 10 while the other parameters remain the same, $V_{out,rip}$ becomes 10mV according to (2-12). In either case, the amplitude of the ripple is quite large, and therefore needs to be attenuated in most applications.

2.4.2 Glitches

The transient waveforms in a chopper amplifier have been drawn in Figure 2-9 (a) and (b), where the effect of charge injection is neglected. In fact, as illustrated in Figure 2-10, charge injection of the input switches causes output glitches [13,14]. First, Φ_{CH} drops, injecting negative charge on the differential input pins. Soon thereafter, Φ_{CHINV} rises, injecting almost the same amount of charges but with positive polarity. Ideally, these negative and positive charges cancel out instantaneously at each input pin, if the transitions of the two clocks occur at the exact same time. In practice, however, there must be some dead time between the two clocks, in order not to short the differential input pins with the switches. This generates short pulses on both input pins, resulting in an output glitch. Since this occurs in the order of a nanosecond, the op-amp is not fast enough to suppress this glitch via its feedback loop. The glitch amplitude depends on the

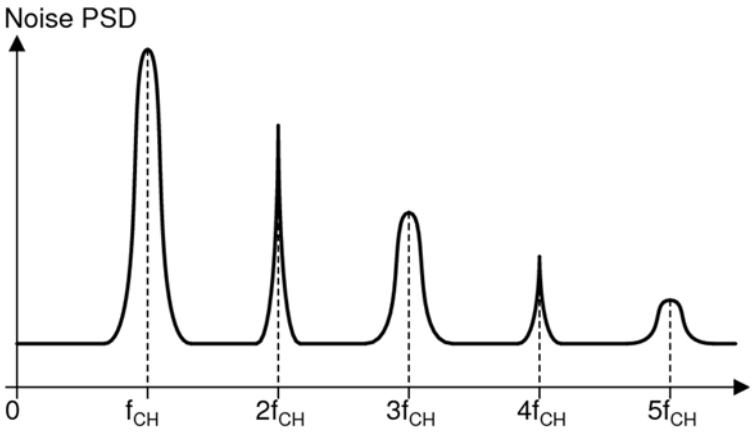

Figure 2-11: Output noise PSD of a chopper op-amp

source impedances, the dead time, and the amount of charge injection. Similarly, after a half chopping period, Φ_{CHINV} drops and Φ_{CH} rises, resulting in another glitch.

Figure 2-11 shows the output noise PSD of a chopper op-amp, taking both the ripple and the glitches into account. The PSD increases at the odd harmonics of the chopping frequency f_{CH} due to the up-modulated ripple, and at the even harmonics of f_{CH} due to the glitches. The noise spectra peak usually need to be attenuated by low-pass filters, which increases cost and limits the usable signal bandwidth [15]. Therefore, manufactures prefer chopper op-amps that have lower noise spectra peak at higher frequencies, so as to relax the requirement of the low-pass filters. On the other hand, a higher f_{CH} will produce higher residual offset and input bias current, as will be explained in the next subsection.

2.4.3 Input Bias Current and Residual Offset

Charge injection mismatch causes DC errors such as residual offset and input bias current [12,16]. Close inspection shows that only the charge injection mismatch in the signal path between the two choppers is down-modulated, and thus contributes to the DC errors. In contrast, the charge injection in the signal path outside the two choppers does not contribute to the DC errors, and therefore is neglected in this subsection for simplicity.

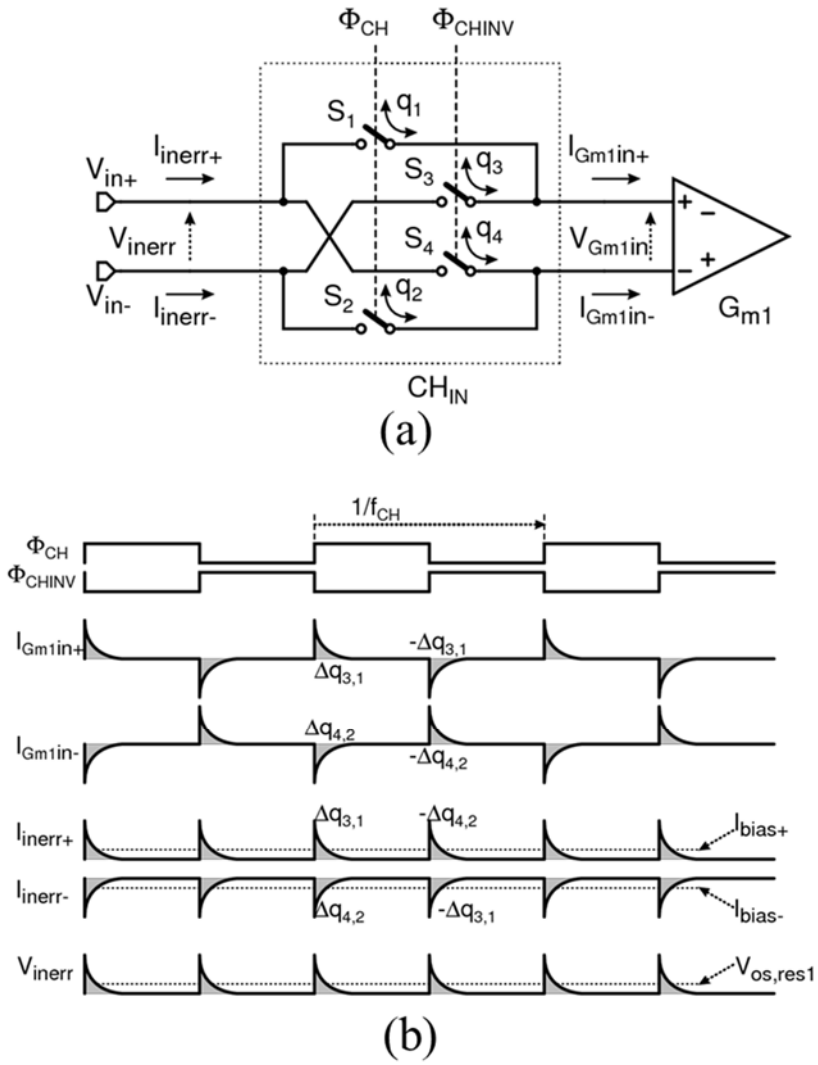

Figure 2-12: Input bias current due to input chopping: (a) circuit diagram; (b) transient waveforms

The charge injection mismatch generated by the input chopper CH_{IN} is down-modulated and flows back to the amplifier's input pins. As shown in Figure 2-12 (a), CH_{IN} consists of four switches $S_{1\text{-}4}$, which inject charges $q_{1\text{-}4}$ during every clock transition. Figure 2-12 (b) shows the resulting transient waveforms along with clock timings Φ_{CH} and Φ_{CHINV}. Ideally, q_3 and q_1 cancel each other out at the input of G_{m1}, as do q_4 and q_2. However, charge injection mismatches $\Delta q_{3,1} = q_3 - q_1$ and $\Delta q_{4,2} = q_4 - q_2$ cause current glitches I_{Gm1in+} and I_{Gm1in-}, respectively. These AC current glitches are down-modulated by CH_{IN}, and flow back to the differential input pins V_{in+}

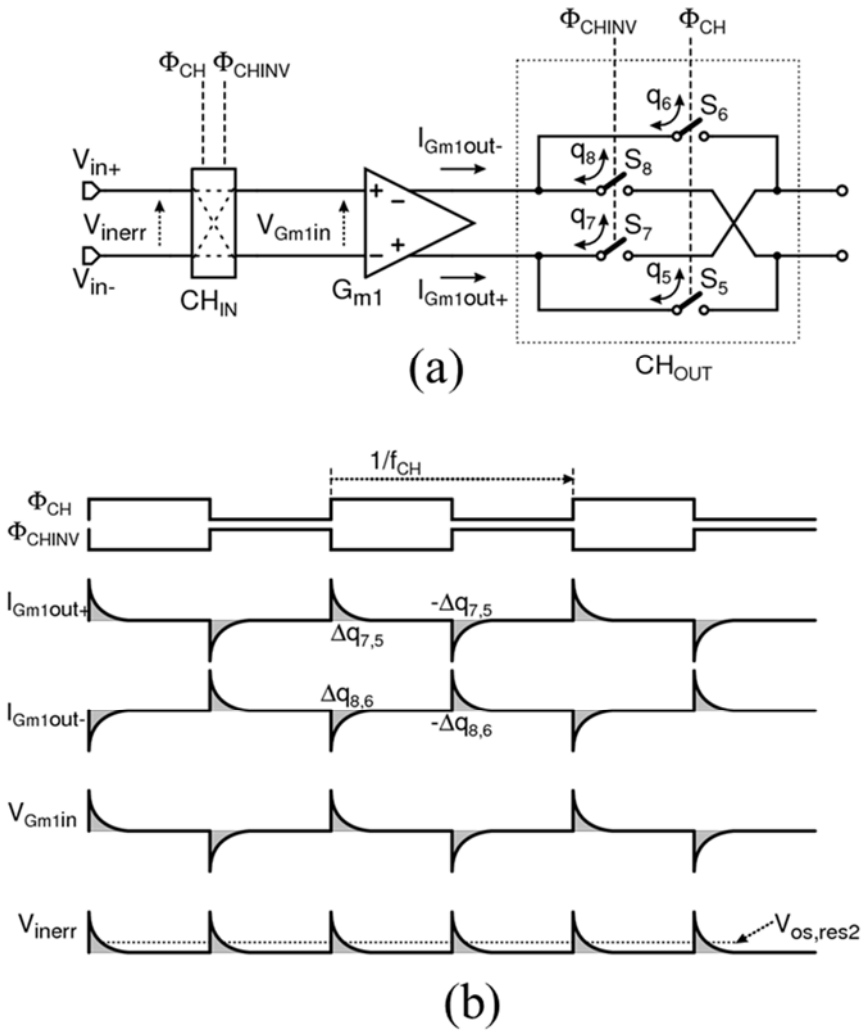

Figure 2-13: Residual offset due to output chopping: (a) circuit diagram; (b) transient waveforms

and V_{in-}. The resulting input error currents I_{inerr+} and I_{inerr-} include the DC bias components I_{bias+} and I_{bias-} given by:

$$I_{bias+} = f_{CH}\left(\Delta q_{3,1} - \Delta q_{4,2}\right) \qquad (2\text{-}13)$$

$$I_{bias-} = -f_{CH}\left(\Delta q_{3,1} - \Delta q_{4,2}\right). \qquad (2\text{-}14)$$

Moreover, in conjunction with the on-resistance of each switch R_{on}, these input bias currents cause a residual input offset voltage $V_{os,res1}$ equal to:

$$V_{os,res1} = 2 f_{CH}\left(\Delta q_{3,1} - \Delta q_{4,2}\right)R_{on}. \qquad (2\text{-}15)$$

Additionally, source resistances driving the input pins should be added in series with R_{on} in the equation above, which will further increase $V_{os,res1}$. For instance, with f_{CH} = 100kHz and R_{on} = 1kΩ, a charge injection mismatch $\Delta q_{3,1} - \Delta q_{4,2}$ = 10fF will result in I_{bias+} = 1nA, I_{bias-} = –1nA, and $V_{os,res1}$ = 2μV. Furthermore, when each input pin is driven by a 10kΩ source resistance, $V_{os,res1}$ increases to 22μV.

The charge injection mismatch of the output chopper CH_{OUT} also causes residual offset. As shown in Figure 2-13 (a), CH_{OUT} consists of four switches $S_{5\text{-}8}$, which inject charges $q_{5\text{-}8}$. The charge injection mismatches $\Delta q_{7,5} = q_7 - q_5$ and $\Delta q_{8,6} = q_8 - q_6$ result in current glitches $I_{Gm1out+}$ and $I_{Gm1out-}$, respectively, as shown in Figure 2-13 (b). The input transconductor G_{m1} absorbs these current glitches, resulting in voltage glitches V_{Gm1in} at its input. The input chopper CH_{IN} then down-modulates V_{Gm1in}, so that the resulting input error voltage V_{inerr} includes a residual DC offset $V_{os,res2}$ equal to:

$$V_{os,res2} = \frac{2 f_{CH} \left(\Delta q_{5,6} - \Delta q_{7,8} \right)}{G_{m1}}. \qquad (2\text{-}16)$$

As indicated in the equations, these DC errors are proportional to the chopping frequency f_{CH}. Furthermore, they indicate that wider switches, which suffer from larger charge injection mismatch, cause larger DC errors.

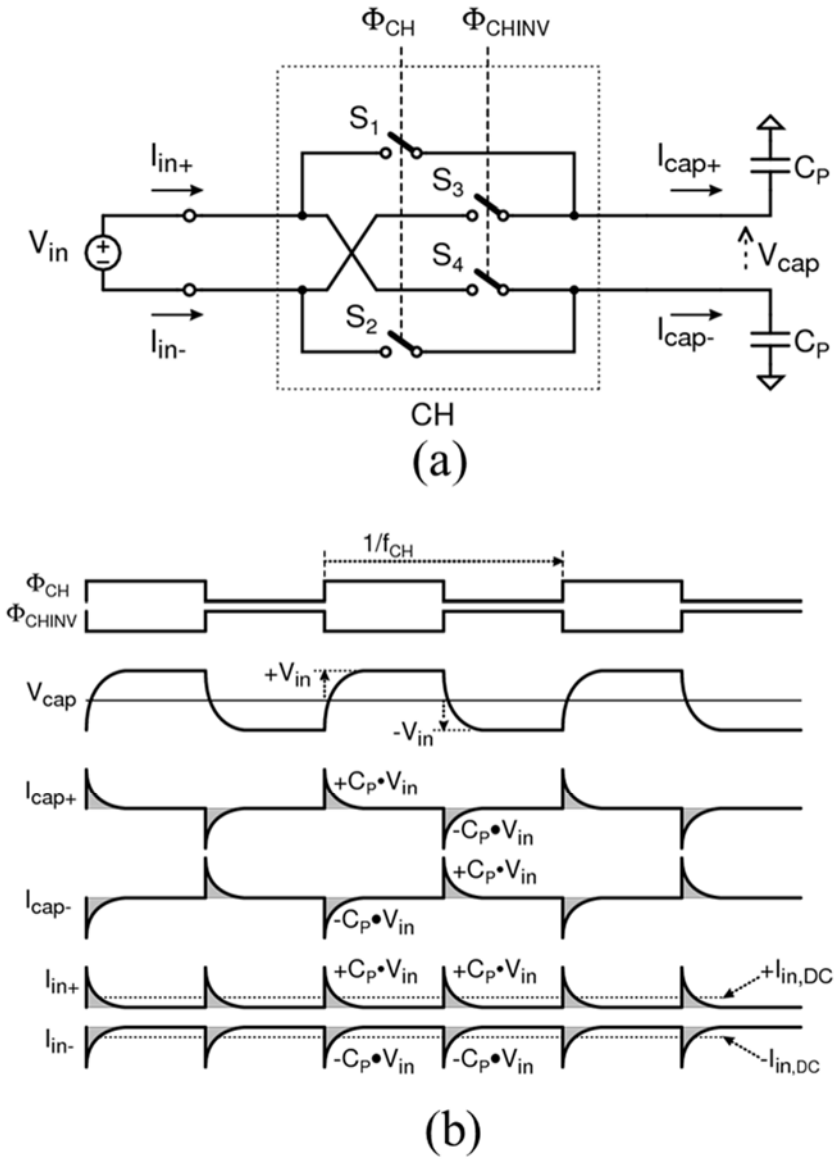

Figure 2-14: Dynamic switching conductance due to chopping: (a) circuit diagram; (b) transient waveforms

2.4.4 Dynamic Switching Conductance

Chopping also generates a dynamic conductance in conjunction with any capacitances at the switching nodes [16]. This is illustrated in Figure 2-14 (a), where a differential input voltage V_{in} is applied to a chopper CH. As shown in Figure 2-14 (b), V_{in} is up-modulated and results in an AC voltage output V_{cap}. Consequently, two capacitances C_P are charged every clock transition, which causes current glitches I_{cap+} and I_{cap-}. These current glitches are down-modulated by CH,

and become input currents I_{in+} and I_{in-}, including DC component $I_{in,DC}$. The dynamic switching conductance G_{switch} is defined as:

$$G_{switch} \equiv \frac{I_{DC,in}}{V_{in}} = 2 f_{CH} C_P \,. \qquad (2\text{-}17)$$

Because of this effect, a chopper amplifier has a finite differential input conductance. However, this is usually not a problem for an op-amp amplifying DC or low frequency signals, since the differential input voltage is kept small by feedback. However, an instrumentation amplifier can have a large differential input voltage, and so should have a sufficiently low differential input conductance.

Additionally, the DC gain of the input transconductor G_{m1} decreases due to the switching conductance associated with the output chopper. This not only reduces the open-loop gain of the op-amp, but it also increases the residual offset contributed by a subsequent gain stage. For instance, with an 80dB gain of G_{m1}, a subsequent gain stage with an input offset of 10mV will give rise to a 1μV residual input offset.

2.4.5 Summary of the Errors

As discussed earlier in this section, the switching artifacts due to chopping cause various DC and AC errors. The up-modulated ripple and the glitches caused by charge injection show up as noise spectra peak at the harmonics of the chopping frequency f_{CH}. Moreover, down-modulated charge injection mismatch causes DC errors such as residual offset and input bias currents.

Design parameters, such as the chopping frequency f_{CH} and the size of the switches, affect these AC and DC errors, and therefore should be properly chosen for a given design target. To sufficiently reduce the $1/f$ noise, f_{CH} should be set above its corner frequency. For applications requiring a wider signal bandwidth, f_{CH} should be further increased to relax the requirements of the low-pass filters. However, this increases the residual offset and input bias current, and decreases the effective DC gain of the input transconductor. Moreover, the variation of f_{CH} over temperature causes residual offset drift.

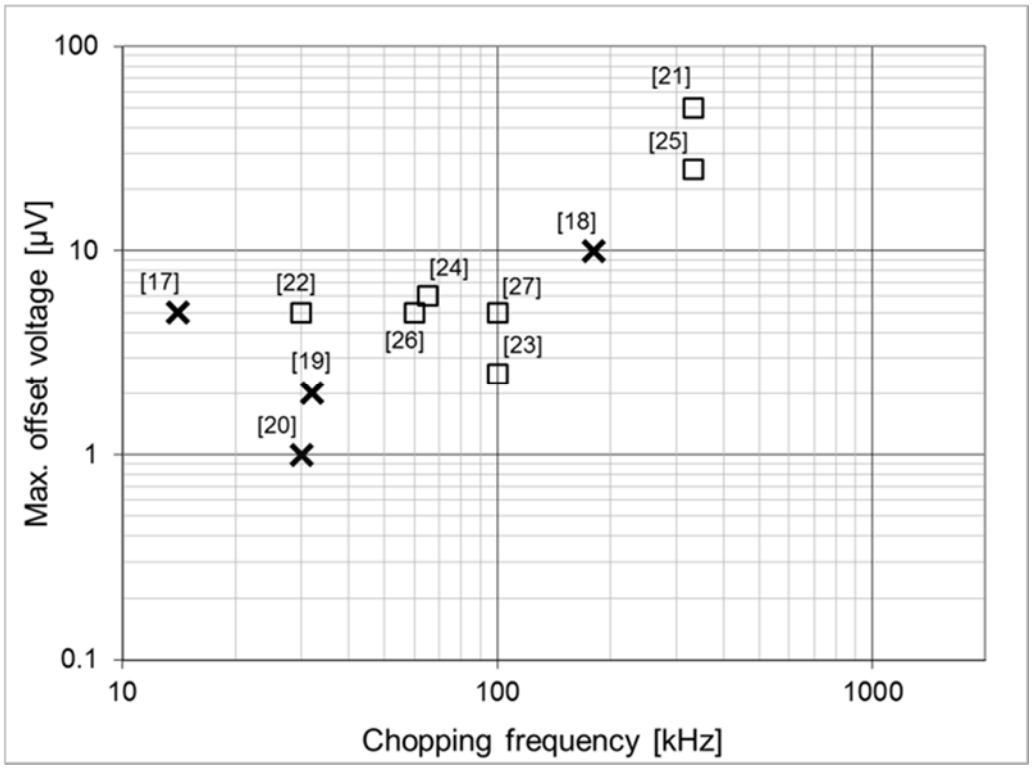

Figure 2-15: Maximum offset versus chopping frequency of previous chopper op-amps

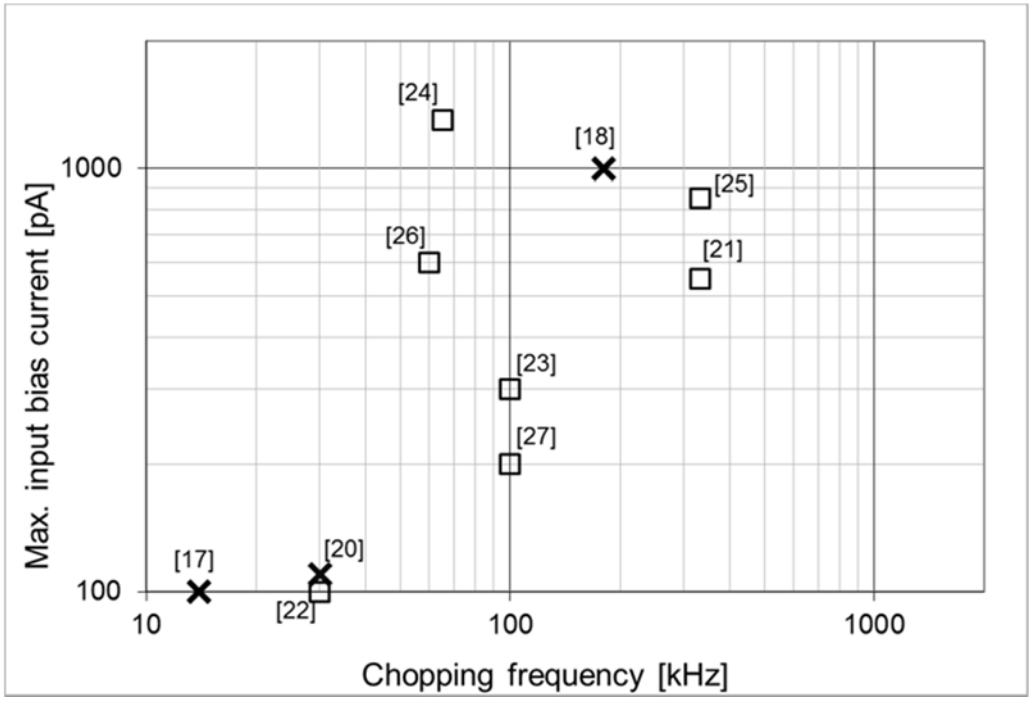

Figure 2-16: Maximum input bias current versus chopping frequency of previous chopper op-amps

The input switches must be made sufficiently wide to reduce the on-resistance for a targeted thermal noise PSD. However, this also increases their charge injection mismatch, and thus increases the residual offset and input bias current. When the chopping clocks have a fixed amplitude, the amount of charge injection changes with the input common-mode voltage. Consequently, the residual offset and input bias current also change with the input common-mode voltage, which degrades the CMRR and the common-mode input impedance. Moreover, wider switches produce larger glitches and hence larger noise spectra peak.

In summary, chopper op-amp design involves trade-offs between the DC error, the chopping frequency, and the noise PSD. Figure 2-15 shows the maximum offset versus the chopping frequency of previous chopper op-amps that have less than 20nV/√Hz noise PSD [17-27]. Note that the specifications derived from conferences or journals are marked by crosses, while those derived from the datasheets of commercial products are marked by squares. It can be seen that their offset tends to increase with chopping frequency, and is typically greater than 10μV for chopping frequencies above 100kHz. Figure 2-16 shows the maximum input bias current versus the chopping frequency. Like offset, input bias current tends to increase with chopping frequency, and is higher than 500pA for chopping frequencies above 200kHz.

Table 2-1: Comparison of the three low offset techniques

	Basic	Trim	Auto-zero	Chopper
Offset	High	Low	Very low	Very low
Offset drift over temperature	High	Medium	Very low	Very low
Offset change with common mode	High	Medium	Very low	Very low
1/f noise	High	High	Very low	Very low
Continuous-time operation	Yes	Yes	* No	Yes
Noise PSD in the base band	High	High	Medium	Low
Noise PSD at fCLK	Low	Low	Low	High
Noise PSD at 2fCLK	Low	Low	Medium	Medium

* Requires ping-pong architecture to provide continuous operation

2.5 Comparison of the Techniques

This chapter has discussed three offset cancellation techniques: offset trimming, auto-zeroing, and chopping. Table 2-1 compares the three techniques with a basic CMOS op-amp that does not use an offset cancellation technique. Offset trimming only corrects offset at post-production test, and thus still results in high offset drift and 1/*f* noise.

Auto-zeroing and chopping both correct offset periodically, and therefore can achieve both very low offset that is stable over temperature, as well as very low 1/*f* noise. However, auto-zeroing introduces dead time, during which the offset is sampled and the op-amp is unavailable for signal amplification. To solve this problem, two input channels with ping-pong operation are required. Moreover, the offset sampling introduces high frequency noise folding, and thus results in higher in-band noise PSD than the initial thermal noise floor.

On the other hand, chopping is a frequency modulation technique that results in continuous-time amplification without requiring an extra input channel. The resulting in-band noise PSD is only slightly higher than the initial thermal noise floor. Therefore, this technique can achieve a low offset and low noise PSD op-amp in a more power efficient manner than auto-zeroing. The next chapter discusses the many techniques reported in recent years to reduce the residual offset and up-modulated ripple of chopper op-amps and instrumentation amplifiers.

2.6 References

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Chapter 3

Methods of Reducing Chopper Switching Artifacts

The previous chapter discussed the various DC and AC errors caused by switching artifacts in chopper amplifiers. This chapter reviews the literature and presents various techniques to reduce these errors.

3.1 Residual Offset Reduction Techniques

As explained in Section 2.4.3, the input and output choppers of a chopper amplifier cause voltage and current glitches due to charge injection mismatch. These glitches can therefore be down-modulated, producing residual offset and input bias current. This section discusses three known techniques to reduce these DC errors. The first two techniques attenuate the glitches that would otherwise be down-modulated to DC. The third technique employs a combination of fast and slow chopping, in such a way that the slow chopping up-modulates the DC errors produced by the fast chopping.

3.1.1 Filtering the Glitches

According to the explanation in Section 2.4.3, the charge injection mismatch of CH_{IN} may cause a residual input offset $V_{os,res1}$ in conjunction with the on-resistance of the switches. In fact, the charge injection mismatch first causes voltage glitches at the input of input transconductor G_{m1}. These glitches are then amplified by G_{m1} and down-modulated by CH_{OUT} to become residual offset. Therefore, residual offset can be reduced by attenuating the glitches before they are down-modulated.

In 1997, Menolfi proposed a band-pass filtering technique to attenuate the glitches [1,2]. A block diagram of the proposed instrumentation amplifier (IA) is shown in Figure 3-1 [2]. The input signal V_{in} is up-modulated to a chopping frequency f_{CH} and is amplified by a pre-amplifier A_1. Consequently, the output of A_1 ($V_{A1,out}$) contains glitches caused by an input chopper CH_{IN} along with the up-modulated signal. A band-pass filter (BPF) attenuates most of the energy in the wideband glitches that would otherwise become residual offset. The center frequency f_{BPF} of the BPF is tuned at f_{CH}, so that the up-modulated signal can pass through it. With $f_{CH} = f_{BPF} = 6$kHz, the proposed IA achieved a 600nV offset (mean + 1σ), a 150dB CMRR, and an 8.5nV/√Hz noise PSD. Although the BPF required a relatively relaxed quality factor of $Q = 5$, 0.5% matching was required between f_{BPF} and f_{CH} [2]. To meet these requirements, the oscillator and the BPF employ identical active integrators, which consume extra current and die area.

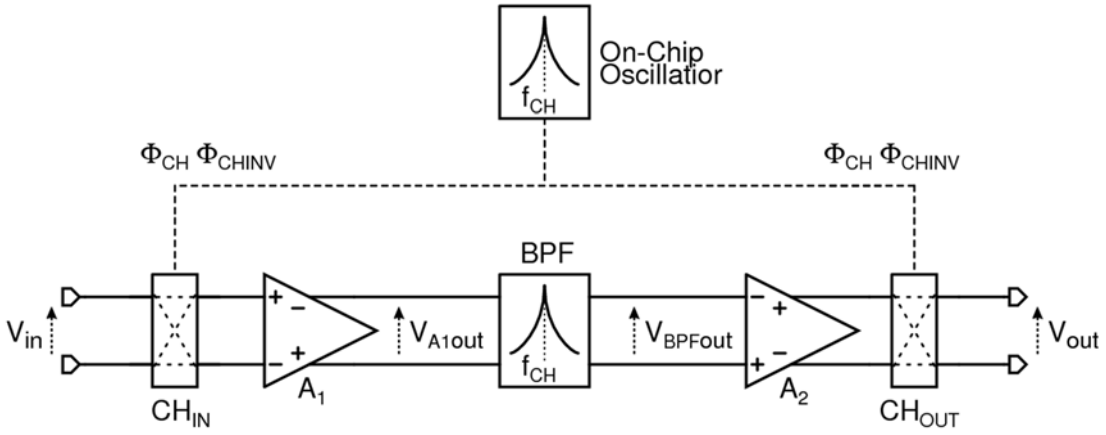

Figure 3-1: Glitch filtering with a band-pass filter

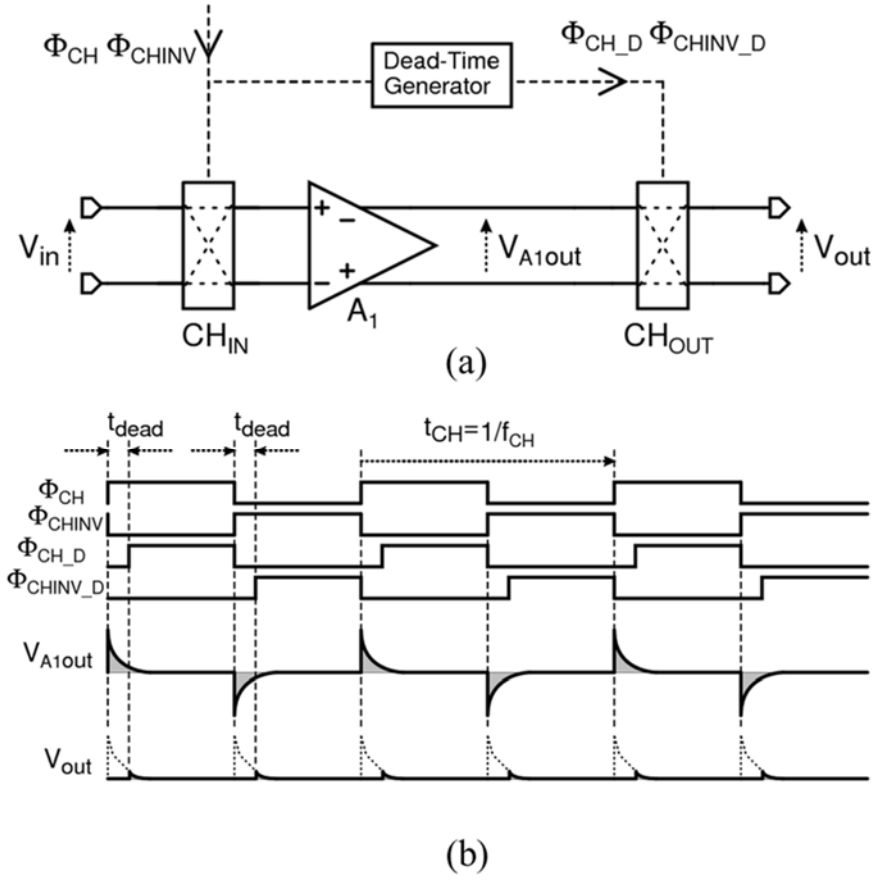

Figure 3-2: Dead-timed down-modulation: (a) circuit diagram; (b) transient waveforms

3.1.2 Dead-Timed Down-Modulation

Later, in 2001, Menolfi proposed another residual offset reduction technique with a much simpler implementation as shown in Figure 3-2 (a) [3]. The timing diagram is given in Figure 3-2 (b), which shows that there is a dead time t_{dead} between the output chopping clocks Φ_{CH_D} and Φ_{CHINV_D}. As a result, the output V_{out} is connected to V_{A1out} after the glitches caused by the input chopping settle. This reduces the glitches at V_{out} and consequently reduces the residual offset. The dead time can be easily implemented with clock delay circuits without consuming quiescent current. With a 5.6kHz chopping frequency, this IA achieved a 200nV offset as well as a 150dB CMRR and a 6.5nV/√Hz noise PSD.

However, this is no longer a true continuous-time amplifier, since it is unable to amplify the input signal during the dead time. So the dead time decreases the effective gain, and thus increases the input-referred noise. To mitigate this problem, t_{CH} needs to be sufficiently longer than t_{dead}, since the resulting effective gain is proportional to $t_{CH}/(t_{CH}+2t_{dead})$, where t_{CH} is the one chopping period. On the other hand, the dead time also needs to be long enough to allow the glitches settle, thus limiting the maximum chopping frequency.

3.1.3 Nested Chopping

Nested chopping, proposed by Bakker in 2000, reduces the residual offset in a different way [4]. Figure 3-3 (a) shows the block diagram that employs two chopping frequencies. An inner set of input and output choppers $CH_{ININner}$ and $CH_{OUTinner}$ are driven by a high chopping frequency f_{CHhigh}. While an outer set of input and output choppers $CH_{INouter}$ and $CH_{OUTouter}$ are driven by a low chopping frequency f_{CHlow}. Figure 3-3 (b) shows the expected transient waveforms along with the clock timings. In this example, $f_{CH,high}$ is set four times higher than $f_{CH,low}$, and only the glitches generated by the inner chopping are shown for simplicity.

First, as explained in Section 2.4.3, charge injection mismatch in $CH_{ININner}$ causes voltage glitches V_{inA1} at the input of amplifier A_1. These glitches are down-modulated by $CH_{OUTinner}$ and thus produce DC error $V_{outinner}$. Then, the outer chopper $CH_{OUTouter}$ up-modulates $V_{outinner}$ again,

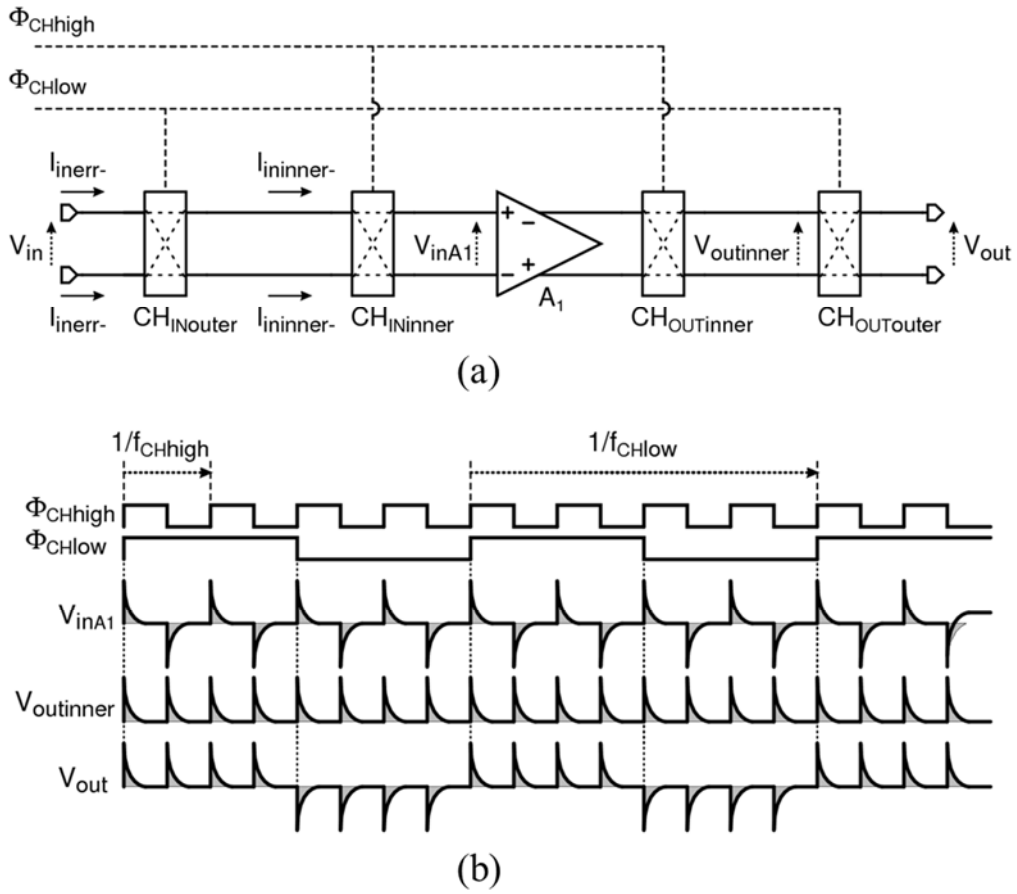

Figure 3-3: Nested chopping: (a) circuit diagram; (b) transient waveforms

so that an output V_{out} contains no residual offset. Similarly, the input bias currents caused by $CH_{ININner}$ are up-modulated by $CH_{INOuter}$, resulting in no DC input bias currents at the overall input pins.

Through the operation of two output choppers, the offset and 1/*f* noise of A_1 are up-modulated to two frequencies $f_{CHhigh} \pm f_{CHlow}$. Therefore, f_{CHlow} can be set even below the 1/*f* noise corner frequency, while almost eliminating the 1/*f* noise from the baseband. Consequently, the residual offset caused by the outer chopper can be reduced to a very low level. In summary, the nested chopping technique utilizes two separate chopping frequencies, so that the 1/*f* noise can be mitigated by a high f_{CHhigh} while the residual offset can be determined by a low f_{CHlow}. With $f_{CH,low}$ = 2kHz and $f_{CH,high}$ = 16kHz, the proposed op-amp achieves a 100nV offset and a 27nV/√Hz noise PSD [4].

In 2005, van der Meer reported a Hall sensor read-out IC employing nested chopping, where the output outer chopper is implemented in the ADC [5]. With $f_{CH,low}$ = 10Hz and $f_{CH,high}$ = 12.5kHz, it achieved a 20nV/√Hz noise PSD and less than 50nV offset.

However, the outer chopper creates spectral peaks at f_{CHlow} and its harmonics, which limits the usable signal bandwidth. Another drawback is that to achieve a targeted noise PSD, wider switches must be used, since the switches used for low frequency chopping are in series with those used for high frequency chopping. The two sets of switches cannot be merged because a separate set of switches is needed to up-modulate the glitches generated by the inner choppers.

3.2 Ripple Reduction Techniques

This section discusses seven techniques to reduce up-modulated ripple. The first three involve filtering, while the following four operate by reducing the initial offset that would otherwise become up-modulated ripple.

3.2.1 Multi-Path Chopper Offset Stabilization

As suggested by Equation (2-11), the up-modulated ripple of a two-stage amplifier can be attenuated by increasing the size of the frequency compensation capacitors. However, this method increases the die size, and decreases the signal bandwidth of the op-amp. The ripple can be attenuated in a more area-efficient manner by a higher order low-pass filter. Additionally, the cutoff frequency of the low-pass filter can be set separately from the signal bandwidth by employing a multi-path op-amp architecture. These ideas were proposed by Witte in 2006 [6], the simplified op-amp block diagram of which is shown in Figure 3-4. This multi-path op-amp consists of a low frequency path (LFP) and a high frequency path (HFP) in parallel. The LFP further consists of the input transconductor G_{m1} and the subsequent three transconductors G_{m2-4}, whereas the HFP consists of the other input transconductor G_{m5} and shares G_{m4} with the LFP.

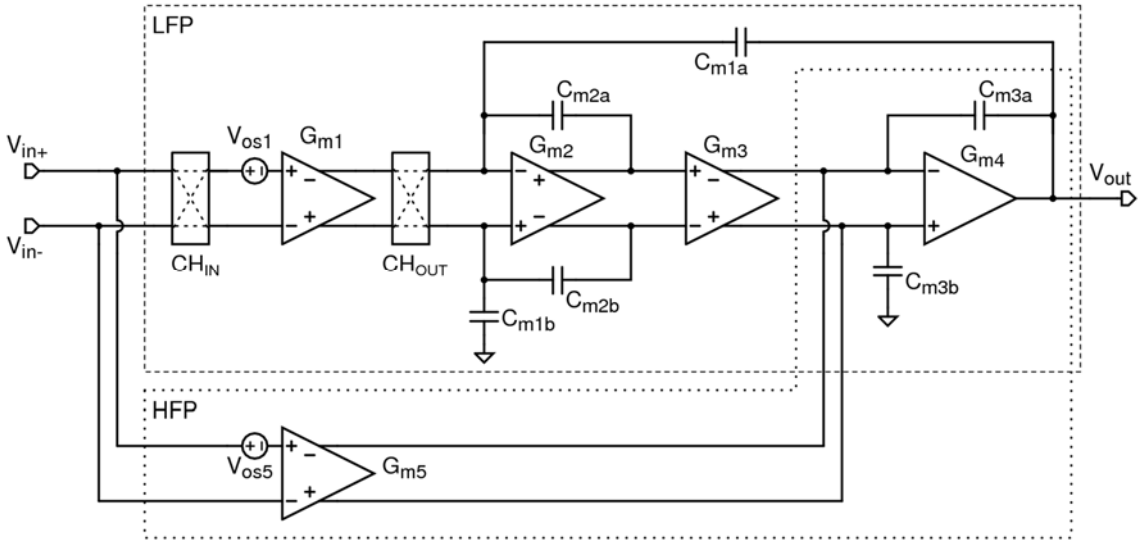

Figure 3-4: Multi-path chopper offset stabilized op-amp

The LFP dominates the low frequency performance of the overall op-amp, and G_{m1} is chopped to achieve low offset. The up-modulated input offset V_{os1} is filtered by two integrators built around G_{m2} and G_{m4}. Because the chopping frequency f_{CH} is set well below the closed-loop bandwidth f_{CL} in this work, the output ripple is produced in a closed-loop manner and the amplitude $V_{out,rip}$ is given by:

$$V_{out,rip} = \frac{G_{m1}}{2 f_{CH} C_{m2a,b}} \cdot \frac{G_{m3}}{G_{m5}} A_{CL} V_{os1}, \qquad (3\text{-}1)$$

where A_{CL} is the closed-loop gain set by the external resistors. Compared to Equation (2-12) where only one integrator is employed, more ripple attenuation is obtained. $V_{out,rip}$ can be reduced by adjusting parameters in the LFP such as G_{m1}, G_{m3}, and $C_{m2a,b}$. On the other hand, the unity gain bandwidth is set by the HFP and is equal to $G_{m5}/(2\pi C_{m3a,b})$.

The offset of the HFP (V_{os5}) is offset stabilized by the LFP. However, in conjunction with the finite voltage gain of the LFP, it produces a residual offset $V_{os,res}$ given by:

$$V_{os,res} = \frac{A_{v5}}{A_{v1} A_{v2} A_{v3}} V_{os5}, \qquad (3\text{-}2)$$

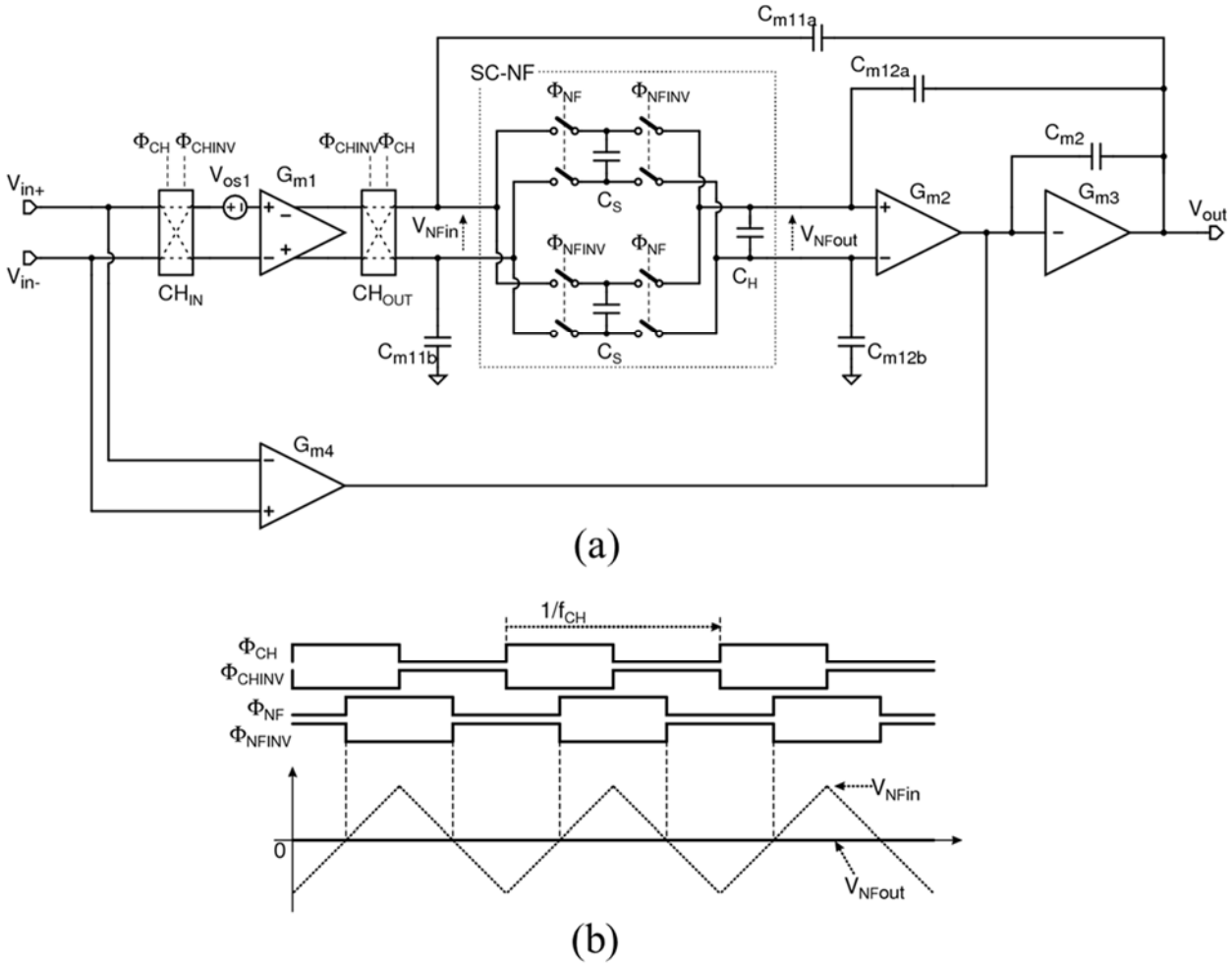

Figure 3-5: Chopper op-amp employing a SC notch-filter: (a) circuit diagram; (b) timing diagram

where $A_{v1,2,3,5}$ are the DC voltage gains of $G_{m1,2,3,5}$, respectively. One drawback is that this technique requires additional transconductors and capacitors to realize multiple integrators. The proposed op-amp achieves a 250µV ripple amplitude, a 1.9µV residual offset (mean + 1σ), and a 1.3MHz unity gain bandwidth, while using a 16kHz chopping frequency and consuming 700µA of current [6].

3.2.2 Switched Capacitor Notch Filter

Since the phase of the ripple is aligned with the chopping clocks, a switched capacitor notch filter (SC-NF) can be implemented with clocks synchronized with the chopping. This was

proposed by Bakker in 1997 [7] and again by Burt in 2006 [8].

Figure 3-5 (a) shows a block diagram of the op-amp proposed in [8]. This again consists of a LFP and a HFP, where the LFP includes a SC-NF following the chopped input transconductor G_{m1}. Figure 3-5 (b) shows the timing diagram of the chopping (Φ_{CH} and Φ_{CHINV}) and the SC-NF (Φ_{NF} and Φ_{NFINV}), as well as the input and output voltages of the SC-NF (V_{NFin} and V_{NFout}). First, V_{NFin} contains a triangular ripple due to the up-modulated output current of G_{m1}. However, since Φ_{NF} and Φ_{NFINV} operate at the same frequency as Φ_{CH} and Φ_{CHINV} but with a 90-degree phase difference, the SC-NF samples the triangular ripple whenever the amplitude becomes zero, and thus results in the ripple free output voltage V_{NFout}. This SC-NF adds a 90-degree phase delay to the signal at the chopping frequency, so that the HFP is required to bypass this phase delay and to stabilize the overall op-amp.

This filter does not consume quiescent current, and thus is more power efficient than active filters. The proposed op-amp consumes 17μA of current and achieves an NEF of 8.7 [8]. However, there are some drawbacks. First, clock skew and sampling capacitor mismatch result in residual ripple. Second, G_{m1} must have a wide output range to tolerate the maximum ripple amplitude, since the ripple still exists there. This problem becomes more severe in low noise designs, where the ripple amplitude is proportional to G_{m1}, as suggested by Equation (2-11). Third, due to the phase delay introduced by the SC-NF, the LFP requires a complicated frequency compensation with split Miller capacitors C_{m11a} and C_{m12a}. Consequently, the ripple can couple to the output through C_{m11a}. Fourth, the sampling action of the SC-NF generates kT/C noise that contributes to the in-band noise PSD.

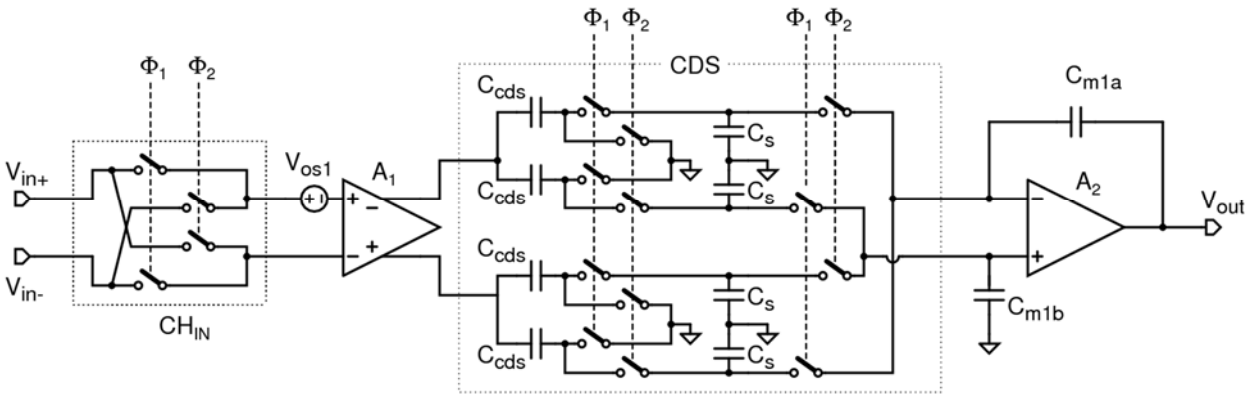

Figure 3-6: Chopper op-amp using CDS down-modulation

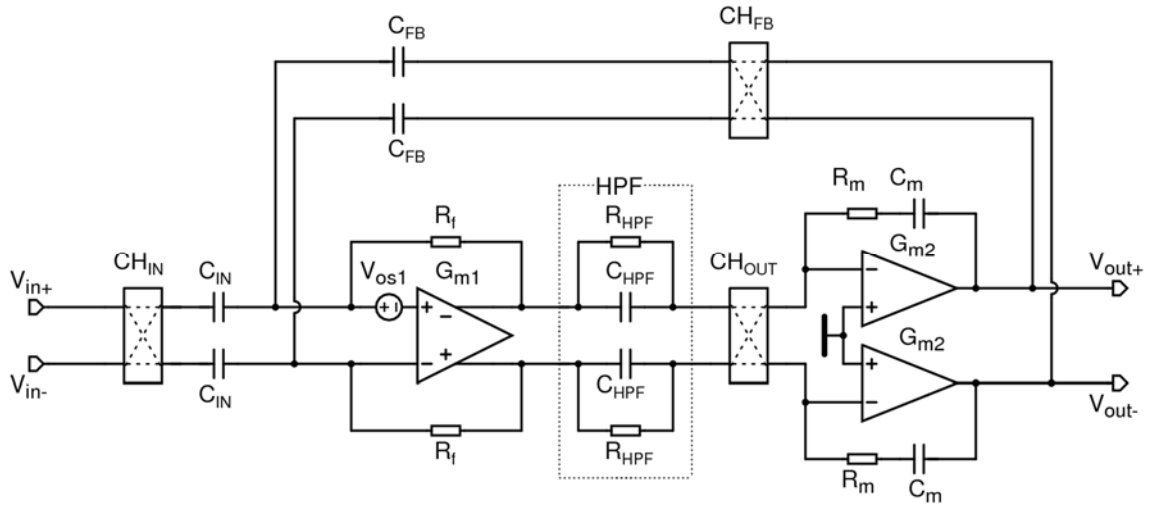

Figure 3-7: Continuous-time high-pass filtering based ripple reduction technique

3.2.3 High-Pass Filtering

Instead of low-pass or notch filters, high-pass filtering can be applied to block the DC offset that would otherwise become up-modulated ripple. The high-pass filter can be realized by correlated double sampling (CDS), which was proposed by Bilotti in 1999 [9] and again by Belloni in 2010 [10]. The block diagram is shown in Figure 3-6. The up-modulated signal is down-converted to the in-band by a correlated double sampling (CDS) stage, instead of by an output chopper. The input chopper and the CDS operate based on common complementary clocks Φ_1 and Φ_2.

Consequently, at the output of input stage A_1, the voltage difference between the two clock phases is detected by the CDS. Thus, the up-modulated signal is down-converted and is then provided to output stage A_2, while the DC offset of A_1 is blocked. In other words, the CDS also acts as a sampling high-pass filter.

However, the DC offset can saturate the output of A_1. To avoid this problem, the gain of A_1 is set relatively low, to 40dB in [9]. In [10], a continuous-time band-pass filter is implemented inside of A_1 to reduce the DC gain. However, this filter requires relatively large capacitors (a total of 60pF) to pass the up-modulated signal. Moreover, the CDS generates kT/C noise that contributes to the overall in-band noise of the op-amp [10].

In 2015, Chandarkumar proposed a continuous-time high-pass filtering ripple reduction technique for a bio-signal amplifier. Figure 3-7 shows a block diagram of the proposed chopper amplifier with a capacitive feedback network that sets a closed-loop gain of C_{IN}/C_{FB} [11]. Through two local feedback resistors R_f, the input-referred offset of G_{m1} (V_{os1}) shows up at its output without being amplified, and is then blocked by a high-pass filter (HPF) realized by R_{HPF} and C_{HPF}. While the input signal is up-modulated by CH_{IN}, is converted to a current by G_{m1}, and passes through the HPF. Therefore, this ripple reduction technique using R_f and the HPF prevents G_{m1} from being saturated without compromising its signal gain.

One drawback is that R_{HPF} needs to be greater than 100MΩ in order to sufficiently block the undesired DC offset, and that R_f also needs to be greater than 100MΩ in order not to affect the signal gain. Later, in 2016, Chandarkumar reported the actual IC implementation using a duty-cycled resistor to realize such large resistors [12]. However, the input bias voltages of G_{m2} are then only provided through such large resistors R_{HPF} and CH_{OUT}. Therefore, once these bias voltages are disturbed by, for instance, a large common-mode input step or a supply voltage change, it will take a long time to be settled to correct bias voltages.

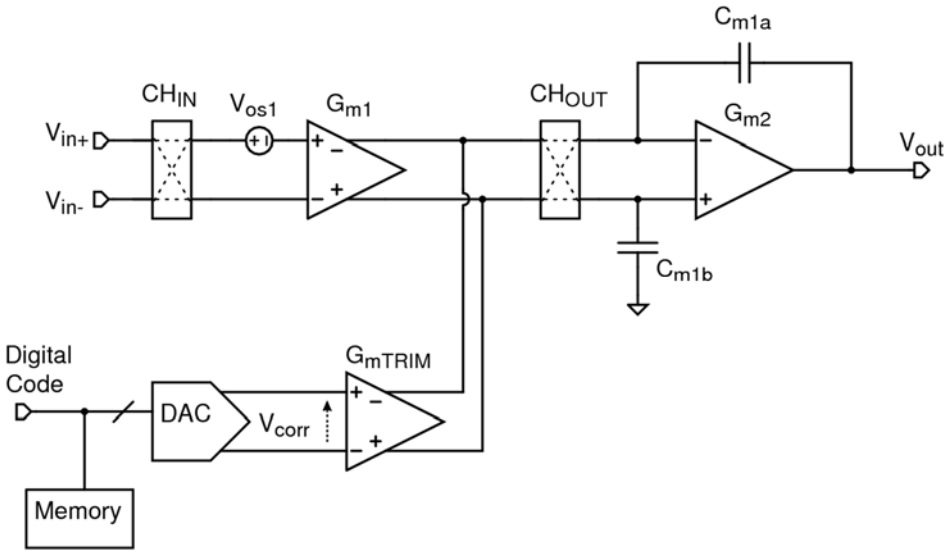

Figure 3-8: Chopper op-amp employing initial offset trimming

3.2.4 Initial Offset Trimming

As suggested by Equations (2.11) and (2.12), the amplitude of the ripple is proportional to that of the initial offset. Therefore, as shown in Figure 3-8, the initial offset can be trimmed to reduce the amplitude of the ripple. The initial offset can be easily measured by turning off the chopping during the trimming. However, as discussed in Section 2.1, the offset drift over temperature is usually not sufficiently compensated by the trimming, and thus can be greater than a few μV/°C. Therefore, the resulting ripple amplitude can easily exceed 100μV when temperature changes by tens of degrees.

3.2.5 Combination with Auto-Zeroing

Instead of offset trimming, auto-zeroing can be implemented to reduce the initial offset with better stability over temperature. As explained in Section 2.3.3, the auto-zeroing results in increased in-band noise PSD due to the noise folding. However, the high in-band noise PSD can be up-modulated by applying chopping after the auto-zeroing. With proper implementation of

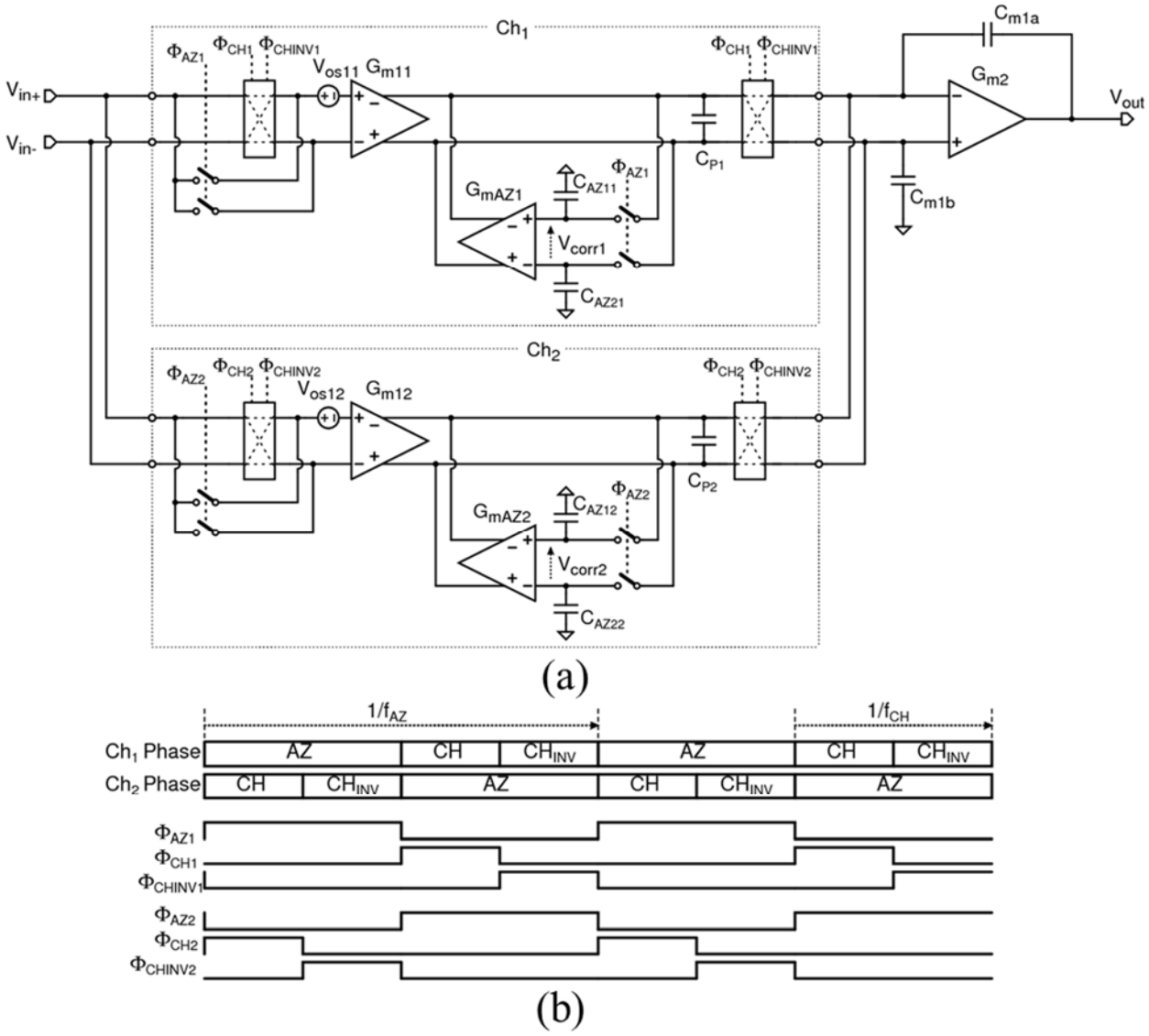

Figure 3-9: A ping-pong auto-zero and chopper op-amp: (a) circuit diagram; (b) timing diagram

auto-zeroing, a residual ripple in the range of few µV can be expected. This technique was proposed by Tang [13] in 2002 and again by Pertijs in 2010 [14].

Figure 3-9 (a) shows a block diagram of the op-amp proposed in [13]. To achieve continuous-time amplification, it ping-pongs two input channels Ch_1 and Ch_2, followed by an output stage G_{m2}. As shown in the timing diagram Figure 3-9 (b), each channel is driven by three clocks $\Phi_{AZ1,2}$, $\Phi_{CH1,2}$, and $\Phi_{CHINV1,2}$, to define auto-zeroing (AZ), chopping (CH), and inverting-chop (CH_{INV}) phases. When one channel is in the AZ phase, the other goes through CH and CH_{INV} phases. The chopping frequency f_{CH} is set at twice the auto-zeroing frequency f_{AZ}.

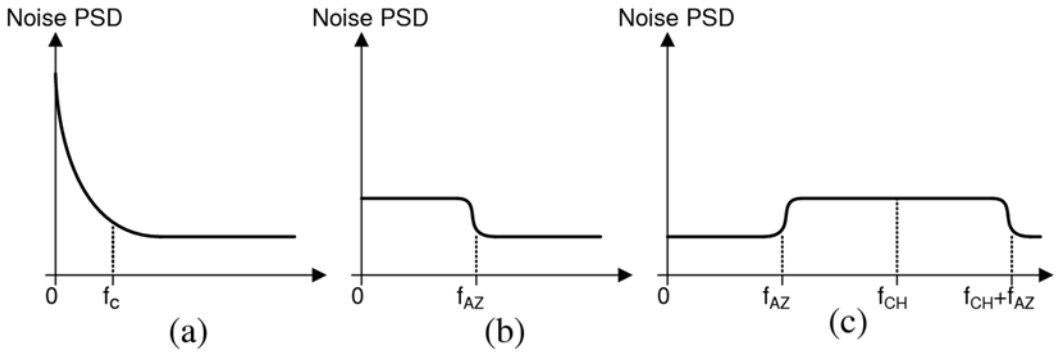

Figure 3-10: Noise PSDs (a) without auto-zeroing or chopping, (b) after auto-zeroing, and (c) after auto-zeroing and chopping

In Figure 3-10 (a), (b), and (c), noise PSDs are shown without auto-zeroing or chopping, after the auto-zeroing, and after the auto-zeroing and the chopping, respectively. The auto-zeroing almost eliminates 1/*f* noise, but introduces increased in-band noise PSD. This increased noise PSD lies in between DC and f_{AZ}, since the offset sampling occurs twice per auto-zeroing period $1/f_{AZ}$. The chopping then up-modulates this high noise PSD up to f_{CH}, to obtain an in-band noise PSD that is only slightly higher than the initial thermal noise floor. Another way, proposed in [14], is to set the auto-zeroing loop bandwidth lower than the auto-zeroing frequency f_{AZ}. This still results in a higher noise PSD at DC, but up to a lower frequency than f_{AZ}. Therefore, the chopping frequency can be set lower than f_{AZ} without degrading the resulting in-band noise PSD.

The op-amp proposed in [13] achieves a 3μV offset and a 20nV/√Hz in-band noise PSD, while consuming 800μA of current (NEF = 21.8). One drawback is the additional current consumption and die area for one extra input channel. Additionally, the ping-pong operation causes transient glitches, since parasitic capacitances C_{P1} and C_{P2} are charged to different voltages due to the mismatch of the offset correction voltages V_{corr1} and V_{corr2}. Moreover, V_{corr1} and V_{corr2} are usually higher than the initial offsets, since $G_{mAZ1,2}$ is set smaller than $G_{m11,12}$ to reduce the charge injection error as suggested by Equation (2-7).

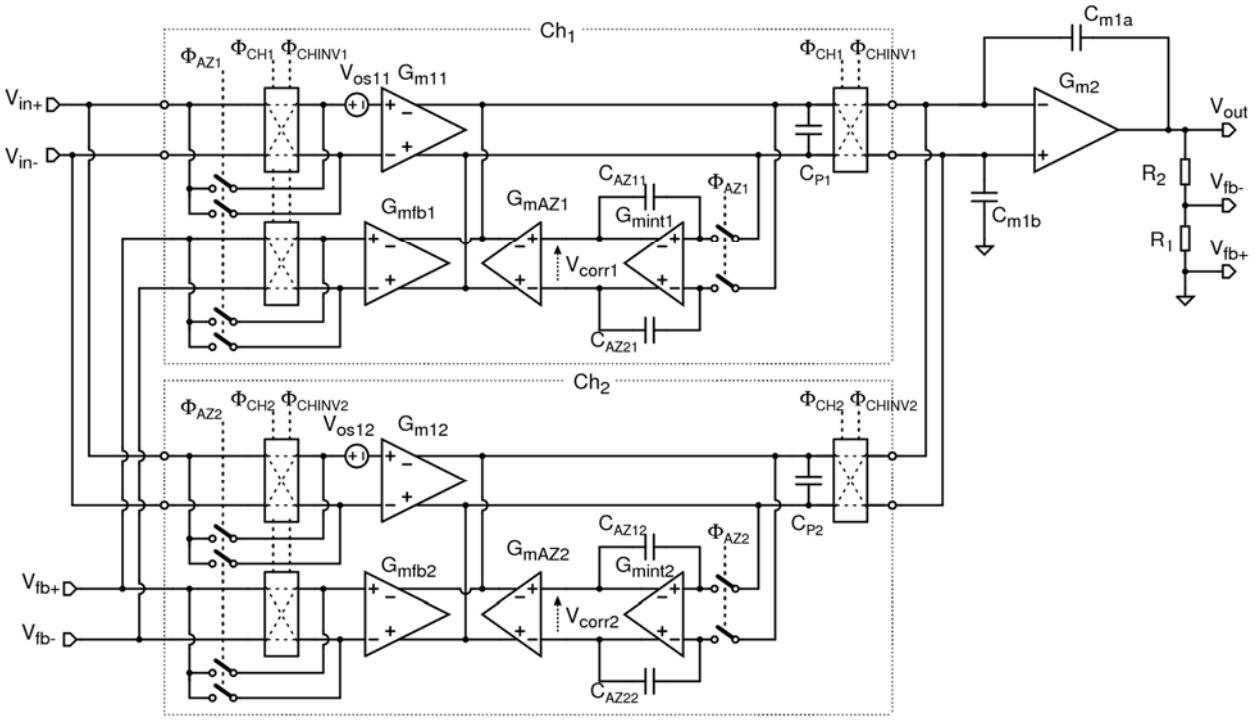

Figure 3-11: A ping-pong auto-zero and chopper CFIA employing active integrator sampling stages

Figure 3-11 presents a block diagram of the current feedback instrumentation amplifier (CFIA) presented in [14]. To mitigate the glitch problem due to the offset correction voltage mismatch, the two auto-zeroing loops each incorporate active integrators built around $G_{mint1,2}$. As a result, the voltages across parasitic capacitances $C_{P1,2}$ are only primarily dominated by the offsets of $G_{mint1,2}$, which are usually lower than the offset correction voltages $V_{corr1,2}$. However, the active integrators come at a cost of extra current consumption and die area.

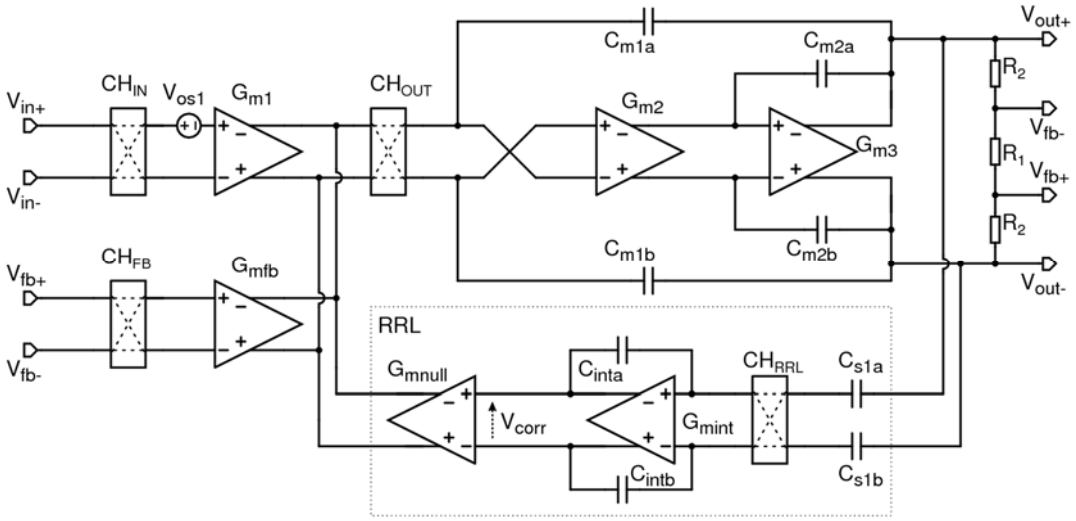

Figure 3-12: Chopper CFIA using AC-coupled ripple reduction loop

3.2.6 AC-Coupled Ripple Reduction Loop

In 2009, Wu proposed an AC-coupled ripple reduction loop (RRL) which senses the up-modulated ripple at the output and forms local feedback to cancel the initial offset [15]. Figure 3-12 shows a block diagram of the proposed current feedback instrumentation amplifier (CFIA). By using resistors, the IA gain is set to $1+2R_1/R_2$, provided that the input and feedback transconductors G_{m1} and G_{mfb} are identical.

The ripple at the output V_{out} is AC-coupled by $C_{s1a,b}$ and is then down-modulated by CH_{RRL}. The down-modulated DC offset is amplified by an integrator built around G_{mint}, generating an offset correction voltage V_{corr}. A nulling transconductor G_{mnull} cancels the initial offset of G_{m1} (V_{os1}) by means of the feedback operation, which reduces the output ripple. The desired DC signal is blocked by $C_{s1a,b}$, and thus is not affected by the RRL.

However, AC signals near the chopping frequency are not distinguished from the ripple, and thus are suppressed by the RRL. In other words, the RRL creates a notch in the frequency transfer function. This notch can cause instability in the overall feedback, if the closed-loop bandwidth is higher than the notch frequency. Besides, since the RRL senses the ripple at the overall output, it can be affected by output transients caused by, for instance, a kickback of the subsequent ADC. This results in a residual output ripple that continues until the RRL recovers.

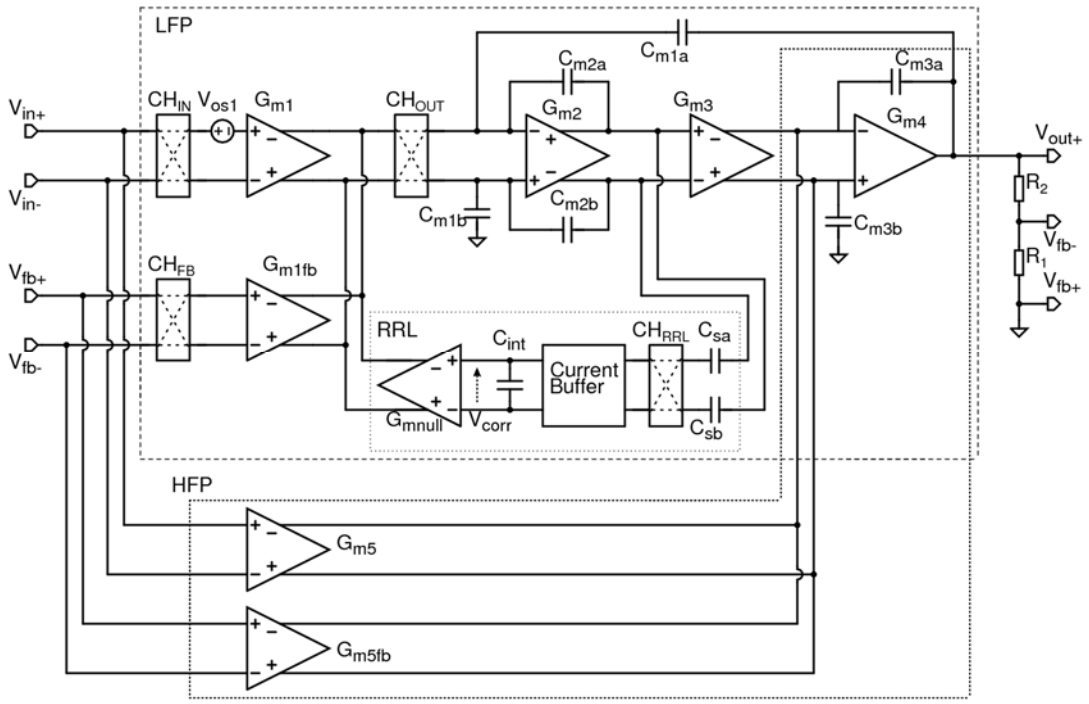

Figure 3-13: Multi-path chopper CFIA using AC-coupled RRL

These drawbacks were solved by Fan in 2010 [16]; the proposed CFIA is shown in Figure 3-13. First, the CFIA consists of a LFP and a HFP. The LFP dominates the low frequency performance of the overall CFIA, and the input and feedback transconductors G_{m1} and G_{m1fb} are chopped. A RRL implemented in the LFP reduces the up-modulated ripple, but creates a notch in the transfer function of the LFP. This notch is bypassed by the HFP, and thus buried in the overall transfer function. The ripple is sensed at the output of an integrator built around G_{m2}, instead of at the overall output. Therefore, this RRL is relatively robust to output transients.

The proposed CFIA can also be used as an op-amp by connecting the input and feedback transconductors in parallel. In this case, it achieves a 1μV offset, a 10.5nV√Hz in-band noise PSD, and a 1.8MHz unity gain bandwidth. The loop bandwidth of the RRL can be lower without affecting the unity gain bandwidth of the overall op-amp. Relatively large capacitors of C_{int} = 30pF and $C_{m2a,b}$ = 24pF are used to reduce a residual second harmonic ripple of the chopping caused by initial offset of the current buffer. The entire CFIA is implemented in a 1.8mm^2 die, and consumes 143μA of current (NEF = 4.8), only 6% of which is consumed by the RRL.

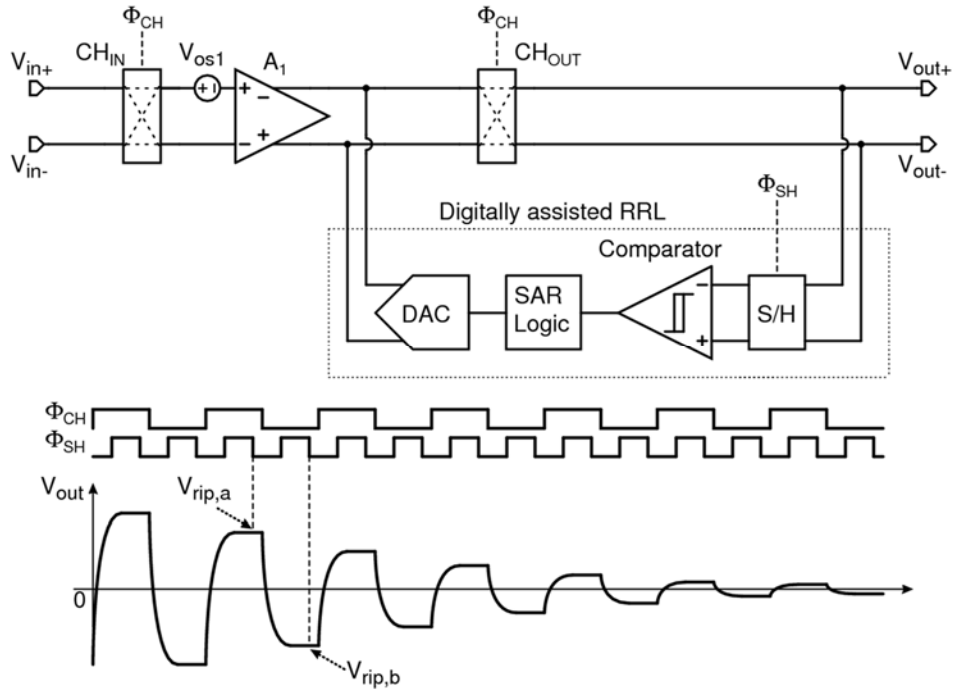

Figure 3-14: Digitally assisted RRL

3.2.7 Digitally Assisted Ripple Reduction Loop

In 2011, a digitally assisted RRL was proposed by Xu [17], a simplified block diagram of which is shown in Figure 3-14. This RRL consists of a sample-and-hold stage S/H, a comparator, a SAR logic, and a current DAC. The S/H samples the two peak voltages of the ripple ($V_{rip,a}$ and $V_{rip,b}$). The comparator then determines a digital bit based on the polarity of $V_{rip,a} - V_{rip,b}$, so that the DAC output current changes such that the offset is reduced. After the circuit starts up, an overall 7-bit digital code is determined by bit trials of the SAR logic, and thus the output ripple is reduced after each bit trial. After all the bit trials are complete, the determined 7 bit is memorized and then the amplifier starts operating.

This digitally assisted RRL can also be continuously activated to correct the offset drift after the start up. This technique only requires additional quiescent current in the 1-bit comparator and the DAC, and thus can be power efficient. Furthermore, it does not require filter capacitor in its feedback path, and thus can be implemented in an area efficient manner. However, some residual ripple remains due to finite digital resolution. For instance, when a 7-bit

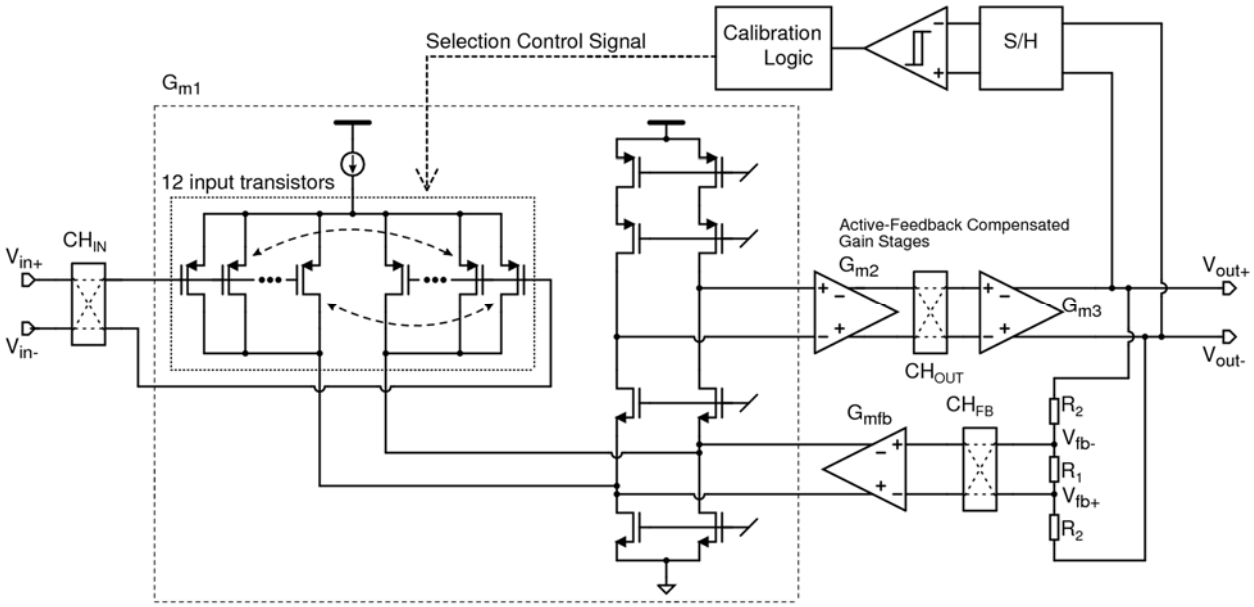

Figure 3-15: CFIA employing digitally assisted dynamic input pair matching

DAC must cover a 5mV maximum offset, the one LSB becomes 40μV, resulting in the worst-case input-referred residual ripple of 20μV. On the other hand, increasing the resolution will complicate the DAC design and increase the number of bit-trials to be completed.

Figure 3-15 shows a CFIA incorporating a digitally assisted RRL which was proposed by Akita in 2013 [18]. Instead of using an offset correction DAC, the input transconductor contains 12 input transistors, each of which makes a random offset contribution. The RRL consists of a comparator and a calibration logic to control the connection of the 12 input transistors, so that the input transistors can be paired to result in the lowest amount of output ripple. This RRL implementation does not require a DAC and thus it can reach greater power efficiency. This work achieves a 3.5μV offset and a 13.5nV/√Hz noise PSD while consuming 194μA (NEF = 7.2). However, similar to the circuit shown in Figure 3-14, some residual ripple remains due to the finite digital resolution. The worst-case ripple out of 12 units is $0.25mV_{p\text{-}p}$, while that without the RRL is $4mV_{p\text{-}p}$.

Table 3-1: Comparison of chopper op-amps employing ripple reduction technique

	Witte [5]	Burt [7]	Belloni [9]	Tang [10]	Fan [13]
Year	2006	2006	2010	2002	2010
I_{SY} [µA]	700	17	14.4	800	143
f_{CH} [kHz]	32	125	500	15	30
Vos max [µV]	3.0	10.0	5.0	5.0	1.0
Ibias max [pA]	** NS	±200	** NS	±100	±110
GBW [MHz]	1.37	0.35	* 0.26	2.5	1.8
en [nV/√Hz]	15	55	37	20	10.5
NEF	15.3	8.7	5.5	21.8	4.8
GBW/Isy	2	20.6	18	3.1	12.6
Die area [mm^2]	3.6	0.7	1.14	0.67	1.8
Ripple reduction technique	Active Filter	SC-NF	Chop + CDS	Auto-Zero	RRL

* Conditionally stable op-amp, ** NS = Data Not Shown

3.3 Comparison of the Techniques

This chapter has reviewed various techniques to reduce DC errors such as residual offset and input bias current. Menolfi proposed a band-pass filtering technique to attenuate the glitches that would otherwise be down-modulated and turn into residual offset [2]. However, this technique requires an additional oscillator and a band-pass filter with a matching center frequency. Later, Menolfi also proposed a dead-timed down-modulation technique that attenuates the glitches without consuming extra current [3]. However, to mitigate the effective gain reduction, one chopping period needs to be sufficiently longer than the dead time, which limits the maximum achievable chopping frequency. By using the nested chopping proposed by Bakker [4], the residual offset and input bias current, caused by the inner fast chopping, are up-modulated by the outer slow chopping. However, this generates a high noise spectrum at the slow chopping frequency, which limits the usable signal bandwidth. Therefore, new circuit techniques should be explored to reduce DC errors, while offering a high usable signal bandwidth.

This chapter has also reviewed the various ripple reduction techniques. Table 3-1

compares the performances of the chopper op-amps employing these ripple reduction techniques. Since some techniques consume more extra current and die area than others, the figures-of-merit, such as the NEF and GBW/Isy, should be compared in addition to the die area. One way to reduce the ripple is to filter the up-modulated ripple by active integrators at the cost of extra current [6]. Instead, a SC notch filter can filter the ripple without consuming extra current [7,8], although the ripple remains at the output chopper, which limits the design of the input transconductor. In [9,10], the output chopping is replaced by CDS that down-converts the up-modulated signal while blocking the DC offset. However, the input amplifier needs to have a relatively low gain [9] or have a band-pass characteristic [10], in order not to saturate its output with the DC offset. In [11,12], local feedback resistors are placed around the input transconductor, in order not to amplify its offset and not to saturate its output. However, these feedback resistors need to be greater than 100MΩ in order not to affect the signal gain, which will increase the time required to recover from some disturbances. In these three ripple reduction techniques, the initial offset remains, which causes problems and/or complicates the design.

Therefore, the preferred approach is to reduce the initial offset that would otherwise turn into the output ripple. One way to reduce an initial offset is simply with trimming, although the offset (i.e. the ripple) will increase when temperature changes. Instead, the initial offset can be auto-zeroed, and then the resulting high noise PSD in the in-band can be up-modulated by the chopping [13,14]. However, to achieve continuous-time amplification, this requires an additional input channel that consumes extra current and die area. Another technique is to use a ripple reduction loop (RRL) that continuously detects the ripple and cancels the initial offset by the feedback [15]. However, this creates a notch in the signal transfer function, which can cause instability in the overall feedback loop. This notch can be buried by adding a HFP [16]. The RRL can be digitally assisted with a comparator, a SAR logic, and a current DAC to cancel the offset [17]. This technique can be more area efficient without requiring filter capacitor in its feedback path, although higher digital resolution is required to reduce the residual ripple.

If auto-zeroing is used, then as indicated by Equation (2-7), the initial offset (i.e. the ripple) can be reduced by a factor equal to the auto-zeroing loop gain, as long as the charge injection related errors are negligible. Similarly, the ripple can be reduced by a factor equal to the gain of the RRL. Therefore, these techniques can achieve microvolt-level ripple. This thesis also

proposes ripple reduction techniques that reduce the initial offset (i.e. the ripple) in a power and area efficient manner. In the designs discussed in Chapter 4 and 5, ripple is detected and then suppressed as in a RRL (Figure 3-13), but a switched-capacitor notch filter is employed in the feedback path instead of a continuous-time filter. In Chapter 6, the initial offset is reduced by auto-zeroing but in a more power efficient manner than the approach shown in Figure 3-9. Provided the ripple is sufficiently reduced, the output glitches caused by charge injection can still result in high noise spectra. Therefore, this thesis also explores new circuit techniques that address both the ripple and the glitches.

3.4 References

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Chapter 4

Chopper Op-Amp with Auto-Correction Feedback[1]

This chapter proposes a ripple reduction technique, called auto-correction feedback (ACFB). It senses the up-modulated ripple in the internal circuit nodes, forms local feedback, and cancels the initial offset to reduce the output ripple. The proposed ACFB has been implemented in a stand-alone chopper op-amp which occupies a 0.64mm^2 die area in a 0.35μm CMOS process augmented by 5V CMOS transistors. The op-amp only draws 13μA from a 1.8V to 5.5V supply, and operates over a rail-to-rail input common-mode voltage range and a –40°C to 125°C temperature range. It achieves a 10μV maximum offset, a 50pA maximum input bias current, a 95nV/√Hz in-band noise PSD, and a 120kHz unity gain bandwidth. With the use of the ACFB, the worst-case ripple spectrum is reduced from 4.8mV$_{rms}$ to 42μV$_{rms}$ at the 50kHz chopping frequency.

First, Section 4.1 describes the motivation for designing a low offset, low power op-amp for portable applications. Next, Section 4.2 presents the overall chopper op-amp architecture employing the ACFB, followed by a residual error analysis in Section 4.3. Section 4.4 then presents transistor-level circuit implementation including the transconductors and the clock generator. Lastly, Section 4.5 discusses the measurement results, and the chapter ends with a conclusion in Section 4.6.

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[1]This chapter is derived from a journal publication of the author: Y. Kusuda, "Auto Correction Feedback for Ripple Suppression in a Chopper Amplifier", *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1436-1445, Aug. 2010.

4.1 Motivation

As described in Section 1.5.1, biomedical sensing applications such as EEG, ECG, and EMG, require precision op-amps that can achieve both low 1/*f* noise and low input bias current below 100pA [1-3]. Additionally, to serve portable and wearable applications, such op-amps should also have a current consumption lower than 20μA, a die size smaller than 0.7mm^2, and a supply voltage range including 1.8V. The bandwidth of these biomedical signals is about 200Hz, which allows the use of an external low-pass filter to reduce ripple, although the op-amp should still have a relatively small output ripple. For instance, to achieve microvolt-level ripple after 40dB filter attenuation, the op-amp must have an output ripple amplitude in the order of 100 microvolts. This is much smaller than the ripple associated with the native offset of a CMOS differential pair, and thus can only be achieved with the aid of an on-chip ripple reduction technique.

Previous ripple reduction techniques were reviewed in Section 3.2 [4-15]. However, the techniques in [4,10-12] consume extra current, while those in [5-9] require higher chopping frequency thus resulting in higher input bias current. The RRL technique in [14] senses and reduces the ripple by feedback in a power efficient way without requiring higher chopping frequency. The digitally assisted RRL in [15] can be implemented in a more area efficient manner without requiring large filter capacitor in its feedback path, although higher digital resolution is required to reduce the residual ripple.

In order to serve the portable biomedical applications described above, another ripple reduction technique, called auto-correction feedback (ACFB), is proposed in this chapter. Similar to the RRL, the ACFB senses and reduces the ripple by feedback with a power efficient manner as well as an area efficient manner. Moreover, it has a design flexibility to select a relatively low chopping frequency, thus achieving a relatively low input bias current. On the other hand, the ripple reduction capability of the ACFB is limited by its relatively small loop gain, although the remaining output ripple can be attenuated by an external low-pass filter in applications such as ECG readout which only require low signal bandwidth. Furthermore, it causes a noise PSD peak around the chopping frequency.

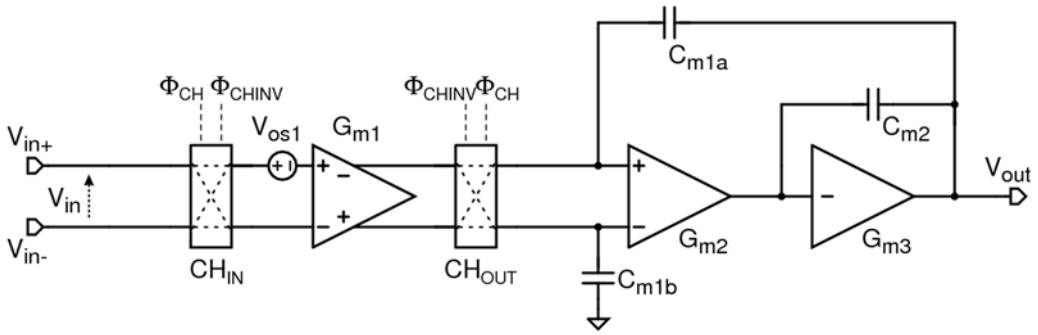

Figure 4-1: Three stage chopper op-amp

4.2 Op-Amp and Ripple Reduction Architecture

4.2.1 Basic Three Stage Chopper Op-Amp

As described in Section 1.2.1, a precision op-amp should provide at least a 100dB open-loop gain to minimize gain errors. However, the achievable gain of a chopped input transconductor is limited by its dynamic output conductance as explained in Section 2.4.4. Moreover, a resistive load further decreases the gain of the output transconductor. Therefore, chopper op-amps often employ an intermediate gain stage, e.g. a second transconductor [6,9]. Adding more gain stages further increases the open-loop gain. However, it also increases the current consumption and die area, and the overall error often does not improve any further due to the presence of input offset. Therefore, the proposed chopper op-amp in this chapter consists of input, second, and output stage transconductors G_{m1}, G_{m2}, and G_{m3}, as shown in Figure 4-1. Additionally, G_{m1} is chopped by input and output choppers CH_{IN} and CH_{OUT} to up-modulate the input offset V_{os1} and $1/f$ noise. Meanwhile, the thermal noise PSD of G_{m1} around the chopping frequency is down-modulated, at which point it dominates the in-band low frequency noise PSD of the overall op-amp. As discussed in the previous section, the up-modulated V_{os1} and $1/f$ noise at the chopping frequency f_{CH} must be reduced by a ripple reduction technique.

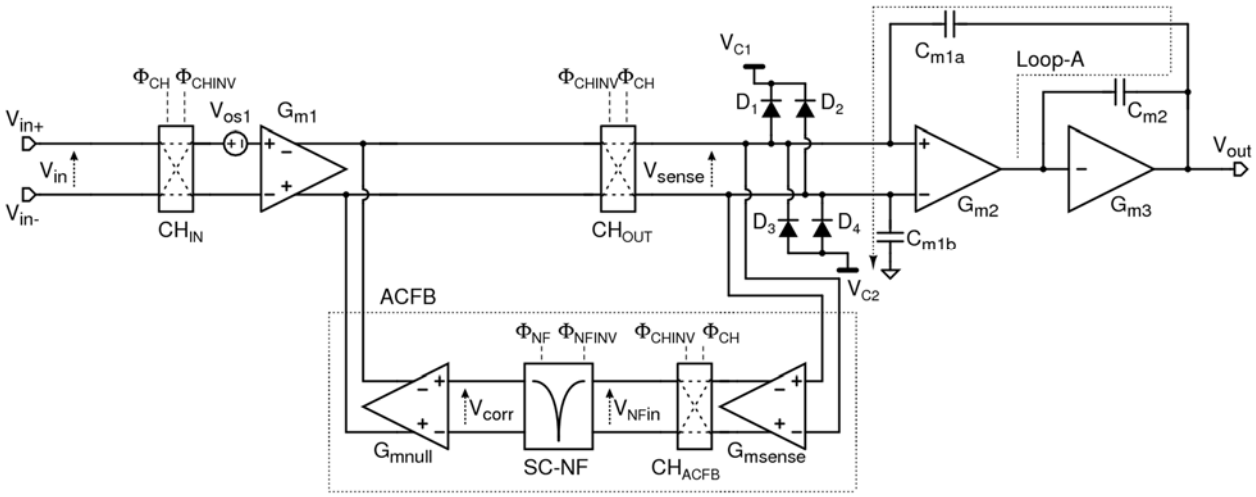

Figure 4-2: Three stage chopper op-amp employing auto-correction feedback (ACFB)

4.2.2 Auto-Correction Feedback

As discussed in Section 2.4.1, the amplitude of the up-modulated ripple can be decreased by reducing the initial offset V_{os1}. Figure 4-2 shows a proposed ripple reduction technique, called auto-correction feedback (ACFB), which is implemented in the three stage chopper op-amp shown in Figure 4-1. The ACFB consists of a sensing transconductor G_{msense}, a chopper CH_{ACFB}, a switched capacitor notch filter SC-NF, and a nulling transconductor G_{mnull}. First, the up-modulated ripple is sensed at the V_{sense} nodes by G_{msense}, and is down-modulated by CH_{ACFB}, which operates with the same clock timing as CH_{IN} and CH_{OUT}. The down-modulated DC offset component passes the SC-NF and generates an offset correction voltage V_{corr}, such that G_{mnull} cancels V_{os1}.

In contrast to [14], the ACFB senses the ripple at the V_{sense} nodes which are at the output of the output chopper. Clamp diodes $D_{1\text{-}4}$ are added, to maintain the V_{sense} nodes stable, and hence the ACFB even in the presence of external output transients. This technique can be applied to chopper op-amps consisting of two or more gain stages without requiring an extra gain stage in their main signal path. On the other hand, as will be analyzed in Section 4.3.1, the V_{sense} nodes are also at the input of G_{m2}, which is a virtual ground, thus resulting in a small ripple amplitude and hence small loop gain of the ACFB.

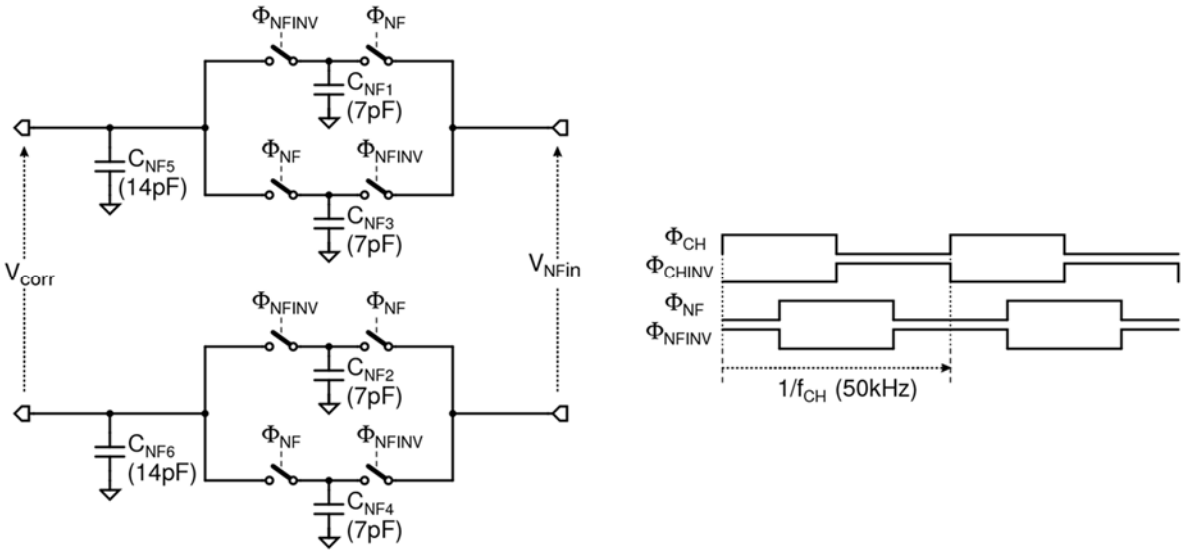

Figure 4-3: Switched capacitor notch filter (SC-NF)

In contrast to [6], the SC-NF is implemented in the ACFB rather than in the main signal path. Additionally, the ACFB requires G_{msense} and G_{mnull}, hence extra current and die area. On the other hand, since V_{os1} is cancelled by the ACFB, the ripple amplitude at the output of G_{m1} can be sufficiently smaller without requiring higher chopping frequency.

4.2.3 Switched Capacitor Notch Filter (SC-NF)

In [14], a continuous-time integrator is implemented in the RRL to selectively reduce the offset without affecting the desired input signal. As discussed in Section 3.2.6, relatively large total capacitor of 78pF is used to reduce a residual second harmonic ripple of the chopping caused by initial offset of the current buffer.

In the proposed ACFB, this selection is realized by the SC-NF shown in Figure 4-3 in an area efficient way. It is a pseudo-differential circuit that samples a differential input V_{NFin} and generates a differential output V_{corr}. The positive and negative signal paths each consist of two sampling capacitors $C_{NF1,2}$ and $C_{NF3,4}$, sampling switches, and a load capacitor $C_{NF5,6}$. The sampling switches are driven by complementary clocks Φ_{NF} and Φ_{NFINV} that operate at the same frequency as the chopping clocks Φ_{CH} and Φ_{CHINV}, but with a 90-degree phase difference.

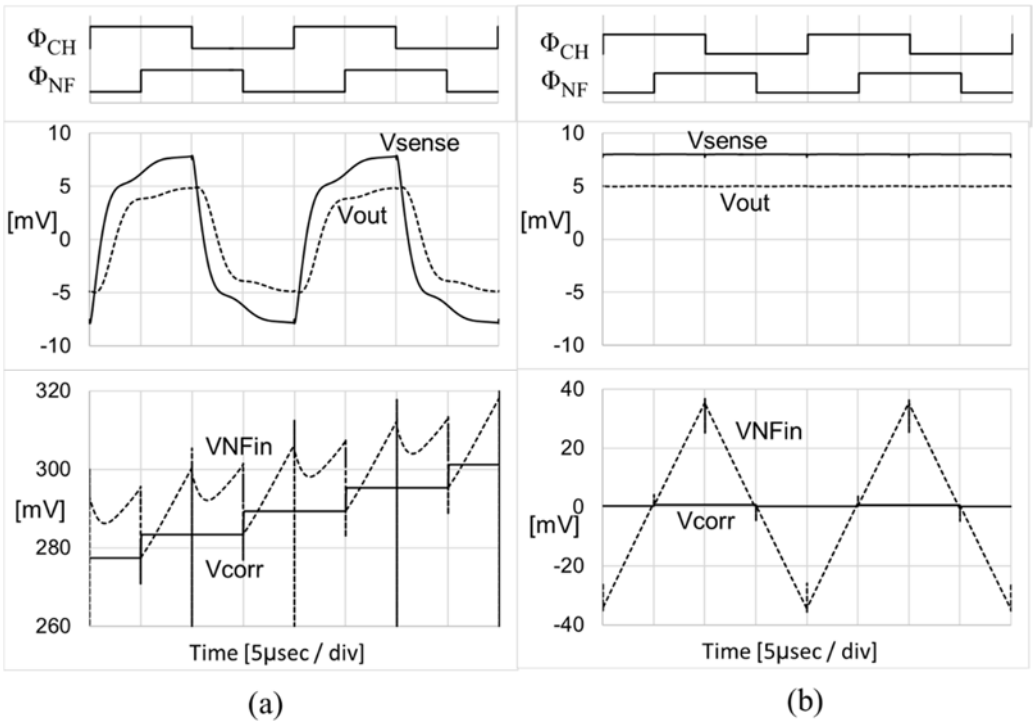

Figure 4-4: Transient simulation of the SC-NF: (a) with 5mV offset; (b) with 5mV DC signal

To understand the operation of the SC-NF, the circuit in Figure 4-2 is simulated, where the ACFB loop is broken at the V_{corr} nodes to observe the behavior clearly. First, with V_{in} = 0mV and V_{os1} = 5mV, Figure 4-4 (a) shows the voltage waveforms at V_{sense}, V_{NFin}, and V_{corr} along with the clock timings. The up-modulated V_{os1} causes a ±7.8mV ripple at V_{sense}. This ripple is converted into a current by G_{msense} and is down-modulated by CH_{ACFB}, resulting in differential currents with constant polarity charging the sampling capacitors. Consequently, V_{NFin} and V_{corr} continue ramping up. Note that when the ACFB loop is closed, V_{corr} will be adjusted to $V_{corr} \approx V_{os1} \bullet (G_{m1}/G_{mnull})$, which reduces the offset, and thus also the output ripple.

Next, with V_{in} = 5mV and V_{os1} = 0mV, Figure 4-4 (b) shows the voltage waveforms at the same nodes. The DC input voltage V_{in} generates a DC voltage at V_{sense} rather than AC ripple, resulting in up-modulated differential currents charging the sampling capacitors. This generates a triangular ripple at V_{NFin}, the amplitude of which becomes nearly zero whenever it is sampled, producing the constant output voltage V_{corr}.

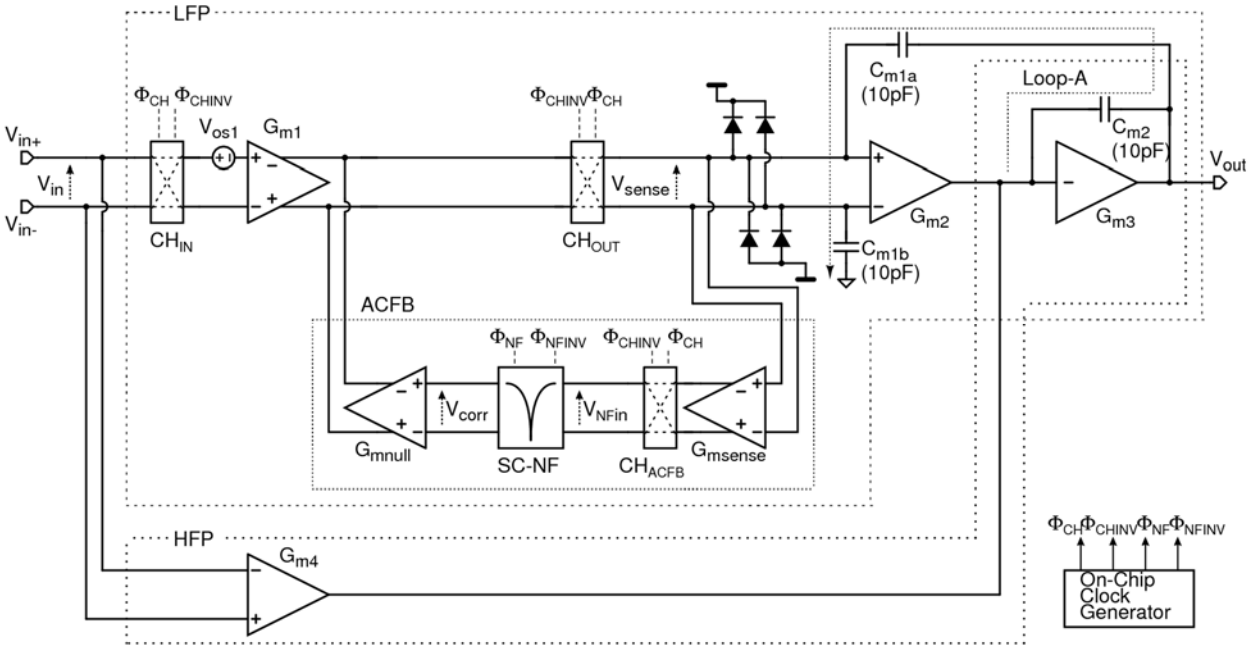

Figure 4-5: Proposed overall op-amp

To a first order, the SC-NF completely eliminates the up-modulated DC signal and its harmonics without requiring large capacitor area. Furthermore, the initial offset of G_{msense} is also eliminated in the same manner. On the other hand, as will be discussed in Section 4.3.1, the sampling action of the SC-NF introduces non-dominant pole, so that the unity gain frequency of the ACFB loop must be reduced by increasing the capacitors in the SC-NF. This actual implementation uses a total capacitor of 56pF realized by high density MOS capacitors, because their linearity does not affect the performance of the ACFB. Alternatively, as proposed in [6], the SC-NF can be implemented by differential sampling and load capacitors, which required poly-poly capacitors with a total value of 14pF.

4.2.4 High Frequency Path (HFP) and Overall Op-Amp

Thanks to the SC-NF, the ACFB does not affect the desired DC nor the low frequency signals while reducing the undesired offset. However, AC signals near the chopping frequency f_{CH} are not distinguished from the up-modulated ripple at V_{sense}, and are also attenuated by the ACFB. This means that the ACFB creates a notch at f_{CH} in the signal transfer function of the main signal path.

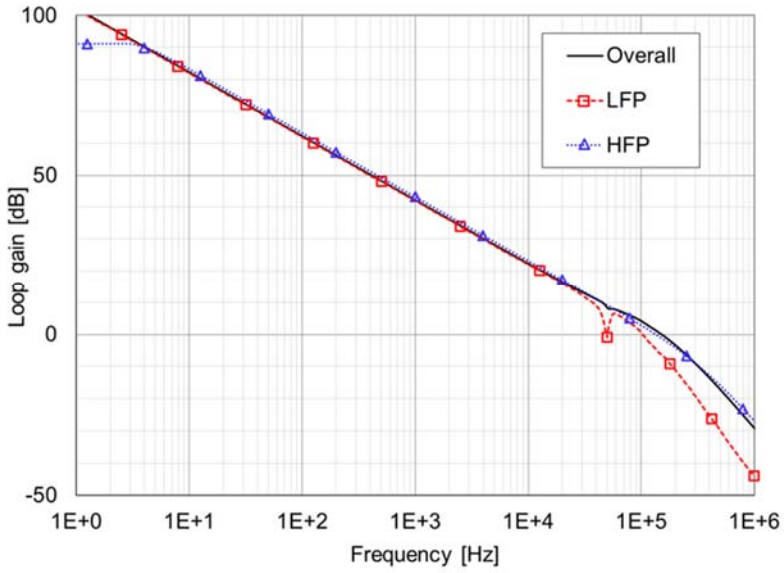

Figure 4-6: Simulated transfer functions of the LFP, HFP, and the overall op-amp

The notch in the transfer function causes a significant phase shift, leading to instability. As described in Sections 3.2.2 and 3.2.5, this notch can be bypassed by adding a high frequency path (HFP) [4,6,14,16]. Figure 4-5 presents a block diagram of the proposed overall op-amp consisting of a low frequency path (LFP) and the HFP. The LFP is the same circuit presented in Figure 4-2 including the chopped input transconductor G_{m1}, the second and output stage transconductors G_{m2} and G_{m3}, and the ACFB. The HFP consists of a feedforward input transconductor G_{m4} and shares G_{m3} with the LFP. The gain of the LFP dominates the overall op-amp in lower frequencies, but significantly drops at the chopping frequency due to the notch. The HFP then takes over the transfer function of the overall op-amp, and determines the unity gain bandwidth f_u given by:

$$f_u = \frac{G_{m4}}{2\pi \cdot C_{m2}}. \qquad (4\text{-}1)$$

In order to avoid a pole-zero doublet, the gains of the LFP and HFP must be matched at the transition frequency by satisfying:

$$\frac{G_{m1}}{2\pi \cdot C_{m1a,b}} = \frac{G_{m4}}{2\pi \cdot C_{m2}}. \qquad (4\text{-}2)$$

Figure 4-6 shows the simulated transfer functions of the LFP, HFP, and the overall op-amp, which achieves a smooth –20dB/dec roll-off.

Table 4-1: Transconductance and supply current of each block

	Transconductance	Supply Current
Gm1	7.5 µS	1.31 µA
Gm2	6.0 µS	0.48 µA
Gm3	125.0 µS	6.63 µA
Gm4	7.5 µS	0.71 µA
Gm,sense	4.0 µS	0.60 µA
Gm,null	0.5 µS	---
Clock Generator	---	1.92 µA
Bias & LDO	---	1.30 µA
(Total)	---	12.95 µA

Table 4-1 shows the transconductance and supply current of each block. The unity gain bandwidth f_u is set to 120kHz by setting $C_{m1a,b} = C_{m2} = 10$pF, while the chopping frequency is set to 50kHz. The current consumption is dominated by G_{m3}, which has to drive an external load capacitor of up to 100pF. Additionally, the required transconductance of G_{m1} is determined by the targeted in-band noise PSD. On the other hand, G_{msense} does not influence the primary specifications of the op-amp, and thus only consumes 5% of the total supply current. Besides, as will be explained in Section 4.4.1, G_{mnull} is actually implemented inside of G_{m1}, and thus does not consume extra current.

4.3 Residual Error Analysis

Not only previous chopper op-amps, but also the proposed chopper op-amp will have a residual ripple and a residual offset due to various circuit imperfections, such as the initial offsets of the transconductors and the charge injection mismatch of the switches. This section presents the analysis and simulation results of these residual errors.

4.3.1 ACFB Loop Gain

Similar to the auto-zeroing loop discussed in Section 2.3.2, the ACFB has a finite loop gain A_{vACFB} which results in residual errors. By using the circuit shown in Figure 4-2, the loop is broken at the V_{corr} nodes, and its gain can be broken down into two parts, i.e. $A_{vACFB} \equiv A_{vACFB1} \bullet A_{vACFB2}$; A_{vACFB1} is the gain from the V_{corr} to V_{sense} nodes through G_{mnull} and CH_{OUT}; A_{vACFB2} is the gain from V_{sense} to the output of the SC-NF through G_{msense} and CH_{ACFB}.

First, V_{corr} is converted into differential currents + $I_{null}/2$ and $-I_{null}/2$ by G_{mnull}, and is then up-modulated by CH_{OUT}. These up-modulated currents are converted into a voltage with an impedance at the V_{sense} nodes. At the chopping frequency f_{CH}, this impedance is dominated by the capacitors $C_{m1a,b}$. By assuming that the input of G_{m3} is a virtual ground, Kirchhoff's voltage law can be applied to a local loop including C_{m2}, C_{m1a}, V_{sense}, and C_{m1b} (Loop-A in Figure 4-2), resulting in:

$$\frac{G_{m2} \cdot V_{sense}}{2\pi j \cdot f_{CH} \cdot C_{m2}} - \frac{\frac{I_{null}}{2}}{2\pi j \cdot f_{CH} \cdot C_{m1a}} + V_{sense} - \frac{\frac{I_{null}}{2}}{2\pi j \cdot f_{CH} \cdot C_{m1b}} \approx 0 . \qquad (4\text{-}3)$$

By applying $I_{null} = G_{mnull} \bullet V_{corr}$, the equation above can be re-formatted to:

$$A_{vACFB\ 1} \equiv \frac{V_{sense}}{V_{corr}} \approx \frac{G_{mnull}}{G_{m2}} \cdot \frac{C_{m2}}{C_{m1a,b}} \cdot \frac{1}{1 + 2\pi j \cdot f_{CH} \cdot \frac{C_{m2}}{G_{m2}}} . \qquad (4\text{-}4)$$

By applying the parameters in Table 4-1, A_{vACFB1} has a 0.07 magnitude (-23dB) and a 32-degree phase delay.

Next, V_{sense} is converted into differential currents by G_{msense} and is down-modulated by CH_{ACFB}. These down-modulated currents flow into the sampling capacitors C_{NF1-4}, which forms an integrator. The resulting voltage V_{NFin} will then be sampled by the clocks Φ_{NF} and Φ_{NFINV}. Since the signal of interests at V_{NFin} is down-modulated, its phase is arbitrary relative to those of Φ_{NF} and Φ_{NFINV}. Therefore, this sampling action will result in a sinc filter rather than a notch filter. The resulting gain A_{vACFB2} is given by:

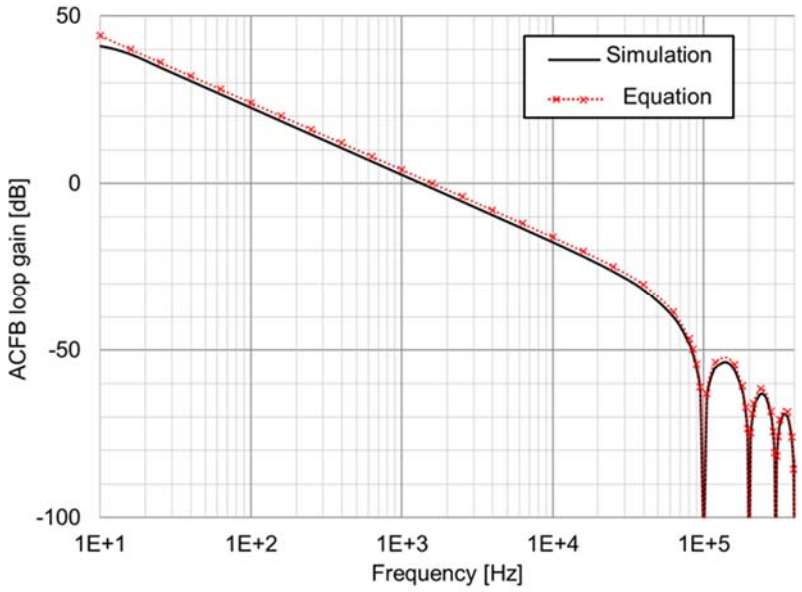

Figure 4-7: Calculated and simulated loop gain of the ACFB

$$A_{vACFB\,2} \approx \frac{G_{msense} \cdot R_{osense}}{1 + 2\pi jf \cdot R_{osense}(2C_{NF\,1-4} + C_{NF,5,6})} \cdot \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_{CH}}\right)}{\frac{\pi}{2}\frac{f}{f_{CH}}}, \qquad (4\text{-}5)$$

where R_{osense} is the impedance at the output of G_{msense}, which is dominated by the dynamic switching conductance of CH_{ACFB} and results in the DC gain ($G_{msense} \cdot R_{osense}$) of 64dB.

By combining A_{vACFB1} and A_{vACFB2}, the overall loop gain A_{vACFB} is 41dB at DC. This gain first drops with a slope of –20dB/dec due to the dominant pole associated with $C_{NF1\text{-}6}$. It then has a notch, hence a significant phase shift, at $2f_{CH}$ due to the sinc filter. Therefore, the unity gain bandwidth of the ACFB f_{uACFB} must be well below $2f_{CH}$ to keep the loop stable. As shown in Figure 4-3, the capacitors are set to $C_{NF1\text{-}4}$ = 7pF and $C_{NF5,6}$ = 14pF, so that $f_{u,ACFB}$ will be 1.5kHz while f_{CH} is 50kHz. This $f_{u,ACFB}$ is still high enough to effectively cancel the $1/f$ noise of G_{m1}, the corner frequency of which is 200Hz. Based on Equations (4-4) and (4-5), the calculated A_{vACFB} is shown in Figure 4-7 along with the simulation result. This simulation was conducted by the SpectreRF Periodic AC analysis (PAC), which includes the dynamic effects of the chopping and the SC-NF [17]. The two plots are reasonably correlated, which validates the analysis in this subsection.

4.3.2 Residual Ripple

Similar to auto-zeroing, the ACFB suffers from a correction voltage error $V_{correrr}$ due to the finite loop gain A_{vACFB} and the charge injection mismatch. Similar to Equation (2-6), $V_{correrr}$ is expressed as:

$$V_{correrr} \approx \frac{1}{1+A_{vACFB}}\left(\frac{G_{m1}}{G_{mnull}}V_{os1} \pm V_{os,null}\right) \pm \frac{\Delta q_{NF}}{C_{NF1-4}+C_{NF,5,6}}, \qquad (4\text{-}6)$$

where V_{os1} and V_{osnull} are the initial offsets of G_{m1} and G_{mnull}, respectively, while Δq_{NF} is the charge injection mismatch in the SC-NF. Additionally, a sampled noise charge (e.g. *kTC* noise) is added along with Δq_{NF}. For convenience, $V_{correrr}$ can be referred back to the input of G_{m1} (V_{Gm1err}) by multiplying G_{mnull}/G_{m1}, resulting in:

$$V_{Gm1err} \approx \frac{1}{1+A_{vACFB}}\left(V_{os1} \pm \frac{G_{mnull}}{G_{m1}}V_{osnull}\right) \pm \frac{G_{mnull}}{G_{m1}}\frac{\Delta q_{NF}}{C_{NF1-4}+C_{NF5,6}}. \qquad (4\text{-}7)$$

The initial offset V_{os1} is reduced by a factor equal to the loop gain A_{vACFB}, if the charge injection error is sufficiently reduced by decreasing G_{mnull} relative to G_{m1}. This residual error voltage will be up-modulated by CH_{OUT} and become the output ripple, the amplitude of which can be obtained by replacing V_{os1} with V_{Gm1err} in Equations (2-11) and (2-12).

As suggested in Equation (4-4), the loop gain A_{vACFB} decreases due to the presence of the local feedback around G_{m2} and G_{m3}. Moreover, unlike [14], charge injection mismatch and sampled noise Δq_{NF} are added due to the sampling action in the SC-NF. Therefore, the ACFB will result in a larger residual ripple amplitude and a larger noise PSD peak than the RRL in [14].

4.3.3 Residual Offset

The combined input offset voltage of G_{m2} and G_{m4} (V_{os2} and V_{os4}) appears at the input of G_{m2}. In conjunction with a finite voltage gain of G_{m1} (A_{v1}), it will cause a residual offset $V_{os,res}$:

$$V_{os,res} = \frac{1}{A_{v1}}\left(V_{os2} + \frac{G_{m4}}{G_{m2}}V_{os4}\right). \quad (4\text{-}8)$$

Furthermore, since G_{msense} is coupled to the input of G_{m2}, it converts this offset into a current along with its own input offset $V_{os,sense}$. Similar to the case of the desired input DC signals discussed in Section 4.2.3, this current is up-modulated by CH_{ACFB} and generates a triangular ripple voltage, the amplitude $V_{NF,rip}$ of which is given by:

$$V_{NF,rip} = \frac{G_{msense}}{4 f_{CH} C_{NF1-4}}\left(V_{os2} + \frac{G_{m4}}{G_{m2}}V_{os4} + V_{os,sense}\right). \quad (4\text{-}9)$$

Although this ripple will be filtered by the SC-NF, the ripple amplitude must be small enough not to affect the operation of G_{msense} and not to decrease the DC gain of the G_{msense}, because otherwise the residual output ripple would increase. By applying V_{os2} = 7.0mV, V_{os4} = 6.5mV, $V_{os,sense}$ = 11.0mV, C_{NF1-4} = 7pF, f_{CH} = 50kHz, and the parameters in Table 4-1, $V_{NF,rip}$ will be 75mV. This amplitude can be reduced by decreasing G_{msense} without degrading the primary op-amp specifications such as the in-band noise or the gain bandwidth. Therefore, C_{NF1-4} and f_{CH} can be set relatively low, which will reduce the die size and input bias current. This design flexibility is a key advantage compared to the SC-NF used in [6], where the ripple amplitude is determined by the input transconductor in the main signal path.

4.3.4 Summary

Transient simulations were performed to evaluate the output ripple and residual offset. The transistor-level schematic of Figure 4-5 is applied to unity gain feedback. Table 4-2 shows the sensitivity to each initial error, where one row represents one simulation result. Input offset was added to each transconductor, while coupling capacitance mismatch was added to each switch network. Additionally, a sampling capacitor mismatch was added in the SC-NF. The magnitudes of these initial errors were set to 4.5σ based on the process characterization data. Also, a 1% clock skew was given between the chopping Φ_{CH} and SC-NF Φ_{NF} clocks, although the actual skew was expected to be less.

Table 4-2: Simulated sensitivity to each initial error

	Initial Error	Ripple	Residual Offset
(No Initial Error)	--	0.2 µVrms	0.0 µV
Gm1	6.1 mV	36.0 µVrms	0.2 µV
Gm2	7.0 mV	1.6 µVrms	3.1 µV
Gm4	6.5 mV	2.6 µVrms	5.2 µV
Gm,sense	11.0 mV	1.0 µVrms	0.0 µV
Gm,null	11.6 mV	3.4 µVrms	0.0 µV
CHIN	0.2 fF	1.2 µVrms	0.4 µV
CHOUT	0.13 fF	1.6 µVrms	1.8 µV
CHACFB	0.13 fF	0.6 µVrms	0.0 µV
SC-NF Switches	0.13 fF	0.4 µVrms	0.0 µV
SC-NF Capacitors	1% Mismatch	0.8 µVrms	0.0 µV
SC-NF Clocks	1% Skew	0.3 µVrms	0.2 µV
(All Errors Added)	--	42.9 µVrms	8.3 µV

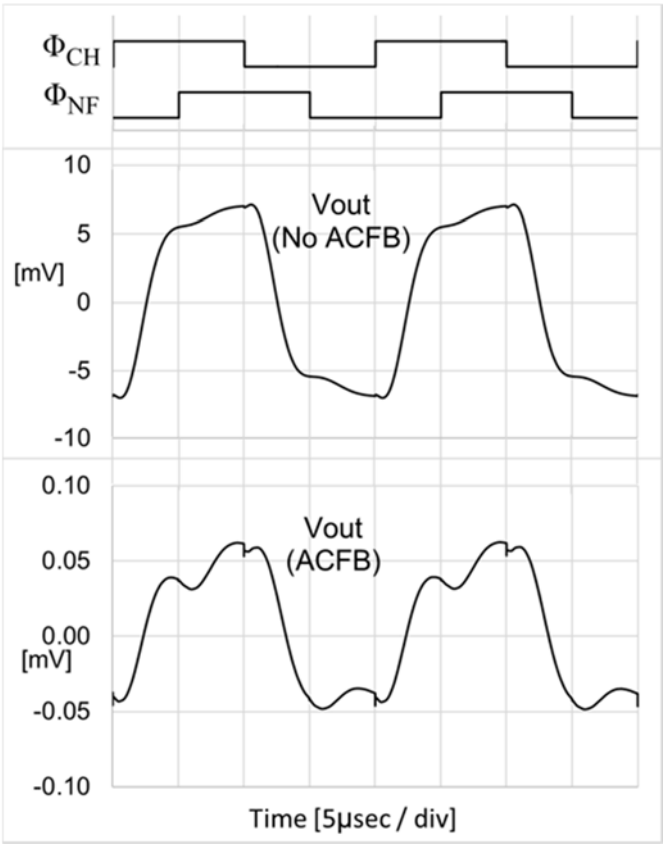

Figure 4-8: Simulated ripple waveforms without and with ACFB

As suggested by Equations (4-7) and (4-8), the initial offset of G_{m1} dominates the residual ripple, while the initial offsets of G_{m2} and G_{m4} dominate the residual offset. Additionally, the charge injection mismatch in CH_{OUT} contributes to the residual offset, as explained in Section 2.4.3. On the other hand, the residual ripple and offset are not sensitive to the errors in the SC-NF including the charge injection mismatch, the sampling capacitor mismatch, and the clock skew, since these errors are suppressed by the ACFB.

The simulation was also performed with all the initial error sources, and the resulting performance is shown in the bottom row in Table 4-2 while the transient waveform is shown in Figure 4-8. The residual ripple and offset are $42.9\mu V_{rms}$ and $7.8\mu V$, respectively. Additionally, the circuit without the ACFB was also simulated for comparison, which resulted in a $5.9mV_{rms}$ residual ripple and a $-43\mu V$ residual offset. By taking the ratio of these two ripple amplitudes, the ripple reduction factor achieved by the ACFB is specified as 42.7dB.

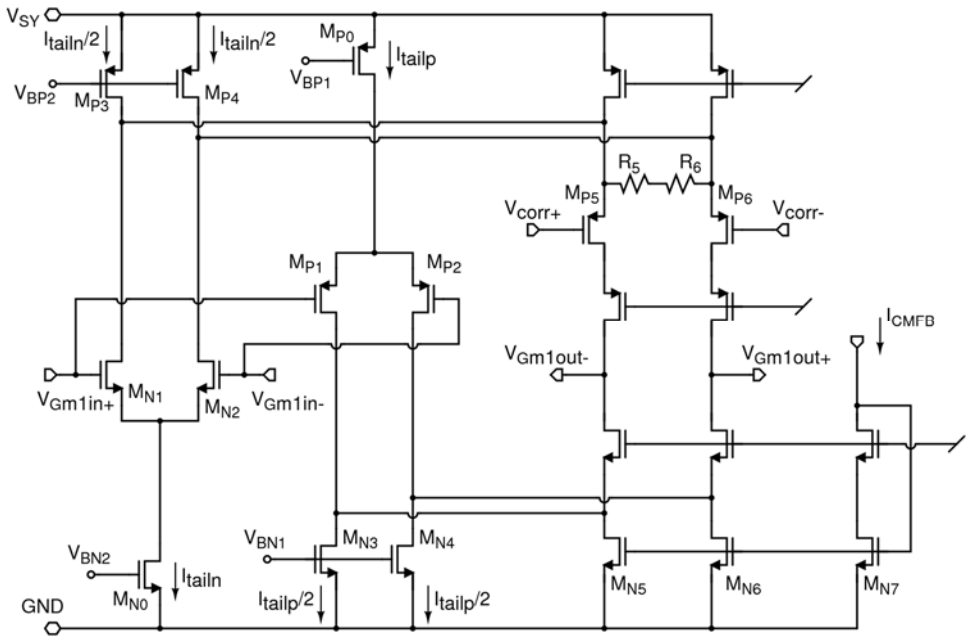

Figure 4-9: The input and null transconductors Gm1 and Gmnull

4.4 Circuit Implementation

4.4.1 Input and Nulling Transconductors

Figure 4-9 presents a circuit diagram of the input and nulling transconductors G_{m1} and G_{mnull}. To achieve a rail-to-rail input common-mode voltage range, G_{m1} consists of two complementary input pairs $M_{P1,2}$ and $M_{N1,2}$ followed by a folded cascode stage. These four input transistors are biased in the weak inversion region ($|V_{GS}| - |V_{TH}| < 30\text{mV}$) to maximize their transconductance for a given bias current [18,19]. Based on the input common-mode voltage V_{CM}, their tail currents I_{tailp} and I_{tailn} are controlled to satisfy $I_{tailp} + I_{tailn} = 0.48\mu\text{A}$. Consequently, the combined transconductance G_{m1} is relatively constant at 7.5μS over its entire rail-to-rail V_{CM} range. On the other hand, the output impedance, hence DC gain of G_{m1}, decreases when the p-channel input pair is in operation (66dB), compared to when the n-channel input pair is in operation (74dB). This is because the output resistance of the current sources $M_{N3,4}$ are lower than that of $M_{P3,4}$. As a result, the residual offset voltage due to the input offset of G_{m2} changes with V_{CM}, which will degrade the CMRR.

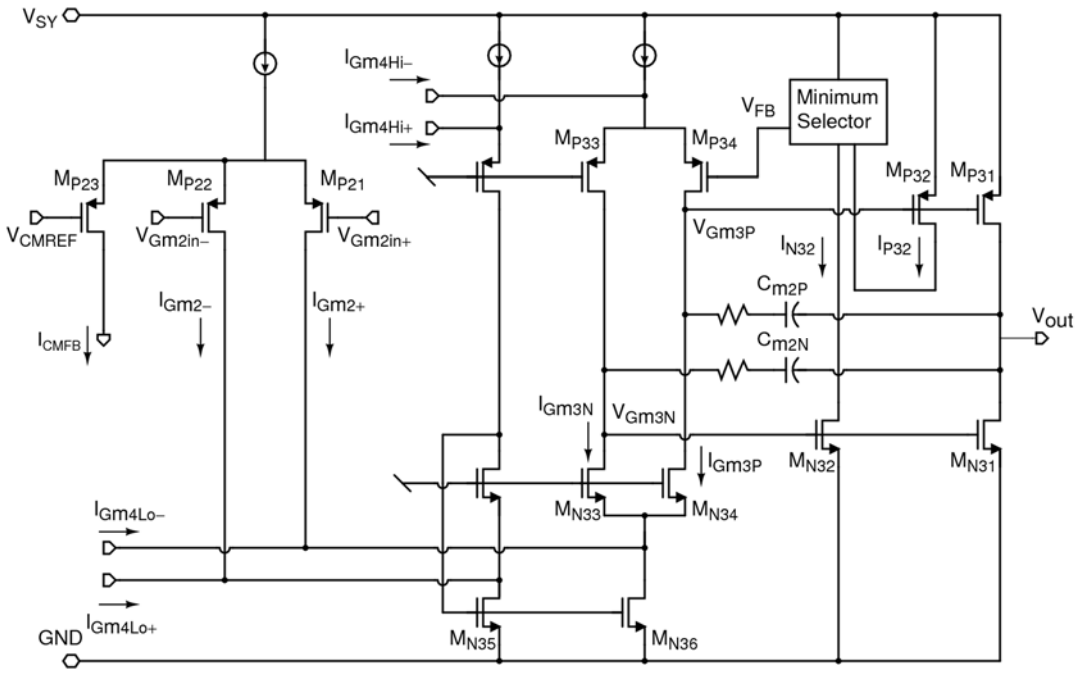

Figure 4-10: The second and output stage transconductors Gm2 and Gm3

G_{mnull} consists of another p-channel pair $M_{P5,6}$ with two degeneration resistors $R_{5,6}$, and is implemented inside of the folded cascode stage to re-use the supply current. $R_{5,6}$ are 2MΩ to set G_{mnull} = 0.5μS, which is 15 times lower than G_{m1}. This will attenuate the errors generated by the SC-NF when referred back to the input, as suggested in Equation (4-7). Furthermore, current signals from the n-channel pair of G_{m1} flow into $M_{P5,6}$ rather than R_1, and thus are not affected by G_{mnull}. As will be shown in the next subsection, the common-mode feedback circuit is implemented with the second transconductor G_{m2}, which results in a feedback current I_{CMFB}.

4.4.2 Second, Output, and Feedforward Transconductors

Figure 4-10 presents a circuit diagram of the second and output stage transconductors G_{m2} and G_{m3}. G_{m2} consists of a p-channel input pair $M_{P21,22}$, and generates differential output currents I_{Gm2+} and I_{Gm2-}. By coupling to M_{P23}, this input pair also works as the common-mode feedback circuit of G_{m1}. The common-mode voltage at the gates of $M_{P21,22}$ is compared with a reference voltage V_{CMREF} = 500mV, and is converted into a feedback current I_{CMFB}.

Similar to G_{m1}, a feedforward transconductor G_{m4} (not shown in Figure 4-10) consists of two complementary input pairs, each of which generates output currents $I_{Gm4Hi+/-}$ and $I_{Gm4Lo+/-}$, respectively. A current mirror $M_{N35,36}$ converts the combined differential currents of G_{m2} and G_{m4} into a single-ended current that further splits into two currents I_{Gm3P} and I_{Gm3N}.

These currents I_{Gm3P} and I_{Gm3N} drive high and low side voltages V_{Gm3P} and V_{Gm3N} in a mesh folded stage, as presented in [20]. These voltages then control high and low side output transistors M_{P31} and M_{N31} to form a class-AB output transconductor G_{m3}. The quiescent current of these output transistors is set to 5 μA by local feedback. Based on one of the replica output currents I_{P32} or I_{N32}, whichever is lower, a minimum selector circuit generates a voltage V_{FB} to adjust the difference of V_{Gm3P} and V_{Gm3N}. This topology can operate below a 1.8 V supply, since it only requires one gate-source voltage plus two drain-source voltages between the supply rails. Two 5pF frequency compensation capacitors $C_{m2P,N}$ together represent C_{m2} in Figure 4-5. When driving a 10 kΩ load, G_{m3} can swing close to each supply rail with 100 mV headroom, while providing a 6dB gain. Combined with the 66dB and 58dB gains of G_{m1} and G_{m2}, respectively, the overall op-amp achieves a 130dB open-loop gain.

4.4.3 Clock Generator

Figure 4-11 presents a block diagram of the clock generator. First, an on-chip oscillator creates a 200kHz master clock Φ_{CLK}. The first D-latch DL_1 then divides down this clock, generating 100kHz complementary clocks with a nearly 50% duty cycle at the Q and QB outputs. Next, the second and third D-latches $DL_{2,3}$ further divide down these complementary clocks, generating two 50kHz clocks with a 90-degree phase difference. A non-overlap clock generator then generates complementary clocks Φ_{CH} and Φ_{CHINV} with a dead time of a few nanoseconds, while another clock generator does the same for complementary clocks Φ_{NF} and Φ_{NFINV}. These dead times avoid shorting the differential nodes with the switches.

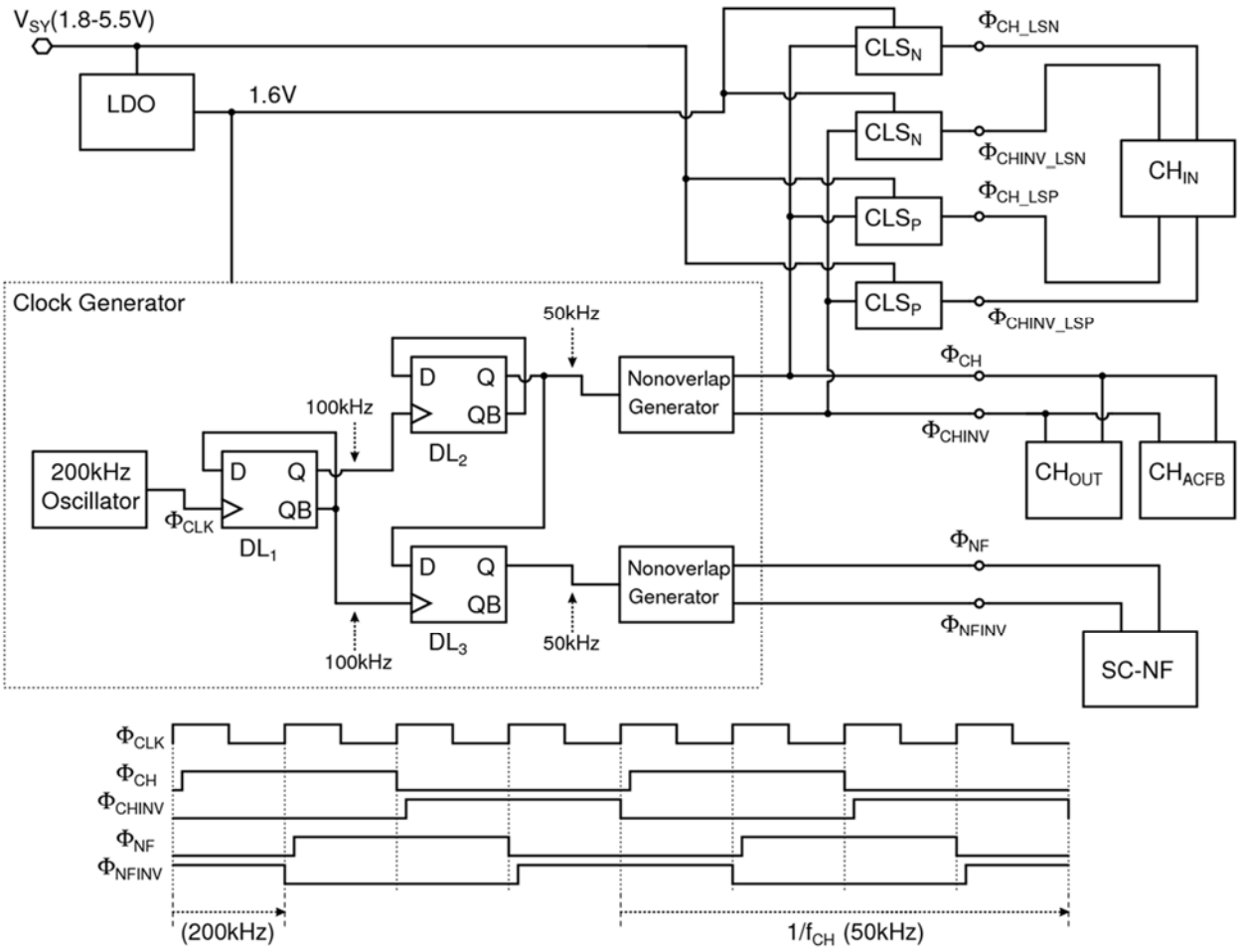

Figure 4-11: Block diagram of the clock generator

The oscillator, D-latches, and non-overlap clock generator circuits all consist of 3V transistors and are supplied by an on-chip 1.6V low dropout (LDO) regulator. This arrangement results in two benefits compared to using 5V transistors directly supplied by an external supply voltage V_{SY}. First of all, the overall die area becomes smaller since a 3V transistor is smaller than a 5V transistor. Second of all, the resulting clock swing is reduced to a 1.6V constant, which decreases the charge injection and eliminates the supply voltage dependency. On the other hand, this clock swing is still sufficiently high to turn on the NMOS switches in CH_{OUT}, CH_{ACFB}, and the SC-NF, since their source potentials are constant at 0.5V.

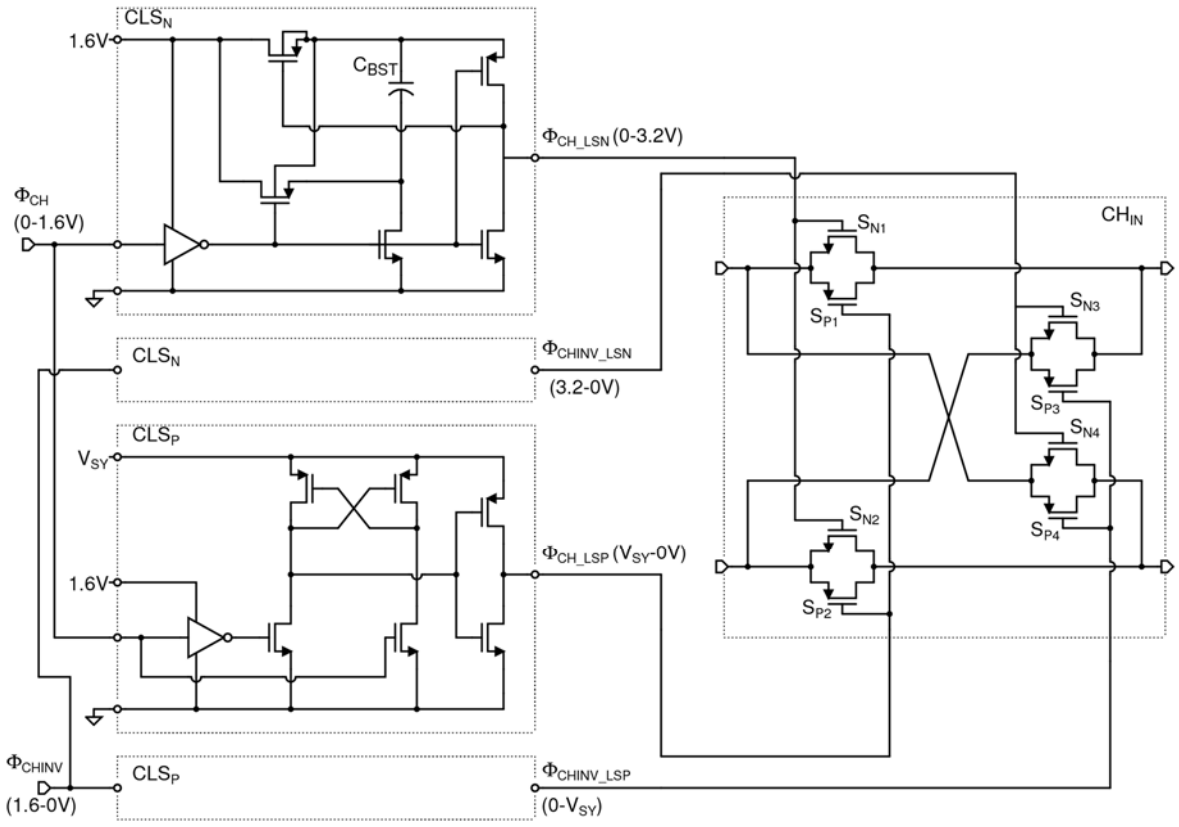

Figure 4-12: Clock level shifters and input chopping circuit

However, the input chopper CH_{IN} must operate with the amplifier's rail-to-rail input common-mode voltage V_{CM} range, and thus requires a higher clock swing to turn on the switches. Figure 4-12 presents a circuit diagram of CH_{IN} along with four clock level shifters CLS_N and CLS_P. CH_{IN} consists of four complementary switches S_{N1-4} and S_{P1-4}. If the clock swing were equal to the supply voltage V_{SY}, neither the NMOS nor the PMOS would receive sufficient overdrive voltage with V_{SY} = 1.8V and V_{CM} = 0.9V. To solve this problem, the clocks of the NMOS switches Φ_{CH_LSN} and Φ_{CHINV_LSN} are boosted by the two clock level shifters CLS_N presented in [21]. A boosting capacitor C_{BST} is pre-charged by the 1.6V LDO, and then it boosts the output clock level to 3.2V. Consequently, the NMOS switches turn on with sufficient overdrive voltage, when V_{CM} is below 2.0V. Additionally, the clocks of the PMOS switches Φ_{CH_LSP} and Φ_{CHINV_LSP} are level shifted to V_{SY} by the other two clock level shifters CLS_P. Consequently, the PMOS switches turn off accordingly with any input common-mode voltage, and turn on with sufficient overdrive voltage when V_{CM} is above 1.6V.

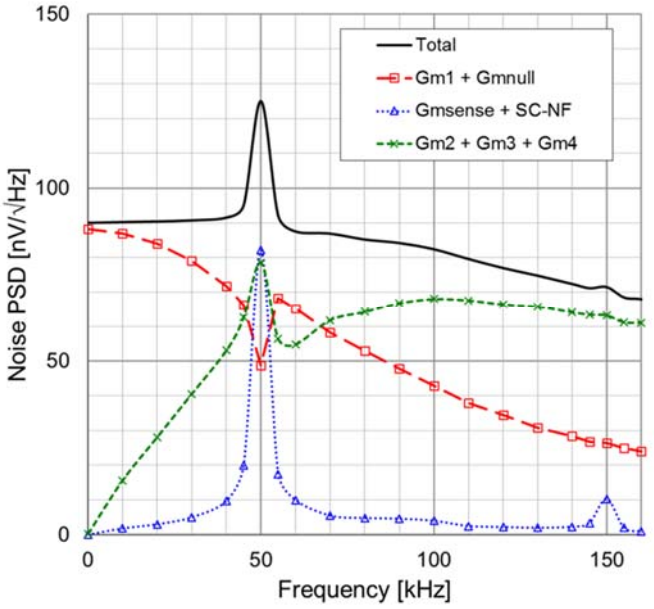

Figure 4-13: Simulated total noise PSD and the contributions from each block

4.4.4 Noise Analysis

Figure 4-13 shows a simulated total input voltage noise PSD along with the contributions from each circuit block. This simulation was performed by the SpectreRF periodic noise analysis to take the chopping and sampling effects into account [17]. The combined down-modulated thermal noise of G_{m1} and G_{mnull} ($e_{n,Gm1}$) dominates the low frequency in-band noise PSD, and is estimated to be:

$$e_{n,Gm1} = \sqrt{8kT\frac{1}{G_{m1}}\left(1+\alpha+\frac{G_{m,null}}{G_{m1}}\right)} \approx 87nV/\sqrt{Hz}\ , \qquad (4\text{-}10)$$

where $\alpha = 0.63$ is the noise contribution of the current sources relative to that of the input pairs, and G_{mnull}/G_{m1} is only 1/15 as explained in Section 4.4.1. The input switches are made sufficiently wide to reduce their combined thermal noise down to 18nV/√Hz. Moreover, the noise of $G_{m2\text{-}4}$ is suppressed by G_{m1} and is therefore negligible in frequencies below 10kHz. This noise contribution increases above the 50kHz chopping frequency, where the gain of the LFP decreases and that of the HFP dominates the overall op-amp.

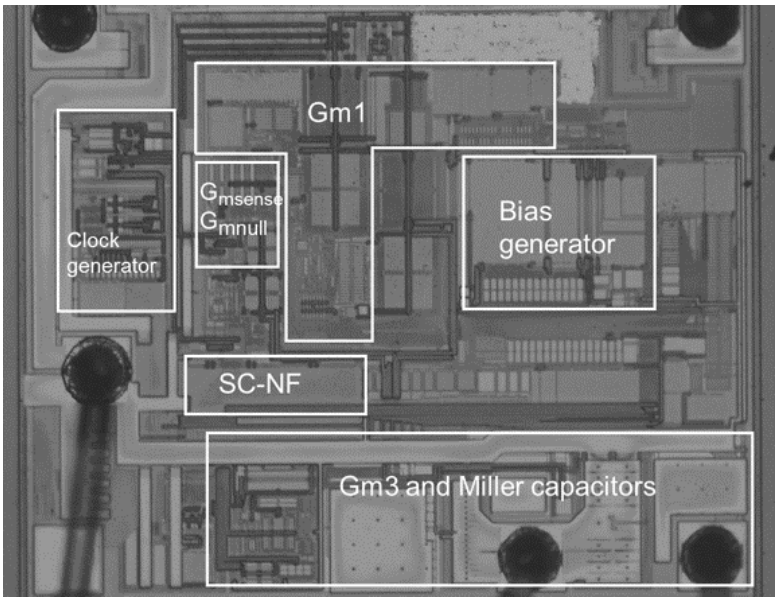

Figure 4-14: Die micrograph of the op-amp

The noise of G_{msense} and the SC-NF are up-modulated, thus resulting in a high noise PSD at the 50kHz chopping frequency. The magnitude of this peak PSD is 125nV/√Hz, which is only increased by a factor of 1.44 ≈√2 compared to the 87nV/√Hz noise floor. Similar to the slow auto-zeroing technique presented in [12], the peak PSD is reduced by setting the loop bandwidth of the ACFB ($f_{u,ACFB}$ = 1.5kHz) much lower than the sampling frequency of the SC-NF. In this case, the overall spectrum at 50kHz will be dominated by the up-modulated residual offset, which is estimated in Table 4-2 but is not included in this noise simulation.

4.5 Measurement Results

The proposed op-amp has been fabricated in a 0.35µm CMOS process augmented by 5V CMOS transistors. Figure 4-14 shows a die micrograph with the entire area, covering 0.64 mm^2, only 8% of which is occupied by the ACFB including G_{msense}, G_{mnull}, and the SC-NF. As described in Section 4.4.3, the clock generator consists of 3V transistors and is supplied by the on-chip 1.6V LDO. All the other circuits consist of 5V transistors and are directly supplied by the external supply. The op-amp only draws 13µA from a 1.8V to 5.5 V supply voltage V_{SY}, and has a rail-to-rail input common-mode voltage V_{CM} range and a –40°C to 125°C temperature range.

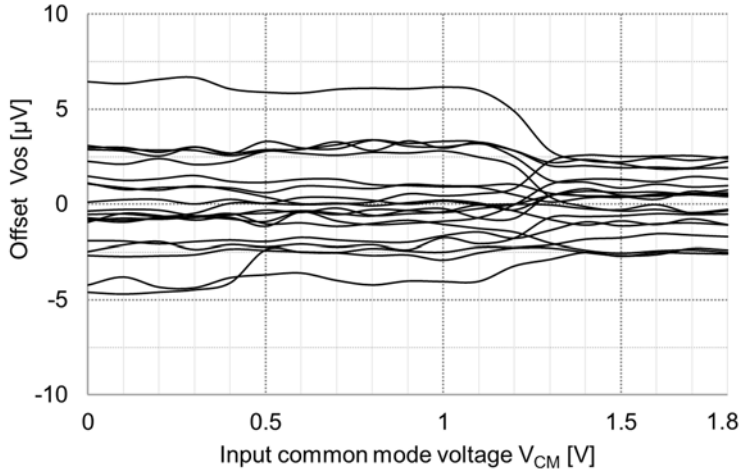

Figure 4-15: Offset voltages over the rail-to-rail V_{CM} range

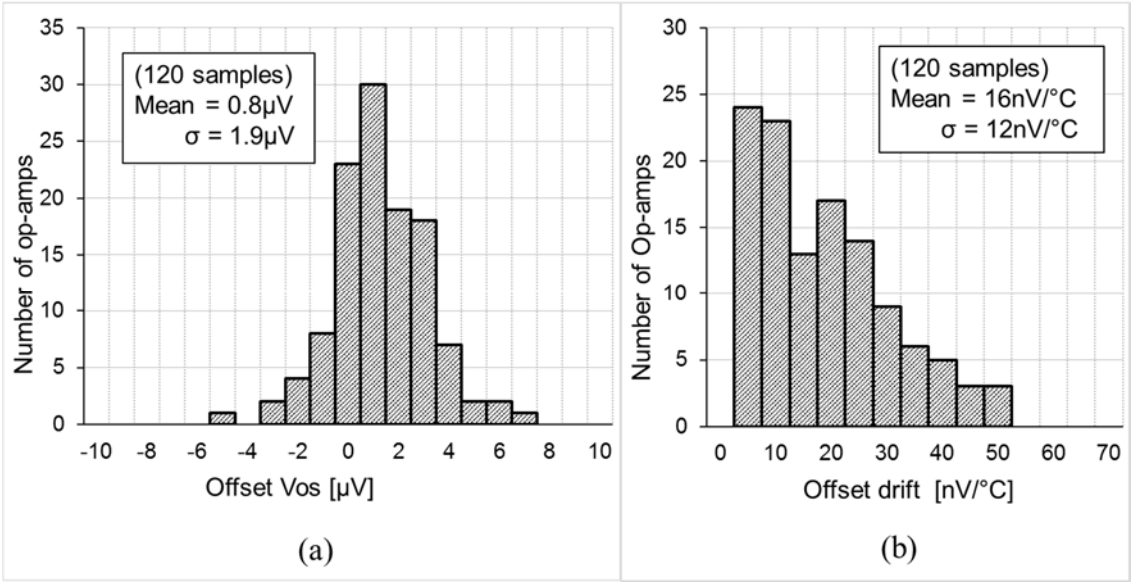

Figure 4-16: Histograms of (a) the offset voltage and (b) the temperature drift

Figure 4-15 shows the input offset voltages of 20 op-amp units over the rail-to-rail V_{CM} range with V_{SY} = 1.8V. The offset increases in the range of V_{CM} = 0 to 1.2V, where the gain of G_{m1} decreases with the p-channel input pair, as explained in Section 4.4.1. In this subsection, the measurement data are obtained with V_{SY} = 1.8V and V_{CM} = 0.9V unless otherwise stated. Figure 4-16 (a) and (b) shows the histograms of the offset voltage and the temperature drift, respectively. The ±6.4µV maximum offset in the histogram is well correlated with the ±7.8µV simulated maximum offset shown in Table 4-2. Offset data are also obtained with V_{SY} = 5.5V and V_{CM} at each supply rail, specifying a 120dB minimum DC PSRR and a 115dB minimum CMRR.

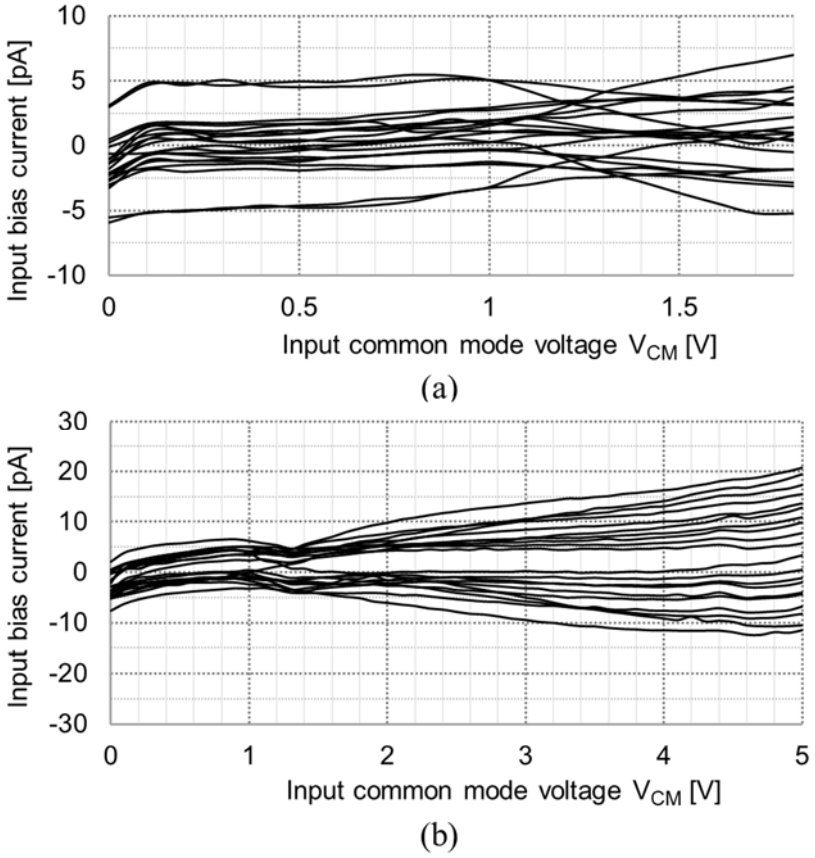

Figure 4-17: Input bias currents (a) with V_{SY}=1.8V and (b) V_{SY}=5V

Figure 4-17 (a) and (b) shows the input bias current of the 20 op-amp units with V_{SY} = 1.8V and 5V, respectively. As explained in Section 2.4.3, this current is generated by the charge injection mismatch in the input chopper. With V_{SY} = 1.8V, the worst-case is lower than ±7.5pA. With V_{SY} = 5V, on the other hand, the current is proportional to V_{CM} up to ±20pA, because the channel charge injection mismatch of the PMOS switches increases with the overdrive voltages. Moreover, the size of the PMOS switches is larger than that of the NMOS switches to compensate for the lower mobility of holes compared to electrons.

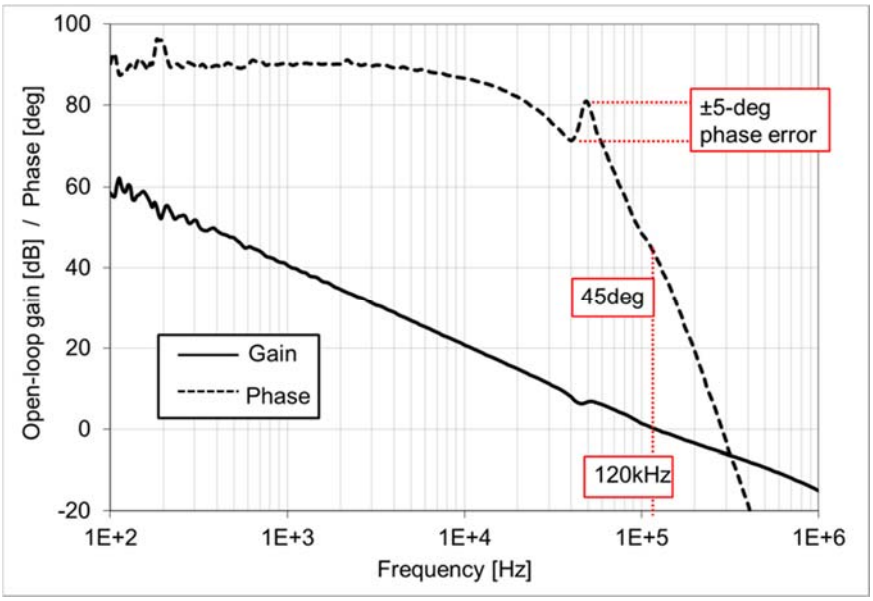

Figure 4-18: Open-loop gain and phase

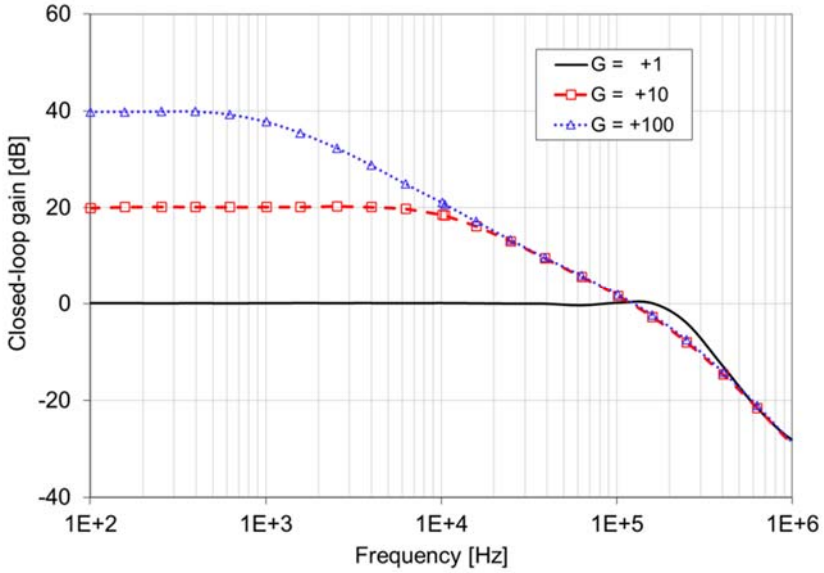

Figure 4-19: Closed-loop gain

Figure 4-18 shows the open-loop gain and phase with a 100pF load capacitor. It can be seen that the op-amp achieves a 120kHz unity gain bandwidth and a 45-degree phase margin. With a 50pF load capacitor, the phase margin improves up to 52 degrees. The notch created by the ACFB is somewhat buried by the HFP, although it still shows a 10-degree phase hump at 50kHz due to the frequency response mismatch between the LFP and HFP. Figure 4-19 shows the closed-loop gain response with the resistor gain settings +1, +10, and +100.

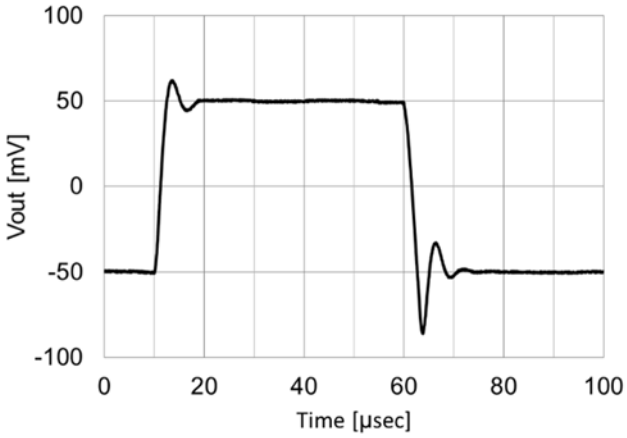

Figure 4-20: Step response with a 100mV signal

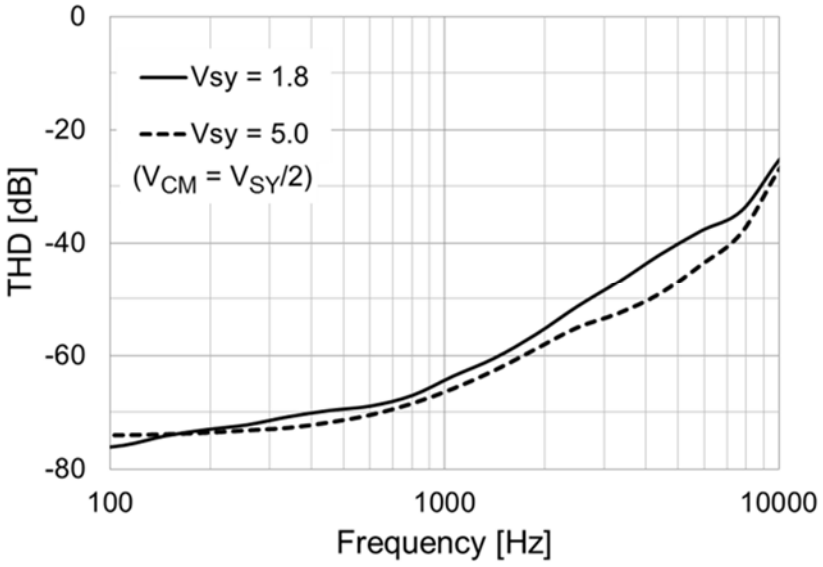

Figure 4-21: THD over the frequency with V_{SY}=1.8V and 5V

Figure 4-20 shows the step response with a 100mV signal, while the op-amp is configured for unity gain and is driving 100pF. Figure 4-21 shows the total harmonic distortion (THD) versus input signal frequency with $1V_{p-p}$ signals, unity gain configuration, and V_{SY} = 1.8V and 5V.

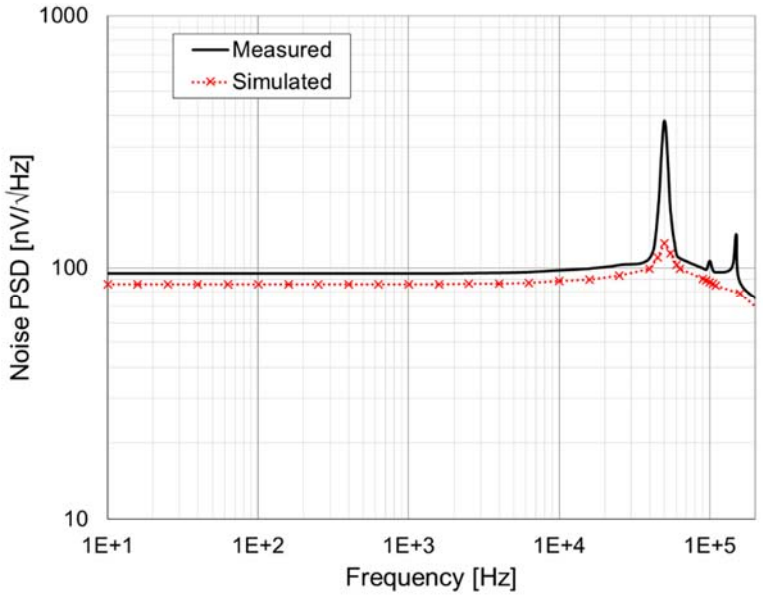

Figure 4-22: Measured and simulated noise PSD

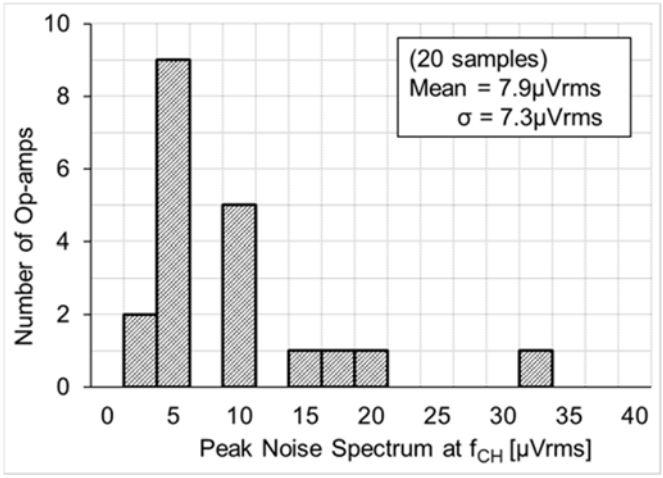

Figure 4-23: Histogram of the peak spectrum at the chopping frequency

Figure 4-22 shows the measured noise PSD with a unity gain configuration along with the simulation result from the SpectreRF periodic noise analysis. The 95nV/√ Hz measured low frequency in-band noise PSD is reasonably correlated with the 86nV/√ Hz simulated one. On the other hand, the 380nV/√ Hz peak PSD at the 50kHz chopping frequency is much higher than the 125nV/√Hz simulated one. As explained in Section 4.3.2, this peak spectral noise is dominated by the up-modulated residual offset, which was not included in the simulation. Therefore, it differs for each op-amp unit as shown in the histogram in Figure 4-23. Here, the peak ripple amplitude is measured at the chopping frequency instead of evaluating the magnitude of the

Table 4-3: Comparison with other state-of-the-art

	This work	Witte [4]	Burt [6]	Belloni [9]	Tang [10]	Fan [14]
Year	2009	2006	2006	2010	2002	2010
V_{SY} min [V]	1.8	5.0	1.8	1.8	2.7	4.0
I_{SY} [µA]	13	700	17	14.4	800	143
f_{CH} [kHz]	50	32	125	500	15	30
Vos max [µV]	10.0	3.0	10.0	5.0	5.0	1.0
Ibias max [pA]	±50	** NS	±200	** NS	±100	±110
CMRR min [dB]	105	** NS	106	124	115	137
GBW [MHz]	0.12	1.37	0.35	* 0.26	2.5	1.8
en [nV/√Hz]	95	15	55	37	20	10.5
NEF	13.2	15.3	8.7	5.5	21.8	4.8
GBW/Isy	9.2	2	20.6	18	3.1	12.6
Die area [mm^2]	0.64	3.6	0.7	1.14	0.67	1.8
Ripple reduction technique	ACFB	Active Filter	SC-NF	Chop + CDS	Auto-Zero	RRL

* Conditionally stable op-amp, ** NS = Data Not Shown

power spectral density (PSD), to simplify the comparison with the simulation. Out of the 20 op-amp units, the worst-case ripple magnitude is $32\mu V_{rms}$, while the simulated worst-case ripple is $42\mu V_{rms}$ as shown in Table 4-2.

The overall specified performance is summarized in Table 4-3, and is compared with other state-of-the-art low power chopper op-amps. The proposed op-amp only draws 13µA from a 1.8V supply and occupies a $0.64mm^2$ die area. It also achieves the lowest maximum input bias current of 50pA among the compared op-amps, as well as a competitive 10µV maximum offset.

4.6 Conclusions

This chapter proposed auto-correction feedback (ACFB), which reduces the initial offset, and consequently reduces up-modulated ripple. It has been implemented in a low power chopper op-amp that targets portable applications. The ACFB senses the ripple at the output of output chopper, and employs a SC-NF in its feedback path to eliminate the up-modulated desired signal in an area efficient manner. As a result, the ACFB only occupies 8% of the $0.64mm^2$ die area of

the overall op-amp. On the other hand, its maximum residual ripple of $32\mu V_{rms}$ is relatively large, due to the limited loop gain of the ACFB and to the presence of the charge injection mismatch and sampled noise in the SC-NF. Although it can be attenuated by an external low-pass filter for low frequency applications, it should be improved for applications which require relatively wide signal bandwidth.

Compared to the implementation in [6], which uses a SC-NF in the main signal path, the ACFB requires two extra transconductors to sense the ripple and to null the initial offset, although they only consume 5% of the total current. On the other hand, the ACFB offers flexibility in choosing a relatively low chopping frequency, which reduces the input bias current. Moreover, the sampled noise in the SC-NF is up-modulated and thus does not contribute to the resulting in-band noise PSD.

4.7 References

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Chapter 5

Chopper Op-Amp with Adaptive Clock Boosting Technique[2]

This chapter presents a 5.6nV/√Hz chopper op-amp realized in a 0.35μm CMOS process augmented by 5V CMOS transistors. Additionally, circuit techniques are proposed to relax the design trade-offs between noise PSD, power consumption, die area, and residual offset, as discussed in Chapter 2. Consequently, the op-amp also achieves a 0.5μV maximum offset and a 15nV/°C maximum offset drift over the amplifier's entire rail-to-rail input common-mode voltage range, while drawing 1.4mA from a 2.1-5.5V supply and occupying a die area of 1.26mm^2.

After describing the motivation for the design in Section 5.1, the overall op-amp configuration is presented in Section 5.2. Frequency compensation is realized in a power and area efficient manner by using a current attenuator and a dummy differential output. In addition, the up-modulated ripple is suppressed by the auto-correction feedback (ACFB) technique presented in Chapter 4. In Section 5.3, the circuit design of the transconductors is presented as well as the noise analysis. Section 5.4 discusses the input chopper and the trade-off between noise PSD and residual offset. It then proposes an adaptive clock boosting technique to drive the NMOS input switches over the amplifier's rail-to-rail common-mode voltage range with a constant overdrive voltage. This minimizes their charge injection and eliminates its common-mode voltage dependency, to achieve low noise, low offset, and high CMRR. The measurement results are discussed in Section 5.5, and the chapter ends with a conclusion in Section 5.6.

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[2] This chapter is derived from a journal publication of the author: Y. Kusuda, "A 5.6 nV/√Hz Chopper Operational Amplifier Achieving a 0.5 μV Maximum Offset Over Rail-to-Rail Input Range with Adaptive Clock Boosting Technique", *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2119-2128, Sept. 2016.

5.1 Motivation

As described in Section 1.4.1, precision op-amps are often configured for closed-loop gains higher than hundred in sensor signal conditioning application [1]. In this case, low offset and low in-band noise are required to minimize the total output error. Buffers for precision references or precision DAC outputs described in Section 1.5.2 are another application [2], in which an op-amp with a wide (ideally rail-to-rail) input common-mode range is required. To cover both these applications, such an op-amp should also provide microvolt-level input offset and low in-band noise over a wide supply voltage, input common-mode voltage, and temperature range. While chopping can be applied to reduce the offset and 1/*f* noise, the resulting up-modulated ripple must be reduced to achieve a wide usable signal bandwidth, especially in buffer applications.

Lowering the in-band noise PSD of a chopper op-amp often compromises other specifications. First, the input transconductance must be increased. Consequently, the frequency compensation capacitors, the transconductances of the subsequent stages, or both, need to be increased to maintain stability. This further increases supply current, die area, or both. Second, as explained in Section 2.4.3, the input chopping switches must be made sufficiently wide to reduce their on-resistance and hence their thermal noise, but which will increase residual offset [3,4]. Moreover, when conventional CMOS switches are used, both their charge injection and on-resistance vary with both the supply and the input common-mode voltages. This degrades the worst-case residual offset voltage as well as the CMRR and the PSRR, especially when rail-to-rail input common-mode voltage range is required at low supply voltages.

Most previous chopper op-amps have more than 10nV/√Hz input noise PSDs [5-11], while achieving maximum offsets ranging from 10μV down to 1μV. A 6nV/√Hz conditionally stable chopper op-amp with a 10μV maximum offset was reported in [12,13], in which a multi-pole feedforward compensation technique is used. Later, in [14], a 6.2nV/√Hz chopper op-amp with a 5.5μV maximum offset was realized, with a minimum supply voltage of 2.7V but whose input common-mode voltage range does not include the positive supply rail.

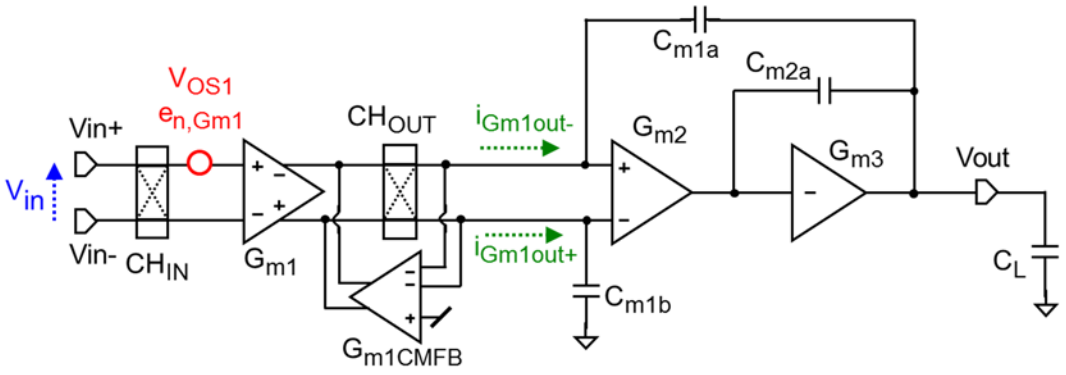

Figure 5-1: A conventional three stage chopper op-amp

5.2 Op-Amp Architecture

5.2.1 Conventional Three Stage Chopper Op-Amp and Frequency Compensation

Many recently designed chopper op-amps consist of three or more gain stages to provide sufficient DC gain [8-13]. Figure 5-1 shows a block diagram of a three stage chopper op-amp consisting of input, second, and output stage transconductors G_{m1}, G_{m2}, and G_{m3}. Additionally, a common-mode feedback transconductor G_{m1CMFB} maintains the output common-mode voltage of G_{m1} stable. Since G_{m1} is chopped by input and output choppers CH_{IN} and CH_{OUT}, the undesired input offset V_{os1} and $1/f$ noise are up-modulated to the chopping frequency f_{CH}. Therefore, below f_{CH}, the resulting in-band noise PSD is primarily dominated by the down-modulated thermal noise PSD of G_{m1} ($e_{n,Gm1}$) without being degraded by the $1/f$ noise. In a proper design, $e_{n,Gm1}$ is dominated by the input differential pair, and is given by:

$$e_{n,Gm1} = \sqrt{\frac{8kT}{G_{m1}}(1+\alpha)}\,, \qquad (5\text{-}1)$$

where G_{m1} is the transconductance of the input pair, and α represents the noise contribution of the load current sources relative to that of the input pair. Additionally, the thermal noise coefficient of the MOSFET (γ) is assumed to be unity, because the input devices will be biased

in the weak inversion region ($|V_{GS}| - |V_{TH}| < 30\text{mV}$) to maximize their transconductance for a given bias current [8-11].

In the time domain, the differential output currents of G_{m1} ($i_{Gm1out+}$ and $i_{Gm1out-}$) will include both a signal component $v_{in}(t)$ and a noise component $e_{n,Gm1}(t)$:

$$i_{Gm1out+}(t) = +\frac{G_{m1}}{2} v_{in}(t) + \frac{G_{m1}}{2} e_{n,Gm1}(t) \qquad (5\text{-}2)$$

$$i_{Gm1out-}(t) = -\frac{G_{m1}}{2} v_{in}(t) - \frac{G_{m1}}{2} e_{n,Gm1}(t) \qquad (5\text{-}3)$$

Note that the common-mode noise at the output of G_{m1} is cancelled by G_{m1CMFB}, so that $e_{n,Gm1}$ complementarily contributes to $i_{Gm1out+}$ and $i_{Gm1out-}$. Although G_{m1CMFB} itself generates common-mode noise at the output of G_{m1}, this noise will be rejected by G_{m2} with its high CMRR.

Nested Miller frequency compensation is realized by capacitors C_{m1a}, C_{m1b}, and C_{m2a}, while C_L is an external load capacitor. According to [15], the unity gain bandwidth f_u, second pole f_{p2}, and third pole f_{p3} of the op-amp are given by:

$$f_u = \frac{G_{m1}}{2\pi \cdot C_{m1a,b}} \qquad (5\text{-}4)$$

$$f_{p2} = \frac{G_{m2}}{2\pi \cdot C_{m2a}} \qquad (5\text{-}5)$$

$$f_{p3} = \frac{G_{m3}}{2\pi \cdot C_L} \ . \qquad (5\text{-}6)$$

These pole frequencies should satisfy $f_{p3} \geq 2 f_{p2} \geq 4 f_u$, to obtain a 60-degree phase margin, and to maintain the stability. However, to reduce the thermal noise in Equation (5-1), G_{m1} must be significantly increased due to the square root relation, resulting in a much higher f_u. Consequently, G_{m2} and G_{m3} must be increased as well to maintain the stability, which further increases the overall current consumption. Alternatively, $C_{m1a,b}$ can be increased to reduce f_u at the cost of die area.

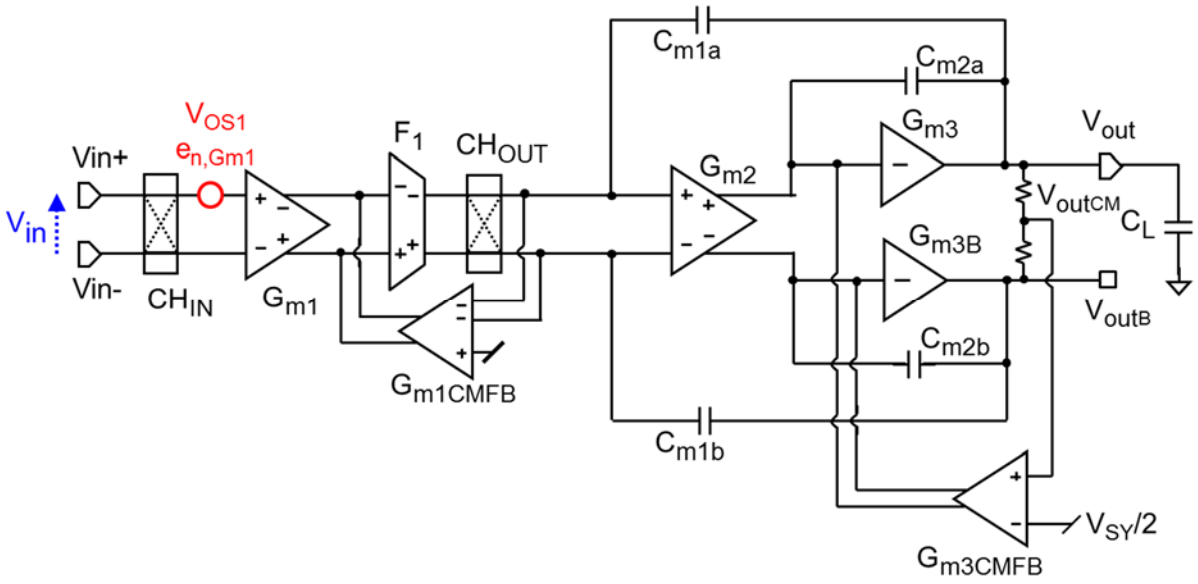

Figure 5-2: Proposed frequency compensation technique implemented in the three stage op-amp

5.2.2 Frequency Compensation Using a Current Attenuator and a Dummy Differential Output

Instead of increasing the capacitor size, the unity gain bandwidth can be reduced by attenuating the output current of G_{m1}. Based on Figure 5-1, a simple change that could be made is to ground the inverting input of G_{m2} and remove C_{m1b}, so that half of the output current signal of G_{m1} is thrown away and the area of C_{m1b} is saved. However, this method will create an impedance mismatch at the output of CH$_{OUT}$, which will increase its charge injection mismatch and hence residual offset [4].

Figure 5-2 presents the proposed frequency compensation technique, incorporating a current attenuator F_1 after G_{m1}. Additionally, a dummy output transconductor G_{m3B} is added to drive a dummy output voltage V_{outB}. Just as described in Equations (5-2) and (5-3), the differential output signal and noise currents of F_1 are complementary, which complementarily moves the voltages V_{out} and V_{outB}. Therefore, by leaving V_{outB} open, half of the signal is eliminated together with half of the noise, without increasing the overall input referred noise of the op-amp. Moreover, this circuit will keep the differential capacitive impedances at the output of CH$_{OUT}$ almost balanced, and thus reduce the charge injection mismatch of CH$_{OUT}$. The

reduced unity gain bandwidth f_u' is given by:

$$f_u' = \frac{G_{m1} \cdot F_1}{2\pi \cdot C_{m1a,b}} \cdot \frac{1}{2}. \qquad (5\text{-}7)$$

However, the noise of F_1 can significantly contribute to the overall input noise, if the signal is attenuated too much. To avoid this scenario, the proposed design sets $F_1 = 0.25$ and $G_{m1} = 3.2$mS. It also targets $f_u' = 4$MHz to reduce the required current consumption in G_{m2} and G_{m3}. According to Equation (5-7), this then requires $C_{m1a,b} = 16$pF, which would be eight times larger with the conventional circuit shown in Figure 5-1. Based on Equations (5-4), (5-5) and (5-6), the second and third poles are set to $f_{p2} = 8$MHz and $f_{p3} = 16$MHz when driving $C_L = 100$pF. On the other hand, the internal capacitor at V_{outB} is only 10pF, which sets the pole at this node $f_{p3B} = 40$MHz. The difference between f_{p3} and f_{p3B} creates a slight transient response mismatch between V_{out} and V_{outB}. However, it will hardly affect the overall settling of the op-amp, since both of its frequency poles are sufficiently higher than f_u'.

This dummy differential output technique requires additional circuitry, including G_{m3B}, an output common-mode feedback transconductor G_{m3CMFB}, and a capacitor C_{m2b}. G_{m3CMFB} compares the output common-mode voltage V_{outCM} with $V_{SY}/2$ and provides feedback currents to the inputs of G_{m3} and G_{m3B}. This common-mode feedback loop bandwidth can be lower than f_u' without compromising the bandwidth of the overall op-amp, as long as V_{outCM} is not affected by any input signal. This can be achieved by designing F_1 to have fully complementary output currents without any common-mode components. Additionally, the transconductance of G_{m3B} is made four times lower than that of G_{m3}, since it does not drive external loads. The comparison for design parameters in Figure 5-1 and Figure 5-2 will be given in Section 5.3.2 after the detailed noise analysis.

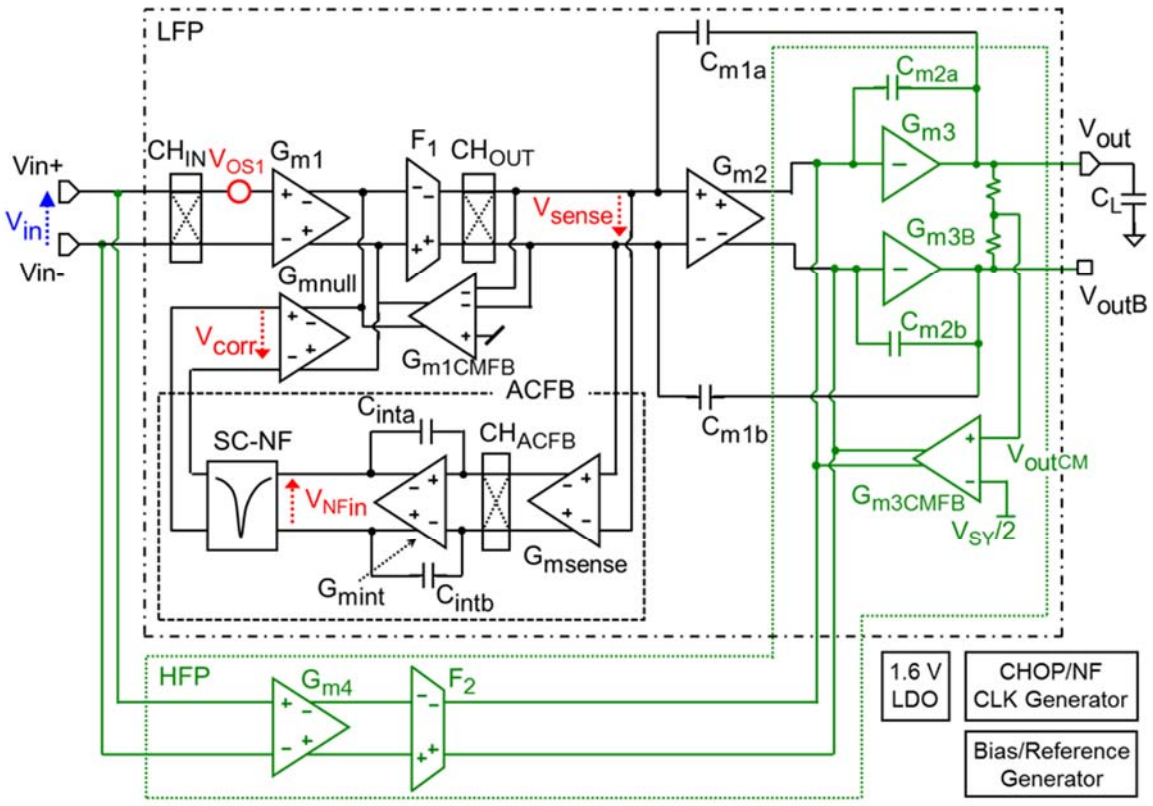

Figure 5-3: Proposed overall op-amp

5.2.3 Overall Op-Amp Employing Auto-Correction Feedback

Figure 5-3 presents a block diagram of the proposed overall op-amp, consisting of a low frequency path (LFP) and a high frequency path (HFP). The LFP is based on the three stage amplifier shown in Figure 5-2, and dominates the gain of the overall op-amp in lower frequencies. The initial offset V_{os1} is up-modulated to the 200kHz chopping frequency f_{CH}. As described in Chapter 4 [11], auto-correction feedback (ACFB) senses the up-modulated ripple at the V_{sense} nodes with a sensing transconductor G_{msense}, down-modulates that ripple with another chopper CH_{ACFB}, forms local feedback, and cancels V_{os1} with a nulling transconductor G_{mnull} to reduce the output ripple. Compared to the ACFB in [11], its loop gain is increased by an active integrator realized by a transconductor G_{mint} and integration capacitors $C_{inta,b}$ in order to reduce the residual ripple. The ACFB creates a notch at the chopping frequency, and then the HFP takes over the overall transfer function, thus burying the notch [10,11].

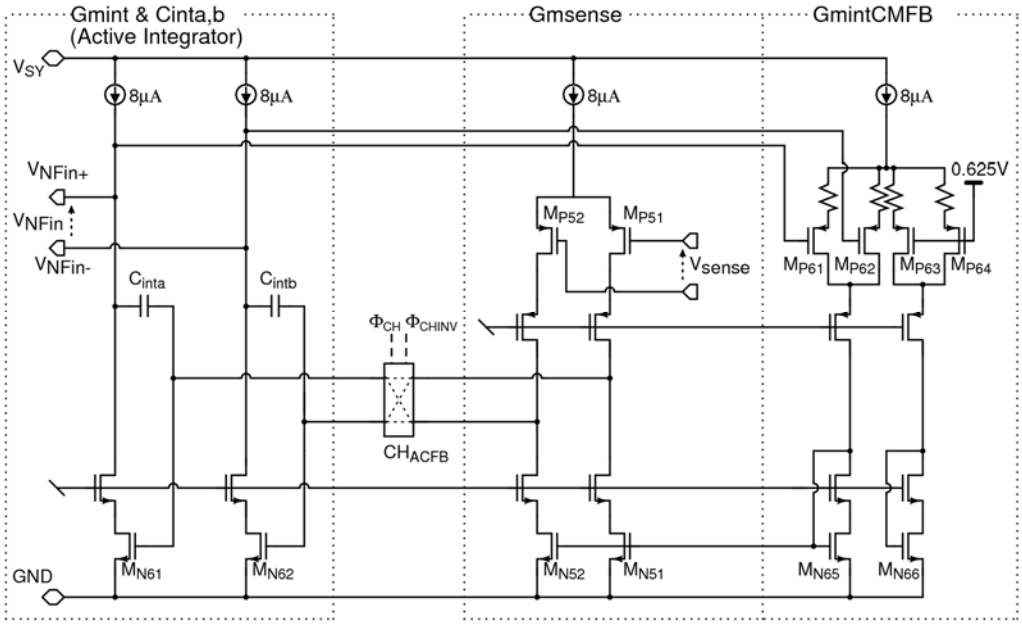

Figure 5-4: The ripple sensing transconductor Gmsense and the active integrator Gmint

5.2.4 ACFB Loop Gain Including Active Integrator

Figure 5-4 presents a circuit diagram of G_{msense}, as well as the active integrator realized by G_{mint} and $C_{inta,b}$. G_{sense} consists of a p-channel input pair $M_{P51,52}$, while G_{mint} consists of a pseudo differential transconductor realized by two common-source transistors $M_{N61,62}$. The common-mode feedback transconductor $G_{mintCMFB}$ consists of four source-coupled PMOS transistors M_{P61-64}, which compare the output common-mode voltage of G_{mint} (V_{NFin+} and V_{NFin-}) with a 0.625V reference, and then adjusts the bias currents of M_{N51} and M_{N52}. M_{P61-64} are de-generated by resistors to expand their differential input range, so that the common-mode voltage of V_{NFin+} and V_{NFin-} can be still detected even in the presence of ripple.

The differential output of G_{mint} (V_{NFin}) drives a switched capacitor notch filter (SC-NF) which consists of the same topology as the one shown in Figure 4-3, but C_{NF1-4} = 1pF and $C_{NF5,6}$ = 2pF are used. The clock timings Φ_{NF} and Φ_{NFINV} operate at the same 200kHz frequency as the chopping clocks Φ_{CH} and Φ_{CHINV} but with a 90-degree phase difference, so that the desired in-band signals are up-modulated by CH_{ACFB} and then rejected by the SC-NF.

As analyzed in Section 4.3.1, the loop gain of the ACFB (A_{vACFB}) can be broken into two

parts $A_{vACFB1} \cdot A_{vACFB2}$; A_{vACFB1} is the gain from the V_{corr} to V_{sense} nodes through G_{mnull} and CH_{OUT}; A_{vACFB2} is the gain from V_{sense} to the output of the SC-NF through G_{msense}, CH_{ACFB}, and the active integrator. A_{vACFB1} is given by the same equation as (4-4), and is estimated to be -20dB. On the other hand, with the addition of the active integrator, the equation for A_{vACFB2} differs from the equation (4-5) and is given by:

$$A_{vACFB\ 2} \approx \frac{G_{msense} \cdot R_{osense}}{1 + 2\pi jf R_{osense} C_{inta,b} (G_{mint} R_{oint})} \cdot \frac{G_{mint} \cdot R_{oint}}{1 + 2\pi jf \cdot \frac{C_{NF\ 1-4}}{G_{mint}}} \cdot \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_{CH}}\right)}{\frac{\pi}{2}\frac{f}{f_{CH}}}, \quad (5\text{-}8)$$

where R_{osense} and R_{oint} are the impedances at the output of G_{msense} and G_{mint}, respectively. The DC gain of $G_{msense} \cdot R_{osense}$ is limited by the dynamic switching conductance of CH_{ACFB}, and is 42dB. On the other hand, that of $G_{mint} \cdot R_{oint}$ is not limited by any switching conductance, and is 60dB. Thus, the DC gain of A_{vACFB2} will be 102dB, which results in 82dB DC gain of A_{vACFB}. The dominant pole of A_{vACFB} will be determined by the Miller capacitors $C_{inta,b}$. One non-dominant pole will be created at $2f_{CH}$ = 400kHz with a significant phase shift due to the sampling action of the SC-NF. Another non-dominant pole is created at the output of the active integrator at $f_{p,int} = G_{mint}/(2\pi \cdot C_{NF1-4})$ = 800kHz. With $C_{inta,b}$ = 8pF, the unity gain bandwidth of the ACFB $f_{u,ACFB}$ is set to 50kHz below the non-dominant poles. This bandwidth is still sufficiently high to reduce the 1/*f* noise of G_{m1}, the corner frequency of which is 5kHz.

As explained in the equation (4-7), the residual error referred to the input of G_{m1} (V_{Gm1err}) is given by:

$$V_{Gm\ 1err} \approx \frac{1}{A_{vACFB}} \left(V_{os\ 1} \pm \frac{G_{mnull}}{G_{m\ 1}} V_{osnull} \right) \pm \frac{G_{mnull}}{G_{m\ 1}} \frac{\Delta q_{NF}}{C_{NF\ 1-4} + C_{NF\ 5,6}}. \quad (5\text{-}9)$$

where V_{os1} and V_{osnull} are the initial offsets of G_{m1} and G_{mnull}, respectively, and Δq_{NF} is the combination of noise charge and charge injection mismatch sampled by C_{NF1-4} in the SC-NF. This residual error will be up-modulated by CH_{OUT} and become the output ripple. After suppression by A_{vACFB} = 82dB, the contribution of the initial offset V_{os1} = 1mV to the residual error V_{Gm1err} is reduced to only 0.08μV. However, the sampled noise charge Δq_{NF} will still

dominate the noise PSD peak at the chopping frequency f_{CH}, even though it will be attenuated by G_{mnull}/G_{m1} = 1/40. This sampled noise is particularly dominated by the thermal noise of G_{mint} which is not band-limited by $C_{inta,b}$ but only by C_{NF1-4}. Moreover, C_{NF1-4} = 1pF is relatively low to push $f_{p,int}$ to a higher frequency. In summary, while the newly added G_{mint} decreases the residual ripple due to the initial offset of G_{m1}, it will add to the up-modulated sampled noise. Overall, this op-amp achieves a 62nV/√Hz maximum noise PSD peak at f_{CH}, which is an improvement on the 820nV/√Hz achieved in Chapter 4.

5.2.5 High Frequency Path (HFP)

The HFP consists of a feedforward transconductor G_{m4} and a current mirror F_2. In addition, output transconductors G_{m3}, G_{m3B}, and G_{m3CMFB} are shared by the LFP and HFP. The unity gain bandwidth of the HFP f_u'' is given by:

$$f_u'' = \frac{G_{m4} \cdot F_2}{2\pi C_{m2a,b}} \cdot \frac{1}{2}. \qquad (5\text{-}10)$$

This must be matched to that of the LFP f_u', otherwise a pole-zero doublet and hence phase error would be introduced into the overall signal transfer function. To achieve this, G_{m1} and G_{m4} employ the same transconductor topology, and capacitors $C_{m1a,b}$ and $C_{m2a,b}$ are laid out identically. Nevertheless, there will be up to ±2% bandwidth mismatch due to the random variation in each transconductance and capacitance, which will result in a phase error of up to ±4 degrees. While F_2 is unity, G_{m4} is set four times smaller than G_{m1} to reduce the amount of current consumed. The noise PSD of G_{m4} will be suppressed by the LFP in frequencies lower than f_{CH}. Since G_{m2} and G_{m4} are not chopped, their input offsets V_{os2} and V_{os4} cause a residual offset V_{os_res} in conjunction with the finite voltage gain of G_{m1} and F_1 (A_{v1}):

$$V_{os\_res} = \frac{V_{os2} + V_{os4}\dfrac{G_{m4}}{G_{m2}}}{A_{v1}}. \qquad (5\text{-}11)$$

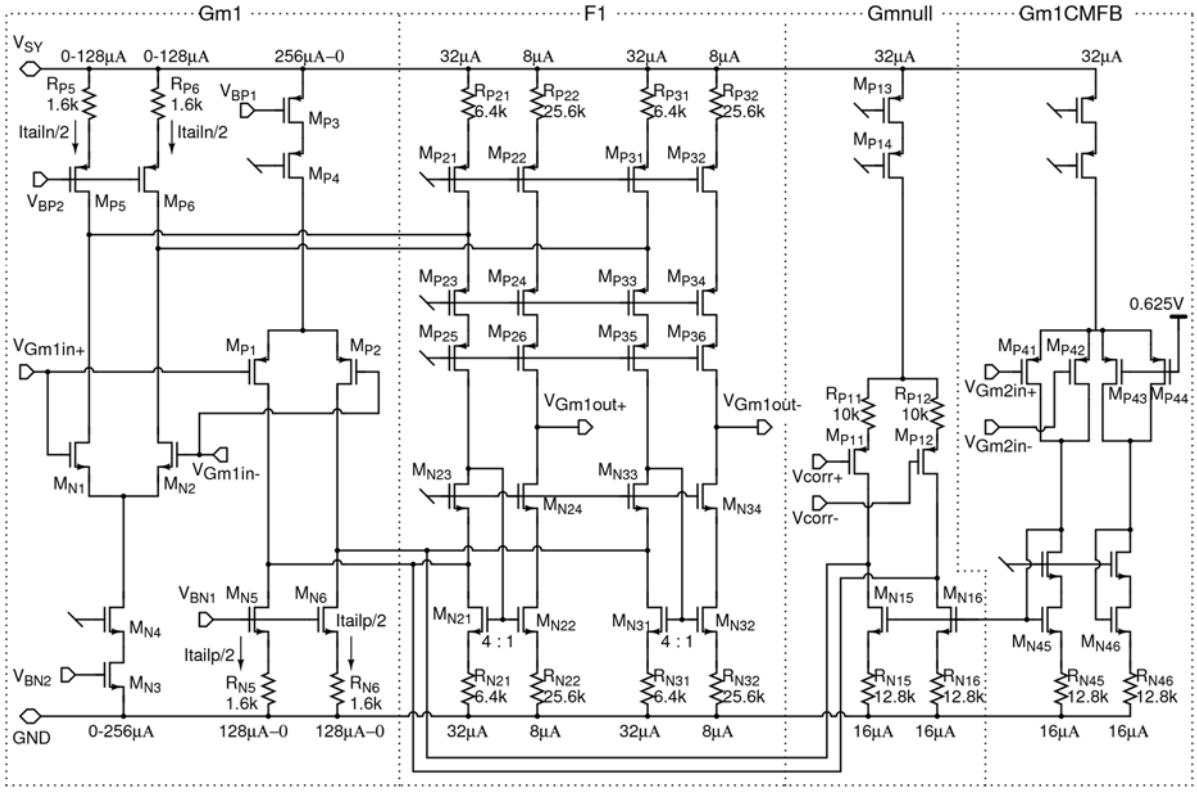

Figure 5-5: The input and null transconductors Gm1 and Gmnull, and the current attenuator F1

5.3 Transconductor Circuits

5.3.1 Input and Nulling Transconductors with the Current Attenuator

Figure 5-5 presents a circuit diagram of the input and nulling transconductors G_{m1} and G_{mnull}, as well as the current attenuator F_1. G_{m1} consists of complementary p-channel and n-channel input pairs $M_{P1,2}$ and $M_{N1,2}$ biased in the weak inversion region. Their tail currents I_{tailp} and I_{tailn} are controlled to maintain $I_{tailp} + I_{tailn} = 256\mu A$, by adjusting bias voltages $V_{BP1,2}$ and $V_{BN1,2}$ based on V_{CM}. This results in a relatively constant transconductance of 3.2mS over the rail-to-rail input common-mode voltage V_{CM} range. G_{mnull} consists of another p-channel pair $M_{P11,12}$ with degeneration resistors $R_{P11,12}$ to set the transconductance to only 80µS, 40 times lower than that of G_{m1}. As suggested by Equation (5-9), this attenuates errors generated at the output of the SC-NF when referred back to the input of G_{m1}. A 1mV worst-case offset of G_{m1} then results in a correction voltage V_{corr} of 40mV which is still within the operating range of G_{mnull}. F_1 is realized

by two 4:1 current mirrors $M_{N21,22}$ and $M_{N31,32}$. The common-mode feedback transconductor G_{m1CMFB} consists of four source-coupled PMOS transistors $M_{P41\text{-}44}$, which compare the output common-mode voltage after the output chopper (V_{Gm2in+} and V_{Gm2in-}) with a 0.625V reference, and then adjusts the bias currents of M_{N15} and M_{N16}. The current sources and mirrors $M_{N5,6}$, $M_{P5,6}$, $M_{P11,12}$, $M_{N15,16}$, $M_{N21,31}$, $M_{P21,31}$, $M_{N22,32}$ and $M_{P22,32}$ are degenerated by resistors $R_{N5,6}$, $R_{P5,6}$, $R_{P11,12}$, $R_{N15,16}$, $R_{N21,31}$, $R_{P21,31}$, $R_{N22,32}$ and $R_{P22,32}$, respectively, to reduce their current noise.

5.3.2 Noise Analysis and Optimization

Based on Equation (5-1), the combined thermal noise PSD of G_{m1}, G_{mnull}, and F_1 ($e_{n,Gm1}'$) is given by:

$$e_{n,Gm1}{}' = \sqrt{\frac{8kT}{G_{m1}}\left(1+\alpha_1+\frac{\alpha_2}{F_1^{\,2}}\right)}, \qquad (5\text{-}12)$$

where α_1 and α_2 are the noise contributions of current sources relative to that of the input pairs of G_{m1}. α_1 represents the combined noise of $M_{N5,6}$, $M_{P5,6}$, $M_{P11,12}$, $M_{N15,16}$, $M_{N21,31}$, $M_{P21,31}$, $R_{N5,6}$, $R_{P5,6}$, $R_{P11,12}$, $R_{N15,16}$, $R_{N21,31}$, and $R_{P21,31}$, while α_2 represents that of $M_{N22,32}$, $M_{P22,32}$, $R_{N22,32}$ and $R_{P22,32}$. Because of the current signal attenuation, α_2 has a high noise gain of $1/F_1^2 = 16$. Therefore, while α_1 is set to 0.33, α_2 is set to 0.02 by increasing each of $R_{N22,32}$ and $R_{P22,32}$ to 25.6kΩ. Their bias current is set to only 8μA to keep the IR drop at an acceptable level with a 2.1V supply at the expense of slew rate performance.

Figure 5-6 shows the noise contributions of the input differential pairs of G_{m1} and the current sources α_1 and α_2, as well as the total noise of the circuit shown in Figure 5-5. In the figure, the current attenuation factor $1/F_1$ is varied, so that α_2 changes. The proposed design selects $1/F_1 = 4$ ($F_1 = 0.25$), resulting in the 4.1nV/√Hz total noise $e_{n,Gm1}'$, which is 30% higher than the 3.2nV/√Hz noise contribution of the input pairs due to the noise from the current sources. Besides, compared to the 3.7nV/√Hz total noise in the case of $1/F_1 = 1$ (no attenuation), it is only increased by 11%. On the other hand, if $1/F_1$ were set above 7, the total noise would be dominated by α_2 and significantly increased.

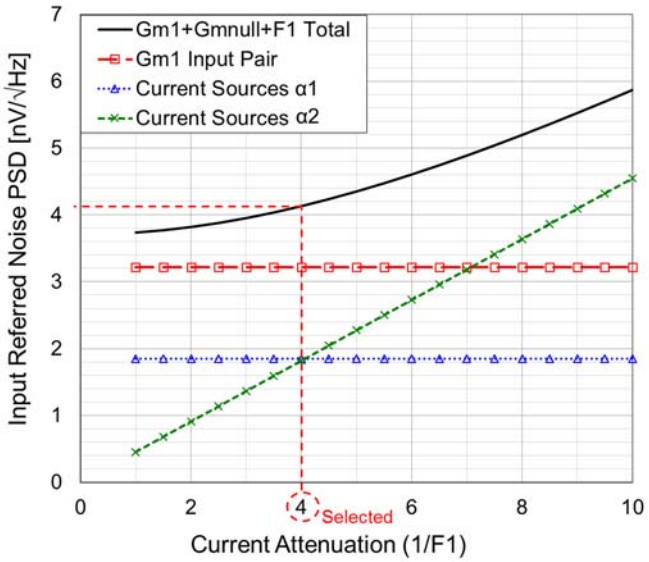

Figure 5-6: Noise contributions of the current sources versus current attenuation

Table 5-1: Design parameter comparison between Figures 5-1 and 5-2

	Figure 5-1 Increasing current	Figure 5-1 Increasing capacitor	Figure 5-2 Proposed design
G_{m1} [µA] / [mS]	280 / 2.6	280 / 2.6	352 / 3.2
G_{m1CMFB} [µA] / [mS]	32 / 0.35	32 / 0.35	32 / 0.35
F_1 [µA] / [A/A]	--	--	16 / 0.25
G_{m2} [µA] / [mS]	731 / 3.9	214 / 1.14	150 / 0.8
G_{m3} [µA] / [mS]	1755 /48.8	514 / 14.3	360 / 10
G_{m3B} [µA] / [mS]	--	--	90 / 2.5
G_{m3CMFB} [µA] / [mS]	--	--	40 / 0.35
C_{m1a} [pF]	21.3	73	16
C_{m1b} [pF]	21.3	73	16
C_{m2a} [pF]	21.3	16	16
C_{m2b} [pF]	--	--	16
Total Current [µA]	2798	1040	1040
Total Capacitor [pF]	64	162	64
Noise PSD [nV/√Hz]	* 4.1	* 4.1	* 4.1
GBW [MHz]	19.5	5.8	4.0
Slew Rate [V/µs]	9.8	2.8	0.5

* Excluding the noise contribution from the input chopper

To evaluate the effectiveness of the proposed frequency compensation techniques, the design parameters used in Figure 5-2 are listed in Table 5-1, and are compared with those in Figure 5-1. Their noise PSDs are set to the same 4.1nV/√Hz (excluding the contribution from the input chopper), so that the required transconductance of G_{m1} is larger in Figure 5-2 to compensate for the extra noise contribution of F_1. Two design cases are considered in Figure 5-1 to maintain the stability of the overall op-amp: increasing the transconductances hence the

currents of G_{m2} and G_{m3} while maintaining the same total capacitor value as Figure 5-2; or increasing the capacitor size while maintaining the total current same as Figure 5-2. While one case in Figure 5-1 consumes 2798μA of current, the case in Figure 5-2 only consumes 1040μA. While the other case in Figure 5-1 requires 162pF of total capacitor, the case in Figure 5-2 only requires 64pF. However, the slew rate of the proposed circuit in Figure 5-2 is 5.6 times less than the case of increasing the capacitor size in Figure 5-1.

5.3.3 Residual Offset and CMRR Analysis

The degeneration resistors $R_{N22,23}$ and $R_{P22,23}$ also increase the output impedance of F_1 with series feedback. As a result, the combined DC gain of G_{m1} and F_1 (A_{v1}) is mainly limited by the dynamic output conductance due to the output chopping [4], and thus is given by:

$$A_{v1} = \frac{G_{m1} \cdot F_1}{4 \cdot f_{chop} \cdot C_{OUTF\,1}} = 86\,\text{dB}\ , \qquad (5\text{-}13)$$

where C_{OUTF1} = 50fF is the combined drain capacitance of the cascode devices M_{N24}, M_{N34}, M_{P26}, and M_{P36}. This gain is sufficiently high to reduce the offset contribution of G_{m2} and G_{m4}. Based on Equation (5-11), their worst-case offsets $V_{os2} = V_{os4}$ = 2mV together will contribute to the overall offset only by 0.14μV. With the change in the input common-mode voltage, the gain A_{v1} and V_{os2} will be mostly constant, but V_{os4} will change due to the offset mismatch between the two complementary input pairs. When V_{os4} changes from –2mV to +2mV with the 2.1V input common-mode voltage change, the residual offset changes from –0.1μV to +0.1μV, corresponding to the 140dB CMRR.

As discussed in Section 5.2.2, F_1 should not generate common-mode output current to avoid affecting the output common-mode voltage V_{outCM}. This is achieved by setting the output source and sink currents to an equal amount during a large signal response. The maximum output source current is 8μA, which is generated by the PMOS current sources M_{P22} and M_{P23}. The gate of the NMOS cascode devices $M_{N24,34}$ is biased such that the maximum output sink current is limited to the same 8μA.

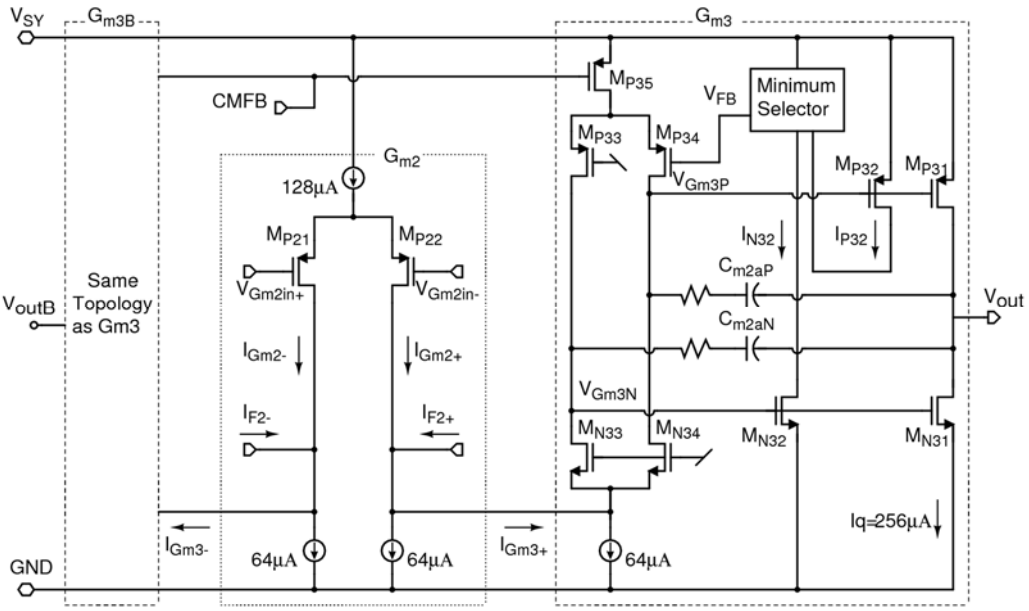

Figure 5-7: The second and output stage transconductors Gm2, Gm3, and Gm3B

5.3.4 Second and Output Transconductors

The feedforward transconductor G_{m4} and the current mirror F_2 use the same topologies as G_{m1} and F_1, to improve the matching of the bandwidth between the LFP and HFP. Figure 5-7 presents a circuit diagram of the second and output stage transconductors G_{m2}, G_{m3}, and G_{m3B}. G_{m2} consists of a p-channel input pair $M_{P21,22}$ and the output currents I_{Gm2+} and I_{Gm2-} are combined with those of F_2 (I_{F2+} and I_{F2-}). One of the combined currents I_{Gm3+} then drives high and low side voltages V_{Gm3P} and V_{Gm3N} in a mesh folded stage [16]. These voltages control high and low side transistors $M_{N31,P31}$ to form a class-AB output transconductor G_{m3}. The quiescent current is set to 256µA by local feedback. Based on one of the replica output currents I_{n32} or I_{p32}, whichever is lower, a minimum selector circuit generates a voltage V_{FB} to adjust the difference of V_{Gm3P} and V_{Gm3N}. This topology can operate below a 2.1V supply, since it only requires one gate-source voltage plus two drain-source voltages between the supply rails. Two 8pF frequency compensation capacitors $C_{m2aP,N}$ together represent C_{m2a} in Figure 5-3. The dummy output transconductor G_{m3B} consists of the same topology as G_{m3}, but the size and bias currents of every transistor are scaled to one-fourth of those in G_{m3}. When driving a 2kΩ load, G_{m3} can swing close to each supply rail with 100mV of headroom, while providing a 10dB gain. Combined with the 86 and 40dB gains of G_{m1} and G_{m2}, respectively, the overall op-amp achieves an open-loop gain of 136dB.

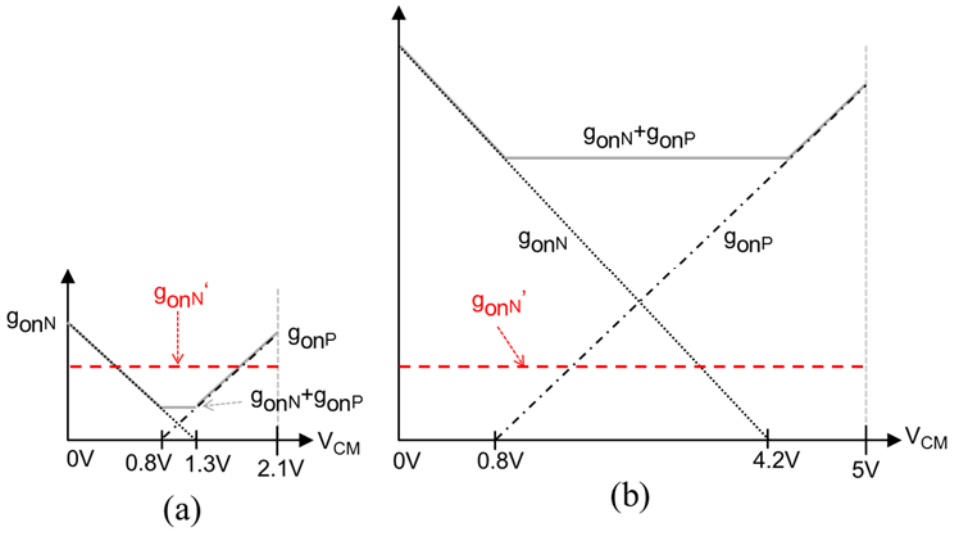

Figure 5-8: On conductances of a conventional CMOS switch $g_{onN}+g_{onP}$ and a NMOS switch with a constant overdrive voltage g_{onN}' (a) with V_{SY}=2.1V and (b) V_{SY}=5V

5.4 Input Chopper

5.4.1 Conventional CMOS Switches

As explained in Section 2.4.3, charge injection mismatch of the input chopping switches causes a residual offset and input bias current [10]. On the other hand, the switches must be made sufficiently wide to reduce the on-resistance and the thermal noise. This requires a trade-off between the in-band noise PSD and the residual offset in chopper op-amp design. Figure 5-8 (a) and (b) shows the on-conductances of an NMOS g_{onN}, a PMOS g_{onP}, and a CMOS switch $g_{onN} + g_{onP}$ over a rail-to-rail V_{CM} range with V_{SY} = 2.1 and 5.0 V, respectively. The PMOS is typically sized three times as wide as the NMOS to compensate for the lower mobility of holes compared to electrons. The on-conductance $g_{onN} + g_{onP}$ is lowest, when V_{SY} is the lowest and V_{CM} is in the middle of V_{SY}. Thus, the switches must be made sufficiently wide to achieve the targeted noise PSD for this voltage condition. Such wide switches are oversized for the other voltage conditions, and thus generate more charge injection. This not only increases the worst-case residual offset over the entire V_{SY} and V_{CM} ranges, but it also degrades the CMRR and the PSRR. This problem can be solved by maintaining the overdrive voltage constant and independent of changes in V_{SY} and V_{CM}, since the on-conductance g_{onN}' will then remain constant as shown in Figure 5-8 (a) and (b).

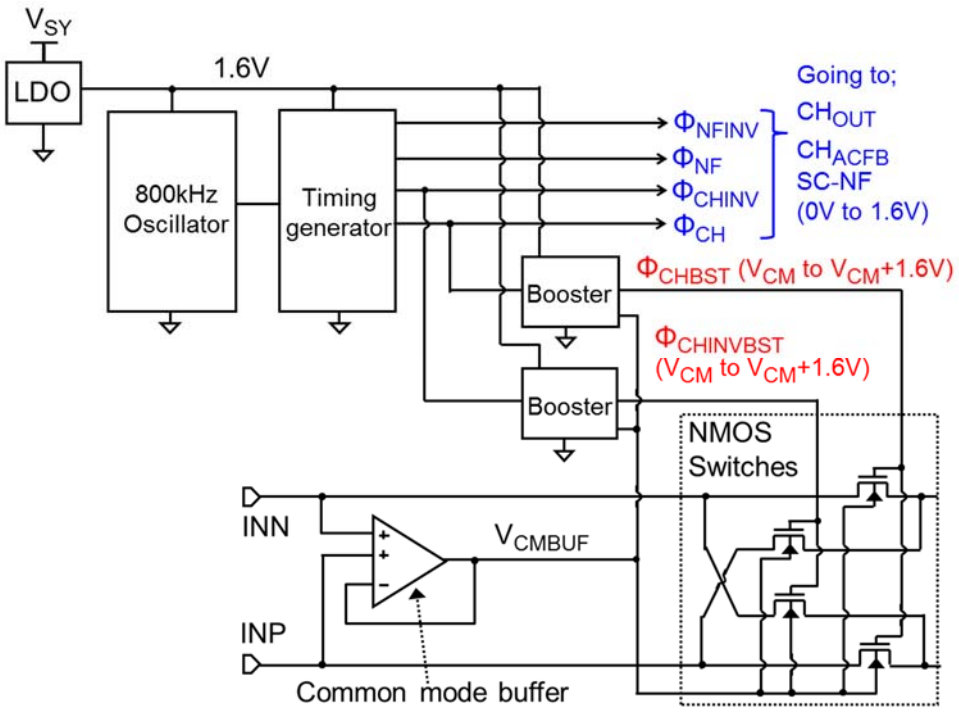

Figure 5-9: The input chopping circuit and clock generator employing an adaptive clock boosting technique

5.4.2 Input Chopper Employing Adaptive Clock Boosting Technique

To maintain the overdrive voltage constant, Abo [17] proposed a bootstrap NMOS switch, the gate of which is driven to $V_{CM} + V_{SY}$ and 0V to turning it on and off, respectively. However, the clock swing and hence the clock feedthrough error still will increase with V_{CM}, which degrades the CMRR. In addition, the bootstrap capacitors must be charged by the input nodes, which will affect the signal source. Later, Fan [18] proposed capacitively-coupled clock boosting technique to maintain both the overdrive voltage and the clock swing constant, although its boosting capacitors are also charged by the input nodes.

Figure 5-9 presents the proposed input chopper CH_{IN} as well as the clock generator. Similar to the one in Figure 4-11, the clock generator consists of an 800kHz oscillator and a timing generator based on D-latches, resulting in two sets of 200kHz complementary clocks with a 90-degree phase shift $\Phi_{CH, CHINV}$ and $\Phi_{NF, NFINV}$. Those clock generator and timing generator are

supplied by a 1.6V LDO. Their output clocks ($\Phi_{CH,\,CHINV}$ and $\Phi_{NF,\,NFINV}$) with the 1.6V amplitude can directly drive NMOS switches used in CH_{OUT}, CH_{ACFB}, and the SC-NF, because the source potentials of the switches are maintained in the range of 0.6 to 0.7V by the common-mode feedback circuits G_{m1CMFB} and $G_{mintCMFB}$. This small and constant clock amplitude reduces the residual offset contributed by the charge injection mismatch, and eliminates the external supply voltage V_{SY} dependency.

Based on the complementary chopping clocks Φ_{CH} and Φ_{CHINV}, two identical adaptive clock boosters generate the boosted output clocks Φ_{CHBST} and $\Phi_{CHINBST}$ by utilizing the 1.6V LDO output and a buffered input common-mode voltage V_{CMBUF} from a common-mode buffer. In each phase, one adaptive clock booster drives two NMOS switches to V_{CMBUF}+1.6V to turn on, while the other drives the other two NMOS switches to V_{CMBUF} to turn off. The common-mode buffer also drives the backgates of the NMOS switches to avoid the body effect. With a fixed 0.8V NMOS threshold voltage, the overdrive voltage and the clock swing are kept constant at 0.8V and 1.6V, respectively, with the changes in the input common-mode and supply voltages. This avoids the use of oversized switches, and improves the worst-case residual offset, the CMRR, and the PSRR.

The targeted total in-band noise PSD of 5.2nV/√Hz is dominated by $e_{n,Gm1}'$ = 4.1nV/√Hz, but the four input NMOS switches and two 100Ω input ESD resistances also contribute. To meet the target, each of the four NMOS switches then should meet a 200Ω on-resistance, requiring a 48μm width at the 0.8V overdrive voltage. If conventional CMOS switches were used, the required width of the NMOS switches would need to be larger to compensate for the overdrive voltage reduction in the middle of V_{SY}. Furthermore, the width of the PMOS switches would need to be even larger due to their lower mobility.

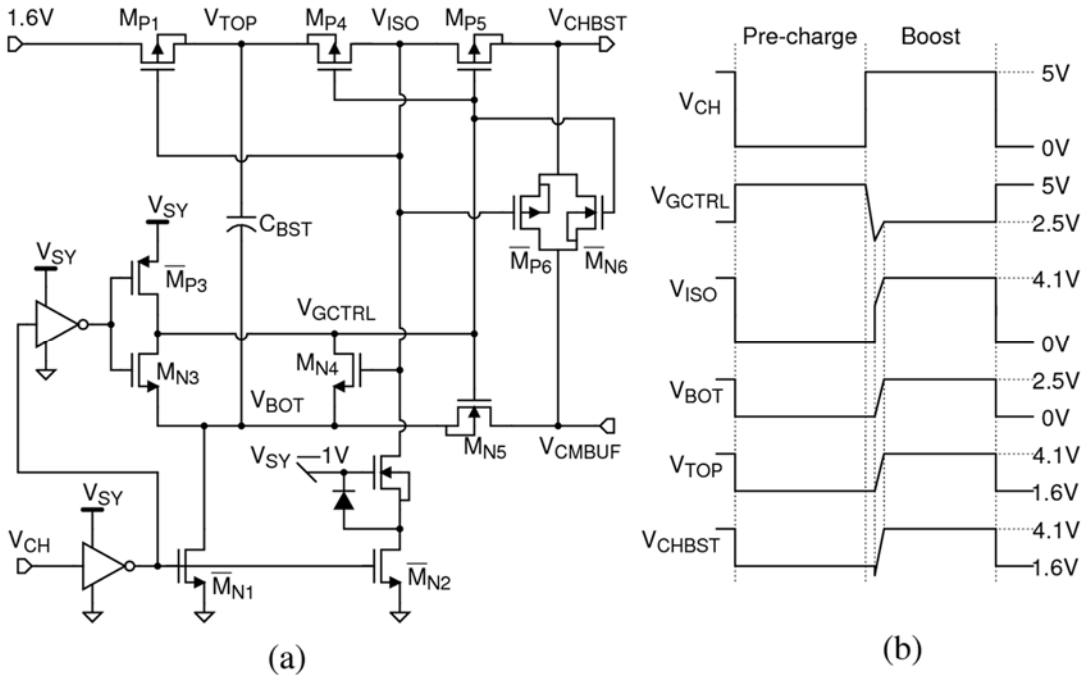

Figure 5-10: Adaptive clock booster: (a) circuit diagram; (b) conceptual waveform

5.4.3 Adaptive Clock Booster Circuit

Figure 5-10 (a) presents a circuit diagram of the adaptive clock booster. Additionally, Figure 5-10 (b) shows the conceptual operating voltage waveforms, with V_{SY} = 5V and V_{CM} = 2.5V. The backgates of all the NMOS switches are isolated from the substrate by the deep n-well tied to V_{SY}. Based on an input clock V_{CH}, this circuit consists of pre-charge and boosting phases. In the pre-charge phase, V_{CH} is driven low to the ground. Consequently, the switches, indicated by the overlined names in the figure, turn on. Capacitor C_{BST} is pre-charged, since M_{N1} connects the bottom plate V_{BOT} to the ground, and M_{P1} connects the top plate V_{TOP} to the 1.6V. The common-mode buffer drives an output V_{CH_BST} to V_{CMBUF} through a CMOS switch $M_{N6,P6}$. V_{TOP} and V_{CH_BST} nodes are isolated by two series PMOS switches M_{P4} and M_{P5}. Their gate V_{GCTRL} is driven high to V_{SY} through M_{P3}. Additionally, their common p-diffusion node V_{ISO} is pulled down to the ground, while their n-backgates are tied to V_{TOP} and V_{CH_BST}, respectively. This turns off all the diodes between the n-backgate and the p-diffusions in M_{P4} and M_{P5}, regardless of the potential of V_{CMBUF}.

In the boosting phase, V_{CH} is driven high to V_{SY}. Consequently, the switches, indicated by the names not overlined in the figure, turn on. First, V_{BOT} and V_{ISO} become disconnected from the ground. V_{GCTRL} goes down toward V_{BOT} due to the discharge through M_{N3}. When V_{GCTRL} reaches below 0.8V, M_{P4} and M_{P5} turn on, connecting V_{TOP}, V_{ISO}, and V_{CH_BST} to the 1.6V together. V_{ISO} then turns M_{P1} off to disconnect V_{TOP} from the 1.6V. Additionally, V_{ISO} turns M_{N5} on, so that V_{BOT} climbs to V_{CMBUF}, which is driven by the common-mode buffer. This boosts V_{TOP}, V_{ISO}, and V_{CH_BST} up to V_{CMBUF}+1.6V through the pre-charged capacitor C_{BST}.

Note that when V_{SY} and V_{CM} are 5V, V_{CH_BST} will be 6.6V in the boosting phase. However, every single transistor has relative terminal voltages less than 5V, to ensure reliability. The gate-source voltages of M_{P4} and M_{P5} are kept at –1.6V by $V_{GCTRL} = V_{CMBUF}$, and that of M_{N5} is kept at 1.6V by $V_{ISO} = V_{CMBUF}$+1.6V. Additionally, the drain-source voltage of M_{N2} is kept less than 5V by an NMOS cascode and a clamp diode.

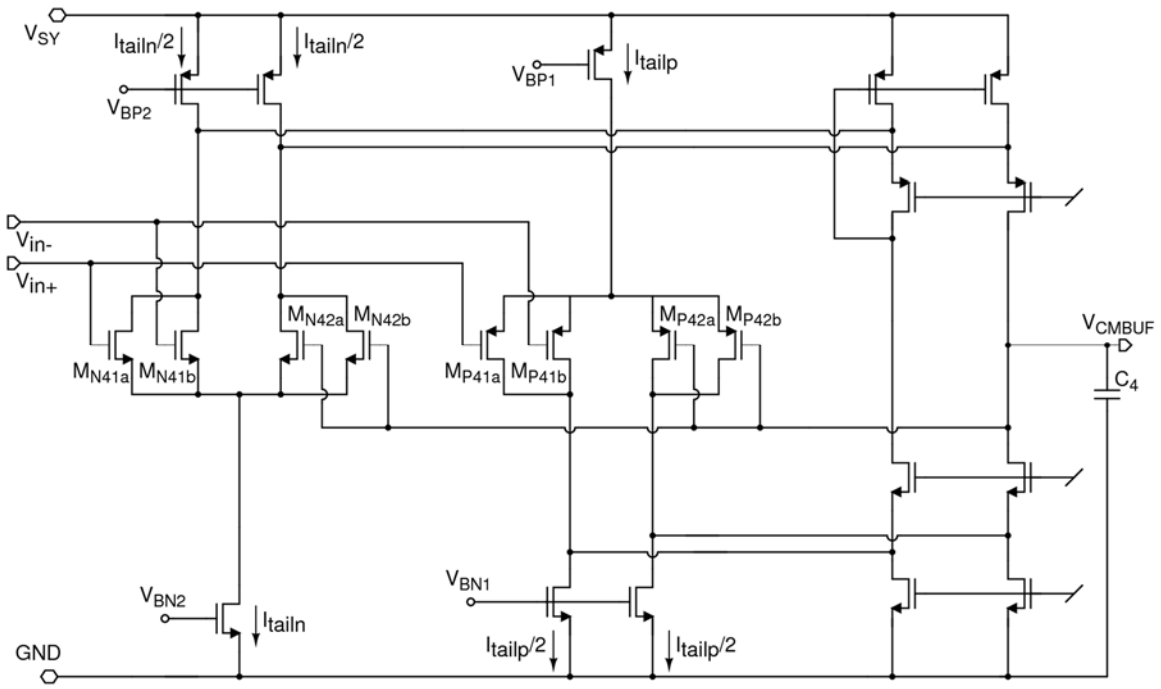

Figure 5-11: Common-mode buffer

5.4.4 Common-Mode Buffer

Figure 5-11 presents the circuit diagram of the common-mode buffer. It consists of complementary p-channel and n-channel input pairs $M_{P41a,41b,42a,42b}$ and $M_{N41a,41b,42a,42b}$, followed by a folded cascode stage. Similar to G_{m1}, the bias voltages $V_{BP1,2}$ and $V_{BN1,2}$ are controlled to set the bias currents, and to realize the rail-to-rail input common-mode voltage range. When the p-channel input pair is operating, two input voltages V_{in+} and V_{in-} are averaged by the two parallel input PMOS $M_{P41a,b}$, and the output voltage V_{CMBUF} will be equal to the averaged input voltage by the feedback through the other two input PMOS $M_{P42a,b}$. The n-channel input pair generates V_{CMBUF} in the same way when operating. This common-mode buffer only drives the backgate of the NMOS switches and the clock boosting capacitors C_{BST}, and thus does not need to provide continuous output current. Therefore, it consists of a single-stage transconductor to conserve power and die area. A 10pF capacitor C_4 is added to maintain the output voltage V_{CMBUF} stable even in the presence of transients to charge C_{BST}.

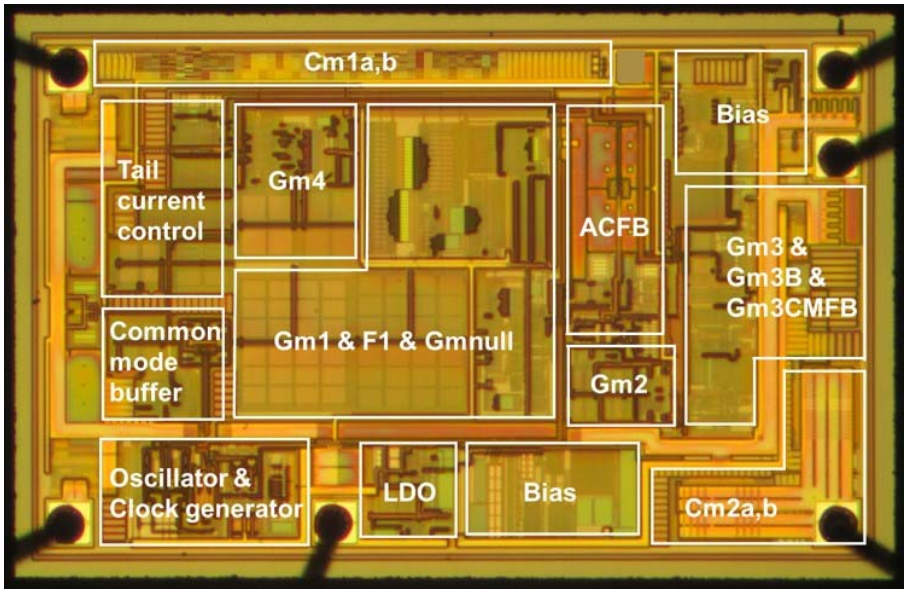

Figure 5-12: Die micrograph of the op-amp

5.5 Measurement Results

The design has been fabricated as a stand-alone op-amp in a 0.35µm CMOS process augmented by 5V CMOS transistors. Figure 5-12 shows a die micrograph with the entire 1.26mm^2 area, only 8% of which is occupied by the capacitors $C_{m1a,b}$ and $C_{m2a,b}$ thanks to the proposed frequency compensation technique. The on-chip clock generator consists of 3V transistors and is supplied by the 1.6V LDO, while all the other circuits consist of 5V transistors. The op-amp draws 1.4mA from a 2.1V to 5.5V supply voltage V_{SY}, and operates over the rail-to-rail input common-mode voltage V_{CM} range and the temperature range of –40°C to 125°C. In addition to the 1040µA listed in Table 5-1, G_{mnull}, the ACFB, G_{m4}, the input common-mode buffer, and the rest of the circuit consume 40µA, 40µA, 80µA, 50µA, 150µA, respectively. The characterization is done at two specified V_{SY}: 2.5V and 5.0V.

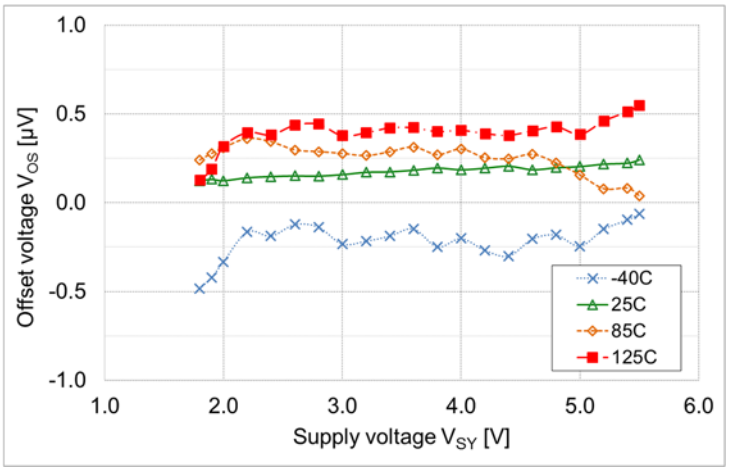

Figure 5-13: Offset voltages over supply voltage

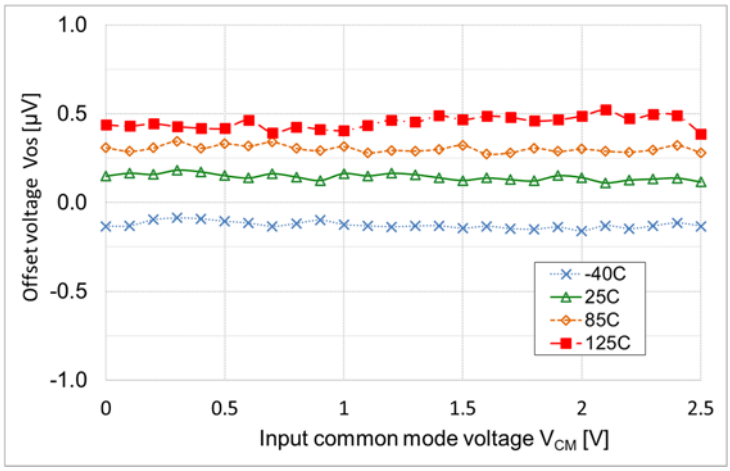

Figure 5-14: Offset voltages over the rail-to-rail V_{CM} range

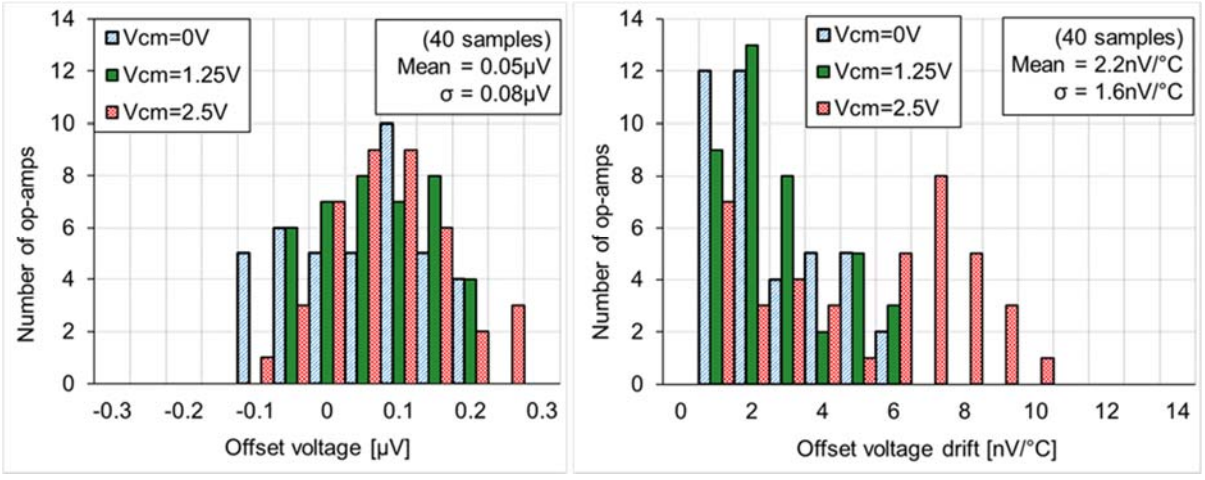

Figure 5-15: Histograms of the offset voltage and (b) the temperature drift

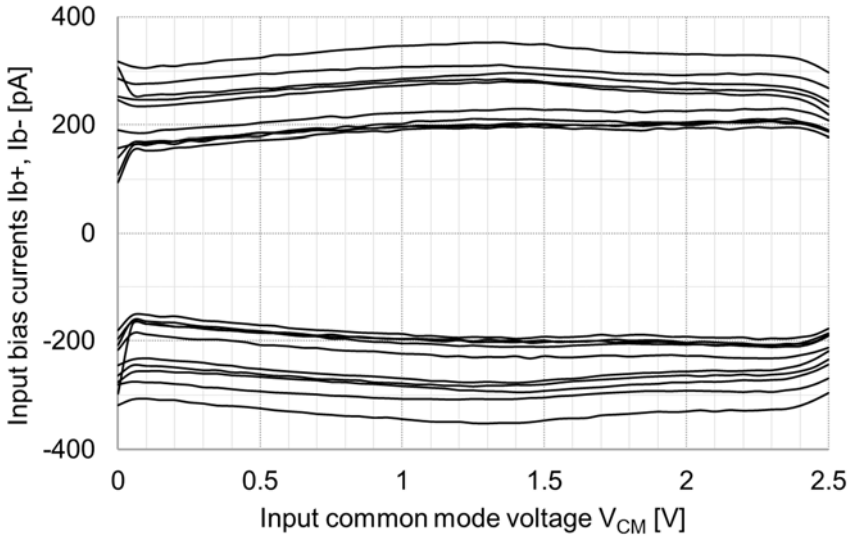

Figure 5-16: Input bias currents over the rail-to-rail V_{CM} range

Figure 5-13 shows the input offset voltages versus V_{SY} with the temperatures at –40°C, 25°C, 85°C, and 125°C. Additionally, Figure 5-14 shows those versus V_{CM} with V_{SY} = 2.5V. The offset voltages are well below ±1μV over the entire V_{SY}, V_{CM}, and temperature range. Figure 5-15 (a) and (b) shows the histograms of the offset voltages and the temperature drift, respectively. The data are obtained with V_{CM} at 0V, 1.25V, and 2.5V with V_{SY} = 2.5V. With all V_{CM} conditions, the offset voltages and the temperature drifts are well below ±0.5μV and ±0.015μV/°C, respectively. Additionally, both the minimum CMRR and PSRR are 142dB. Figure 5-16 shows the input bias currents of ten op-amps, all of which are relatively flat and below ±400pA. Almost every unit shows about a 50pA change near each supply rail, because the output of the input common-mode buffer then saturates.

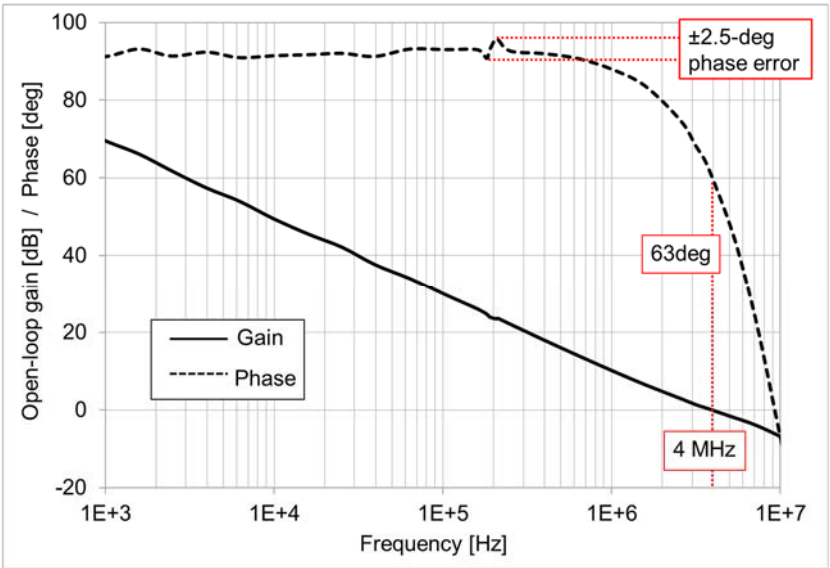

Figure 5-17: Open-loop gain and phase

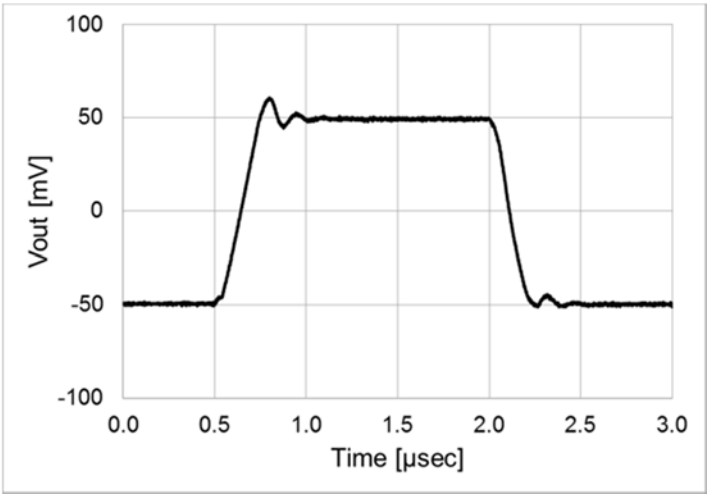

Figure 5-18: Step response with a 100mV signal

Figure 5-17 shows the open-loop gain and phase with a load capacitor of 100pF. It can be seen that the op-amp achieves a 4MHz unity gain bandwidth and a 63-degree phase margin. The notch created by the ACFB is almost buried by the HFP, although a small pole-zero doublet and hence a ±2.5-degree phase hump at 200kHz can still be seen. This is the largest hump among 20 op-amp units, the mean value of which is ±1.6 degrees. As explained in Section 5.2.5, this is caused by the frequency response mismatch between the LFP and HFP associated with transconductor and capacitor mismatch. Figure 5-18 shows the step response with a 100mV signal, while the op-amp is configured for unity gain and is driving 100pF.

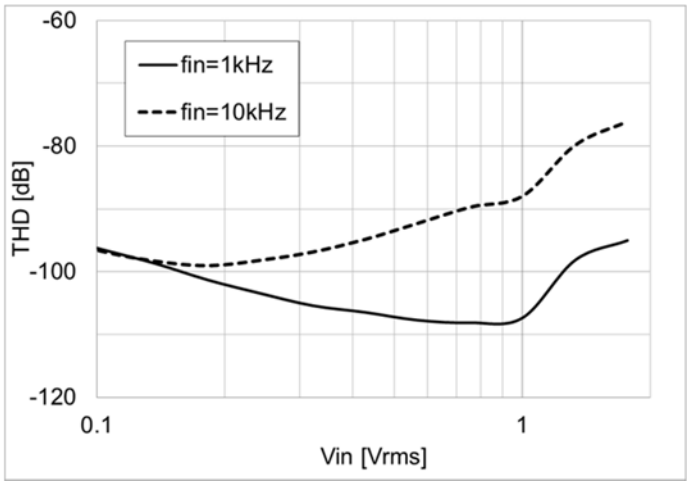

Figure 5-19: THD versus signal amplitude

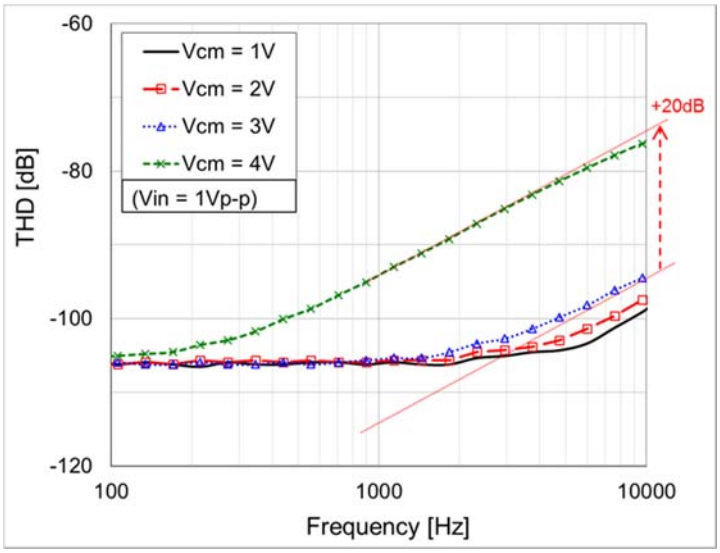

Figure 5-20 THD over the frequency with V_{CM} = 1V, 2V, 3V, 4V

Figure 5-19 shows the total harmonic distortion (THD) versus input signal amplitude with 1kHz and 10kHz signals, unity gain configuration, and V_{SY}=5V. The result indicates that the total error is dominated by the distortion when the signal amplitude increases above $1V_{rms}$. Figure 5-20 also shows the THD over input signal frequency with a $1V_{p-p}$ signal amplitude and V_{CM} = 1, 2, 3, and 4V. In the higher frequencies above 1kHz, the THD is worse with V_{CM} = 4V by 20dB. This is because, when the input common-mode voltage crosses over 3.8V, the operation of the input stage G_{m1} transitions between p-channel and n-channel pairs, each of which has unique initial offset. After this transition occurs, the ACFB has to be settled to a different value of initial offset, during which residual ripple is generated. This residual ripple occurs twice every input signal period, which causes extra distortion.

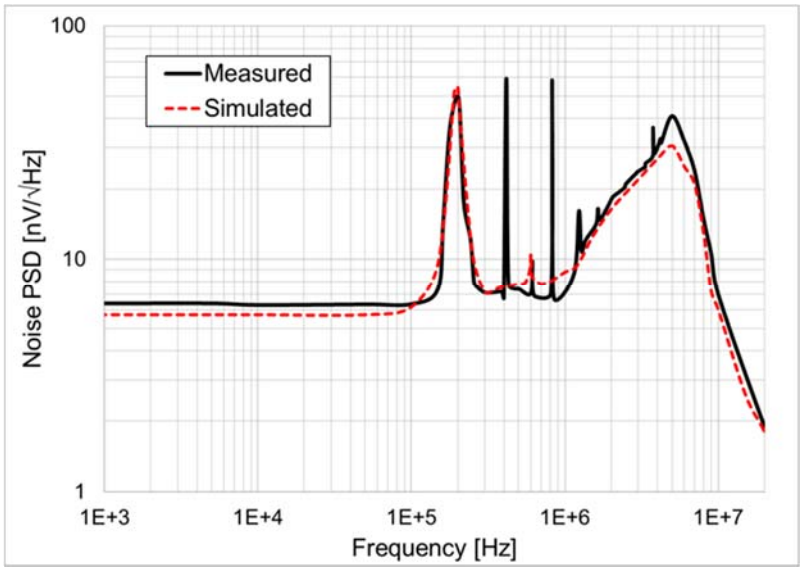

Figure 5-21: Measured and simulated noise PSD

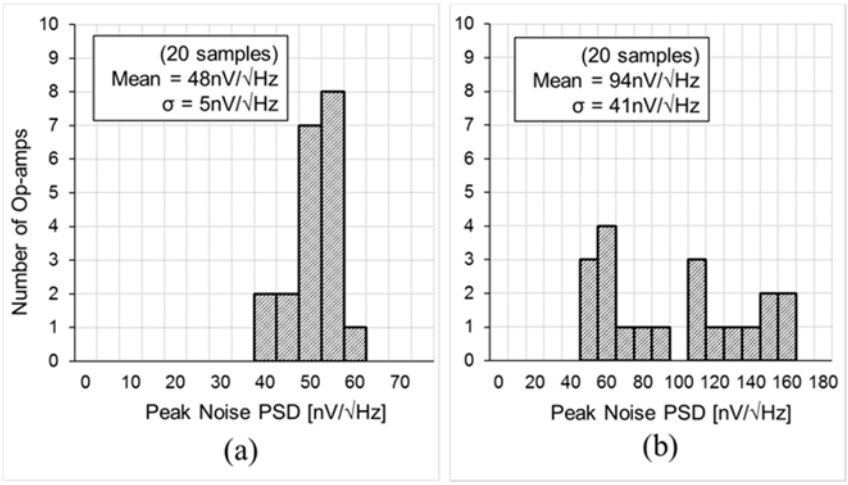

Figure 5-22: Histograms of the peak PSD magnitude (a) at 200kHz and (b) 400kHz

Figure 5-21 shows the measured noise PSD with a unity gain configuration along with the simulation result by the SpectreRF periodic noise analysis [19]. The measurement indicates a 5.6nV/√Hz in-band noise PSD floor and a 0.22Hz *1/f* noise corner frequency. The 49nV/√ Hz noise PSD peak at the 200kHz chopping frequency is well correlated to the 55nV/√ Hz simulated one since it is dominated by the up-modulated sampled noise, hence its inclusion in the simulation. On the other hand, the peak PSD at 400kHz is due to the glitches caused by the input charge injection, and is thus not included in the simulation. By measuring 20 op-amp units, Figure 5-22 (a) and (b) shows histograms of these peak PSDs at 200kHz and 400kHz, respectively.

Table 5-2: Comparison with other state-of-the-art

	This Work	[7]	[10]	[12]	[14]
Year	2011	2009	2010	2002	2011
Min. Operating V_{SY} [V]	2.1	2.2	4.0	2.7	2.7
Specified V_{SY} [V]	2.5	2.5	5.0	5.0	3.3
R-R Input Range	Yes	No	No	No	No
I_{SY} [mA]	1.4	0.95	0.14	2.1	1.1
fchop [kHz]	200	* 30	30	200	200
Max. Vos [μV]	0.5	5.0	1.0	10	5.5
Max. Vos drift [μV/°C]	0.015	0.020	0.023	0.050	0.018
Min. CMRR [dB]	142	105	137	115	120
Max. Ibias [pA]	±400	±100	±110	±1000	±1100
GBW [MHz]	4.0	5.0	1.8	** 4.8	10.0
Slew Rate [V/μs]	0.5	2.5	NS	5.0	5.0
en [nV/√Hz]	5.6	11.0	10.5	6.0	6.2
NEF	8.1	13.0	4.8	10.6	7.9
Die area [mm^2]	1.26	NS	1.8	NS	NS

* Extracted as the noise PSD peak frequency in the datasheet
** Conditionally stable op-amp, *** NS = Data not shown

Lastly, the specified performance is summarized in Table 5-2, and is compared with the other state-of-the-art chopper op-amps operating below a 5V supply. The listed numbers are obtained at the specified supply voltage (V_{SY}) of each op-amp. The proposed op-amp is specified with the lowest supply voltage of 2.5V and offers a rail-to-rail input range. It also achieves the lowest maximum offset voltage of 0.5μV, the lowest noise PSD of 5.6nV/√Hz, and a high minimum CMRR of 142dB.

5.6 Conclusion

A 5.6nV/√Hz chopper op-amp has been realized by employing frequency compensation technique using the current attenuator and the dummy differential output. This technique relaxes the trade-off between in-band noise PSD, current consumption, and capacitor size, so that the op-amp only draws 1.4mA from a 2.1V to 5.5V supply and occupies a die area of 1.26mm^2. It also achieves a 4MHz unity gain bandwidth while driving a load capacitor of up to 100pF. Moreover, ACFB is used to suppress the up-modulated ripple, and the resulting notch at the 200kHz

chopping frequency is buried by the HFP. Compared to the implementation in Chapter 4, the loop gain of the ACFB is increased from 43dB to 82dB by adding an active integrator, thus reducing the residual ripple. Consequently, the maximum peak PSD at the chopping frequency was reduced down to 62nV/√Hz, although further peak PSD reduction is limited by the noise contribution of the active integrator to the sampled noise in the SC-NF.

To drive the NMOS input chopping switches, an adaptive clock boosting technique is employed, so that the charge injection is minimized and maintained independent of changes in the supply and input common-mode voltages. Consequently, the residual offset contributed by their charge injection mismatch is reduced, and 0.5μV maximum offset and 15nV/°C maximum offset drift are achieved over the entire rail-to-rail input common-mode voltage range and a –40°C to 125°C temperature range.

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Chapter 6

Auto-Zero and Chopper Op-Amp with Clock Interleaving and Input Bias Current Trimming Techniques[3]

This chapter presents an auto-zero and chopper operational amplifier that operates from a 4.5V to 60V supply and is realized in a 0.18μm CMOS process augmented by 5V CMOS and 60V DMOS transistors [1]. It achieves a 0.02μV/°C maximum offset voltage drift, a 145dB minimum CMRR, a 5.8nV/√Hz noise PSD, and a 3.1MHz unity gain bandwidth, while consuming 840μA of current.

First, Section 6.1 describes the motivation for reducing the ripple and glitch errors for wide bandwidth applications, as well as the associated technical challenges. In Section 6.2, a capacitively-coupled auto-zeroed and chopped input transconductor is proposed consisting of six parallel channels, each of which is driven by interleaved 800kHz clocks. While the auto-zeroing reduces the initial offset and therefore the up-modulated ripple, the interleaving technique pushes the majority of the glitch energy up to 4.8MHz. Section 6.3 proposes an on-chip charge mismatch compensation circuit to reduce the maximum input bias current from 1.5nA to 150pA at a post-production test. The overall op-amp design is described in Section 6.4, and the measurement results are discussed in Section 6.5. The chapter ends with a conclusion in Section 6.6.

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[3] This chapter is derived from a journal publication of the author: Y. Kusuda, "A 60 V Auto-Zero and Chopper Operational Amplifier With 800 kHz Interleaved Clocks and Input Bias Current Trimming", *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2804-2813, Dec. 2015.

6.1 Motivation

As explained in Section 1.5.3, industrial applications require precision amplifiers with supply operation above 30V, a wide input common-mode range, and a wide signal bandwidth [2-4]. Most precision amplifiers are realized using Bipolar or JFET processes, to achieve 1μV/°C maximum offset voltage drifts, 10nV/√Hz in-band noise PSDs, and 2MHz unity gain bandwidths. Recently, op-amps with similar specifications have been reported using CMOS-based processes with the addition of high voltage DMOS transistors [5-8]. They utilize auto-zeroing and/or chopping techniques to reduce the high offset voltage drift and *1/f* noise associated with CMOS input transconductors [9]. Such op-amps can be manufactured at a lower cost, and can achieve lower offset voltage drift and *1/f* noise than Bipolar and JFET op-amps.

As explained in Section 2.4, chopping generates up-modulated ripple and glitches, resulting in peak PSDs at the chopping frequency f_{CH} and its harmonics. Such noise PSD peaks usually need to be attenuated by low-pass filters, which limits the usable signal bandwidth well below f_{CH}. On the other hand, a higher chopping frequency will increase the charge injection per unit of time, and thus degrade the DC specifications such as the offset drift and input bias current [10]. The charge injection also increases when wider input switches are used for lower on-resistance and hence, lower thermal noise. A 0.02μV/°C maximum offset drift, a 600pA maximum input bias current, and a 9nV/√Hz voltage noise PSD have been achieved [7], although the 60kHz chopping frequency limits the usable signal bandwidth. In [5], a higher chopping frequency of 333kHz is used, resulting in a somewhat worse DC performance: a 0.085μV/°C maximum offset drift, an 850pA maximum input bias current, and an 8.8nV/√Hz voltage noise PSD.

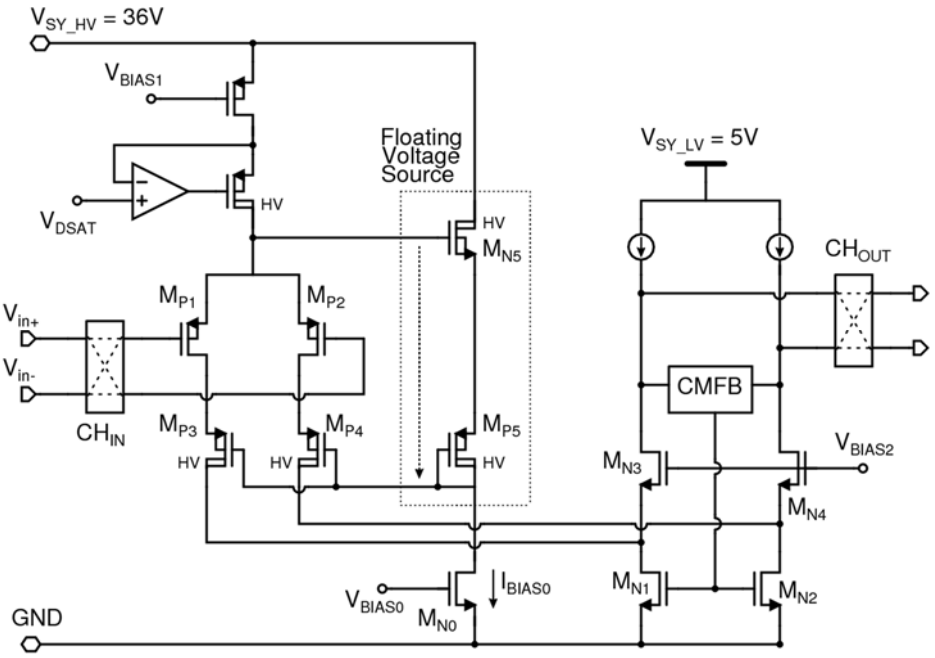

Figure 6-1: Input transconductor employing adaptive high voltage cascode transistors

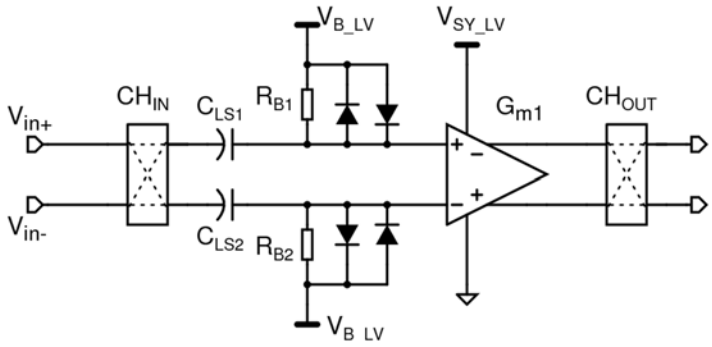

Figure 6-2: Previous capacitively-coupled chopper input transconductor

6.2 Input Transconductor Architecture

The input transconductor must offer a 30V level input common-mode voltage range, preferably including the ground to expand the range of applications. Additionally, it must employ auto-zeroing and/or chopping to remove the offset and 1/*f* noise from the in-band frequencies, and the resulting switching artifacts should be minimized and located at a higher frequency.

6.2.1 Previous High Voltage Input Transconductors

Figure 6-1 is a chopper input transconductor that offers a 30V level input common-mode voltage V_{CM} range [3]. The input pair $M_{P1,2}$ consists of low voltage transistors that have lower offset and noise than high voltage (HV) transistors for a given device size. The drain-source voltages are kept lower than the breakdown voltages with adaptive HV cascode transistors $M_{P3,4}$ and a floating voltage source. However, this transconductor will probably not perform well with the input voltages near the ground, since $M_{P3,4}$ will decrease the voltage headroom of $M_{P1,2}$. Moreover, it will consume relatively high power due to a high supply voltage V_{SY_HV}, which might degrade the performance due to the heat generated near the input pair.

An alternative topology is shown in Figure 6-2, namely the capacitively-coupled chopper input transconductor proposed by Fan [6,11,12]. Two level shift capacitors $C_{LS1,2}$ block the DC input common-mode voltage V_{CM}, while the inputs of a transconductor G_{m1} are biased at a fixed low voltage V_{B_LV} through bias resistors $R_{B1,2}$. In this case, G_{m1} can be supplied by a low supply voltage V_{SY_LV} and consist of low voltage transistors. DC differential input signals V_{in} are up-modulated to the chopping frequency f_{CH}, and then become AC-coupled to G_{m1}. On the other hand, AC differential input signals near f_{CH} are down-modulated to DC and then blocked by $C_{LS1,2}$, resulting in a notch at f_{CH}. A HFP can be added to bypass the notch, although it still creates a pole-zero doublet due to the mismatch between the two signal paths. Moreover, $R_{B1,2}$ needs to be greater than 100MΩ to sufficiently reduce the thermal noise contribution, resulting in slow settling after a large input common-mode voltage step. Therefore, this topology is less preferred for applications, where the amplifier's output must quickly settle with large step input signals.

Various other approaches to realize a wide input common-mode voltage range are introduced in [12].

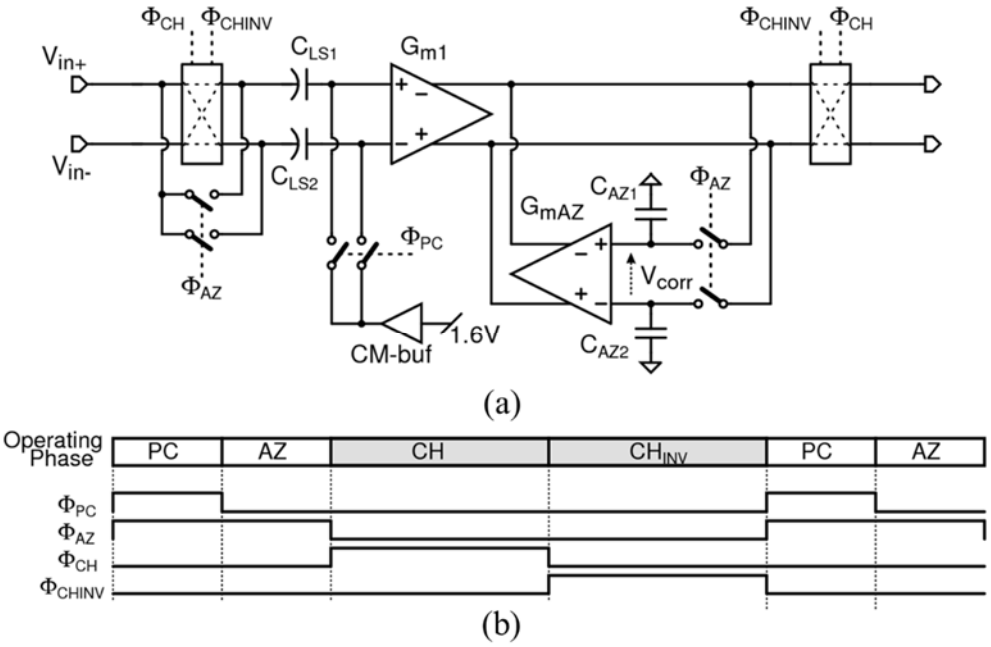

Figure 6-3: Capacitively-coupled auto-zero and chopper input transconductor: (a) circuit diagram; (b) timing diagram

6.2.2 Capacitively-Coupled Auto-Zero and Chopper Input Transconductor

Figure 6-3 (a) presents the proposed capacitively-coupled auto-zero and chopper input transconductor, along with the timing diagram in Figure 6-3 (b). During a pre-charge PC phase, two level shift capacitors $C_{LS1,2}$ are charged by a non-inverting input voltage V_{in+} and a 1.6V common-mode buffer CM-buf. The input voltages of an input transconductor G_{m1} are then biased at 1.6V and left floating in the subsequent auto-zero AZ, chopping CH, and inverting-chop CH_{INV} phases. In the AZ phase, the charge injection mismatch sampled by $C_{LS1,2}$ are cancelled along with the input offset of G_{m1}, by forming local feedback with an auto-zeroed transconductor G_{mAZ}. At the end of the AZ phase, the resulting correction voltage V_{corr} is sampled by two auto-zero capacitors $C_{AZ1,2}$. In the subsequent CH and CH_{INV} phases, the differential inputs and outputs of G_{m1} are connected to the signal path, amplifying the input signal V_{in}, while being chopped. The two $C_{LS1,2}$ work as floating voltage sources after the PC phase, and thus transfer the input signals to G_{m1} without creating a notch. Moreover, the auto-zeroing reduces the offset and consequently the ripple, while the residual error generated in V_{corr} is up-modulated to the chopping frequency, as will be discussed in Section 6.4.2 below.

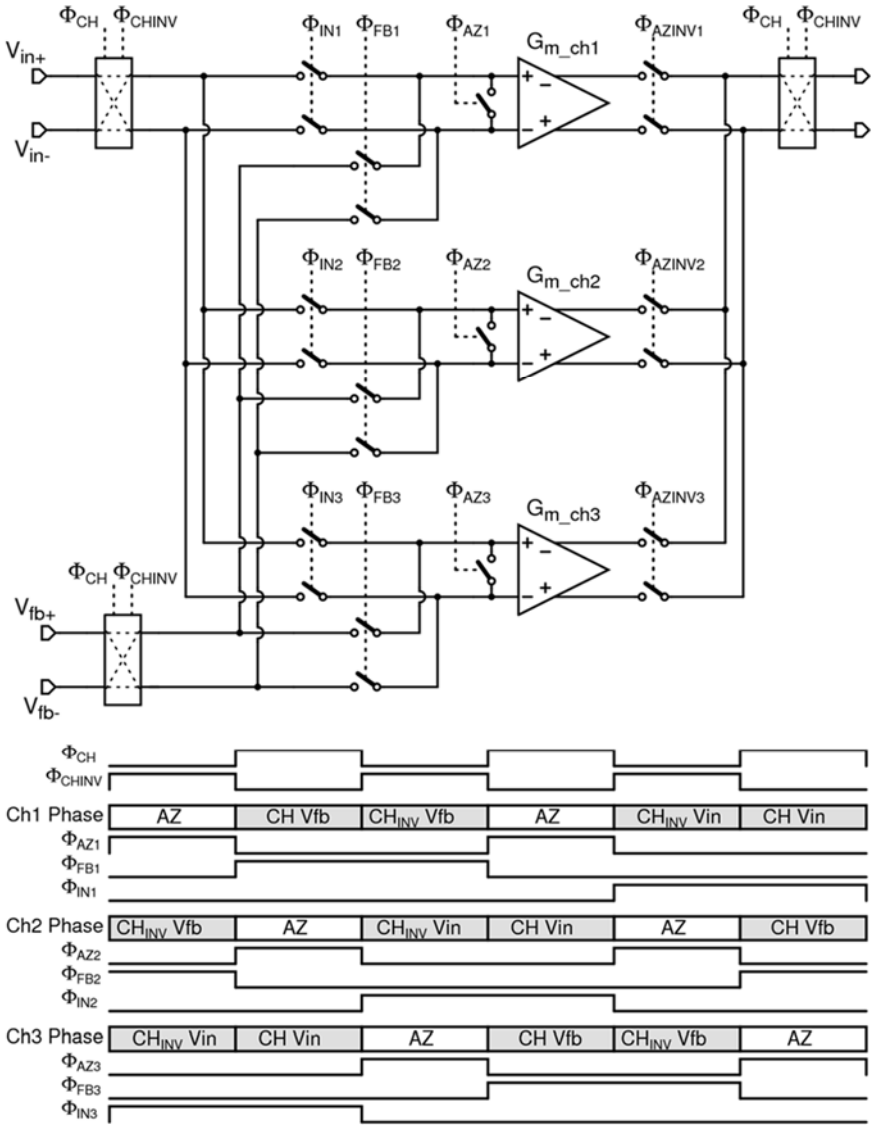

Figure 6-4: Ping-pong-pang auto-zero and chopper input transconductor for CFIA

6.2.3 Six Input Channels and Clock Interleaving

As explained in Section 3.2.4, the transconductor is unable to amplify the input signal during the auto-zero phase. The input signal can be continuously amplified by ping-ponging two identical input transconductors as shown in Figure 3-9 [13,14]. However, it consumes the twice the current and occupies the twice the area compared to the non-auto-zeroed chopped transconductor shown in Figure 2-8. To mitigate this problem, Sakunia proposed a ping-pong-pang auto-zero and chopper current feedback instrumentation amplifier (CFIA), incorporating three identical

input transconductor channels as shown in Figure 6-4 [15]. The timing diagram shows that while one channel is auto-zeroed, the other two work as input and feedback transconductors, one at a time. In this case, the three transconductors together consume 1.5 times the amount of current of a basic non-auto-zeroed CFIA with two transconductors.

Another remaining problem is that the various previous ripple reduction techniques only reduce the up-modulated ripple without reducing the glitches caused by charge injection [13-19]. As explained in Chapters 2 and 3, while the ripple can be reduced by a factor equal to the auto-zeroing loop gain, the glitches increase with the size of the switches and thus can result in the higher noise PSD.

Figure 6-5 (a) presents the proposed input transconductor in its entirety, consisting of six identical channels $Ch_{1\text{-}6}$ in parallel. This transconductor reduces both the ripple and glitches, as well as the extra current consumption for the auto-zeroing. Each channel consists of the capacitively-coupled auto-zeroed and chopped transconductor shown in Figure 6-3, and operates with identical and interleaved timing phases as shown in Figure 6-5 (b). Each channel goes through the PC, AZ, CH, and CH_{INV} phases. At any given time, one channel is in the PC phase, while another channel is in the AZ phase, and the other four channels are in either the CH or CH_{INV} phases, thus amplifying the input signal in parallel. This reduces the required transconductance of G_{m1} and the width of the switches in each channel. Therefore, to achieve the same in-band noise PSD, all six input transconductors only consume 1.5 more current than the non-auto-zeroed chopped transconductor shown in Figure 2-8.

The current consumption can be further reduced by increasing the number of channels operating in the CH or CH_{INV} phases relative to the total number of channels, for instance having a total of eight channels and assigning one channel to the PC, another channel to the AZ, and the other six channels to the CH or CH_{INV} phases. This, however, decreases the amount of settling time available for the PC and AZ phases during the full operating period, and thus increases the required bandwidth and therefore also the current consumption of CM-buf and G_{mAZ}. Moreover, the die size will also increase, due to the layout spacing required between each channel. Therefore, the total channel count of six is used to optimize the overall current consumption and the die size.

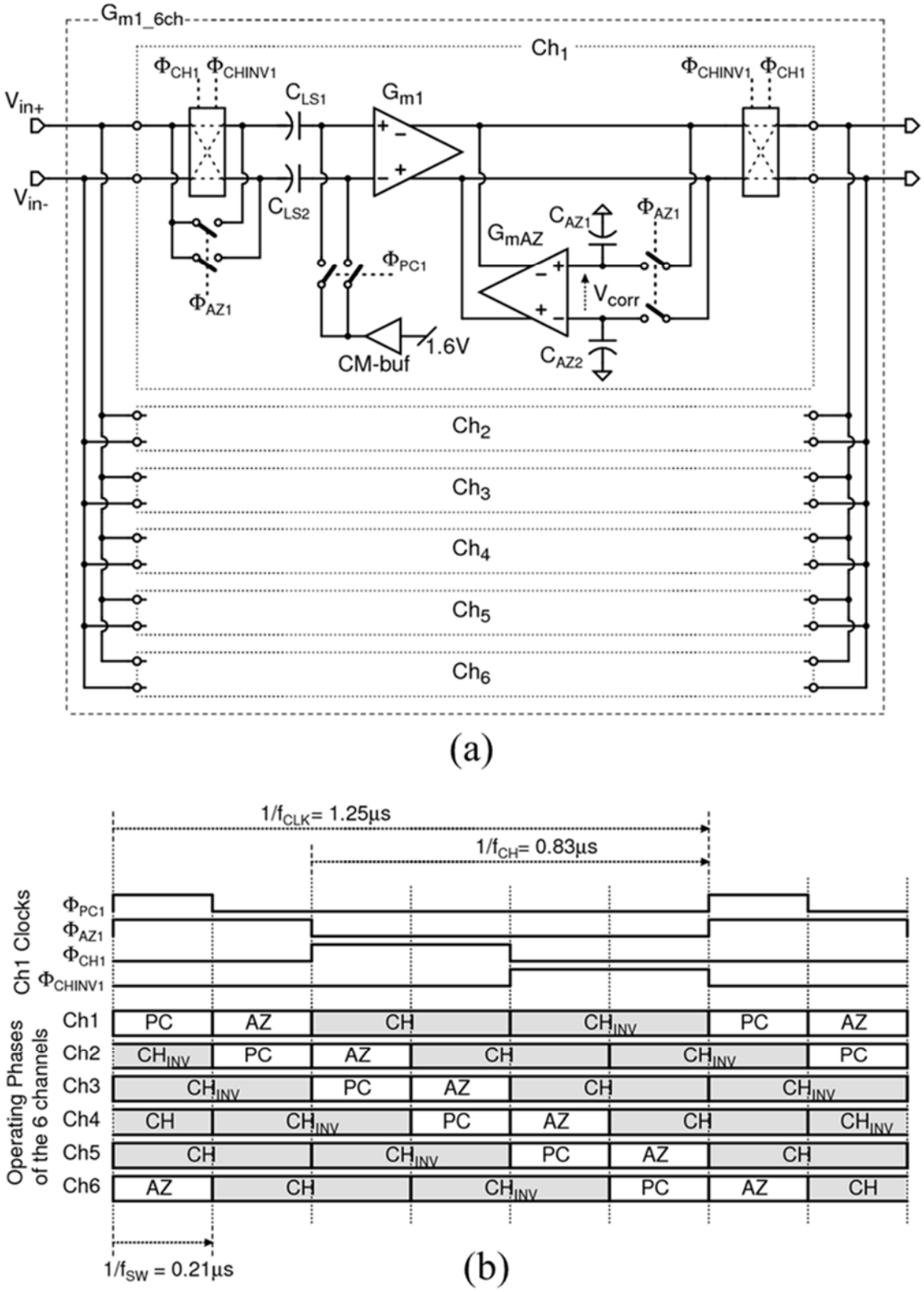

Figure 6-5: Proposed overall input transconductor consisting of six channels: (a) circuit diagram; (b) timing diagram

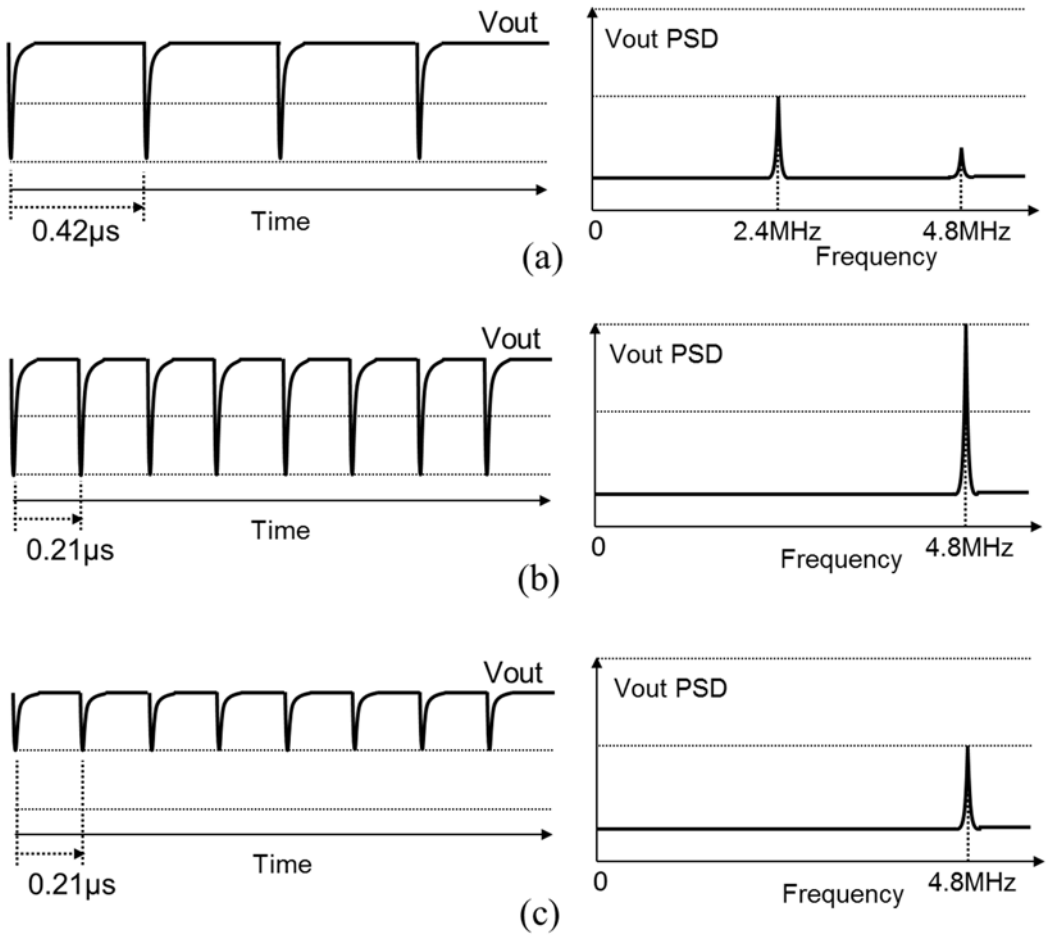

Figure 6-6: Glitch comparison in the time and frequency domains

As shown in the timing diagram, the full period of one channel amounts to 1.25µs, corresponding to an 800kHz fundamental clock frequency f_{CLK}. By dividing this full period by six, 0.21µs is assigned to each of the PC and AZ phases, while the remaining 0.83µs is assigned to the chopping, corresponding to a 1.2MHz chopping frequency f_{CH}. The combined complete circuit conducts the switching every 0.21µs, corresponding to a 4.8MHz switching frequency f_{SW}. The resulting noise PSD should then increase at 1.2MHz due to the up-modulated chopper ripple, and at 4.8MHz due to the glitches caused by charge injection. It should not increase at 800kHz as long as each channel generates identical glitch waveforms. The input bias voltage of each input transconductor is reset to 1.6V every 1.25µs. Even with a large input common-mode voltage step, at least one of the six transconductors is reset, returning to normal operation within 0.21µs.

The complete input transconductor proposed results in a smaller magnitude for the glitch per individual switching, thanks to the reduced size of the switches. Figure 6-6 illustrates the comparison of the expected output voltage waveform V_{OUT} and noise PSD from three circuits: the two channel circuit shown in Figure 3-9 with f_{CH} = 1.2MHz (Figure 6-6 (a)), the same two channel circuit but with f_{CH} = 2.4MHz (Figure 6-6 (b)), and the six channel circuit shown in Figure 6-5 with the interleaved f_{CH} = 1.2MHz (Figure 6-6 (c)). For simplicity, the figure only illustrates the glitches caused by charge injection, but not the up-modulated chopper ripple. First, comparing Figure 6-6 (b) with Figure 6-6 (a) shows that the glitches occur more frequently and that each one has the same magnitude. As a result, the peak PSD is pushed up to 4.8MHz, but its magnitude increases, which will not relax the requirements of the low-pass filter. Moreover, higher chopping frequency will increase the charge injection generated per unit of time, hence the DC errors. Next, comparing Figure 6-6 (c) with Figure 6-6 (a) shows that the glitches occur more frequently but that each one has a smaller magnitude, and thus the energy is spread out in the time domain without increasing the charge injection generated per unit of time. As a result, the peak PSD is pushed up to 4.8MHz without increasing the magnitude. This then relaxes the requirements of the low-pass filter, and thus extends the usable signal bandwidth.

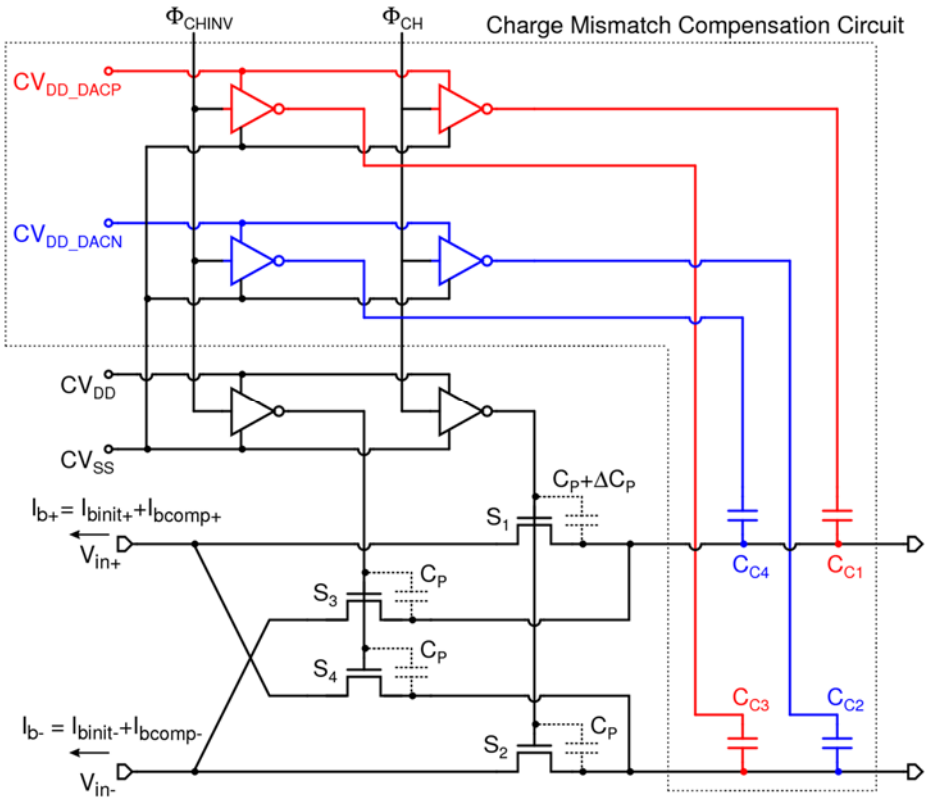

Figure 6-7: Input switching circuit SW_{IN} incorporating a charge mismatch compensation circuit

6.3 Input Bias Current Trimming

As presented in the previous section, the proposed op-amp employs a high 800kHz operating frequency f_{CLK}, to extend the usable signal bandwidth in conjunction with the ripple and glitch reduction techniques. As explained in Section 2.4.3, however, a higher f_{CLK} will increase the DC errors such as the residual offset and input bias current due to the charge injection mismatch [10]. In some bipolar op-amps, continuous current sources are implemented to offset the input base currents [20]. However, this method will not sufficiently compensate for the charge injection mismatch error due to the variation of f_{CLK} over the process skew and temperature. Alternatively, nested chopping technique explained in Section 3.1.3 could be implemented so that the outer slow chopping up-modulates the charge injection mismatch error caused by the inner fast chopping [21]. This, however, results in a high noise PSD at the slow chopping frequency, and thus limits the usable signal bandwidth.

6.3.1 Input Switching Circuit Employing a Charge Mismatch Compensation Circuit

Figure 6-7 presents the proposed input switching circuit SW_{IN}, incorporating a charge mismatch compensation circuit. The four NMOS switches $S_{1\text{-}4}$ conduct the switching operation required for the auto-zeroing and the chopping, and are driven by positive and negative clock supplies CV_{DD} and CV_{SS} through inverters. Let us assume S_1 is associated with a coupling capacitor $C_P+\Delta C_P$, while each of the other three switches is associated with C_P. As explained in Section 2.4.3, this capacitance mismatch ΔC_P causes a charge injection mismatch per clock period $1/f_{CLK}$, generating initial input bias currents I_{binit+} and I_{binit-} equal to:

$$I_{binit+} \equiv I_{binit} = f_{CLK} \cdot \Delta C_P \cdot (CV_{DD} - CV_{SS}) , \qquad (6\text{-}1)$$

$$I_{binit-} \equiv -I_{binit} = -f_{CLK} \cdot \Delta C_P \cdot (CV_{DD} - CV_{SS}) . \qquad (6\text{-}2)$$

To offset these error currents, the charge mismatch compensation circuit can inject charge mismatches with opposite polarity through four metal-metal coupling capacitors $C_{C1\text{-}4}$. An adjustable positive supply CV_{DD_DACP} drives C_{C1} and C_{C3}, while another adjustable positive supply CV_{DD_DACN} drives C_{C2} and C_{C4}. By adjusting these supply voltages, the resulting compensation input bias currents I_{bcomp+} and I_{bcomp-} can be controlled to allow:

$$I_{bcomp+} \equiv I_{bcomp} = 2 f_{CLK} \cdot C_{C1\text{–}4} \cdot (CV_{DD\_DACP} - CV_{DD\_DACN}) , \qquad (6\text{-}3)$$

$$I_{bcomp-} \equiv -I_{bcomp} = -2 f_{CLK} \cdot C_{C1\text{–}4} \cdot (CV_{DD\_DACP} - CV_{DD\_DACN}) . \qquad (6\text{-}4)$$

$C_{C1\text{-}4}$ = 2fF is only one-tenth of C_P, which will not significantly increase the absolute amount of charge injection nor, consequently, the magnitude of transient glitches. The resulting input bias currents I_{b+} and I_{b-} are given by:

$$I_{b+} = I_{binit} + I_{bcomp} , \qquad (6\text{-}5)$$

$$I_{b-} = -(I_{binit} + I_{bcomp}) . \qquad (6\text{-}6)$$

Both I_{b+} and I_{b-}will be pushed toward zero by adjusting $I_{bcomp} = -I_{binit}$.

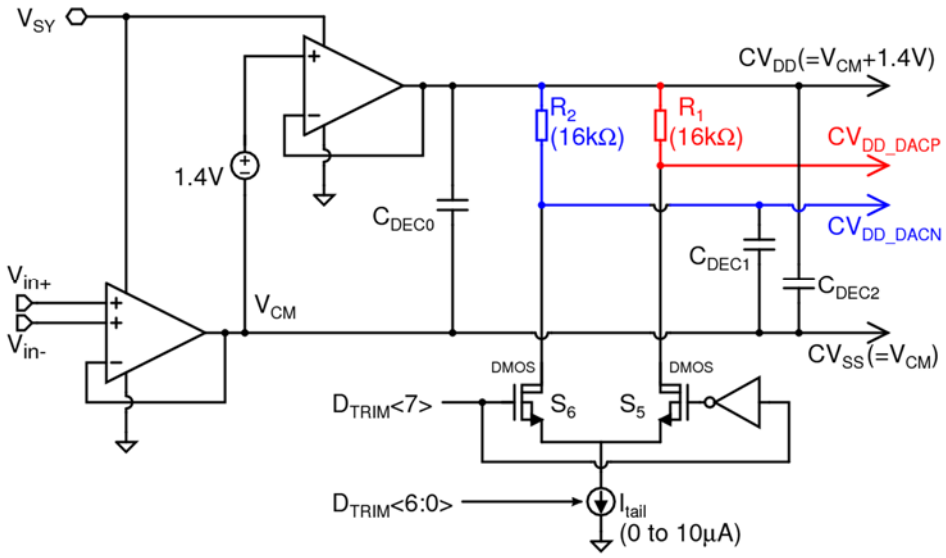

Figure 6-8: Common-mode tracking regulator CM-Reg

6.3.2 Common-Mode Tracking Regulator

Figure 6-8 presents a common-mode tracking regulator circuit CM-Reg that generates the clock supplies CV_{SS}, CV_{DD}, CV_{DD_DACP}, and CV_{DD_DACN}. All the clock supplies track an input common-mode voltage V_{CM}, and are shared across the six channels. CV_{SS} and CV_{DD} are set to V_{CM} and V_{CM}+1.4V, respectively, so that the NMOS switches in SW_{IN} always receive a 1.4V gate-source voltage to be turned on. Additionally, the backgates of the switches are driven by CV_{SS} to avoid the threshold voltage changes caused by the body effect. This maintains the amount of charge injection and on-resistance constant and independent of change in V_{CM} [22].

An 8-bit digital control signal D_{TRIM} controls the amount of tail current I_{tail} and switches S_5 and S_6. The MSB $D_{TRIM}<7>$ turns on either S_5 or S_6, so that either CV_{DD_DACP} or CV_{DD_DACN} decreases from CV_{DD} with a voltage drop across R_1 or R_2. The rest of the bits $D_{TRIM}<6:0>$ linearly control the tail current $I_{tail} = 80\text{nA} \cdot N_{TRIM}$ from 0 to 10µA, where N_{TRIM} is the decoded integer number of the bits. Based on Equation (6-3), the compensation input bias current of the combined six channels I_{bcomp_6ch} becomes:

$$I_{bcomp\_6ch} = 6 \cdot 2 f_{CLK} \cdot C_{C1-4} \cdot S_{TRIM} \cdot R_{1,2} \cdot 80\text{ nA} \cdot N_{TRIM}\,, \qquad (6\text{-}7)$$

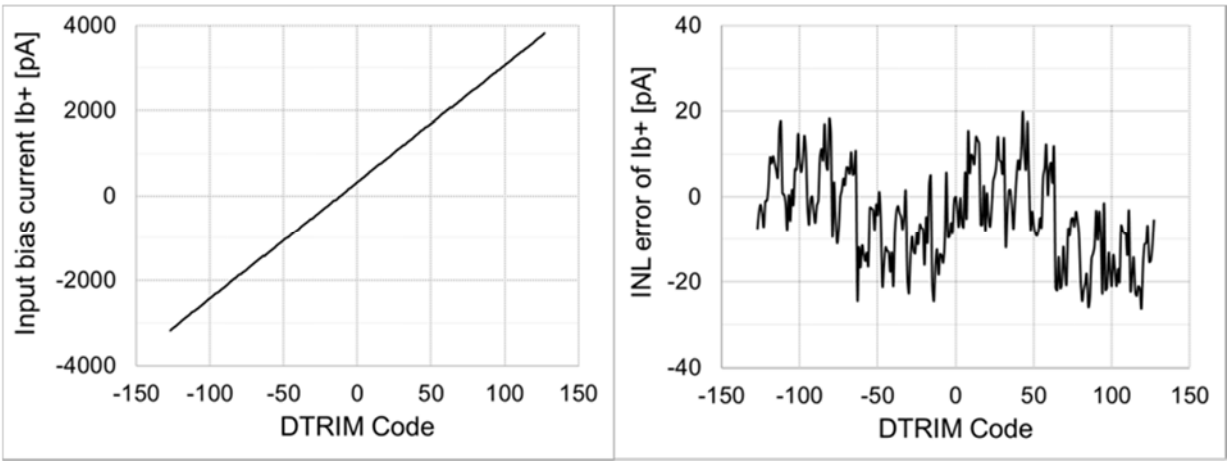

Figure 6-9: Measured input bias current versus trimming code

where S_{TRIM} is the polarity of $D_{TRIM}<7>$ and can be either +1 or –1. By applying f_{CLK} = 800 kHz, $C_{C1\text{-}4}$ = 2fF, and $R_{1,2}$ = 16kΩ, I_{bcomp_6ch} varies by 24.6pA with one LSB change, and increases up to a ±3.124nA full scale. This full scale covers the worst-case initial input bias current of ±1.5nA; the one LSB is sufficient to adjust the resulting input bias currents down below 100pA. The reference current of I_{tail} consists of an on-chip bandgap reference voltage divided by a poly-resistor that is the same type as R_1 and R_2. Thus, I_{bcomp_6ch} and, accordingly, the resulting input bias current will be stable over temperature. However, the trimming gain, which is defined as the sensitivity of I_{bcomp_6ch} to N_{TRIM}, can deviate due to the initial value variations in the bandgap reference voltage, metal-metal capacitors $C_{C1\text{-}4}$, and the clock frequency f_{CLK}. Therefore, it is calibrated at the post-production trimming by measuring the resulting input bias current change with two different D_{TRIM} codes.

Figure 6-9 shows the measured resulting input bias current and the integral non-linearity error INL when sweeping the trimming code D_{TRIM} from the negative full scale –127 to the positive full scale +127. The maximum INL error of 25pA is sufficiently low to achieve a trimmed input bias current below 100pA. Decoupling capacitors C_{DEC0}, C_{DEC1}, and C_{DEC2} are placed to maintain CV_{DD}, CV_{DD_DACN}, and CV_{DD_DACP} stable even in the presence of clock transients. These capacitors also reduce the thermal noise of CM-Reg at the 1.2MHz chopping frequency, so that the resulting overall in-band noise does not degrade.

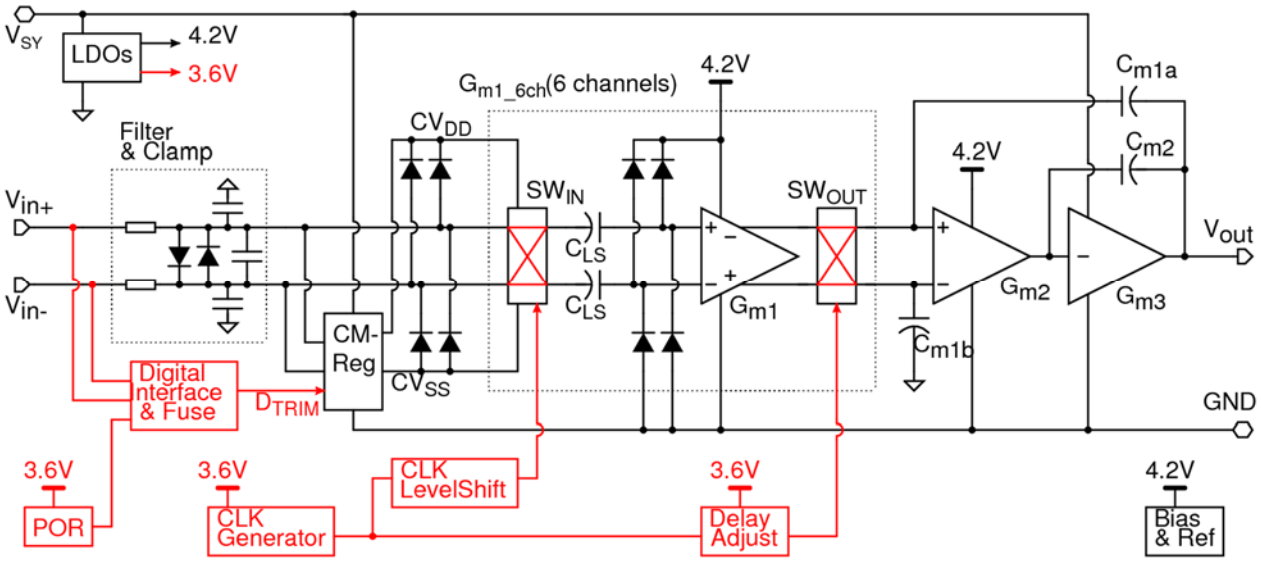

Figure 6-10: Proposed overall op-amp

6.4 Overall Op-Amp Implementation

6.4.1 Overall Op-Amp Architecture

Figure 6-10 presents a block diagram of the overall op-amp with five pin-outs: V_{SY}, GND, V_{in+}, V_{in-}, and V_{out}. The proposed six channel input transconductor G_{m1_6ch} is followed by the second and output stage transconductors G_{m2} and G_{m3}. G_{m3} provides a 30dB DC gain when driving a 10kΩ output load resistor. In addition, G_{m1_6ch} and G_{m2} provide 70dB and 50dB DC gains, respectively, resulting in the 150dB overall open-loop DC gain. The 5mV worst-case offset of G_{m2} contributes to the residual offset due to the finite gain of G_{m1_6ch}: 5mV/70dB = 1.6μV. This residual offset is insignificant, and the overall residual offset is dominated by the charge injection mismatch in SW_{IN}. The input signal is amplified by four parallel channels at a time, each of which has a 400μS transconductance for G_{m1}, resulting in a 1.6mS overall transconductance for G_{m1_6ch}. The transconductances of G_{m2} and G_{m3} are 500μS and 4mS, respectively. Nested Miller frequency compensation is realized by capacitors $C_{m1a} = C_{m1b} = 80pF$ and $C_{m2} = 10pF$. These parameters determine the unity gain bandwidth $f_u = 1.6mS/(2\pi \cdot 80pF) =$

3.2MHz and the second pole f_{p2} = 500μS/(2π•10pF) = 8.0MHz. The third pole is created at the output with an external load C_L. This pole can be pushed to a higher frequency with the cascode Miller compensation technique [19], the circuit of which will be discussed in Section 6.4.3 below.

During the production test, the initial input bias current I_{binit_6ch} is measured externally, and D_{TRIM} code is provided through an input digital interface. The determined D_{TRIM} code is stored in an on-chip polyfuse memory array, which is read every power up cycle triggered by an on-chip power-on reset circuit POR. Therefore, after the post-production trimming is complete, the op-amp works as a stand-alone op-amp without relying on external digital resources.

The selected process is based on a 0.18μm CMOS technology augmented by 5V CMOS and 60V DMOS transistors. The 5V CMOS transistor can handle gate-source and drain-source voltages up to 6V, and can be formed in an isolated backgate with a more than 60V breakdown voltage to the substrate. The 60V DMOS transistor can handle gate-source voltages up to 6V and drain-source voltages up to 60V, although it occupies a larger area and generates higher offset and noise than the 5V CMOS transistor. Therefore, the key blocks in the signal chain, including SW_{IN}, G_{m1}, SW_{OUT}, and G_{m2}, consist of the 5V CMOS transistors, while the 60V DMOS transistors are used to isolate these blocks from high supply and input voltages. A CM-Reg circuit maintains the supply voltage difference $CV_{DD} - CV_{SS}$ to 1.4V to protect SW_{IN}. Since C_{LS} level-shifts the input signals down to 1.6V, G_{m1}, SW_{OUT}, and G_{m2} are all supplied by a 4.2V regulated voltage. Additionally, an input RC filter and clamping diodes are implemented to protect SW_{IN} and G_{m1} from high voltage transient inputs.

Metal-metal fringing capacitors with a more than 60 V breakdown are used for the input RC filter, C_{LS}, C_{m1a}, C_{m1b}, and C_{m2}. The clocks are generated with a 3.6 V regulated supply, and a clock level shifter is used before SW_{IN}. A delay circuit is added before SW_{OUT}, to align the clock phases at SW_{IN} and SW_{OUT}. The overall op-amp consumes an 840μA supply current: 320μA for G_{m1_6ch}, 180μA for G_{m2}, 180μA for G_{m3}, 50μA for CM-Reg, 50μA for the clock generator and level shifter, and 60μA for the rest including the POR, LDOs, and bias circuits.

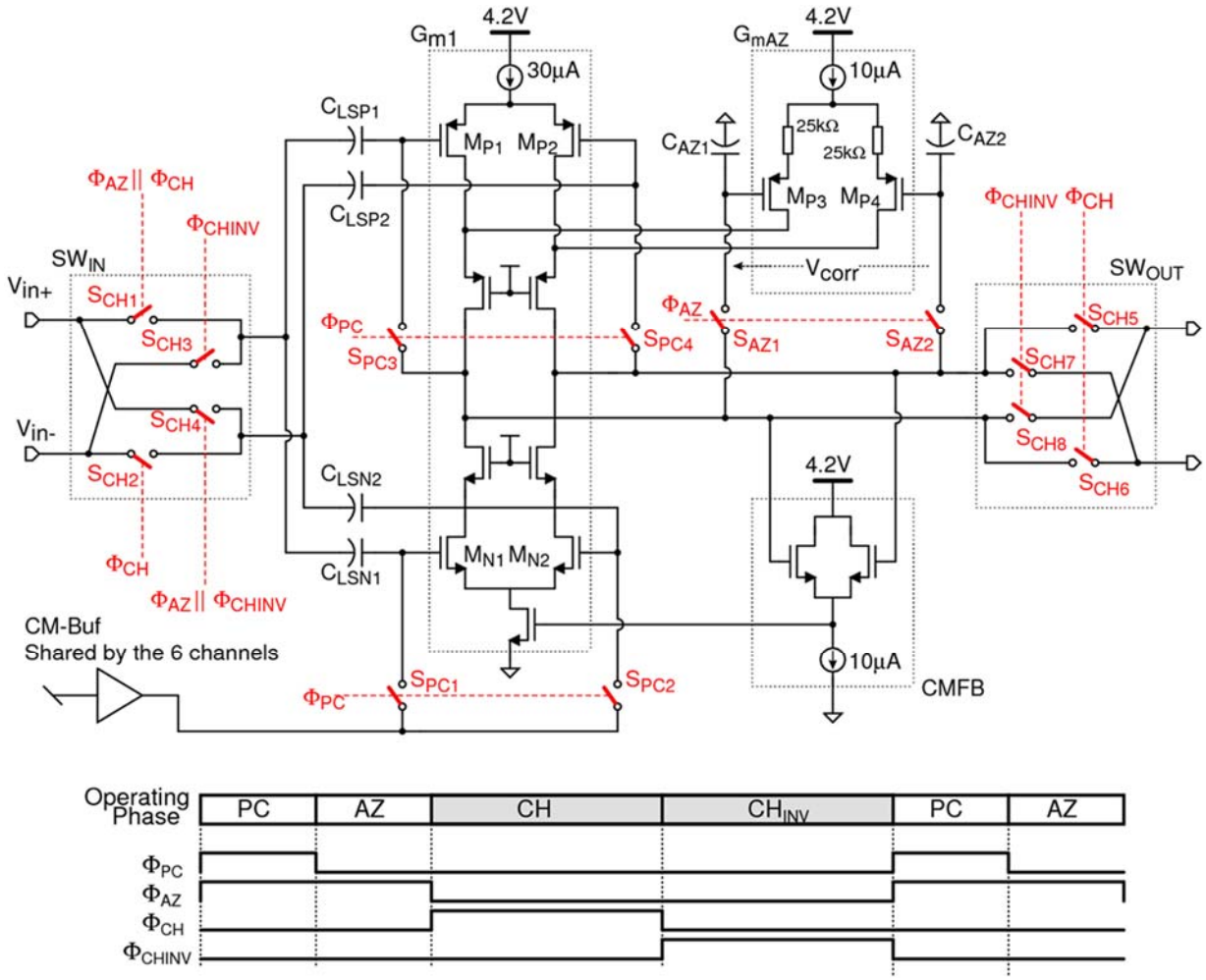

Figure 6-11: Circuit diagram of one input channel

6.4.2 One Channel Input Transconductor

Figure 6-11 presents a circuit diagram of a one input channel, incorporating the input switching circuit SW_{IN} and the capacitively-coupled auto-zeroed and chopped transconductor proposed in the previous sections. The input transconductor G_{m1} consists of an n-channel pair $M_{N1,2}$ and a p-channel pair $M_{P1,2}$. The two pairs share the bias current to realize a combined transconductance of 400µS in a power efficient manner. The input gates are coupled by four 1pF level shift capacitors $C_{LSN1,2}$ and $C_{LSP1,2}$ to receive level shifted input signals. $C_{LSP1,2}$ also work as coarse auto-zero capacitors in the pre-charge phase. To further reduce the residual offset, a fine auto-

zero is conducted by an auto-zeroed transconductor G_{mAZ} with another p-channel pair $M_{P3,4}$ and two 1pF auto-zero capacitors $C_{AZ1,2}$. A common-mode feedback circuit CMFB controls an NMOS tail current source, to keep the output common-mode voltage at 1.8V in all operating phases.

As discussed in Section 6.2.3, one channel goes through the pre-charge PC, the auto-zero AZ, the chopping CH, and the inverting-chop CH_{INV} phases. During the PC phase, a non-inverting input voltage V_{in+} charges the bottom plates of $C_{LSN1,2}$ and $C_{LSP1,2}$ through switches S_{CH1} and S_{CH4}. Meanwhile, the common-mode buffer CM-Buf charges the top plates of $C_{LSN1,2}$ through switches $S_{PC1,2}$. Additionally, switches $S_{PC3,4}$ form feedback around G_{m1} to charge the top plates of $C_{LSP1,2}$. At the end-of this phase, S_{PC1-4} turn off, and $C_{LSN1,2}$ and $C_{LSP1,2}$ become floating voltage sources. At the same time, a 3mV maximum initial offset for G_{m1} is sampled by $C_{LSP1,2}$, and thus auto-zeroed. Instead, a maximum charge injection mismatch Δq_{PC1-4} = 0.1fC flows into $C_{LSN1,2}$ and $C_{LSP1,2}$ and dominates the residual offset in this phase $V_{os,resPC}$ = 0.1fC/1pF = 100μV. In the next AZ phase, G_{mAZ} forms a fine auto-zero feedback through switches $S_{AZ1,2}$ to cancel $V_{os,resPC}$. It is degenerated with two 25kΩ resistors, so that the transconductance is only 25μS, i.e. 16 times lower than that of G_{m1}. The resulting correction voltage V_{corr} = $(G_{m1}/G_{mAZ})\bullet V_{os,resPC}$ is sampled by $C_{AZ1,2}$ along with the final residual error $V_{correrr}$. When the CH phase starts, the differential inputs and outputs of G_{m1} become connected to the signal path through the input and output switches $S_{CH1,2}$ and $S_{CH5,6}$. Moving to the CH_{INV} phase, SW_{IN} and SW_{OUT} invert the polarity by closing $S_{CH3,4}$ and $S_{CH7,8}$, to up-modulate the final residual error $V_{correrr}$ to the 1.2MHz chopping frequency f_{CH}.

Based on Equations (2-6) and (2-7), the magnitude of the up-modulated input error voltage V_{Gm1err} is given by:

$$V_{Gm1err} = \frac{G_{mAZ}}{G_{m1}} V_{correrr} = \frac{1}{A_{vAZ}} V_{os,resPC} \pm \frac{G_{mAZ}}{G_{m1}} \frac{\Delta q_{AZ}}{C_{AZ}}, \qquad (6\text{-}8)$$

where A_{vAZ} = 50dB is the loop gain of the fine auto-zero feedback, and $\Delta q_{AZ1,2}$= 0.05fC is the maximum charge injection mismatch of $S_{AZ1,2}$. Additionally, the sampled noise charge is added along with $\Delta q_{AZ1,2}$. First, $V_{os,resPC}$ = 100μV is suppressed by A_{vAZ}, only resulting in a 0.3μV error. Second, $\Delta q_{AZ1,2}$ is attenuated by G_{mAZ}/G_{m1} = 1/16, resulting in a 3.1μV error. The combined

3.4μV error per channel is averaged out with the other three channels operating in parallel, and thus further reduced to 1.7μV. It is insignificant, and thus is hidden by the 12.5nV/√Hz up-modulated sampled noise PSD at f_{CH}, as will be shown in the measurement result.

Thanks to the proposed dual coarse-fine auto-zero technique, G_{mAZ} only has to correct the 100μV maximum residual offset rather than the 3mV initial offset, resulting in two benefits. First, the maximum correction voltage V_{corr} is only 1.6mV, and thus does not cause a significant glitch when switching the six channels as explained in Section 3.2.4. Second, the fine auto-zero loop has the relaxed gain requirement, and thus can consist of a single transconductor stage without requiring the active integrator used in [14].

A high DC CMRR should be expected since $C_{LSN1,2}$ and $C_{LSP1,2}$ block the DC common-mode voltage. On the other hand, AC common-mode noise will be coupled to G_{m1}, and then rejected by the CMFB with a 4MHz loop bandwidth.

6.4.3 Second and Output Transconductors

Figure 6-12 presents the second and output stage transconductors G_{m2} and G_{m3} together. G_{m2} consists of a p-channel differential pair $M_{P21,22}$ followed by a folded cascode stage. The p-channel differential pair is supplied by the regulated 4.2V supply voltage, while the output common-mode voltage of G_{m1} is maintained at 1.8V. In the folded cascode stage, 60V NDMOS transistors $M_{N25,26}$ keep the potentials of four low side 5V NMOS transistors M_{N21-24} below 4V. Similarly, a 60V PDMOS transistor M_{P27} keeps the potentials of four high side 5V PMOS transistors M_{P23-26} within 4V of V_{SY}.

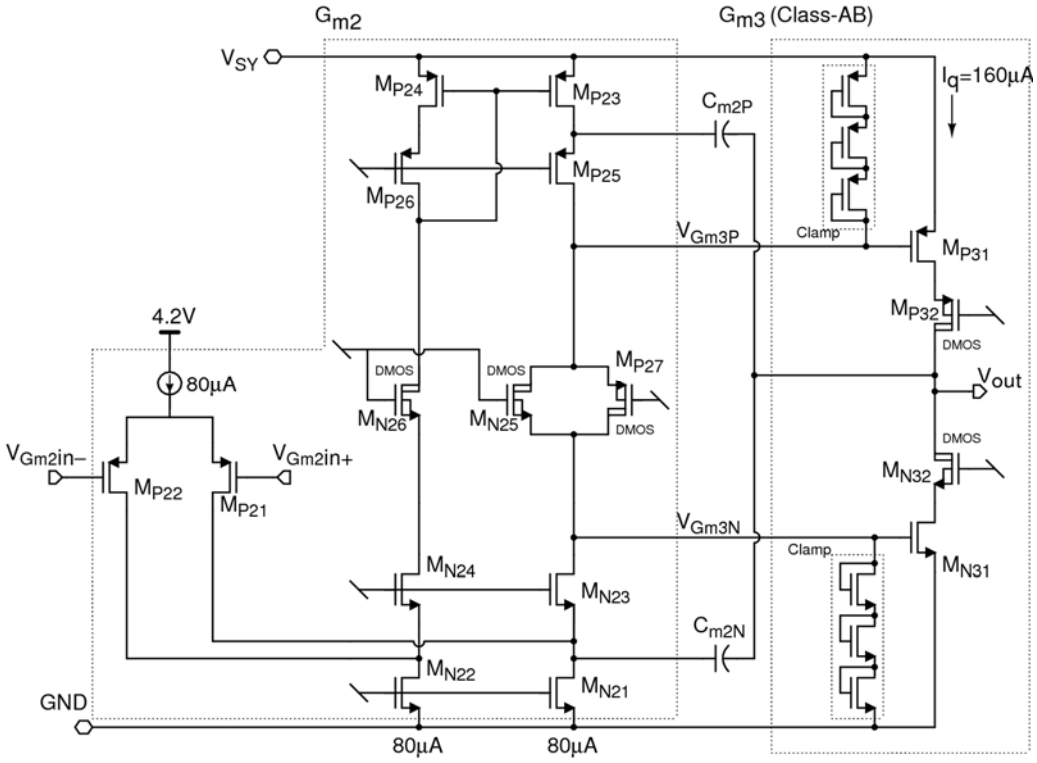

Figure 6-12: The second and output stage transconductors Gm2 and Gm3

The folded cascode stage drives the gates of low and high side transistors M_{N31} and M_{P31} to form a class-AB output transconductor G_{m3}. Each of these gate voltages V_{Gm3N} and V_{Gm3P} is clamped with three series diodes, and thus is kept within 4V of each supply rail even in the presence of output transient or overcurrent events. Additionally, cascode DMOS transistors M_{N32} and M_{P32} keep the drain potentials of M_{N31} and M_{P31} within 3V of each supply rail. Two 5pF frequency compensation capacitors C_{m2N} and C_{m2P} together represent C_{m2} in Figure 6-10, and they are fed back to the sources of M_{N23} and M_{P25}, respectively. This cascode Miller frequency compensation, as presented in [19], pushes the third pole, occurring at the output of G_{m3}, to a higher frequency, and thus reduces the current consumption of G_{m3} required to make the op-amp stable.

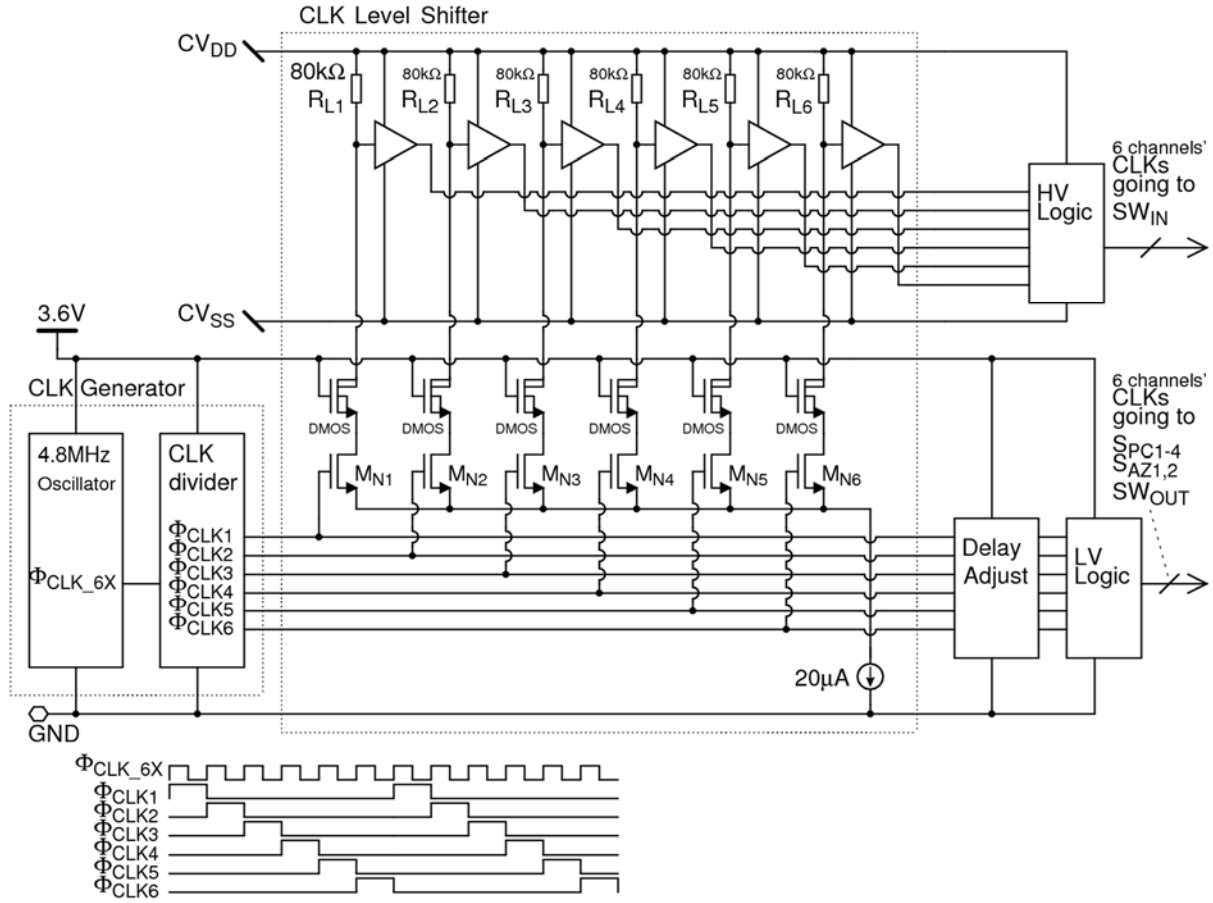

Figure 6-13: The clock generator and level shifter

6.4.4 Clock Generator and Level Shifter

Figure 6-13 presents the clock generator and level shifter, which provide the timing clocks to SW_{IN}, SW_{OUT}, S_{PC1-4}, and $S_{AZ1,2}$ in *Gm1_6chs*. The clock generator consists of a 4.8MHz oscillator and a clock divider to generate six interleaved 800kHz clocks Φ_{CLK1-6}. As shown in the figure, the clock generator is supplied by internally regulated 3.6V. The resulting 3.6V output clock level is sufficiently high to turn on the NMOS switches in SW_{OUT}, S_{PC1-4}, and $S_{AZ1,2}$, the source potentials of which are maintained at either 1.6V or 1.8V. On the other hand, as shown in Figure 6-7, the clocks need to be level-shifted to CV_{DD} and CV_{SS} in order to turn the NMOS switches in SW_{IN} on and off, respectively. The clock level shifter consists of a 20μA tail current source, six source-coupled input NMOS switches M_{N1-6}, six NDMOS cascode transistors, and six 80kΩ load resistors R_{L1-6} supplied by CV_{DD}. Based on Φ_{CLK1-6}, the 20μA current flows into either one of the

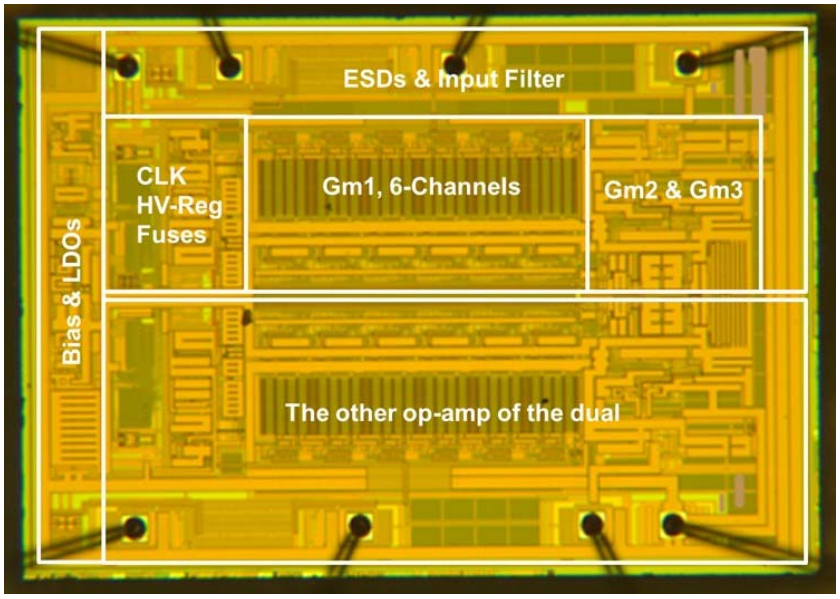

Figure 6-14: Die micrograph of the dual op-amp

switches $M_{N1\text{-}6}$, and then generates a 1.6V voltage drop across one of $R_{L1\text{-}6}$ to realize a logic-low state. Based on the six resulting level-shifted clock timings, the subsequent logic circuit will generate the required clocks to the SW_{IN} circuit in all six channels.

This clock level shifter circuit will add a clock delay in the order of 10ns. To adjust the clock delay, the clock path to SW_{OUT}, $S_{PC1\text{-}4}$, and $S_{AZ1,2}$ incorporates a delay adjustment circuit that consists of the same topology as the clock level shifter.

6.5 Measurement Results

Figure 6-14 presents the die micrograph of the proposed dual op-amp that occupies a 1.5mm x 2.1mm die area (1.58mm^2 per single op-amp). The ESD protection devices occupy 15% of the total area, and high voltage metal-metal fringing capacitors occupy another 15%. On the other hand, the digital circuit for the input bias current trimming only occupies 2.5% of the total area including the poly fuse memory array and the readout circuit. The op-amp is specified and tested over the supply voltage V_{SY} range from 4.5V to 60V, the input common-mode voltage V_{CM} range from the ground up to 1.5V below V_{SY}, and the temperature range from –40°C to 125°C.

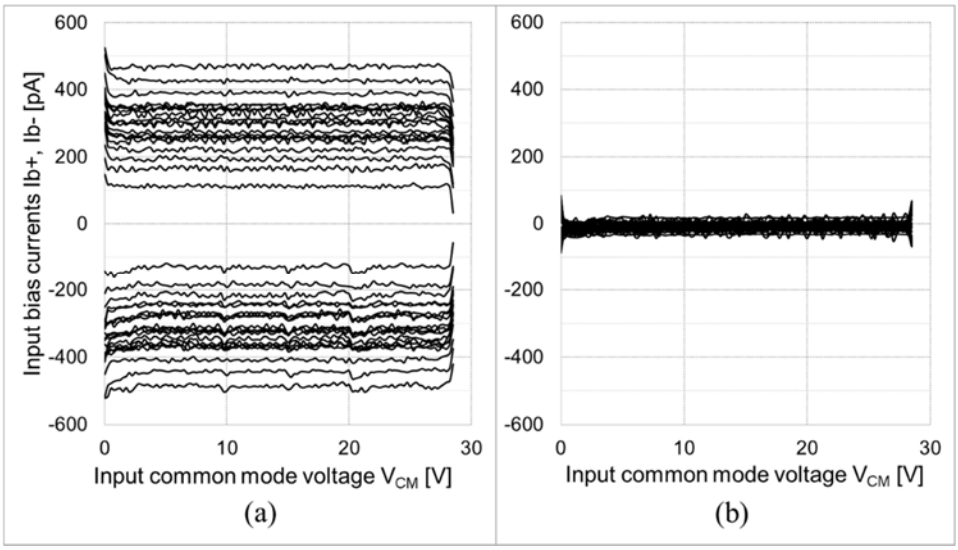

Figure 6-15: Input bias currents (a) before and (b) after the trimming

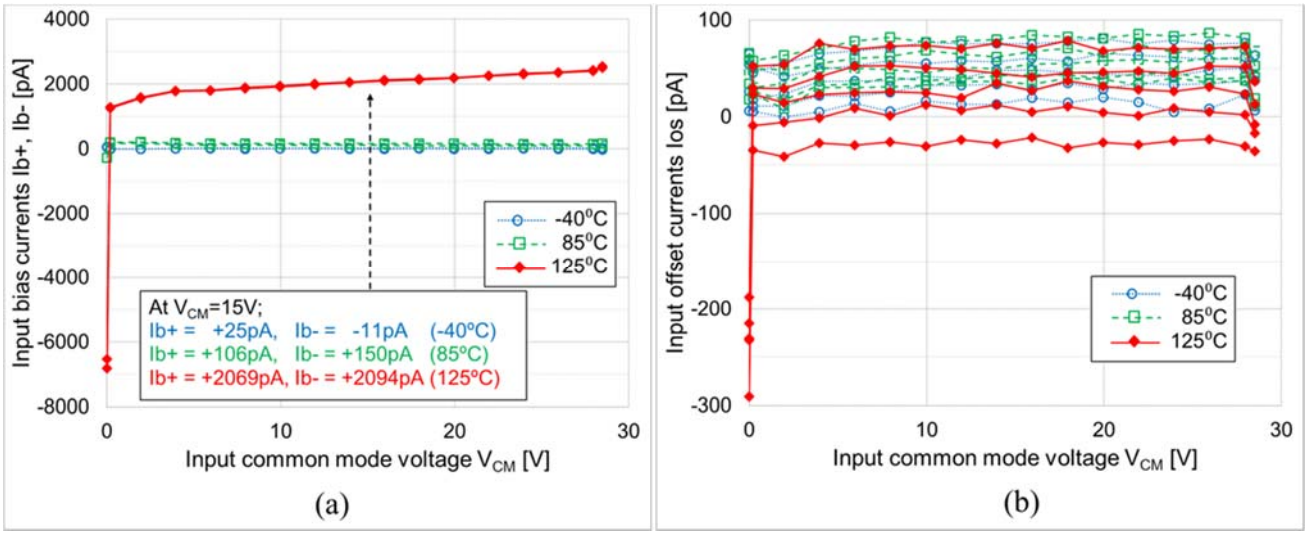

Figure 6-16: (a) Input bias currents and (b) offset currents over temperature

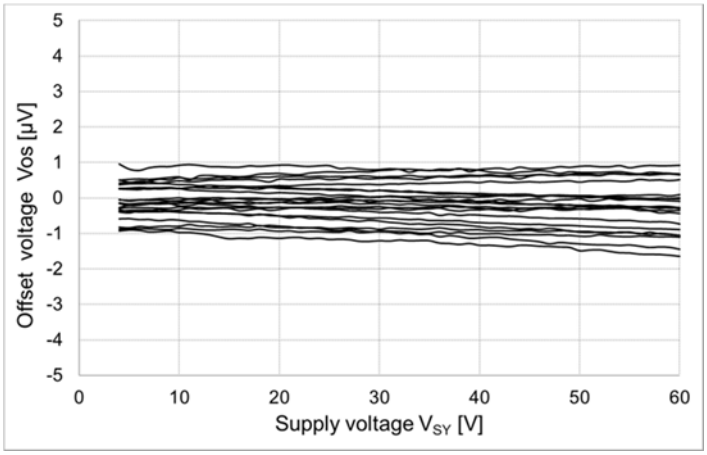

Figure 6-17: Offset voltages over supply voltage

Figure 6-15 (a) and (b) shows the input bias currents before and after the trimming, respectively. The same 20 op-amp units are tested with a V_{SY} of 30V and V_{CM} range of 0V to 28.5V. Before the trimming, the input bias currents are distributed up to ±500pA, all of which are almost constant thanks to the common-mode tracking regulator CM-Reg. These constant input bias currents can be corrected with a single bias point trimming with V_{SY} = 5.5V, V_{CM} = 2.75V, and ambient temperature. After the trimming, the worst-case input bias current is reduced to ±40pA in the middle of V_{CM}. This increases up to ±90pA near the upper and lower limits of the V_{CM} range, because one of the clock supply voltages CV_{SS} or CV_{DD} saturates near the ground or V_{SY}. After adding the error band due to the part-part distribution and the test inaccuracy, the maximum input bias current is specified at ±150pA which would be ±1.5nA without trimming. Figure 6-16 (a) shows the input bias currents of one op-amp unit at three different temperatures: –40°C, 85°C, and 125°C. At 125°C, the currents increase above +2nA due to the increased ESD diode leakage. Note that each input pin is clamped against VSY and GND pins through two diodes, and that the diode connected between input and GND generates more reverse leakage current due to its structure. Moreover, the currents at 125°C quickly drops below –6nA near V_{CM} = 0V, because the common-mode tracking regulator CM-Reg saturates, which drives the source-backgate diodes of the input chopper switches slightly into forward-bias condition. Figure 6-16 (b) shows the input offset currents of five op-amp units to evaluate residual charge injection mismatch over temperature. At 125°C, the offset currents drop to –300pA near V_{CM} = 0V due to the increased ESD diode leakage current mismatches. The input offset currents are less than ±100pA in any other conditions, demonstrating the temperature stability of the proposed charge mismatch compensation circuit. Figure 6-17 shows the offset voltages of the 20 op-amp units over a V_{SY} from 4.5V to 60V. Additionally, Figure 6-18 shows the offset voltages over a V_{CM} from 0V to 28.5V with V_{SY} = 30V. Similar to the input bias currents, any given unit exhibits relatively constant offset with the changes in V_{SY} and V_{CM}. As a result, the minimum DC CMRR and PSRR are 145dB and 150dB, respectively. Figure 6-19 (a) and (b) shows the histograms of the offset voltage and the temperature drift, the maximum values of which are well below ±5μV and 20nV/°C, respectively. Figure 6-20 shows the AC CMRR and PSRR versus the frequencies. More rejection is obtained when stimulating the V_{SY} pin (PSRR+), rather than the GND pin (PSRR–), because of the use of on-chip LDOs.

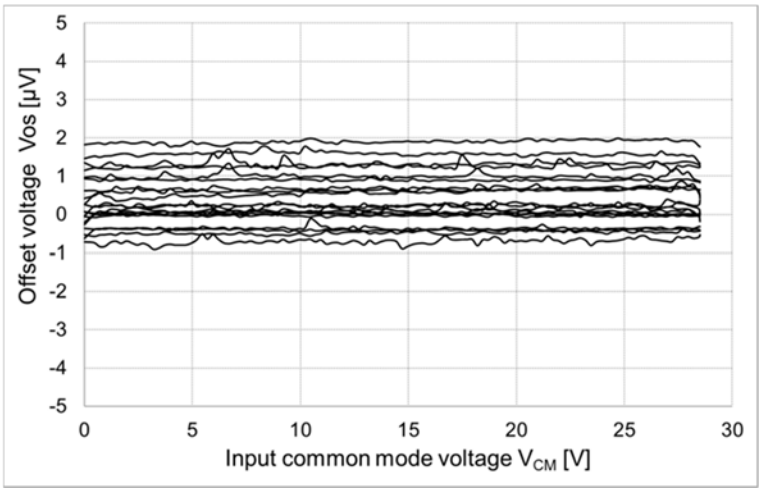

Figure 6-18: Offset voltages over specified V_{CM}

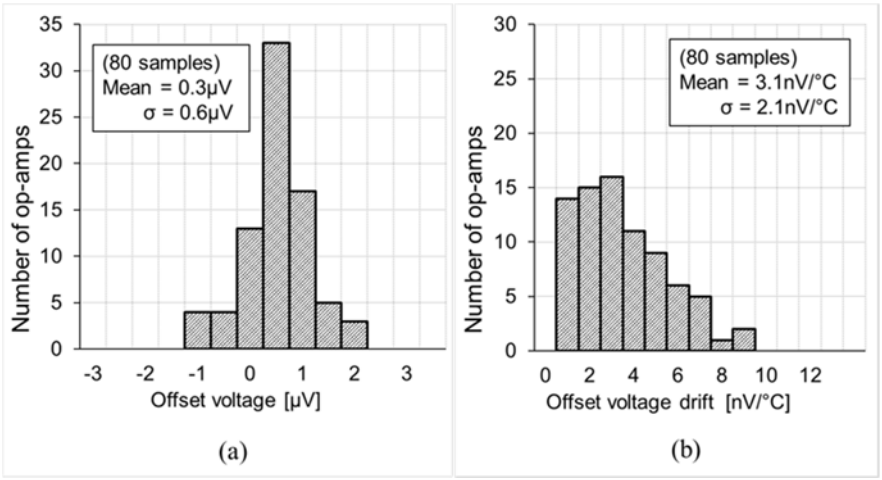

Figure 6-19: Histograms of (a) the offset voltage and (b) the temperature drift

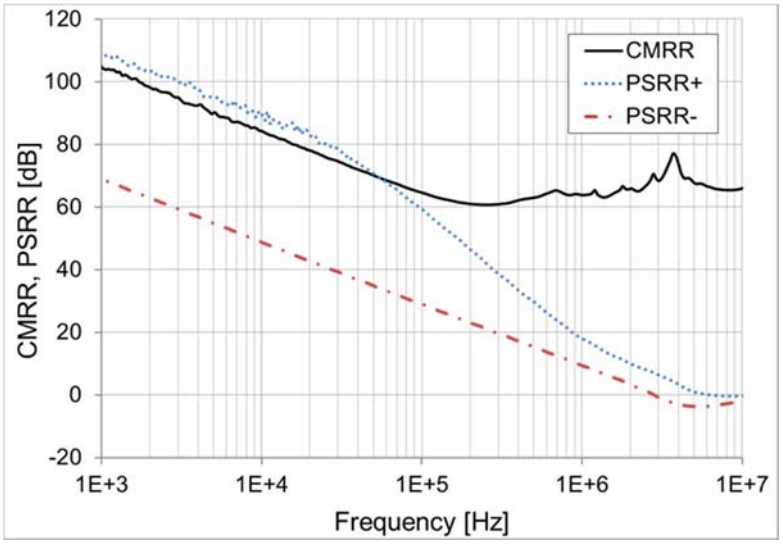

Figure 6-20: CMRR and PSRR over the frequency

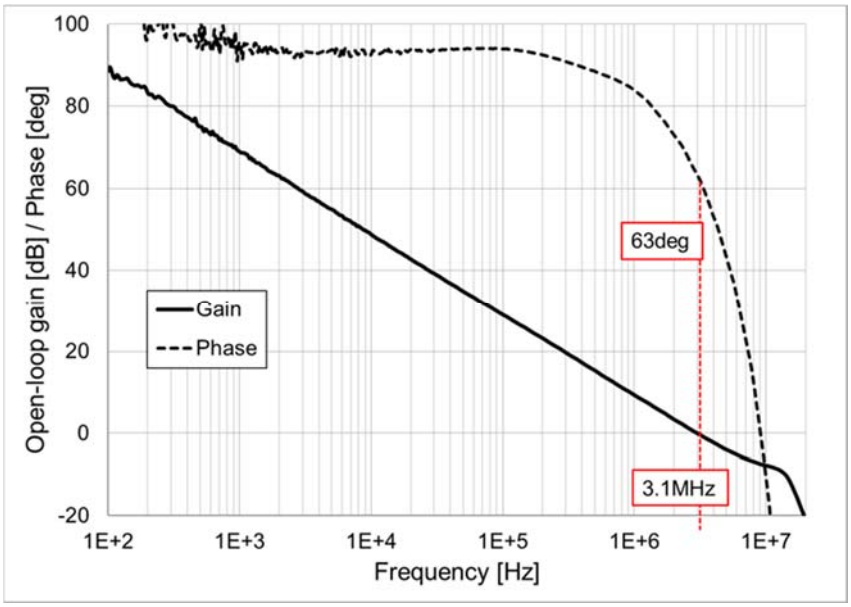

Figure 6-21: Open-loop gain and phase

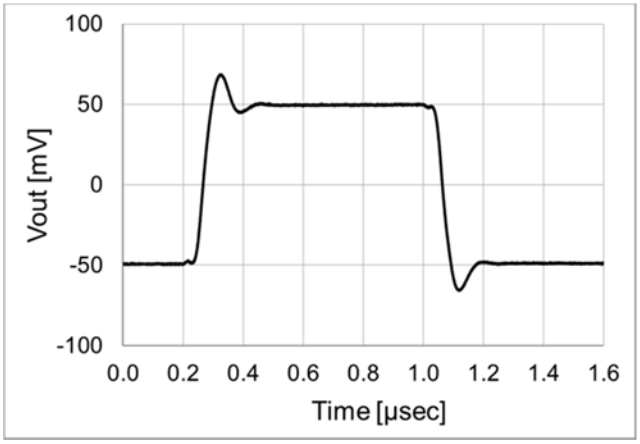

Figure 6-22: Step response with a 100mV signal

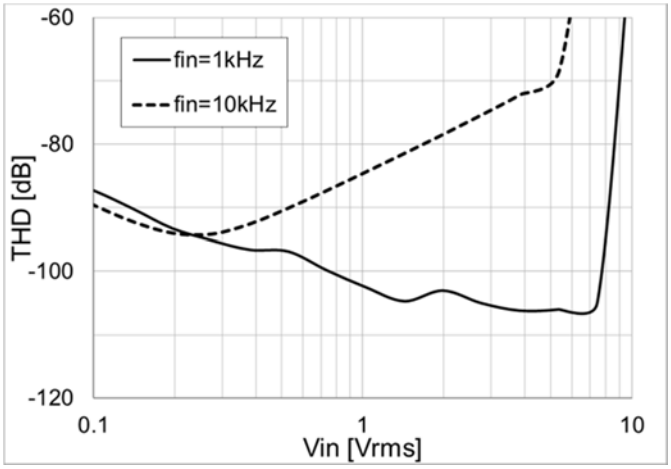

Figure 6-23: THD versus signal amplitude

Next, the measured AC performance is shown, while the op-amp is configured for unity gain with V_{SY} = 30V and is driving 100pF unless otherwise stated. Figure 6-21 shows the open-loop gain and phase. It can be seen that the op-amp achieves a 3.1MHz unity gain bandwidth f_u and a 63-degree phase margin *PM*. Testing twelve units with the three different V_{SY} at 5V, 30V, and 60V, the maximum variations in f_u and *PM* are ±0.24MHz and ±1.0 degree, respectively. No pole-zero doublet is observed below f_u, since the op-amp consists of a single gain path. Figure 6-22 shows the 100mV step response, where the output settles to a 0.1% error band with less than 0.4μs. Figure 6-23 shows the THD versus signal amplitude V_{in}. With the signal frequency f_{in} = 1kHz, it achieves a –106dB peak performance, and rises above –40dB when V_{in} increases beyond $10V_{rms}$ and approaches the supply rails. With f_{in} = 10kHz, it achieves a –95dB peak, and rises above –40 dB, when V_{in} increases beyond $7.5V_{rms}$ and reaches the slew rate limit.

Figure 6-24 shows the measured voltage noise PSD, along with the one simulated by the SpectreRF periodic noise analysis [23]. The measurement indicates a 5.8nV/√Hz in-band noise PSD and a 0.15Hz *1/f* noise corner frequency. At higher frequencies, it has two humps at 1.2MHz and 6MHz, as well as two peak PSDs at 800kHz and 4.8MHz. The first PSD hump of 12.4nV/√Hz is the up-modulated sampled noise as explained in Section 6.4.2. The second PSD hump of 23.0nV/√Hz is dominated by the thermal noise of G_{m2} and G_{m3}, due to the gain reduction of G_{m1} at a higher frequency. These measured humps and the in-band noise PSD are reasonably correlated with the simulation. On the other hand, the two peak PSDs are due to glitches caused by the charge injection, and thus are not included in the simulation. The magnitudes differ for each op-amp unit as shown in the histogram in Figure 6-25. Thanks to the proposed interleaving technique, the majority of the glitch energy is located at 4.8MHz. Consequently, 80% of the units have sufficiently low peak PSDs at 800kHz, which are hidden by the noise floor. The remaining 20% of the units show that the peak PSDs are higher than the noise floor, because of the mismatched glitch waveform among the six channels. With any degree of mismatch, the glitch energy at 800kHz is only a fraction of that at 4.8MHz, so that its maximum value is still 27.5 nV/√Hz among the 20 op-amp units.

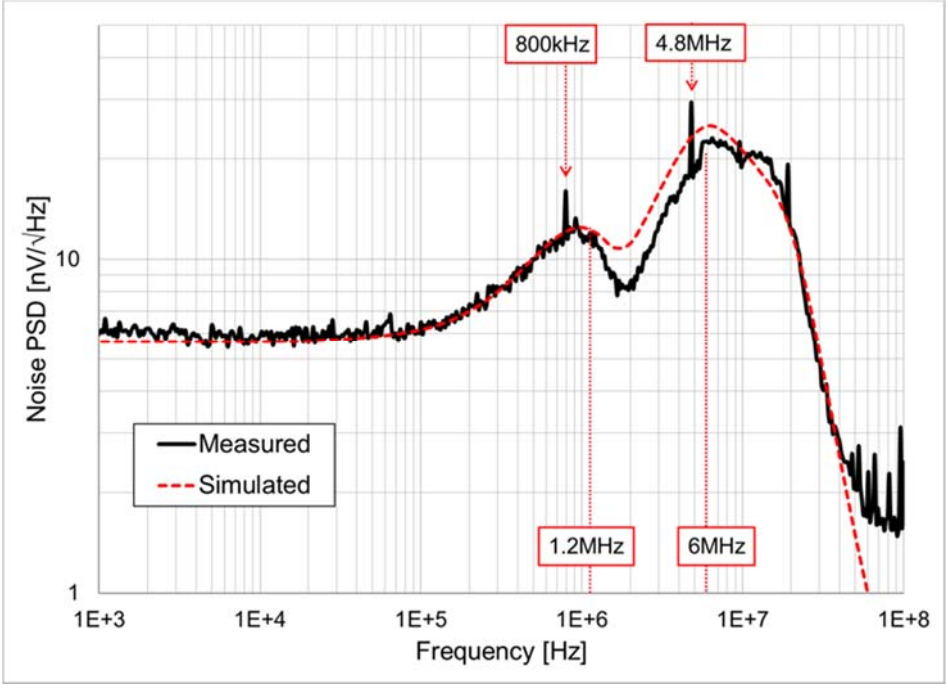

Figure 6-24: Measured and simulated noise PSD

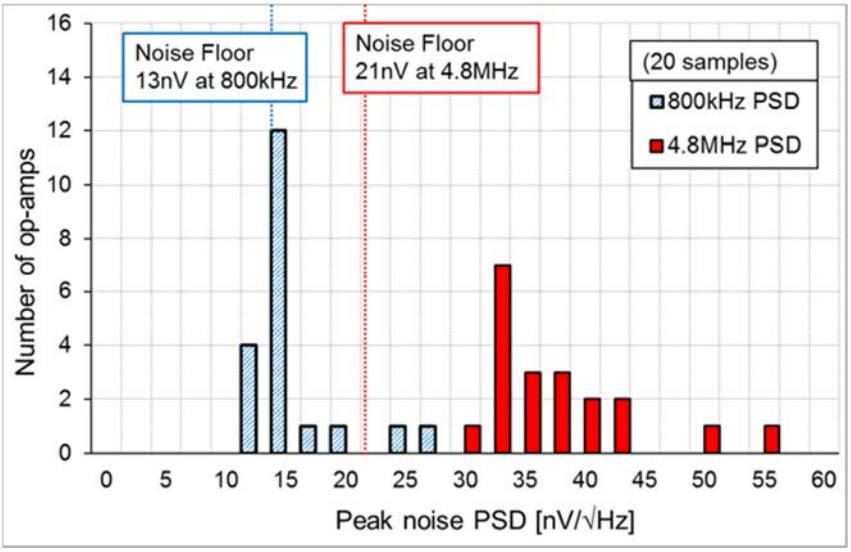

Figure 6-25: Histogram of the noise PSDs at 800kHz and 4.8MHz

Table 6-1 compares the overall performance with the other state-of-the-art precision op-amps above 20V operation. With the exception of one JFET op-amp [4], this work achieves the highest chopping frequency of 1.2MHz and the lowest in-band noise PSD of 5.8nV/√Hz among the other chopper op-amps [5,7,8,11]. Additionally, it achieves nearly the best DC specifications including a 20nV/°C maximum offset drift, a 150pA maximum input bias current, and a 145dB minimum CMRR.

Table 6-1: Comparison with other state-of-the-art

	This Work	[4]	[5]	[7]	[8]	[11]
Year	2015	2011	2011	2012	2013	2013
Max. Vsy [V]	60	40	36	36	60	* 20
Isy [µA]	840	1800	415	420	800	8
f_{CH} [kHz]	1200	JFET	333	60	100	50
Max. Vos [µV]	5	120	25	5	4	3
Max. Vos drift [µV/°C]	0.020	1.000	0.085	0.020	0.015	NS
Max. Ibias [pA]	±150	NS	±850	±600	±200	±107
Min. CMRR [dB]	145	NS	120	146	114	148
Min. PSRR [dB]	150	NS	130	148	133	120
GBW [MHz]	3.1	11.0	2.0	5.0	1.5	** 0.8
Slew Rate [V/µs]	1.3	20.0	0.8	3.8	0.45	NS
en [nV/√Hz]	5.8	5.1	8.8	9.0	10.5	55
NEF	6.5	8.3	6.9	7.1	11.4	6.1
Die area [mm^2]	1.58	2.1	NS	NS	NS	1.35

* Maximum input common mode range with the supply voltage of 5 V
** Stable with close loop gains greater than 20, *** NS = Data not shown

6.6 Conclusion

An auto-zero and chopper op-amp operating in the 4.5V to 60V supply range has been realized in the 0.18µm CMOS process augmented by 5V CMOS and 60V DMOS transistors. The input transconductor is capacitively-coupled and utilizes auto-zero and chopping techniques to achieve low offset, low ripple, and a wide input common-mode voltage range. The auto-zeroing consists of coarse and fine auto-zero phases to sufficiently reduce the residual ripple without requiring an active integrator stage. Moreover, it employs six parallel input channels with 800kHz interleaved clocks to mitigate the glitches caused by charge injection. This pushes the majority of the glitch energy up to 4.8MHz, while leaving the residual energy at 800kHz due to channel-channel mismatches. It relaxes requirements of the low-pass filter, and thus achieves a wider usable signal bandwidth. Furthermore, the trade-off between the chopping frequency and the DC performance is overcome by the post-production trimming with the on-chip charge mismatch compensation circuit, reducing the maximum input bias current from 1.5nA to 150pA.

6.7 References

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Chapter 7

Conclusion

This chapter summarizes the work accomplished in this thesis and draws some conclusions. First, Section 7.1 compares the performances among the three proposed chopper op-amps, and reviews their evolution. In particular, a comparison is presented of the DC errors and the noise PSD peaks due to switching artifacts, so that the proposed switching artifact reduction techniques can be evaluated. Next, Section 7.2 compares the achieved performances with the other state-of-the-art designs. In Section 7.3, some suggestions for future work are presented. Lastly, Section 7.4 lists the original contributions of this work.

Table 7-1: List of the proposed circuit techniques in the three chapters

	Chapter 4	Chapter 5	Chapter 6
Ripple reduction	ACFB	ACFB + active integrator	6-channel auto-zero + chopper
Charge injection: glitch reduction	--	--	6-channel CLK interleaving
Charge injection: V_{CM} dependency reduction	--	V_{CM} tracking CLK supplies	V_{CM} tracking CLK supplies
Charge injection: mismatch reduction	--	--	Charge mismatch compensation circuit
Op-amp signal path	LFP + HFP	LFP + HFP	Single path

Table 7-2: Performance comparison of the three proposed op-amps

	Chapter 4	Chapter 5	Chapter 6
Year	2009	2011	2015
Vsy range [V]	1.8 – 5.5	2.1 – 5.5	4.5 – 60
Isy [µA]	13	1400	840
f_{CH} [kHz]	50	200	1200
Max. Vos [µV]	10	0.5	5
Max. Vos drift [µV/°C]	0.070	0.015	0.020
Max. Ibias [pA]	±50	±400	±150
Min. CMRR [dB]	105	142	145
GBW [MHz]	0.12	4.0	3.1
en [nV/√Hz]	95	5.6	5.8
NEF	13.2	8.1	6.5
Technology Node [µm]	0.35	0.35	0.18
Die area [mm^2]	0.64	1.26	1.58

7.1 Evolution over the Three Projects

Chapters 4, 5, and 6 each presented the individual chopper op-amp design [1-3]. Table 7-1 shows the proposed circuit techniques that mitigate the switching artifacts of chopping. In Chapter 4, auto-correction feedback (ACFB) is proposed to reduce the up-modulated ripple. In the op-amp of Chapter 5, the residual ripple is further reduced by adding an active integrator to the ACFB. The ACFB creates a notch which is bypassed and hence buried by adding a high frequency path (HFP). However, the signal transfer function mismatch between the two signal paths creates a pole-zero doublet, making this approach not well suited for wideband applications. On the other hand, the op-amp in Chapter 6 employs a combination of auto-zeroing and chopping to reduce

chopper ripple without introducing a notch into the signal transfer function. Therefore, this op-amp consists of a single gain path and can be used in wideband applications. Moreover, the input transconductor consists of six channels, four of which amplify the signal in parallel to improve its power and area efficiency compared to the ping-pong auto-zero-and-chopper op-amp [4]. Furthermore, the six channels operate with 800kHz interleaved clocks, which pushes the majority of the glitch energy up to 4.8MHz.

While the op-amp in Chapter 4 has a 95nV/√Hz noise PSD, those in Chapters 5 and 6 achieve noise PSDs of below 6nV/√Hz, which require wider input switches, and hence more charge injection is generated. To mitigate this problem, the input switches in the Chapters 5 and 6 op-amps are driven by local clock supply voltages that track the common-mode voltages. With this technique, their charge injection is minimized and maintained independent of changes in the supply and common-mode voltages, resulting in a low input bias current, a low residual offset, and a high CMRR. The input bias current in Chapter 6 is further reduced by post-production trimming using the proposed on-chip charge injection mismatch compensation circuit.

Table 7-2 compares the performance of the op-amps in the three chapters. A higher chopping frequency is used in the later chapters. The offset, offset drift, and CMRR are improved from Chapter 4 to 5, primarily thanks to the adaptive clock boosting technique. These DC specifications still remain competitive in Chapter 6, even though the chopping frequency increases up to 1.2MHz. The input bias current increases from Chapter 4 to 5, due to the higher chopping frequency and wider input switches. It is reduced to 150pA in Chapter 6 by post-production trimming with the help of an on-chip charge mismatch compensation circuit. The die area increases from Chapter 4 to 5 primarily as a result of targeting a lower noise PSD, and from Chapter 5 to 6 primarily due to the larger area of the high voltage ESD protection devices and high voltage capacitors. The NEF also improves over the three projects.

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[4] The integrated RMS noise increases by 26.5μV_{rms}, 9.1μV_{rms}, and 2.7μV_{rms}, respectively, as a result of the noise PSD peaks at these frequencies.

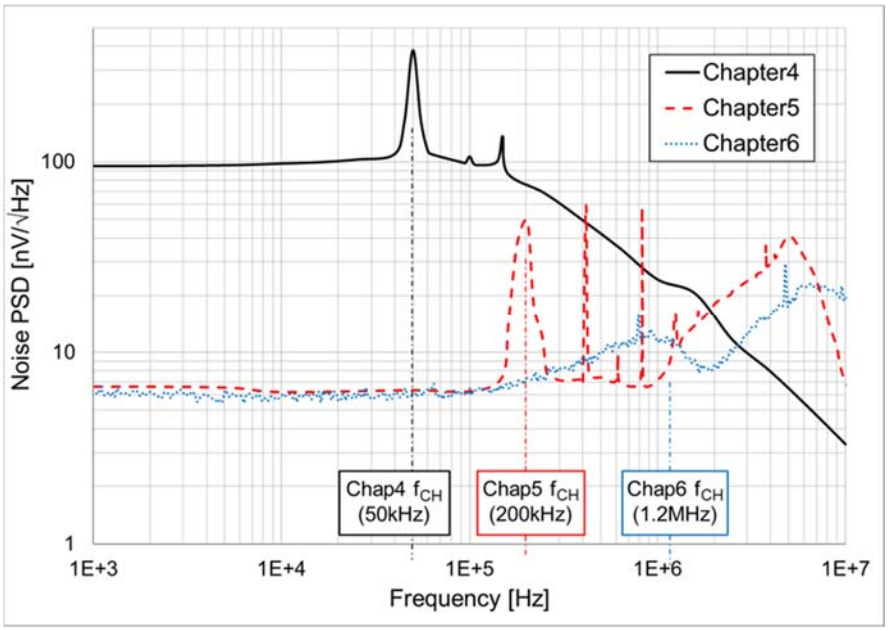

Figure 7-1: Noise PSD comparison of the three proposed op-amps

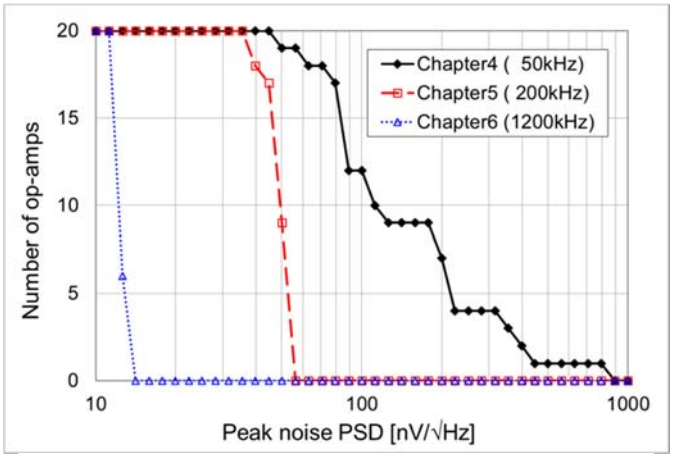

Figure 7-2: Cumulative chart of the ripple PSD

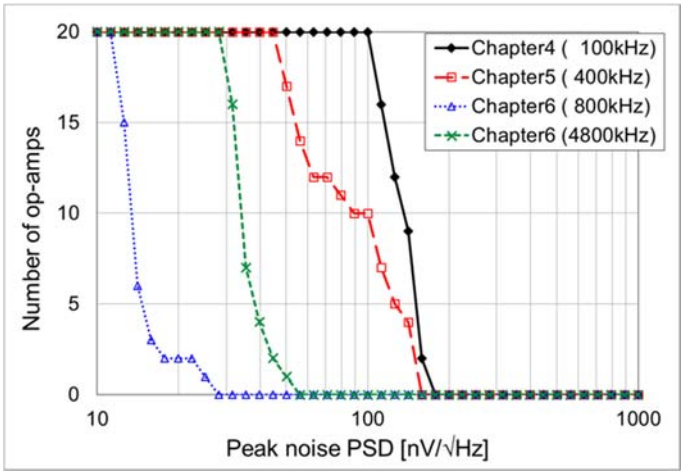

Figure 7-3: Cumulative chart of the PSD due to glitches

Figure 7-1 compares the noise PSDs of the three op-amps. All of them increase at the chopping frequencies f_{CH} = 50kHz, 200kHz, and 1.2MHz[4] due to the up-modulated ripple. Additionally, in Chapters 4 and 5, glitches due to charge injection cause noise PSD peaks at $2 \cdot f_{CH}$. On the other hand, in Chapter 6, the clock interleaving technique pushes the noise PSD peak up to 4.8MHz, while leaving a residual peak PSD at 800kHz.

Figure 7-2 shows the cumulative chart of the ripple PSD magnitude at f_{CH} by testing 20 op-amp units from each chapter. In Chapter 4, the PSD is widely distributed from 45nV/√Hz to 800nV/√Hz, since it is dominated by the initial offset in conjunction with the finite loop gain of the ACFB. In Chapter 5, the loop gain of the ACFB is increased by the added active integrator, which sufficiently reduces the initial offset. However, the thermal noise of the active integrator is sampled in the SC-NF without being effectively band-limited, and is then up-modulated to dominate the 50nV/√Hz noise PSD peak. In Chapter 6, the initial offset is sufficiently reduced by the dual coarse-fine auto-zero technique with the single auto-zeroing transconductor stage, resulting in a relatively low noise PSD peak in the range of 12nV/√Hz to 13nV/√Hz.

Similarly, Figure 7-3 shows the cumulative chart of the peak PSD magnitude due to glitches. In Chapter 4, the PSD is contributed both by the thermal noise floor and the glitches, and thus remains relatively constant in the range of 100nV/√Hz to 150nV/√Hz. In Chapter 5, on the other hand, it has a lower thermal noise floor but higher glitch energy due to wider input switches. Consequently, the peak PSD is widely distributed from 46nV/√Hz to 158nV/√Hz due to various random glitch factors. In Chapter 6, the majority of the glitch energy is located at 4.8MHz, the magnitude of which is distributed from 29nV/√Hz to 54nV/√Hz. At 800kHz, 16 units out of 20 show a noise PSD below 13nV/√Hz without a peak, while the remaining 4 units show the peak PSDs distributed up to 26nV/√Hz due to the mismatch of the glitches among the six channels.

Based on the noise PSD in Figure 7-1, Figure 7-4 shows the integrated RMS noise over frequency. Below f_{CH}, the integrated noise increases linearly over frequency due to the constant in-band noise floor. The integrated noise of the designs in Chapter 4 and 5 quickly increase above f_{CH} = 50kHz and 200kHz, respectively, due to relatively high peak PSDs. On the other hand, the integrated noise of the design in Chapter 6 only increases slightly above f_{CH} = 1.2MHz, thanks to the proposed switching artifact reduction techniques. This provides significant

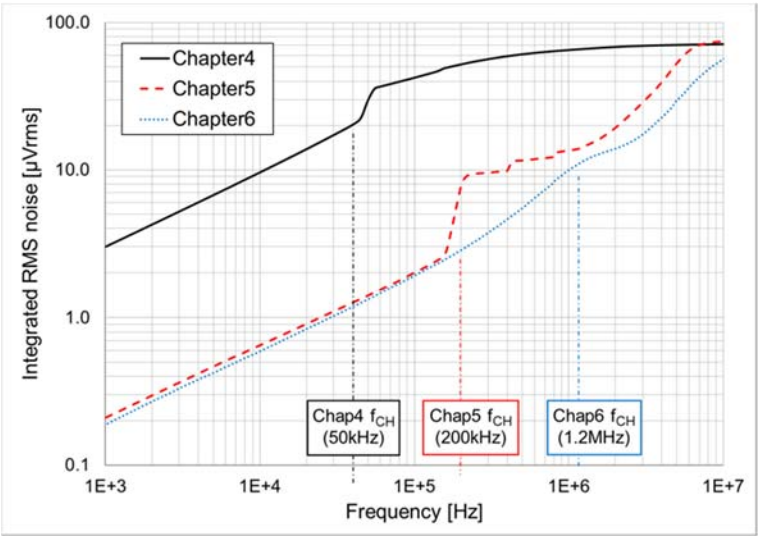

Figure 7-4: Integrated RMS noise over the frequency

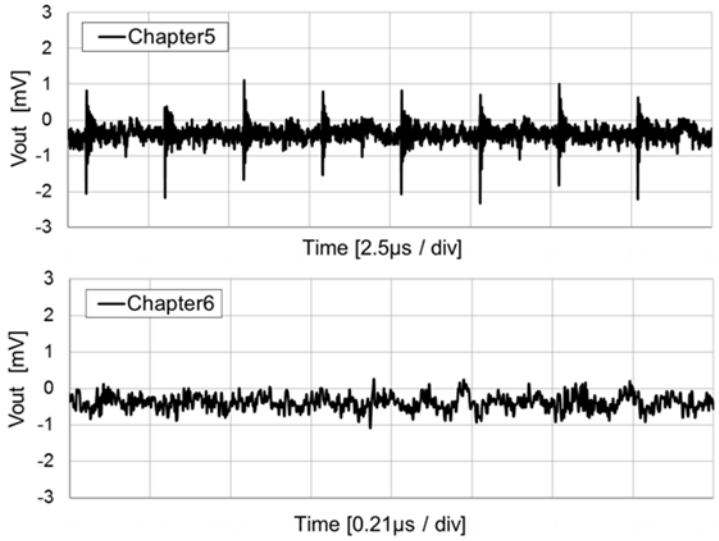

Figure 7-5: Transient output waveforms

advantages, for instance reducing the integrated noise within a given signal bandwidth and/or extending usable signal bandwidth with a given integrated noise target. For instance, for a 500kHz bandwidth, the integrated noise of the designs in Chapter 5 and 6 are 11.6µV_{rms} and 5.4µV_{rms}, respectively. From another perspective, to target 10µV_{rms} input-referred noise, the usable signal bandwidths of the designs in Chapter 5 and 6 are 400kHz and 1MHz, respectively. Figure 7-5 shows the measured transient output waveforms of the op-amps configured for unity gain. The design in Chapter 5 clearly shows 1.5mV peak glitches that can cause errors in subsequent stages if not filtered. On the other hand, the glitches are invisible in the design in Chapter 6.

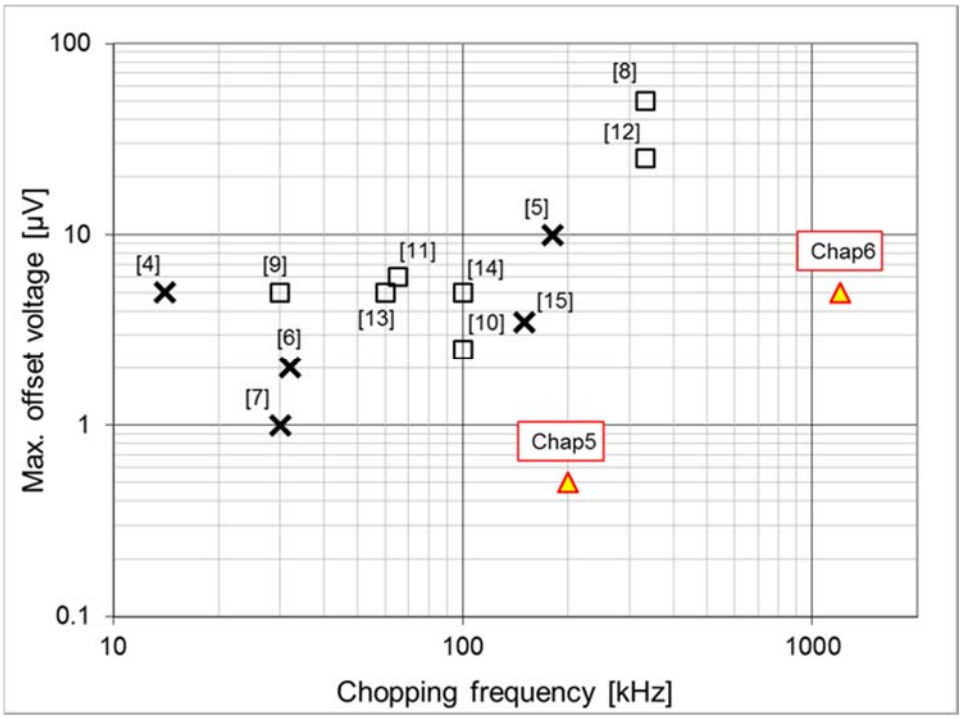

Figure 7-6: Maximum offset versus chopping frequency of the proposed and previous chopper op-amps

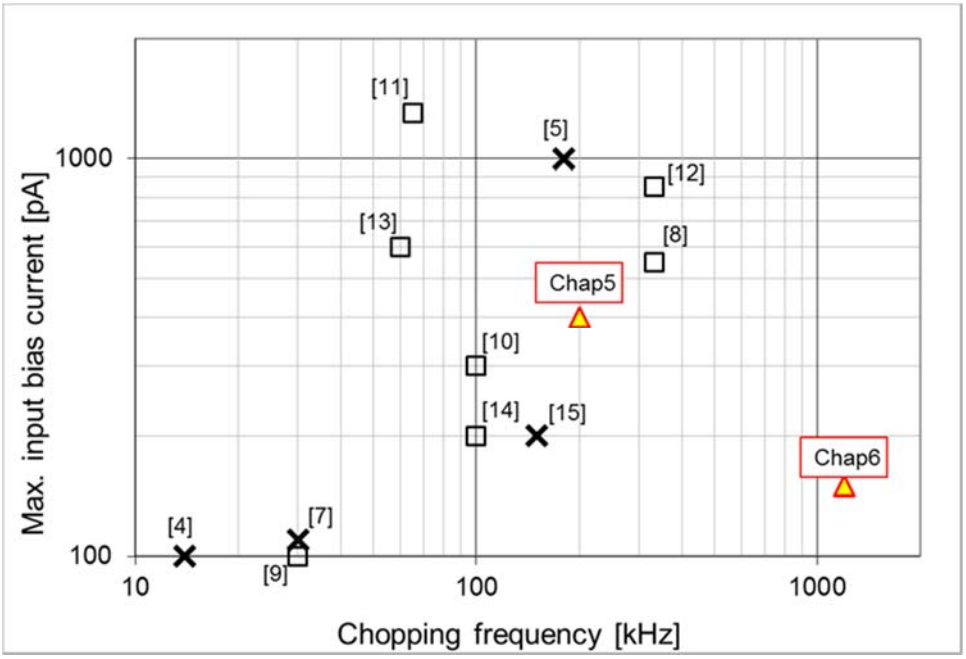

Figure 7-7: Maximum input bias current versus chopping frequency of the proposed and previous chopper op-amps

7.2 Benchmark

As explained in Section 2.4, chopper op-amp design involves trade-offs between the DC errors, the chopping frequency, and the noise PSD. To compare these specifications among different designs, Figure 7-6 plots the chopping frequency versus the maximum offsets, and Figure 7-7 plots the chopping frequency versus the maximum input bias currents. The plots [4-14] are the specifications of previous state-of-the-art chopper op-amps that were reported before 2013, and have less than 20nV/√Hz noise PSD. Note that the specifications derived from conferences or journals are marked by crosses, while those derived from the datasheets of commercial products are marked by squares. It can be seen that their offsets and input bias currents tend to increase with chopping frequency, and are typically greater than 10μV and 500pA, respectively, for chopping frequencies above 200kHz.

The work described in this thesis proposed design techniques that simultaneously achieve low DC errors and a high chopping frequency. As plotted in Figure 7-6 and Figure 7-7, the work in Chapter 5 (first reported in 2011) achieved a 0.5μV maximum offset and a 400pA maximum input bias current with a 200kHz chopping frequency, and then the work in Chapter 6 (first reported in 2015) achieved a 5μV maximum offset and a 150pA maximum input bias current with a 1.2MHz chopping frequency.

In 2016, Ivanov reported another state-of-the-art chopper op-amp that employs a ripple reduction loop, where a switched-capacitor notch filter is used in the same manner as the ACFB, but its ripple sensing input is capacitively-coupled to the main signal path [15]. This work achieved a 3.5μV maximum offset, a 200pA maximum input bias current, and a 6.5nV/√Hz voltage noise PSD with a 150kHz chopping frequency, while drawing 1.625mA current from a 1.8-5.5V supply.

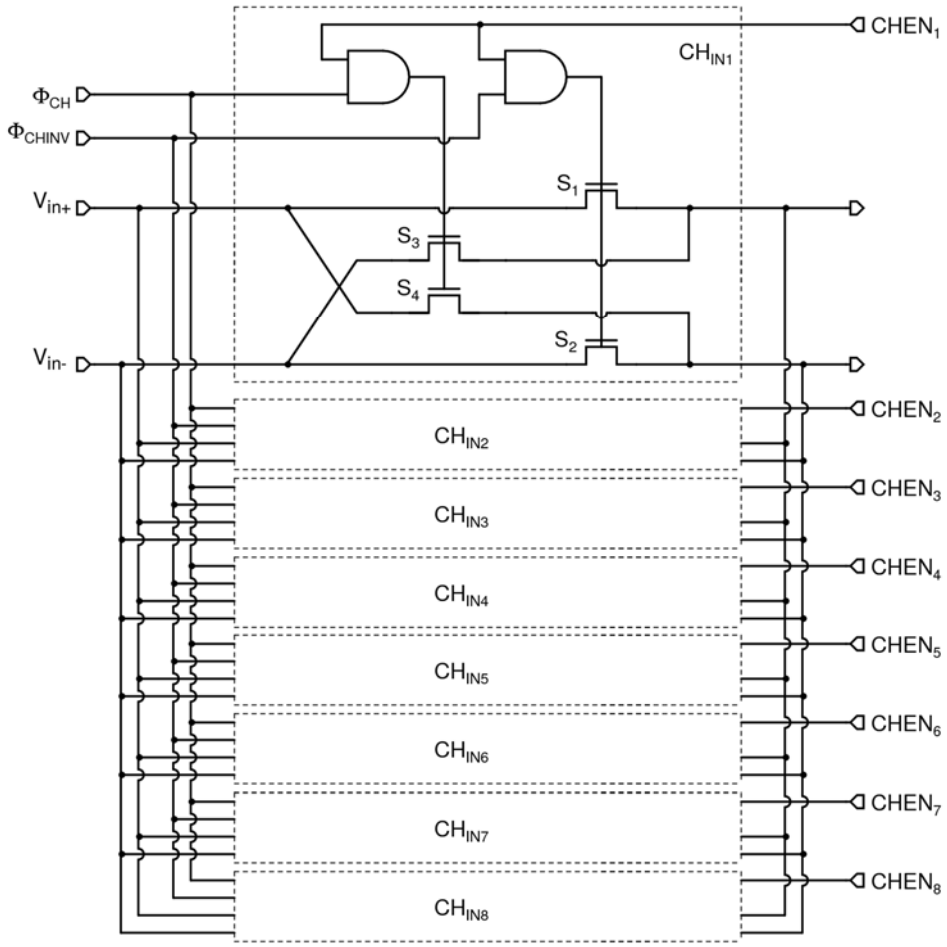

Figure 7-8: Proposed input chopper for low input bias current

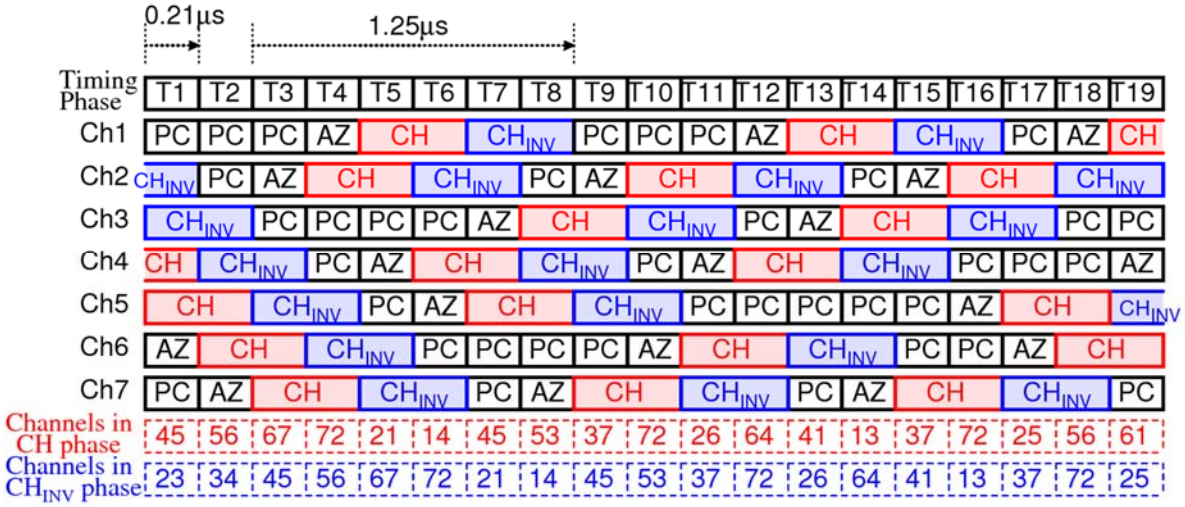

Figure 7-9: Proposed timing diagram for seven input channels with random sequencing

7.3 Future Work

In Chapter 6, a charge mismatch compensation circuit was proposed, with which an op-amp achieved a 150pA maximum input bias current with a 1.2MHz chopping frequency. By using this technique with a chopping frequency below 100kHz, an input bias current less than a few tens of pico-Ampere should be achievable. However, there are applications that require even lower input bias current, such as photodiode current detection and electrochemical sensor signal acquisition [16]. Therefore, a future project would be to design a chopper amplifier that simultaneously achieves low offset and a sub-pA input bias current.

One drawback of the charge mismatch compensation circuit is that it generates extra charge injection, which possibly increases the magnitude of transient glitches. Another drawback is that the accuracy of the input bias current cancellation is limited by the accuracy of the DAC, which consists of bias current array, poly resistors, and coupling capacitors.

A proposed input chopper for future project is presented in Figure 7-8, where eight identical input chopper channels CH_{IN1-8} are connected in parallel. Each chopper channel is driven by common chopping clocks Φ_{CH} and Φ_{CHINV}, as well as separate enable bit $CHEN_{1-8}$. In each chopper channel, Φ_{CH} and Φ_{CHINV} are gated by $CHEN_{1-8}$, so that the switching action can be disabled. In production testing, by controlling $CHEN_{1-8}$, the input bias current of each chopper channel can be measured separately. After measuring all the chopper channels, for instance, 4 chopper channels out of the total 8 can be enabled, in order to achieve the lowest combined input bias current.

As long as the input bias current of every chopper channel is randomly spread between positive and negative values, the combined input bias current can be indefinitely reduced by increasing the number of total chopper channels. For instance, total 16 chopper channels can be implemented, and 4 chopper channels out of the 16 can be enabled, which will achieve lower combined input bias current than the circuit presented in Figure 7-8. Furthermore, this technique does not generate extra charge injection. One drawback is that disabled chopper channels will add extra input capacitance, and will add extra die area. Besides input current due to charge injection mismatch, leakage current from ESD diodes could be reduced by connecting such

diodes to the buffered input voltage, instead of supply voltages [17].

Another future project would be to further reduce the spectral peak associated with transient glitches. In the design of Chapter 6, the majority of the glitch energy was pushed up to 4.8MHz, by driving six parallel input channels with 800kHz interleaved clocks. However, there is still residual energy left at 800kHz, because, due to channel-channel mismatch, one input channel would still generate a large transient glitch which would then occur every 1.25µs (800kHz frequency).

A proposed technique for a future project would be to randomly sequence the phase of every channel, rather than to sequence them with a fixed order. Figure 7-9 presents its proposed timing diagram for seven input channels ($Ch_{1\text{-}7}$), which contains one additional channel compared to the circuit in Chapter 6. Similar to the timing diagram presented in Figure 6-5 (b), each channel goes through pre-charge PC, auto-zero AZ, chopping CH, and inverting-chop CH_{INV} phases. With one additional channel, total two channels are in the PC phase in one timing phase. Then, in the next timing phase, one channel out of the two is randomly selected to be advanced to the AZ phase, while the other channel stays in the PC phase. For instance, in the timing phase T_1, Ch_1 and Ch_7 are in the PC phase. In the next timing phase T_2, Ch_7 is selected to be advanced to the AZ phase, Ch_1 stays in the PC phase, and Ch_2 is advanced to the PC phase.

As in the Chapter 6 design, two channels are in the CH phase and other two channels are in the CH_{INV} phase at a time (total four channels are in the signal path), so that the overall amplifier will achieve the same low frequency noise PSD and signal bandwidth specifications. On the other hand, the combination of those four channels will be different after a period of 1.25µs, so that a fixed-amplitude transient glitch will not repeat every 1.25µs. For instance, while Ch_6 and Ch_7 are in the CH phase in T_3, Ch_3 and Ch_7 are in the CH phase in T_9 (1.25µs later). Consequently, the residual spectral peak at 800kHz will be spread out in the frequency domain. One drawback of this proposed technique is the additional current consumption and die area for one extra input channel.

7.4 Original Contributions

- The invention of the auto-correction feedback (ACFB) loop (Chapter 4)
- Full analysis of the ACFB loop (Chapter 4)
- The invention of a frequency compensation technique using a current attenuator and a dummy differential output (Chapter 5)
- The invention of an adaptive clock boosting technique in an input chopper (Chapter 5)
- The realization of a capacitively-coupled auto-zeroed and chopped transconductor (Chapter 6)
- The realization of a multi-channel auto-zeroed and chopped transconductor with interleaved clocks (Chapter 6)
- The invention of input bias current trimming using an on-chip charge mismatch compensation circuit (Chapter 6)
- A comparison of the performance of different switching-artifact reduction techniques (Chapter 7)

7.5 References

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Summary

This thesis describes the theory, design, and implementation of chopper operational amplifiers (op-amps) in CMOS integrated circuits (ICs). The chopping technique periodically corrects DC errors of such op-amps, so that low 1/*f* noise and stable, microvolt-level offset can be achieved. However, chopping causes switching artifacts at the amplifier's output, e.g. up-modulated ripple and glitches, which are usually attenuated by low-pass filtering. Therefore, chopper op-amps have mainly been limited to low frequency applications. In this thesis, advanced circuit techniques are proposed to attenuate such switching artifacts without decreasing the usable signal bandwidth, thus enabling the use of chopper op-amps in a broader range of applications. Three chopper op-amps are designed, fabricated, and measured, so that the proposed techniques can be evaluated and compared with those of the other state-of-the-art designs.

In Chapter 1, the advantages and disadvantages of CMOS chopper op-amps compared to traditional bipolar op-amps are discussed. Without any offset cancellation techniques, CMOS op-amps usually suffer from higher offset, temperature drift, and thermal and 1/*f* noise than bipolar op-amps, given the same die size and current consumption. On the other hand, bipolar op-amps are ruled out in many applications due to their manufacturing cost, high input bias current, and difficulty of co-integration with CMOS ADCs and DACs. Additionally, digital logics and analog switches can be easily implemented in CMOS process, which enables the use of dynamic offset cancellation techniques such as auto-zeroing and chopping. These techniques can reduce maximum offset and maximum offset drift of amplifiers to less than 10μV and 0.1μV/°C, respectively, which can hardly be matched by bipolar op-amps.

In this chapter, traditional applications of chopper op-amps in sensor signal conditioning and current sensing are reviewed. In such applications, signal frequencies are relatively low and so switching artifacts can be attenuated by low-pass filtering. Signal source impedances are also low, so that some input bias current can be tolerated. Next, newer applications of chopper op-amps are reviewed, such as in DAC buffers and industrial process control, in which signal frequencies are too high for the use of low-pass filtering to suppress switching artifacts. In certain applications, e.g. biomedical sensing, source impedances can be quite high, and so input

bias currents must be less than 100pA.

In Chapter 2, in addition to the chopping technique, other offset cancellation techniques—offset trimming and auto-zeroing—are reviewed. Trimming only corrects offset at post-production test, and thus still results in high offset drift and 1/*f* noise. Like chopping, auto-zeroing periodically corrects offset, and therefore effectively reduces offset drift and 1/*f* noise as well. However, auto-zeroing introduces some dead time, during which the offset is sampled and the op-amp is unavailable for signal amplification. To achieve continuous-time amplification, at least two input channels are required. Moreover, sampling the offset causes high frequency noise folding, and thus results in an in-band noise PSD that is higher than the initial thermal noise floor. Chopping, on the other hand, is a frequency modulation technique which neither involves sampling nor introduces noise folding, so that the resulting in-band noise PSD is only slightly higher than the initial thermal noise floor. Therefore, chopping can achieve both low offset and low in-band noise PSD in a more power efficient manner than auto-zeroing.

AC and DC errors caused by the switching artifacts in chopper amplifiers are then reviewed, including up-modulated ripple, glitches caused by charge injection, residual offset, and input bias current. Additionally, design trade-offs related to these errors are explained. AC switching artifacts—ripple and glitches—can be pushed toward higher frequencies by increasing the chopping frequency. However, this increases the amount of charge injection mismatch generated per unit of time, thus increasing DC errors such as residual offset and input bias current. These DC errors also increase when wider input switches are used for lower on-resistance and hence, lower thermal noise. Due to these trade-offs, previous chopper op-amps (with chopping frequencies above 200kHz and noise PSDs less than 20nV/√Hz) could only achieve residual input offsets and input bias currents greater than 10μV and 500pA, respectively.

In Chapter 3, three known techniques to reduce the DC errors are reviewed. One technique employs a band-pass filter (BPF) to attenuate the glitches caused by charge injection mismatch, before they are down-modulated and turned into DC errors. However, this requires active circuitry to realize the BPF and thus is not power efficient. Another technique is to use a down-modulation clock with a dead-band, so that the amplifier's output is frozen until the glitches settle. However, the amplifier is unavailable during the dead-band, which decreases its effective

gain and increases its input referred noise PSD. Yet another technique, called nested chopping, employs a combination of fast and slow chopping. In this case, while amplifier offset and 1/*f* noise are up-modulated by the fast chopping, the resulting DC errors are up-modulated by the slow chopping. However, it results in a high noise PSD at the slow chopping frequency, which limits the usable signal bandwidth.

Additionally, known ripple reduction techniques are also reviewed. An active filter can be used to attenuate up-modulated ripple at the cost of extra current. Alternatively, a passive switched-capacitor notch filter (SC-NF) can be used, although the up-modulated ripple will still be present at its input. A relatively high chopping frequency is then required to ensure that this ripple does not saturate the output of the input transconductor. To avoid such ripple, the initial offset at the output of an input transconductor can be blocked by a correlated double sampling (CDS) or an RC high-pass filter. However, the gain of the input transconductor must be limited to ensure that its output is not saturated by the initial offset. With these filtering techniques, the up-modulated ripple and/or initial offset still remain, which restricts and/or complicates the design.

Therefore, the preferred approach is to cancel the initial offset that would otherwise turn into output ripple. One way of doing this is by trimming the initial offset, although this, and the associated ripple, will then drift with temperature. Instead, the initial offset can be auto-zeroed, and the resulting high in-band noise PSD can be up-modulated by chopping. However, to achieve continuous-time amplification, this requires an additional input channel that consumes extra current and die area. Another technique is to use a ripple reduction loop (RRL) that continuously detects the ripple and uses this information to cancel the initial offset. The notch created by the RRL can be buried by adding a high frequency path (HFP). Furthermore, instead of using a continuous-time filter in its feedback path, the RRL can also be realized digitally with a ripple-sensing comparator and a DAC in a more area efficient manner, although higher digital resolution is required to reduce the residual ripple.

In Chapter 4, a ripple reduction technique called auto-correction feedback (ACFB) is proposed, which also continuously detects the ripple and uses this information to cancel the initial offset. In contrast to the RRL, ACFB senses the ripple at the output of the output chopper,

and employs a switched-capacitor notch-filter (SC-NF) in its feedback path to selectively reduce the initial offset without affecting desired DC and low frequency signals. Since the SC-NF is not used in the main signal path, its clock frequency can be set relatively low, which will reduce the residual offset and input bias current. However, its ripple sensing point is also the input of the subsequent transconductor stage, which decreases the loop gain of the ACFB, and hence its ripple reduction capability. Like the RRL, the ACFB requires a high frequency path to bury the notch and to maintain the stability.

The proposed ACFB has been implemented in a stand-alone chopper op-amp that targets portable applications. This only draws 13μA from a 1.8V to 5.5V supply and occupies a 0.64mm^2 die area. Compared to a previous ripple reduction technique that used a SC-NF in the main signal path, ACFB requires sensing and nulling transconductors, although they only consume 5% of the op-amp's supply current. Furthermore, the use of ACFB allows the chopping frequency to be set to a relatively low 50kHz, thus only resulting in a 50pA maximum input bias current.

In Chapter 5, a chopper op-amp that achieves a 5.6nV/√Hz noise PSD is presented, as well as circuit techniques to relax the design trade-offs between noise PSD and other specifications. With the proposed frequency compensation technique, based on a current attenuator and a dummy differential output, the overall op-amp only draws 1.4mA from a 2.1V to 5.5V supply and occupies a die area of 1.26mm^2. In contrast to the design in the previous chapter, an active integrator is employed in the ACFB to boost its loop gain, thus suppressing its own residual offset, and hence the residual ripple. On the other hand, the active integrator also contributes to the sampled noise in the SC-NF, and hence to the up-modulated noise PSD at the chopping frequency.

In general, residual offset tends to increase when targeting lower noise PSD, due to increased charge injection mismatch from the wider input switches required for low thermal noise. Moreover, when the input chopping clocks have a fixed amplitude, extra wide switches are required to compensate for the lower overdrive voltages associated with mid-range input common-mode voltages. To overcome this problem, an adaptive clock boosting technique is proposed to drive NMOS input switches, so that charge injection mismatch is minimized and

independent of changes in the supply and input common-mode voltages. As a result, 0.5µV maximum offset and 0.015µV/°C maximum offset drift are achieved over the op-amp's entire rail-to-rail input common-mode range and a –40°C to 125°C temperature range.

In Chapter 6, a chopper op-amp is realized primarily for industrial applications, where wide supply and input common-mode voltage ranges are required as well as wide signal bandwidth. To achieve a 4.5V to 60V supply range, the op-amp is realized in a 0.18µm CMOS process augmented by 5V CMOS and 60V DMOS transistors. The capacitively-coupled input transconductor is pre-charged, auto-zeroed, and then chopped to achieve low offset, low output ripple, and wide input common-mode voltage range without creating a notch in the signal transfer function. The initial offset of the input transconductor is suppressed by a dual coarse-fine auto-zero technique without relying on extra gain stages in the auto-zero loop, thus avoiding excess sampled noise. To achieve continuous-time amplification, the whole input transconductor consists of six parallel channels, four of which amplify the input signal at a time. This reduces the input transconductance and switch width required in each channel. Consequently, to achieve the same in-band noise PSD, all six input transconductors only consume 1.5 more current than a non-auto-zeroed input transconductor. Moreover, due to the smaller switches, smaller glitches are produced per channel, thus pushing the PSD peak to 4.8MHz when each channel is driven by interleaved 800kHz clocks. Furthermore, an on-chip charge mismatch compensation circuit is employed to reduce the maximum input bias current from 1.5nA down to 150pA in post-production trimming.

In Chapter 7, the performances of the realized three chopper op-amps are compared with each other and with the other state-of-the-art. In later designs, the proposed techniques allow higher chopping frequencies to be used, while DC errors either improve or remain competitive. In the op-amps of Chapter 5 and 6, the input switches are driven by local clock supply voltages that track their input common-mode voltage, thus reducing their charge injection mismatch and hence residual offset. In the op-amp of Chapter 6, the charge injection mismatch is further reduced by an on-chip charge mismatch compensation circuit in post-production trimming. Consequently, the op-amps in Chapter 5 and 6 both achieve less residual offset and less input bias current than other comparable designs, i.e. with less than 20nV/√Hz noise PSDs and chopping frequencies greater than 200kHz. In the op-amp of Chapter 4, the maximum noise PSD

peak at the chopping frequency is 820nV/√Hz, which is dominated by the ACFB's residual offset due to its finite loop gain. In Chapter 5, an active integrator is employed in the ACFB to boost its loop gain. However, the sampled noise in the SC-NF is increased by the active integrator, which dominates the maximum noise PSD peak of 62nV/√Hz. In Chapter 6, the residual offset in the auto-zero loop is suppressed by the dual coarse-fine auto-zero technique without relying on additional gain stages, thus avoiding excess sampled noise and achieving the maximum noise PSD peak of 13.5nV/√Hz. Moreover, in the Chapter 6 design, the noise PSD peak due to glitches is pushed up to 4.8MHz by the clock interleaving technique.

Samenvatting

Dit proefschrift beschrijft de theorie, het ontwerp en de implementatie van chopper operationele versterkers (op-amps) in CMOS geïntegreerde schakelingen (ICs). De chopping techniek corrigeert periodiek DC fouten van zulke op-amps, zodat lage 1/*f* ruis en stabiele, microvolt-niveau offset bereikt kan worden. Chopping veroorzaakt echter schakelartefacten op de uitgang van de versterker, zoals omhoog-gemoduleerde rimpel en glitches, die meestal worden onderdrukt door laagdoorlaatfilters. Daardoor is het gebruik van chopper op-amps vooral beperkt tot laagfrequente toepassingen. In dit proefschrift worden geavanceerde circuittechnieken voorgesteld om deze schakelartefacten te onderdrukken, zonder daarbij de bruikbare signaalbandbreedte te verminderen. Hierdoor wordt het gebruik van chopper op-amps in een breder scala van toepassingen mogelijk. Drie chopper op-amps zijn ontworpen, gefabriceerd en gemeten, zodat de voorgestelde technieken geëvalueerd en vergeleken kunnen worden met andere state-of-the-art ontwerpen.

In Hoofdstuk 1 worden de voor- en nadelen van CMOS chopper op-amps in vergelijking met traditionele bipolaire op-amps besproken. Zonder enige offset wegwerk technieken, hebben CMOS op-amps last van hogere offset, temperatuur verschuivingen en thermische en 1/*f* ruis dan bipolaire op-amps, gegeven een vergelijkbare chip grootte en stroomverbruik. Aan de ander kant zijn bipolaire op-amps in veel toepassingen uitgesloten vanwege de hoge productiekosten, hoge ingangs-biasstroom en moeilijke integratie met CMOS ADCs en DACs. Daarnaast zijn digitale logica en analoge schakelaars makkelijk implementeerbaar in CMOS processen, wat het gebruik van dynamische offset compensatie technieken, zoals auto-zeroing en chopping, mogelijk maakt. Deze technieken kunnen de maximale offset en maximale offset drift van versterkers reduceren tot respectievelijk minder dan 10μV en 0.1μV/°C, welke moeilijk geëvenaard kunnen worden door bipolaire op-amps.

In dit hoofdstuk worden de traditionele toepassingen van chopper op-amps in sensor signaalconditionering en stroommetingen besproken. In dergelijke toepassingen zijn signaalfrequenties relatief laag en kunnen schakelartefacten dus verminderd worden door laagdoorlaat filtering. Signaalbronimpedanties zijn ook laag, waardoor wat ingangsstroom

getolereerd kan worden. Daarna worden nieuwe toepassingen van chopper op-amps besproken, zoals DAC buffers en industriële procescontrole, waarin signaalfrequenties te hoog zijn voor het gebruik van laagdoorlaatfilters om schakelartefacten te verminderen. In bepaalde toepassingen, zoals biomedische detectie, kunnen bronimpedanties vrij hoog zijn en moet de ingangs-bias-stroom dus lager zijn dan 100pA.

In Hoofdstuk 2 word naast de chopping techniek, de andere offset reductie technieken - offset trimmen en auto-zeroing - besproken. Trimmen corrigeert offset alleen tijdens de na-productietest en zal dus nog steeds resulteren in een hoge offset drift en 1/*f* ruis. Net als chopping corrigeert auto-zeroing de offset periodiek en zorgt daardoor ook voor een effectief lagere offset drift en 1/*f* ruis. Auto-zeroing introduceert echter wat dode tijd, gedurende welke de offset bemonsterd wordt en de op-amp niet beschikbaar is voor versterking. Om tijd-continue versterking te bereiken zijn tenminste twee ingangskanalen nodig. Daarnaast zorgt het bemonsteren van de offset voor het terugvouwen van hoogfrequente ruis en dit resulteert in een in-band ruis PSD die hoger is dan het initiële thermische ruis niveau. Aan de andere kant is chopping een frequentiemodulatie techniek waarbij geen sprake is van bemonstering of het terugvouwen van ruis. Hierdoor is de resulterende in-band ruis PSD slecht licht verhoogd ten opzichte van het initiële thermische ruis niveau. Daarom kan chopping zowel lage offset als lage in-band ruis PSD bereiken op een meer vermogens-efficiënte manier dan auto-zeroing.

AC en DC fouten veroorzaakt door de schakelartefacten in chopper versterkers worden vervolgens besproken, inclusief omhoog-gemoduleerd rimpel, glitches veroorzaakt door ladingsinjectie, overgebleven offset en ingangs-biasstroom. Daarnaast worden ontwerp-compromissen gerelateerd aan deze fouten besproken. AC schakelartefacten – rimpel en glitches – kunnen naar hogere frequenties gedrukt worden door een hogere chopfrequentie te gebruiken. Echter verhoogt dit ook de hoeveelheid mismatch van de ladingsinjectie gegenereerd per tijdseenheid, wat dus de DC fouten zoals overgebleven offset en ingangs-biasstroom verhoogd. Deze DC fouten worden ook groter als bredere ingangsschakelaars gebruikt worden voor lagere aan-weerstand en dus lagere thermische ruis. Door deze compromissen, konden eerder chopper op-amps (met chopfrequenties boven 200kHz en ruis PSDs lager dan 20nV/√Hz) alleen overgebleven ingangs-offset en ingangs-biasstroom bereiken respectievelijk groter dan 10µV en 500pA.

In Hoofdstuk 3 worden drie bekende technieken om DC fouten te verminderen besproken. Een techniek gebruikt een banddoorlaatfilter (BPF) om glitches veroorzaakt door de mismatch van ladingsinjectie te verminderen, voordat deze omlaag-gemoduleerd worden in DC fouten. Dit vereist echter actieve circuits om de BPF te realiseren en is dus niet vermogens-efficiënt. Een andere techniek is om een klok voor omlaag-modulatie te gebruiken met een dode-tijd, zodat de uitgang van de versterker wordt vastgezet totdat de glitches tot rust zijn gekomen. De versterker is echter niet beschikbaar gedurende de dode-tijd, wat de effectieve versterking verlaagt en de ingangsruis PSD verhoogt. Een andere techniek, genaamd nested chopping, gebruikt een combinatie van snel en langzaam choppen. In dit geval wordt de versterker zijn offset en 1/*f* ruis omhoog gemoduleerd door snel te choppen, terwijl de resulterend DC fouten omhoog gemoduleerd worden door langzaam te choppen. Dit resulteert echter in een hogere ruis PSD bij de lage chopfrequentie, wat de bruikbare bandbreedte beperkt.

Daarnaast worden bekende rimpel reductie technieken besproken. Een actief filter kan gebruikt worden om omhoog-gemoduleerde rimpel te onderdrukken, ten kosten van extra stroom. Als alternatief kan een passief geschakelde-capaciteit bandstopfilter (SC-NF) worden gebruikt, hoewel de omhoog-gemoduleerde rimpel nog steeds op de ingang aanwezig blijft. Een relatief hoge chopfrequentie is dan noodzakelijk om te zorgen dat deze rimpel de uitgang van de ingangstransconductor niet verzadigt. Om dit soort rimpel te voorkomen, kan de initiële offset op de uitgang van de ingangstransconductor geblokkeerd worden door gecorreleerde dubbele bemonstering (CDS) of een RC hoogdoorlaatfilter. De versterking van de ingangstransconductor moet echter gelimiteerd zijn, om te zorgen dat de uitgang niet verzadigt wordt door de initiële offset. Met deze filtertechnieken blijven omhoog-gemoduleerd rimpel en/of initiële offset nog over, wat het ontwerp beperkt en/of compliceert.

Daarom wordt de voorkeur gegeven aan een benadering waarbij de initiële offset wordt opgeheven, die anders tot uitgangs-rimpel zou leiden. Een manier om dit te doen is door de initiële offset te trimmen, al zal deze en de bijbehorende rimpel dan verschuiven met temperatuur. In plaats daarvan kan de initiële offset geauto-zeroed worden en kan de resulterende hoge in-band ruis PSD omhoog-gemoduleerd worden door te choppen. Echter, om tijd-continue versterking te verkrijgen, vereist dit een additioneel ingangskanaal die extra stroom en oppervlakte consumeert. Een andere techniek is om een rimpel reductie lus (RRL) te gebruiken

die continu de rimpel detecteert en deze informatie gebruikt om de initiële offset op te heffen. De bandstop gecreëerd door de RRL kan bedekt worden door een hoogfrequentpad (HFP) toe te voegen. Daarnaast kan in plaats van het gebruik van een tijd-continu filter in het terugkoppelpad, de RRL ook digitaal gerealiseerd worden met een rimpel-voel comparator en een DAC in een oppervlak effectievere manier, al is een hoge digitale resolutie dan noodzakelijk om de overgebleven rimpel te reduceren.

In Hoofdstuk 4 wordt een rimpel reductie techniek genaamd auto-correctie terugkoppeling (ACFB) voorgesteld, die ook continu de rimpel detecteert en deze informatie gebruikt om de initiële offset op te heffen. In tegenstelling tot de RRL detecteert ACFB de rimpel op de uitgang van de uitgangschopper en gebruikt het een geschakelde-capaciteit bandstopfilter in zijn terugkoppelpad om de initiële offset selectief te reduceren, zonder de gewilde DC en laagfrequente signalen te beïnvloeden. Aangezien de SC-NF niet wordt gebruikt in het hoofdsignaalpad, kan de klokfrequentie ervan relatief laag worden ingesteld, wat de overgebleven offset en de ingangs-biasstroom verlaagt. Het rimpel uitleespunt is echter ook de ingang van de volgende transconductietrap, wat de lusversterking van de ACFB verlaagt en daarmee zijn vermogen om de rimpel te reduceren. Net als de RRL heeft de ACFB een hoogfrequentpad nodig om de bandstop karakteristiek te verbergen en om stabiliteit te behouden.

De voorgestelde ACFB is geïmplementeerd in een opzichzelfstaande chopper op-amp voor gebruik in mobiele applicaties. Het gebruikt slechts 13µA van een 1.8V tot 5.5V voeding en neemt een oppervlak vaan 0.64mm^2 in beslag. In vergelijk met een eerdere rimpel reductie techniek die een SC-NF gebruikt in het hoofdsignaalpad, vraagt ACFB voel- en opheftransconductors, alhoewel deze slechts 5% van de op-amps voedingsstroom gebruiken. Verder staat het gebruik van ACFB toe dat de chopfrequentie op een relatief lage 50kHz word ingesteld, wat resulteert in een maximale ingangs-biasstroom van slechts 50pA.

In Hoofdstuk 5 wordt een chopper op-amp gepresenteerd die een 5.6nV/√Hz ruis PSD bereikt, als mede circuittechnieken om de ontwerpcompromissen tussen ruis PSD en ander specificaties te verzachten. Met de voorgestelde frequentie-compensatietechniek, gebaseerd op een stroomverzwakker en een dummy differentiëleuitgang, gebruikt de gehele op-amp slechts 1.4mA van een 2.1V tot 5.5V voeding en neemt slechts 1.26 mm^2 in. In tegenstelling tot het

ontwerp uit het vorige hoofdstuk wordt een actieve integrator gebruikt in de ACFB, om de lusversterking te verhogen, wat de eigen overgebleven offset onderdrukt en daarmee de overgebleven rimpel. Aan de andere kant draagt de actieve integrator ook bij aan de gesampelde ruis in de SC-NF en daardoor de omhoog-gemoduleerd ruis PSD op de chopfrequentie.

In het algemeen leidt een streven tot lagere ruis PSD tot hogere overgebleven offset, door de toegenomen ladingsinjectie van de bredere ingangsschakelaar die nodig zijn voor lage thermische ruis. Daarnaast, als de ingangs-chopklokken een vaste amplitude hebben, zijn er extra brede schakelaars nodig om te compenseren voor de lagere overstuurspanning, in relatie tot het midden van het ingangs-common-mode spanningsbereik. Om dit probleem te overkomen, wordt een adaptieve klok boost techniek voorgesteld om de NMOS ingangsschakelaars aan te sturen, zodat de mismatch van de ladingsinjectie geminimaliseerd wordt en onafhankelijk is van veranderingen in de voedings- en ingangs-common-mode spanning. Dit resulteert in een maximale offset en offset drift van respectievelijk 0.5µV en 0.015 µV/°C, over het gehele rail-to-rail ingangs-common-mode bereik van de op-amp en over een temperatuurbereik van –40°C tot 125°C.

In Hoofdstuk 6 is een chopper op-amp gerealiseerd primair voor industriële toepassingen, waar grote voedings- en ingangs-common-mode spanningsbereik vereist zijn alsmede een grote signaalbandbreedte. Om een 4.5V tot 60V voedingsbereik te verkrijgen, is deze op-amp gerealiseerd in een 0.18µm CMOS proces aangevuld met 5V CMOS en 60V DMOS transistoren. De capacitief-gekoppelde ingangstransconductor is voor-geladen, geauto-zeroed en vervolgens gechopped om lage offset, uitgangsrimpel en een groot ingangs-common-mode spanningsbereik te verkrijgen zonder een bandstop in de signaaloverdracht te krijgen. De initiële offset van de ingangstransconductor wordt onderdrukt door een dubbele grof-fijn auto-zero techniek zonder gebruikt te maken van extra versterkingstrappen in de auto-zero lus, wat overmatig bemonsterde ruis voorkomt. Om tijd-continue versterking te verkrijgen bestaat de ingangstransconductor uit zes parallelle kanalen, waarvan vier per keer het ingangssignaal versterken. Dit reduceert de benodigde ingangstransconductantie en breedte van de ingangsschakelaars per kanaal. Daardoor consumeren de zes ingangstransconductors slechts 1.5 keer meer stroom dan een niet geautozeroede ingangstransconductor, om dezelfde PSD van de in-band ruis te bereiken. Bovendien produceren de kleinere schakelaars kleinere glitches per kanaal, wat de PSD piek naar

4.8MHz duwt wanneer ieder kanaal wordt aangestuurd door een 800kHz interleaved klok. Daarnaast wordt een op-de-chip compensatie circuit gebruikt voor de mismatch van de ladingsinjectie. Dit reduceert de maximale ingangs-biasstroom van 1.5nA naar 150pA in een na-productie trim.

In Hoofdstuk 7 worden de prestaties van de drie gerealiseerde chopper op-amps vergeleken met elkaar en met de rest van de state-of-the-art. In de latere ontwerpen staat de voorgestelde techniek het gebruik van hogere chopfrequenties toe, terwijl DC fouten verbeterd worden of hetzelfde blijven. In de op-amps van Hoofdstuk 5 en 6 worden de ingangsschakelaars aangestuurd door een voedingsspanning die de ingangs-common-mode spanning volgt. Dit vermindert de mismatch van de ladingsinjectie en verlaagt daarmee ook de overgebleven offset. In de op-amp uit Hoofdstuk 6 wordt de mismatch van de ladingsinjectie verder gereduceerd door het gebruikt van een op-de-chip compensatiecircuit voor de mismatch van de ladingsinjectie in een na-productie trim. Daardoor behalen beide op-amps in Hoofdstuk 5 en 6 lagere overgebleven offset en lagere ingangs-biasstroom dan andere vergelijkbare ontwerpen, met minder dan 20nV/√Hz ruis PSDs en een chopfrequentie hoger dan 200kHz. In de op-amp uit Hoofdstuk 4 is de maximale ruis PSD piek 820nV/√Hz bij de chopfrequentie. Dit wordt gedomineerd door de overgebleven offset veroorzaakt door de beperkte lusversterking van de ACFB. In Hoofdstuk 5 wordt een actieve integrator gebruikt in de ACFB om de lusversterking te verhogen. De bemonsterde ruis in de SC-NF wordt echter verhoogd door de actieve integrator, wat de maximale ruis PSD piek van 62nV/√Hz domineert. In Hoofdstuk 6 wordt de overgebleven offset in de auto-zero lus onderdrukt door een dubbele grof-fijn auto-zero techniek, zonder gebruikt te maken van extra versterkingstrappen, wat overmatig gesampelde ruis voorkomt en een maximale ruis PSD piek van 13.5nV/√Hz oplevert. Daarnaast, in het ontwerp van Hoofdstuk 6, is de ruis PSD piek als gevolg van de glitches omhoog geduwd naar 4.8MHz door een klok interleave techniek.

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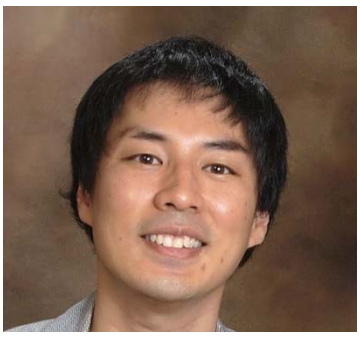
About the author



Yoshinori Kusuda received the B.S. degree in electrical and electronic engineering in 2002, and M.S. degree in Physical Electronics in 2004, both from Tokyo Institute of Technology. Upon his graduation in 2004, he joined the Japan Design Center of Analog Devices as an IC design engineer. Since then, he has been with the same company, and is currently based in San Jose, CA, U.S.A., working for the Linear and Precision Technology Group. He has been working for precision CMOS analog designs, including stand-alone amplifiers and application specific mixed-signal products. This has resulted in presentations and papers at IEEE conferences and journals, as well as nine issued U.S. patents. Since August 2015, he has been registered as a guest in the Electronic Instrumentation Laboratory of the TU Delft, pursuing his Ph.D. degree on the subject of reducing switching artifacts in chopper amplifiers.

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