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Electromagnetic-Thermal Performance Trade-offs in Phased Arrays With Shaped Elevation Patterns

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Abstract—Both thermal and electromagnetic performance of substrate-integrated waveguide (SIW) and microstrip line-fed shaped-beam arrays with slot and patch radiating elements are conducted. Three array types operating at 26 GHz band, namely SIW slot array, SIW array with patches, and proximity coupled patch array, are considered. The array performances regarding shaped radiation pattern stability with frequency and maximal temperature at the power amplifier chips are discussed. The study highlights intriguing trade-offs between radiation pattern performance and cooling ability in phased arrays.

I. INTRODUCTION

Next-generation base station phased arrays at millimeter-wave bands between 24-40 GHz promise increased data rate and connectivity [1]. However, they suffer from large beamforming complexity and extreme heat generation by the power amplifiers [2]. Therefore, the electromagnetic (i.e. bandwidth, radiation pattern) and thermal (i.e. maximal array temperature, temperature uniformity) requirements should be jointly considered in a modern antenna system design [3].

A phased array of series center-fed subarrays with fixed and cosecant-squared (csc^2) shaped elevation pattern decreases the complexity of beamforming at the base stations, while ensuring equalized powers at the line-of-sight users [4]. Such subarrays can be realized with different feeding techniques (e.g. microstrip line, substrate-integrated-waveguide (SIW)) and with different radiators (e.g. slot, slot and patch), which leads to different electromagnetic and thermal performances.

In complementary to the work in [5], this paper analyzes, for the first time, the electro-thermal trade-offs in different types of 26 GHz phased arrays with shaped elevation patterns with a focus on array temperature distributions and frequency-dependent radiation pattern performances.

Section II describes the antennas under investigation. Section III and IV discuss the electromagnetic and thermal performances, respectively. Section V concludes the paper.

II. ANTENNA MODEL

Three 12x12 planar arrays based on three types of 12x1 subarray designs are used: (1) SIW-fed slotted array, shown in Fig. 1(a), which is extended from the design in [5] and adjusted for center-feeding. (2) SIW-fed slot-patch array, shown in Fig. 1(b), which is adopted from [5] and adjusted for center-feeding. (3) Microstrip-line-fed proximity-coupled patch array, shown in Fig. 1(c), which is taken from [5].

The detailed design parameters of all three designs can be found in [6]. Losses are included in simulations. Waveguide ports are utilized to adjust feeding amplitudes and phases at the two half-sections (up and down) of the array.

III. ELECTROMAGNETIC PERFORMANCE OF ARRAYS

The full-wave simulations of the three planar arrays were performed in CST Microwave Studio using the time-domain solver. Fig. 2 compares the elevation patterns radiated from three planar arrays compared with the synthesized csc^2 pattern from a 12x1 subarray based on the array factor (excluding the element gain) [5].

Following the error formulations in [5], Fig. 3 shows the beam squint and csc^2 pattern-shape distortion (with normalized gain) comparison with frequency. Among the arrays under investigation, the proximity-coupled array shows the most steady pattern shape and beam pointing, which is followed by SIW-fed slot with patch, and the most basic SIW-fed slot. The realized gain (max. co-pol at scan direction and max. cross-pol. in visible space) vs azimuth scan angle (0-30-60 deg.) at 26 GHz is shown in Table I. It is seen that the proximity-coupled array performs the best among the three phased arrays both in co-pol and cross-pol levels.

IV. THERMAL PERFORMANCE OF ARRAYS

The thermal performances of the arrays are evaluated by considering the power amplifier (PA) chips as heat sources. In this study, a generic PA chip that feeds four subarrays is considered. The thermal performance of the arrays are obtained by exciting three PA chips simultaneously with unity power. ANSYS ICEPAK software is employed for steady-state computational-fluid-dynamics based thermal simulations. The side view of one chip to array surface and the two-resistor thermal model [3] used for the chip can be seen in Fig. 4. Following the assumption in [3], the junction-case (R_{jc}) and junction-board (R_{jb}) resistances are equal to 10 and 15 Kelvin/Watts (K/W).

The environment is chosen to be still air; therefore, results represent temperature values under natural convection. The

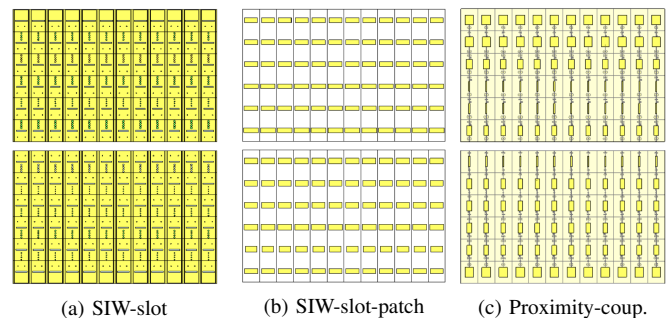


Fig. 1. Center-fed planar array models (probe feed is not realized).

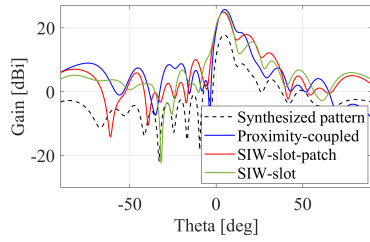


Fig. 2. Comparison of elevation pattern shapes at 26 GHz.

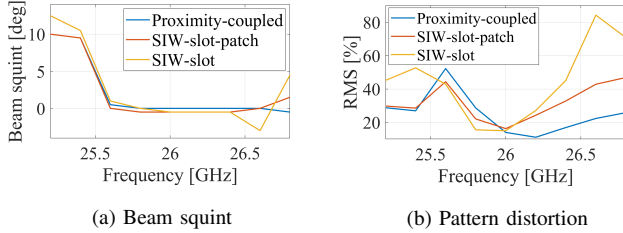


Fig. 3. Comparison of beam squint and csc2-pattern distortion with frequency.

TABLE I
REALIZED GAIN VS AZIMUTH SCAN ANGLE AT 26 GHz

	Proximity-coupled	SIW-slot-patch	SIW-slot
Scan angle 0 deg			
Max. co-pol (dBi)	25.66	24.79	24.98
Max. x-pol (dBi)	-5.75	-3.88	-4.77
Scan angle 30 deg			
Max. co-pol (dBi)	25.16	24.85	24.64
Max. x-pol (dBi)	-4.68	-0.96	-1.66
Scan angle 60 deg			
Max. co-pol (dBi)	22.88	22.22	21.87
Max. x-pol (dBi)	-1.94	4.09	3.05

array surface temperature plots belonging to three different arrays can be seen in Fig. 5. The results demonstrate that arrays having SIW type of feeding structure perform better compared to arrays having microstrip type of feeding regardless of the radiator type (slot or patch). The SIW slot array thermally performs the best due to its large metallic surface creating a boundary between the environment and hot metal. This boundary greatly increases the natural convection; therefore, yields lower temperatures by 10^0C .

Furthermore, the maximal junction temperatures are compared in Table II, where the SIW-fed slot array performance with different ground thickness values (than the standard 0.035 mm thickness) is also included. As the SIW structure acts as a large metallic heatsink, increasing its thickness will increase the heat transferred from the junction, resulting in lower junction temperatures. By arranging the ground thickness, the junction temperature can be reduced below 125^0C without

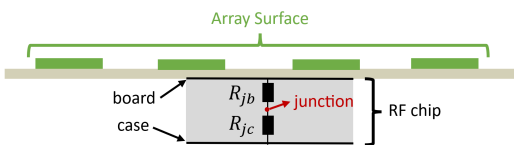


Fig. 4. Side view of the generic ICEPAK simulation environment and the thermal model of the PA chip.

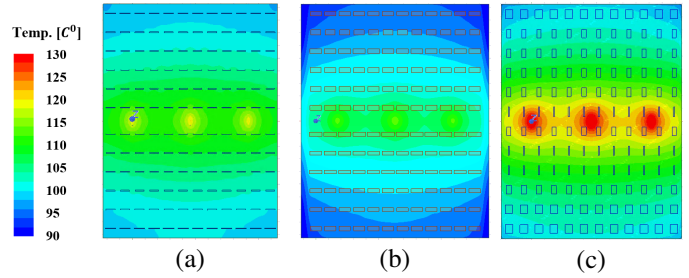


Fig. 5. Surface temperature of (a) SIW-fed slot array, (b) SIW-fed slot-patch, (c) proximity-coupled patch array (rotated by 90 deg. with respect to Fig. 1).

TABLE II
JUNCTION TEMPERATURES OF DIFFERENT ARRAYS WITH NATURAL CONVECTION (PASSIVE COOLING)

	Ground Thickness [mm]	Junction Temp. [0C]
Proximity Coupled	0.035	150.2
SIW-slot-patch	0.035	143.53
SIW-slot	0.035	139.01
	0.05	134.2
	0.1	127.7
	0.15	124.3

affecting the radiation characteristics.

V. CONCLUSIONS

For the first time, both electromagnetic and thermal performances of SIW- and microstrip-fed arrays with slot and patch radiating elements have been analyzed. Three shaped-beam arrays are used for demonstration: SIW-fed slot array, SIW-fed slot-patch array, and proximity-coupled patch array. Through multiphysics simulations, it is shown that the SIW-based slot array fully outperforms two other arrays in terms of thermal performance yielding maximum junction temperature to be about 10^0C lower than in other arrays. At the same time, the proximity-coupled patch array shows the most stable performance over a large frequency band. From this comparison, one can conclude that SIW technology is preferable for relatively narrow-band arrays if thermal performance matters.

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