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# A Programmable-Gain Floating Inverter Low-Noise Amplifier for Ultrasound Imaging Analog Frontends

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***Abstract*—Wearable ultrasound devices for imaging and therapeutic applications demand low-power and low-area integrated circuits to interface with ultrasound transducers. In the case of ultrasound imaging front-ends, discrete time-gain compensation (TGC) simplifies gain control in ultrasound imaging (USI) ASICs, but higher gain-step resolution increases area and power dissipation, while high PSRR is needed to suppress switching noise from co-integrated HV digital circuits. This work presents a programmable-gain floating inverter low-noise amplifier (FIALNA) architecture in 28nm CMOS for low-power, wide-bandwidth USI. A thermometer-encoded variable reservoir capacitance enables fine TGC with five PVT-robust gain steps, achieving 53.6dB PSRR and an area of 0.0023mm², an order of magnitude smaller than current PGA designs. The FIALNA dissipates 116µW and achieves 59µVrms input-referred noise, making it suitable for low-power wearable ultrasound devices.**

***Index Terms*—Discrete TGC, PGA, LNA, Floating Inverter Amplifier, Ultrasound Imaging, PMUT Matrix**

## I. Introduction

Vagus nerve stimulation (VNS) is a clinically approved therapy for epilepsy and treatment-resistant depression. Of the several methods to perform VNS, image-guided ultrasound neuromodulation (IGUN) offers the optimal compromise between non-invasiveness and precision [1, 2]. However, IGUN still relies on bulky equipment with form-factors [2] incompatible with wearable technologies, which hamper existing treatments. Recent advances in 2D US transducer arrays with integrated stimulation [3, 4] and imaging ASICs [5] allow for the miniaturization of IGUN systems and reduce reliance on expensive imaging techniques like MRI and CT, though integration and portability challenges remain for truly wearable US systems [1]. In VNS applications, one of such challenges is obtaining accurate ultrasound images of the vagus nerve such that its coordinates can be transferred to the neuromodulation sub-system. This, in turn, demands compact and power-efficient ultrasound receiver integrated circuit front-ends [2].

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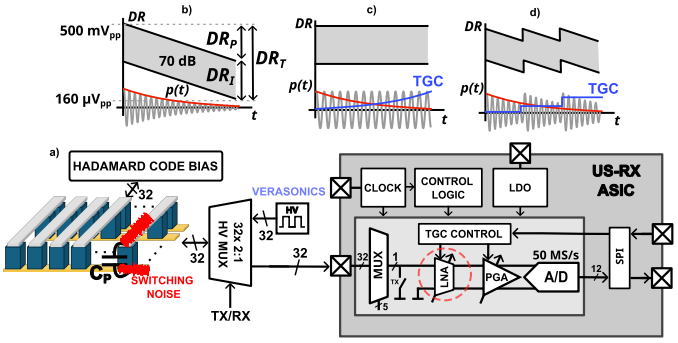


Fig. 1. a) USI system overview. b) Vagus nerve imaging application dynamic range breakdown, c) Continuous TGC readout US signal, d) Discrete TGC readout US signal.

Considering an average attenuation coefficient $\alpha_T$ for soft tissue of approximately 0.55 dB · (MHz cm)$^{-1}$ [6], imaging the vagus nerve (VN) imposes a propagation dynamic range ($DR_P$) up to 30dB at a typical center frequency $f_0$ of 4MHz, given the average human neck radius ($D = 7.6$cm) [7, 8], which in turn require higher resolution analog-to-digital converters and higher power consumption and area. Considering an instantaneous DR ($DR_I$) of 40dB for US signals, the total input DR can achieve 70dB (Fig. 1c) [5, 9]. Linear-in-dB time-gain compensation (TGC) enables the compression of the US signal's DR (Fig. 1b), and hence a relaxed DR of the analog frontend (AFE) [9]. Continuous TGC implementations (Fig. 1c) improve image quality but often rely on static current-mode variable-gain amplifiers (VGAs), which are prone to PVT variations without feedback and add complexity to gain control [10]. Programmable-gain amplifiers (PGAs) using discrete-gain steps (Fig. 1d) implemented through variable capacitance feedback networks greatly simplify gain control, while leading to significant power-dissipation overhead in wide-bandwidth USI ASICs [5, 9, 11]. Moreover, discrepancies between gain steps and US signal attenuation rates can cause imaging artifacts [10, 11]. Increased discrete TGC resolution greatly increases area in PGAs[10]. In-band supply noise from co-integrated circuits can degrade LNA performance, and although inverter OTAs reduce power dissipation, their poor PSRR requires regulated supply nodes, further increasing area and power dissipation[5, 9].

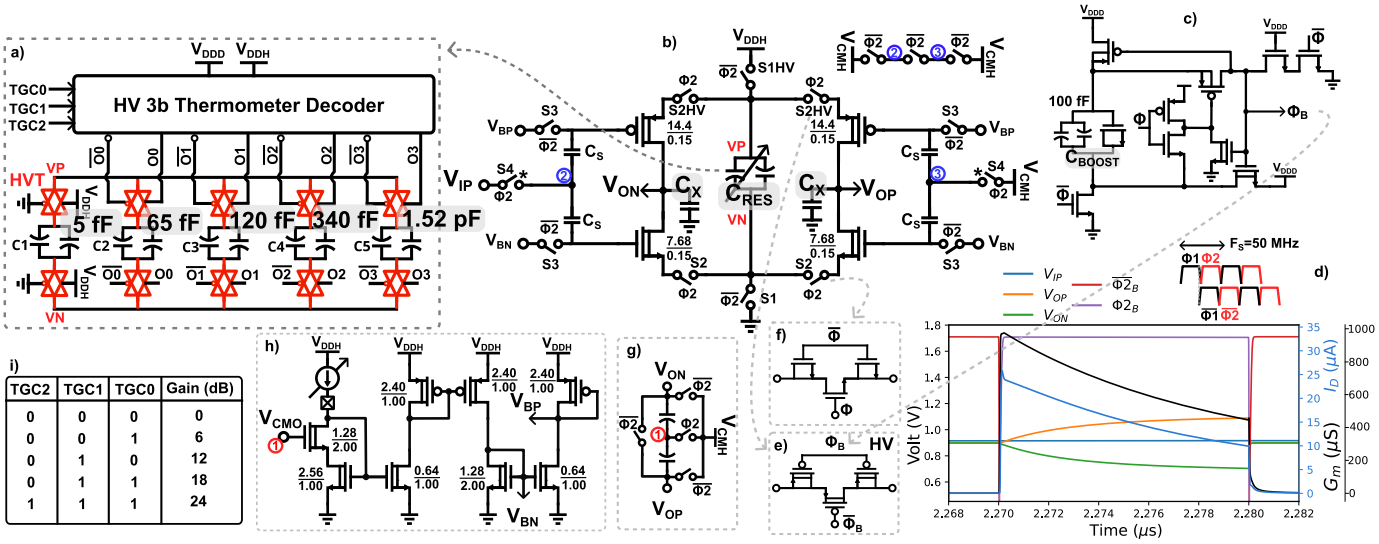


Fig. 2. a) Thermometer-encoding scheme for $C_{RES}$ control, b) FIALNA topology, c) dynamic clock-boosting circuit, d) simulated transient waveforms, e) high-VT S2/S1 P-switches, f) standard-VT S2/S1 N-switches, g) output CM detector, h) output CM-controlled gate-biasing circuit, i) 3-bit discrete TGC function.

This work presents an open-loop LNA architecture using a programmable-gain floating inverter amplifier (FIALNA) in standard-bulk 28nm CMOS technology for low-power, wide-bandwidth USI. A variable-capacitance reservoir capacitor ($C_{RES}$) enables discrete TGC via programmable capacitive source degeneration[11–13]. Fully-differential operation enhances PSRR, while thermometer encoding for $C_{RES}$ ensures fine linear-in-dB gain steps without significant area overhead.

## II. US Imaging System

The USI RX ASIC (Fig. 1a) integrates a 2D PMN-PT matrix using a row-column indexing scheme. Due to the 28nm standard bulk technology lacking high-voltage devices, integration with the 2D matrix is done at the PCB level. Each column is multiplexed into a single US RX channel in the ASIC. A coherent planar wave compounding (CPWC) imaging scheme performs RX beamforming in the digital backend [14], while a Fresnel lens modulates the RX sensitivity transfer function in the elevational (row) direction, performing row-level beamforming [15], with HV pulses and plane-wave angle-dependant 32b Hadamard code top-plate biasing (for Fresnel lens control) generated off-chip using a Verasonics machine.

## III. Proposed Programmable Gain LNA

The proposed LNA is based on a floating-inverter amplifier (FIA) (Fig. 2b) with thermometer-decoded programmable-capacitance $C_{RES}$ (Fig. 2a) for linear-in-dB gain steps of 6dB (Fig. 2i). An analog voltage supply ($V_{DDH}$) of 1.8V is used to facilitate the FIA's linearity when targetting the large input/output DR. HV device logic (Fig. 2a,e,f) enabled by a dynamic clock-boosting circuit (Fig. 2c) was used to allow proper switch-on/off near the HV supply and ensure circuit reliability. Dedicated gate-biasing (Fig. 2h) is required to maintain the devices in weak inversion during the amplification phase (Φ2) due to the increased voltage headroom, reducing gain error [16]. The common-mode rejection ratio (CMRR), defined as $\mathrm{CMRR}(T_S) = -2C_P/C_{RES}$ [17], is enhanced through parasitic capacitance equalization using anti-parallel MoM capacitors, with a complementary feedback circuit mitigating differential CM offset increase as $C_{RES}$ decreases (Fig. 2g), thereby preserving the amplifier's linearity.

### A. Gain of the FIALNA

It has been shown that $I_D(t) = I_{D,0^+}/\left(1+(t-T_S/2)/\tau_{w,i}\right)$ accurately represents the FIA's dynamic biasing current during Φ2 (Fig. 2d) [17, 18]. The parameter $\tau_{w,i} = 2\cdot C_{RES}/G_m(0^+)$, where $G_m(0^+)$ is the initial channel transconductance, us used to represent the time required for the inverter's devices to reach weak inversion, with its value dependent on the size of the reservoir capacitor and biasing current [17]. Due to the approximate relationship $G_m \propto I_D$, the average $G_m/I_D$ value of the inverter's devices throughout the Φ2 is used to approximate the inversion level during amplification as a constant value $(G_m/I_D)_{avg} = \frac{1}{T_S}\int_0^{T_S}\frac{G_m}{I_D}(\tau)\,d\tau$, simplifying the remaining steps of the analysis (1). Despising the finite output resistance of the FIA and noting that $\Delta V_{OD}(t) \approx \frac{\Delta V_{ID}}{C_X}(G_m/I_D)_{avg}\int_0^t I_D(\tau)\,d\tau$, we finally arrive at the gain expression for the FIA (2).

$$\int_0^t G_m(\tau)d\tau \approx \frac{G_m}{I_D}_{avg}\left(I_D(t)T_S - I_{D,0^+}T_S\right) \approx \quad (1)$$
$$\approx \frac{G_m}{I_D}_{avg}\int_0^{T_S} I_D(\tau)d\tau$$

$$A_v(T_S) \approx -\frac{2C_{RES1}}{C_X}\frac{(G_m/I_D)_{avg}}{(G_m/I_D)_{0^+}}\cdot\ln\left(1+\frac{T_S}{2\tau_{w,i}}\right) \quad (2)$$

### B. Noise Analyis

The FIA's total output-referred noise comprises sampled thermal noise, $v^2_{tn,o} = kT/C_X$ $[V^2]$, and sampled shot noise, $i^2_{sn,o} = 2qI_D(t)$ $[A^2H_z^{-1}]$. The $kT/C$ noise is reduced by a sufficiently large output capacitor ($C_X = 100$ fF), while shot noise dominates as devices enter weak inversion, scaling with the dynamic bias current, aggravated to $i^2_{sn,o} = 4qI_{D,sat}(t)$ $[A^2H_z^{-1}]$ upon $V_{DS} < 5kT/q$ [17, 19–21]. The input-referred noise is derived as in [16, 17], resulting in (3). As shown in (3), increasing $C_{RES}$ reduces input-referred noise but raises power dissipation and area. Larger $C_{RES}$ also increases $\tau_{w,i}$, which lowers $(G_m/I_D)_{avg}$ during $\Phi 2$, counteracting noise reduction—an effect not well captured in previous analyses [16, 17]. Optimal noise suppression is achieved by biasing the inverter's devices into weak inversion since the start of $\Phi 2$.

$$\sigma^2_{i,d}(T_S) = \frac{\sigma^2_o(T_S)}{(A_V(T_S))^2} \approx \frac{4q\ (G_m/I_D)_{0^+}}{C_{RES}\cdot \ln\left(1+\frac{T_S}{2\,\tau_{w,i}}\right)(G_m/I_D)^2_{avg}}\ \frac{V^2}{Hz} \tag{3}$$

### C. Power-Supply Rejection Ratio of the FIALNA

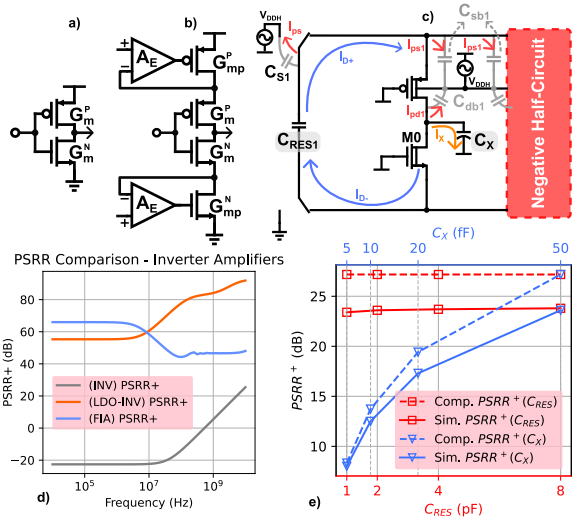


Fig. 3. a) Single-ended inverter amplifier, b) LDO-regulated single-ended inverter amplifier, c) FIA positive half-circuit used for PSRR analysis, d) single-ended inverter amplififfers PSRR comparison simulation, e) Comparison between simulated and computed single-ended FIA PSRR.

A comparison of the single-ended PSRR for a standard inverter, LDO-regulated inverter, and FIA (Fig. 3a,b,c, respectively) was performed using a dedicated simulaion testbench. Simulation parameters used were $C_{RES} = 2$pF, $C_X = 50$fF, error amplifier gain of $A_E = 80$dB, transistor finger widths $F_{W,n}/F_{W,p} = 220/440$nm, channel length $L_{ch} = 120$nm, number of fingers $NF = 4$, input frequency $F_{in} = 100$kHz, and clock frequency $F_S = 100$MHz. The error amplifier and switches were implemented using non-ideal linear models. A 20mV sinusoidal signal was applied to the positive rail, and output voltage was measured to assess PSRR. The unregulated inverter acts as a common-gate (CG) amplifier with PSRR inversely proportional to the gain ($\text{PSRR}^+_{\text{INV}} = |G_{ds}/(G_m + G_{ds})|$), while an LDO-regulated inverter shows improved PSRR directly proportional to the LDO open-loop gain ($\text{PSRR}^+_{\text{LDO-INV}} \approx |G_{ds}(1 + A_{E0})/(G_{m,p} + G_{ds,p})|$). For the FIA, a time-domain approach was used to obtain (4), where supply ripple affects output through sampled ripple ($\Delta V_{ripple}(T_S/2) = \Delta V_{DD}(1-e\{-T_S/(2\,C_{RES}\,2R_{ON,S1})\})$) during reset phase ($\overline{\Phi 2}$) and parasitic coupling during $\Phi 2$. The sampled ripple from the $\overline{\Phi 2}$ features strong non-linear attenuation at high $F_S$ and due to source-nodes discharging during $\Phi 2$, being despised in the analysis. From the KCL applied to the FIA's current-reuse loop (Fig. 3c), and computing the total charge redistributed during $\Phi 2$, we arrive at the single-ended PSRR of the FIA in (4), where the voltage transfer function is modeled as a CG amplifier, expressed as $\Delta V_S(T_S) = \Delta V_X(T_S)/\text{A}_{\text{V,CG}}(\text{T}_\text{S})$, with $\text{A}_{\text{V,CG}}(\text{t}) \approx -A_V(t)$. Small device widths and ideal reset switches enable the PSRR of the FIA to acheive a similar performance to the LDO-regulated inverter (Fig. 3d), with the FIA's PSRR degrading as the supply ripple's frequency achieves similar orders of magnitude to $F_S$. Computed FIA PSRR features good agreement with simulated values (Fig. 3e). The 3dB error of (4) is associated with 1)the despise of the finite output impedance, 2) ideal resistive switches usage,3) CG amplifier $\text{A}_{\text{V,CG}}(\text{T}_\text{S})$ approximation, and 4) parasitic capacitance coupling due to S2 HVT switches (possible to be accounted for in $C_{S1}$), further degradading (4). Finally, supply ripple sampled during $\overline{\Phi 2}$ affects both FIA differential branches with the same magnitude and phase, enabling the achievement of differential PSRR values in the range of 50dB for this inverter-based topology, being mainly dependant on device mismatch ($C_{db,sb} \pm \Delta C$, and $A_{V,CG} \pm \Delta A_{V,CG}$).

$$\text{PSRR}^+_{\text{FIA}}(\text{T}_\text{S}) \approx \left|\frac{C_X + C_{db,1} + \frac{C_{S1}/2+2C_{sb,1}}{A_{V,CG}(T_S)}}{C_{db,1} + C_{S1}/2 + 2C_{sb,1}}\right| \tag{4}$$

### D. Design and Trade-offs

DC decoupling anti-parallel MoM capacitors ($C_S = 500$fF, total 1pF) are employed to independently establish the common-mode of the PMUT array sensors while allowing the multiplexed RX channel to be grounded during the US TX phase [17]. $C_{RES}$ is set to approximately 2pF, enabling a maximum gain setting of 21dB, while device widths are optimized for minimum bandwidth ($\omega_{p1}(t) = 1/(R_{out}(t)C_X) = G_m(t)/(A_V(t)C_X)$), designed at half the sampling rate ($F_S/2$) to facilitate wide-band USI. A dedicated gate-biasing circuit stabilizes the FIA's devices ($|V_{GS}| - |V_T|$) at approximately 50mV, thereby minimizing sensitivity to PVT variations and input-referred noise due to the increased logarithmic gain compression [16].

## IV. Simulation Results

Schematic simulations were obtained with 2048 points transient at conservative settings (Fig. 4). A differential

PSRR of 53.6dB is achieved, efficiently decoupling supply noise from the output differential signal (Tab. I). Noise simulations show an input-referred noise density (IRND) of 18.4nV/$\sqrt{\text{Hz}}$ at a center frequency of $f_0 = 4$MHz (Fig. 4a), leading to 59µVrms single-ended (118µVrms differential) input-referred noise ($v_{n,rms}$), allowing the detection of a 70dB DR, 80µV single-ended US signal. The differential LNA topology doubles the input-referred noise, aggravated by the lack of negative feedback and a reduced $C_{RES}$ for area optimization, explaining the increased noise floor. Enhancing the open-loop gain of the base FIA design [16] and employing noise-cancelling techniques using the DC-decoupled AFE's cascaded gain stages [22] leads to a reduction the impact of input-referred noise in the AFE at the cost of a reduced output-swing. Increasing TX pulse voltage amplitude to raise TX power, thereby offsetting the total 70dB DR to higher voltage levels (Fig. 1b), can also mitigate the impact of noise. The use of HVT transmission gates slightly increases gain at low settings due to the increased parasitic capacitance at VP and VN nodes, but ultimately reduces overall gain across all settings due to the additional resistive source degeneration (Fig. 2a). Increased output capacitance due to the CM detector circuit (Fig. 2g), further reduces each gain-step, resulting in a discrete TGC function with five PVT-robust gain steps averaging 4.7dB (Fig. 4b,c,d). The -3dB bandwidth $f_{-3\text{dB}}$, inversely proportional to $C_{RES}$ (Fig. 4b), is established at $F_S/2$ in the maximum gain setting ($f_{-3dB} = 26.5$MHz for $F_S = 50$MHz - 2× higher than the reported SOTA (Tab. I). Cascaded low-pass filtering stages can enforce $f_{-3\text{dB}}$ at $F_S/2$ for lower gain settings of the FIALNA. At a maximum gain of 21.1dB, the measured total harmonic distortion (THD) at the 1dB gain-compression point was -46.4dB for a 35mV single-ended input amplitude, a value within state-of-the-art (SOTA) results (Fig. 4c). The extreme FF process corner at 85°C and a +10% supply voltage variation ($V_{DDH} = 1.98$V) collapses FIALNA gain due to significantly decreased $G_m/I_D$ during Φ2 (Fig. 4d), compensated through the external current source (Fig. 2h). A $|\Delta A_V| < 3$dB across all gain settings (Fig. 4d,e) is achievable in the remaining PVT corners.

## V. Conclusions

An open-loop FIALNA in 28nm standard-bulk CMOS for a wide-bandwidth USI ASIC employing a programmable reservoir capacitor was proposed, achieving 53.6dB differential PSRR while eliminating LDO-regulator area and power-dissipation overhead. The variable capacitive source degeneration was implemented using a thermometer encoding scheme for the control of $C_{RES}$, leading to an estimated area of 0.0023mm$^2$, representing an improvement by an order of magnitude comparing to the reported PGA SOTA for USI applications (Tab. I). A total dissipated power of 116µW at a 1.8V supply was achieved, leading to a nominal noise efficiency factor (NEF) of 4.7 (5) - considering the 26.8µArms current biasing the FIALNA devices in the maximum gain setting. The presented FIALNA enables area and energy-efficient readout of 70dB DR input single-ended signals, converting them to differential (maximizing the SNDR of the AFE) while allowing for a enhanced-resolution, linear-in-dB, discrete TGC function - easing the DR specification of the subsequent interface circuits and minimizing the impact on 2D and 3D USI quality.

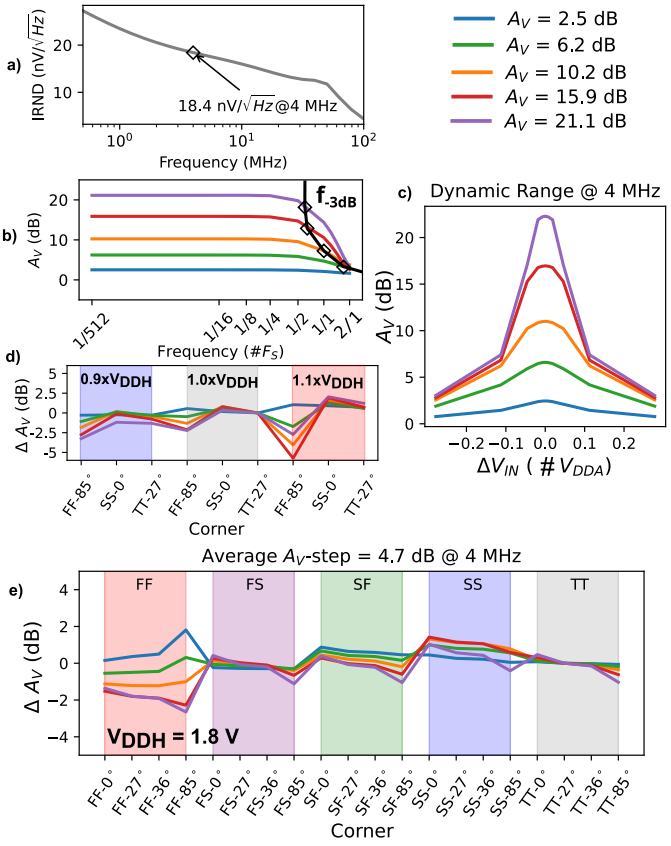


Fig. 4. a) Simulated input-referred noise-density (IRND), b) gain transfer function at -3dB BW, c) input DR and gain compression, d) gain variation $\Delta A_V$ vs. supply voltage variations, e) $\Delta A_V$ vs. process-and-temperature corners (at nominal supply: 1.8V).

TABLE I
State-of-the-art comparison

| Work | [23] | [9] | [24](SCMF) | **This Work*** |
|---|---|---|---|---|
| Tech. (nm) | 350 | 180 | 180 | **28** |
| TGC | Discrete | Discrete | Discrete | **Discrete** |
| Closed-Loop | Yes | Yes | Yes | **No** |
| Differential | Yes | No | Yes | **Yes** |
| Supply (V) | 3.3 | 1.8 | 1.8 | **1.8** |
| Dynamic | No | No | No | **Yes** |
| $A_V$ (dB) | 31.0/16.0 | 22.5/4.7/-13.2 | 26.6 | **21.1/15.9/ 10.2/6.2/2.5** |
| $f_{-3\ dB}$@$A_{V,max}$(MHz) | 6.6 | 9.8 | 7.0 | **26.5** |
| $f_0$(MHz) | 2.5 | 4.0 | 3.0 | **4** |
| THD$_{1\ dB\ \text{Comp.}}$ (dB) @$A_{V,max}$ | -40@34.5mVin | -40@273mVin (@$A_{V,min}$) | -51.5@35mVin | **-46.4@35mVin** |
| PSRR@$f_0$ (dB) | NA | 45.8 | NA | **53.6** |
| IRND@$f_0$ (nV/$\sqrt{\text{Hz}}$) | 5.42 | 5.9 | 5.3 | **18.4** |
| $P_D$ (mW) | 0.900 | 0.135 | 0.270 | **0.116** |
| NEF | 6.8 | 3.0 | 4.3 | **4.7** |
| Area/ US RX Channel(mm$^2$) | 0.0340 | 0.0100 | NA | **0.0023**** |

*Simulation Results, **Estimated from schematic

$$NEF = v_{n,rms}\sqrt{\frac{2I_{TOTAL}}{4\pi kTU_T BW}} \quad (5)$$

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