A 15-bit ΔΣ Capacitance-to-Digital Converter For Position Sensing with Electrically Floating Targets

Samira Amani

June, 2017

Supervisor:

Dr. Stoyan N. Nihtianov

Submitted to the Office of Graduate Studies of

The Delft University of Technology

In partial fulfilment of the requirements for the degree of

MASTER OF SCIENCE

Committee Members:

Dr. Stoyan N. Nihtianov

Dr. ir. Michiel A.P. Pertijs

Prof. dr. ir. Wouter A. Serdijn

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Abstract

This thesis presents a capacitive sensing technique which is suitable for measuring small displacements with one floating target electrode. A capacitive sensor interface, which does not require electrical contact with the target, while demonstrating performance comparable with the state-of-the-art, is proposed. The designed prototype is intended for displacement measurement with a measurement range from 10 μm to 100 μm, and a resolution better than 3 nm.

The proposed design implants the sensor capacitor into the input branch of a capacitance-to-digital converter (CDC), which results in a simpler system that saves power and reduces the error sources.

The CDC is taped out in the TSMC 0.18 μm CMOS process with V_{dd} = 1.8 V. The total chip area is 2.3 mm^2 of which 0.5 mm^2 is occupied by the CDC. In frequency range from DC to 2 kHz, the resolution of the CDC is thermal noise limited, whereas the quantization noise is shaped to higher frequency. After applying a low-pass digital filter with a bandwidth of 1 kHz, the dynamic range is better than 15 bits, corresponding to 3 nm displacement resolution.

Chapter 1 Capacitive Sensor with Floating Target

1.1 Introduction

Capacitive position measurement with sub-nanometer resolution is a preferred solution in many advanced industrial applications due to its compactness, excellent performance, and power efficiency. However, the sensor capacitance is typically measured by connecting it in a closed-loop configuration as shown in Figure 1.1(a). This requires an electrical contact between the target and the electronic interface (in some cases via ground) which compromises the contactless measurement advantage [1]. Even worse, acting as an "antenna", the relatively large closed loop, incorporating the target, becomes susceptible to magnetic field interferences and is also a source of parasitic cable capacitance, which both degrade the sensor resolution. The reported solution is based on a fully contactless interface configuration, employing the so-called "push-pull" principle [2, 3]. With this approach, the magnetic-field-susceptibility and the parasitic capacitance are minimized and a true contactless position sensing is realized.

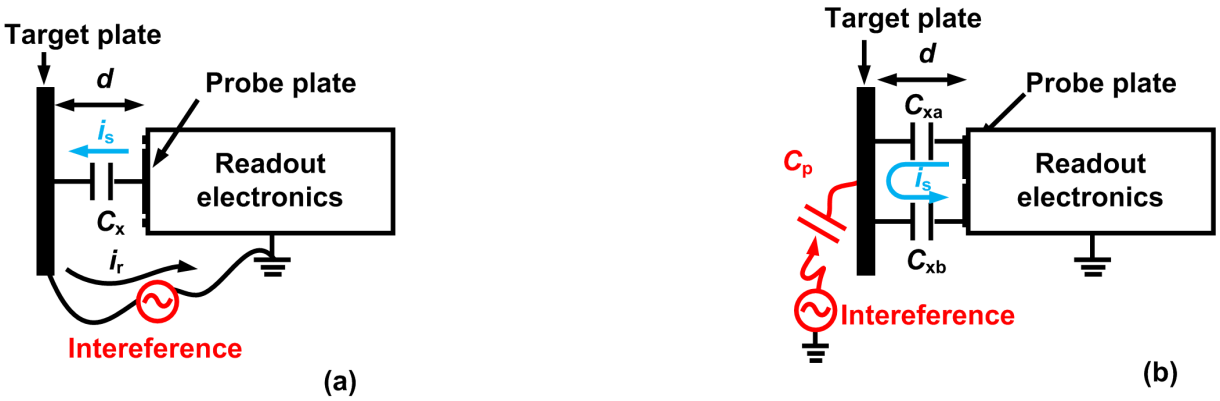

Figure 1.1 (a) Conventional capacitive position sensing system, in which the closed loop incorporates the target electrode and the input of the interface electronics; (b) Push-pull capacitive position sensing system with floating target electrode and significantly reduced closed loop incorporating only the sensing electrodes.

Figure 1.1(b) shows the basic principle of sensing the position of a floating target. The capacitive sensor has two identical sensing electrodes, positioned in the proximity to the target electrode, hence forming two capacitors in series with nominally equal values C_{xa}=C_{xb}=C_x, which vary with the distance to the target d. These two capacitors are charged with two anti-phase voltages and the stored charge Q_{Cs} is measured by integrating the current i_s. The price to pay for reducing the sensor loop area is the parasitic capacitance C_p between the floating target and the surrounding environment, which is a path for electric field interferences.

1.2 Proposed sensing principle with suppression of the interference

Figure 1.2 shows the equivalent circuit of the capacitive sensor with a floating target. By using the two-channel out-of-phase technique, the two capacitors C_{xa} and C_{xb} are connected to the electronic interface circuit at points A and B, while the target is point C. If C_{xa} = C_{xb} are equal, the noise source (electric field interferences introduced) at node C will be equally split between inputs A and B and will be treated as a common mode signal in a fully symmetrical differential front-end circuit.

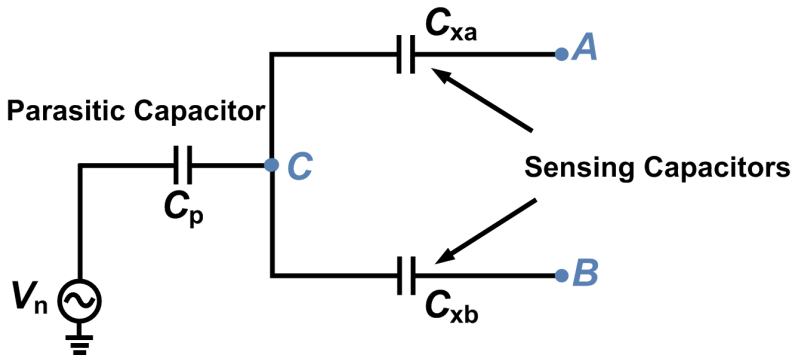

Figure 1.2 Proposed sensor structure [8].

Figure 1.3 shows a simple circuit used to measure the change of a capacitance with one grounded electrode. The same principle is used in the proposed capacitive sensor interface solution in this thesis, but in differential configuration and with floating target. In Figure 1.3, the sensing capacitor C_x is first charged by means of a reference voltage V_{ref} and then is connected to an amplifier. Assuming an ideal amplifier (virtual ground is zero), the amount of transferred charge in one operational cycle is:

$$Q = C_X . V_{ref} \qquad 1.1$$

which leads to an output voltage of

$$V_O = -(C_X / C_f) . V_{ref} \qquad 1.2$$

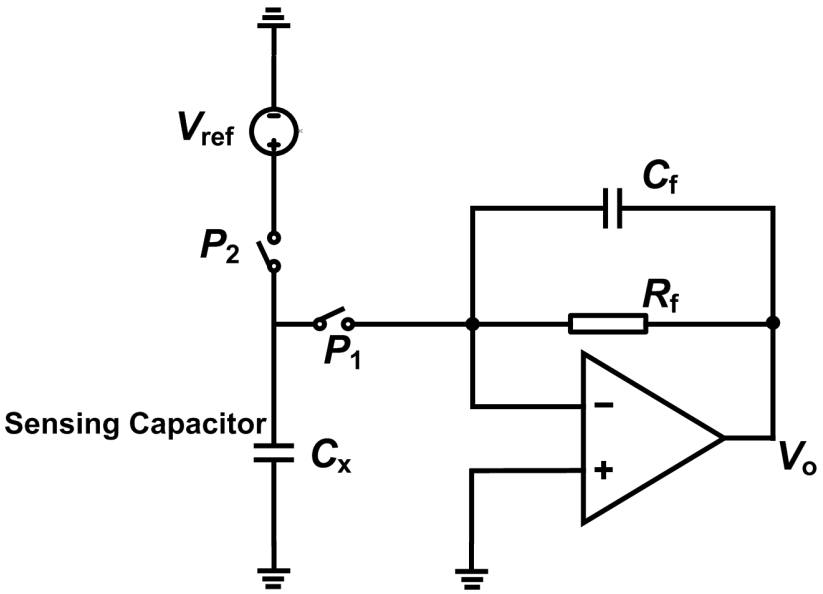

Figure 1.3 A simple capacitive sensor interface.

1.3 Prior Work

The simplified circuit diagram and the timing scheme of the prior work [7] are illustrated in Figure 1.4. In this structure, the sensing capacitors C_{xa} and C_{xb} are first charged by the reference voltage V_{dd}, then this amount of charge will be transferred to voltage via the feedback capacitors across the differential amplifier [7].

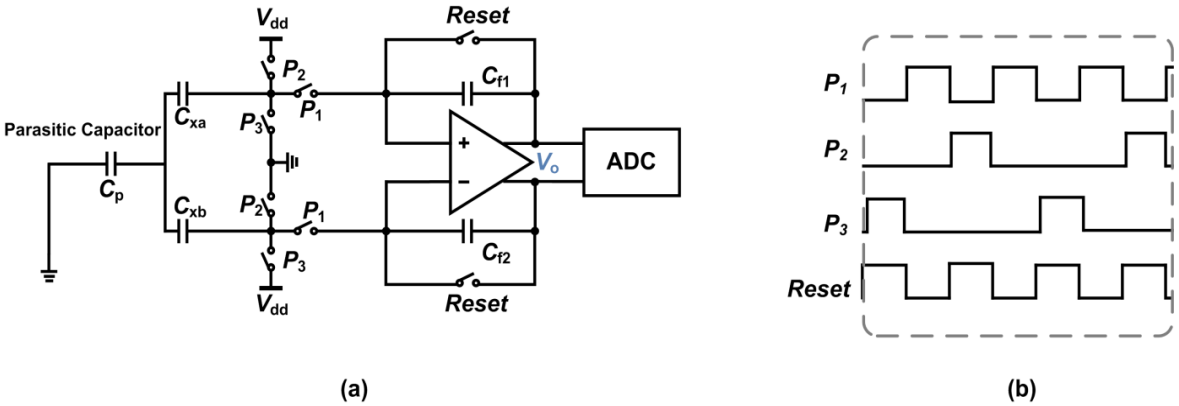

Figure 1.4 (a) Prior work front-end of the interface circuit; (b) and its timing scheme [5].

There are four clock phases (P_1, P_2 ,P_3 and *Reset*). In the first phase (Figure 1.4(a)), when only P_3 and *Reset* are on, C_{xa} and C_{xb} are charged to $V_{dd}/2$, while the feedback capacitors (C_{f1} and C_{f2}) are reset to zero. In the second phase, in which P_1 turns on, the charge stored on C_{xa}

and C_{xb} is transferred to the feedback capacitors. Assuming $C_{xa} = C_{xb} = C_x$ and $C_{f1} = C_{f2} = C_f$, the output voltage is:

$$V_o = (C_X/C_f).V_{dd} \quad 1.3$$

As explained in [7], the OTA's offset and flicker noise are chopped, and hence their impacts on the capacitive sensing are suppressed. In [7], V_o is then digitized by a subsequent ADC.

1.4 Proposed Interface Principle

In contrast to the prior work [7], which first converts the sensor capacitances to a proportional voltage and then digitizes it by means of an analog-to-digital converter (ADC), this work directly embeds the sensor capacitor into the input branch of a capacitance-to-digital converter (CDC). This leads to a simpler structure with lower die area and lower power consumption, which also reduces the number of potential error sources in the circuit. As shown in Figure 1.5, the sensing plates are driven by two anti-phase square-wave signals toggling between ground and V_{dd} and periodically connected to a switched-capacitor integrator.

To achieve high resolution (15 bits in this work), a $\Delta\sum$ ADC is the best candidate. Considering an integrator as a key building block of a $\Delta\sum$ modulator, in this work the sensor capacitor C_x is embedded into an integrator. During every clock phase, a differential charge of C_xV_{dd} is transferred to the integrator, while the noise on the floating target leads to a common-mode charge transfer suppressed by the common-mode rejection ratio of the interface.

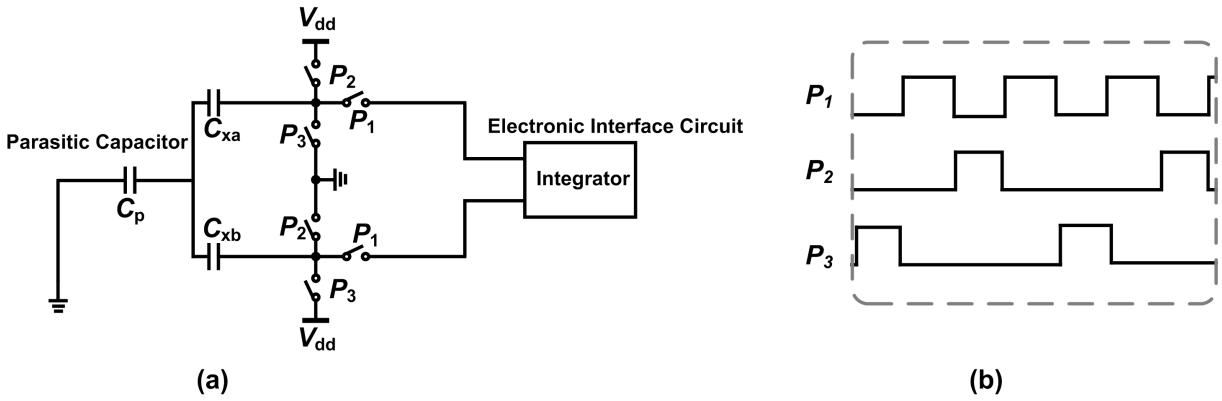

Figure 1.5 (a) Proposed interface circuit, (b) and its timing scheme.

1.5 Aim and Scope Of The Thesis

Section 1.1 has discusses that in order to have stable operation, normally capacitive sensor electronic interfaces need electrical contact with the moving target (membrane). However, this results in picking up external interferences and causing error in capacitive sensing.

The goal of this project is to design a capacitive sensor interface, which does not require such an electrical contact with the target and demonstrates performance comparable with the state-of-the-art. The designed prototype is intended for displacement measurement with a measurement range from 10 µm to 100 µm, and a resolution better than 15 bits. Considering the capacitor plate area, the sensor capacitor ranges from 0.6 pF to 6 pF. Table 1.1 lists the targeted sensor's features and technology's parameters of this project.

Table1.1 The targeted specifications in this project.

Parameter	Value
Technology	0.18 µm CMOS
Input range	0.6 pF -6 pF
Conversion time	1 ms
Supply voltage	1.8 V
Resolution	15 bits

1.6 Thesis Outline

The thesis includes five chapters, which present four different phases of the work on the project: investigation, simulations, design, and measurements. The thesis is organized as follows:

Chapter 1: an introduction to the work and discussion of the state of the art.

Chapter 2: proposed architecture and simulations results.

Chapter 3: circuit implementations and design details at circuit level.

Chapter 4: measurement results.

Chapter 5: conclusions and recommendations for future work.

Chapter 2 Architecture

2.1 Introduction

For producing digital output, a smart sensor has to incorporate an analog-to-digital converter (ADC). ΔΣ ADCs are suitable for high-resolution (> 12 bits) sensor applications [8] and therefore such converter is chosen in this work. Since an integrator is a key building block of a ΔΣ modulator, it will first be shown how the sensor capacitor C_x can be embedded into an integrator. Next, we will explain how other elements such as feedback DAC and zooming parasitic cancellation capacitors are added to the integrator.

2.2 Functional Block Diagram

Figure 2.1 shows the functional block diagram, which consists of the input capacitance C_x, zooming parasitic cancellation capacitors, feedback DAC, an integrator and the comparator. It can be seen that the sensor capacitor embeds into the input branch of a CDC. To optimize the use of the CDC's dynamic range, the modulator uses a programmable zoom-in DAC C_z to cancel the standoff sensor capacitance before digitizing. The charge, transferred to the integrator, is counterbalanced by a reference branch, which is composed of a reference capacitor C_{fb}. The details of each block will be presented in the following sections.

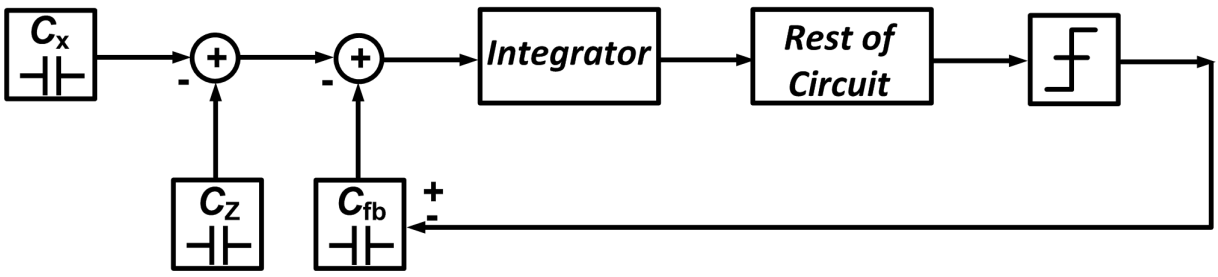

Figure 2.1 The functional block diagram.

2.3 Integrator

Figure 2.1 shows how the sensing capacitors C_{xa} and C_{xb} are embedded into an integrator. The circuit uses four different clocks (P_1, P_2 , P_3 and P_{ch}). Figure 2.2 depicts the circuit configuration at different clock phases. The following analysis is based on two assumptions: 1) the two sensing capacitors have equal values, 2) there is no static charge presented on the left plate of C_{xa} and C_{xb}.

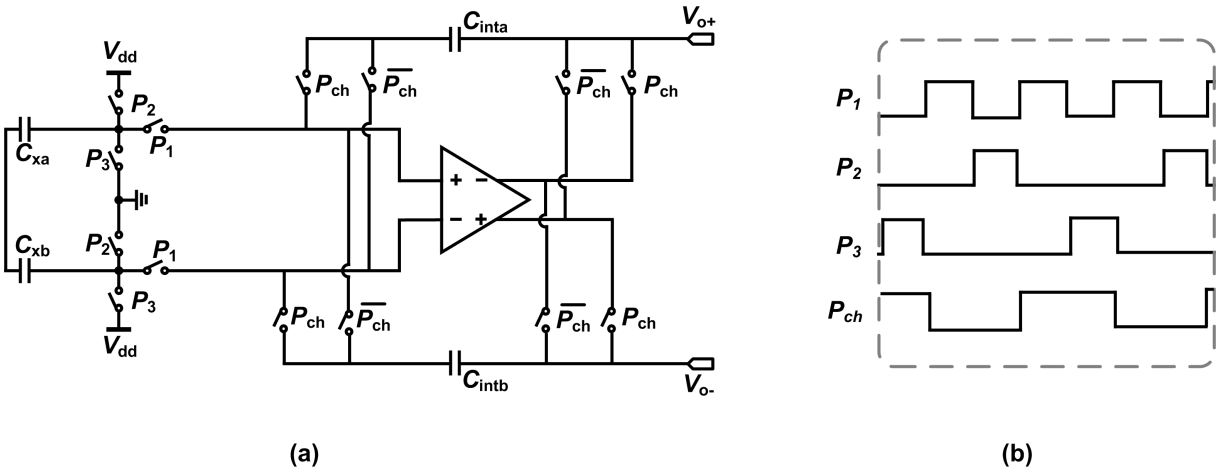

Figure 2.2 (a) An integrator with the sensor capacitor C_x, (b) and its timing diagram.

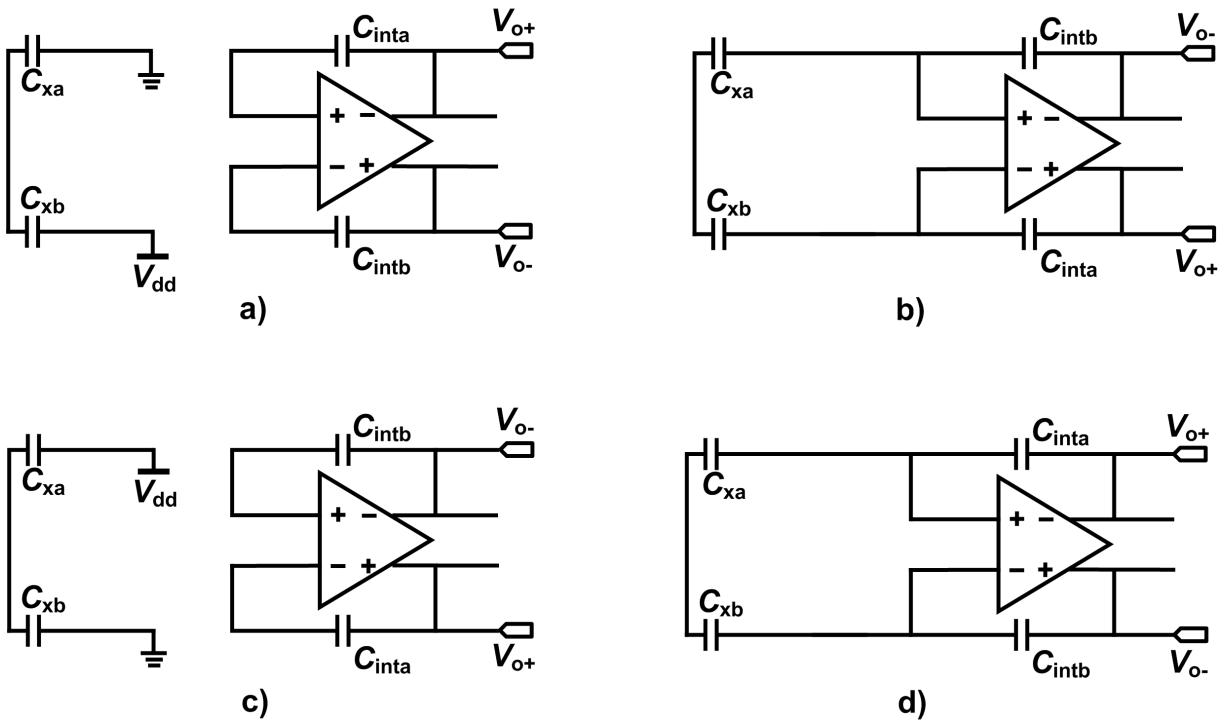

Figure 2.3 The circuit configuration in Figure 2.1 at different clock phases.

In the first phase (Figure 2.2(a)), when only P_3, P_{ch} are on, C_{xa} and C_{xb} are charged by $-V_{dd}/2$ $+V_{dd}/2$, respectively, while the output voltage holds its previous value $V_{out}(n-1)$. In the second phase, in which P_1 and P_{ch_B} turn on, the charge stored on C_{xa} and C_{xb} is transferred to the feedback capacitors C_{inta} and C_{intb}, respectively. Assuming that $C_{inta} = C_{intb} = C_{int}$, this leads to a new value of output voltage:

$$V_{out}(n) = V_{out}(n-1) - V_{dd}/2(C_{xa} + C_{xb})/C_{int} \qquad 2.1$$

In the third phase, C_{xa} and C_{xb} are charged to the voltages with opposite polarity to that in the first phase. The stored charge will be then transferred to the feedback capacitors during the fourth phase. The resulting output voltage is:

$$V_{out}(n+1) = V_{out}(n) - V_{dd}/2(C_{xa} + C_{xb})/C_{int} \qquad 2.2$$

As is clear from Figure 2.2, C_{inta} and C_{intb} are continuously changing their positions, in such a way that C_{inta} will always accumulate negative charge, while C_{intb} always accumulates positive charge, thus resulting in an integration action.

2.4 Offset Cancellation

Offset and flicker noise of the integrator's OTA degrades the capacitive-sensing performance. This section shows how the effect of these non-idealities, and hence how their impacts on the capacitive sensing are suppressed. The analysis in the previous section can be performed at the presence of an offset voltage V_{os} at the integrator's amplifier. With the aid of the circuit configuration in each of the 4 phases shown in Figure 2.3, equations (2.1) and (2.2) are modified as follows:

$$V_{out}(n)= V_{out}(n-1) - (V_{dd}/2((C_{xa} + C_{xb}) + C_{xa}V_{os}))/C_{int} \quad 2.3$$

$$V_{out}(n+1)= V_{out}(n) - (V_{dd}/2((C_{xa} + C_{xb}) - C_{xa}V_{os}))/C_{int} \quad 2.4$$

This shows that the offset (along with the flicker noise) is up-modulated to half of the integrator operating frequency and hence can be filtered out by the digital decimation filter.

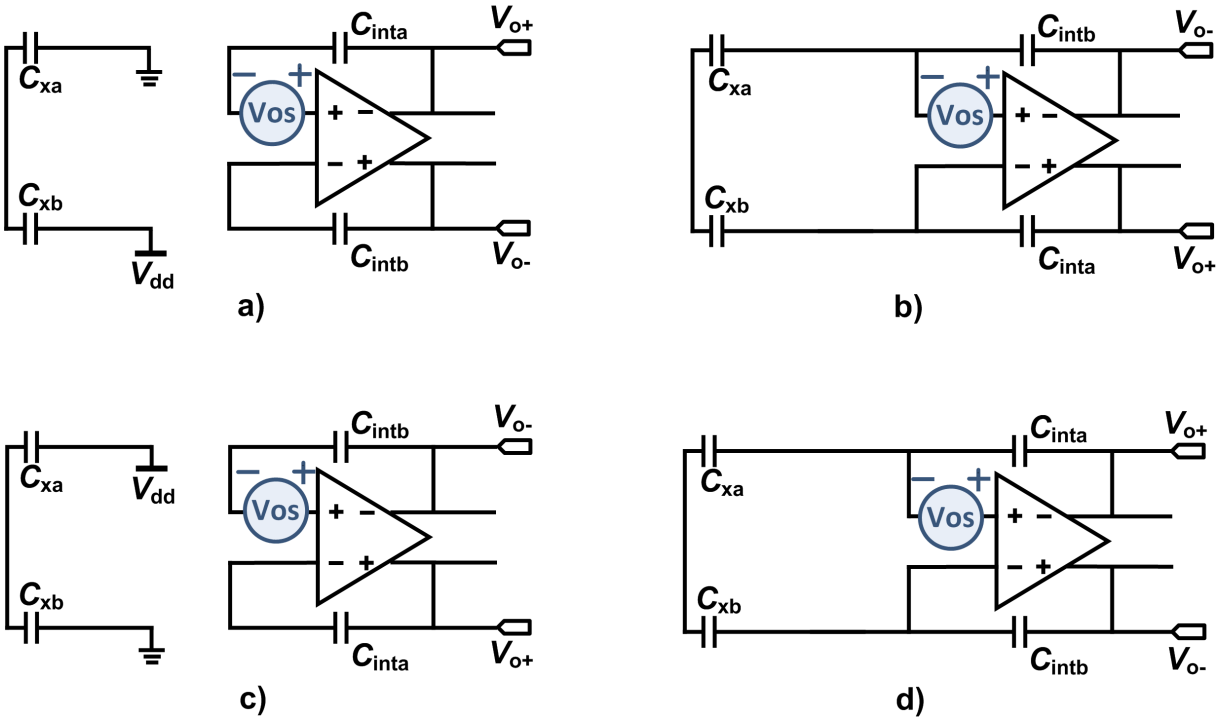

Figure 2.4 The four phases of operation of the integrator, with the help of which the offset is cancelled.

2.5 Feedback DAC Reference

Feedback DAC is a key element of a ΔΣ ADC. As is shown in Figure 2.4, the operating principal of the feedback branch is similar to the input branch. So, while the input capacitors (C_{xa} and C_{xb}) are being charged, the feedback capacitors (C_{fb}) are transferring their charged to the integrator and the other way around.

The polarity of the charge transferred by feedback capacitors to the integrator is controlled by the CDC output bit-stream; For example, if the value of a bit stream is -1 then the output voltage is:

$$V_{out}(n+1)=V_{out}(n) - V_{dd}(C_x/C_{int}) + V_{dd}(C_{fb}/C_{int}) \quad 2.5$$

And if the value of BS is +1 then:

$$V_{out}(n+1)=V_{out}(n) - V_{dd}(C_x/C_{int}) - V_{dd}(C_{fb}/C_{int}) \quad 2.6$$

Therefore, the average (decimated) value μ is

$$\mu = C_x/C_{fb} \quad 2.7$$

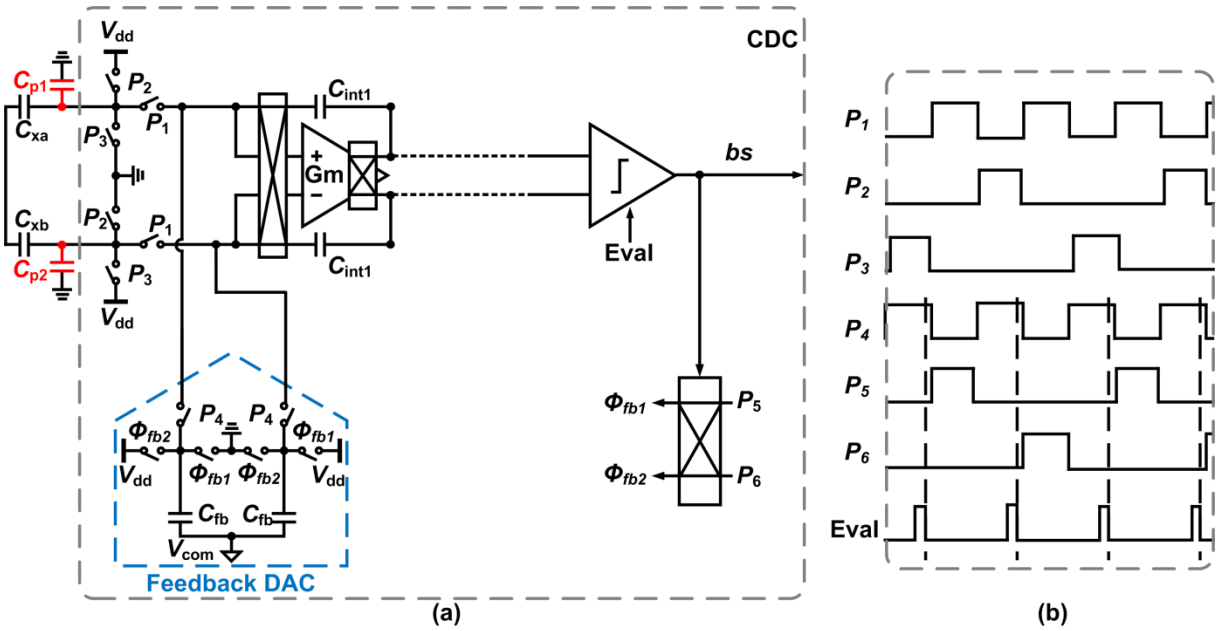

Figure 2.5 (a) The first integrator of the ΔΣ modulator with the feedback DAC, (b) and the timing scheme.

2.6 Zoom-in Capacitor

The wiring between the sensing probe and the readout electronics introduces a parasitic capacitance to ground. The crux of the matter is that these parasitic capacitors are adding to the sensing capacitance. On the one hand, the feedback capacitance should be greater than C_x+C_p while on the other hand, the value of C_p is unknown and C_{fb} cannot be too large (big quantization noise out of DSM), the cancellation of C_p is of crucial importance. As a result, to optimize the use of the CDC's dynamic range, the modulator uses a programmable zoom-in DAC C_z to cancel the standoff sensor capacitance before digitizing.

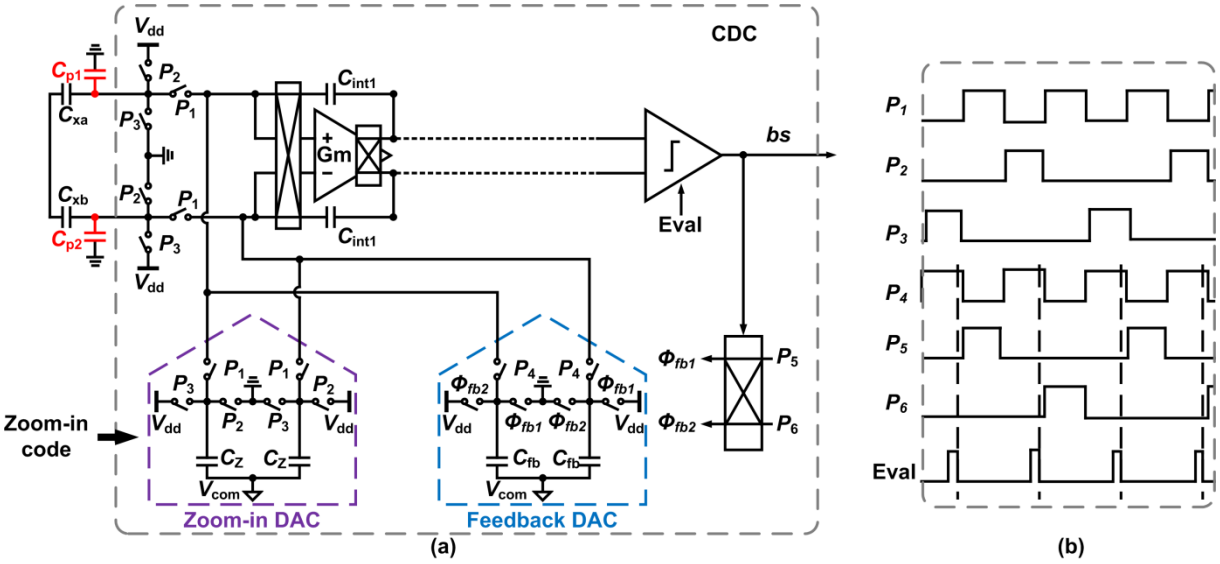

Figure 2.6 (a) The first integrator of the ΔΣ modulator with feedback DAC and the Zoom-in capacitor, (b) and the timing diagram.

So far, all three input branches have been discussed in details. Figure 2.5 shows all input branches. To summarize, the total input signal charge is:

$$\text{Total input signal charge} = (C_x + C_p - C_z \pm C_{fb}).\ V_{dd} \qquad 2.8$$

2.7 Selection of The C_{fb}

It has been discussed that in order for the ΔΣ ADC to be operating and to be stable, the feedback DAC capacitor C_{fb} should be larger than the total effective input capacitor $C_x+C_p-C_z$. The sensor capacitor C_x ranges from 0.6 pF to 6 pF. This is accompanied with a parasitic capacitor C_p on the order of 10 pF, for which a programmable zoom-in parasitic-cancellation capacitor (0 pF < C_z < 31 pF) is added to the circuit. Assuming that C_p and C_z cancels each other, C_{fb} of 10 pF satisfies the condition $C_{fb} > C_x+C_p-C_z$.

The detection limit of the capacitive sensing C_{res} for 15-bit resolution performance can be calculated as,

$$C_{res} = (6\text{ pF} - 0.6\text{ pF})/\ 2^{(15+1)} = 80\text{ aF} \qquad 2.9$$

Multiplying C_{res} by V_{dd} leads to resolution in input charge

$$Q_{res} = C_{res} \cdot V_{dd} \approx 140 \text{ aC} \quad (2.10)$$

The total input charge noise is determined by the *kTC* noise of the total input capacitor of the input capacitor C_{in} [9]

$$C_{in} = C_x + C_{fb} + C_p + C_z = 6\text{pF}+10\text{pF}+30\text{pF}+30\text{pF}=76\text{pF} \quad (2.11)$$

As shown in [9], the total input charge noise in one clock cycle can be approximated as

$$Q_n = \sqrt{4\text{kTCin}} \quad (2.12)$$

This charge noise is uniformly distributed from DC to half of the sampling frequency $F_s/2$, while the noise in the signal bandwidth spans from DC to bandwidth of interest F_b. The charge noise in the signal bandwidth therefore can be calculated as

$$Q_{res} = \sqrt{8\text{kT}Cin(\frac{\text{Fb}}{\frac{\text{Fs}}{2}})} \quad (2.13)$$

This equation implies that the only degree of freedom to reduce the noise is the sampling frequency F_S; increasing F_S leads to a better noise performance. However, at the same time, it proportionally increases the power consumption, as the switched-capacitor circuit should sufficiently settle in a shorter time period. For power efficiency purpose, as a result, we should choose the minimum required F_S. Combining (2.10), (2.11), and (2.13) results in

$$\sqrt{8\text{kT } 76 \text{ pF } (\frac{1\text{KHz}}{\frac{\text{Fs}}{2}})} < 140 \text{ aC} \quad (2.14)$$

This requires the minimum sampling frequency F_S of 300KHz for the modulator.

2.8 Architecture choice of the ΔΣ Modulator

A ΔΣ modulator consists of a loop filter, which by means of a charge-balancing scheme performs noise shaping on its digital output signal. The oversampling ratio (*OSR*) is defined as $OSR = F_s/2F_b$, where F_s is the sampling frequency and F_b is the bandwidth frequency. ΔΣ modulators shape the quantization noise by pushing it away from the frequency band of interest to outside of that band. This out-of-band noise can then be filter out with the following digital decimation filter. An energy efficient design of this modulator mandates the in-band noise to be dominated by the thermal noise rather than the quantization noise. This is because reducing thermal noise requires significant power consumption (1 bit improvement in thermal noise entails 4x increase in power consumption), while the quantization noise can be reduced by a small power penalty [9]. In order to find the most appropriate order of ΔΣ modulator, in which thermal noise is limited within the bandwidth frequency F_b and Quantization noise will be out of F_b, some behavioral simulations have been done.

The behavioral simulation starts with a 1st order ΔΣ modulator with a single-bit quanrizer as it is the simplest one. The diagram of Figure 2.6 is simulated in MATLAB. The simulation results are presented in Figure 2.7. The simulations confirm that 1st-order ΔΣ has high quantization noise and in order to make it thermal noise limited (push the q-noise output of the bandwidth), sampling frequency should be above 5 MHz. This sampling frequency is much higher than what required by the thermal noise and comes at expense of significant power penalty.

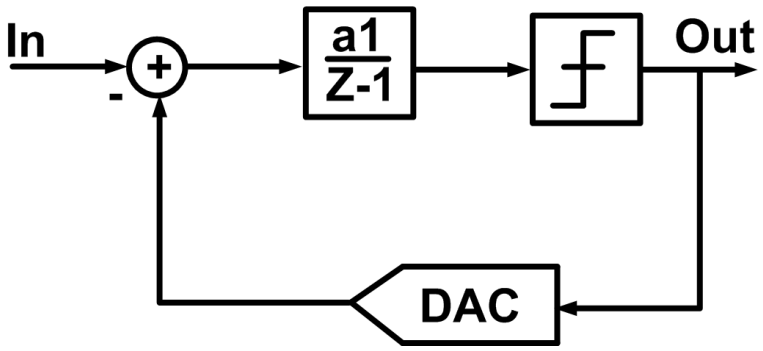

Figure 2.7 Block diagram of a 1st order ΔΣ modulator.

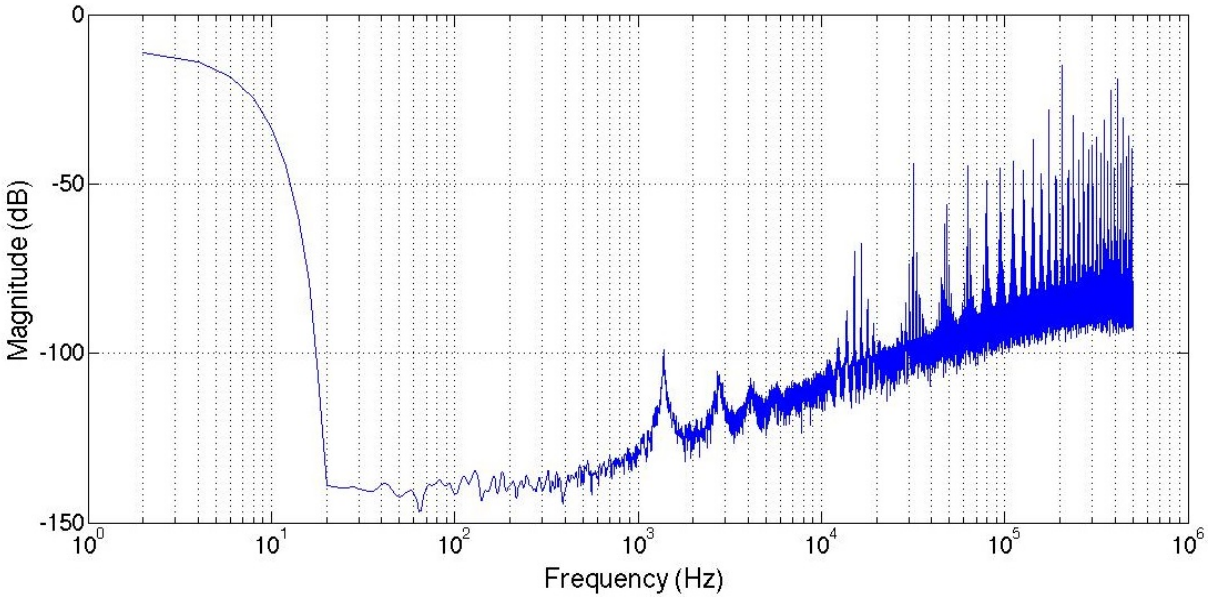

Figure 2.8 The noise shaping simulation results of a 1st order ΔΣ modulator.

Alternatively, the quantization noise can be suppressed by using either a multi-bit quantizer or increasing the order of the loop filter. Using a multi-bit quatizer, however, requires a multi-bit feedback DAC, which introduces non-linearity due to its components mismatch [8]. This non-linearity, which directly impacts the capacitive sensing performance, can be mitigated by using dynamic-element-matching (DEM) techniques. However, it adds complexity and hence is not a primary choice for use in this work. Instead a 2nd order ΔΣ is considered for further investigations.

However, using the same simulations for 2nd order ΔΣ modulator (see Figure 2.9) show that with a sampling frequency of 1 MHz, a 2nd order ΔΣ is thermal noise limited within fb=1 KHz. Therefore, to reduce the required sampling frequency and thermal noise a 2nd order ΔΣ is preferable. A 2nd order ΔΣ modulator can be implemented either with distributed feedback or distributed feedforward topologies (or even a combination). To reduce the signal swing a feedforward structure (shown in Figure 2.8) is chosen. As it is shown in Figure 2.8, to ensure the stability of the modulator, a feedforward branch (C_1) is applied from the first integrator output to the second integrator output.

Although with a 3rd order ΔΣ modulator, sampling frequency can be further reduced, it trades off with the loop stability and circuit complexity. In addition F_S is bounded to 300 kHz by the thermal noise requirements and the choice of F_S = 1 MHz is reasonable in this design. To conclude, a 2nd order feed-forward ΔΣ ADC with F_S = 1 MHz is used in this work.

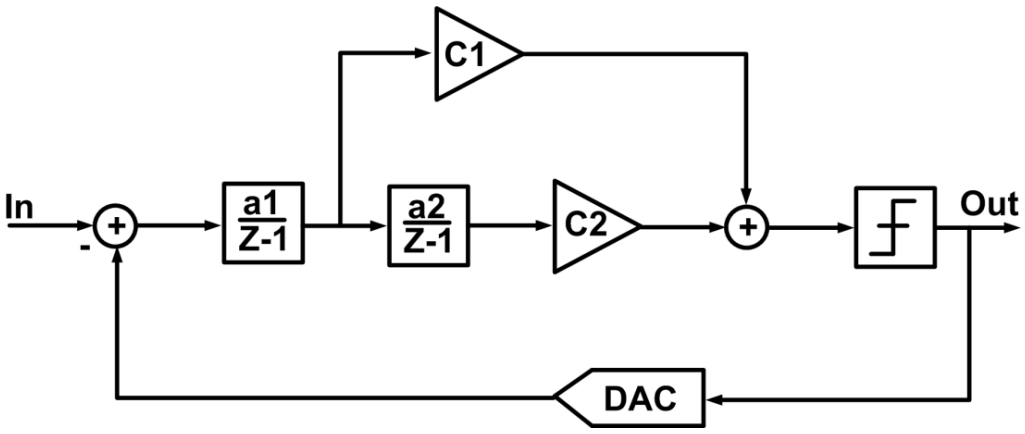

Figure 2.9 Block diagram of a 2nd order ΔΣ modulator with feedforward topology.

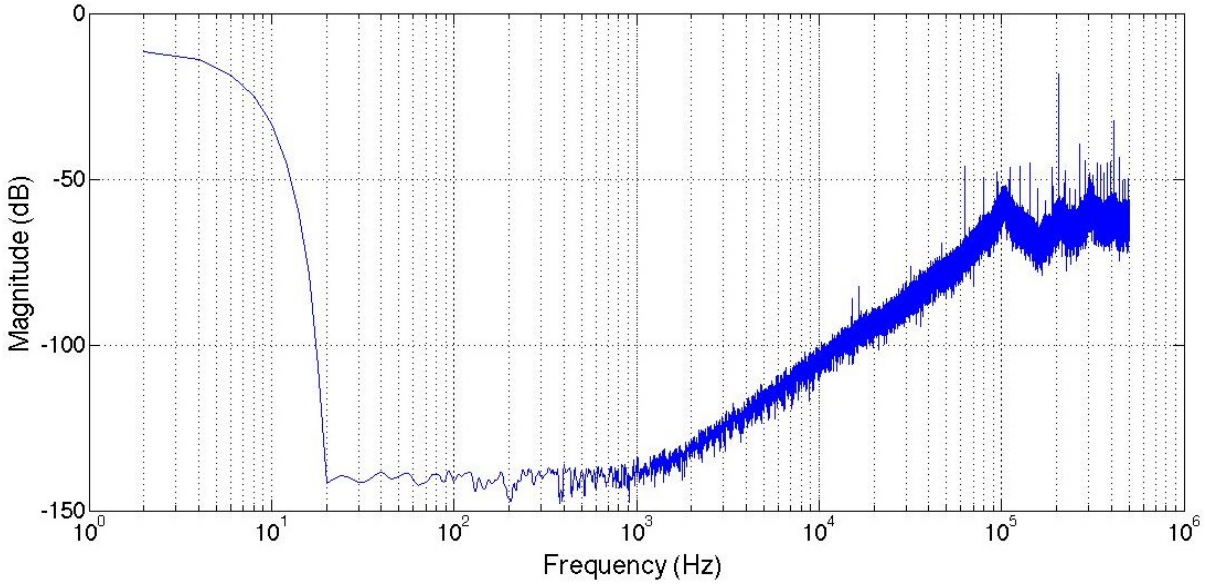

Figure 2.10 The noise shaping simulation results of a 2nd order ΔΣ modulator.

2.9 Conclusion

It is shown that in contrast to [2] which uses anti-phase sinusoidal driving currents and measures the voltage drop over C_s, and [7] which first converts Q_{Cs} into a proportional voltage and then digitizes it, this work directly embeds the sensor capacitor into the input branch of a CDC and digitizes the signal in charge domain. This leads to a lower power consumption and reduces the number of potential error sources. The sensing plates are driven by two anti-phase square-wave signals toggling between ground and V_{dd} and periodically connected to a switched-capacitor integrator. During every clock phase, a differential charge of C_sV_{dd} is transferred to the integrator, while the noise on the floating target leads to a common-mode charge transfer suppressed by the common-mode rejection ratio of the interface. To optimize the use of the CDC's dynamic range, the modulator uses a programmable zoom-in DAC C_z (up to 31 pF) to cancel the standoff sensor capacitance before digitizing. The chopper, placed at the integrator OTA's input, rectifies the square-wave charge delivered by the input capacitors and accumulates it in the integration capacitors C_{int1}. In addition, it up-modulates the OTA's offset and flicker noise to the chopping frequency, which is then cancelled by the

output decimation filter. The differential charge, transferred to the integrator, is counterbalanced by a reference branch, which is composed of a reference capacitor C_{fb} (=10 pF). Depending on the output bit-stream, it delivers a charge packet of $\pm C_{fb}V_{dd}$. This conversion results in an output bit-stream with an average value of $(C_s - C_z)/C_{fb}$.

Chapter 3 Circuit-level design and implementation

3.1 Introduction

This chapter presents the circuit-level design of the building blocks presented in the previous chapter. Following a top-down design approach - from a system concept to its implementation, this chapter provides functionality and architecture of OTAs, passive adder, comparator, biasing and the layout.

3.2 OTAs design

The design methodology of an op-amp depends on the specifications that the circuit must meet. In this work, the OTA used in the integrator should provide enough trans-conductance for the switched-capacitor circuitry to sufficiently settle within 0.5 us (F_S = 1 MHz). In one cycle the input capacitance is equal to C_x+C_p+C_z and in the other cycle, the input capacitance is equal to C_{fb}. To calculate the value of g_m, the worst-case situation, i.e., with the larger input capacitor of C_{in}=C_x+C_p+C_z is considered.

Assuming a worst-case situation in which, C_x, C_p, C_z are equal to 6 pF, 30 pF, and 30 pF, respectively, the input capacitor C_{in} value is 66 pF. Knowing F_s = 1 MHz and having 15-bit resolution, a very conservative estimation of f_{-3dB} is [9]:

$$f_{-3dB} > f_s(n+1)\frac{ln(2)}{\pi} \rightarrow f_{-3dB} > 10^6(15+1)\frac{ln(2)}{\pi} \rightarrow f_{-3dB} = 3.5 \text{ MHz} \qquad 3.1$$

Then

$$g_m = 2\pi \cdot f_{-3dB} \cdot C_{in} = 1.5 \text{ mS} \qquad 3.2$$

Assuming the transistors in the input pair of the OTA are in weak inversion, their required bias current can be estimated as:

$$g_m = I_D / 1.5 \cdot V_T \Rightarrow I_D = 57\mu A \quad (3.3)$$

In which V_T is the thermal voltage and its value is 26 mV at room temperature. This suggests a tail bias current of 114 uA for the OTA input pair. However, as mentioned, this is a conservative estimation and the OTA can usually be realized with lower value of g_m and hence with lower power consumption. For the sake of the flexibility, the OTA's transconductance g_m is made programmable; the OTA's bias current is made programmable such that g_m values of 0.5 mS, 1 mS, 1.5 mS and 2 mS can be achieved. The details of the biasing circuit can be found in section 3.3. Measurement in Chapter 4 shows that target specifications can be met with g_m = 0.5 mS.

Figure 3.1 and 3.2 illustrate the 1st OTA (for g_m = 0.5 mS) and 2nd OTA structures, respectively. For both OTAs, in order to achieve high gain, the folded cascade structure with PMOS input pair is chosen. The details of OTAs such as transistors size and branch currents are also shown in these figures.

Since the amplifier is fully differential with high output impedance, a common-mode feedback (CMFB) circuitry is needed to ensure that the output common-mode level of transconductor at the desired value (0.9 V in this design). The CMFB circuitry is shown by a symbol (VCMFB) in Figures 3.1 and 3.2.

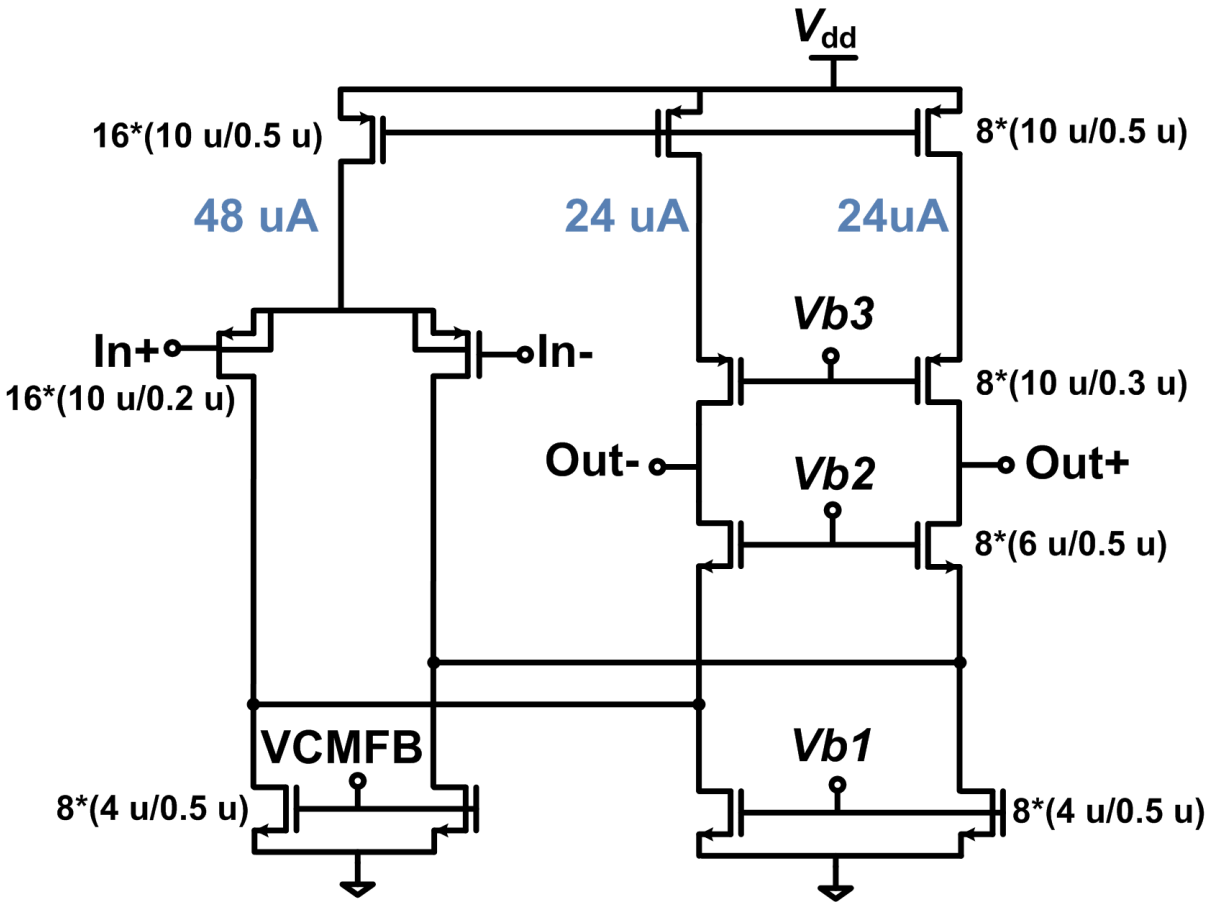

Figure 3.1 A simplified schematic of the 1st OTA and transistors values.

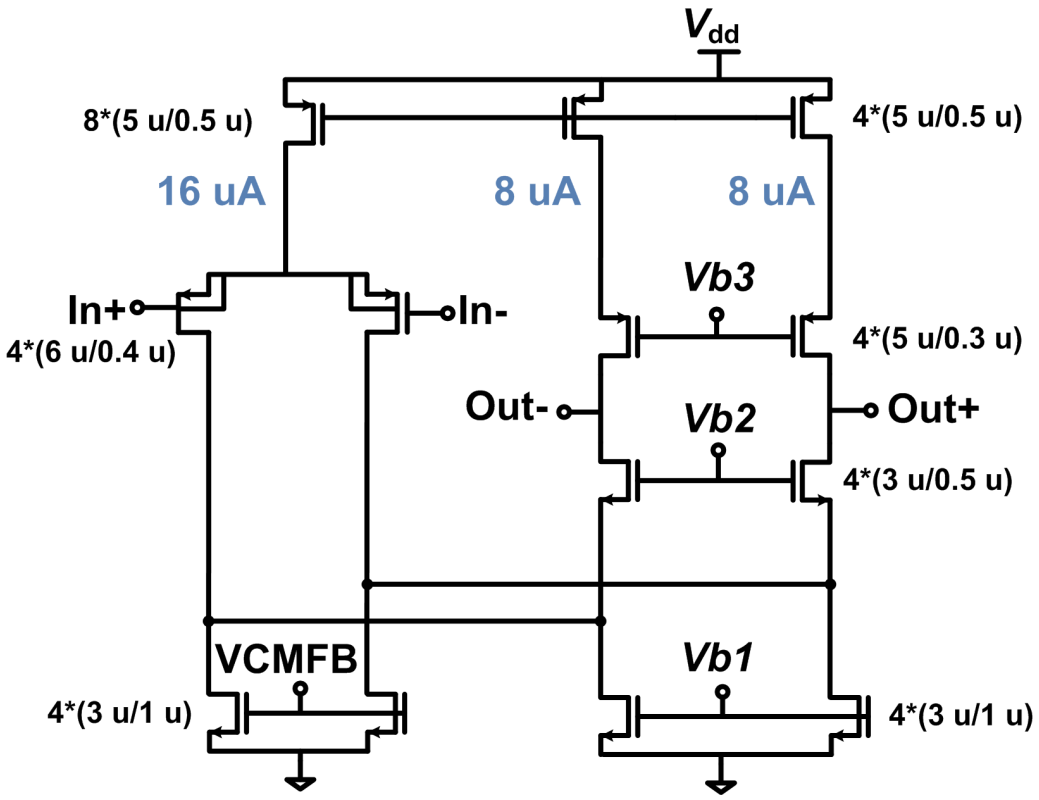

Figure 3.2 A simplified schematic of the 2nd integrator's OTA and its transistors' sizes.

3.3 Switches' Size

Choosing the size of the switches involves a compromise between its ON-resistance R_{on} and its charge injection. Increasing the size of the switch (by increasing its width W) helps to reduce its R_{on}, which is better for settling, but leads to more charge injection. In practice, the switches are resized in a way that the integrator settling is mainly determined by the OTA's gm value, meaning that $1/g_m$ must be larger than the switches R_{on}. This implies that the switches' R_{on} must be less than 0.5 kΩ.

Figure 3.3 shows the type input switches of the 1st integrator: 1) SW_N, tied to ground, is implemented by means of NMOS transistors, each with an aspect ratio W/L = 1μm/0.18μm, resulting in a nominal R_{on} equal to 0.3 kΩ, 2) SW_P, tied to V_{dd}, is realized by means of PMOS transistors with an aspect ratio W/L = 2μm/0.18μm, resulting in a nominal R_{on} equal to 0.4 kΩ,

3) SW_T, located at the virtual ground with a common mode voltage of 0.9V, are transmission gate switched, with NMOS and PMOS aspect ratio of 4μm/0.18μm and 10μm/0.18μm, respectively, which leads to its R_{on} = 1 kΩ. Obviously, this is twice the value calculated above and it should be reduced in the next improved design.

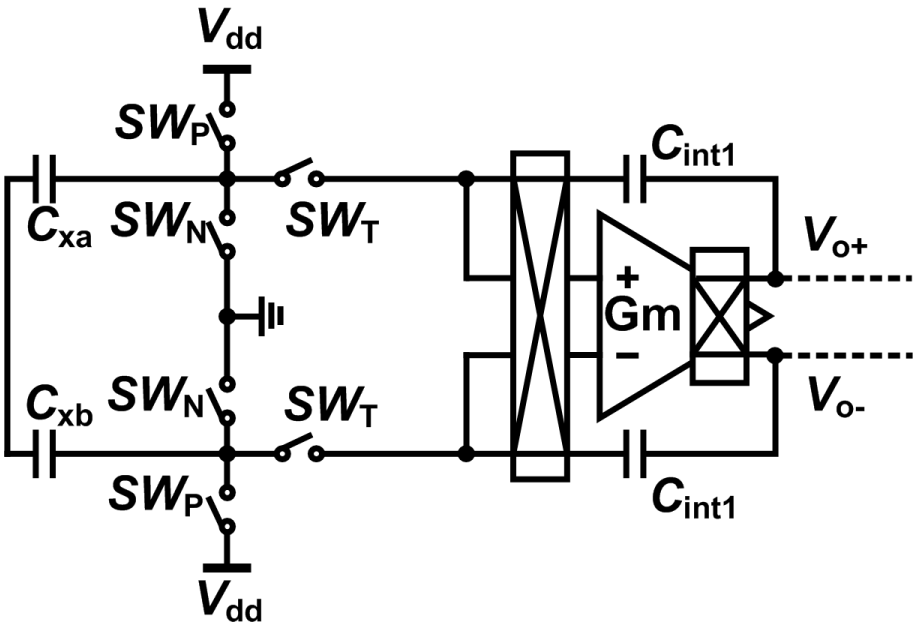

Figure 3.3 The type of input switches of the first integrator.

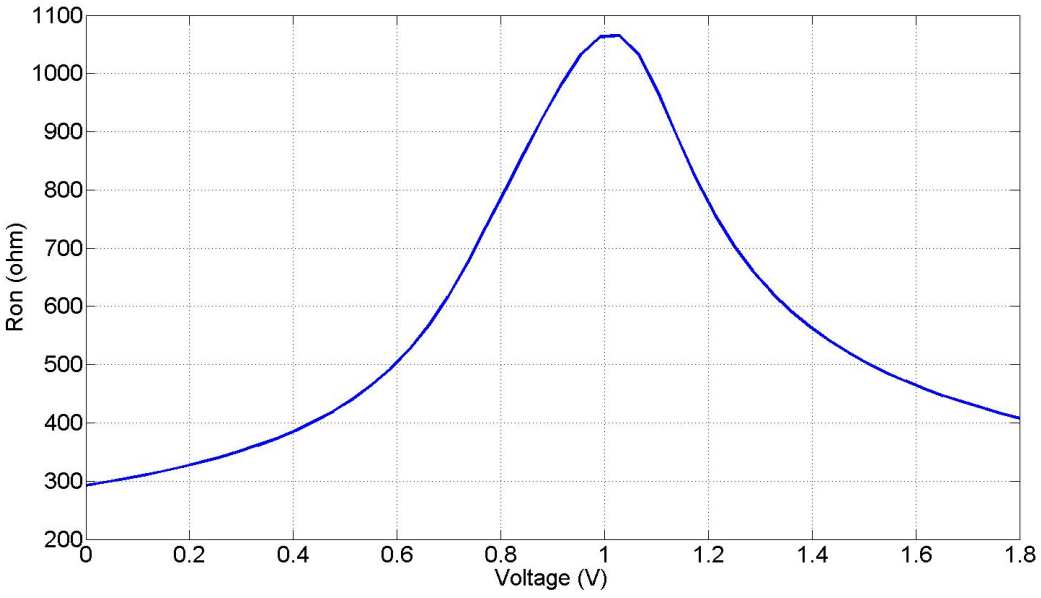

Figure 3.4 On-resistance of a T-gate switch versus its input voltage.

3.4 Modulator's Complete Circuit Diagram

Figure 3.5 depicts the complete circuit diagram of the modulator. The 2nd integrator is also a switch-capacitor one with a sampling capacitor of 206 fF. The feedforward path is realized by mean of a switched-capacitor passive adder at the input of the comparator. This adder is reset at P_1 and adds the two integrators' outputs at P_2.

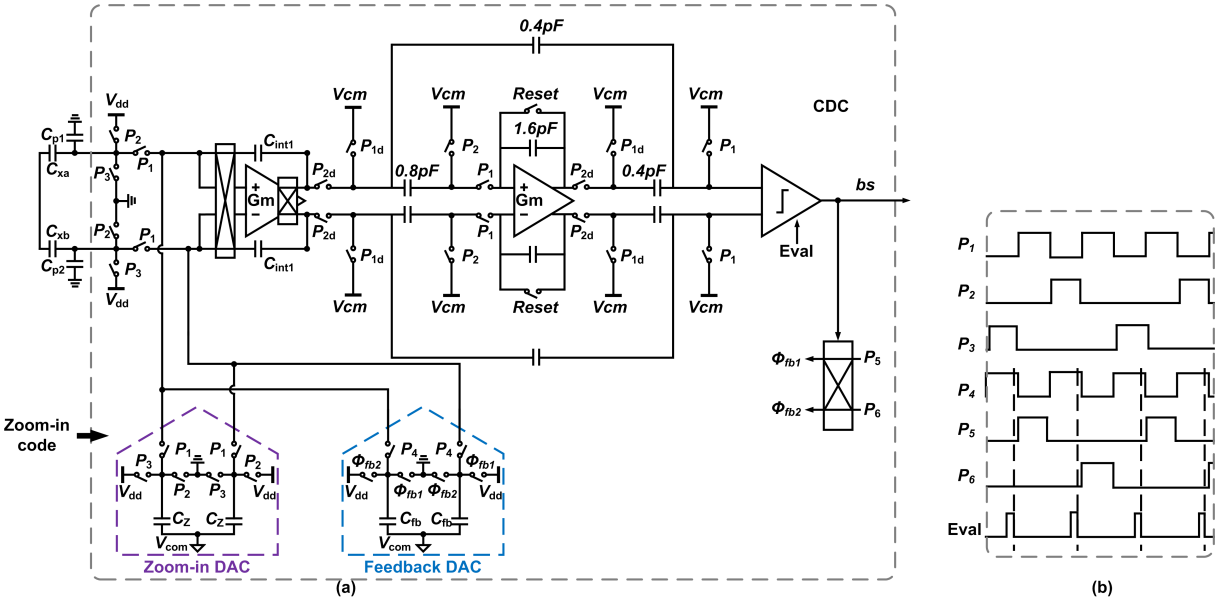

Figure 3.5 (a) Second stage schematic, (b) and its timing diagram.

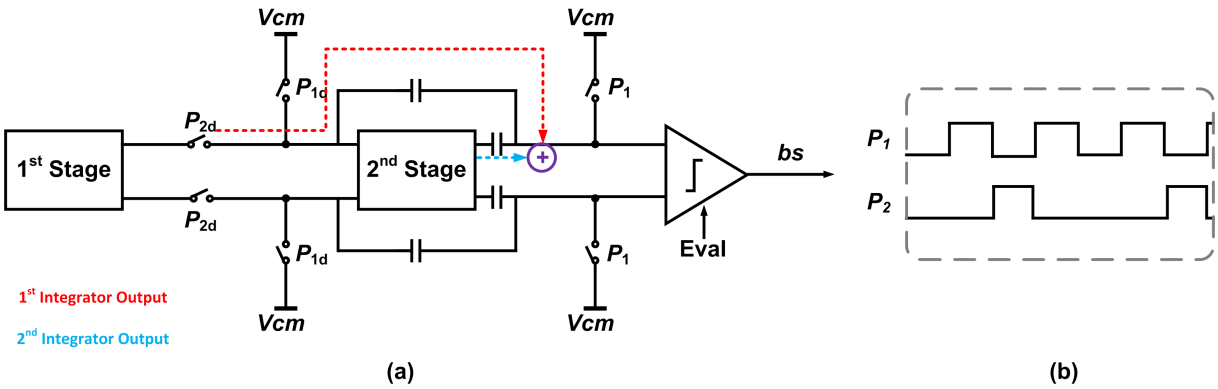

Figure 3.6 (a) The passive adder structure, (b) and its timing diagram.

3.5 Comparator

The comparator is implemented as a dynamic latch proceeded by two preamplifiers (Figure 3.7). Each pre-amplifier provides a voltage gain of 5, while consuming 3 uA of supply current. The output loads of the pre-amplifiers are chosen to be as a combination of normal and cross-coupled diode-connected NMOS transistor. This helps to increase the preamplifier output impedance and hence its voltage gain. The gain can be expressed as

$$A_{\text{Pre-amp}} \approx -g_{m1} / (g_{m2} - g_{m3}) = -g_{m1} / (3g_{m1}/5 - 2g_{m1}/5) = -5 \qquad 3.4$$

When P_{Eval} is zero, the comparator is reset. At the rising edge of the clock signal P_{Eval} the comparator makes a decision. The comparator's decision time T_{Eval} should be much shorter than half a clock period of 5 us. In this design, by consuming enough current in the pre-amplifier and choosing minimum gate length L = 0.18 um for the transistor in the latch, T_{Eval} for a small comparator input voltage of 100 uV is ensured to be lower than 20 ns.

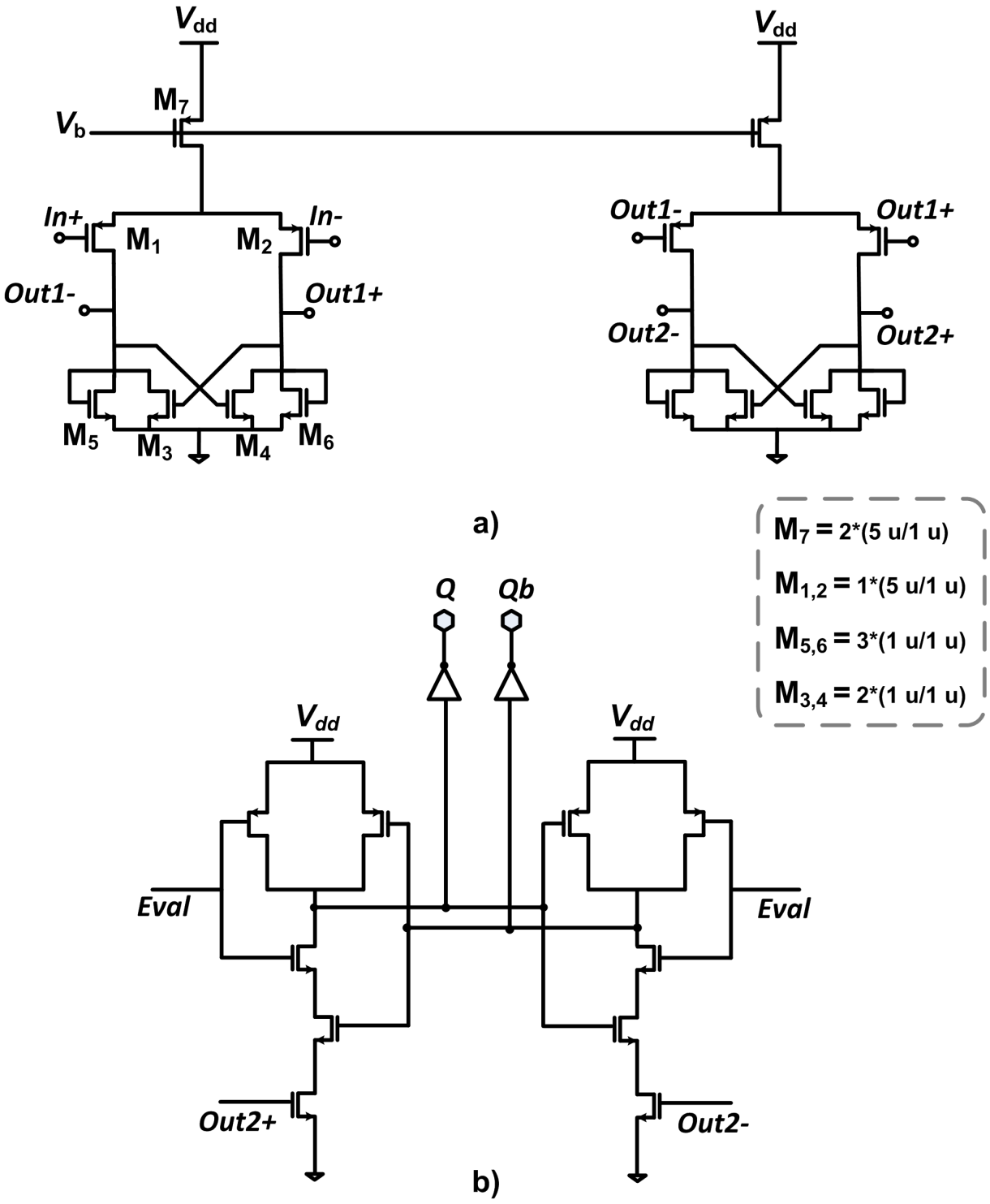

Figure 3.7 Comparator implementation (a) The two preamplifiers, (b) and a dynamic latch.

3.6 Biasing

This section deals with the design of current mirrors as biasing elements [11]. Figure 3.8 shows how biasing currents for 1st OTA, 2nd OTA, and comparator is created. The design of current sources in each block is based on copying currents from the reference current shown in Figure 3.8.

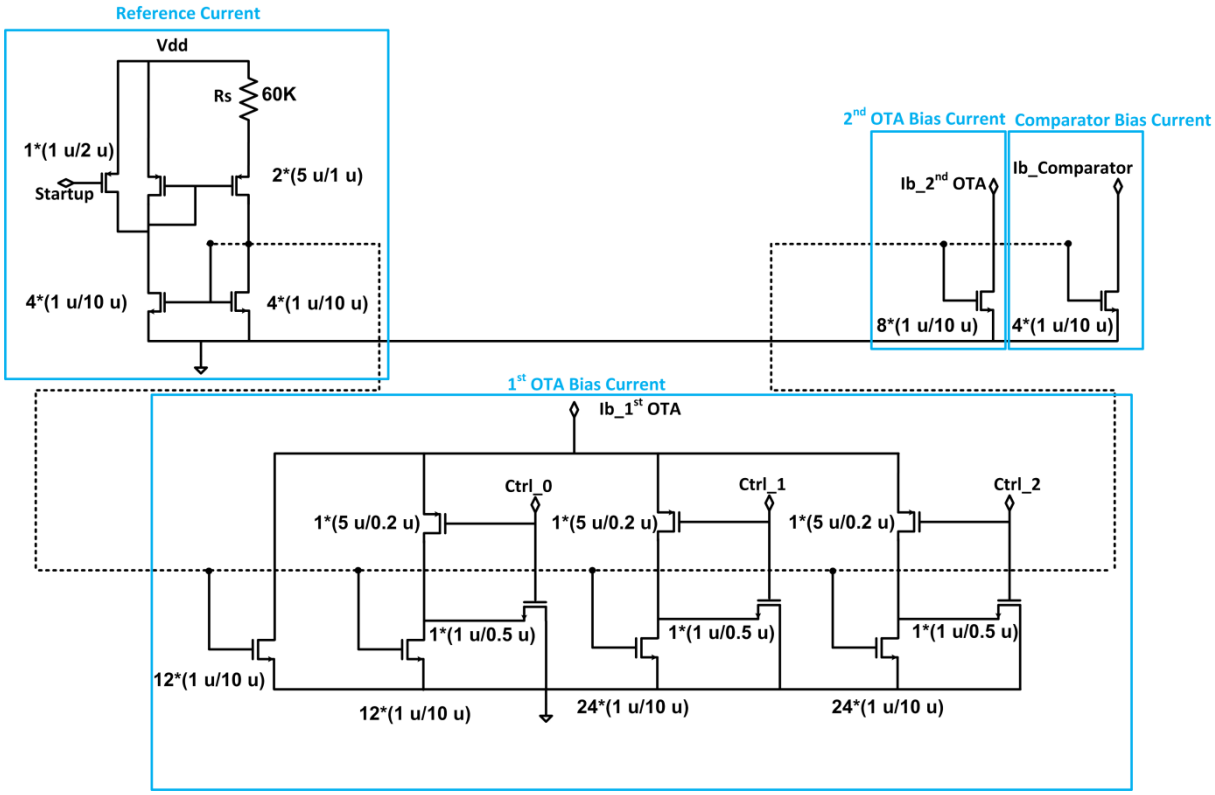

Figure 3.8 Biasing Circuit.

3.7 Layout

After finalizing of all verifications, the chip is taped out. Figure 3.9 depicts the layout of the test chip in which some important parts are highlighted.

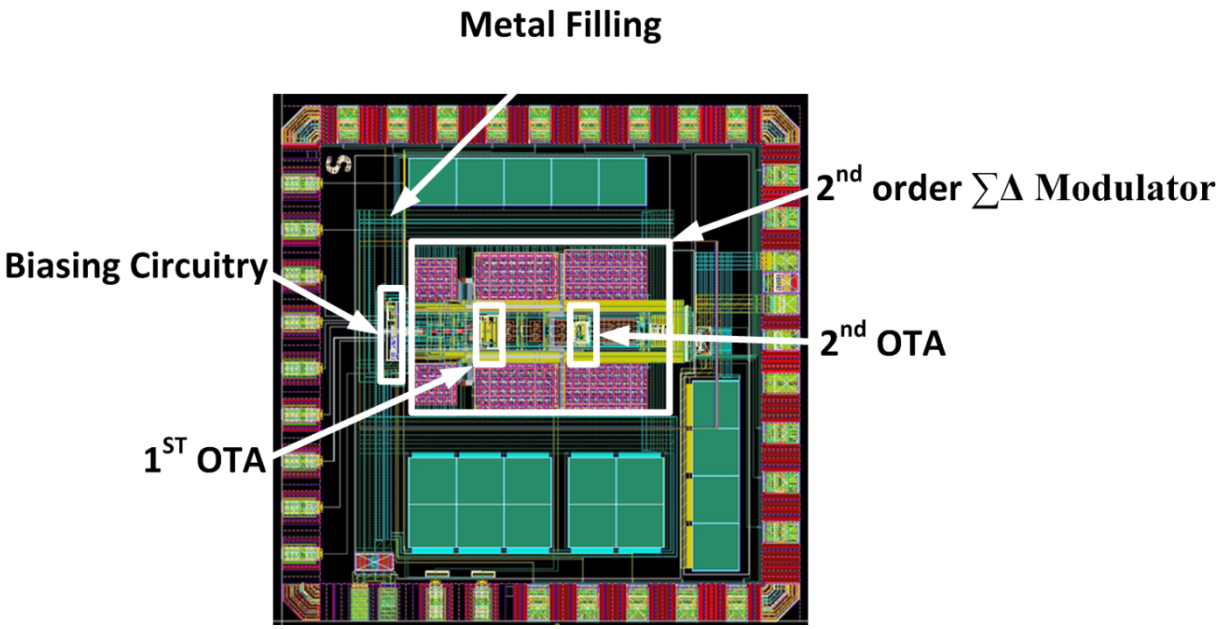

Figure 3.9 The layout of the test chip.

Chapter 4 Measurement results

4.1 Introduction

The CDC was realized in a standard 0.18µm TSMC CMOS process (Figure 4.1). It occupies an active area of 0.5mm^2 and is packaged in a DIL40 ceramic package.

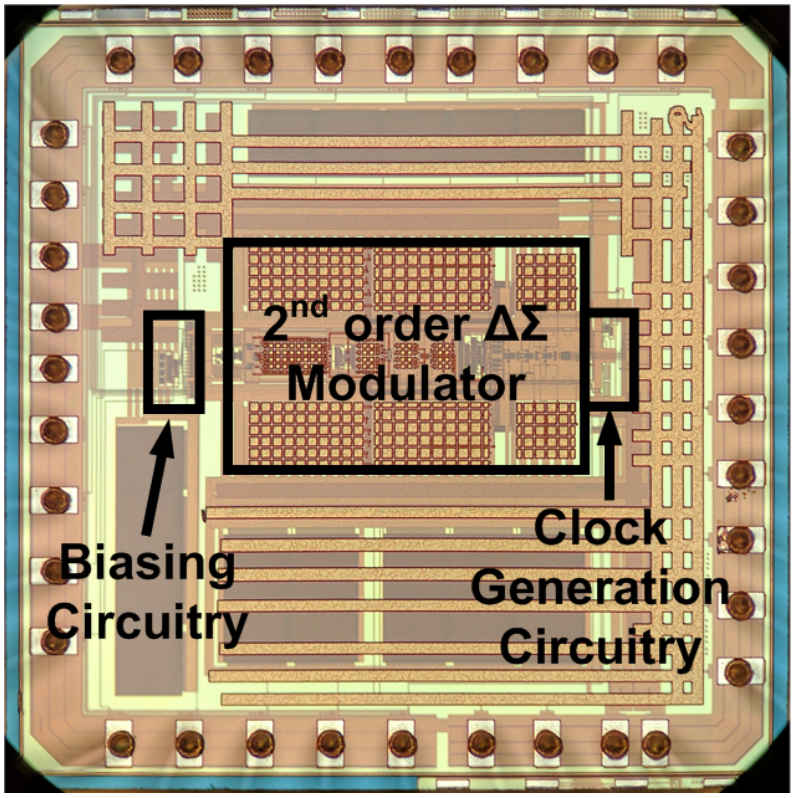

Figure 4.1 Die micrograph.

The setup of the measurement is shown in Figure 4.2. The CDC draws 200 µA from a 1.8 V supply. For flexibility, the decimation filter is implemented off-chip. At a sampling clock frequency of 1 MHz, and up to 6 kHz of bandwidth, the CDC is *kT/C* noise limited (Figure 4.3), achieving 15-bit resolution in a conversion time T_{conv} of 1ms. Figure 4.4 shows the CDC's measured transfer characteristics without zoom-in.

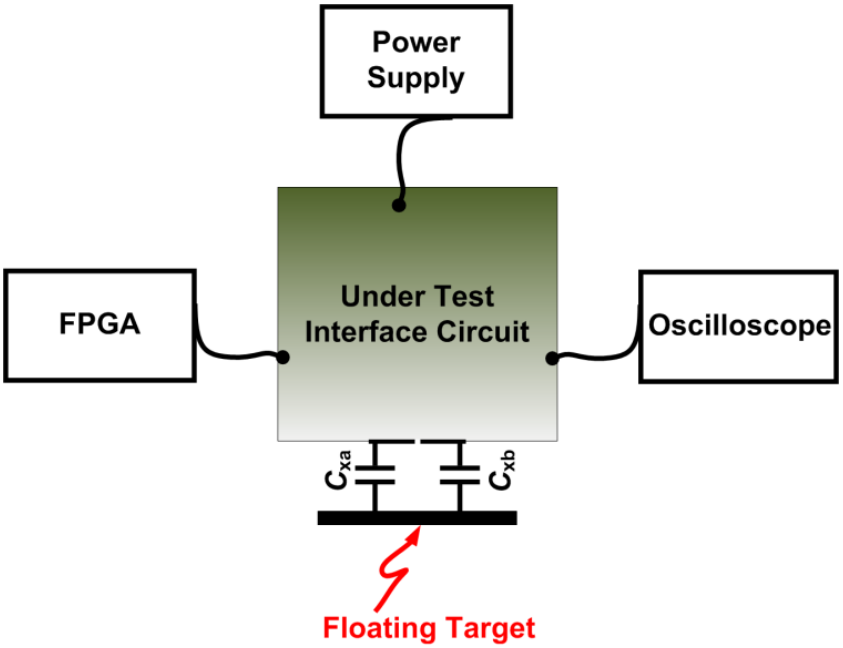

Figure 4.2 Measurement setup.

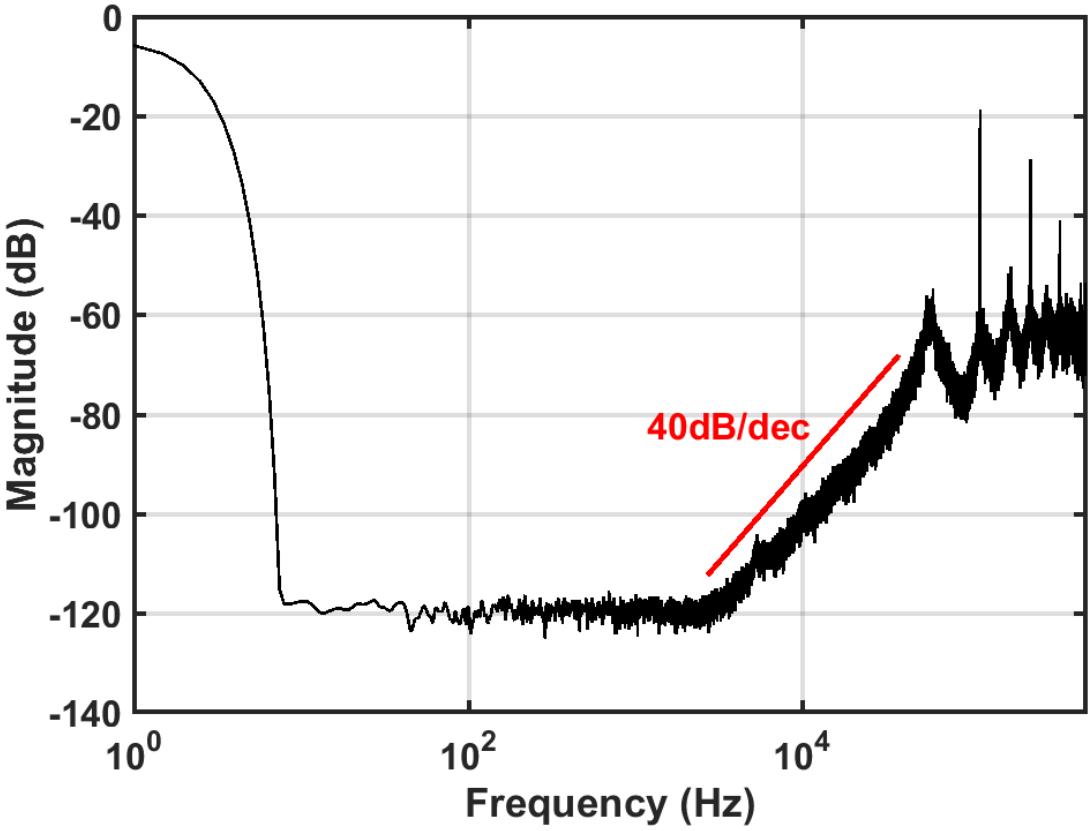

Figure 4.3 FFT of CDC output bit-stream.

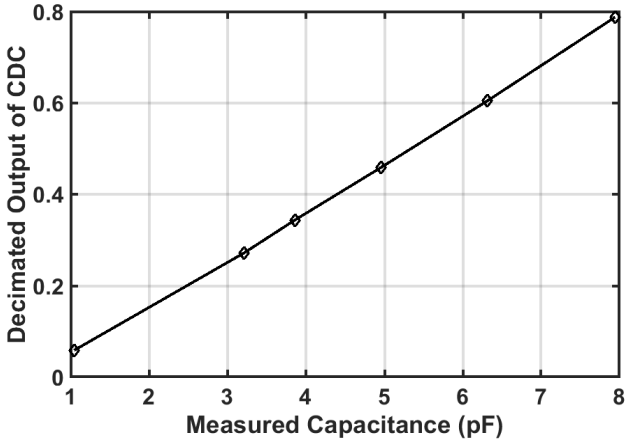

Figure 4.4 CDC input-output characteristics.

To evaluate the interference rejection ratio of the proposed CDC, interferences with different frequencies are injected into the floating electrode through a 10 pF capacitor (C_p), driven by a sinusoidal voltage source with 9 V_{rms} amplitude. As shown in Figure 4.5, the in-band interference rejection ratio of the CDC is higher than 104 dB.

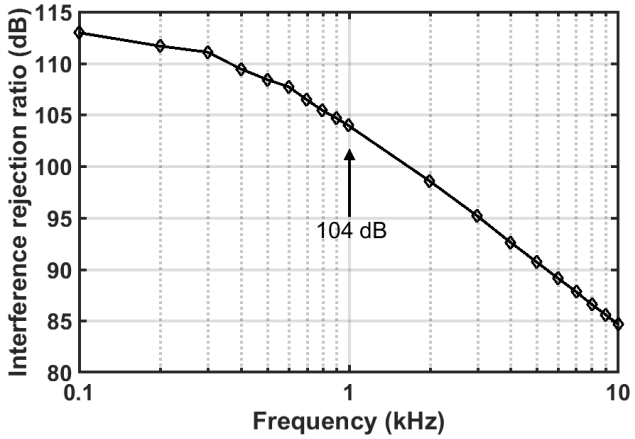

Figure 4.5 Interference rejection ratio.

In table 4.1, the performance of the CDC is summarized and compared with the state-of-the-art. It achieves comparable resolution FoM while offering floating target sensing capability with excellent interference immunity.

Table 4.1 Performance summary and comparison table.

	This work	**[3]**	**[4]**	**[5]**	**[6]**
Technology (µm)	0.18	PCB-level	0.35	0.35	0.18
Method	ΔΣ	CVC + ADC	PM	ΔΣ	PM
Floating sensing	Yes	Yes	No	No	No
Input range (pF)	0~10	0~10	0~6.8	8.4~11.6	0~8
T_{conv} (ms)	1	0.1	7.6	0.02	6.86
Power (mW)	0.36	121	0.21	15	0.014
Resolution (bits)	15	15	15	15.3	14.6
FoM (pJ/c-s)	11	369	49	7.4	3.9

.

Chapter 5 Conclusion and Future Work

The thesis objective was to develop an on-chip capacitance-to-digital converter (CDC) for position sensing with an electrically floating target. The main focus of our work in this context was designing an efficient sensor interface in terms of area and power consumption. To do so, a new interface that directly uses the sensor capacitances as the sampling capacitances of a delta-sigma ADC was proposed. Compared to previous design [7], this helps to simplify the analog portion of the design which in turn reduces the area and the power consumption.

While this thesis has demonstrated the world's first on-chip capacitance-to-digital converter (CDC) for position sensing with electrically floating target, due to time constraints of a master thesis period, some opportunities for improvement have been left for the future. These are listed below.

1. The developed interface can be tested with an *actual* sensor intended for position sensing of floating target. This help to demonstrate the position sensing capability and to evaluate the accuracy and resolution of the system in term of distance.
2. Due to the presence of large noise and interference on the floating target, the mismatch between the sensor capacitance pair can negatively impact sensor resolution and accuracy. Even better performance can be achieved if sensor capacitance pair are well matched.
3. A new package for the system can be used in which the wire routing from the sensor capacitances to the ADC input are improved. For instance, the length of wire routing can be minimized and well shielded. This helps to minimize the value of the parasitic capacitance and effect of the external interference.

4. In order to further improve the power-efficiency of the sensor interface, current-reused topology can be used for the integrator's OTA [10]. Making both PMOS and NMOS input pair share the same bias current, this topology helps to increase the OTA transconductance g_m by 2x for a given bias current.

Chapter 6 Acknowledgment

First of all, I would like to express my deep gratitude to my supervisor, Prof. Stoyan Nihtianov. I appreciate all his contributions, ideas, and support, without whom finalizing of this work would have been impossible.

My appreciation extends to my committee members for their time, comments and discussions.

I give my sincere thanks to Zu-yao and Lukasz for their patience, strong support, and commitment. Thanks to Atef for all his support and helps during my tape-out. I would also like to thank Joyce for all the administrative support.

Many thanks go to Hui, who helped me with doing measurements, writing conference papers, and whose comments have been instrumental in my work.

I wish to thank all my friend and colleagues here at EI lab. My group members, Hui, Vikram and Johan for design reviews, rehearsals and interesting discussions that we had together. Further, My officemates, Yikun, Michele, Said, Arjan, Costantino, Douwe, Sining, Long and Weichen for all the technical and non-technical discussions.

I also would like to thank my dearest friend and classmate, Magda, she is the best friend that anybody could hope for.

Good friends are hard to find but I was fortunate to have such great friends here in Netherlands that are true and real: Somi, Negin, Mina, Haleh, Bahar, Maryam, Hanieh, Bahareh, Mohi, Morteza, Mohsen, Milad, and Masoud. You have had a terrific impact on my life.

I would like to express my deepest gratitude to my beloved family. To my awesome mom who has always been there any time that I have needed her. She taught me how to love, how

to fight and how to believe in myself. To my gorgeous Dad, Who always told me educating myself will get me anywhere I wish for. My Dad is my spiritual guides and my hero. I am so very grateful for every single thing that my parents have done for me and I cannot imagine my life without them. My cute sister, Elmira, she is to live what salt is to food, water is to fish and night is to stars, irreplaceable. Love you so much, sis.

Last but not least, I would like to express my sincere gratitude to my husband, Saleh. You were not only my best friend but also my best teacher who taught me to never give up. Honestly, I would not be here if you weren't there for me. Words cannot express my feelings, nor my thanks. I also wish to thank your lovely family for their kindness and encouragement.

Samira,

TUDelft

02-03-2017

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