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Research on Design Optimization of Temperature and Current Sharing Uniformity of SiC HybridPACK Drive Power Modules Under Multi-Physics Coupling

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***Abstract*—The rapid expansion of the electric vehicle industry has accelerated the adoption of Silicon Carbide (SiC) HybridPACK Drive (HPD) power modules to meet the escalating demand for high-efficiency power conversion. However, under high power density conditions, these modules encounter significant reliability challenges stemming from intricate multi-physics interactions across electrical, thermal, and mechanical domains. This study employs multi-physics simulations to systematically evaluate the synergistic effects of several critical design variables—including pin-fin geometry and gradient arrangements, die-attach materials and processes, and chip interconnection structures—on the module's temperature and current-sharing uniformity. Based on the simulation results, an optimal configuration was identified for sample fabrication and experimental validation. By correlating empirical measurements with simulation data, this research elucidates the configurations that provide superior performance under constant heat flux conditions. The findings establish a robust theoretical and practical framework for enhancing the reliability and operational consistency of SiC HPD power modules through multi-factor comprehensive optimization.**

Keywords—SiC HPD Power Module; Temperature Uniformity Performance; Current Sharing Performance; Multi-Physics Simulation; Design Variables

I. INTRODUCTION (*HEADING 1*)

SiC HPD power modules have emerged as a cornerstone for high-performance automotive and industrial power conversion, exploiting the intrinsic advantages of wide-bandgap materials to achieve unprecedented efficiency and power density. However, their reliability in demanding service environments remains a significant concern, as performance and operational longevity are strictly dictated by complex electro-thermal-mechanical multi-physics coupling effects[1]-[3]. Within these intricate operating conditions, current-sharing consistency and temperature uniformity are recognized as the primary benchmarks for packaging integrity[4]-[7]. A uniform thermal field is indispensable for mitigating thermo-mechanical stress induced by the Coefficient of Thermal Expansion (CTE) mismatch between heterogeneous materials, thereby forestalling critical failure modes such as solder fatigue cracking and bond-wire lift-off[1]. Simultaneously, optimized current sharing among parallelized chips suppresses current crowding and the subsequent formation of localized hot spots, which are the primary catalysts for accelerated device degradation[8].

To address these reliability challenges, substantial research has focused on thermal management optimization and innovative electrical interconnections. In the domain of thermal management, investigations into pin-fin architectures have demonstrated that streamlined (water-drop) designs significantly reduce hydraulic resistance and enhance heat transfer coefficients compared to conventional circular geometries, effectively lowering junction temperatures and overall thermal resistance[9]-[12]. Regarding die-attach technologies, traditional tin-based solders are increasingly being superseded by advanced sintering processes due to their inherent limitations in high-temperature stability and thermal conductivity. Specifically, silver and copper sintering technologies—offering thermal conductivities three to five times higher than those of standard solders—provide superior thermo-mechanical resilience and substantially extend module service life[1]-[7]. From an electrical perspective, the transition from traditional aluminum wire bonding to copper clip (Cu-Clip) interconnection represents a major technological leap. Cu-clip bonding not only mitigates parasitic inductance and resistance while boosting current-carrying capacity but also alleviates thermo-mechanical stress through improved CTE matching with the chip. Crucially, this

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technology enhances current-sharing consistency by minimizing electrical parameter disparities between parallel branches [13][14].

Notwithstanding these isolated technical advancements, a systematic analysis of how disparate design variables interact within a multi-physics framework remains underserved in current literature [15]. The primary objective of this study is to elucidate the influence of multiple design variables on the temperature and current-sharing uniformity of SiC HPD modules through an integrated approach of simulation and experimental validation. We employ a comprehensive simulation suite—comprising Icepak, Simplorer, and Q3D—to analyze the underlying mechanisms of key factors, including pin-fin geometry/arrangement, die-attach materials, and interconnection architectures. Double-pulse simulations are conducted in Simplorer to evaluate dynamic current-sharing performance. Based on these insights, an optimal configuration is selected for fabrication and subjected to constant heat flux testing to assess its real-world performance. Finally, the correlation between simulation predictions and empirical results is verified to establish a robust design methodology.

II. Multi-Physics Simulation of SiC HPD Power Modules

A. Establishment of Simulation Model

The simulation framework is grounded on a commercial, mass-produced SiC HPD power module. The detailed geometric configuration and critical dimensions of the baseline module are provided in Figure 2.1 (a).

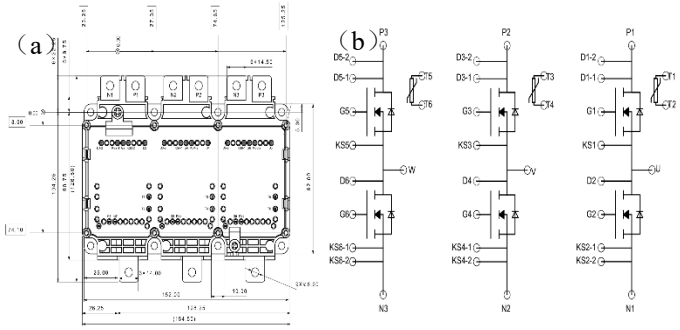


Figure 2.1 (a) Module design drawing with dimension markings (b) Topological circuit diagram of the module

Multi-physics coupling serves as the methodological cornerstone for evaluating the operational performance of SiC HPD modules. This approach characterizes the intricate interplay between electrical, thermal, and mechanical domains through rigorous mathematical modeling. In the electrical domain, the analysis focuses on current distribution, voltage drop, and parasitic inductance—parameters that directly dictate the module's switching dynamics and conversion efficiency. Concurrently, the thermal analysis examines heat generation and dissipation pathways, where the chip's power loss acts as the primary heat source. The topological circuit of the module, illustrated in Figure 2.1 (b), reveals a three-phase architecture (U, V, and W) where each phase comprises two units (H and L, e.g., UH and UL). Each unit further integrates four parallelized SiC chips. To capture these multi-physics interactions, a co-simulation environment leveraging Ansys Icepak, Simplorer, and Q3D is employed. The resulting simulation model, reflecting the actual physical dimensions and circuit topology, is shown in Figure 2.2.

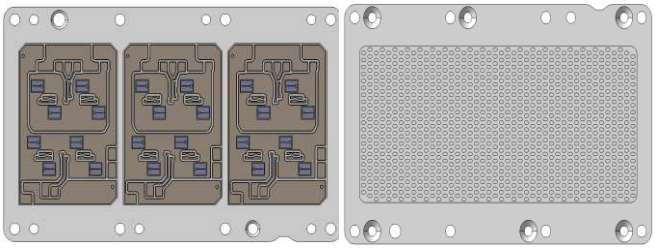


Figure 2.2 Front and back views of the module simulation model

B. Influence of Pin-Fin Geometry and Arrangement

The architecture of the pin-fin array is a decisive factor in the module's convective heat transfer efficiency. In this study, conventional circular pin-fins are replaced with streamlined, water-drop geometries to minimize coolant flow resistance and suppress boundary layer separation. This modification yields a more uniform flow velocity profile and enhances the volumetric flow rate within the cold plate, thereby boosting overall thermal dissipation. Furthermore, the pin-fin spacing across the three phases is optimized via a gradient-density arrangement to compensate for uneven coolant distribution and mitigate localized thermal accumulation.

To evaluate the impact of geometry, both circular and water-drop pin-fins were simulated under identical boundary conditions. Figure 2.3 presents the resulting temperature contours of the cold plate. The water-drop configuration exhibits a significantly more homogenous temperature field and a marked reduction in peak temperature, validating its superior thermal performance.

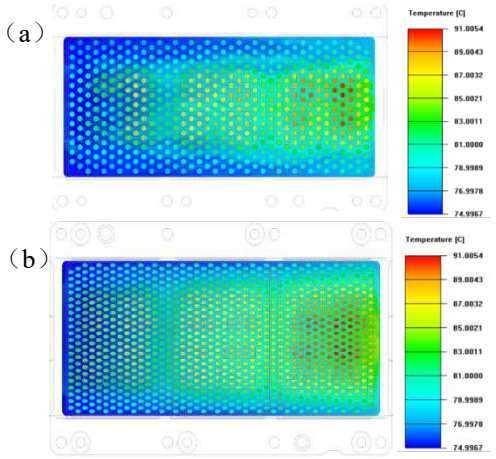


Figure 2.3 Cold plate temperature distribution contours (a) Circular pin-fins (b) Water-drop shaped pin-fins

Regarding the arrangement, three distinct density profiles were investigated. Module A has uniform pin-fin density for all three phases with a spacing of 1.2 (the value represents the spacing between pin-fins; the smaller the value, the better the heat dissipation effect). Module B has three-phase pin-fin spacing of 1.2 for U-phase, 1.0 for V-phase, and 0.8 for W-phase. Module C has three-phase pin-fin spacing of 1.2 for U-phase, 0.9 for V-phase, and 0.72 for W-phase. Icepak is used to simulate the three modules under the same operating conditions to obtain the temperature distribution contours under working conditions. As shown in Figure 2.4, the

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maximum chip temperature (HT) of the three phases in Module A is 137.759°C, the maximum temperature of Module B is 133.788°C, which is 2.88% lower than that of Module A, and the maximum temperature of Module C is 133.019°C, which is 3.44% optimized compared with Module A and 0.57% optimized compared with Module B.

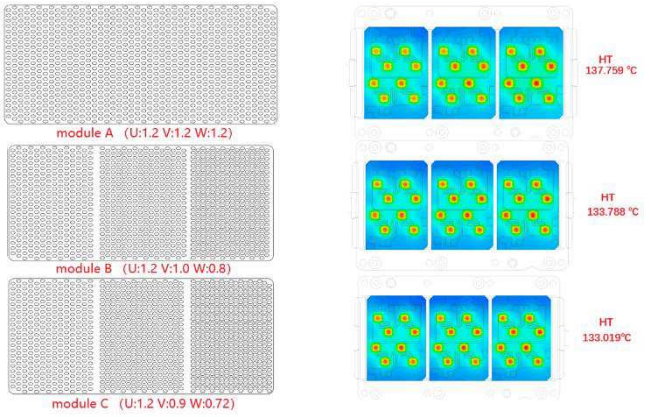


Figure 2.4 Front temperature distribution contours of the three modules

To further elucidate these trends, a comparative analysis was conducted including a circular pin-fin reference (Module R). Steady-state and transient thermal resistance data were extracted for each of the six units. As illustrated in Figure 2.5, the water-drop geometry consistently outperforms the circular design. Moreover, the transition from uniform to gradient spacing significantly reduces individual unit thermal resistance and harmonizes its distribution. Module C demonstrates the lowest thermal resistance and the highest degree of unit-to-unit consistency, representing the optimal configuration for thermal management

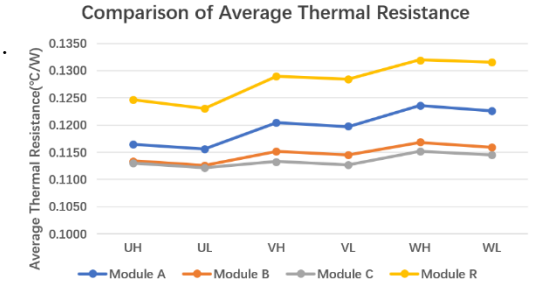


Figure 2.5 Comparison of thermal resistance of six units among Module A, B, C and R

C. *Influence of Die Attach Material and Process*

The die-attach interface is pivotal in determining the thermal and electrical integrity of SiC HPD modules. Traditional tin-based solders, limited by their relatively low thermal conductivity ($\approx 30\mathrm{W/(m\cdot K)}$), often introduce significant thermal barriers that elevate junction temperatures. Conversely, advanced silver or copper sintering creates a dense metallic network with thermal conductivities 3 to 5 times higher than those of solders, alongside lower electrical resistivity.

In this study, Module D (solder bonding) was compared against Module C (silver sintering), keeping all other design variables constant. Figure 2.6 shows that Module D reaches a peak temperature of 134.917° C, exceeding that of Module C. The comparative thermal resistance data in Figure 2.7 further confirms that the sintering process provides a superior thermal pathway, significantly enhancing the module's heat conduction efficiency.

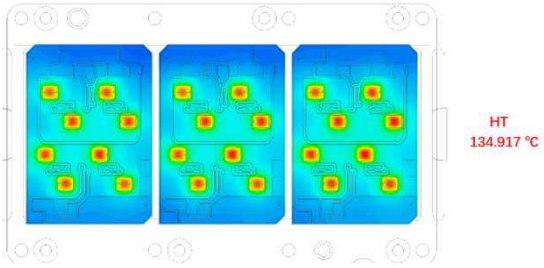


Figure 2.6 Front temperature distribution contour of Module D

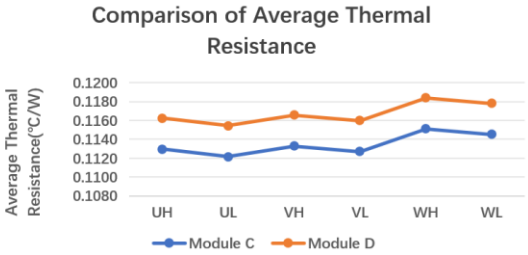


Figure 2.7 Comparison of thermal resistance of six units between Module C and D

D. *Influence of Chip Interconnection Structure Design*

The internal interconnect architecture fundamentally governs the module's current-sharing efficiency. Compared to conventional aluminum wire bonding, copper clip (Cu-Clip) interconnection enhances current sharing by improving the impedance consistency of parallel branches and minimizing junction temperature disparities.

To quantify this, Module E (aluminum wire bonding) was compared with Module C (Cu-Clip) via double-pulse simulations in Simplorer (850 V DC bus, 600 A load [7]). The evaluation metrics focused on current and loss imbalance, defined as:

$$Imbalance = \frac{I_{Dmax} - I_{Dmin}}{I_{Davg}} \times 100\%$$

Where I_{Dmax} is the maximum current of each chip, I_{Dmin} is the minimum current of each chip, and I_{Davg} is the average of the maximum and minimum values). The results, summarized in Figure 2.8, demonstrate that Cu-Clip technology significantly stabilizes current distribution. During the second turn-on transient, the current imbalance for Module C (UH: 24.79% and UL: 25.75%) is substantially lower than that of Module E (UH: 53.08% and UL: 51.34%). Similarly, the turn-off imbalance is reduced from 0.48%-0.58% (Module E) to 0.20%-0.29% (Module C). Furthermore, Figure 2.9 illustrates that the loss inconsistency among parallel chips in the UH unit is curtailed from over 40% in Module E to approximately 17.7% in Module C, highlighting the decisive advantage of Cu-Clip structures in ensuring operational reliability

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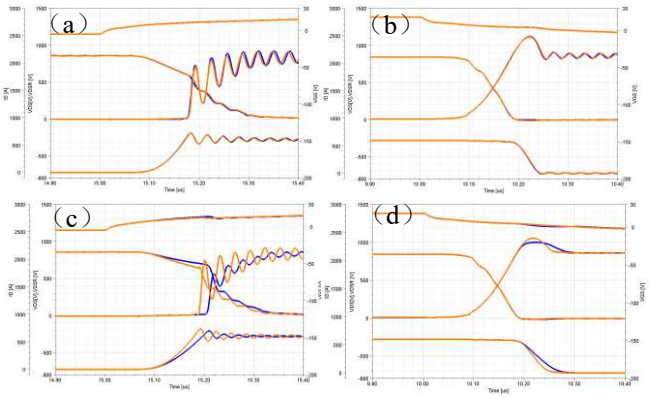


Figure 2.8 (a) Turn-on waveform of Module C (b) Turn-off waveform of Module C (c) Turn-on waveform of Module E (d) Turn-off waveform of Module E

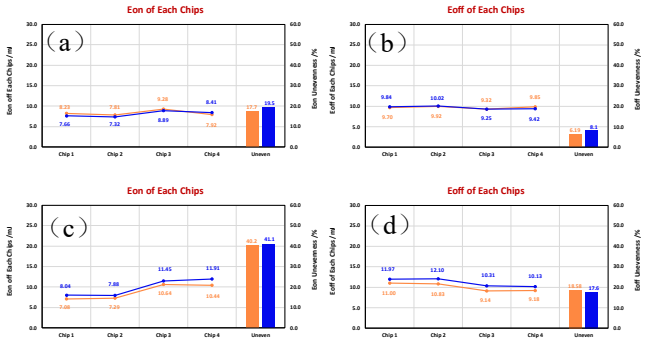


Figure 2.9 (a) Turn-on loss of Module C (b) Turn-off loss of Module C (c) Turn-on loss of Module E (d) Turn-off loss of Module E

III. Experimental Verification

A. Experimental Sample Fabrication

Guided by the multi-physics simulation insights, Module A and the optimized Module C—featuring streamlined water-drop pin-fins, a variable-density array, silver sintering, and copper clip interconnections—were selected for prototype fabrication. Comparing the empirical performance of these physical modules against computational predictions serves to verify the fidelity of the simulation models.

The assembly of the SiC modules followed a rigorous, standardized process flow [16]. Initially, a thorough compliance inspection was performed on core raw materials, including the DBC substrates, SiC power chips, Ag paste, and package housings. Following material validation, Ag paste was screen-printed onto the preset DBC pads and subjected to pre-curing to ensure morphological stability; subsequently, the SiC chips were precisely attached and sintered to establish high-strength, high-conductivity thermal pathways, with plasma cleaning employed throughout to eliminate surface oxides and micro-contaminants. The electrical architecture was then established via wire bonding between the chip electrodes and DBC pins, followed by the integration of auxiliary components—such as resistors and capacitors—through a meticulous sequence of vacuum reflow soldering and intermediate DBC testing to guarantee structural integrity. Structural encapsulation was achieved via laser welding of key components, reinforced by adhesive curing for housing-to-substrate bonding and ultrasonic welding for external pin connectivity. To finalize the assembly, internal insulation and mechanical stability were enhanced through epoxy potting and post-curing treatment, concluding with cover plate mounting to produce the completed SiC HPD modules. The resulting physical prototypes are illustrated in Figure 3.1.

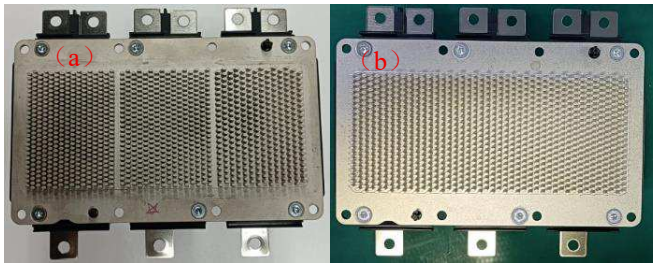


Figure 3.1 (a) Fabricated sample of Module C (b) Fabricated sample of Module A

B. Temperature Uniformity Performance Test

Thermal characterization utilized a dual-monitoring approach, combining K-type thermocouples and infrared thermal imaging to comprehensively map the module's temperature distribution across varied operating regimes. Specifically, multiple thermocouples were strategically positioned at critical junctions—including the SiC chip surfaces, the DBC substrate centers, and the base plate edges—for real-time localized monitoring. Simultaneously, an infrared thermal imager recorded broader surface temperature profiles to reveal heat concentration zones and diffusion patterns. Bench testing was executed under a constant heat flux density of 800 V and 400 A, with a fixed coolant flow rate of 8 L/min and an ambient temperature maintained at 25°C. Data were acquired at a frequency of 50 Hz over a continuous 30-minute duration to ensure the system reached a stable thermal equilibrium. The detailed test bench configuration is shown in Figure 3.2.

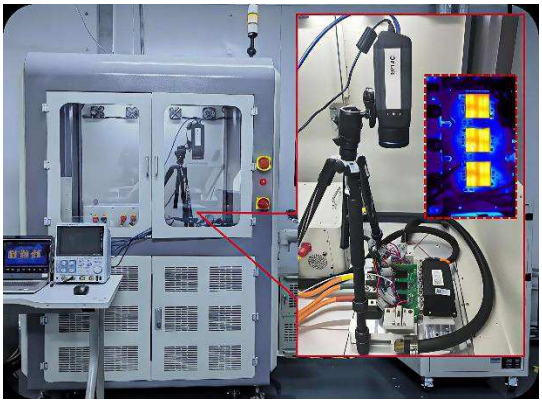


Figure 3.2 Test bench setup

Thermal mapping of the baseline Module A (Figure 3.3) reveals a maximum junction temperature of 174.68°C at the V-phase low-side bridge arm, contrasted with a minimum of 149.52°C at the U-phase. The resulting overall temperature differential of 25.16°C highlights the significant thermal non-uniformity inherent in conventional uniform-density pin-fin arrangements.

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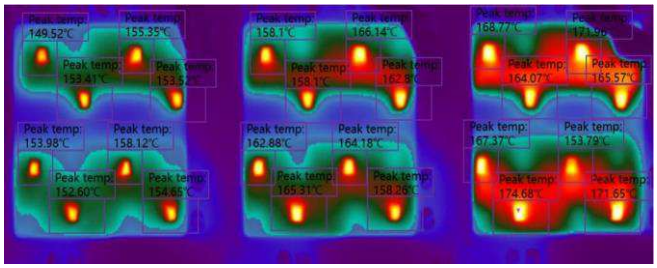


Figure 3.3 Thermal image of Module A from the bench test

In contrast, the optimized Module C (Figure 3.4) demonstrated markedly enhanced thermal performance during the bench test. The maximum junction temperature was curtailed to 172.53°C (located at the U-phase low-side arm), while the minimum temperature rose to 154.73°C at the U-phase high-side. This resulted in an overall module temperature difference of only 17.8°C. These results confirm that the variable-density pin-fin configuration provides a decisive advantage in temperature homogenization compared to traditional uniform designs.

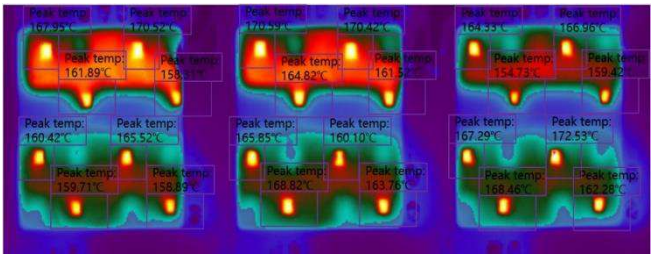


Figure 3.4 Thermal image of the optimal Module C from the bench test

IV. Results and Analysis

A holistic comparison between multi-physics simulation outcomes and experimental data for Module C reveals a high degree of correlation in terms of peak junction temperature, thermal uniformity, and current-sharing trends. However, minor quantitative discrepancies exist, which merit detailed analytical discussion.

Regarding peak junction temperatures, both empirical measurements and numerical simulations confirm that the optimized Module C outperforms the baseline Module A. Specifically, the maximum junction temperature was reduced by 1.3% in the bench tests and 3.4% in the simulation environment. While the overall trend validates the reliability of the simulation framework, the absolute temperatures recorded during physical testing were consistently higher than those predicted by the model. This thermal offset is likely attributable to the idealized boundary conditions assumed in the simulation—such as perfect interface contacts—and the stochastic dispersion of process parameters during actual fabrication, such as slight variations in sintering layer thickness or voiding.

In terms of thermal distribution, the overall temperature differential across Module C was significantly smaller than that of Module A in both simulated and experimental scenarios. The observed variation ranges closely align with the simulation's predictions, corroborating that the variable-density pin-fin arrangement effectively optimizes coolant flow distribution and mitigates localized heat accumulation. This consistency underscores the efficacy of gradient-density architectures in enhancing the thermal homogeneity of SiC HPD modules.

Characterizing the current distribution of individual chips during high-speed operation remains a significant metrological challenge due to the high-density integration of the HPD module, the gap-free sintered interfaces, and the absence of internal test points. Consequently, the evaluation of current-sharing performance relies primarily on validated simulation data. A comparison between Module C (Cu-clip) and Module E (aluminum wire bonding) demonstrates that copper clip interconnections yield a substantial improvement in current-sharing consistency.

In summary, the steady-state and transient simulations at room temperature effectively predict the core performance trends and operational logic of the module, demonstrating robust alignment with the measured empirical laws.

V. Conclusion

This research systematically elucidated the influence of critical design variables on the temperature and current-sharing uniformity of SiC HPD power modules through an integrated framework of multi-physics simulation and experimental validation. The investigation demonstrates that pin-fin geometry and arrangement, die-attach materials, and interconnection architectures exert a profound synergistic impact on the module's overall electro-thermal performance. Specifically, the variable-density pin-fin configuration optimizes the thermal dissipation profile. Concurrently, the transition from traditional soldering to advanced sintering significantly boosts heat conduction efficiency, effectively lowering peak junction temperatures and enhancing thermal homogeneity. Furthermore, the implementation of copper clip interconnections substantially improves intra-unit current-sharing consistency compared to conventional aluminum wire bonding, a benefit further bolstered by improved module-level temperature uniformity.

In the experimental verification phase, prototypes based on the optimized simulation configuration were fabricated and subjected to rigorous testing. Empirical data confirm that the optimized design achieves an approximately 30% enhancement in junction temperature uniformity among units relative to traditional configurations. Complementary simulation results indicate a 28% improvement in current-sharing capability for the optimal scheme. These findings underscore the efficacy of multi-physics-driven optimization in elevating the operational reliability and performance of SiC HPD power modules. In summary, this paper clarifies the underlying mechanisms by which diverse design variables govern module uniformity and proposes a robust, multi-factor optimization methodology to advance the design and reliability of high-performance power electronics packaging.

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