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A Fully Synthesizable Fractional-*N* MDLL With Zero-Order Interpolation-Based DTC Nonlinearity Calibration and Two-Step Hybrid Phase Offset Calibration

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***Abstract*— In this paper, a fully-synthesizable digital-to-time (DTC)-based fractional-*N* multiplying delay-locked loop (MDLL) is presented. Noise and linearity of synthesizable DTCs are analyzed, and a two-stage synthesizable DTC is proposed in which a path-selection DTC is used as the coarse stage and a variable-slope DTC is used as the fine stage. To calibrate the DTC nonlinearity, a highly robust zero-order interpolation based nonlinearity calibration is proposed. Besides, the static phase offsets (SPO) between bang-bang phase detector (BBPD) and multiplexer (MUX) are calibrated by a proposed hybrid analog/digital phase offset calibration, while the dynamic phase offsets (DPO) are removed by a proposed complementary switching scheme. The co-design of the analog circuits and digital calibrations enable excellent jitter and spur performance. The MDLL achieves 0.70 and 0.48 ps root-mean-square (RMS) jitter in fractional-*N* and integer-*N* modes, respectively. The fractional spur is less than −59.0 dBc, and the reference spur is −64.5 dBc. The power consumptions are 1.85 mW and 1.22 mW, corresponding to figures of merit (FOM) of −240.4 dB and −245.5 dB.**

***Index Terms*— Multiplying delay-locked loop (MDLL), phase-locked loop (PLL), injection locking, fully-synthesizable, digital-to-time converter (DTC), nonlinearity calibration, variable-slope DTC, path-selection DTC, phase offset, bang-bang phase detector (BBPD).**

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I. Introduction

As CMOS processes reach sub-20nm scales, various challenges complicate the analog/mixed-signal circuit design, such as low supply, high variations and limited model accuracy [1]. Therefore fully-synthesizable designs are becoming more attractive. Significant efforts have been devoted to realizing fully synthesizable PLLs [2]–[12], data converters [13], and wireless transceivers [14]–[16].

Fig. 1(a) shows the design and implementation flow of a fully-synthesizable MDLL as a "soft" intellectual property (IP). Digitally designed analog circuits such as digitally controlled oscillator (DCO), digital-to-time converter (DTC) are designed with standard cells and are described in a gate-level netlist. Whereas the digital control logic is described in register-transfer level (RTL) hardware description language (HDL) code. The physical implementation is carried out using the standard digital place and route (P&R) tools. Such a flow eliminates the burden of manual layout design with complex design rules, which is especially problematic in sub-20 nm FinFET processes. However, high systemic mismatches from P&R have severely constrained the fully-synthesizable designs, making their performance inferior to their manually designed counterparts. While techniques such as relative placement [17] and region constraints can be used to reduce the P&R systemic mismatches, as shown in Fig. 1(b), the mismatches from routing cannot be eliminated. Therefore, new circuit topologies that are friendly for digital synthesis must be devised. Besides, efficient calibrations are required to mitigate the non-idealities in synthesizable circuits.

In this paper, a fully-synthesizable fractional-*N* DTC-based MDLL is presented. A synthesizable DTC architecture is proposed, with a thorough analysis and optimization of jitter, power, and nonlinearity. A robust digital nonlinearity calibration that is suitable for the synthesizable DTC is proposed. Besides, to reduce the reference spurs, hybrid analog-digital calibrations are proposed to reduce both static and dynamic phase offsets to levels sufficiently below thermal noise floor.

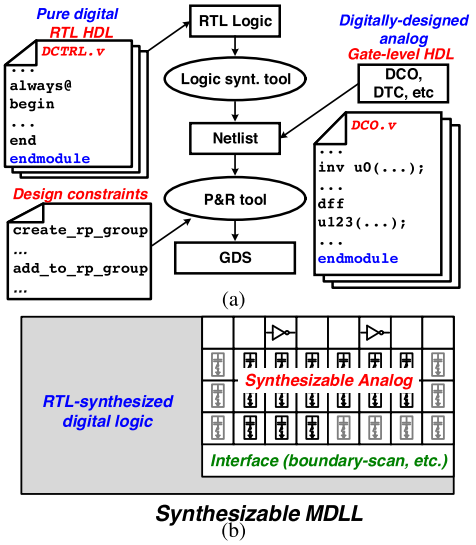

Fig. 1. Design of a fully-synthesizable MDLL, (a) digital compatible design process, (b) synthesized layout with relative placement and region constraints.

The remainder of this paper is organized as follows. Section II presents the system overview of the proposed fractional-*N* MDLL. Design considerations and optimizations of the fully-synthesizable DTC are explained in Section III, and the proposed DTC nonlinearity calibration is presented in Section IV. Phase offset calibration in MDLL is presented in Section V. Detailed circuit implementations are explained in Section VI, and measurement results are presented and analyzed in Section VII. Section VIII concludes the paper.

II. Fully-Synthesizable MDLL System Architecture

A variety of injection-locked PLLs (IL-PLLs) and MDLLs have been developed in recent years [3], [5], [7]–[9], [11], [12], [18]–[32]. Due to the high bandwidth offered by the IL-PLLs/MDLLs, excellent jitter performance has been achieved. However, inherently ILPLLs/MDLLs are limited to integer-*N* operation, whereas in many applications fractional-*N* operation is desired. To extend injection locking to fractional-*N* operation, various architectures have been proposed [7], [18], [33]. In this study, a DTC-based MDLL architecture is adopted. The DTC is placed on the reference path to introduce a time-varying delay to the injection signal, thereby enabling the realization of fractional-*N* injection locking.

The system diagram of the proposed fractional-*N* MDLL is shown in Fig. 2(a). The upper part contains the synthesizable timing generation blocks, which consists of a DTC, an injection edge and window generator, a DCO, a symmetrical MUX, and a sub-sampling (SS) BBPD. However, the MDLL has various non-idealities which degrade the performance. Therefore, extensive digital background calibrations are integrated, which are shown in the bottom part of Fig. 2(a). First of all, the DCO frequency and phase error are calibrated by the frequency lock loop (FLL) and PLL to ensure correct frequency and phase alignment. Besides, the DTC gain, which is defined as the output delay versus input digital control code, is calibrated by a least-mean-square (LMS) based gain calibration. The DTC nonlinearity, which causes in-band fractional spurs, is calibrated with a proposed zero-order interpolation based nonlinearity calibration. Moreover, the phase offsets between the MUX and BBPD cause large reference spurs and needed to

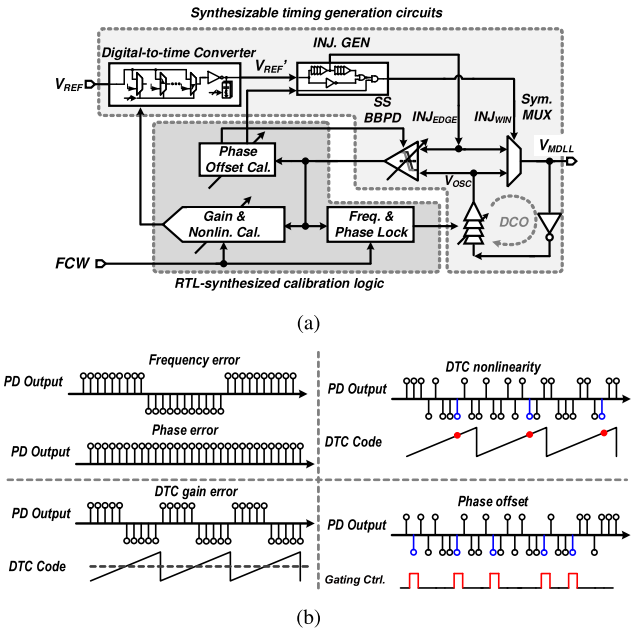

Fig. 2. (a) System diagram of proposed fully-synthesizable DTC-based fractional-*N* MDLL, and (b) conceptual waveform of simultaneous calibration operations.

be minimized. The phase offsets include both static ones which are caused by systemic mismatch from P&R and dynamic ones which are caused by the time-varying injection control signal. The static phase offsets are calibrated by a two-step analog/digital hybrid offset calibration schemes, in which the offset can be calibrated with arbitrarily fine resolution. For the dynamic phase offsets, a complementary-switching MUX/BBPD is proposed.

All of the calibrations utilize the same BBPD output, which ensures the calibration results are consistent and free of mismatch. The system nonidealities, such as frequency/phase error, DTC gain error and nonlinearity, and phase offset exhibit different statistic distribution, and are correlative to different control signal sequences, as shown in Fig. 2(b). By setting independent calibration control signal sequences and proper bandwidths, all the calibration could operate simultaneously in background.

III. Multi-Stage Fully-Synthesizable DTC

DTCs have found extensive usage in high performance PLLs. Many different DTC implementations have been devised, such as constant-slope (CS) [34]–[38], variable-slope (VS) [39]–[42], and path-selection (PS) based topologies [10], [19], [43], [44]. Considering the feasibility of standard cell implementation, VS and PS DTCs are preferred. However, these two DTC architectures have different noise and nonlinearity characteristics, which merit careful examinations to find the optimal architecture.

A. Jitter-Power Analysis

The jitter variance $J_{\mathrm{DTC,VS}}$ (unit is s^2) and power $P_{\mathrm{DTC,VS}}$ (unit is mW) product of a VS DTC can be expressed as [45]

$$J_{\mathrm{DTC,VS}} \cdot P_{\mathrm{DTC,VS}} = 4kT \cdot [1 + \frac{2\gamma V_{\mathrm{DD}}}{V_{\mathrm{OV,N}}}] \cdot f_{\mathrm{REF}} \cdot t^2_{\mathrm{TOT,VS}} = C \cdot t^2_{\mathrm{TOT,VS}} \quad (1)$$

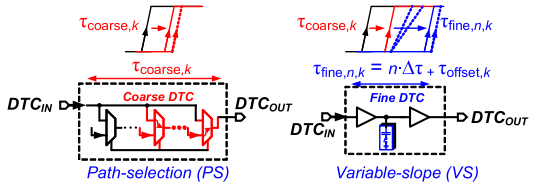

Fig. 3. Synthesizable path-selection DTC and variable-slope DTC.

where k is the Boltzmann constant, T is the temperature, $t_{\mathrm{TOT,VS}}$ is the total delay of VS DTC, f_{REF} is the reference frequency. The γ is the excessive noise factor, V_{DD} is the supply voltage, $V_{\mathrm{OV,N}}$ the over-drive voltage of NMOS transistor, and C is $4kT\cdot[1+\frac{2\gamma V_{\mathrm{DD}}}{V_{\mathrm{OV,N}}}]\cdot f_{\mathrm{REF}}$. However, the full scale tunable range of VS DTC $t_{\mathrm{FS,VS}}$ is a fraction of the total delay $t_{\mathrm{TOT,VS}}$. Effects such as the limited ON/OFF capacitance ratio of digital varactors causes considerable fixed delay offset. For synthesizable not-and (NAND)-3 based digital varactors, the ON/OFF ratio $k_{\mathrm{ON/OFF}}$ is approximately 3/2 [11], thus

$$J_{\mathrm{DTC,VS}}\cdot P_{\mathrm{DTC,VS}} = C\cdot(k_{\mathrm{var}}\cdot t_{\mathrm{FS,VS}})^2 \tag{2}$$

$$k_{var} = \frac{t_{\mathrm{TOT,VS}}}{t_{\mathrm{FS,VS}}} = \frac{k_{\mathrm{ON/OFF}}}{k_{\mathrm{ON/OFF}}-1}\approx 3 \tag{3}$$

where k_{var} is ratio between t_{TOT} and t_{FS}.

On the other hand, PS DTCs tune delay by selecting N delay cells, and the delay offset is negligible, therefore the full scale tunable range $t_{\mathrm{FS,PS}}$ is approximately equal to total delay $t_{\mathrm{TOT,PS}}$. Assuming the noise of each delay cell is independent, the jitter-power product of PS DTC can be expressed as

$$\begin{aligned} J_{\mathrm{DTC,PS}}\cdot P_{\mathrm{DTC,PS}} &= (N\cdot J_{\mathrm{DTC,PS,0}})\cdot(N\cdot P_{\mathrm{DTC,PS,0}}) \\ &= N^2\cdot C\cdot(\frac{t_{\mathrm{FS,PS}}}{N})^2 = C\cdot t_{\mathrm{FS,PS}}^2 \end{aligned} \tag{4}$$

Thus, the jitter-power product of a VS DTC is k_{var}^2 times worse than a PS DTC.

However, the PS DTC resolution $t_{\mathrm{RES,PS}}$ is larger than 20 ps in a 65 nm CMOS process. Therefore, a two-stage PS + VS DTC is proposed, as shown in Fig. 3. The proposed two-stage DTC provides a better jitter/power tradeoff. For a given delay range t_{FS} and jitter J_{DTC}, the power consumption of a one-stage VS DTC can be expressed as

$$P_{\mathrm{DTC,one-stage}} = \frac{C\cdot(k_{\mathrm{var}}\cdot t_{\mathrm{FS}})^2}{J_{\mathrm{DTC}}} \tag{5}$$

On the other hand, assuming the VS DTC range $t_{\mathrm{FS,VS}}$ equals to $n\cdot t_{\mathrm{RES,PS}}$, in which n is a over-design factor larger than 1 to account for margins for PVT and nonlinearity calibration. The PS DTC and VS DTC contribute $(1-k_{\mathrm{jitter}})\cdot J_{\mathrm{DTC}}$ and $k_{\mathrm{jitter}}\cdot J_{\mathrm{DTC}}$ respectively, in which k_{jitter} is the jitter contribution ratio. The power consumption of proposed two-stage DTC is

$$\begin{aligned} P_{\mathrm{DTC,two-stage}} &= P_{\mathrm{DTC,PS}} + P_{\mathrm{DTC,VS}} \\ &= \frac{1}{1-k_{\mathrm{jitter}}}\cdot\frac{C\cdot t_{\mathrm{FS}}^2}{J_{\mathrm{DTC}}} + \frac{1}{k_{\mathrm{jitter}}} \\ &\quad\cdot\frac{C\cdot(k_{\mathrm{var}}\cdot n\cdot t_{\mathrm{RES,PS}})^2}{J_{\mathrm{DTC}}} \end{aligned} \tag{6}$$

The optimal $k_{\mathrm{jitter,opt}}$ for the minimum power consumption $P_{\mathrm{DTC,two-stage,min}}$ can be expressed as

$$k_{\mathrm{jitter,opt}} = \frac{1}{1+\frac{t_{\mathrm{FS}}}{k_{\mathrm{var}}\cdot n\cdot t_{\mathrm{RES,PS}}}} \tag{7}$$

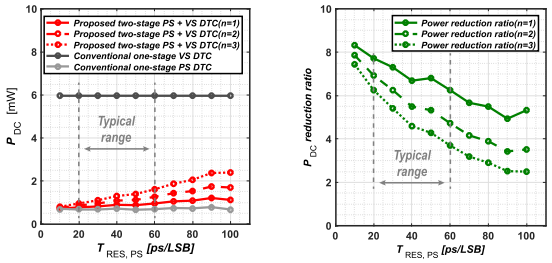

Fig. 4. Power consumption (a) and ratio (b) of one-stage VS DTC and the proposed two-stage PS-VS DTC at different $T_{\mathrm{RES,PS}}$ and over-design factor n. The t_{FS} is 1 ns, J_{DTC} is $(0.1\,\mathrm{ps})^2$, and k_{var} is 3.

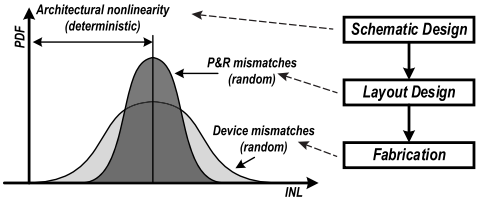

Fig. 5. Conceptual composition of DTC nonlinearities.

$$P_{\mathrm{DTC,two-stage,min}} = \frac{C\cdot t_{\mathrm{FS}}^2}{J_{\mathrm{DTC}}}\cdot(1+\frac{k_{\mathrm{var}}\cdot n\cdot t_{\mathrm{RES,PS}}}{t_{\mathrm{FS}}})^2 \tag{8}$$

$$\frac{P_{\mathrm{DTC,two-stage,min}}}{P_{\mathrm{DTC,one-stage}}} = (\frac{1}{k_{\mathrm{var}}}+\frac{n\cdot t_{\mathrm{RES,PS}}}{t_{\mathrm{FS}}})^2 \tag{9}$$

Since k_{var} is determined by technology, and t_{FS} is determined by MDLL system architecture, only $t_{\mathrm{RES,PS}}$ and n are available for optimization. The relationship between power consumption and $t_{\mathrm{RES,PS}}$ with different n is shown in Fig. 4. The proposed two-stage DTC reduces the power consumption by about than 7.3 times from 6 mW to 0.817 mW when $t_{\mathrm{RES,PS}}$ is 30 ps/LSB and n equals to 1. Even in consideration of margins for PVT variations and calibrations, in which a large over-design factor n equals to 3 is adopted, the power saving is 5.4 times with 30 ps/LSB $t_{\mathrm{RES,PS}}$, validating the advantage in the power efficiency.

B. Nonlinearity Analysis

The jitter analysis predicts the minimum power consumption required for a given jitter. However, practical DTCs often have much higher power consumption to meet linearity requirements [42]. The major nonlinearity sources of DTCs include 1) device mismatches, 2) systemic mismatches from P&R, and 3) architectural nonlinearity from circuit effects such as nonlinear slope-dependent propagation delay [39], [41], [42], [46]. These nonlinearity sources come from different design phases, and have different properties, as shown in Fig. 5. The architectural nonlinearity is deterministic and can be predicted with schematic simulation. On the other hand, nonlinearities from device mismatches and systemic mismatches from P&R are statistical and follow normal distribution [47]. The systemic mismatches from P&R are introduced during layout design, whereas the device mismatches are introduced in chip fabrication. Therefore, the nonlinearity of a fabricated DTC can be expressed as

$$\mu_{\mathrm{INL,tot}} = \mu_{\mathrm{INL,Arch.}} \tag{10}$$

$$\sigma_{\mathrm{INL,tot}} = \sqrt{\sigma_{\mathrm{INL,Dev.}}^2+\sigma_{\mathrm{INL,P\&R}}^2} \tag{11}$$

TABLE I
IMPLEMENTATION OF DTCS AND ASSOCIATED NONLINEARITY CALIBRATION

	Synth.?	DTC design	INL/DNL before Cal.*	Cal.	INL/DNL after Cal.*
JSSC'14 [39]	No	6-bit VS + 6-bit VS	1.2%/0.1%	4-bit 1st-order	0.1%/0.1%
JSSC'15 [19]	No	7-bit PS + 6-bit VS	NA	4-bit 1st-order	NA
JSSC'16 [48]	No	10-bit VS	0.2%/0.05%	5-bit 1st-order	NA
This work	Yes	6-bit PS + 8-bit VS	0.75%/1.5%	6-bit 1st-order	0.75%/1.5%
				6-bit zero-order	0.05%/0.05%

* Normalized to DTC full-scale range.

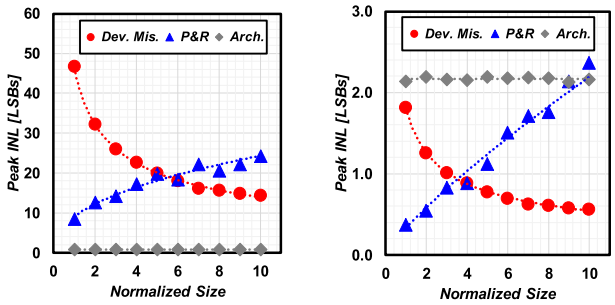

Fig. 6. Simulated peak INL of (a) PS DTC (b) VS DTC. The PS DTC has 6-bit with resolution of 33.2 ps, and VS DTC has 8-bit with resolution of 0.43 ps. The peak INLs due to device mismatches and P&R systemic matches are 3σ values. Both PS and VS DTC INL are normalized to VS DTC resolution (0.43 ps/LSB).

where $\mu_{\text{INL,tot}}$ is the mean of total DTC integral nonlinearity (INL), $\mu_{\text{INL,Arch.}}$ is the mean of INL from architectural nonlinearity. The $\sigma_{\text{INL,tot}}$ is the total standard deviation of DTC INL, and $\sigma_{\text{INL,Dev.}}$ and $\sigma_{\text{INL,P\&R}}$ are standard deviations of INL from device mismatches and P&R respectively.

In conventional custom-designed DTCs, the $\sigma_{\text{INL,P\&R}}$ is minimized by meticulous layout design. The $\sigma_{\text{INL,Dev.}}$ can be reduced by increasing device sizes and thus power consumption. Therefore, the $\mu_{\text{INL,Arch.}}$ dominates the overall nonlinearity. However, the synthesizable DTCs have different nonlinearity characteristic when used as soft IPs. The $\sigma_{\text{INL,P\&R}}$ and $\sigma_{\text{INL,Dev.}}$ have contradicting trends with regard to device sizes. To see the difference, the simulated $\sigma_{\text{INL,P\&R}}$, $\sigma_{\text{INL,Dev.}}$ and $\mu_{\text{INL,Arch.}}$ of PS DTCs and VS DTCs at different sizes are shown in Fig. 6. As clear from the figure, the VS DTC has large $\mu_{\text{INL,Arch.}}$. Besides, the $\sigma_{\text{INL,Dev.}}$ is inversely proportional to device size, whereas the $\sigma_{\text{INL,P\&R}}$ is proportional. To the first order, longer routing lines are used in larger devices, which have larger resistance and variations. Therefore, there is an optimal device size which gives the minimum $\sigma_{\text{INL,tot}}$. For PS DTC, similar trends are observed, except that the $\mu_{\text{INL,Arch.}}$ is much smaller than $\sigma_{\text{INL,Dev.}}$ and $\sigma_{\text{INL,P\&R}}$. Besides, the peak INL PS DTC is larger than 20 LSBs, which is much larger than the fine VS DTCs. Therefore, the nonlinearity of the proposed two-stage PS+VS DTC is dominated by the PS stage. Consequently, the scaling trend and the optimal device sizing of proposed two-stage DTC are basically the same as the PS DTC, and VS DTC only marginally degrade the overall INL.

IV. ZERO-ORDER INTERPOLATION NONLINEARITY CALIBRATION

A. Calibration of Mismatch Dominated DTC

Look-up table (LUT) based piece-wise linear interpolation (PWLI) are widely used to calibrate DTC nonlinearity in PLLs and MDLLs [19], [39], [48]. In this work, the proposed synthesizable DTC nonlinearity is dominated by random mismatches, instead of the architectural nonlinearity [10]. Therefore, the conventional PWLI is modified in two ways to accommodated the mismatch-dominated DTC, which is summarized in Table I. Firstly, the number of LUT entries is designed to match the number of the coarse DTC stages, and each coarse DTC code is calibrated individually. Secondly, zero-order interpolation (ZOI) is adopted instead of the first-order interpolation (FOI) used in previous works [19], [39], [48]. The ZOI effectively applied an offset to each coarse code. The difference of FOI and ZOI is illustrated in Fig. 7. The code 0 of fine VS DTC corresponds to the middle of the delay range, and the fine DTC can realize both positive and negative relative delays. Assume the INL of coarse PS DTC code n and $n+1$ are $INL_C[n]$ and $INL_C[n+1]$ respectively, and the maximum of the fine VS DTC is $INL_{F,max}$, the maximum calibration error $\epsilon_{\text{max,FOI}}$ with FOI calibration occurred at the border of two neighboring coarse codes, and can be expressed as

$$\epsilon_{\text{max,FOI}} = \frac{INL_C[n] + INL_C[n+1]}{2} - (INL_C[n] + INL_{F,max}) = \frac{INL_C[n+1] - INL_C[n]}{2} - INL_{F,max} \quad (12)$$

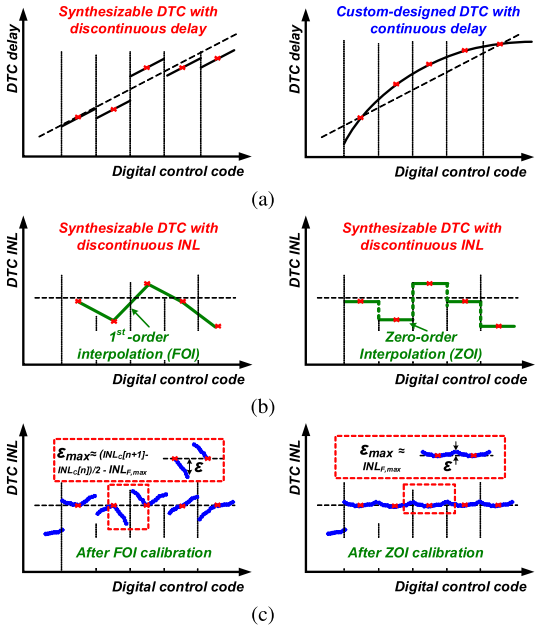

Fig. 7. (a) Delay characteristics of synthesizable PS+VS DTC and custom-design DTC (b) concept of FOI and ZOI based nonlinearity calibration for synthesizable PS+VS DTC with mismatch dominated nonlinearity, and (c) the INL after calibration with both FOI and ZOI based nonlinearity calibration.

On the other hand, the ZOI based calibration utilize the known information that which coarse code is actually used to generate the delay. The maximum calibration error $\epsilon_{\max,\mathrm{ZOI}}$ with ZOI calibration can be expressed as

$$\begin{aligned}\epsilon_{\max,\mathrm{ZOI}} &= INL_C[n] - (INL_C[n] + INL_{F,max}) \\ &= -INL_{F,max} \end{aligned} \tag{13}$$

For conventional custom-designed DTCs with continuous nonlinearity characteristic, such as the one in Fig. 7(a), suppose the $INL_C[n] = 10\,\mathrm{LSBs}$, $INL_C[n+1] = 15\,\mathrm{LSBs}$, and $INL_{F,max} = 2\,\mathrm{LSBs}$, $\epsilon_{\max,\mathrm{FOI}}$ and $\epsilon_{\max,\mathrm{ZOI}}$ are 0.5 LSBs and $-2\,\mathrm{LSBs}$ respectively. However, for mismatch-dominated synthesizable DTCs, suppose the $INL_C[n] = 10\,\mathrm{LSBs}$, $INL_C[n+1] = -15\,\mathrm{LSBs}$, and $INL_{F,max} = 2\,\mathrm{LSBs}$, $\epsilon_{\max,\mathrm{FOI}}$ and $\epsilon_{\max,\mathrm{ZOI}}$ are $-14.5\,\mathrm{LSBs}$ and $-2\,\mathrm{LSBs}$ respectively, as shown in Fig. 7(c). Therefore, the ZOI based calibration is more effective for mismatch-dominated synthesizable DTCs employed in this work.

To validate the effectiveness of the proposed ZOI based calibration, time-domain behavioral simulations were performed. The DTC is modeled as a two-stage implementation with 6-bit PS DTC coarse stage and 8-bit VS DTC fine stage. The resolutions of coarse and fine DTC resolution are 30 ps and 0.3 ps respectively. The fixed delay offset is 100 ps. To stress-test the proposed calibration algorithm, the DTC was modeled with random INLs as large as 15 ps and DNLs as large as 30 ps.

The calibration results with both proposed ZOI and FOI based nonlinearity calibrations are shown in Fig. 8. The modeled DTC INL is shown as the grey dots in Fig. 8(c), which has large DNLs to stress test the proposed ZOI calibration. Fig. 8(a-b) showed the time-domain plot of the calibration codes. With the same 6-bit LUT, the ZOI based calibration converged to correct value, whereas the FOI based calibration failed to converge and saturate at the calibration limit, which is 100 LSBs in this design. Fig. 8(c-d) showed the INL before and after calibration. The proposed ZOI based calibration effectively removed the nonlinearity within the used DTC range, and reduced the phase error. On the contrary, the FOI based calibration introduced larger error and degrade the INL, which contributes to the increased phase error in Fig. 8(f). The phase noise of the MDLL with and without ZOI based nonlinearity calibration is shown in Fig. 9. With the calibration, the nonlinearity induced spur and noise folding are greatly reduced, validating the effectiveness of proposed calibration.

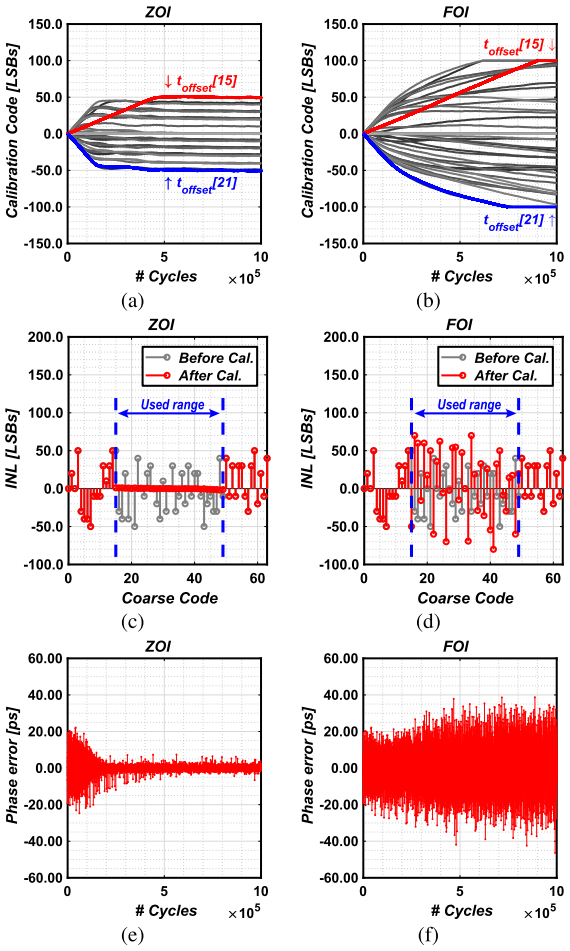

Fig. 8. Behaviorial simulations of the proposed ZOI (a,c,e) and FOI based calibration (b,d,f). The FCW $= 10+2^{-6}+2^{-12}$, $f_{\mathrm{REF}} = 100\,\mathrm{MHz}$ and DSM order is 1. Plots (a-b) are time-domain plot of calibration codes, (c-d) are INL before and after calibration, and (e-f) are phase error present at the BBPD input.

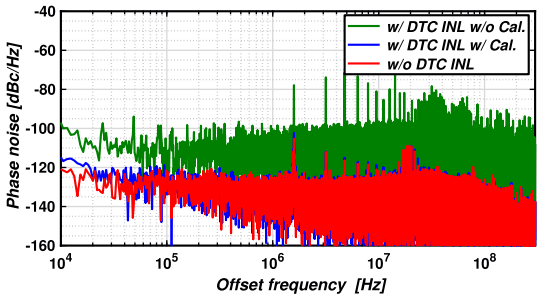

Fig. 9. Simulated phase noise of fractional-*N* MDLL (a) with perfect linear DTC, (b) with nonlinear DTC and without nonlinearity calibration, and (c) with nonlinear DTC and ZOI nonlinearity calibration.

B. Hardware Implementation

The implementation of the DTC calibration logic is shown in Fig. 10(a), which includes both gain calibration and nonlinearity calibration. 1st-order delta-sigma modulator (DSM) is used to reduce the required DTC range. Besides, with highly nonlinear DTC, 1st-order DSM could provide better noise performance than higher order ones [36]. Admittingly the 1st-order DSM could slow the gain calibration speed with very small fractional FCWs. However, for the target applications of this MDLL, such as SoC clocking, techniques such as spread-spectrum clocking introduces a modulated FCW which effectively obviates the operation with very small fractional FCWs. The bandwidth of nonlinearity calibration is smaller than that of gain calibration, and bandwidth of both calibrations is smaller than the phase lock path to avoid race condition. The implementation of coarse stage LMS gain calibration is shown in Fig. 10(b). and the ZOI PWLI implementation is shown in Fig. 10(c).

To save the power consumption and area, several techniques are employed in the digital logic implementation. The DTC gain calibrations employ sign-error LMS algorithm to avoid full precision multipliers 10(b). Besides, the LMS gain calibration step and PLL loopfilter coefficients are designed be power of 2, so the multiplication can be realized as shift operation. What is more, pipeline is inserted to relax the timing constraints. The depth of pipeline is adjustable with

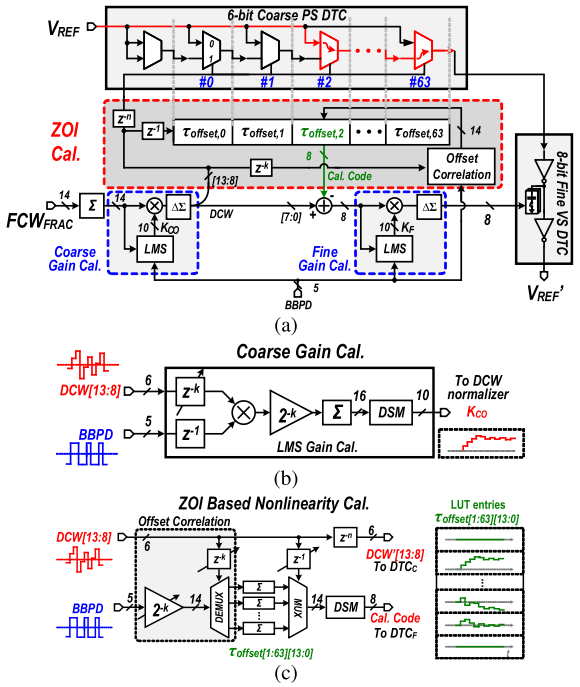

Fig. 10. Implementation of DTC gain and nonlinearity calibrations, (a) system architecture, (b) gain calibration and (c) ZOI nonlinearity calibration.

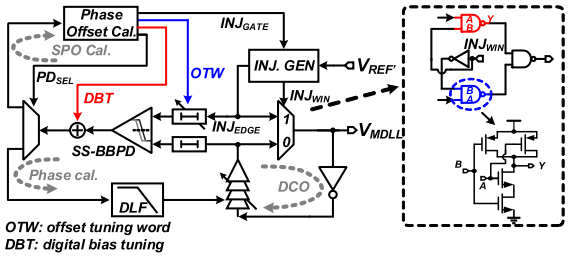

Fig. 11. System diagram of proposed MDLL phase offset calibration.

the variable delay k in the calibration logic in Fig. 10. And extensive clock gating is used in blocks such as LUTs to avoid unnecessary update and save power consumption.

V. MDLL Phase Offset Calibration

In this work, the reference signal is used for both edge replacement and phase calibration, as shown in Fig. 11. It is commonly known that any phase offsets between these two paths would raise the reference spur [19], [49]. The time domain model is shown in Fig. 12(a). INJ_{EDGE} and V_{OSC} are reference edge and oscillation edge respectively. $\Delta\tau_1$ and $\Delta\tau_2$ are static phase offsets (SPO) caused by device mismatches and P&R systemic mismatches, which is time-invariant during MDLL operation. On the other hand, conventional NAND2-based multiplexer presents different load capacitance to the two input signals INJ_{EDGE} and V_{OSC}, as shown in Fig. 11. The load difference is dependent on the INJ_{WIN}, and introduces dynamic phase offsets (DPO) $\Delta\tau_{DPO}$. In this model, the $\Delta\tau_{DPO}$ is used to represent the value of $(\tau_{B=0} - \tau_{B=1})$, in which $\tau_{B=1}$ and $\tau_{B=0}$ are delays when the signal at terminal B of NAND2 is logic 1 and 0 respectively. When INJ_{WIN} equals to 1, the B terminal of NAND2 on the INJ_{EDGE} path is 1, whereas the B terminal of NAND2 on the V_{OSC} path

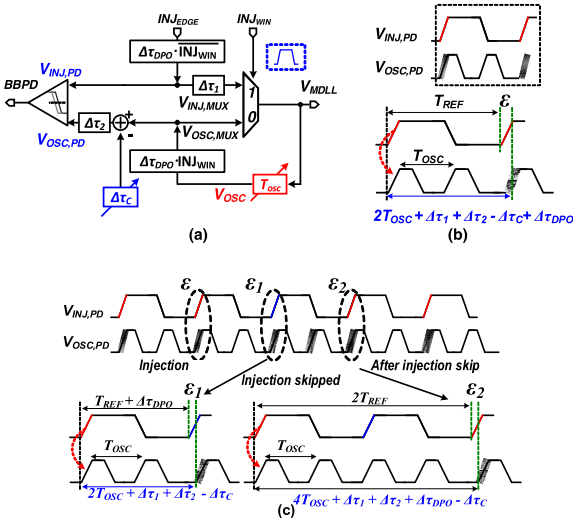

Fig. 12. MDLL phase offset calibration (a) time domain model, (b) waveform of conventional operation and (c) waveform of proposed gated edge replacement.

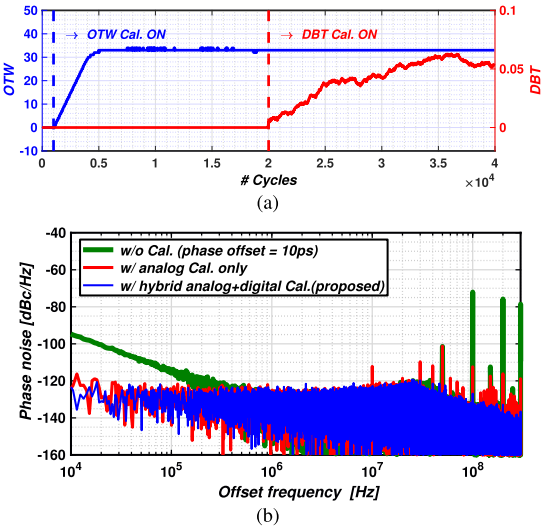

Fig. 13. Simulation results of proposed phase offset calibration (a) time-domain waveforms of calibration codes and (b) phase noise after calibration. Simulation conditions: Integer-N mode with $f_{OUT} = 1\,\text{GHz}$, $f_{REF} = 100\,\text{MHz}$, $\Delta\tau_1 + \Delta\tau_2 = 10\,\text{ps}$, and $K_{DTC} = 0.3\,\text{ps/LSB}$.

is 0. Therefore, $\Delta\tau_{DPO}$ presents on the V_{OSC} path, which is represented as $\Delta\tau_{DPO} \cdot \overline{INJ_{WIN}}$. Conversely, $\Delta\tau_{DPO}$ presents on the INJ_{EDGE} path when INJ_{WIN} equals to 0, and denoted as $\Delta\tau_{DPO} \cdot INJ_{WIN}$. Depending on the INJ_{WIN} state, $\Delta\tau_{DPO}$ appears on INJ_{EDGE} path or V_{OSC} path in a time-interleave manner.

To analyze their effects on MDLL operation, an integer-N operation with a frequency multiplication ratio N of 2 is used for simplicity. Note that the BBPD detects the time difference of $V_{INJ,PD}$ and $V_{OSC,PD}$. While $V_{INJ,PD}$ is updated at every reference period, $V_{INJ,PD}$ is a delayed version of the preceding injected edge INJ_{EDGE}. And the delay is affected by not only the DCO delay T_{OSC}, but also SPOs $\Delta\tau_{1,2}$ and DPOs and $\Delta\tau_{DPO}$. When V_{OSC} is replaced continuously, the phase error ϵ present at BBPD is

$$\begin{aligned}\epsilon &= T_{REF} - [\Delta\tau_1 + N \cdot T_{OSC} + \Delta\tau_{DPO} + \Delta\tau_2] \\ &= [T_{REF} - N \cdot T_{OSC}] - [\Delta\tau_1 + \Delta\tau_2 + \Delta\tau_{DPO}] = 0 \quad (14)\end{aligned}$$

where T_{REF} is the reference period, T_{OSC} is the oscillator period. Therefore, if the $\Delta\tau_1 + \Delta\tau_{\mathrm{DPO}} + \Delta\tau_2$ is not zero, the [T_{REF} cannot match $N \cdot T_{\mathrm{OSC}}$]. As a result, the PLL output would have a period distortion at the rate of f_{REF}, which translates into reference spurs. In this work, the $\Delta\tau_{\mathrm{DPO}}$ is eliminated with a proposed complementary-switched MUX and BBPD, which will be explained in more detail in VI-B. The $\Delta\tau_1 + \Delta\tau_2$ is removed by a compensation delay $\Delta\tau_{\mathrm{C}}$. By gating the edge replacement, three different phase errors can be detected, as shown in Fig. 12(c). The phase errors during continuous edge replacement, at the gating cycle and immediately after gating are expressed as is ϵ, ϵ_1 and ϵ_2 respectively, and can be expressed as

$$\epsilon = [T_{\mathrm{REF}} - N \cdot T_{\mathrm{OSC}}] - [\Delta\tau_1 + \Delta\tau_2 - \Delta\tau_{\mathrm{C}} + \Delta\tau_{\mathrm{DPO}}] \quad (15)$$

$$\epsilon_1 = [T_{\mathrm{REF}} - N \cdot T_{\mathrm{OSC}}] - [\Delta\tau_1 + \Delta\tau_2 - \Delta\tau_{\mathrm{C}} - \Delta\tau_{\mathrm{DPO}}] \quad (16)$$

$$\epsilon_2 = 2[T_{\mathrm{REF}} - N \cdot T_{\mathrm{OSC}}] - [\Delta\tau_1 + \Delta\tau_2 - \Delta\tau_{\mathrm{C}} + \Delta\tau_{\mathrm{DPO}}] \quad (17)$$

The ϵ and ϵ_1 are used for phase lock, whereas the ϵ_2 is used for offset calibration. Since all the three phase errors are forced to zero on average and $\Delta\tau_{\mathrm{DPO}}$ is zero by circuit design, the $\Delta\tau_{\mathrm{C}}$ must be equal to $\Delta\tau_1 + \Delta\tau_2$.

Gating injection technique has been proposed in [50], [51] to calibrate the static phase offset. Yet the DPO also contributes to the DCO period distortion and interferes with SPO calibration, as demonstrated in above analysis. Moreover, $\Delta\tau_{\mathrm{C}}$ is realized with DTCs as an analog domain delay in [50], [51]. However, the residue reference spur is limited by the finite DTC resolution [29]. Besides, the gating operation introduces fractional spurs to the PLL output [27], [50]. Therefore, $\Delta\tau_{\mathrm{C}}$ is realized as a hybrid of analog domain delay and digital domain digital bias to BBPD output in this work In the first step, an offset tuning word (OTW) is calculated and applied to DTCs at BBPD input to reduce the SPO into the linear region of BBPD. Delay difference of two DTCs are used to compensate both positive and negative SPOs. Then a digital bias tuning (DBT) code is added to BBPD output to remove residue offset in digital domain. In this way, the $\Delta\tau_{\mathrm{C}}$ can be realized with arbitrarily fine resolution. To ensure the correct operation, the residue offset $\Delta\tau_{\mathrm{residue}}$ must be smaller than the linear region of BBPD. Under worst case, the $\Delta\tau_{\mathrm{residue}}$ is about half of DTC residue t_{res}, which is 0.2 ps. On the other hand, with $\geq$ 0.48 ps RMS jitter, this requirement is easily met. The DBT value is automatically found by the type-I feedback loop, and is not sensitive to the exact BBPD gain. The simulated OTW and DBT waveforms are shown in Fig.13(a), and the simulated phase noise with and without proposed calibration are shown in Fig.13(b). With the proposed hybrid offset calibration, both the reference spurs and gating-induced fractional spurs can be greatly suppressed. Besides, proposed calibration creates one additional feedback loop, which helps to suppress the flicker noise at low offset frequency. The proposed offset calibration compensates the differential mode delay between the edge replacement and phase calibration paths. It is independent from the DTC gain and nonlinearity calibrations, which control the common mode delay. Besides, the phase offset calibration uses gating control signal to correlate with BBPD error, which is independent from the DTC control word. Therefore, the phase offset calibration and DTC calibrations will not interfere with each other.

Fig. 14 shows the implementation of the proposed SPO calibration. For simplicity, only the offset calibration logic part is shown. A programmable counter with a self-dithered

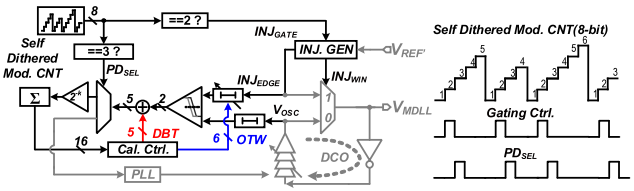

Fig. 14. Implementation of proposed two-step hybrid offset calibration.

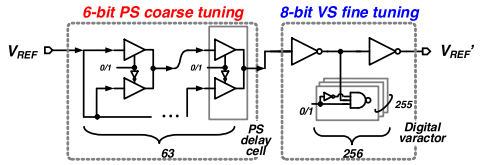

Fig. 15. Implementation details of proposed two-stage PS-VS DTC.

modulus value is used to generate the PD_{SEL} and gating control signal INJ_{GATE}. A one-cycle pulse is generated when the counter value is 2, which is used as INJ_{GATE}. The PD_{SEL} is generated in a similar way with the trigger value set to 3. The self-dithered modulus counter dynamically changes the instantaneous frequency of INJ_{GATE} and PD_{SEL}, thus avoid idle tones at PLL output. Phase error ϵ_2 is accumulated. In the first step, the 6-bit MSBs of the accumulator is used as OTW to tune the delay of INJ_{EDGE}. A calibration controller monitors the OTW value variation to freeze the OTW value after settle and starts the DBT adaptation. To ensure the residue error is within the BBPD linear region, the calibration DTC resolution K_{DTC} is designed to 0.3ps/LSB, and the whole calibration range is around $\pm$10 ps. The accumulator is reset and used to generate a 5-bit DBT. The 2-bit BBPD output is expanded to a signed 5-bit number and added with the DBT, which has been validated to be sufficient by system simulations. The calibration DTCs add about 30 ps delay to BBPD input, which negligibly affects BBPD gain and quantization noise. Since the MDLL output noise dominated by the reference injection path [11], the calibration will have very small effect on the MDLL output jitter.

VI. Circuit Implementation

A. Design and Optimization Procedure

With the standard cell only circuit design, the MDLL is designed and optimized follows a procedure that only uses the timing library [52]. Among the MDLL building blocks, DCO and DTC contribute most to the overall MDLL noise [11]. Both DTC and DCO noise can be estimated with delay, power consumption, and supply voltage obtained from the timing library [53]. Therefore, a rough estimation of the noise of DTC, DCO and MDLL noise is possible. Transistor-level analog simulations are only required for accurate noise characterizations. Thus, circuit design and optimization can be carried out before analog process design kit (PDK) is available, easing design in new processes.

B. Synthesizable Timing Generation Circuits

The implementation of the proposed two-stage DTC is shown in Fig. 15, and the details about delay and range are summarized in Table II. The coarse stage delay cells are

TABLE II

SIMULATED IMPLEMENTATION DETAILS OF PROPOSED TWO-STAGE SYNTHESIZABLE DTC

	Control bits	PVT condition	Range [ps]	Resolution [ps]
Coarse	6-bit	TT*	2090.0	33.2
		SS**	3374.6	53.6
		FF***	1355.1	21.5
Fine	8-bit	TT*	108.5	0.43
		SS**	155.2	0.61
		FF***	78.0	0.31

* TT corner, temp. = 27°, V_{DD} = 1.2 V ** SS corner, temp. = 80°, V_{DD} = 1.1 V *** FF corner, temp. = −20°, V_{DD} = 1.3 V

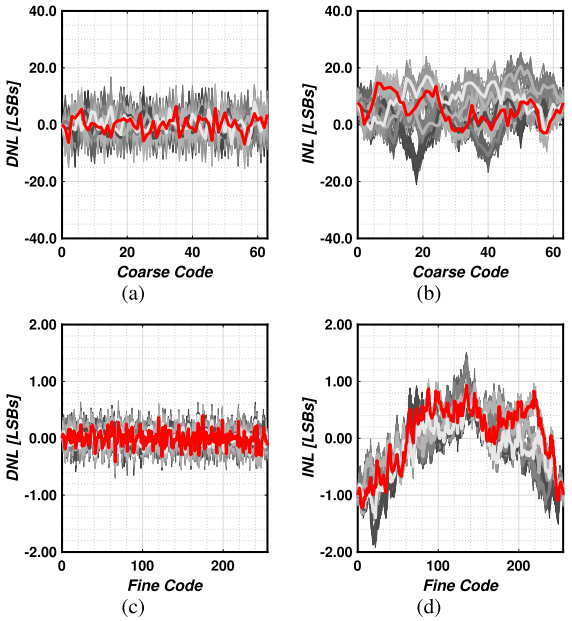

Fig. 16. Two-stage synthesizable DTC nonlinearity characteristics under typical corner with different automatic P&R trials, (a) DNL of coarse stage and (b) INL of coarse stage, (c) DNL of fine stage and (d) INL of fine stage.

implemented with tristate buffers, and the fine stage delay cells are implemented with NAND3 based varactors. The DTC range is designed to be more than 1 ns under PVT variations. Besides, the fine stage VS DTC range is designed to ensure continuous coverage and nonlinearity calibration. The DNL and INL of both coarse and fine stage DTCs are obtained from LPE simulations, with 5 different P&R trials. Each P&R trial is with 50 Monte-Carlo runs to reflect device mismatches. Increasing the Monte-Carlo run number from 50 to 200 changes the standard deviation by less than 1%. Therefore, a run number of 50 is adopted to reduce the simulation time. The results are shown in Fig. 16. As evident from the simulations, the nonlinearity of the coarse stage PS DTC is dominated by systemic mismatches from automatic P&R and device mismatches. On the other hand, the nonlinearity of fine stage VS DTC is dominated by deterministic architectural nonlinearity, which is similar to those custom-designed VS DTCs [39], [40]. The simulated DTC nonlinearity under voltage and temperature variations are shown in Fig. 17(a). The PS DTC nonlinearity does not change much, which is expected since all the delay elements' driving strength and loads are changed in the same way. On the other hand, the PS DTC has larger variations, because the driving strength and load has different temperature and supply sensitivity. However, since the fine DTC VS nonlinearity is

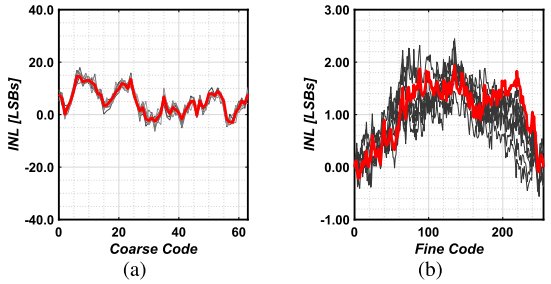

Fig. 17. Two-stage synthesizable DTC nonlinearity characteristics under different voltages (1.1/1.2/1.3 V) and temperatures (−20/27/80°C), (a) INL of coarse stage, (b) INL of fine stage.

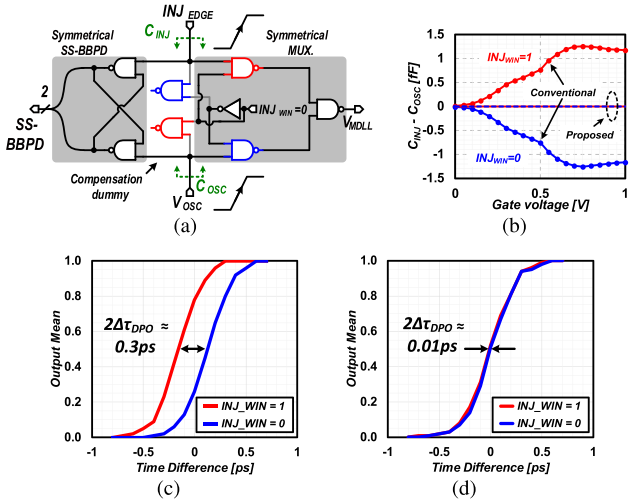

Fig. 18. Proposed DPO compensated BBPD (a) circuit implementation, (b) simulated capacitance variation, (c) simulated DPO of conventional BBPD and (d) simulated DPO of proposed BBPD.

relatively small compared to coarse PS DTC, the overall DTC nonlinearity does not change much.

The proposed DPO-compensated MUX and BBPD are shown in Fig. 18(a). Two complementary-switched dummy NAND2 gates are added to remove the load capacitance modulation by INJ_{WIN}. Fig. 18 shows the simulated difference between load capacitance C_{INJ} and C_{OSC} when INJ_{WIN} is "0" and "1". In conventional implementation [11], the peak capacitance difference is about 2.6 fF, which affects the signal slope and the propagation delay. On the other hand, with the proposed complementary switching, the capacitance difference is effectively eliminated. The simulated effective dynamic phase offset at BBPD output is shown in Fig. 18(c) and Fig. 18(d). With the proposed complementary switch, the dynamic delay offset is reduced from 150 fs to 5 fs, which has a negligible effect on reference spur.

The implementation of DCO and gated injection edge and window generator are shown in Fig. 19. The DCO tuning is separated into three banks, including a 4-bit PS coarse bank, 4-bit VS medium bank and 6-bit VS fine bank. The DCO implementation is similar to the one presented in [11], but a wider fine tuning range is used to facilitate the fractional-N phase locking. The DCO delay range and resolution of each bank are shown in Table III. The gated injection generator derives injection edge and window signal, and ensures the injection edge is around the middle of injection window. Besides, two identical inverters are added on the INJ_{EDGE} and

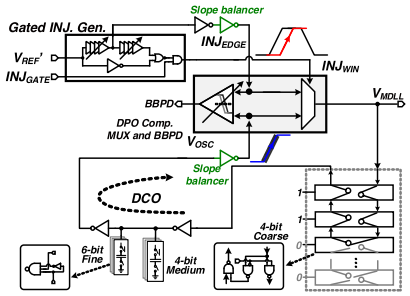

Fig. 19. Implementation of the DCO and the gated injection edge and window generator.

TABLE III
SIMULATED IMPLEMENTATION DETAILS OF DCO

	Control bits	PVT condition	Range [ps]	Resolution [ps]
Coarse	4-bit	TT*	1030.9	68.7
		SS**	1591.3	106.1
		FF***	699.4	46.6
Medium	4-bit	TT*	90.0	6.0
		SS**	121.8	8.1
		FF***	69.3	4.6
Fine	6-bit	TT*	22.5	0.36
		SS**	30.2	0.48
		FF***	17.5	0.28

* TT corner, temp. = 27°, V_{DD} = 1.2 V ** SS corner, temp. = 80°, V_{DD} = 1.1 V *** FF corner, temp. = −20°, V_{DD} = 1.3 V

TABLE IV
MEASURED POWER CONSUMPTION OF PROPOSED MDLL

	DCO*	DTC*	INJ. Gen.*	Dig. Logic*	Total*
Fractional-*N*	1.068	0.456	0.072	0.252	1.85
Integer-*N*	1.068	–	0.072	0.084	1.22

* all in mW.

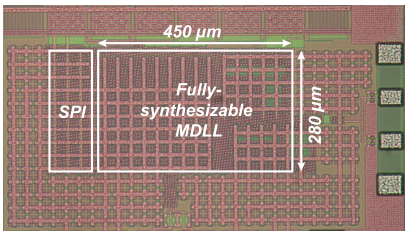

Fig. 20. Chip micro-graph of the fully-synthesizable fractional-*N* MDLL.

V_{OSC} paths to ensure the same drive strength. Together with the DPO compensated MUX and BBPD, the same signal-slope is ensured.

VII. MEASUREMENT RESULTS

The entire MDLL is synthesized using commercial digital design tools with a non-modified standard cell library. The core area of the MDLL is 0.126 mm^2, which is fabricated in TSMC 65 nm LP CMOS process. The active area of DTC, DCO and digital logic is 0.0042 mm^2, 0.0051 mm^2, and 0.0244 mm^2 respectively. The total active area is 0.0337 mm^2. The rest of the core area is occupied by decoupling capacitors and filler cells, which are used to provide sufficient decoupling. The nominal supply voltage is 1.2 V, and is used across all measurements unless otherwise stated. Fig. 20 shows the die photo. The phase noise is measured by a signal source analyzer (Keysight E5052B), the spectrum is measured by a

TABLE V
MEASURED RANGE AND RESOLUTION OF DCO AND DTC

	DCO			DTC	
Temp.[°C] /Voltage[V]	Coarse [ps]	Medium [ps]	Fine [ps]	Coarse [ps]	Fine [ps]
−20/1.3	940.8/62.7	85.6/5.7	21.6/0.34	1911.9/30.3	102.4/0.40
−20/1.2	1086.2/72.4	95.5/6.4	24.8/0.39	2220.2/35.2	119.6/0.47
−20/1.1	1217.4/81.2	106.6/7.1	27.1/0.43	2567.9/40.8	130.9/0.51
27/1.3	899.3/59.9	83.0/5.5	20.7/0.33	1846.4/29.3	96.4/0.38
27/1.2	1051.5/70.1	91.8/6.1	23.3/0.37	2161.1/34.3	110.8/0.44
27/1.1	1150.1/76.7	102.8/6.9	26.0/0.41	2404.7/38.2	122.6/0.48
80/1.3	860.3/57.4	78.5/5.2	19.2/0.30	1811.3/28.8	96.6/0.38
80/1.2	977.8/65.2	85.9/5.7	21.9/0.35	2004.9/31.8	105.3/0.41
80/1.1	1085.7/72.4	97.6/6.5	24.8/0.39	2292.5/36.4	117.8/0.46

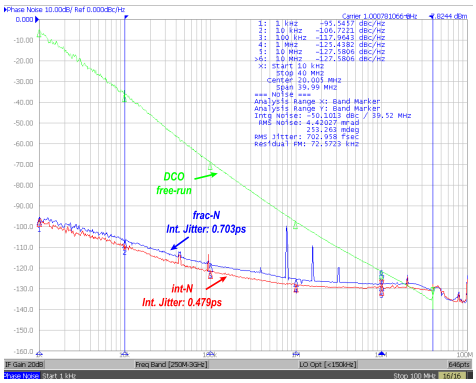

Fig. 21. Measured phase noise in (a) DCO free-run mode (b) integer-*N* mode and (c) fractional-*N* mode.

spectrum analyzer (Anritsu MS2830A), and the reference is provided by a signal generator (Rhode&Schwartz SMA100). The core power consumption excluding IO buffers of proposed MDLL is shown in Table IV. The total power consumption is 1.85 mW in the fractional-*N* mode. The power consumption in the integer-*N* mode can be reduced to 1.22 mW by bypassing DTC and gating off part of calibration logic. The measured range and resolution of DCO and DTC are shown in Table V. The measured DCO coarse/medium/fine resolution under 1.2V/27°C are 70.1/6.1/0.37 ps/LSB respectively, and the DTC coarse/fine resolution are 34.3/0.44 ps/LSB respectively, which are close to TT case simulated results in Table III and Table II.

Fig. 21 shows the measured phase noise with a 100 MHz reference clock. The DCO free-run mode phase noise is −97.6 dBc/Hz at 1 MHz offset frequency, and the power consumption is 1.068 mW at 1 GHz. The MDLL achieves 0.48 ps jitter at 1 GHz output in integer-*N* mode, and 0.70 ps jitter in fractional-*N* mode, both integrated from 10 kHz to 40 MHz. The fractional spur and integrated jitter across different fractional channels are shown in Fig. 23(a) and Fig. 23(b). The worst-case fractional spur is lower than −59.0 dBc, as shown in Fig. 22, and the worst-case jitter is 0.70 ps. Assume the residual INL after calibration is sinusoidal, the peak-to-peak INL magnitude Δt_{INL} can be estimated by $\Delta t_{\mathrm{INL}} = 2/\pi \cdot T_{\mathrm{DCO}} \cdot 10^{\mathcal{L}_{spur}/20}$ [39], in which T_{DCO} is the DCO period. The estimated INL is about 0.7ps, which agrees well with the simulation results, validating the effectiveness of proposed ZOI-based calibration.

The measured reference spur at 1.2 V is −64.5 dB, and reference spurs across different supply voltage is shown in Fig. 25. Lower than −60 dBc reference spur is achieved

TABLE VI

PERFORMANCE SUMMARY AND COMPARISON WITH RING OSCILLATOR BASED INTEGER-*N* IL-PLLS/MDLLS

	JSSC'13 [49]	JSSC'15 [19]	JSSC'19 [54]	JSSC'19 [29]	ISSCC'19 [55]	VLSIC'18 [27]	ISSCC'17 [9]	SSCL'18 [56]	SSCL'19 [11]	**This Work**
	Custom-design						Fully-synthesizable			
Architecture	MDLL	MDLL	ILCM	MDLL	ILCM	BBDPLL	IL-PLL	TDC-PLL	MDLL	MDLL
Osc. Type	Ring	Ring	Ring	Ring	Ring	Ring	Ring	Ring	Ring	Ring
CMOS Tech.	130 nm	65 nm	65 nm	28 nm	65 nm	7 nm	65 nm	14 nm	65 nm	65 nm
Area [mm^2]	0.25	0.09	0.16	0.0056	0.055	0.018	0.028	0.009	0.035	0.126
f_{OUT} [GHz]	0.8~2.0	1.6~1.9	2.6~5.2	1.55~3.35	2.2~2.5	0.48~4	0.52~1.15	1.0~5.5	-	0.6~1.6
f_{REF} [MHz]	375	50	54**	200	100	30~250	150	50	100	100
P_{DC}/f_{OUT} [mW/GHz]	0.89/1.5	2.4/1.6	6.5/4.752	1.45/3.0	11.0/2.4	6.3/4	3.8/0.9	9.7/5.0	1.2/1.0	**1.22/1.0**
Int. Jitter [ps]	0.4	0.47	0.366	0.292	0.14	0.427	0.42	4.71	0.4	**0.48**
Int. BW [Hz]	1M~100M	30k~30M	10k~30M	10k~40M	10k~40M	100k~1G	10k~10M	–	10k~10M	10k~40M
FOM† [dB]	-248.5	-242.7	-240.6	-249.1	-246.7	-239.4	-241.7	-216.8	-247.2	**-245.5**
Ref. Spur [dBc]	-55.6	-55.3	-53	-44	-72	-61	–	-40*	-52	**-64.5**
DJ_{RMS} †† [ps]	0.25	0.24	0.11	0.47	0.02	0.05	–	0.41	0.57	0.13

* estimated from figure ** with reference quadrupler † $FOM = 10 \cdot \log_{10}[(\text{Int.Jitter}/1s)^2(P_{DC}/1mW)]$ †† $DJ_{RMS} = 10^{L_{S\,pur}/20}/(\sqrt{2}\pi f_{OUT})$ [57]

TABLE VII

PERFORMANCE SUMMARY AND COMPARISON WITH DTC-BASED AND SYNTHESIZABLE FRACTIONAL-*N* PLLS/MDLLS

	JSSC'14 [39]	JSSC'18 [36]	JSSC'18 [51]	JSSC'19 [42]	JSSC'19 [30]	ISSCC'15 [7]	JSSC'19 [47]	CICC'18 [10]	SSCL'20 [12]	**This Work**
	Custom-design					Fully-synthesizable				
Architecture	DTC + BBDPLL	DTC + TDC-PLL	DTC + ILCM	DTC + Samp. PLL	DTC + MDLL	Soft-inj. IL-PLL	DI-TDC PLL	DTC + MDLL	DTC + MDLL	**DTC + MDLL**
Osc. Type	*LC*	*LC*	*LC*	*LC*	Ring	Ring	Ring	Ring	Ring	Ring
CMOS Tech.	65 nm	65 nm	65 nm	28 nm	65 nm	65 nm	28 nm	65 nm	5 nm	65 nm
Area [mm^2]	0.2	0.23	0.27	0.45	0.0275	0.05	0.0043	0.12	0.0036	0.126
f_{OUT} [GHz]	3~4	2.0~2.8	6.75~8.25	5.5~7.3	1.6~3.0	0.8~1.7	0.1~2.01	0.6~1.7	0.4~1.5	0.6~1.6
f_{REF} [MHz]	40	26†	115	52†	100	380	80	100†	100	100
P_{DC}/f_{OUT} [mW/GHz]	4.2/3.6	0.98/2.44	3.25/7.36	18.9/6.33	2.5/1.65	3.0/1.5	6.95/2.056	2.5/0.97	0.95/1.0	**1.85/1.0**
Frac. Spur [dBc] (best/worst)	-63*/ -51.7	-75*/ -56	-59*/ -42.4	-68.2*/ -64	-53*/ -51.5	–	-50*/ -24*	-58.5	-49.2/ -44.3	**-61.9/ -59.6**
Int. Jitter [ps] (best/worst)	0.7	0.53/ 0.59	0.11/ 0.17	0.075/ 0.085*	0.395	3.6	2.13	1.2	0.97/ 1.9	**0.56/ 0.70**
Int. BW [Hz]	100k~10M	10k~10M	10k~30M	10k~10M	30k~30M	1k~100M	10k~100M	10k~10M	10k~10M	10k~40M
FOM [dB] (best/worst)	-236.9	-246/ -245	-254/ -250	-249.7/ -248.6	-244.0	-224.2	-225.0	-234.4	-240.5/ -234.7	**-242.3/ -240.4**
Ref. Spur [dBc]	–	-72	-52	-70.2	-56	–	-52	–	-30.9	**-64.5**
DTC Cal.	Gain +INL	Gain	Gain	Gain	Gain +INL	–	–	Gain +INL	Gain +INL	Gain +INL

* estimated from figures † w/ reference doubler

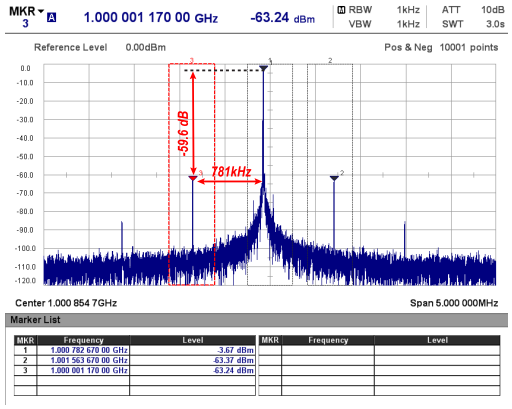

Fig. 22. Measured fractional spurs of a near-integer ($FCW = 10 + 2^{-7}$) channel.

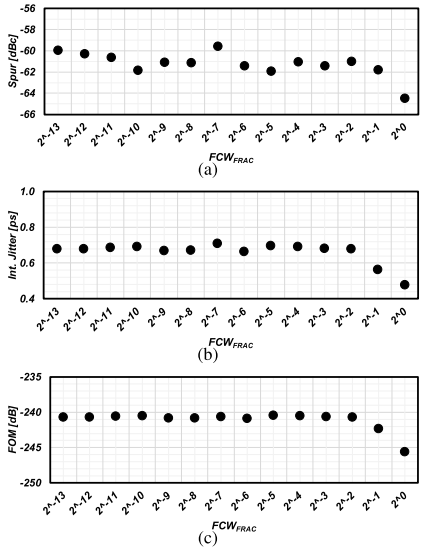

Fig. 23. Measured (a) fractional spur, (b) integrated jitter and (c) FOM at different fractional FCWs with $FCW_{INT} = 10$ and $f_{REF} = 100$ MHz.

across 1.15−1.25 V supply voltage. The measured reference spur is measured with input reference signal power of 7 dBm, and is limited by parasitic coupling through IO pads and supply/substrate. Reducing the reference signal power to 5 dBm improves the reference spur by 1−2 dB, but the in-band phase noise is much elevated. And further reducing the power below 5 dBm causes the IO pad fail to work. In comparison, when the phase offset calibration is disabled, the lowest reference spur is −52.7 dBc at 1.2 V nominal supply, which corresponds to 2.3 ps phase offset. The reference spur degrades as supply deviates from 1.2 V, as the slope mismatch becomes larger

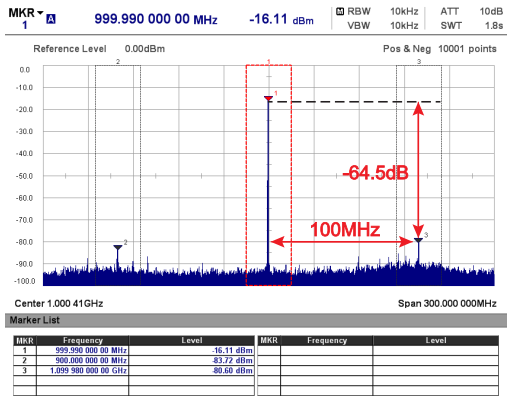

Fig. 24. Measured reference spur with phase offset calibration ON.

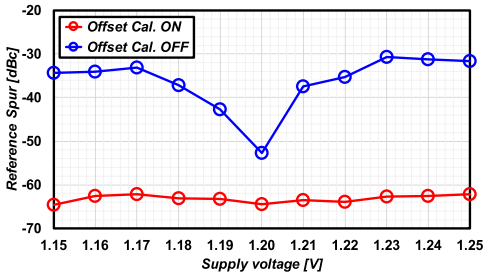

Fig. 25. Measured reference spur versus supply voltage with phase offset calibration ON and OFF at 1 GHz.

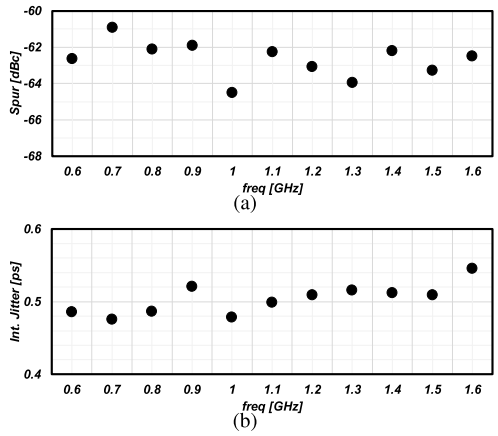

Fig. 26. Measured (a) reference spur, (b) integrated jitter at different integer-N channels.

and the phase offset increases. The measured reference spur and integrated jitter at different integer-N channels are shown in Fig. 26. Consistent reference spur performance is observed across different frequencies. The DCO measured supply sensitivity is about 1 GHz/V at 1 GHz carrier frequency. However, thanks to the wide bandwidth, the MDLL supply sensitivity is attenuated by 20 dB at 3 MHz frequency offset, which greatly improved the overall supply sensitivity

Table VI and Table VII summarize the measured performance of the proposed MDLL in integer-*N* and fractional-*N* modes respectively, and compare with the state-of-the-art PLLs/MDLLs. Compared to other fully-synthesizable PLLs/MDLLs, proposed MDLL achieved the best jitter and spur performance. Besides, the results are compared favorably to those of custom-designed digital PLLs/MDLLs, validating the effectiveness of the proposed synthesizable circuits and digital calibrations.

VIII. Conclusion

A fully-synthesizable fully calibrated fractional-*N* MDLL is presented in this paper. Based on noise and linearity analysis of different DTC architectures, a low-power, high-performance synthesizable DTC is proposed and implemented, along with the proposed digital nonlinearity calibration optimized for the synthesizable design. Besides, both SPO and DPO are calibrated to reduce the reference spur. The SPO is calibrated by a two-step hybrid with arbitrarily fine resolution, and the DPO is calibrated by a proposed complementary switched MUX and BBPD. The MDLL achieves worst-case 0.70 ps RMS jitter and −59.6 dBc fractional spur with 1.85 mW power consumption in the fractional-*N* mode, corresponding to −240.4 dB FOM. Besides, both SPO and DPO are compensated, resulting in less than −60 dBc reference spur is achieved across 1.15−1.25 V.

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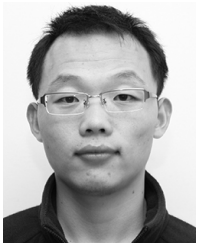

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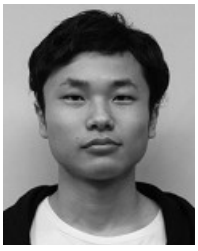

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