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MMC Control Strategy for Converter Lifetime Optimization Based on Thermal Stress Analysis of Lower IGBT Device in Half-Bridge Submodules

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***Abstract*—GigaWatt-scale offshore wind farms are being connected using the Modular Multilevel Converter (MMC), in which submodules act as the main building block. The extensive number of connections has a significant effect on the system's security of supply. Periodic weather conditions and time-dependent labor capacity complicate maintenance, emphasizing the need for more flexibility when replacements are required. Traditionally, submodules are redundant or over-dimensioned to increase reliability, but do not resolve flexibility issues faced by operators. This article presents a novel operation method introducing flexibility in the submodule stress distribution. Specific submodules can be used more or less frequently depending on maintenance achievability. The technical condition of each submodule is determined, and then a selection window with a configurable length determines the submodule-specific insertion frequency, affecting the remaining useful lifetime. The capacitor voltage balance can be guaranteed with traditional sorting methods and is compatible with the lifetime optimization algorithm using a priority factor. The priority can be divided between lifetime optimization and capacitor voltage balancing depending on the operator's needs. This is superior to the traditional methods due to the ability to control the submodule-specific deterioration pace. Analytical evaluation and simulation studies demonstrate the effectiveness of this control approach.**

***Index Terms*—IGBT, insertion control, lifetime optimization, MMC, power losses, reliability.**

I. Introduction

TO ACHIEVE climate agreement targets, gigawatt-scale wind farms are being connected offshore, building High-Voltage Direct Current (HVDC) connections. In recent years, Modular-Multilevel Converters (MMC) have replaced line-commutated converters as the preferred technology for transferring renewable energy due to benefits in, e.g., full active and reactive power control, grid forming capabilities, and reduced harmonic distortion [1]. The converter offshore placement brings significant challenges for Transmission System Operators (TSOs) regarding maintenance. Onsite inspections are costly and challenging due to reduced labor capacity and outage window possibilities affecting the system's reliability.

An MMC arm consists of N_s submodules connected in series each with DC storage capacitors and power semiconductors. The submodules are constantly switched in and bypassed from the arms such that a desired sinusoidal arm voltage is generated. The reliability of the submodule semiconductors has been studied widely [2], [3], [4]. In [2], the authors presented a model to estimate the remaining useful lifetime for the IGBT semiconductors in the submodules based on the device characteristics and converter mission profile. Although unrealistic lifetime estimations were obtained for gigawatt-scale MMCs due to the exclusion of the di-ionized water cooling loop heat exchanger, the methodologies indicated influences from the IGBT thermal impedance and the inverse effect of power losses on the converter's remaining useful lifetime. Namely, higher power losses reduce the semiconductor's useful lifetime [3]. Several thermal optimization categories have been reported in the literature [4], [5], [6], [7], [8], [9]. The first is related to the MMC design, the second to the modulation strategy, and the last to control system implementations [4].

The design classification implies mainly the addition of extra components such as described in the reliability-centred maintenance approach in [5]. Reliability enhancement was observed when redundant submodules were added to the arms. An optimized maintenance interval with a downward trend between submodule failures was determined according to the number of faulted elements reducing subsequent costs. In [7] an additional diode parallel to the bottom switch in half-bridge configured submodules was proposed to reduce thermal stress and, thus, improve the lifetime of the submodules. These improvements however all require hardware modifications resulting in additional costs. Several modulation strategies were presented such as a discontinuous pulse width modulation in [6] and [9] which clamps the arms to the DC-poles during specific intervals. This reduces the semiconductor power losses and thus increases lifetime but affects the power quality.

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Control solutions were studied such as the second-order harmonic circulating arm-current injection in [4] to improve the thermal distribution among the submodule semiconductors. The methodology was also demonstrated under reduced operational DC-pole voltages [10]. The critical submodule semiconductors operate at a lower junction temperature which increases their useful lifetime. The circulating current injection was also shown to reduce the peak arm current in [8] and thus bring down the stress on the submodule semiconductors. The foregoing studies focused on the optimized submodule maintenance schedule or the extension of the submodule lifetime, but neglected the TSO's main challenge concerning maintenance interval flexibility. Nowadays inspections and replacements are merely determined by external factors such as weather conditions, disconnection permits, and maintenance crew availability. The MMC shall be operated so that submodule replacements are needed during fitting time intervals, which depend on external factors. Another aspect is the imbalance in thermal stress between the upper and lower IGBT devices within a submodule. While in theory, lifetime optimization could be achieved on an individual IGBT level, in practice, these devices are often packed in a single housing and are not individually exchangeable. For a TSO, it is thus more beneficial to have lifetime optimization on the submodule level instead of the semiconductor level.

This article proposes a novel MMC submodule insertion control methodology considering an optimized submodule power semiconductor lifetime with respective failures at favored intervals. The expected moment of submodule semiconductor failure can be adapted using a priority factor configuring the operational precedence between arm capacitor voltage balance and submodule semiconductor lifetime optimization. The contribution of the article is twofold:

- Introducing MMC submodule semiconductor lifetime optimization focused on the TSO maintenance challenges.
- Presenting an MMC arm insertion strategy based on submodule remaining useful lifetime and time-dependent maintenance possibility.

First, the semiconductor power losses are investigated together with the half-bridge submodule topology switching states. The lifetime balancing methodology is introduced after the submodule sorting principle is explained. Next, the effectiveness of the proposed technique is analytically evaluated in which the critical semiconductor junction difference is studied. Finally, a control system implementation is suggested with a simulation that indicates the insertion differences between submodules to confirm the presented methodology so that the remaining useful lifetime can be adjusted according to the time-dependent maintenance availability.

II. Semiconductor Power Losses

A half-bridge configured submodule consists of four semiconductors and a DC-storage capacitor as depicted in Fig. 1. The semiconductors should be operated to an extent the voltage over the capacitor remains within the specified tolerance band.

When switch *S1* is in ON-state for time duration τ, the capacitor conducts AC-current i_{xy} and the DC-storage capacitor

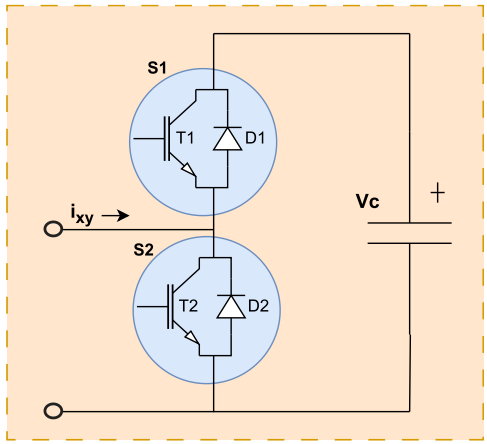


Fig. 1. Circuit diagram of the half-bridge configured submodule.

TABLE I
Switching States of the Half-Bridge Submodule [11]

Switching State	S_1	S_2	V_{SM}	$i_{xy}>0$	$i_{xy}<0$
1	1	0	V_c	$V_c \uparrow$	$V_c \downarrow$
2	0	1	0	$V_c \approx$	$V_c \approx$

$\uparrow$ = Increasing, $\approx$ = No change, $\downarrow$ = Decreasing

voltage V_{c} changes:

$$V_c\left(t+\tau\right)=\frac{1}{C}\int_{t}^{t+\tau} i_{xy}(t)S_1 dt+V_c(t). \tag{1}$$

The effect of possible switching states and current direction in half-bridge submodules is summarized in Table I.

The alternating arm-current and different switching states create power losses on these switching devices, affecting the devices' remaining useful lifetime. These power losses are often calculated based on converter operational conditions as in [12]. Here, analytical expressions for the MMC arm currents and respective semiconductor power losses have been formed.

With the three AC phases being symmetrical, only one has been used in derivation $(v_{\mathrm{a}}, i_{\mathrm{a}})$. First, the voltage and current for a single phase in the AC system can be written as:

$$\begin{aligned} v_a(t) &= E_m \sin\left(\omega_n t\right), \\ i_a(t) &= I_m \sin\left(\omega_n t+\theta\right), \end{aligned} \tag{2}$$

with E_{m} and I_{m} representing the respective voltage and current amplitudes. Neglecting the circulating currents [12], [13], the phase-A upper arm current i_{au} and lower arm current i_{al} can be written as,

$$\begin{aligned} i_{au}(t) &= \frac{I_{dc}}{3}+\frac{i_a(t)}{2}, \\ i_{al}(t) &= \frac{I_{dc}}{3}-\frac{i_a(t)}{2}, \end{aligned} \tag{3}$$

as the expressions dependent on the DC-pole current I_{dc} and AC-system phase-A current i_{a}. By substituting $i_{\mathrm{a}}(t)$ from (2) into (3) and using current ratio $k=3I_m/2I_{dc}$, the arm currents

can we written as function of variables ω_n, θ, and I_{dc},

$$i_{au}(t) = [1 + k\sin(\omega_n t + \theta)]\frac{I_{dc}}{3}$$
$$i_{al}(t) = [1 - k\sin(\omega_n t + \theta)]\frac{I_{dc}}{3}, \quad (4)$$

which can be measured at the converter terminals, and assures the methodology can be applied in practice since these are widely available in converter control systems. The average conduction current per semiconductor device in half-bridge configured submodules can further be calculated using the inserted probability and time instants at which a specific semiconductor operates.

The resulting average conduction losses for the Insulated Gate Bipolar Transistor (T) and Free Wheeling Diode (D) semiconductors can finally be calculated,

$$P_{c,T/D} = |I_{av}|\,V_0 + R_0 I_{rms}^2, \quad (5)$$

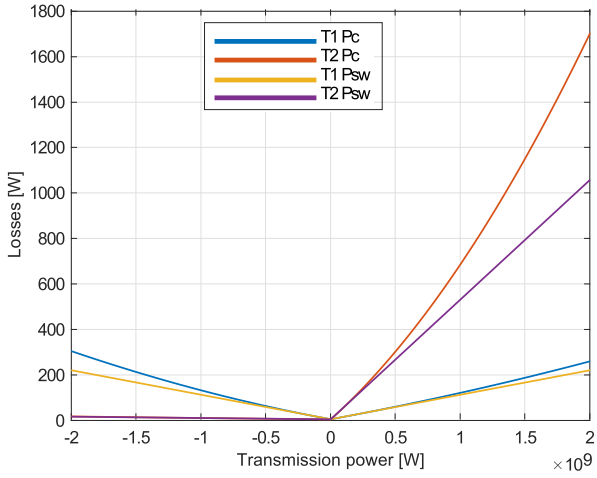
with I_{av} representing the average current through the device, V_0 being the forward device voltage, R_0 the conduction state resistance, and I_{rms} the RMS current through the device, all in the period corresponding to the losses computation time interval.

It was found that the average IGBT switching losses are approximately linearly scalable with the average current [14]. The average losses of IGBT switching P_{sw} and diode recovery P_{rec} can subsequently be approximated by multiplying the loss of one switching action by the switching frequency. Here, the losses of a switching action are scaled linearly from the datasheet measurement reference voltage $V_{\mathrm{ref,T/D}}$ and reference current $I_{\mathrm{ref,T/D}}$ to the current and blocking voltage in the operational condition [15]:

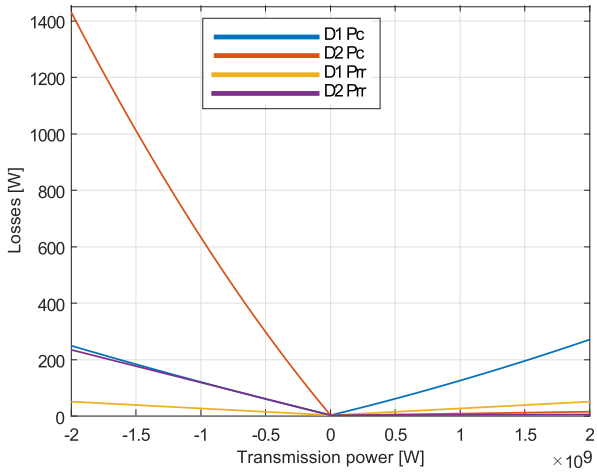
$$P_{sw} = (E_{on} + E_{off})\frac{V_c\,|I_{av}|\,f_{sw}}{V_{ref,T} I_{ref,T}},$$
$$P_{rec} = E_{rec}\frac{V_c\,|I_{av}|\,f_{sw}}{V_{ref,D} I_{ref,D}}. \quad (6)$$

These power loss components are calculated for a single converter unit (pole level) in a 525 kV symmetrical bipolar MMC rated 2 GW as shown in Fig. 2. The individual converter units, each with a 1 GW rating, are assumed to operate in the steady-state decoupled mode, implying the units can be controlled separately and do not influence each other. All submodules are half-bridge configurations with *5SNA 3000K452300* [16] Hitachi Energy IGBT devices, wherein the conditions for the loss measurements are: $V_{\mathrm{cc}} = 2.8\,\mathrm{kV}$, $I_{\mathrm{c}} = 3\,\mathrm{kA}$, $R_{\mathrm{g}} = 1.5\,\Omega$, $C_{\mathrm{GE}} = 330\,\mathrm{nF}$, $V_{\mathrm{GE}} = 15\,\mathrm{V}$, $L_\sigma = 130\,\mathrm{nH}$.

The IGBT semiconductor losses with predominantly T2 transistor conduction losses are the highest in inverter mode (transmission power >0), while diode D2 conduction losses are the highest in rectifier mode (transmission power <0). This is a result of the DC offset in the arm current. In inverter mode, IGBTs conduct more during the positive half-cycle, while in rectifier mode, diodes conduct more during the negative half-cycle, and these components have different loss characteristics. Since D2 has low reverse recovery losses in inverter mode, the overall effect on lifetime is limited. On the contrary, T2 has high switching and high conduction losses in inverter mode, characterizing the ratio of how frequently a submodule is inserted (switching losses in T2) compared to bypassed (conduction losses in T2) mainly defines a submodule's lifetime.



(a)



(b)

Fig. 2. Semiconductor conduction (P_{c}), switching (P_{sw}), and reverse-recovery (P_{rr}) loss components in 150 Hz switched (f_{sw}) half-bridge configured submodules, while $Q = 0\,\mathrm{MVar}$. (a) IGBT semiconductor. (b) FWD semiconductor.

III. Methodology

To achieve the desired sinusoidal arm voltage, a specific number of submodules, denoted as $n_{\mathrm{ins}}(t)$, within an arm needs to be activated. The higher the derivative of the amplitude of the sinusoidal reference waveform, the greater the number of submodules that need to be transitioned from a bypassed to an inserted mode. In general, this depends on factors such as the voltage balancing strategy and allowed voltage ripples. The allowed voltage ripples are adjustable via the thresholds of the reference waveform. In contrast, the voltage balancing is assured by changing individual submodule insertion vectors based on the arm current direction and other factors as will be explained in the following paragraphs. The determination of which exact

submodules in the arm should be switched from the bypassed to the inserted mode is carried out by the arm controller and is currently primarily driven by the submodule capacitor energy balancing process, assuring equal submodule capacitor voltages.

Methods for monitoring the IGBT technical condition have been developed and proposed, e.g. in papers [17] and [18]. These methods utilize ON-state collector-emitter voltage $v_{ce,on}$ measurement equipment to estimate the remaining useful lifetime of submodules.

A. Influencing Lifetime

In the case of a converters's submodule operating in inverter mode that has an IGBT device with a lower remaining useful lifetime and a maintenance interval is known, it is advantageous to bypass this specific submodule more frequently (resulting in an increased P_{sw} at *T2*). Hence, this specific submodule deteriorates faster. This strategy ensures that the submodule fails within the maintenance interval. By increasing the bypass frequency of this particular submodule, other submodules need to be bypassed less frequently (decreasing P_{sw} at *T2*), leading to a longer estimated lifetime for these submodules. This adjustment is made possible by modifying the generation of the individual submodule gate signal as a function of both the submodule capacitor voltages and the IGBT condition indicators.

B. Sorting Principle

The conventional capacitor voltage balancing algorithm usually sorts the capacitor voltages based on the unbalance factor γ at different voltages [19],

$$\gamma = \frac{\Delta U_{c,\max}}{U_{c,rated}} = \frac{U_{c,i} - U_{c,rated}}{U_{c,rated}}, \tag{7}$$

in which sorting algorithms, such as quicksort and bubble sort, can be used. Similarly, submodule condition indicators can be sorted using a new vector,

$$\delta = \frac{\Delta V_{ce,on}}{V_{ce,on,av}} = \frac{V_{ce,on,i} - V_{ce,on,av}}{V_{ce,on,av}}, \tag{8}$$

implying the condition indicators are based on the relative submodule condition in an arm. This sorting algorithm is applied for each current direction, implying that the SM with the highest capacitor voltage has the highest priority when the current is negative through its capacitor. During the optimization period, the selected IGBT is switched more frequently, causing the submodule to be bypassed and its capacitor to charge more slowly compared to others. Once the IGBT is no longer used, conduction shifts to the diode, allowing the capacitor to charge more rapidly until voltage balance is restored. Since the selection window is limited to submodules between B_{l} and B_{u}, well within the total number of submodules, overall voltage balancing across the converter arm remains effective.

As the capacitor voltage balance has the highest priority, the submodules shall first be sorted on capacitor voltage priority and afterward, a specific part, denoted as a selection window, of the resulting vector can be re-sorted on δ. This means the sorting process is extended and is based on two parameters where both are decoupled allowing parallel sorting. A generic flow diagram of the proposed extended sorting algorithm applied on a converter arm with eight submodules and a selection window of four submodules is depicted in Fig. 3.

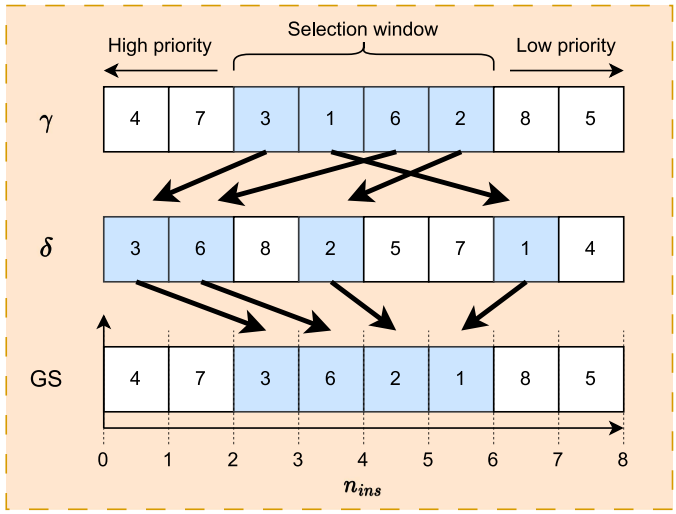


Fig. 3. Extended sorting methodology with capacitor voltage balance vector γ and ON-state collector-emitter vector δ. Based on the selection window, the final gate signal vector is generated, and based on n_{ins}, several submodules are switched to inserted mode.

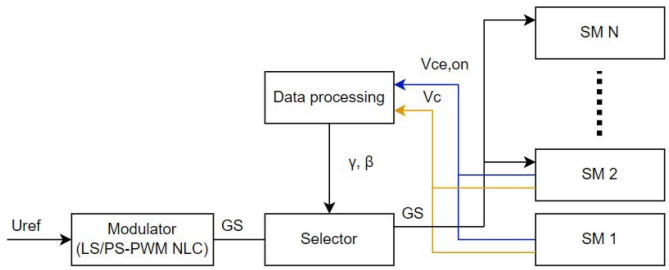


Fig. 4. Block diagram of the extended sorting method including capacitor voltage balancing and lifetime optimization control methodology.

As seen in Fig. 3, submodule 4 has the highest priority to be inserted to provide capacitor voltage balance over the submodules. The selection window length W_{L} is four, implying successively submodules 3, 1, 6, and 2 are re-appointed according to δ. After re-arranging the submodule priority inside the selection window, the Gate Signal (GS) vector is generated based on $n_{\mathrm{ins}}(t)$.

A block diagram of the extended sorting methodology is depicted in Fig. 4. First, each submodule reports the $v_{\mathrm{ce,on}}$ and capacitor voltage v_{c} measurements to a data processing unit where γ and δ are formed. Based on W_{L}, a look-up action is performed, and the respective gate signals are sent to the submodules.

IV. Quantifying the Effectiveness

An analytical approach is presented to verify the effectiveness of the proposed control methodology. As the existing control

methodology has no lifetime optimization component, the proposed methodology is verified based on performance requirements of the traditional method, such as capacitor balancing. First, the selection window determination and limitations are discussed, whereafter the loss components are outlined, and finally, the junction temperature differences in the selected submodule and the remaining submodules are studied.

A. Selection Window Determination

Considering the LS/PS-PWM NLC method, the junction temperature T_{j} of a semiconductor in a half-wave current cycle increases from the instant when this semiconductor starts conducting ($t_{\mathrm{a,i}}$) till the instant 75 % of the half-wave cycle has passed ($t_{\mathrm{b,max}}$); the last 25 % of the half-wave current cycle the junction temperature will decrease [20]. After this 75 % instant, the semiconductor is no longer used and thus cools faster, increasing the difference between maximum and minimum temperature and so the magnitude of the temperature cycle. The instant when this peak temperature is reached will be further considered as also applicable to DC-biased arm currents. To be effective, the lifetime optimization methodology should thus be operational in this 75 % of the half-wave cycle. For a bypassed *T2* in inverter mode, the semiconductor conducts if the arm current gets positive, meaning the start $t_{\mathrm{a,i}}$ and the end of the positive half-wave cycle $t_{\mathrm{b,i}}$ instants can be written,

$$t_{a,i} = \frac{1}{\omega_N}\left[-\theta - \sin^{-1}\left(\frac{1}{k}\right) + 2\pi\left(1+K\right)\right],$$
$$t_{b,i} = \frac{1}{\omega_N}\left[-\theta + \sin^{-1}\left(\frac{1}{k}\right) + \pi\left(1+2K\right)\right], \quad (9)$$

as a function of the angular fundamental AC frequency ω_N, current phase angle θ, current index k, and period integer K. The 75 % half-wave boundary where the maximum $\mathrm{T_j}$ occurs is thus,

$$t_{b,\max} = \frac{t_{a,i} + 3t_{b,i}}{4}, \quad (10)$$

for the first period. If the respective submodule is bypassed for this entire period, conduction energy losses $\mathrm{E_c}$ are generated in *T2* and can be calculated by the instantaneous value,

$$E_c = \int_{t_{a,i}}^{t_{b,\max}} V_{ce,on}[1 + k\sin\left(\omega_N t + \theta\right)]\frac{I_{DC}}{3}dt, \quad (11)$$

in case $v_{\mathrm{ce,on}}$ is treated as constant. Another simplified approach is to multiply the average conduction power losses of *T2* with the time of conduction $\Delta t = t_{b,\max} - t_{a,i}$.

The reference arm voltage determines how many submodules should be inserted. Neglecting the second harmonic, and taking the upper arm as example, the number of submodules inserted in this arm,

$$N_{su}(t) = \frac{N_s}{2} - \frac{mN_s}{2}\sin\left(\omega_N t\right) \quad (12)$$

is denoted by the arm's modulation index m, the total number of submodules N_{s} in this arm (even number), and the angular fundamental system frequency ω_N. It is important to note N_{su} is the short-time average value of n_{ins} which is further explained

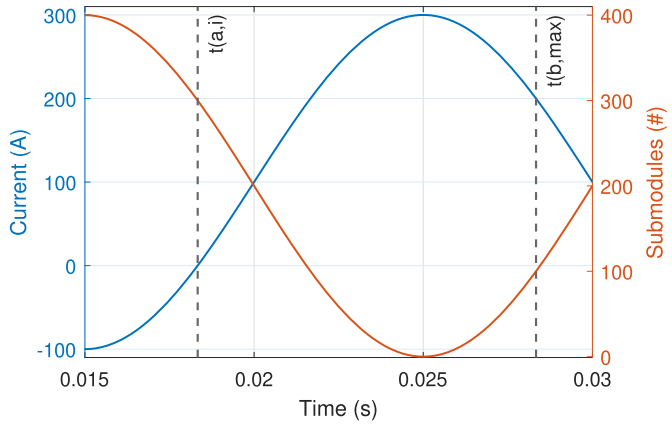


Fig. 5. Illustration of arm current and N_{su}. It should be noted there is no ripple ($\mathrm{n_{ins}}$) shown over $\mathrm{N_{su}}$. $N_{\mathrm{s}} = 400$.

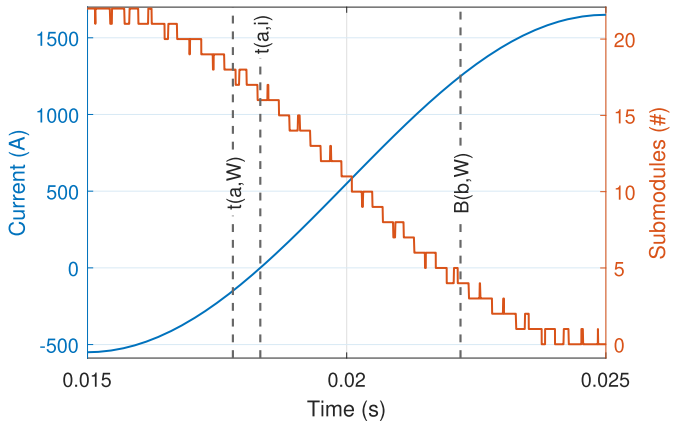


Fig. 6. Illustration of arm current and $\mathrm{n_{ins}}$ with time boundaries equal to the selection window. The arm has 22 submodules, $B_{\mathrm{l}} = 4$, $B_{\mathrm{u}} = 18$, $I_{\mathrm{dc}} = 1.65\,\mathrm{kA}$, $\theta \approx 0$, and the submodule switching frequency is 150 Hz.

using Fig. 6; there is a ripple seen over N_{su} which waveform is represented as n_{ins}. The selection window boundaries B_{l} and B_{u} are integers that should be significantly in between $\{0, N_s\}$ and in the middle as much as possible, so that the highest priority is given to the capacitor voltage balancing process. The more submodules are available for the capacitor balancing process, the better the capacitor voltages can be balanced. Only a fraction of the submodules will be sorted by condition indicator $V_{\mathrm{ce,on}}$ as otherwise the capacitor balancing process is jeopardized. Because the arm current $i_{\mathrm{au}}(t)$ is 180 degrees out-of-phase with the number of submodules that should be inserted in an arm $N_{\mathrm{su}}(t)$ for $\theta = 0$, the selection window starts when the arm-current increases and $N_{\mathrm{su}}(t)$ decreases as illustrated in Fig. 5.

In between $t_{\mathrm{a,i}}$ and $t_{\mathrm{b,max}}$ the inner controller should change the insertion vector so that the most losses occur in the selected submodule *T2* device causing increased ΔT_{j} and other submodules have reduced losses and a lower ΔT_{j} in their *T2* device.

The insertion vector $\{0, N_s\}$ has a selection window with lower boundary B_{l} and upper boundary B_{u} where it holds that $(0 < B_l < B_u < N_s)$. Both B_{l} and B_{u} could be even or odd

integers. The ratio J_{L} given $(B_u - B_l)/N_s$ defines the freedom the controller has to move losses from any submodule to the selected submodule, whereas the ratio $J_{\mathrm{C}} = (N_s - B_u + B_l)/N_s$ defines the remaining freedom for the inner arm capacitor voltage balancing. Both boundaries also define when the controller can start with interchanging insertion indices and when it stops. These time instants can be calculated as:

$$t_{a,W} = \frac{1}{\omega_N}\left[-\sin^{-1}\left(\frac{N_s - 2B_l}{mN_s}\right) + \pi\left(1+2K\right)\right],$$
$$t_{b,W} = \frac{1}{\omega_N}\left[-\sin^{-1}\left(\frac{N_s - 2B_u}{mN_s}\right) + \pi\left(1+2K\right)\right]. \quad (13)$$

As the 75 % instant of the half-wave cycle is before the end of the respective cycle, it is clear that $t_{\mathrm{b,W}} < t_{\mathrm{b,i}}$, meaning $t_{\mathrm{b,W}}$ defines the end of the selection window in the time domain. The start of the selection window in the time domain is defined by the maximum of $t_{\mathrm{a,W}}$ and $t_{\mathrm{a,i}}$.

B. Ripple Estimation

The ripple over N_{su} can be studied with the boundaries set. The decreasing part of $n_{\mathrm{ins}}(t)$ as resulting from phase shifted-PWM modulation, thus including the ripple, together with the increasing arm current $i_{\mathrm{au}}(t)$ is shown in Fig. 6.

The time window where the controller can act for interchanging vector indices is shown to be $(t \in [t_{\mathrm{a,i}}, t_{\mathrm{b,W}}])$ in this example. If the arm current $i_{\mathrm{au}}(t)$ would horizontally offset by at least $t_{\mathrm{a,i}} - t_{\mathrm{a,W}}$ seconds (phase-shift θ), the lower boundary is determined by $t_{\mathrm{a,i}}$. The fluctuations of n_{ins} over the plane staircase function N_{su} in this time interval determine how many times the selected submodule can be switched from bypassed mode to inserted mode and equals seven during the selected time window in the illustration.

When a submodule is switched to inserted mode during a ripple instant over the plane staircase function, the conduction losses P_{c} in *T2* decrease as only *D1* conducts if the submodule is inserted and the arm current is positive. This means that the higher the submodule switching frequency, the lower the conduction losses in *T2*. To calculate the reduction in conduction losses, the carrier waves should be studied, as no plane function could be found in literature describing the time duration of the ripple as a function of the switching frequency and the number of submodules.

The triangular carriers in phase-shifted PWM can be written as periodic linear functions,

$$c_u(t) = 2N_s f_{sw}\left(t - \frac{K}{f_{sw}} - \frac{i}{f_{sw}N_s}\right),$$
$$c_d(t) = N_s - 2N_s f_{sw}\left(t - \frac{K}{f_{sw}} - \frac{i}{f_{sw}N_s}\right), \quad (14)$$

where integer *K* indicates the switching frequency period number and integer *i* represents the submodule phase shift number $(0 < i < N_s)$. The carrier belonging to the first submodule has no phase-shift $(i = 0)$, whereas the carrier belonging to the second submodule is phase-shifted with $1/(f_{sw}N_s)$, meaning $i = 1$. This process repeats itself until the carrier of the submodule N_{s} is phase shifted with $i = N_s - 1$. For the next period, $K = 1$ and $i = 0$ again. For simplicity, $(K/f_{sw} - i/(f_{sw}N_s))$ can thus be altered to $i/(f_{sw}N_s)$ with $(0 < i < \infty)$ due to these periodical properties.

If the submodule switching frequency is at least twice the integer multiple of the fundamental system frequency, two important things can be noticed in the selection window $\{B_l, B_u\}$:

- The intersection of an upward carrier waveform $c_{\mathrm{u}}(t)$ with the short-time average arm voltage reference waveform $N_{\mathrm{su}}(t)$ causes n_{ins} to drop by exactly one submodule.
- The intersection of a downward carrier waveform $c_{\mathrm{d}}(t)$ with the short-time average arm voltage reference waveform $N_{\mathrm{su}}(t)$ causes n_{ins} to rise by exactly one submodule.

This means that during the decreasing N_{su} in the operating window time frame $(t \in [t_{\mathrm{a,W/i}}, t_{\mathrm{b,W}}])$, the intersection with the downward periodical carriers initiates a ripple over the plane-decreasing staircase function. The intersection time instant t_{start} defining the start of the ripple,

$$\frac{N_s}{2} - \frac{mN_s}{2}\sin\left(\omega_n t_{start}\right) = N_s - 2N_s f_{sw}\left(t_{start} - \frac{i}{f_{sw}N_s}\right), \quad (15)$$

cannot be solved algebraically and should therefore be solved numerically. The first subsequent intersection of an upwards carrier waveform $c_{\mathrm{u}}(t)$ defines the end of this ripple t_{end} over the plane decreasing staircase function:

$$\frac{N_s}{2} - \frac{mN_s}{2}\sin\left(\omega_n t_{end}\right) = 2N_s f_{sw}\left(t_{end} - \frac{i}{f_{sw}N_s}\right). \quad (16)$$

However, the periodic properties $(0 < i < \infty)$ of the linear carrier notation give infinite intersections while only the intersections in between $(t \in [t_{\mathrm{a,W/i}}, t_{\mathrm{b,W}}])$ are of interest for interchanging insertion indices. Therefore, i should be a vector with a length of the number of intersections starting from the first carrier with horizontal offset $i_{\mathrm{d,s}}$ till the last crossing carrier with horizontal offset $i_{\mathrm{d,e}}$. For the downward carriers, these instances can be calculated using,

$$i_{d,s} = \left\lceil N_s f_{sw}\left(t_{a,W/i} - \frac{N_s + N_s m\sin\left(\omega_n t_{a,W/i}\right)}{4N_s f_{sw}}\right)\right\rceil,$$
$$i_{d,e} = \left\lfloor N_s f_{sw}\left(t_{b,W} - \frac{N_s + N_s m\sin\left(\omega_n t_{b,W}\right)}{4N_s f_{sw}}\right)\right\rfloor, \quad (17)$$

while for the upwards carriers, these instances can be computed similarly, however, by replacing the c_{d} function part with the function from c_{u} from (14).

C. Verification of the Analytical Model

A comparison is made between the estimated ripple time instantons using the analytical approach presented and a MATLAB / Simulink simulation. The number of submodules in the arm is 22, with a selection window lower boundary B_{L} of 7 and a selection window upper boundary B_{u} of 15. This means the parameter J_{L} equals $(15 - 7)/22 = 0.4$ while the

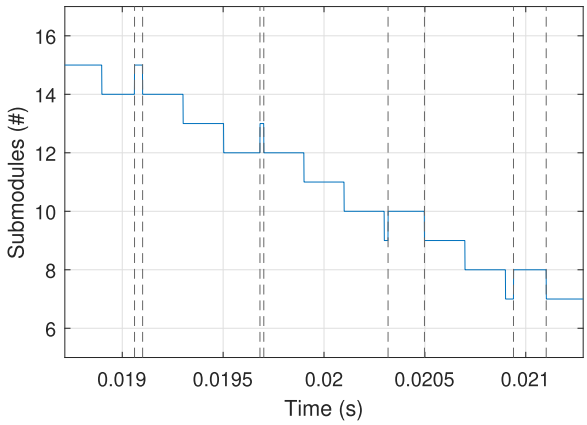


Fig. 7. Comparison of the analytical estimation of the ripple instants in dotted lines with the MATLAB/Simulink n_{ins} simulation during the complete submodule index interchanging interval, implying the selection window in the time domain.

remaining capacitor voltage balancing coefficient J_c equals $(22-15+7)/22=0.6$. The modulation index m is 1, while the DC-current I_{dc} is set 1.5 kA. The submodule switching frequency f_{sw} is 150 Hz and the AC phase-shift θ is assumed to be zero. The results are depicted in Fig. 7.

It is seen that the estimated ripple initiation and ending time instants are very accurate to the MATLAB/Simulink simulation.

D. Energy Loss Transfer

The length of each pair of ($t \in [t_{start}, t_{end}]$) defines exactly the time duration that conduction losses are dissipated in *D1* instead of in *T2* for the selected submodule. In between these pairs, *T2* experiences conduction losses. To calculate those conduction losses, the average and RMS-squared currents through *T2* in those time windows can be computed,

$$I_{T2,av} = \frac{\int_{t_{end,i}}^{t_{start,i+1}} \left[1 + k\sin\left(\omega_n t + \theta\right)\right] \frac{I_{dc}}{3}\, dt}{t_{start,i+1} - t_{end,i}},$$

$$I^2_{T2,rms} = \frac{\int_{t_{end,i}}^{t_{start,i+1}} \left[1 + k\sin\left(\omega_n t + \theta\right)\right]^2 \frac{I^2_{dc}}{9}\, dt}{t_{start,i+1} - t_{end,i}}, \quad (18)$$

with which the conduction losses in these periods ($t \in [t_{end,i}, t_{start,i+1}]$) can be solved using (5). Another approach is to subtract the average conduction losses in (5) with average current boundaries ($t \in [t_{start,i}, t_{end,i}]$) as in (18) from the conduction losses computed in (11) where it is assumed that no switching action takes place.

For the switching energy losses in the time window, the controller should interchange insertion indices ($t \in [t_{a,W/i}, t_{b,W}]$), the average current through *T2* during each switching action should be estimated. In this case the time boundaries for $I_{T2,av}$ and $I^2_{T2,rms}$ in (18) should be adjusted to $t_{start,i}$ and $t_{end,i}$ as a single ripple duration over the plane staircase function is normally very small and the average current through *T2* during switching from bypassed to inserted mode can be assumed to be identical to the average current through *T2* during switching to bypassed mode again. The resulting switching energy losses in the time window can thus be calculated using a discrete summation:

$$E_{sw} = (E_{on} + E_{off})\frac{U_{cx}}{U_{ref,T}} \sum_{j=1}^{length(i_{d,s})} \frac{|I_{T2,av}(j)|}{I_{ref,T}}, \quad (19)$$

The trade-off between switching as much as possible and completely bypassing the selected submodule to generate more losses in the selected submodule can now be examined. For the analysis, the *5SNA 1500E330305* [21] and the *5SNA 3000K452300* [16] Hitachi Energy IGBT devices are studied. The subsequent characteristics of these devices are indicated in Table II.

TABLE II
RELEVANT SPECIFICATIONS OF THE IGBT DEVICES

IGBT Device	U_0 [V]	$r_{0,t}$ [mΩ]	E_{on} [J]	E_{off} [J]	$U_{ref,T}$ [kV]	$I_{ref,T}$ [kA]
5SNA 1500E330305	3.1	2.0	2.15	2.80	1.8	1.5
5SNA 3000K452300	1.6	0.67	15.5	15.1	2.8	3.0

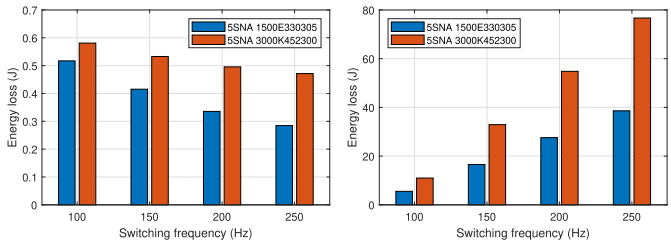


Fig. 8. Comparison between the energy losses in one single *T2* device during the lifetime optimization controller selection window for a converter arm with 200 submodules, B_l is 90, and B_u is 110 and 2 kV rated submodules. (a) Conduction losses. (b) Switching losses.

It is important to note that the two studied devices differ significantly in characteristics. While the *5SNA 1500E330305* IGBT device has switching losses ($E_{on} + E_{off}$) equal to 15.4 J, with the loss measurement references linearly scaled to $U_{ref,T}$ is 2.8 kV and $I_{ref,T}$ equal to 3.0 kA, these energy losses are a factor of two higher (30.6 J) for the *5SNA 3000K452300* IGBT device.

Both IGBT devices are analyzed in an MMC operating in inverter mode with submodules in half-bridge configurations. There are 200 submodules per arm (N_s) whereas each submodule capacitor is rated 2 kV. The DC-current I_{dc} equals 1.5 kA, defined by the upper limit of the older *5SNA 1500E330305* IGBT device conduction current rating and the converter is assumed to be operating in steady-state. The lifetime optimization controller selection lower limit B_l is set to 90 while the upper limit B_u is set to 110. This means J_L equals $(110-90)/200 = 0.1$ while the remaining inner arm capacitor voltage balancing freedom coefficient J_C equals $(200-110+90)/200 = 0.9$. The resulting energy losses for a single *T2* device are shown in Fig. 8.

It is noticeable from the results that the conduction energy losses (Fig. 8(a)) are only a fraction of the switching energy losses (Fig. 8(b)) for both IGBT devices during the lifetime

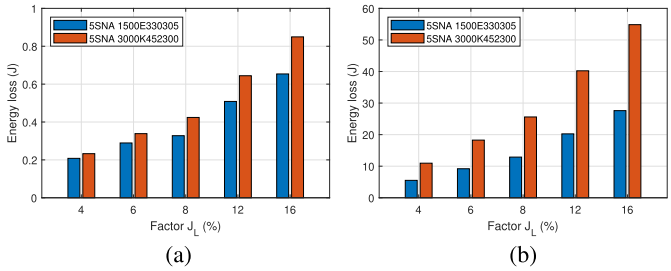


Fig. 9. Comparison between the energy losses in one single *T2* device during the lifetime optimization controller selection window for a converter arm with 200 submodules, submodule switching frequency 150 Hz, and 2 kV rated submodules. (a) Conduction losses. (b) Switching losses.

optimization controller selection window $\{B_l, B_u\}$. This seems to contradict the semiconductor power loss estimations shown in Fig. 2, where it was determined that the conduction power losses are higher compared to the switching power losses for *T2* configured in half-bridge with the MMC operating in inverter mode. However, this difference can be explained by the following arguments:

- During average power loss estimations, it was assumed *T2* switches exactly once during each submodule switching frequency cycle. For the lifetime optimization controller, *T2* switches multiple times during each submodule switching frequency cycle, increasing the switching energy losses.
- For the computation of the average power losses, the total energy loss during a switching action (E_{on} + E_{off}) was multiplied by the period $1/f_{sw}$ of the submodule switching frequency. Since the activation period ($t_{\text{a,W/i}}$ - $t_{\text{b,W}}$) of the lifetime optimization controller is much shorter than $1/f_{sw}$, the switching energy losses contribute much more to the total energy loss in *T2*.

Furthermore, it can be seen that a higher submodule switching frequency results in lower conduction energy losses in *T2*. This confirms the assumption that when a submodule is switched from bypassed to inserted mode and the arm current $i_{\text{au}}(t)$ is positive, *D1* conducts instead of *T2* which subsequently reduces respective conduction losses in *T2*. The more this process repeats (higher submodule switching frequency), the lower the conduction energy losses in *T2* will be. Since the submodule must be bypassed after every switching action to inserted mode, these losses will never drop to zero. An obvious opposite phenomenon can be seen for the switching energy losses; the higher the submodule switching frequency, the higher the switching energy losses in *T2*.

The effect of the selection window width ($B_{\text{u}} - B_{\text{l}}$), as defined in parameter J_{L} (%) as a function of the total number of submodules in an arm N_{s} and the selection boundaries has been analyzed. Here, it is assumed the submodule switching frequency is fixed at 150 Hz and further converter and device characteristics are identical to the previous study. The results of the generated energy losses in a single selected submodule IGBT *T2* are shown in Fig. 9.

Here, it is confirmed that the higher parameter J_{L}, the more energy losses can be generated in the selected submodule IGBT *T2*. The most significant losses are in the switching energy losses, as was also emphasized in Fig. 8.

E. Junction Temperature Effect

For the selected submodule where more losses must be generated, the junction temperature fluctuation ΔT_j in *T2* should be estimated to assess the effect on the remaining useful lifetime of the submodule. The methodology for calculating the temperature ripple was presented in [20]. Here, it was shown that by first dividing the losses over a half-wave period into four instants,

$$P_{1,4}=8f_0\int_0^{\frac{1}{8f_o}}\pi P_{T/D,av}\sin(\omega_n t)\,dt=P_{T/D,av}\left(4-2\sqrt{2}\right)$$
$$P_{2,3}=8f_0\int_{\frac{3}{8f_o}}^{\frac{1}{8f_o}}\pi P_{T/D,av}\sin(\omega_n t)\,dt=P_{T/D,av}2\sqrt{2}, \tag{20}$$

the maximum junction temperature occurs after the third instant and the minimum at the start of the first instant. Using the fact that for steady-state operation, the minimum junction temperature of a cycle is equal to the minimum of the next cycle and conversely for the maximum junction temperature, the steady-state minimum $T_{\text{j,k}'}$ and maximum junction temperature $T_{\text{j,k}}$ can be written as function of the device fourth order thermal resistances Z_{th} and time constants τ:

$$T_{j,k'}=\frac{P_1 Z_{th}(3\Delta t)\,e^{\frac{-5\Delta t}{\tau}}+(P_2-P_1)\,Z_{th}(2\Delta t)\,e^{\frac{-5\Delta t}{\tau}}}{1-e^{\frac{-8\Delta t}{\tau}}} \tag{21}$$
$$+\frac{P_1 Z_{th}(\Delta t)\,e^{\frac{-4\Delta t}{\tau}}}{1-e^{\frac{-8\Delta t}{\tau}}},$$
$$T_{j,k}=\frac{P_1 Z_{th}(\Delta t)\,e^{\frac{-7\Delta t}{\tau}}+P_1 Z_{th}(3\Delta t)+(P_2-P_1)\,Z_{th}(2\Delta t)}{1-e^{\frac{-8\Delta t}{\tau}}}. \tag{22}$$

Subtraction of the maximum and minimum junction temperature during steady state gives the correct expression contrary to [20] for the temperature ripple:

$$T_{jk}-T_{jk'}=\frac{P_1 Z_{th}(\Delta t)\left[e^{\frac{-7\Delta t}{\tau}}-e^{\frac{-4\Delta t}{\tau}}\right]}{1-e^{\frac{-8\Delta t}{\tau}}}$$
$$+\frac{P_1 Z_{th}(3\Delta t)\left[1-e^{\frac{-5\Delta t}{\tau}}\right]+(P_2-P_1)\,Z_{th}(2\Delta t)\left[1-e^{\frac{-5\Delta t}{\tau}}\right]}{1-e^{\frac{-8\Delta t}{\tau}}}. \tag{23}$$

However, slight modifications have to be made to the average power loss computation since the conventional expression as in (6) assumes that *T2* switches exactly once during each submodule switching frequency cycle, while it switches multiple times during each cycle with a lifetime optimization controller; the device switches one time due to its carrier wave, and an amount of the total ripple n_{r} during the interchanging indices window (e.g. n_{r} equals 4in Fig. 7). As a result, the average switching

TABLE III
RESULTS OF THE ANALYTICAL MODEL WITH THREE STUDY CASES $J_{\mathrm{L}} = 6\,\%$, $8\,\%$, AND $10\,\%$

Number of submodules	P_{av} [kW]	ΔT_j [K]	
1	7.34	4.01	$J_L = 6\%$
5	1.82	0.99	
194	2.74	1.50	
1	9.19	5.02	$J_L = 8\%$
7	1.82	0.99	
192	2.74	1.50	
1	10.1	6.03	$J_L = 10\%$
9	1.82	0.99	
190	2.74	1.50	

N_s = 200. Each case shows for the selected submodule, the number of submodules with reduced junction temperature swing n_r, and the remaining unaffected submodules in the arm, the effect on average power losses on the *T2* device's and the subsequent junction temperature swing inside the device's.

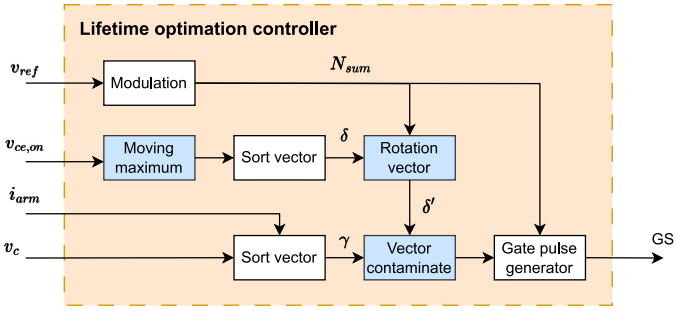


Fig. 10. Control system implementation of the lifetime optimization controller with capacitor voltage balancing. Inputs are the condition indicators $v_{\mathrm{ce,on}}$, arm current for sorting i_{arm}, capacitor voltages v_{c}, and arm reference voltage v_{ref}. The colored blocks are further outlined in detail.

power losses,

$$P_{sw} = (E_{on} + E_{off}) \frac{U_{cx} \left| I_{Tx,av} \right| f_{sw} (1 + n_r)}{U_{ref,T} I_{ref,T}}, \qquad (24)$$

increase by the factor $(1 + n_{\mathrm{r}})$. The total power losses in the selected submodule can similarly be computed using a linear summation of average power switching losses and average power conduction losses ($P_{\mathrm{c}} + P_{\mathrm{sw}}$) in the device.

A specific number of submodules (n_{r}) does not switch in this period, as the selected submodule is used instead to execute the needed switching actions. To calculate the average power losses for these submodules, a rough estimation can be made that these consist only of submodule conduction losses. In reality, there will also be some switching losses, as the lifetime optimization controller has a selection window shorter than the device heating period ($t \in [t_{\mathrm{a,i}}, t_{\mathrm{b,imax}}]$). The remaining submodules in the arm ($N_{\mathrm{s}} - n_{\mathrm{r}}$), are not affected and therefore have conventional computed power losses with a single switching action in each f_{sw} period.

Analysis has been done on an MMC configured with 200 half-bridge submodules per arm N_{s}. The DC-current equals $1.5\,\mathrm{kA}$ while the modulation index is unity, the submodule switching frequency is $150\,\mathrm{Hz}$, and AC phase-angle is zero. The device used in the analysis is the *5SNA 3000K452300* Hitachi Energy IGBT. The resulting average power losses and junction temperature swings for the selected submodule, submodules with a reduced junction temperature swing (n_{r}) as a consequence of the selection window, and the remaining submodules in the converter arm for three different J_{L} factors are shown in Table III. The results in the table are obtained through the analytical model as presented in Ch. IV.

The selected submodule experiences the highest junction temperature ripple for all three J_{L} factors. The higher J_{L} is, the larger the selection window; thus, the more submodules have a reduced junction temperature ripple. Whereas for J_{L} is $6\,\%$ only 5 submodules have a reduced junction temperature ripple, for J_{L} equal to $10\,\%$, already 9 submodules have a reduced junction temperature ripple and proves the initial assumptions of the influence of the selection window width of the number of switching actions that can be transferred.

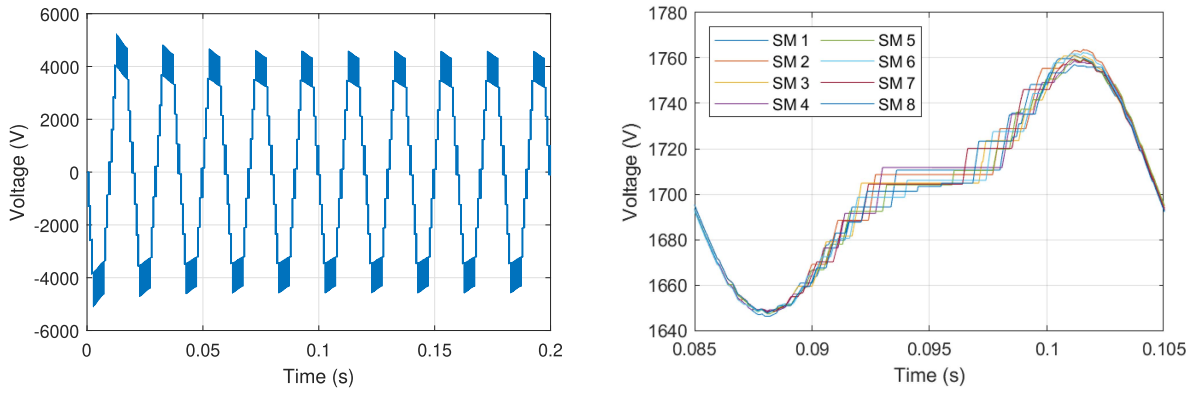
V. CONTROL SYSTEM IMPLEMENTATION

The lifetime optimization controller can be implemented using control system blocks. A general overview of the control system is shown in Fig. 10. There are four inputs in the system. First, v_{ref} is needed for modulation and defining the number of submodules that should be inserted in the arm. Afterward, the *T2* $v_{\mathrm{ce,on}}$ measurements from each submodule in the respective arm are needed as condition indicators. The arm current and capacitor voltages are lastly used for conventional capacitor voltage balancing with γ. The process of selection window determination with the highlighted blocks is briefly elaborated:

- *Moving maximum:* To show the general purpose of the lifetime optimization insertion indices, a moving maximum has been used for the measurement aggregation between the submodules. The time interval is set $20\,\mathrm{ms}$ so one period is covered in the $50\,\mathrm{Hz}$ AC-system. This short time window is justified because the modulation index is unity, and all submodules are used in the arm.
- *Rotation vector:* After δ is formed, the selected submodule position, is always located on the high-priority side of the selection window. This is only effective when B_{L} submodules have to be inserted. A rotation algorithm is applied based on N_{sum} that relocates the selected submodule to the position of N_{sum}, forming δ'. The selected submodule is thus always in the position where the ripple over the plane staircase function occurs in the selection window.
- *Vector contaminate:* The selection window from δ' is contaminated with the remaining part of the capacitor voltage vector γ before the gate pulses are generated.

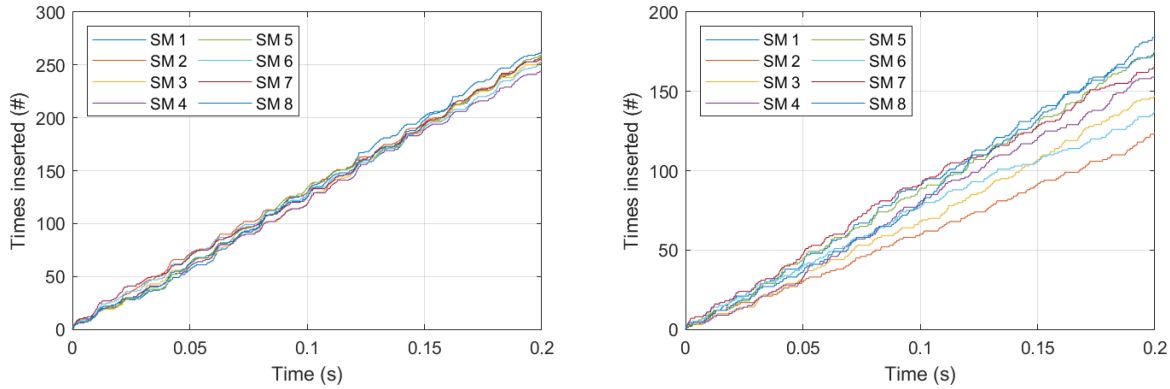
The presented control system has been implemented in MATLAB/Simulink together with a single leg of an MMC to validate the working of the proposed controller, including capacitor voltage balancing and lifetime optimization. Both arms in the leg consist of eight half-bridge submodules, and only the upper arm is modeled, including *T2* deterioration. The DC-poles are rated $8\,\mathrm{kV}$ and each submodule is rated at $2\,\mathrm{kV}$.

To mimic the effect of increasing $v_{\mathrm{ce,on}}$ during deterioration, a resistor in series to *T2* increases according to the number of instances the respective device has been switched between inserted and bypassed modes. This respective resistance R_{s}



(a) (b)

Fig. 11. Generation of the AC-phase voltage and the capacitor voltage balancing between the eight submodules. (a) Generated AC phase voltage. (b) Capacitor voltages.



(a) (b)

Fig. 12. Number of times a submodule has been inserted with two scenarios considered. (a) Capacitor voltage balancing control. (b) Lifetime optimization and capacitor voltage balancing control.

TABLE IV
LIFETIME DETERIORATION PARAMETER SETTINGS α AND β PER SUBMODULE IN THE UPPER ARM

Submodule number	α	β
1	1×10^{-6}	1.40
2	1×10^{-6}	1.00
3	1×10^{-6}	1.05
4	1×10^{-6}	1.10
5	1×10^{-6}	1.08
6	1×10^{-6}	1.10
7	1×10^{-6}	1.00
8	1×10^{-6}	1.20

equals,

$$R_s = \alpha \left(N_{sw}\right)^{\beta}, \tag{25}$$

with N_{sw} representing the number of times the corresponding series *T2* device has switched, α the deterioration offset factor, and β the deterioration scaling factor. The parameters per series resistor in the upper arm are listed in Table IV.

First, the capacitor voltage balancing and the generation of the AC-phase voltage can be seen in Fig. 11.

The capacitor voltages are seen to be balanced and follow a sinusoidal pattern. This balancing process confirms the working of the intended capacitor voltage balancing algorithm. The increasing half of the sinusoidal waveform has a more block shape compared to the decreasing half of the sinusoidal waveform because in the first half, the arm current is strongly positive such that the capacitors are charging fast, while in the second half, the arm current is only slightly negative and the capacitors are discharging slowly. In reality, there are hundreds of submodules per arm, instead of the simulated eight submodules. The simplification reduces the computational burden. A simulation case with 200 submodules per arm was performed with the analytical model developed, and the results are shown in Table III.

The evaluation of the selection window control considers two scenarios; disabling the selection window such that only the capacitor voltage balancing controller is active and enabling both controllers implying the complete presented control methodology is simulated. The number of times a submodule is inserted by both strategies is shown in Fig. 12.

According to the scenario with only having active the capacitor voltage balancing controller, the submodules are being inserted evenly over time. This confirms the philosophy of the capacitor voltage balancing controller which inserts submodules over time to balance the capacitor voltages. When the lifetime optimization controller is activated, the insertion frequency between the submodules starts to differ over time. It can be seen that submodule 1 is inserted most frequently while submodule 2 is inserted the least as expected from Table IV. In the simulation, a higher switching frequency of 1250 Hz is applied to clearly demonstrate the effect of the proposed lifetime optimization controller within a short time window. For real MMC systems, a much lower frequency (around 100 Hz) is typically used, however, the increased frequency in the simulation enhances the visibility of the controller's impact.

VI. Conclusion

The deployment of GigaWatt-scale offshore wind farms presents increasing challenges in the security of energy supply and operational flexibility, requiring innovative solutions. Traditional MMC submodule reliability approaches do not address the critical need for transmission system operators to align maintenance schedules with labor availability and unpredictable offshore conditions. This article introduces a novel control methodology that optimizes the lifetime of MMC submodule semiconductors based on which the operators may influence the timing of submodule failures. By applying a new sorting and selection principle, submodules are prioritized based on their technical condition and the system's operational needs. A unique arm operational principle is also presented, incorporating adjustable performance parameters that balance semiconductor lifetime optimization with capacitor voltage balancing. Both analytical and simulation results highlight the effectiveness of this approach, providing a powerful system for flexible maintenance planning and robust operation in large-scale offshore energy systems. The performance evaluation done by comparing with the traditional methodology conditions demonstrates that the proposed method provides operational flexibility and effectively addresses the key challenges in maintenance and system management.

References

[1] M. Eremia, C.-C. Liu, and A.-A. Edris, "Power semiconductor devices for Hvdc and facts systems," in *Proc. Adv. Solutions Power Syst.: HVDC, FACTS, Artif. Intell.*, 2016, pp. 11–34, doi: 10.1002/9781119175391.ch2.

[2] G. Lv, W. Lei, M. Wang, J. Zhao, H. Qu, and J. Cao, "Reliability and lifetime analysis considering IGBT thermal resistance performance degradation based on hydropower mission profile of MMC," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 2485–2489.

[3] B. Wang et al., "A lifetime estimation method of MMC submodules based on the combination of FEA and physical lifetime model," in *Proc. IEEE 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 1–6.

[4] J. Zhao, F. Deng, W. Hu, Y. Du, and S. Abulanwar, "Thermal optimization strategy based on second-order harmonic circulating current injection for mmcs," *IEEE Access*, vol. 9, pp. 80183–80196, 2021.

[5] P. Yu, W. Fu, L. Wang, Z. Zhou, G. Wang, and Z. Zhang, "Reliability-centered maintenance for modular multilevel converter in HVDC transmission application," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3166–3176, Jun. 2021.

[6] R. Picas, J. Zaragoza, J. Pou, S. Ceballos, G. Konstantinou, and G. J. Capella, "Study and comparison of discontinuous modulation for modular multilevel converters in motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2376–2386, Mar. 2019.

[7] F. Hohmann and M.-M. Bakran, "Improved performance for half-bridge cells with a parallel presspack diode," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3091–3097, Apr. 2019.

[8] Y. Wang et al., "Peak arm current minimization of modular multilevel converter using multiple circulating current injection," *Electronics*, vol. 12, no. 7, 2023, Art. no. 1695.

[9] G. Konstantinou, H. R. Wickramasinghe, and X. Zhang, "Loss comparison and thermal performance of modular multilevel converters under discontinuous pulse width modulation," in *Proc. IEEE 9th Int. Conf. Power Energy Syst.*, 2019, pp. 1–6.

[10] T. Bandaru, D. Samajdar, P. S. Varma, T. Bhattacharya, and D. Chatterjee, "Optimum injection of second harmonic circulating currents for balancing capacitor voltages in hybrid MMC during reduced DC voltage conditions," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1649–1660, Mar./Apr. 2020.

[11] S. Du, A. Dekka, B. Wu, and N. Zargari, "Fundamentals of modular multilevel converter," *Modular Multilevel Converters: Anal., Control, Appl.*, pp. 37–78, 2018, doi: 10.1002/9781119367291.ch2.

[12] H. Wang, G. Tang, Z. He, J. Cao, and X. Zhang, "Analytical approximate calculation of losses for modular multilevel converters," *IET Gener., Transmiss. Distrib.*, vol. 9, no. 16, pp. 2455–2465, 2015.

[13] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[14] T. Bruckner and S. Bernet, "Estimation and measurement of junction temperatures in a three-level voltage source converter," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 3–12, Jan. 2007.

[15] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Proc. 2008 IEEE Power Electron. Specialists Conf.*, 2008, pp. 174–179.

[16] *SNA 3000K452300 StakPak IGBT Module*, vol. 11. Zurich, Switzerland: Hitachi Energy, 2017.

[17] M. Asoodar, M. Nahalparvari, C. Danielsson, and H.-P. Nee, "A condition monitoring scheme for semiconductor devices in modular multilevel converters with cascaded h-bridge submodules," in *Proc. 24th Eur. Conf. Power Electron. Appl.*, 2022, pp. 1–9.

[18] S. Chen, S. Ji, L. Pan, C. Liu, and L. Zhu, "An on-state voltage calculation scheme of MMC submodule IGBT," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7996–8007, Aug. 2019.

[19] Z. Yang, J. Zhao, S. Wang, and C. Zhang, "A capacitors voltage balancing control strategy of MMC sub-modules based on dynamic threshold for PV system," in *Proc. IEEE 40th Chin. Control Conf.*, 2021, pp. 5965–5970.

[20] X. Wang, Z. Li, F. Yao, and S. Tang, "Simplified estimation of junction temperature fluctuation at the fundamental frequency for IGBT modules considering mission profile," *IEEE Access*, vol. 7, pp. 149308–149317, 2019.

[21] *5SNA 1500E330305 HiPak IGBT Module*, vol. 10. Zurich, Switzerland: Hitachi Powergrids, 2020.

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