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Defect Oriented Testing for Analog/Mixed-Signal Devices

Nivesh Rai

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Abstract

Testing of Analog/Mixed-Signal (AMS) integrated circuits (ICs) has been one of the most challenging topics in the test technology community; this is because it is very time consuming and it is hard to distinguish between pass and fail as it is the case for digital circuits. For some applications, such as automotive industry, the quality requirements for AMS ICs can be as severe as zero Parts Per Million (PPM) level. This requires, in addition of optimizing test time, also test for all possible defects in the IC. Bridges and opens are the common defects considered for AMS circuits; they are analyzed in Defect Oriented Testing (DOT) flow in order to develop appropriate test program. With high/severe quality requirements new failure mechanisms have to be considered for test purposes. Investigating such defects and their impact on the quality is important especially for zero PPM level application.

This thesis investigates the effect of dislocation defects for an NXP AMS IC which is an automotive product, manufactured in 140 nm technology. Dislocation defects cause leakage related failures while crossing a PN-junction of the device. It is very challenging in AMS testing to detect these defects. A schematic-based extraction methodology is proposed to extract the dislocation defects based on studying the cross-sections of different devices present in an IC. Using the proposed methodology for extraction, the defect list is limited to only 8% of the total active devices present in the IC. This is useful in guiding the failure analysis process and reducing the simulation effort considerably. These defects possess a high resistive signature and were simulated for different sets of resistance values. It was found that the detectability of these defects decreases as the resistance value is increased. Test selection algorithms such as 'greedy' and 'unique detects first' are used to obtain an optimal test set which is able to detect all the defects, including dislocation defects. The performance of both the algorithms in terms of test reduction is compared. The optimal test set obtained is used for validating the production data consisting of 1.3 million dies. The escaped ICs are diagnosed using a fault dictionary approach. The diagnosis results reveal that the current production data set does not suffer from dislocation defects. However, extra tests obtained for detecting dislocation defects can be kept for advanced technology nodes in the future, if these defects show up in the production environment.

TU Delft Delft University of Technology

Faculty of Electrical Engineering, Mathematics and Computer Science

Defect Oriented Testing for Analog/Mixed-Signal Devices

THESIS

submitted in partial fulfillment of the
requirements for the degree of

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in

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by

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This thesis investigates the effect of dislocation defects for an NXP AMS IC which is an automotive product, manufactured in 140 nm technology. Dislocation defects cause leakage related failures while crossing a PN-junction of the device. It is very challenging in AMS testing to detect these defects. A schematic-based extraction methodology is proposed to extract the dislocation defects based on studying the cross-sections of different devices present in an IC. Using the proposed methodology for extraction, the defect list is limited to only 8% of the total active devices present in the IC. This is useful in guiding the failure analysis process and reducing the simulation effort considerably. These defects possess a high resistive signature and were simulated for different sets of resistance values. It was found that the detectability of these defects decreases as the resistance value is increased. Test selection algorithms such as 'greedy' and 'unique detects first' are used to obtain an optimal test set which is able to detect all the defects, including dislocation defects. The performance of both the algorithms in terms of test reduction is compared. The optimal test set obtained is used for validating the production data consisting of 1.3 million dies. The escaped ICs are diagnosed using a fault dictionary approach. The diagnosis results reveal that the current production data set does not suffer from dislocation defects. However, extra tests obtained for detecting dislocation defects can be kept for advanced technology nodes in the future, if these defects show up in the production environment.

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Dedicated to my mother .....

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1 Introduction

Developments in the integrated circuit (IC) technology, with continuous scaling of transistors, have allowed fabrication of much larger electronic systems. Semiconductor manufacturing process suffer from irregularities and is not perfect. Therefore, it is required to test extensively to distinguish between the good and faulty devices. Structural testing methods have been applied successfully to test digital circuits to reduce the test time. However, production test time for analog and mixed-signal (AMS) devices is a matter of concern within the industry and still remains a challenging problem for the researchers. Defect oriented testing is an approach to test AMS ICs in a structural way.

This chapter provides some basics about IC testing and highlights the major challenges involved in AMS testing. It is organized as follows. Section 1.1 gives a brief overview about the AMS circuits. Section 1.2 discusses about the importance and need for testing in the semiconductor industry. A basic MOS IC fabrication process is also discussed as an example. Section 1.3 outlines the challenges involved in testing AMS circuits. A brief comparison of the methodologies and approaches used in digital and AMS circuits testing is done. Shortcomings of the existing testing techniques for AMS circuitries are also discussed. Section 1.4 highlights the contribution of the research work. Section 1.5 presents the organization of this thesis.

1.1 Analog and mixed-signal circuits

Digital circuits with their low power consumption and reliability dominate chip areas in a typical SOC (system on chip). However, many electronic systems still have analog components, because signals originating from physical sensors, disk drives, communication media and audio and video products are basically analog. The signals from digital circuits are also outputted in analog form with the help of displays, actuators and media devices. The use of analog and mixed-signal components such as ADC's (analog-to-digital converters), voltage references, PLLs (phase-locked loops), PGAs (programmable gain amplifiers), filters, etc becomes necessary in such cases.

1.2 Importance of testing circuits

Design, verification, fabrication process and testing are the major constituents in the development of an IC. Verification is done to check for any possible design errors. Developing a higher product quality, requires a robust design, a controlled manufacturing process and an effective test strategy. Fig 1.1 depicts the non-idealized IC realization process. In idealistic conditions, design, process and test should perfectly overlap. It essentially means that an ideal design, realized in an ideal manufacturing process should

give 100% yield. In this scenario, the role of testing would be non-existent. In a real world, all these three steps have some amount of uncertainity associated with them, which makes it far away from an idealized world. The shaded area in Fig 1.1 shows there is only a partial overlap amongst the three major steps. The figure signifies that a subset of manufactured ICs are faulty and only a subset of these are detected by the testing process. Continuous effort is being put towards reaching the near optimum and maximize the overlap of the three areas. Hence a better product quality could be attained while satisfying the economic constraints.

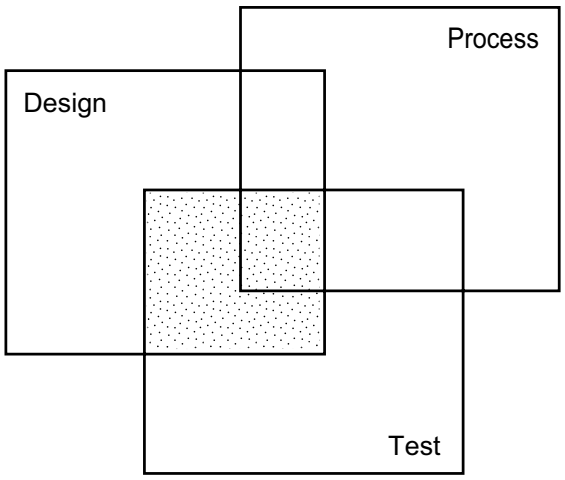


Figure 1.1: Non-idealized IC realization process [1]

Testing lets us know if something went wrong with the IC fabrication process. Diagnosing a faulty device could help us know what exactly went wrong and where. Diagnosis consists of identifying the physical location of the fault in the IC. The information extracted from diagnosing a faulty device, could also help in the alteration of process steps such that manufacturing errors could be minimized.

An effective test strategy helps in two ways, providing quality to the customer and minimizing the production cost. VLSI chips realization process contains a series of steps after the specifications are obtained from the discussion with customer. Example of specifications are power, noise, frequency of operation, range of temperature, reliability etc. Once the specifications are finalized, designers can proceed with the design of circuits. Starting from system level architecture, transistor level design is made. After design completion, the circuit realization is done with chip layout which enables the physical mapping of the design directly onto silicon. This is done by converting the chip layout to photo-masks which are used in the fabrication steps of the silicon chips. IC manufacturing process is very complicated and it would be naive to assume that even a perfectly controlled process will produce all the good devices, without any defects. Impurities in manufacturing environment, material defects, test equipment malfunctions, handling of wafers are some of the causes out of many, through which a device can become faulty. Testing therefore plays a major role in sorting out the faulty chips such that these devices are not shipped to the customer.

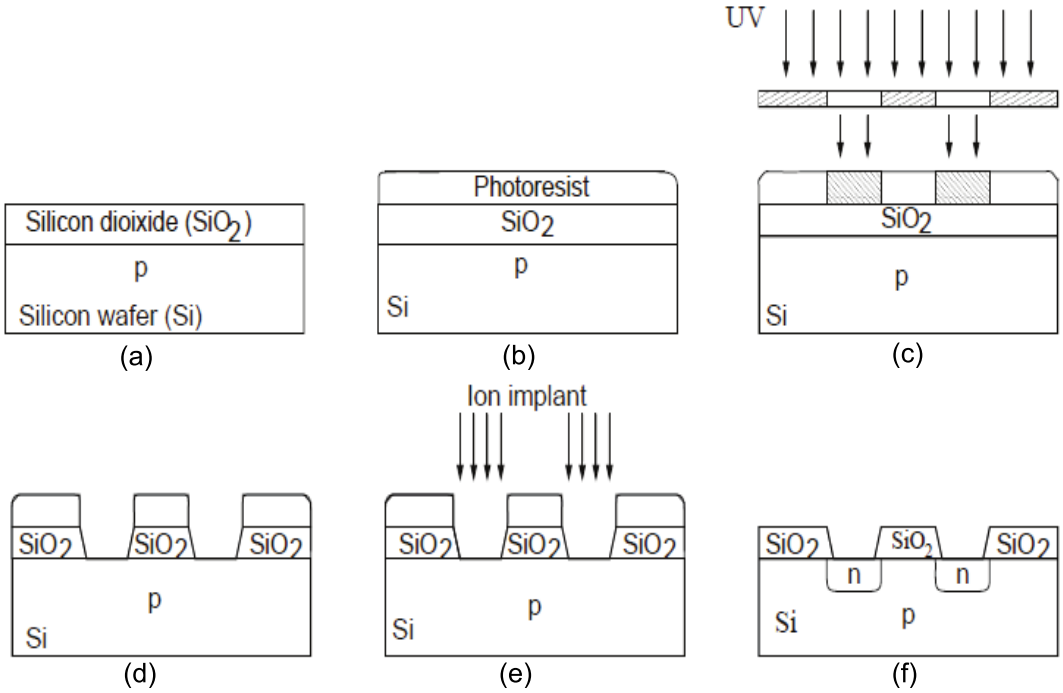


Figure 1.2: Basic MOS process [2]

IC fabrication process is very complex including a series of steps such as photolithographic printing, etching and doping steps. A basic MOS process is shown as an example in Figure 1.2. The process starts with the wafer that can be doped with the positively or negatively charged carriers. In the Figure 2(a), the wafer is doped with positively (p) charge carriers. Then, an oxide layer (SiO_2) is created on the silicon with a thermal oxidation step. A layer of negative photoresist is then coated on top of the silicon dioxide as shown in Figure 2(b). The photoresist coating is then exposed to the Ultra-Violet (UV) light through the mask patterns as shown in Figure 2(c). The photoresist areas which are not exposed to UV light are being dissolved using an organic solvent, creating patterns in the photoresist layer as shown in Figure 2(d). These mask patterns eventually define the sources, drains, channels and the diffusion regions of the transistor. The wafer is then heated to hard bake the remaining photoresist, followed by etching the oxide layer. In the subsequent step, exposed areas of silicon surface are doped either by ion-implantation or diffusion process to form an N-well. Finally, the remaining photoresist layer can be stripped using special chemical solvents as shown in Figure 2(f). An IC manufacturing process contains many such steps of photolithographic printing, etching, masking, and doping for its complete fabrication.

Actual fabricated ICs suffer from many non ideal physical effects that could not be entirely controlled by the semiconductor manufacturing process. There might be defects due to photolithographic process, doping variations, underetching or overetching of vias or maybe even due to the defects which are stress induced, such as the dislocation defects. Analog-mixed signal ICs are very sensitive towards the process variations. These

variations might arise due to non-uniform doping levels, imperfect or rounded metal tracks, or there might be slight shifts in photolithographic masks alignment. In these conditions, circuit might still be fully functional but it may fail some required specifications due to some parasitics introduced in the signal path. This is also the reason, for the exhaustive testing of AMS ICs to prevent against defects which might not necessarily be catastrophic but may have profound impact on the signal characteristics of the circuit.

1.3 Analog/Mixed-Signal test challenges

Test cost for Analog/Mixed-signal ICs is a growing concern within the industry [3]. Test time split up for system-on-chip device for mobile phones is shown in Figure 1.2. As can be clearly seen, a huge chunk of the production test cost comprises of the AMS/RF testing times.

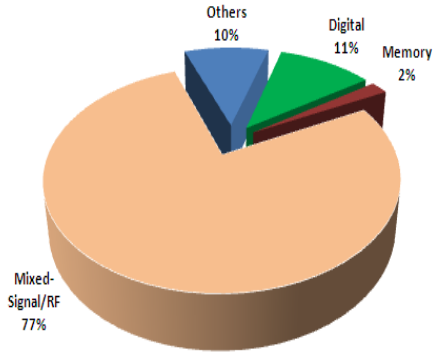


Figure 1.3: Test times per circuitry type, adopted from [3]

The main problems associated with AMS testing can be summarized as follows:

- Digital circuits enjoy the clear distinction between pass and fail, whereas the pass and fail boundaries for AMS circuitry is rather hazy. The continuous nature of the output values of the AMS circuits makes them more susceptible to defects and difficult to model. Therefore effective test procedures are needed to discriminate between various faulty and the non-faulty conditions.

- Digital DFT (Design for Testability) techniques simplify the boolean relationships between input and output in digital circuits to reduce test complexity. Structural DFT techniques when applied to AMS domain could not enjoy much success because of the lack of ability to correctly model circuit's performance.

- Analog systems are often non-linear and their performance strongly depends on circuit parameters. Process variations within allowable limits can also cause unacceptable performance degradation. Deterministic methods for modeling such variations are often inefficient.

- For many AMS circuits, test program development and debugging time takes a considerable amount from time-to-market. There are many automatic test pattern

generation (ATPG) tools that simplify the task of formulating the tests for digital circuits. These generated tests could be tested on various levels such as register transfer level (RTL) software descriptions, gate level and even on the FPGA (field programmable gate array) prototypes. This helps in validating the tests and design upfront, even before the first silicon is out. ATPG tool support is much less developed for AMS circuits and may require much iterations between design and test to reach the goal of realizable testable design, meeting the desired specifications.

- For the testing of digital parts in an IC there are widely accepted fault models, which greatly reduce the testing time. Use of scan chains and built-in-self-test techniques are mature in the arena of digital circuits and further bring down the test cost. However, the use of such fault models is questionable in the analog domain. In the absence of acceptable fault model, test generation has been ad-hoc and testing has been largely functional. Effectiveness of test sets of a new design henceforth, depends largely on the designer's and test engineer's experience in the AMS domain.

- AMS testing also suffers from automatic test equipment (ATE) related issues. For example, when noise level in test environment is not acceptable, complex shielding techniques are required. Furthermore, the integrity of test depends on interface, interconnections, probe card, etc.

The problems mentioned above are the main contributors to the long testing times of AMS circuits. These long testing times together with the expensive test equipments, production personnel and the basic operating costs makes AMS testing an expensive business and take a large fraction of production test time [4]. Techniques such as multi-site testing are used successfully to share the testing equipments with multiple devices at a time, but they are reaching their limitations and novel directions for test time reduction need to be investigated. Testing digital ICs in a structured manner is much matured in industry, while testing AMS ICs structurally is still evolving [5]. Defect oriented testing (DOT) is a suggested alternative to test the AMS devices in a structured manner. Although the methodology from digital testing differs slightly, generally the flow contains defect extraction, fault modeling and simulation and finally the tests are applied.

Typically, DOT process includes the defects which are very common such as, shorts and opens. Since, the DUT is an automotive product with very high quality requirements (zero PPM), other failure mechanisms such as dislocations also need to be investigated. Dislocation defects may not result in a complete failure of the IC, but may pose a reliability risk (i.e, the IC fails over time). It is typically very challenging in AMS testing to detect these defects. To the best of our knowledge, none of the existing research studies have addressed the issue of extracting and analyzing the behaviour of these defects.

1.4 Contribution of thesis

This thesis work analyzes a new class of defects called dislocation defects using the defect oriented testing framework. This research work is carried out on one of the existing

AMS product of NXP semiconductors, which is already in volume production. Along with dislocation defects, simulation results of the shorts (bridges) from the work done previously at NXP semiconductors are also analyzed in context with the dislocation defects. Complete methodology for the extraction of dislocation defects is developed studying the cross sections of all library models present in the process design manual. Extracted dislocation faults are then simulated by DOTSS (Defect Oriented Test Simulation Software) framework, used by NXP. Different sets of resistance values are used to analyze the variation of dislocation defects with resistance.Various test selection algorithms are used to choose the optimal test set to cover all the dislocation defects in the existing product.

Finally, the measurement data of 1.3 million dies from the production testing is analyzed to check if the device under consideration suffers from the dislocation defects. This is done through various methods of comparing the signature of simulations with the signature of failing dies. The results show that the dislocations defects require extra tests for detection. However, no such tests are needed for the current production data lot and these tests can be used in the future, if the dislocation defects become more prominent due to process variations. To summarize, the main contributions of this work can be specified as following:

1. A schematic-based extraction methodology is developed to extract the dislocation defects from the DUT. By using the proposed approach for extraction, the defect list can be limited to only 8% of the active devices. This helps in reducing the simulation effort considerably and guiding failure analysis to appropriate locations.

2. The dislocation defects have a high resistive signature and cause leakage related failures. These defects are simulated across various resistance values and the effect of resistance values on the detectability of these defects is analyzed.

3. The performance of various test selection algorithms are compared to optimize the test set obtained for detecting dislocation defects.

4. A fault dictionary based approach is used to diagnose the escaped ICs for dislocation defects. A dictionary based approach uses the simulation results of the defects and compares the obtained signatures with the faulty ICs. This approach is further refined by incorporating the calculation of impact factors for effective diagnosis.

1.5 Organization of thesis

The concept of inductive fault analysis (IFA) technique for making more realistic fault models is presented in chapter 2. This realistic fault model development originating from IFA forms the basis for defect oriented testing. This chapter also briefly describes the IC under consideration. Defect oriented test methodology and its utilization for reducing test time, increasing fault coverage and diagnosis of defective devices is discussed.

Chapter 3 presents the details about the defect extraction process for shorts and dislocation defects. A parasitic capacitance extraction approach is used for the extraction of shorts/bridges. The physical origin of dislocation defects and their impact on device

characteristics is also discussed here. Extraction of all possible dislocation defects from device models is done after analyzing the device structures from process design manual. Finally, all the dislocation defects are listed after flattening the netlist hierarchy.

Chapter 4 presents the analysis of the simulation results of dislocation defects for four sets of resistance values. This chapter also presents the details of test selection process utilizing the simulation results for shorts (bridges) and dislocation defects. This test selection process is done with the help of algorithms like, 'greedy' and 'unique detects first'. The results for the both the approaches are compared.

Chapter 5 presents the validation of the reduced test set with production data. A brief survey of different diagnostic approaches for AMS circuits is presented. An impact factor based technique is used to match the signature of faulty chips which could not be identified using the reduced test set when only the shorts were considered as faults for the existing design. Chapter 6 presents the conclusion of the project work.

2 Defect Oriented Testing

Defect Oriented Testing (DOT) is an approach to test Integrated Circuits (ICs) in a structural way. This chapter presents an overview about the Defect Oriented Testing flow. For the successful application of DOT, defect list used in fault simulations should accurately reflect process defects occurring in a real environment. Inductive Fault Analysis(IFA) is an approach to predict all the faults likely to occur in an IC. Given an IC layout, spot defects are generated and randomly sprinkled on the IC to obtain the defect list. DOT approach utilizes layout/schematic details to generate realistic defect list but takes a slightly different approach from IFA. Defects are not sprinkled uniformly over an IC, instead values of extracted parasitic capacitances or resistances are extracted from the layout to generate a weighted defect list. Functional approaches to test modern ICs lag significantly behind in terms of product quality and economics. Defect Oriented Testing has a significant role to play in semiconductor industry to realize the objectives of high product quality and low test costs.

This chapter is organized as follows. Section 2.1 presents an overview about the defect-fault relationship. This section provides the basic understanding about the defects that are considered in IFA analysis. Section 2.2 presents the details about the IFA methodology. Various steps involved in the IFA procedure are explained. Section 2.3 presents an example study to compare the IFA and schematic-level based fault simulation approach for a mixed signal IC. Section 2.4 explains the DOT framework used in this thesis. Various steps involved in the DOT setup are presented. Potential utilization of DOT for defect coverage improvement, test optimization and electrical failure analysis is discussed briefly.

2.1 Defect-Fault relationship

The IC fabrication process involves a series of basic processing steps performed on a batch of wafers. In [6], it has been summarized that the outcome of a manufacturing process is mainly dependent on three major factors: the process control parameters, IC layout and some random environmental variations, called disturbances. The control of a manufacturing process consists of a set of parameters that should be manipulated to achieve the desired changes in the fabricated IC structure. Examples of control parameters include process equipment settings like temperature, step duration, gas pressure, etc. The layout of an IC can be described as a set of masks distinguishing transparent areas from opaque areas at each process step. The disturbances are environmental factors that can influence the end result of a manufacturing operation. These manufacturing process disturbances are studied in greater details in the works of [6][7]. Some of the example disturbances are: human errors and equipment failures, instabilities in process conditions, material instabilities, substrate inhomogeneities, lithography spots,

etc. From an IFA perspective, it is important to know that all these disturbances do not affect IC performance equally. The disturbances that deform the IC can be grouped among different deformation classes. All process disturbances can be categorized into electrical and geometrical deformations [6]. For example, a contamination (disturbance) on the wafer causes a metal line break (deformation), which falls in the category of geometrical deformation. Similarly, a temperature variation (disturbance) during gate oxide formation can cause a shift in threshold voltage (electrical deformation).

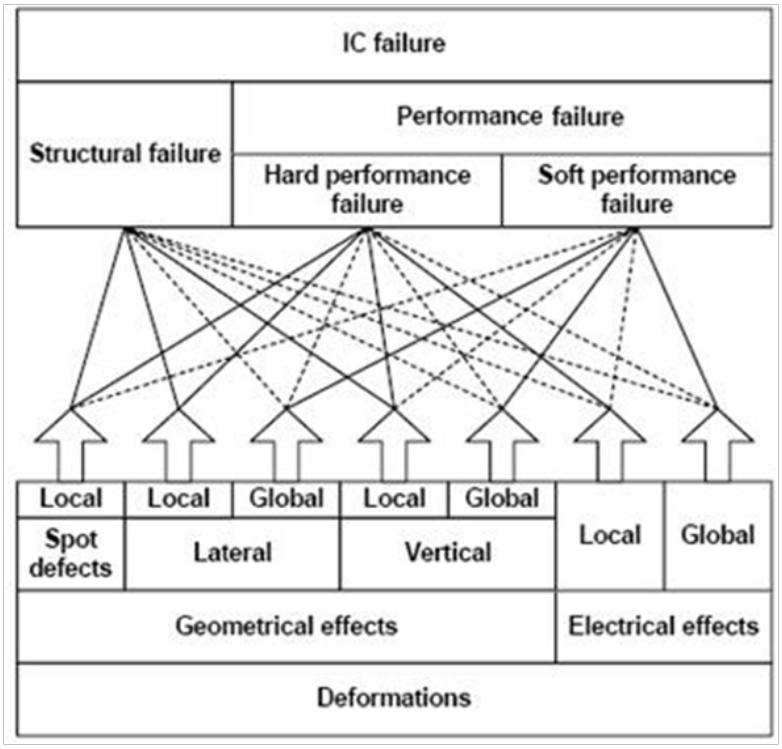


Figure 2.1: Relationship of manufacturing process deformations with IC faults [6]

Figure 2.1 shows the classification of different deformations and their relationship with corresponding IC failure mechanisms. The lower half describes the physical phenomenon responsible for yield loss and the upper half shows the fault classification (structural and performance faults). Geometrical and electrical deformations could influence the IC locally or globally. Local effects indicate that the parameters influencing IC performance limit to a region smaller in comparison to the total area of an IC. All deformations that affect all IC elements in the same way can be termed global. Each physical deformation (geometrical or electrical) can cause different kind of faults, but some faults are more likely (shown with solid lines) than others. IC faults can be classified into structural and performance faults. Structural faults affect the topology of circuit or electrical diagram representing an IC. In the case of performance faults, IC topology remains unaffected, but some IC performance parameters such as critical path delay, dissipated power, etc. may fall out of tolerance limits. For an in-depth discussion of IC faults and physical deformations the reader is referred to [6]. As could be seen from

the Figure 2.1, soft performance failures are more likely to be caused by global effects. Likewise, structural or hard performance failures are more likely caused by spot defects. Since, global deformations affect large parts of wafer, they can be detected early in a production testing environment. In addition, major process errors causing global defects are kept well under control in a mature manufacturing process. Hence, IFA based fault modeling and testing takes only local deformations or defects into account.

2.2 Inductive Fault Analysis

The field of Inductive Fault Analysis got developed in 1980's. In one of the published study [8], it has been suggested that the layout level information should be taken into account for fault model development. It was argued that stuck-at fault models are not sound enough with the increasing chip density. In an analysis of 4-bit microprocessor chips it was found that most of the physical failures consist of shorts and opens. The gate-level fault model could not appropriately account for these common defects and the layout level details were utilized to facilitate the testing procedures. In [9], it was demonstrated that the complete understanding of the effect of physical failures in ICs is necessary to design appropriate testing methods and circuitry to tolerate them.

The early works of [8][9][10], on the subject of utilizing actual manufacturing process defects to determine circuit level faulty behavior, forms the core of Inductive Fault Analysis procedure. Shen et al., have demonstrated an extensive treatment to the subject of Inductive Fault analysis and the whole methodology is derived for MOS Integrated circuits. The major steps involved in IFA procedure are [11]:

- Generation of realistic physical defects utilizing the statistical data from manufacturing process.
- Extraction of circuit level faults originating from these defects.
- Classification and ranking of faults according to their likelihood of occurrence.

Hence, an IFA procedure is capable to generate fault model and a ranked fault list utilizing the information from layout, technology and fabrication process characteristics. IFA differs from the approach in which a fault model is defined at the logic level of an IC. The most well known example of such a model is the stuck-at model which assumes that a node is stuck at VDD (supply voltage) or GND (ground) levels even if no such lines are in the neighborhood. Higher level fault model is derived examining the defects at lower (physical) levels. In other words, defects are induced in a circuit by simulating (or mimicking) actual defect creation process. Hence the word "inductive", which essentially means that the higher level fault models are induced from lower level defects.

The manufacturing defects occurring in an IC fabrication process and their impact on performance strongly depends upon IC design and layout. IFA also has the potential to identify design areas that are difficult to test. Hence, utilizing the information from IFA, measures for robust design and yield improvement can be adopted. The following subsections presents an overview about the important considerations of the IFA methodology such as defect sensitive layout, defect generation and implementation of fault extractor.

2.2.1 Defect sensitive layout

IC layout contains vital information for realistic fault extraction, modeling and yield prediction. Size of a defect and its position in the IC are the key parameters determining whether it is catastrophic or not. The concept of critical area utilizes these parameters and is defined in [12]. The critical area has been defined for a defect of radius R, as the area on the IC on which a center of a circular defect must lie for a fault to occur, which is shown in Figure 2.2. The size and the probability of defects is characterized by defect density distribution (DDD). For a fabrication line, DDD data can be obtained for each layer and defect types. DDDs provide the information about the probability of a defect in a certain layer with respect to other layers and the relationship of defect probability in a certain layer to the size of defect [1]. Most probable defect radius can be found if the defect density distribution is given. Thus, the critical area can be computed for a given defect radius. For a given IC, if the critical area increases, the yield decreases. This information can be applied to minimize the critical area of an IC. For this purpose, IFA can be used to find layout or design related yield sensitivity.

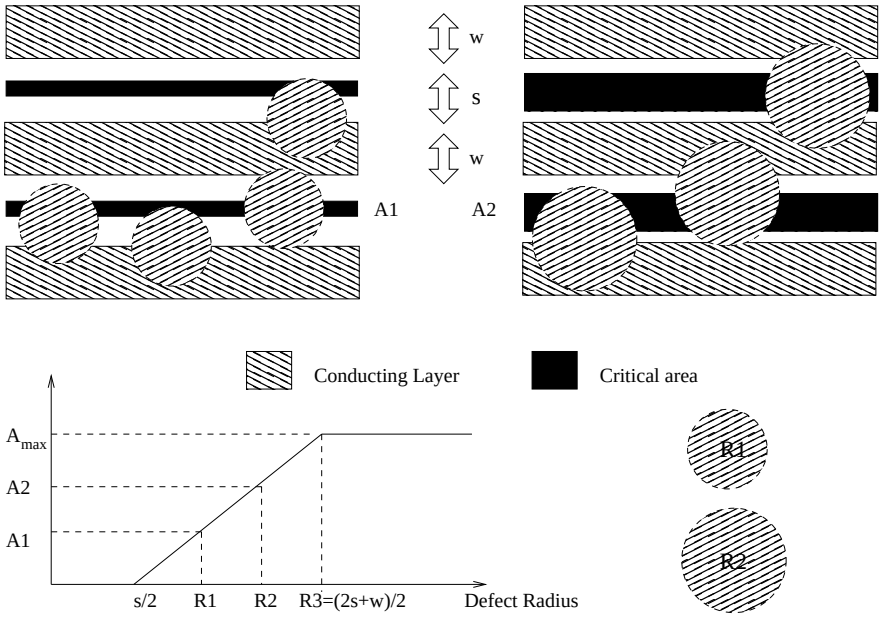


Figure 2.2: Critical area as a function of defect radius [1]

Amount of critical area is directly dependent on the spacings in the layout. Techniques such as wire spreading can be used to minimize the critical areas in an IC layout and reducing the potential for short-circuit faults. Figure 2.3 shows the reduced critical area after wire spacing for a given defect diameter. These techniques can ramp-up the yield significantly.

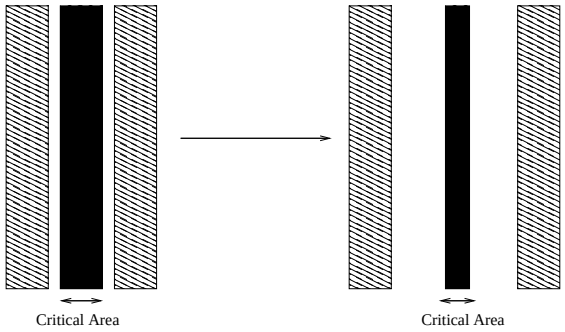


Figure 2.3: Reduction of critical area using wire spreading

2.2.2 Defect generation and analysis

Given an IC layout, a list of point defects can be generated using the information obtained from manufacturing process. A point defect can be interpreted as a missing material or an extra material for a particular layer. Two main attributes for statistical characterization are: defect density per unit area and probability density function of defect sizes. In the implementation of the defect generator of [11], it was assumed that defects distribute themselves uniformly over an IC. Defects could be assumed either round or square. Any probability density function can be used for generating defect sizes. Therefore, the IFA approach can be customized to generate defects for a particular fabrication process if the defect statistics are known. Figure 2.4 illustrates the concept of randomly generated defect. An appropriate probability density is used to generate the coordinates (x and y) and the radii of defect.

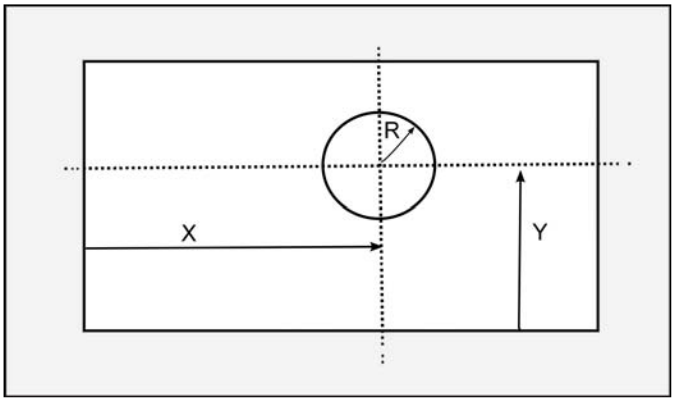


Figure 2.4: Random defect generation [11]

The generated defect is then examined to have an effect on the circuit level. The size and location of the defect play a major role in determining its significance at structural level. A significant defect at structural level may or may not be significant electrically (circuit level). For example, a pin hole defect in oxide layer is an apparent defect at structural level, but it may not have any effect on circuit level, if no conducting regions are present above it (to create a short).

After defect extraction circuit level faulty behavior can be extracted from the identified significant defects. The fault extraction is very similar to standard circuit extraction process. Circuit extraction provides the circuit netlist, given a layout of the circuit. Similarly, a fault extraction process uses both the layout and fault-free circuit and produces the faulty netlist. The layout used in the fault extraction process is the modified layout with an embedded defect. Circuit faults could then be grouped and ranked. A circuit fault can be the manifestation of one or more defects. Likelihood of a particular circuit fault is dependent on the number of defects causing it. For example, a fault caused by manifestation of large number of defects is much more probable to occur than the fault caused by relatively few number of defects. Thus, the circuit faults can be ranked based on their likelihood of occurrence and a ranked fault list can be obtained.

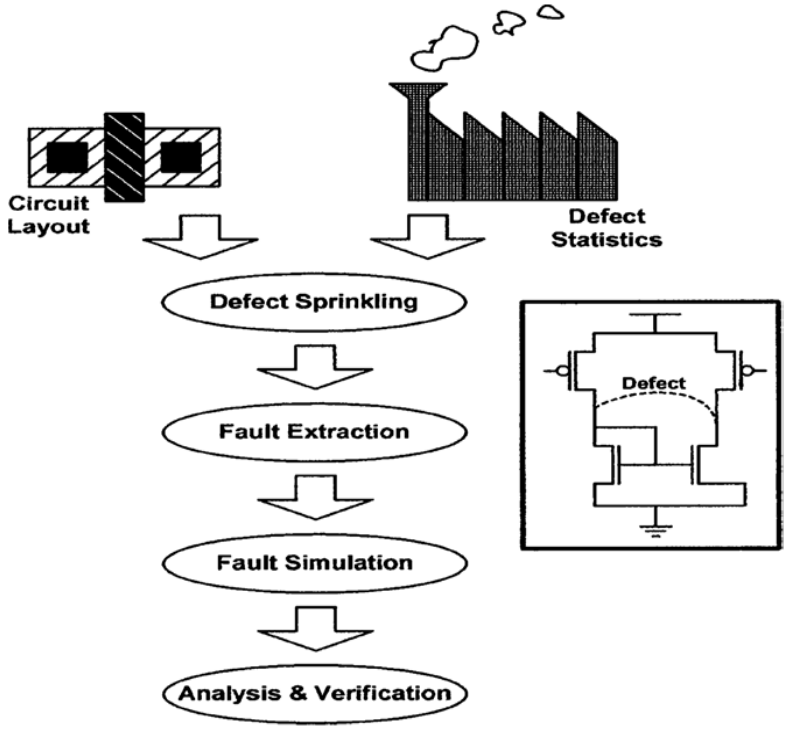


Figure 2.5: Graphical representation of complete IFA procedure [1]

2.2.3 Summary

The layout of a circuit significantly influences the faulty circuit behavior. IFA is based on the assumption that the defect probability at a particular site is a function of the local layout characteristics and distribution mechanisms observed during manufacturing process. Figure 2.5 summarizes the important steps involved in the IFA procedure. IC layout and defect statistics from the manufacturing process form the inputs. CAD tools such as VLASIC [13], CARAFE [14], etc. can be used to sprinkle these defects onto the layout. These defects are extracted and their circuit behavior is modeled for fault

simulation. The fault simulation results can be used to guide Design for Testability (DFT) solutions, building fault tolerance, etc. Finally, the verification of simulation results can be done with silicon data.

2.3 IFA versus schematic-level based fault simulation

This section presents a case study from [15], where two fault list generation approaches: IFA and Schematic-level based are compared and evaluated for a mixed signal IC. Qualitative results of the founding are presented, without delving much into the quantitative results. The circuit used in this study is switched current memory cell. Implementation of IFA is carried through VLASIC (VLSI Layout Simulation for Integrated Circuits) [13] which is able to recognize analogue layouts. It performs its circuit analysis in Monte-Carlo fashion to place random spot defects on IC layout. Figure 2.6 provides an overview of the basic steps in the fault extraction process using VLASIC.

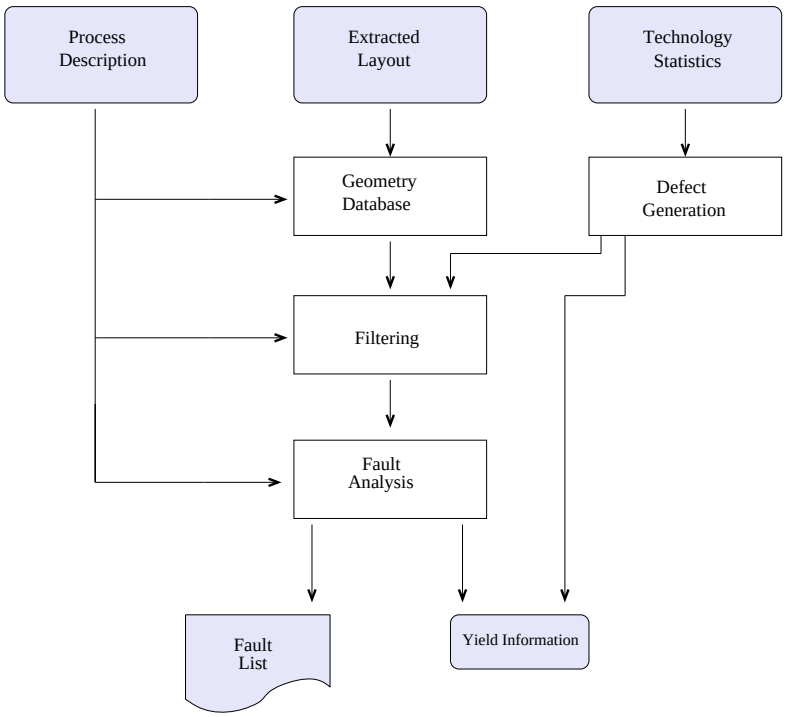


Figure 2.6: Important steps involved in implementation of VLASIC [15].

Process description, extracted layout and technology statistics forms the input to the extraction flow. Process description has the required information about the physical layers, contacts, connectivity and the potential faults that may occur. Extracted layout describes the design on physical level and the defect density distribution could be obtained from technology statistics. The tool performs the analysis at each layer by extracting information about different defect densities, defect size and defect placement to model realistic defects in the IC. Defect extraction is followed by a filtering step, where

defects that do not cause any IC faults are filtered out. Finally, a weighted fault list is created with circuit net names attached to each fault. A resistive level fault model is used to simulate the faults.

Resistance (R) of the defect is modeled by equation 2.1 and the different parameters involved are calculated from process defect statistics. Resistivity (ρ) can be found from the layers that compose the defect. Figure 2.7 shows the transistor level fault model to simulate open and short-circuit faults. This model accommodates only two opens and 3 shorts for each transistor. The short resistance value is usually in the low ohmic range and was chosen as 100 Ohms. The open circuit resistance value is in the high ohmic range and is chosen to be 10 MOhms.

$$R = \rho\frac{L}{A} \approx \rho\frac{L_{min}}{Diameter.Thickness} \tag{2.1}$$

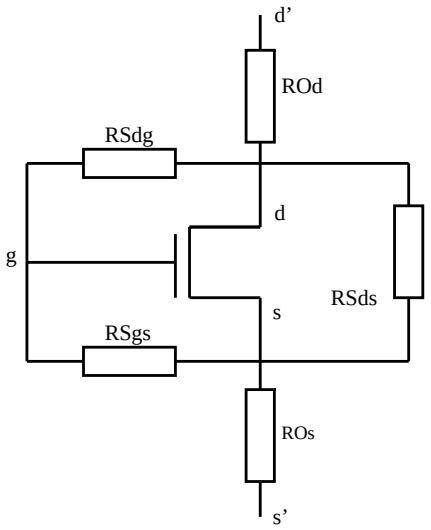


Figure 2.7: Transistor level fault-model with resistors RO to model open-circuit faults and RS to model for short-circuit faults [15].

Table 2.1 adopted from [15] presents the comparison of two fault simulation approaches. In total, 28% of the physical faults are not represented with the transistor level fault model. Fault coverage based on IFA analysis is 84% for the unweighted (all faults with equal weight) case and 87% for the weighted case. The fault coverage results for the transistor level fault model are much lower with 61%. Thus the fault generation approaches have significant impact on the fault coverage and it was concluded that "Transistor level fault models are not descriptive enough for mixed-signal fault simulations" [15].

2.4 Defect Oriented Test framework

Figure 2.8 shows the Defect Oriented Test (DOT) framework used for the thesis project. The DOT approach used for this project also targets realistic faults, but details differ

	IFA Fault Simulation Route	**Transistor-Level Model Fault Simulation Route**
Information from CUT	Layout, Schematic and Process Information	Only Schematic/Netlist.
Components/Structures considered for Defects/ Faults	Transistors, Capacitors, Resistors, Interconnect (Layers, Vias, Contacts)	Only Transistors.
Fault Models used	Open/short model with statistically modeled fault resistance values (single layer, intra layer, contacts, vias)	Open/Short model with predefined, fixed resistance values.
Fault Weighting	Faults weighted according to statistical probability occurrence	All Faults weighted the same.
Fault List Generation effort	Complex tool set-up and time consuming	Easy to generate
Interpretation of Simulation Results	Quantitative as well as qualitative information	Only qualitative results.
Fault Coverage	Unweighted **84%** & Weighted **87%**	Shorts **72%**, Opens **31%** & Total **61%**

Table 2.1: Comparison between IFA based fault simulation and the transistor-level model fault simulation [15]

slightly compared to the IFA approach. In an IFA based approach defects are generated randomly and then sprinkled onto the layout. The circuit level faulty behaviors are then obtained for the corresponding defects and a fault list is obtained. DOT approach utilizes a layout or schematic based flow to extract the defects in the DUT. For extracting bridging defects, value of parasitic capacitance is utilized to calculate the adjacency between two conducting layers. Thus, the probability of shorts between conducting layers is derived and a weight can be associated with each defect. Hence, a weighted defect list for shorts can be obtained. A schematic based flow is used to extract dislocation defects based on the susceptible PN junctions identified from the process design manual. This section presents the overview of the whole flow and the details of the Device Under Test (DUT). The main steps of the flow include:

- Defect extraction from layout or schematic.
- Generation of defect list.
- Test program generation.
- Defect modeling and simulation.
- Generation of defect simulation database.

The DUT analyzed in this project work is an automotive AMS product, already in volume production. This product is a CAN (control area network) transceiver chip and

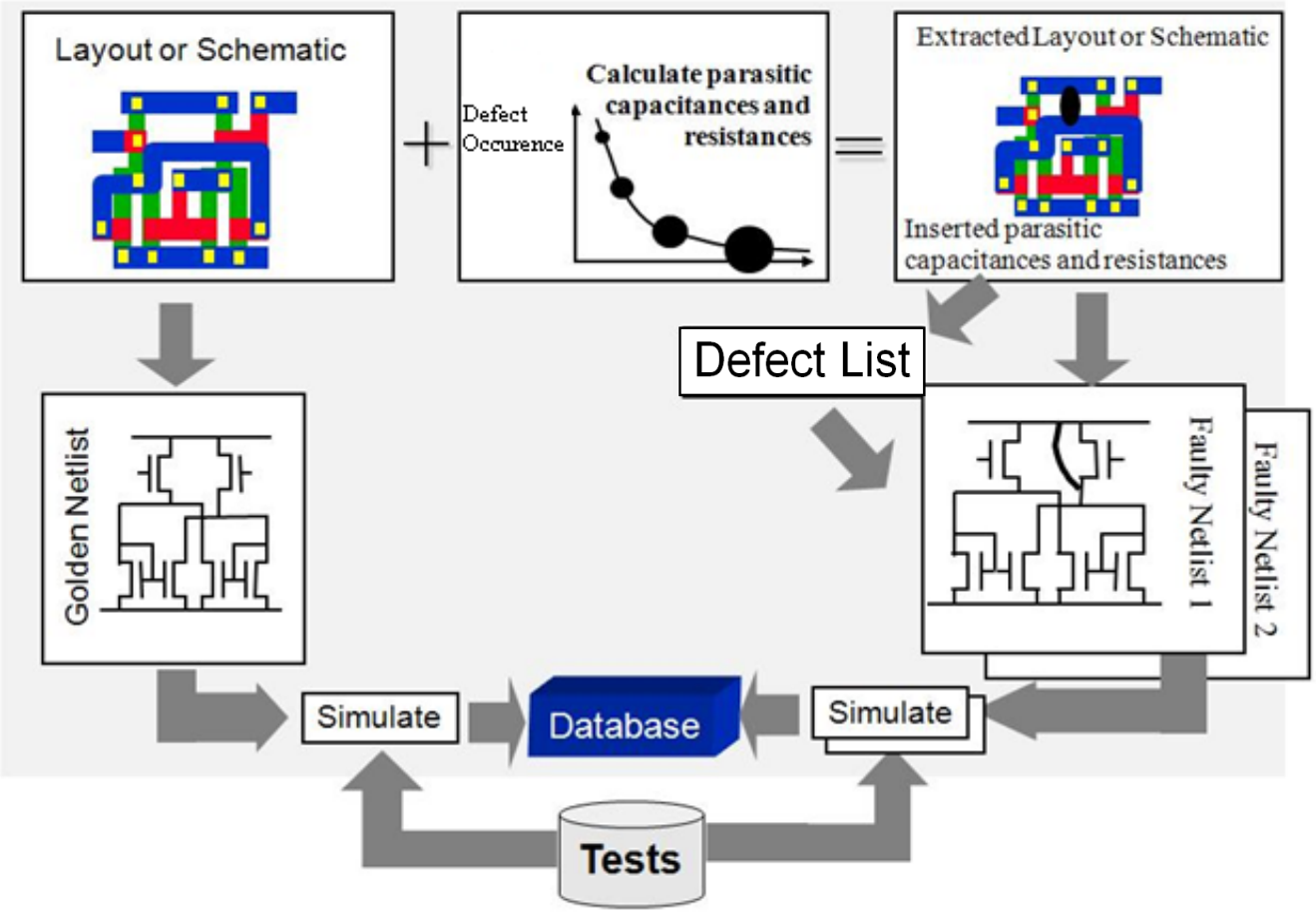


Figure 2.8: Defect Oriented Testing Flow

has zero defects quality requirement. It is manufactured in BiCMOS-DMOS (BCD) process. Figure 2.9 shows the block diagram of the chip. This product is primarily intended for low speed applications in passenger cars. The operating voltage range is from -5 to 40V and the temperature specifications varies from -40 to 125^o C.

Since the product is very mature, the defect statistics for the product are known from the production. The production data suggests that shorts are the most likely defects followed by dislocations. Open-circuit faults are very rare, because via doubling is used to make interconnection between layers. In this technique a redundant via is inserted to enhance the via yield and reliability. Defect extraction is done with the help of an extraction tool developed at NXP semiconductors. Defect extraction for shorts is layout based and is achieved by calculating parasitic capacitance and a weighted fault list is obtained. Dislocation defect extraction is schematic/netlist based. Details of defect extraction for the DUT are presented in Chapter 3. Test program generation is achieved by modeling production tests in the PSTAR[1] format. The test program

[1]Inhouse analog Simulator of NXP

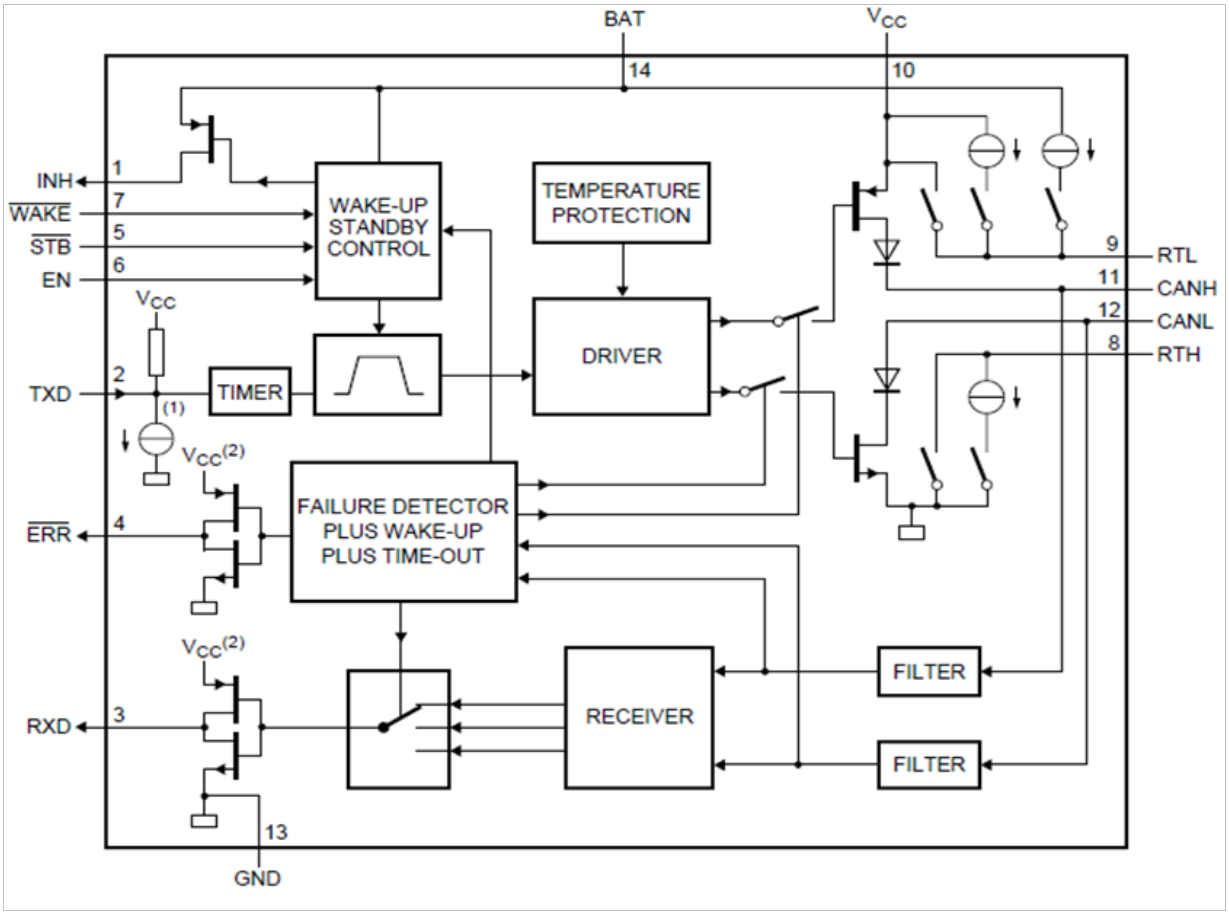


Figure 2.9: Block diagram of the chip

generation is very tedious task and requires extensive manual effort to model production tests accurately. Finally, the faults are simulated using the generated test set and the fault simulation database can be prepared. Data thus obtained for the simulated faulty netlist could be used for the generation of detection matrix. The detection matrix thus generated, can be used for various purposes:

- Defect coverage improvement.
- Test set optimization.
- Electrical failure analysis.

Figure 2.10 shows an example of a detection matrix. The rightmost column contains the defect list. The detection matrix shown contains sixteen tests. “D” represents the defect detected by a specific test. It can be seen that the third defect is missed by all the tests. One of the advantage of the DOT process is that exact location of the missed defect can be identified. Thus suitable tests can be added which are capable to detect the defect. This detection matrix can also act as a guide to adopt suitable DFT measures

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	total	Defects
D	D				D			D	D				D		D	7	bridge__NET18.AN2_I4__C__1
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__2
																0	bridge__C__VDD!__3
		D		D	D	D	D			D		D	D	D	D	10	bridge__NET18.AN2_FIRST__A__4
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__5
						D								D		2	bridge__A__VDD!__6
D	D			D	D			D	D			D	D		D	9	bridge__Z__NET18.AN2_I4__7
D	D			D	D			D	D			D	D			8	bridge__Z__VDD!__8
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__9
		D		D	D	D	D			D	D	D	D	D	D	11	bridge__TUSSEN__NET18.AN2_FIRST__10
		D	D	D		D				D	D	D		D		8	bridge__TUSSEN__VDD!__11
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__12
D	D	D		D	D	D		D	D	D	D	D	D	D	D	14	bridge__NET18.AN2_I4__TUSSEN__13
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__14
		D	D	D		D				D	D	D		D		8	bridge__TUSSEN__VDD!__15
		D	D		D		D			D	D		D		D	8	bridge__NET18.AN2_FIRST__B__16
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__17
											D					1	bridge__B__VDD!__18
D	D			D	D			D	D			D	D		D	9	bridge__Z__NET18.AN2_I4__19
					D								D		D	3	bridge__Z__0__20

Figure 2.10: Example of a Detection Matrix

for improving the quality level of the design. In the work of [16], the DOT approach was applied to improve the fault coverage of a mixed-signal block in an industrial IC. Tests were added appropriately by utilizing the information from extensive DOT simulations so that a high fault coverage could be obtained. Detection matrix can also be used for optimal test selection and electrical failure analysis. Test optimization can be achieved by selecting the minimal test set covering all the defects. Electrical failure analysis can be done by matching the physical signature of faulty IC with the simulated signatures in the generated database. These topics will be covered in greater depth in Chapter 4 and 5.

3 Defect Extraction

The Analog/Mixed-Signal (AMS) product under analysis is susceptible to two major kinds of faults: shorts/bridges or dislocations. Defect extraction is the primary step in the Defect Oriented Testing (DOT) flow. This chapter presents the details about the defect extraction of shorts and dislocations. Defect extraction for shorts is done using a layout based extraction flow. A weighted defect list for shorts is created based on the value of capacitance value between two conducting layers. A schematic-based extraction methodology is proposed for the extraction of dislocation defects by identifying hierarchical net names of each defect. The methodology parses the schematic (netlist) and locates dislocation defects according to pre-determined rules. The cross-section of different devices from the design manual of a process technology are studied and the possible dislocation spots related to PN junctions are listed in a rule file.

This chapter is organized as follows. Section 3.1 presents the extraction flow for bridging defects. Different steps involved in the parasitic capacitance based extraction approach are discussed. Section 3.2 introduces the dislocation defects. Dislocation defect types, origin and impact of these defects on circuit performance is presented. Section 3.3 presents the prior work done to understand the dislocation defects. Section 3.4 presents a novel methodology to extract dislocation defects based on schematic-level analysis.

3.1 Extraction of bridging defects

There are two kinds of bridging defects that are extracted for the AMS product under analysis: intra-layer bridging defects and the inter-layer bridging defects. Spot defects are the primary cause for catastrophic faults such as shorts and opens. This section mainly focuses on the extraction of short-circuit defects. These defects can be modeled as being circular in nature, present on different layers with a diametric distribution. The involved layers can be metal-metal or metal-polysilicon. There are 3 metal layers present in the Device Under Test (DUT).

Bridging defects caused by process errors are usually three dimensional in nature, but modern chemical mechanical polishing steps limits their effect primarily to the mask layer in which they occur [17]. Due to huge numbers of wiring elements and complex routing, it is not feasible to test for all the possible bridging faults between all pairs of nets present in the design. Hence an efficient and effective framework is required to determine which nets are physically adjacent to each other and which of them are most likely susceptible to bridging faults.

One of the ways for realistic extraction of bridging faults depends upon critical area and defect size distribution. The concept of critical area is explained in section 2.2.1. The critical area is directly proportional to the defect size. The larger the defect size, the larger the critical area. Exact calculation of critical areas is a costly process for typ-

ical layouts. This is primarily due to the assumption of circular defects, which implies Euclidean polygon expansion to compute the critical area between two polygons [18]. Computation of weighted critical area further complicates the matter by computing critical area as a function of defect size and then convolving the result with defect diameter distribution. Researchers have invested a significant amount of effort to calculate exact or near-exact critical areas [19]. In practice there is little need for it, since the defect diameter distribution is poorly characterized, varies across different manufacturing units and changes over time [18].

An alternative to a critical area based extractor is to use a coupling capacitance extractor. Parallel conducting layers which are sufficiently long and close to each other tend to have higher capacitance values and higher critical area. Therefore, capacitance extraction rules can be utilized to find the most probable bridging faults. The biggest advantage of the extraction flow based on parasitic capacitance is that the capacitance extraction is a part of the design flow. So, little extra effort is needed to incorporate the defect extraction of bridging faults in the whole flow. The capacitance between two conducting layers using the parallel plate model is given by:

$$C = \epsilon \frac{A}{D} \tag{3.1}$$

where A is the overlap area, ϵ is the interlayer dielectric constant, D is the distance between the two layers. Bridging defect probability between two conducting layers is directly proportional to the overlap area and inversely proportional to the distance between them, the capacitance C from equation 3.1 has the same relationship with A and D. Hence comparing the capacitance between two sets of adjacent conducting layers, can indicate which set is more likely to sustain a bridging defect. If there exists a difference between ϵ for the two sets, it can be simply taken care of by dividing with ϵ. Therefore, only the ratio of A/D is left, to represent the bridging defect probability at any given site. Figure 3.1 illustrates that the two adjacent conducting layers running parallel to each other for a longer distance ($L_1 >> L_2$) are more likely to sustain bridging faults, even though the distance (D) between the layers is same. Similarly, two conducting layers which are very close to each other ($D_1 << D_2$) are more likely to contain a bridging defect, even though lengths remain the same.

Figure 3.2 illustrates the flow to extract the bridging defects from the layout. There are three inputs to the defect extraction process:

- Schematic/Netlist File.
- IC Layout.
- Defect Extract Rules.

The golden netlist file is the netlist of the design (schematic view) without any injected faults in it. This file is in the PSTAR[1] format. Assura is a Cadence tool used for parasitic extraction of the IC. Defect extract rules provide the information about

[1]In-house Analog Simulator of NXP

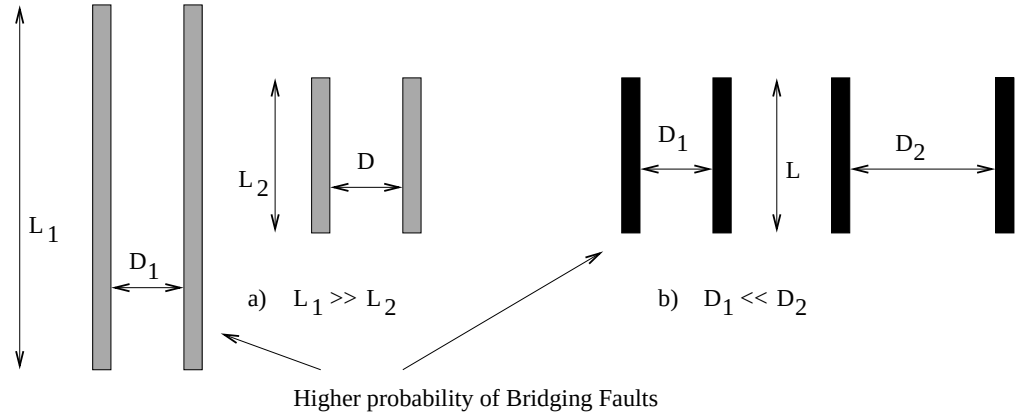


Figure 3.1: Capacitance vs. Probability of Bridging Faults [20].

the minimum capacitance value that need to be extracted, which can manifest itself in a bridging fault. The extracted netlist is the output of a layout extraction (performed by Cadence Assura) where the layout is checked for possible bridging faults. This is a 'flat' netlist, which essentially means that hierarchy from top to bottom modules is flattened out and a hierarchical netlist is obtained. An LVS (layout vs. schematic) check is required, where the node names of the schematic netlist and the extracted netlist are compared and mapped to each other. LVS check is followed by the defect extraction process where ranked defect list can be obtained. This defect list is passed to the Fault Injector which takes the golden netlist and the defect list, and generates the faulty netlists by injected defects into the golden netlist.

Figure 3.3 & 3.4 shows the plot of defect weight vs. the number of extracted defects for inter-layer and intra-layer bridging faults respectively. There are three metal layers: in1, in2, in3 present in the IC, alongwith one polysilicon (ps) layer. For the inter-layer bridging defects the maximum number of defects are extracted between in3-in2 metal layers and the minimum number of defects are extracted for in1-ps layer. For the intra-layer bridging defects, the maximum number of defects are found for the in2 layer, but the maximum cumulative weight corresponds to the in1 layer. It can be seen that the cumulative weight of the defects rises rapidly with the initial few defects of high probability and tends to saturate, as the weight of the subsequent defects decreases. These graphs can be very helpful in pruning the defect list, as the weight of the defects added in the last is much smaller and hence the probability of their occurrence is negligible.

3.2 Introduction to dislocation defects

There are two basic types of dislocations, edge dislocations and the screw dislocations. Figure 3.5(a) shows the edge dislocation defect with an extra plane of atoms in upper crystal lattice, disrupting the regular crystal structure. Screw dislocations are shown in Figure 3.5(b), where a step or ramp is formed by displaced atoms in a crystal plane. Both edge and screw dislocations belong to the category of line defects. Edge dislocations

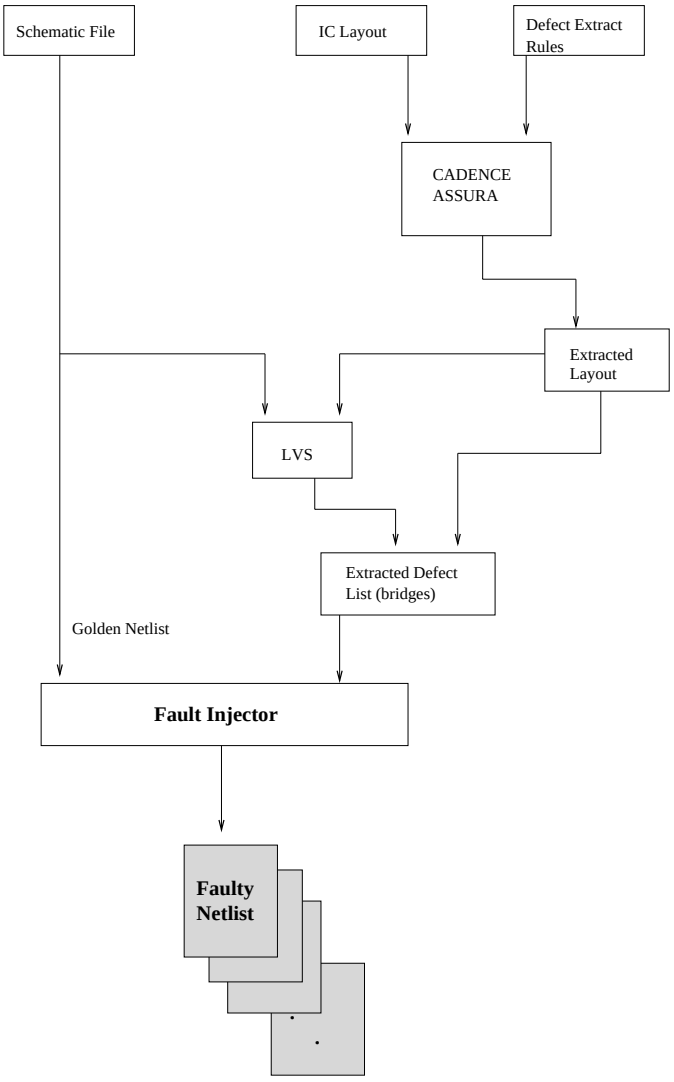


Figure 3.2: Extraction Flow for Bridging Defects

move in parallel with the direction of the shear stress applied, whereas the defect line movement in a screw dislocation is perpendicular to the shear stress. Dislocation loops are formed if a dislocation containing the extra or missing plane of atoms lie entirely within the crystal. Most of the times, the dislocations are the hybrid combination of edge dislocations and the screw dislocations. Transmission Electron Microscope (TEM) images of some of the observed dislocation defects are shown in Figure 3.6. Dislocation line defect is shown in Figure 3.6(a) and the half loop dislocation faults are shown in Figure 3.6(b). Half loop dislocations are caused by pitting of trench sidewall during trench oxidation and Figure 3.6(b) reveals their origin from the trench wall.

Dislocation defects tend to show a high resistive behavior and the observed leakage current is significantly less than the circuit with bridge (short) defects. Dislocations may not result in a complete failure of the IC, but may pose a reliability risk (i.e., the IC fails

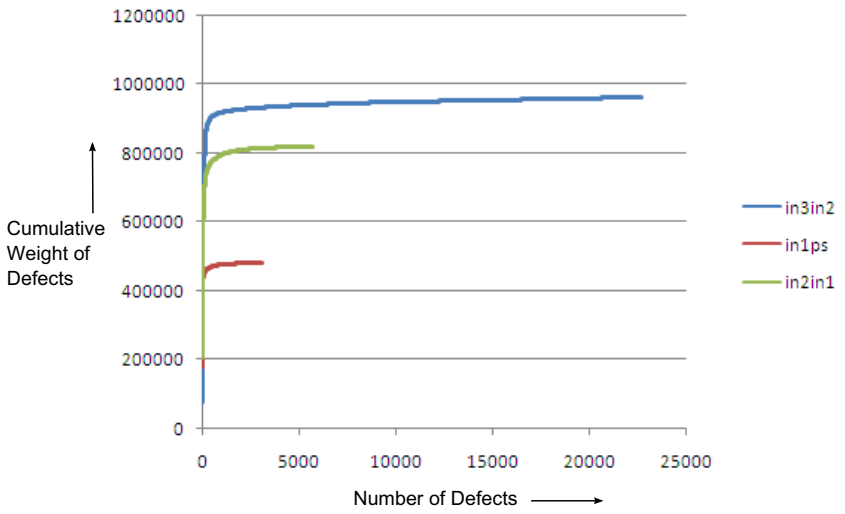


Figure 3.3: Cumulative weighted distribution of inter-layer defects

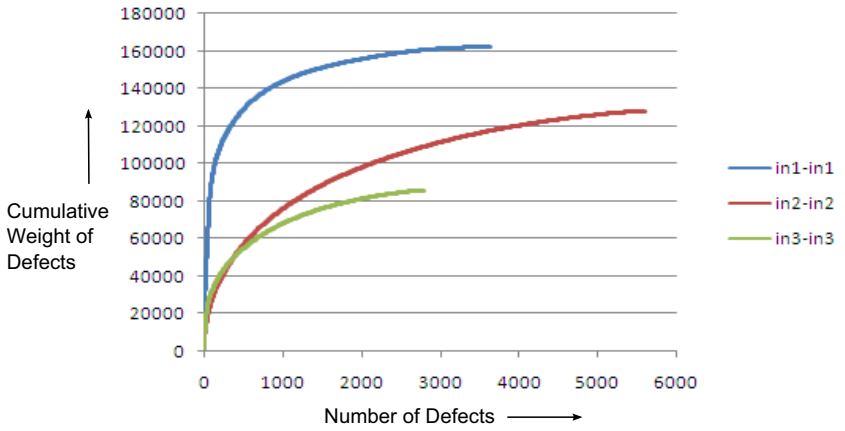
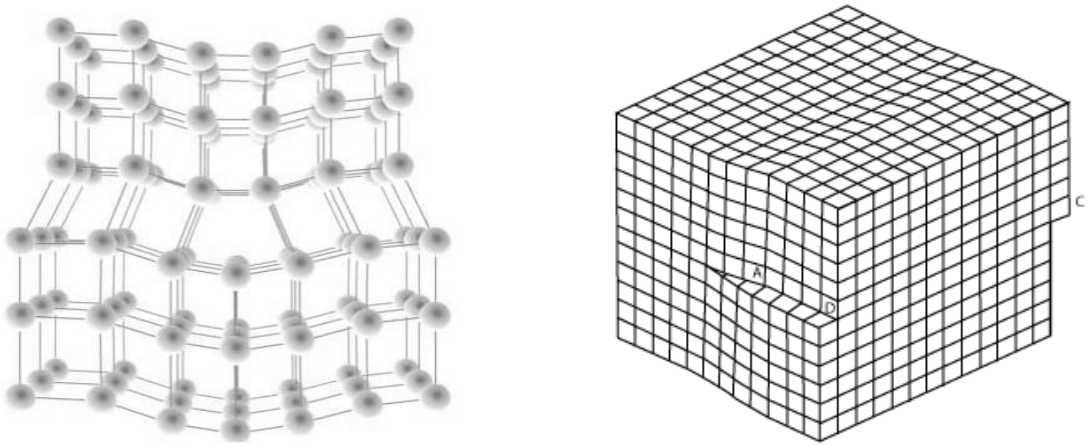


Figure 3.4: Cumulative weighted distribution of intra-layer defects

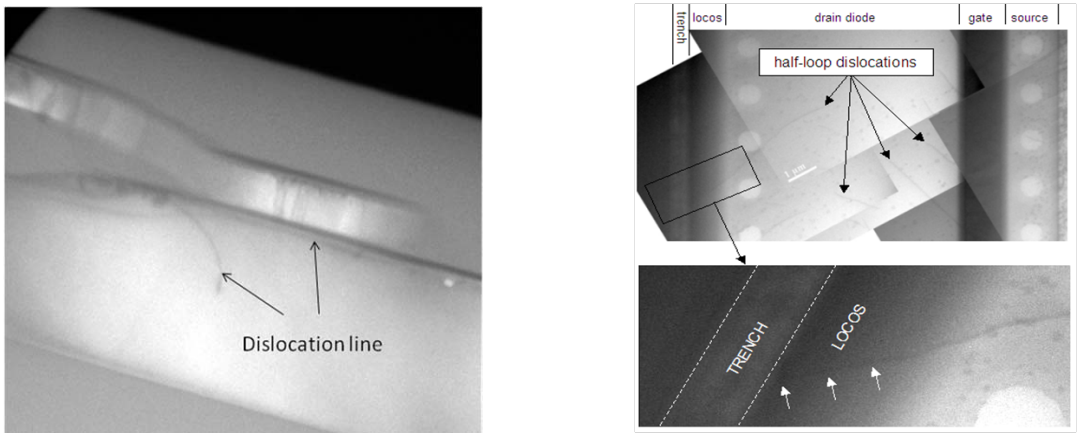
over time). It is typically very challenging in AMS testing to detect these defects. High stress levels in a substrate are associated with dislocation defects. High accumulation of stress during formation of shallow trench isolation structures and oxidation steps can extend the effect of dislocations to larger distances. IC fabrication process also involves stress build up, with the use of materials having thermal expansion coefficients different than silicon, deposition of films with intrinsic stress and non-planar surface oxidation [21].

Dislocations have been identified as one of the major contributors to leakage related failures, while crossing PN junction of a device [22][23][24]. Formation of dislocation defects is a two step process: 1) the dislocations should be nucleated and 2) they should grow into areas where they can affect device characteristics [25]. The nucleation of dislocation defects has been attributed to process mechanisms such as ion-implantation and oxidation [26]. Ion-implantation is used in many steps of advanced bipolar and CMOS



(a) (b)

Figure 3.5: Crystal line defects: (a) Edge dislocations with extra plane of atoms in the lower part of crystal lattice (b) Screw dislocation with screw-like slip of atoms in the upper part of crystal lattice.



(a) (b)

Figure 3.6: TEM image of (a) dislocation line defect and (b) half loop dislocations originating from trench.

technologies, it disrupts the regular crystalline structure of silicon and subsequent annealing steps are required to repair this damage. Even after treating the silicon substrate with annealing steps, some crystal structure residual damages are always left [27]. This residual damage does not alter the device characteristics if it is present in the areas outside the space-charge (critical) regions of the device. However, high stress built up in device structures have a compounding effect on these defects, which can become dislocations and can propagate to larger distances [21]. Much of the work has been performed on the root causes and behavior of dislocations [21][26][28]. Nevertheless, none of them has addressed the extraction of these defects.

3.3 Prior work related to dislocation defects

Dislocations defects have attracted the researchers and continuous effort has been put to understand the behavior and the root cause of these defects. Fahey et al. have provided an excellent study to understand the stress induced dislocation defects [21]. The study focuses on the effect of different process steps used in IC fabrication process such as oxidation, ion implantation and their role in the formation and promotion of dislocation defects. Stress levels associated with shallow trench isolation structures (STI) are also discussed in detail. Stress induced by gate stack formation also helps in promotion of the dislocation defects [29]. The effect of dislocations in heavily doped silicon substrate is studied in [30]. It was found that in n-type silicon, the dislocations behave as acceptors and a donor like behavior is shown in p-type material. This is the underlying cause for the formation of leakage path in the device junctions affected by dislocations [31].

In a separate work, detailed Transmission Electron Microscope (TEM) imaging of these defects is done to perform in-depth analysis, where the physical information about the defect is related with the observed electrical characteristics, by measuring various leakage currents [26]. Figure 3.7 shows the measured drain-source current corresponding to the dislocation defect which was observed, spanning from source to drain terminals. The reference transistor curves point to the drain current versus drain voltage of a MOS transistor at different gate voltages while the leaky transistor curves illustrate how the normal behavior of the transistor can be affected due to the dislocation defect. All leaky transistors have additional current component due to the presence of dislocation defect.

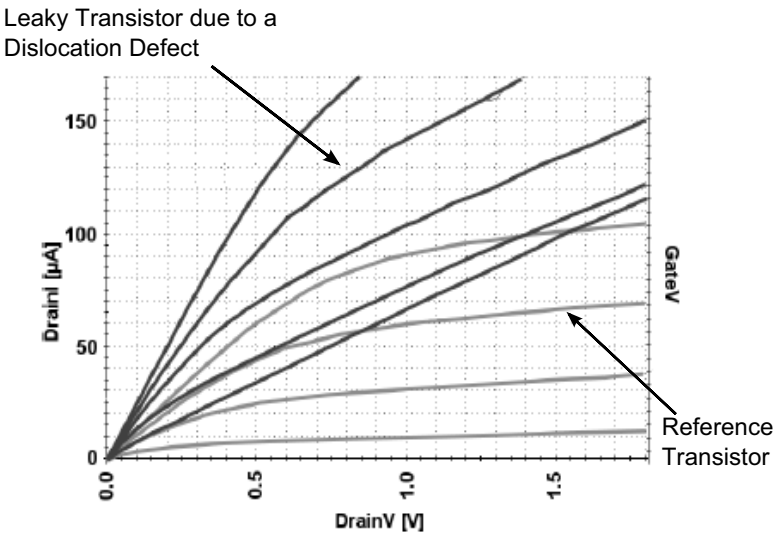


Figure 3.7: Electrical characteristics of a failing transistor (dark lines) due to source-drain leakage current as compared with a reference transistor (bright lines) [26].

Bipolar analog devices are also considerably affected by trench processing conditions resulting in altered device characteristics [32]. It has been shown that stresses and dislocations caused by silicon on insulator (SOI)/trench processing can result in collector-

emitter leakage current. In a similar study done in [33], dislocation defects were found for STI/SOI CMOS devices. The dislocation defects found in this study, can become electrically active only if they extend the entire distance from source to drain.

3.4 Extraction framework for dislocation defects

Defects can be extracted at different levels of details. For the extraction of bridging defects layout details are passed to a parasitic capacitor extractor and the capacitance values are used to calculate the probability of a short between two nets. These nets can be either, two metal tracks or a metal and a polysilicon layer. The level of abstraction is layout and the parameter used for defining the set of rules for extraction is parasitic capacitance. For the extraction of dislocation defects the level of abstraction is netlist (or design schematic) and the rules are derived from studying the process design manual of different devices, where the possible dislocation defects can occur.

Figure 3.8 shows the main steps involved in the extraction of dislocation defects. The important steps involved in the extraction of dislocation defects include the analysis of the design manual, creation of a rule file and the implementation of defect extractor. In this section, the details of each step are presented. A device structure obtained from the process design manual is also shown and discussed at the subsequent steps of the flow.

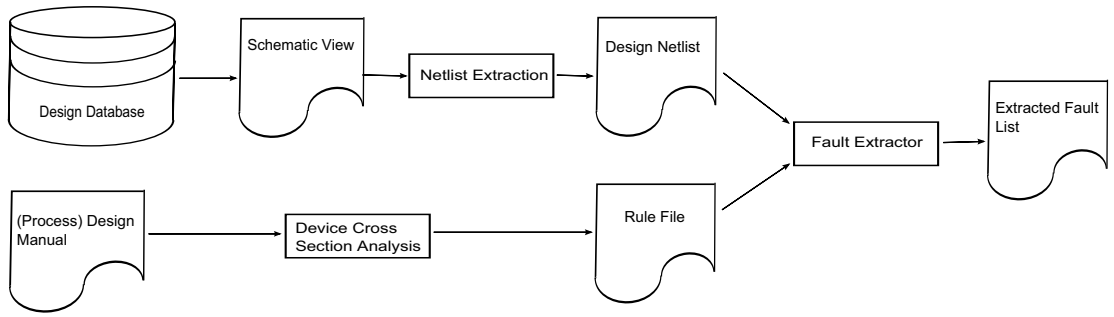


Figure 3.8: Extraction framework for dislocation defects.

3.4.1 Analysis of design manual

The Device Under Test (DUT) has many different types of devices present in the design database. These devices are instances of models present in the design manual. Examples are different types of diodes, capacitors, MOS transistors and Bipolar Junction Transistors (BJTs). These devices are fabricated to operate at different conditions, for example voltage levels can vary in the range of low, medium to very high voltage levels (120 V).

The goal of the analysis is to study the cross-section of all device models to understand the formation of device structures and the PN junctions potentially susceptible to dislocation defects. For example, isolation structures surrounding certain devices play an important role in the formation of dislocation defects and they have a significant contribution while analyzing the process models.

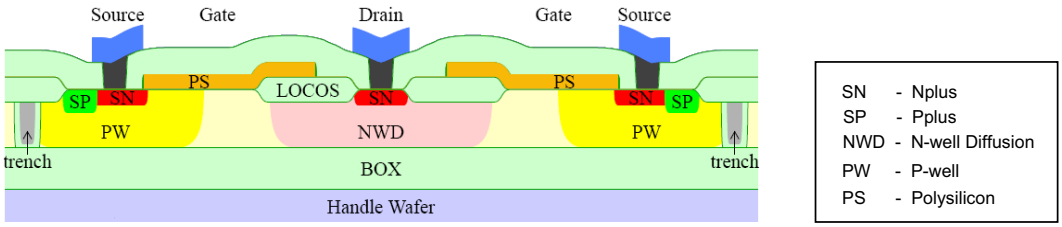


Figure 3.9: Process Design block of an NMOS transistor with fold=2 (drain centered device).

Figure 3.9 shows the cross-section of an extended drain N-channel MOS device, with maximum gate voltage as 12V and maximum drain voltage as 60V from the design manual of the BCD processes. As can be seen from the figure, the device is surrounded by a trench isolation structure that is filled with oxide and undoped polysilicon down to the buried oxide (BOX). These trenches can aid in the formation of dislocation defects. If a dislocation defect is present which extends in the channel region, then a source-drain leakage current is observed. Many other devices such as BJTs and diodes have also been identified as the potential target for dislocation defects.

3.4.2 Rule file creation

After analyzing the cross-sections of all the device structures in the design manual, a rule file is created. The rule file is a text file that includes an entry for each of the devices where at least one dislocation-susceptible junction can be present. The entry for a device includes its model name from the design manual (which is later matched with the device instances in the netlist), the list of all its pins (contacts), and the potential dislocation defects between its pins.

The pins must be in the same order designer uses when he instantiates devices of that model. For example, the standard order of drain, gate, source, body, (D,G,S,B) is used for a MOS device. The potential dislocations are given by pairs of pins (contacts) along which the leakage current can occur due to dislocation defect. The pin names are separated by whitespace, e.g, a dislocation between source and drain of a MOS device will be written by “S D” in the rule file. Comments are possible in the rule file for the sake of readability. In our implementation, the model name, pins, and dislocation defects must each occur on a separate line. The entry ends with the keyword “end”.

For the device shown in Figure 3.9, the model name is SMNDE and the contacts to this device are Drain (D), Gate (G), Source (S), Body (B) and Handle Wafer (HW). The only potential dislocation defect is between S & D pins. The basic structure of the rule file and the corresponding entries are shown in Figure 3.10. Similarly, many diode structures and BJTs, susceptible to dislocation defects are identified from the design manual and the corresponding rule file entries are created.

3.4.3 Defect extractor

The defect extractor takes the rule file and the design netlist as input and is written in PERL language. The netlist extracted from the design database is in PSTAR format.

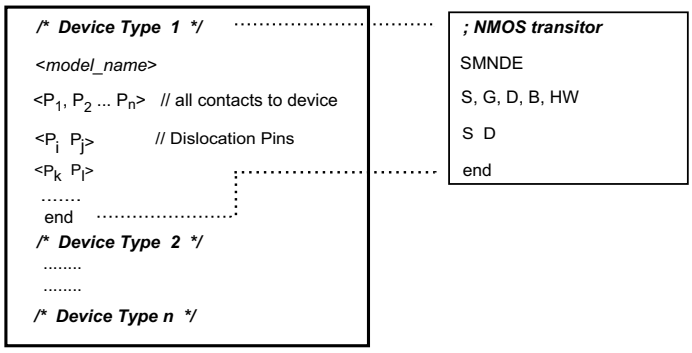


Figure 3.10: The structure of a rule file (left) and an example (right).

The defect extractor parses the netlist and flattens the design hierarchy. This is necessary such that the hierarchical net names can be obtained. After flattening, every device instance in the netlist is checked versus all the device models in the rule file. If the model of the device instance matches any of the device models in the rule file, the pins corresponding to the potential dislocation defects of that model are extracted by finding their hierarchical net names. The hierarchical net names are written in the output file as a potential dislocation defect.

For the MOS device shown in Figure 3.9, the device instance names present in the netlist are matched with model name of the MOS device and the pins (S & D) for the potential dislocation defect are obtained. The hierarchical net names for the corresponding source and drain contacts are then added to the defect list. The basic functionality of the defect extractor is shown in Algorithm 1.

Example: A high voltage N-type DMOS based (HV-NDMOS) diode is shown in 3.11. The diode is formed between the drain contact and SPD (body diffusion). The anode is contacted by SP and the drain forms the cathode. PS (polysilicon) is also contacted to anode. The PN junction diode thus formed is susceptible to dislocation defect. There are three contacts to this device, namely, anode (A), cathode (K) and handle wafer (HW). The pins for a potential dislocation defect are anode and cathode. Therefore, the information about the contacts and the pins for a dislocation defect is to be added in the rule file. In the subsequent step, the defect extractor is executed with the design netlist and the rule file as input. After flattening the design hierarchy in the netlist, the device model of the HV-NDMOS (diode) is searched in the model instances present in the netlist. Once the model instance is found in the netlist, the hierarchical net names corresponding to anode and cathode of the HV-NDMOS diode are then added to the defect list.

This extraction framework is applied to the DUT containing 16859 active devices. In total, 1438 dislocation defects have been extracted. The number of susceptible dislocations is around 8% of the active number of devices. By performing the dislocation extraction as proposed, we can limit the defect list to only 1438 potential locations out

```
Data: Netlist and Rule file
Result: Extracted Defect List for Dislocations
read the netlist and flatten design hierarchy;
read the rule file;
D ⟵ ∅ ; // Defect set, initially empty
foreach device instance in the netlist do
    get the device instance model;
    foreach device model in the rule file do
        get the device model;
        if the device instance model in the netlist = device model in the rule file
        then
            foreach dislocation defect in the model do
                get the dislocation defect pins;
                get the hierarchical net names attached to the pins;
                D ⟵ D ∪ {hierarchical net names};
            end
        end
    end
end
```

Algorithm 1: Algorithm for defect extractor.

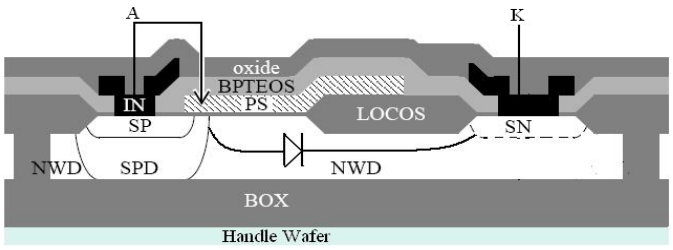


Figure 3.11: The cross-section of a high voltage N-type DMOS based transistor.

of 16859 active devices. This is useful in guiding failure analysis to relevant locations as well as speeding up the DOT process. In DOT, one uses an extensive defect list which is simulated. Truncating the defect list to relevant defect locations reduces the simulation effort considerably. Defect extraction is the primary step in DOT process, which is followed by test application and defect simulation. After simulating all the defects, a fault simulation database can be prepared which can be used for test optimization purposes. Details about generating the simulation database and test optimization process are discussed in chapter 4.

Defect Simulation and Test Optimization

4

In the previous chapter, details about the defect extraction were presented. For the purpose of defect simulation a test stimuli is applied. This chapter discusses about the various aspects of test stimuli such as test setup and derivation of test limits. Simulation results for the bridging defects are discussed briefly. The dislocation defects are simulated across various resistance values and the behavior is analyzed. Simulation of extracted defects for the applied test program facilitates the generation of the detection matrix. The use of detection matrix for test optimization purpose is described. Various algorithms are presented for test optimization, preserving the industrial requirements. Finally an optimized test set is obtained detecting all the (detectable) defects.

This chapter is organized as follows. Section 4.1 presents the preparation for fault simulation by discussing about the test program used. Section 4.2 describes the generation of the fault simulation database. Section 4.3 presents the results for simulation of bridging defects. Analysis of simulation results for dislocation defects is presented in section 4.4. Section 4.5 compares the simulation results with the actual silicon measurements. Section 4.6 formalizes the detection matrix and discusses about its generation. Details about the test optimization process and the various algorithms used are presented in section 4.7.

4.1 Preparation for defect simulation

In the DOT flow, defect extraction is followed by simulating the faulty netlists. Faulty netlists are obtained by injecting faults one by one in the (fault-free) golden netlist. Thus, the faulty netlists contain a defect embedded into them. This section presents an overview about the test setup and the test limits used for simulation. Various issues encountered during the test simulation are also discussed briefly.

4.1.1 Test setup

These faulty netlists are subjected to simulation by the application of test stimuli. The test stimuli considered for this project contains various kinds of tests such as:

- Voltage measurements
- Current measurements
- Timing measurements
- Readout tests
- Hysteresis tests

Timing measurements are used to check the different parameters such as rise time, fall time, propagation delay, etc. Readout tests generally include reading out the output bits at certain pins when appropriate input levels are set. Hysteresis tests present in the DUT (Device Under Test) are generally used to measure the differences between high and low level threshold voltages. Each of these tests is measured at three different voltage conditions. These conditions are:

- Minimal (V_{bat} = 5V, V_{cc} = 4.75V)
- Nominal(V_{bat} = 14V, V_{cc} = 5V)
- Maximal (V_{bat} = 40V, V_{cc} = 5.25 V)

Here V_{bat} stands for the battery voltage and V_{cc} stands for the supply voltage of the chip.

4.1.2 Test limits

The effectiveness of each test is related to the test limits. Test limits are decided for a good circuit behavior keeping the process variations in mind. They are set in such a way that the industrial requirements are met and unnecessary yield loss is kept to a minimum. In case of automotive products these limits are generally set very tight due to very high quality requirements. There are two choices to decide upon the test limits:

- Monte-Carlo analysis
- Production test program

Test limits based on Monte-Carlo simulations give a good impression of the circuit sensitivity to different process parameters. In such an analysis, design can be simulated across various process corners and thus the test limits can be derived. These kinds of analysis are generally helpful for setting the limits in ICs which are introduced for the first time in production test environment. The current DUT is a mature product in volume production. It has a proven test coverage. Hence, instead of relying on monte-carlo simulations test limits can be based on production data.

4.1.3 Simulated tests

In total, 461 tests were originally simulated. Figure 4.1 shows the profile of the 461 originally simulated tests. Out of these tests, only 399 tests were considered for simulation. The remaining tests are not considered for simulation for the following reasons:

- **Limits off:** This includes the cases when the golden (fault free) value is skewed by more than 200% from the production test limits. One of the reasons of this large skew is the error in modeling the production tests. The tests performed at the production site are modeled manually in the PSTAR[1] format. This modeling is not always perfect and hence some errors are bound to be caused in the test programs thus generated.

[1]In-house analog simulator of NXP Semiconductors

- **Missing limits:** There are few tests which are part of the test plan but got removed from the production testing during the product life cycle. Since the production test limits are applied during simulation setup, these limits do not exist anymore and thus classified as missing limits.

- **Simulation issue:** Some tests when simulated have convergence issues while simulating. One of the reasons is that the simulator is not able to find a DC operating point and hence not able to converge.

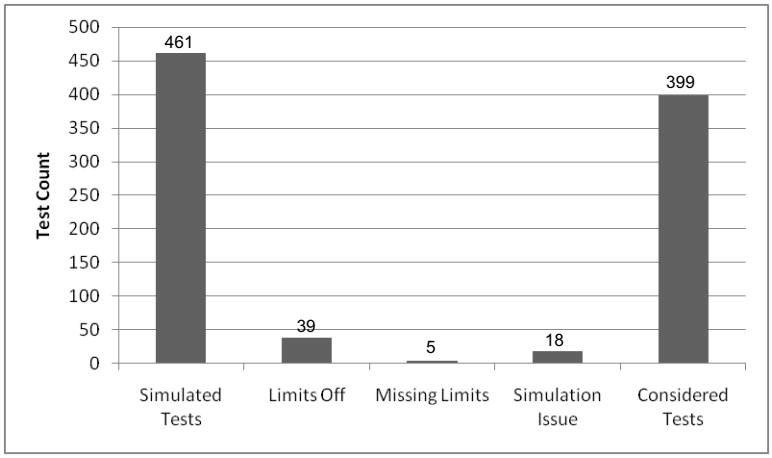


Figure 4.1: Profile of the originally simulated 461 tests

4.2 Generation of defect simulation database

The defect simulation database is created with the help of AnalogShell. AnalogShell is a test and fault analysis environment for analog designs. It is a very flexible interface allowing users to modify analysis flows or create new scripts around them by using the integrated TCL (Tool Command Language) shell. As shown in Figure 4.2, AnalogShell facilitates the generation of fault simulation database. The inputs to AnalogShell are:

- *Test program file:* Test program file contains the production tests modeled in the format of analog simulator.

- *Golden netlist:* Golden netlist is the design netlist without any injected faults in it.

- *Defect list:* This file contains the net-names of all the extracted defects.

- *Process design kit file:* This file contains the process model parameters of all the active and passive elements present in the circuit. These parameters are used by the circuit simulator to predict the performance of the design.

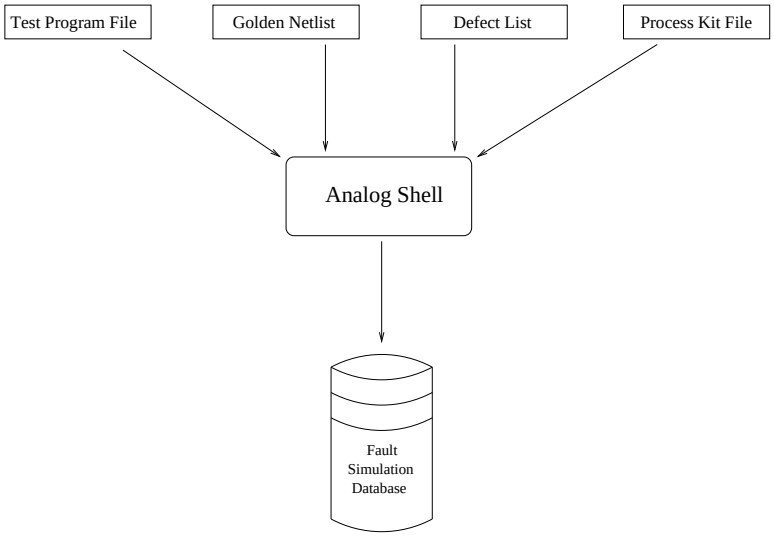


Figure 4.2: Fault simulation database generation by AnalogShell

AnalogShell takes the golden netlist as input and injects the defects between the nodes present in the defect list. For each defect present in the defect list, a faulty netlist is created. The resistance of the defect to be simulated can be set from the interface depending on the signature of the defect. For example, simulating the bridging defects a low resistance value can be used, in the order of few ohms. Each of the faulty netlist with an embedded defect is then simulated separately using circuit simulators running on different servers. In total, there are 40 servers used in the current work environment. The number of servers used for simulation can also be configured in the AnalogShell. A simulation database is then created when the golden netlist and all the faulty netlists simulations are finished. This database contains the actual simulation results for all the applied tests of the golden netlist as well as the faulty netlists.

4.3 Simulation results for bridging defects

This section presents the results of the fault simulation of the bridging defects and the dislocation defects. Bridging defects are extracted based on the value of parasitic capacitance between two conducting layers. The capacitance value is used to calculate the relative likelihood of bridging defects. Figure 4.3 presents an overview of the amount of bridging defects that were extracted for the DUT. Each column represents a likelihood class, for example the 208 defects in the >10 PPM class are defects between two 'large' analog elements in the design and hence, more likely to occur. The defects in the 0.0001 to 0.1 PPM class typically involve defect between digital elements. The digital elements are typically smaller in size and therefore less likely to occur. However, they are also included in the analysis because the number of such defects is very large.

A list of 37932 bridging defects was simulated for the DUT. Since the bridging defects have a low resistive signature, a value of 10 Ohms was used for the simulation purpose.

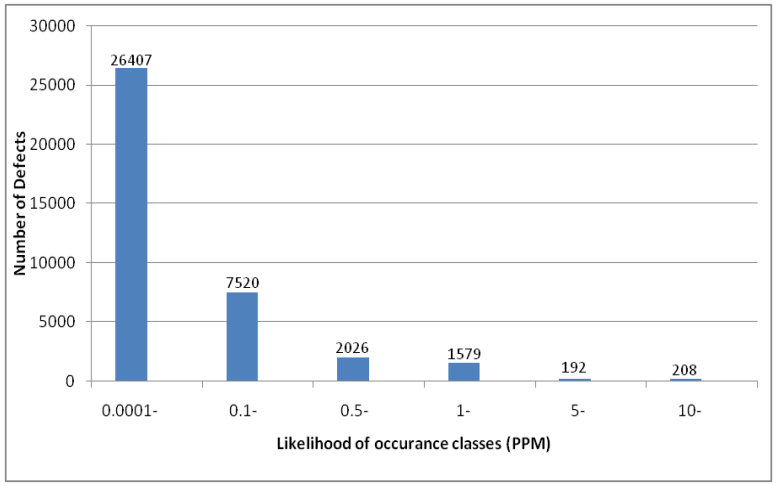


Figure 4.3: Defect likelihood distribution

One major bottleneck for simulating all the bridging defects is the required simulation time. For example, if simulating hundreds of tests for a faulty circuit takes one hour, it still takes several years to perform these simulation for 37932 faulty circuits. A novel technique has been developed at NXP Semiconductors to reduce the simulation time considerably and is applied to the DUT [34]. Out of 37932 defects considered, 24999 defects are detectable by the considered tests. Since the AMS product under consideration is a mature product in volume production with proven test coverage, the escaped defects do not pose any threat. These defects are either detected by the not modeled tests or the impact of the escaped defects on the output is so small that they do not manifest themselves into a faulty circuit.

4.4 Analysis of simulation results for dislocation defects

Dislocation defects as discussed in chapter two are the stress induced defects which disrupt the regular crystal lattice structure in silicon causing leakage related failures. Unlike shorts between metal layers, the dislocation defects tend to have a high resistive signature. These defects were also found in an existing design of NXP semiconductors manufactured in a similar technology as the DUT and the signature of these defects was found in the range of 20K (1K=1000) Ohm. Based on this analysis, the extracted dislocation defects have been simulated for four different values of resistances. These dislocation defects have been simulated for 1K, 10K, 100K and 1M(1000K) Ohm resistance values. The behavior of these dislocation defects for different resistance values has been shown in Figure 4.4. The x axis shows the tests which were simulated and the y axis represents the total defects detected by each test. On the right side of the curve there are many sensitive current tests which check the faults in the power domain of the circuit. There are two power domains in the DUT: V_{bat}, which supplies power to large part of the circuitry and V_{cc} which supplies power to less part of the circuitry. The tests designed to check the faults in the V_{bat} domain are generally more sensitive

than V_{cc} domain. Usually a V_{bat} domain test is followed by a V_{cc} domain test in the test plan, which explains the spiky nature of the curve. Another graph (Figure 4.5) has been generated which is sorted according to the number of defects detected by different tests (or by the sensitivity of the tests). This graph clearly shows that the 1K resistive range has the maximum detectability followed by 10K, 100K and 1M range.

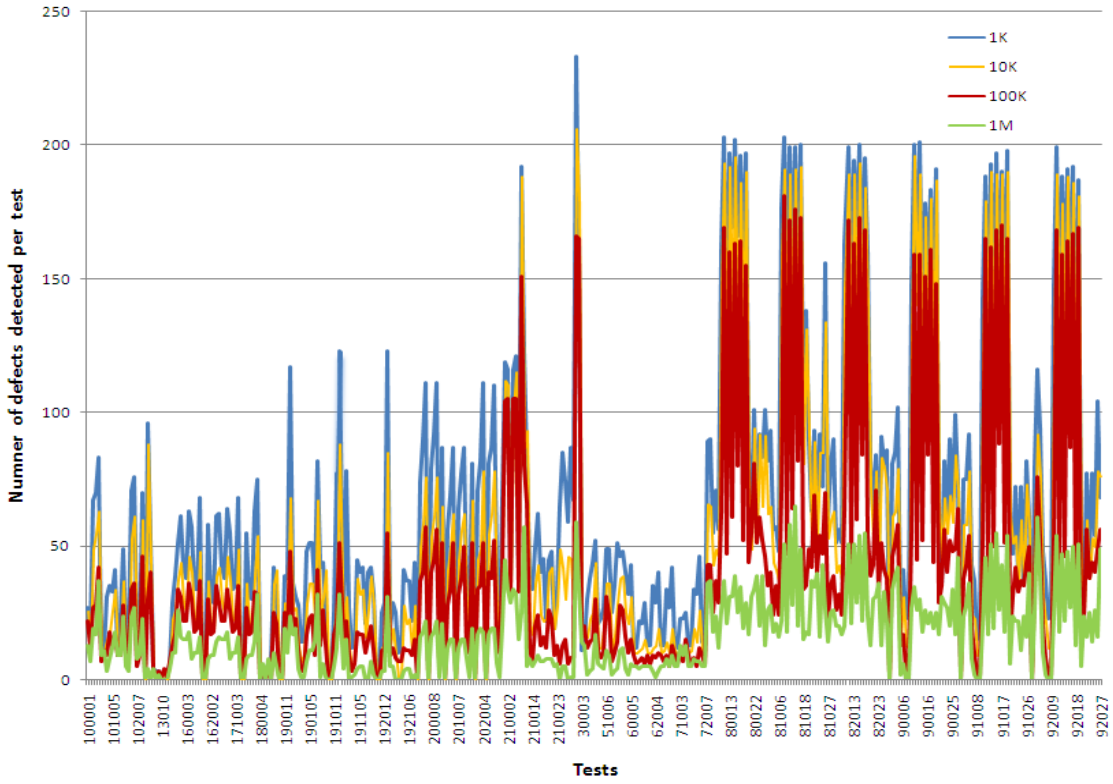


Figure 4.4: Simulation results of dislocation defects across various resistances.

One of the important conclusions that can be drawn from the analysis of this simulation results is: *Detectability of a dislocation defect decreases as the resistance value increases.* Since these defects cause leakage related failures, more detectability is found for the sensitive current tests. Detectability decreases significantly in the mega-ohmic resistive range. The total number of detected defects across various resistive ranges is shown with the help of a Venn diagram in Figure 4.6. As can be seen, the maximum defects detected belong to the 1K Ohm resistive range, along with the maximum unique detects. Out of the total defects detected, 95% are detected in the 1K resistive range, along with the 77% of unique detects. The unique detects decrease as we move from 1K Ohm resistive range to higher resistive range. The 1M Ohm resistive range was left for the further analysis because of the very low detection capability seen from Figure 4.4.

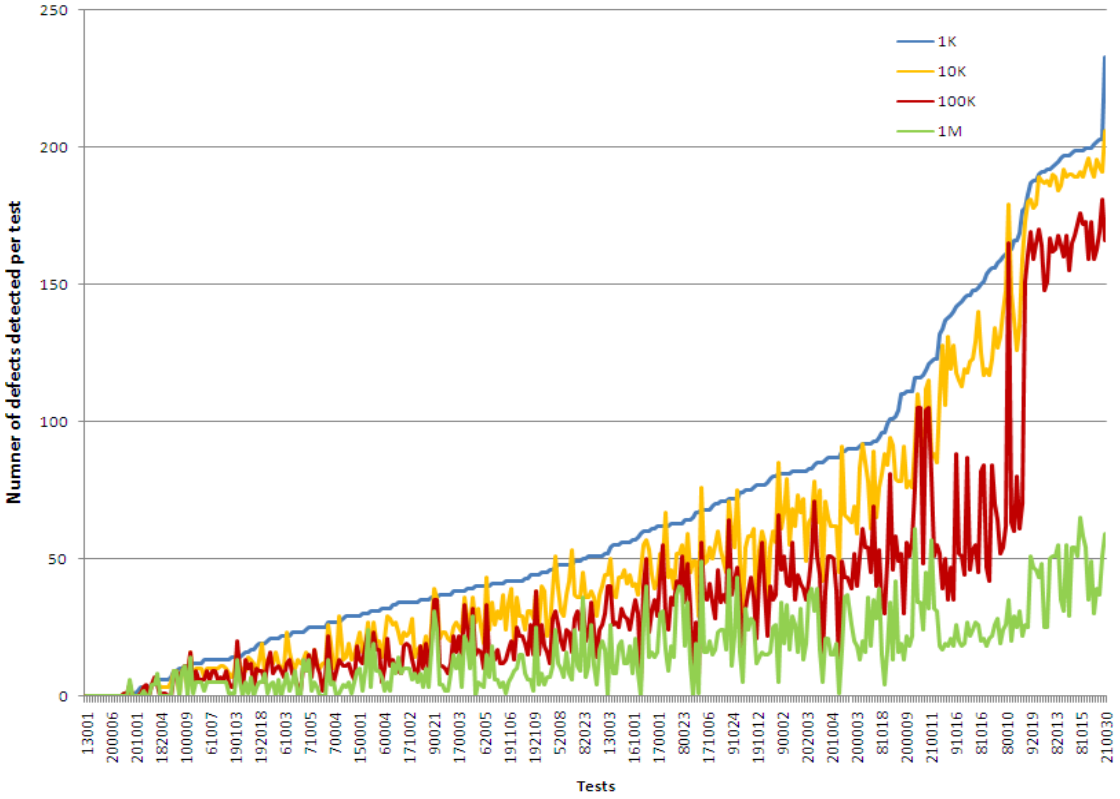


Figure 4.5: Simulation results of dislocation defects across various resistances sorted for 1K defects.

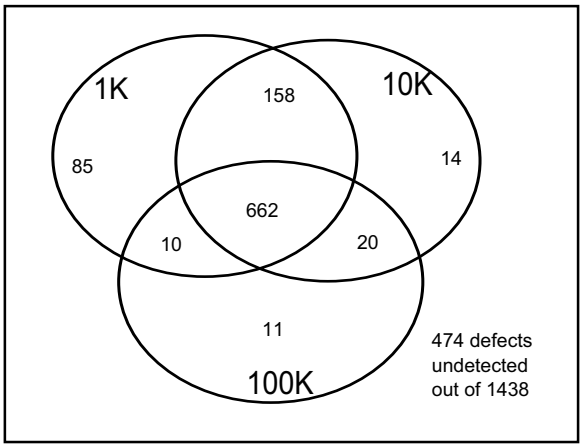


Figure 4.6: Defects detected across various resistances.

4.5 Simulation vs. measurement

The graph in Figure 4.7 shows the number of detected dislocation defects in simulation and the Figure 4.8 shows the observed results in production testing for failing ICs. In this

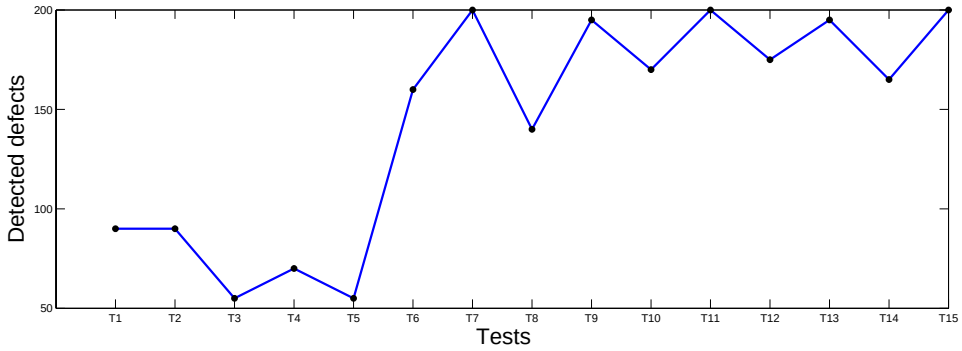


Figure 4.7: Detection trends observed during simulation.

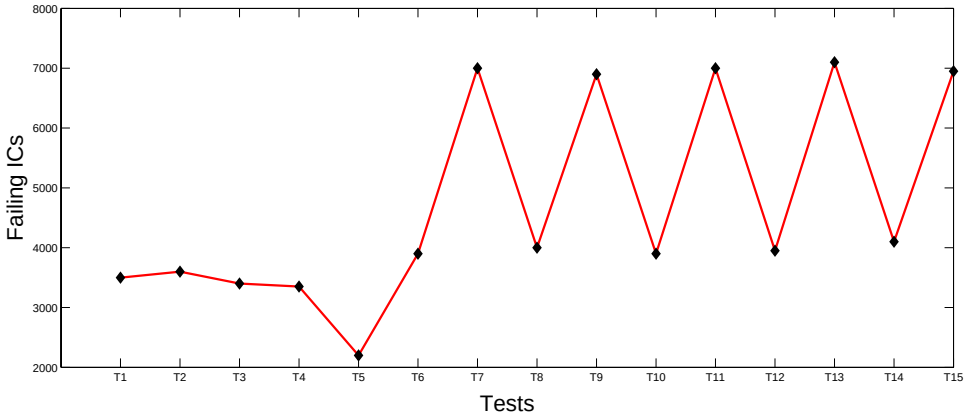


Figure 4.8: Detection trends observed in silicon during production testing.

comparison a subset of tests (current) is used. From the graphs it can be seen that the general detection trends are the same for simulation and the actual silicon results for the sensitive odd numbered tests. Such analysis increases the credibility in the simulation results and can be performed as an intermediate check to verify simulation results.

4.6 Generation of detection matrix

The fault simulation step is followed by the generation of a detection matrix. Mathematically the concept of detection matrix can be defined as follows: let D be the defect matrix of all the defects in a given DUT and let D_0, the first element of the matrix, be the fault free element. Moreover, let S be the matrix of test stimuli applied to the DUT and let R be the matrix of the faulty and fault-free responses (i.e., the detection matrix). Furthermore, assuming that there are n defects in the DUT , then the size of the defect matrix taking into account the fault-free element also, is $(n + 1) \times 1$. The defect matrix D can be formulated as:

$$D = \begin{bmatrix} D_0 \\ D_1 \\ D_2 \\ . \\ . \\ . \\ D_n \end{bmatrix}$$

For the formulation of the stimuli matrix, let us assume that there are m tests present in the test program. Hence the stimuli matrix can be written as:

$$S = \begin{bmatrix} S_1 & S_2 & S_2 & . & . & . & S_m \end{bmatrix}$$

where m is the total number of tests present. The Detection (response) matrix R is a function of the defect matrix as well as the stimuli matrix.

$$R = f(D \times S)$$

Each element of the detection matrix can be given as follows:

$$r_{ij} = f_{ij}(D_i \times S_j)$$

where $0 \leq i \leq n$ and $1 \leq j \leq m$.

The circuit is simulated to find out all the d_{ij} of the detection matrix. The first row of the matrix R contains the fault free responses. The size of R is $(n+1) \times m$.

The fault simulation database generated after simulating the faulty netlists is huge (38K $\times$ 399 entries). The data is spread over several files. Each file contains a subset of tests and the defect list. For generating the detection matrix from the simulation database, all the files need to be parsed and the test limits need to be applied to the actual measurement values obtained after simulating the faulty netlist. The golden (fault-free) netlist simulation values are then checked to coincide with the mean of test limits. If there is a skew between the mean value of test limits and the golden simulation value, corrective measures need to be taken. This skew can be because of the offset introduced while modeling the test programs in the format of circuit simulator. Another reason could be that the parasitics involved with the ATE (Automatic Test Equipment) can not be modeled. Only the device and test behavior is modeled, but the load part specific to the test system is not modeled. The skew introduced can be corrected in two ways:

- Shifting the golden simulation value to coincide with the mean of test limits. The same offset is applied to all other faulty netlists measurement values for that particular test.
- Shifting the test limits without changing the golden simulation value such that the mean of test limits and the golden simulation value coincides with each other. In this case, no adjustment needs to be done for the other faulty netlists.

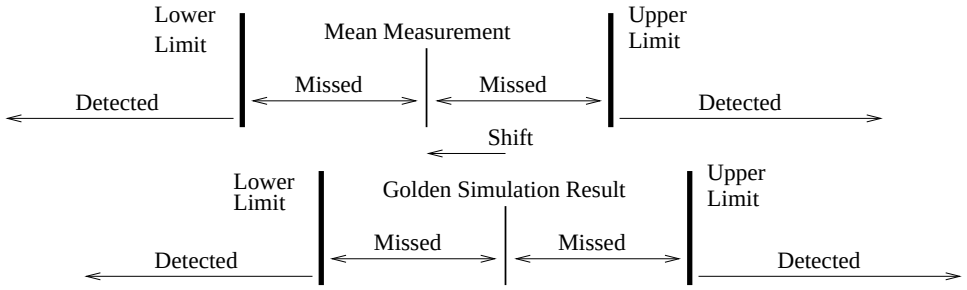


Figure 4.9: Shifting the golden simulation result to match with the mean measurement.

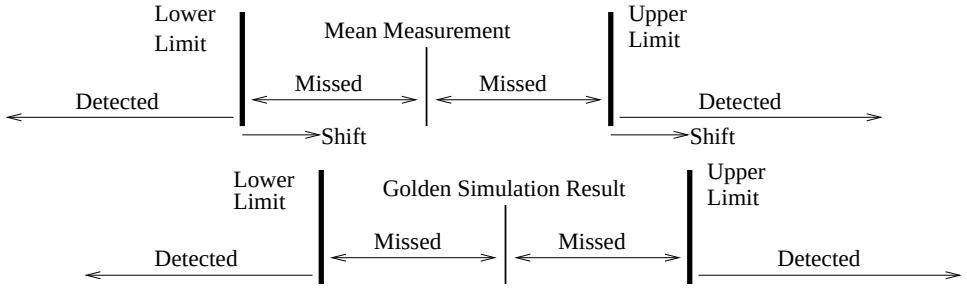


Figure 4.10: Adjusting the limits to match with the golden simulation value.

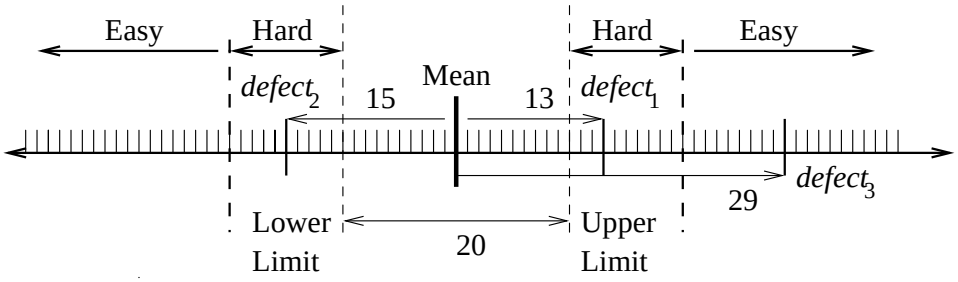
These approaches are graphically explained in Figure 4.9 & 4.10. This work uses the approach in Figure 4.9 to identify the detection status of a defect for a particular test because shifting the limits has the disadvantage if the test engineers do not know about pass/fail modifications. Once the detection status of all the defects is identified, a detection matrix can be generated. The defects in the detection matrix are identified by the unique reference keys. The detection matrix can be used for various purposes like improving the defect coverage, test optimization process and electrical failure analysis. Use of detection matrix for test optimization purposes is explained later in section 4.7.

4.7 Test optimization

In the early product life cycle, failure information is more important, whereas test time reduction is more important for mature products. The AMS product under analysis is a very mature product and has zero PPM quality requirements. Most of the tests used in the production environment are applied at three voltage conditions to achieve the quality requirements. From the historical pass/fail data obtained over a period of time it has been established that the test program for the DUT under consideration is well developed to maintain the stringent quality requirements, along with providing a good yield. The process variations are well under control and parametric yield is close to 100%. Hence, defects are the only yield limiting factors, which makes the design well suited to apply the Defect Oriented Testing flow.

Test optimization is the process which selects a small (minimal) subset of the pro-

duction tests that covers a required percentage of detectable defects. Since the subset is smaller than the original set, test time reduction can be achieved leading to significant savings in production test cost. The percentage of covered defects can be adjusted by the user. However, the current optimization flow tries to cover all detectable defects (100% defect coverage). The detection matrix discussed in the previous section forms the input to the test optimization process. Due to the analog nature of the tests, the entries for the results of the simulated tests are continuous numbers. For each considered test there are two limits (upper and lower): if a test result falls inside the limits, it is considered to be passed, else failed. Figure 4.11 shows the approach to classify hard and easy to detect defects based on the deviations from the mean value.



Detect (d_1) = 13/10 = 1.3
Detect (d_2) = 29/10 = 2.9
Detect (d_3) = 20/10 = 2.0

Figure 4.11: Classification of hard and easy to detect defects.

The larger deviation[2] from the test limits implies a stronger detection; for example, 2.9 (defect d_3) is more stronger detection than 1.3 (defect d_1). The defects can be categorized into hard and easy to detect defects. The stronger detections come under the category of easy to detect defects (current limit set at 2.0). The threshold limit for the easy and hard to detect defects can be set by the user to customize the test selection process. For example, a test selection process can be optimized in a way such that the primary focus is on hard to detect defects. Very weak detections (value set by the user) can also be removed from consideration. This is useful in accounting for the process variations or to accommodate modeling errors in the simulation setup, because out of limit measurements do not necessarily imply a faulty DUT. After setting a detection threshold, entries for the detection matrix can be made. An example of a detection matrix is shown in Figure 5.6, where sixteen tests have been used for simulation and only three are necessary to detect all the (detectable) defects. An entry of "D" represents that the defect is detected by a specific test. A blank value denotes the non-detection status.

For selecting the minimal test set, the detection matrix can be mapped to a set-covering problem. In a set-covering problem, several sets are given as input which can have common elements between them. From these sets, one is required to select a minimal

[2]the values normalized with respect to distance from mean to one of the limits

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	total	Defects
D	D				D			D	D				D		D	7	bridge__NET18.AN2_I4__C__1
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__2
																0	bridge__C__VDD!__3
		D		D	D	D	D			D		D	D	D	D	10	bridge__NET18.AN2_FIRST__A__4
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__5
						D								D		2	bridge__A__VDD!__6
D	D			D	D			D	D			D	D		D	9	bridge__Z__NET18.AN2_I4__7
D	D			D	D			D	D			D	D			8	bridge__Z__VDD!__8
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__9
		D		D	D	D	D			D	D	D	D	D	D	11	bridge__TUSSEN__NET18.AN2_FIRST__10
		D	D	D		D				D	D	D		D		8	bridge__TUSSEN__VDD!__11
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__12
D	D	D		D	D	D		D	D	D	D	D	D	D	D	14	bridge__NET18.AN2_I4__TUSSEN__13
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__14
		D	D	D		D				D	D	D		D		8	bridge__TUSSEN__VDD!__15
		D	D		D		D			D	D		D		D	8	bridge__NET18.AN2_FIRST__B__16
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__17
											D					1	bridge__B__VDD!__18
D	D			D	D			D	D			D	D		D	9	bridge__Z__NET18.AN2_I4__19
					D								D		D	3	bridge__Z__0__20

Figure 4.12: An example of test reduction by using detection matrix

number of these sets so that the selected sets contain all the elements present in the union of these sets. Similarly, in the mapped version, the tests represent the input sets and the defects detected by them represent the set elements. Now the problem translates into selecting a minimal set of tests such that all the defects are covered. Set-covering problem is proved to be an NP-complete problem [35]. However, heuristics exist to solve it efficiently. A greedy algorithm is one such heuristic that can be used to obtain the minimal test set. In this approach, a test that detects most of the defects is selected at each step. These defects are then removed and not considered for the subsequent steps. This algorithm iterates until no defects are left to be detected. The heuristic approach is described in algorithm 2.

Data: Detection matrix
Result: Minimal test set
$T \longleftarrow Tests$; `// original tests`
$D \longleftarrow Defects$; `// detectable defects`
$S \longleftarrow \emptyset$; `// minimal test set, initially empty`
while $D \neq \emptyset$ **do**
  $t \longleftarrow$ the test that detects most defects;
  $S \longleftarrow$ S $\cup$ {t};
  $T \longleftarrow T - \{t\}$;
  $D \longleftarrow$ D $-$ defects detected by t;
end

Algorithm 2: Select the minimal test set

The test optimization process also includes additional constraints, for example, some of the tests are customer required specification tests and need to be included uncon-

ditionally in the final optimized test set. The test selection process must makes sure that these specification tests are always included in the final test set. The presence of specification based tests make sure that certain defects can be removed from the defect set prior to the selection process. Thus the modified version of algorithm satisfying the above constraint is presented in algorithm 3.

Data: Detection matrix and spec tests
Result: Minimal test set
$T \longleftarrow$ Tests ; `// original tests`
$D \longleftarrow$ Defects ; `// detectable defects`
$T_s \longleftarrow$ Spec Tests ; `//` $T_s \subset T$
$S \longleftarrow \emptyset$; `// minimal test set, initially empty`
$T \longleftarrow T - T_s$;
while $T \neq \emptyset$; `// remove defects detectable by spec tests`
do
  $t \longleftarrow$ any test of T_s;
  $T \longleftarrow T - \{t\}$;
  $D \longleftarrow D-$ defects detected by t;
end
while $D \neq \emptyset$ **do**
  $t \longleftarrow$ the test that detects most defects;
  $S \longleftarrow$ S $\cup$ {t};
  $T \longleftarrow T - \{t\}$;
  $D \longleftarrow$ D $-$ defects detected by t;
end

Algorithm 3: Select the minimal test set while preserving spec tests

The analog tests considered for the DUT are not completely independent, often the same test is applied at three different voltage conditions. This gives rise to another constraint in the test selection process: where at-least one voltage condition for each test has to be present in the final test set. This essentially means all three voltage conditions for a particular test cannot be removed. Thus an extension of algorithm 3 is presented in algorithm 4 exercising the above constraint. This extension basically checks at the end if there are any tests without any supply condition. If any of the three voltage conditions are not present for a particular test, then the most frequently used supply condition is selected and added for that test. Supply voltage switching in the production testing environment can be minimized by using this feature.

Algorithm 3 was applied to detect all the bridging defects present in the DUT. Out of the considered 399 tests for simulation a minimal set of 176 tests was achieved sufficient to detect all the bridging defects. However, when the reduced set was applied to validate the production data of 1.3 million ICs, 11 ICs could not be detected (validation details presented in chapter 5). This would translate to around 10 PPM in terms of quality. Since the current DUT is an automotive product with zero PPM quality requirements, this would not be acceptable. This raises an important question, whether considering the bridging defects only as the failure mechanism for the DUT is sufficient or not?

Algorithm 2(T, D, T_s, S) ; `// Run Algorithm 2`
$c \longleftarrow$ supply condition appearing most in S;
for $t \in T$ **do**
  if *no condition of* $t \in S$ **then**
    $S \longleftarrow \mathrm{S} \cup \{\mathrm{t}_c\}$; `// select condition c of t`
  end
end

Algorithm 4: Select the minimal test set while preserving spec tests, and ensuring that at least one supply condition of any test is present

To answer the above question, dislocation defects have been considered for analysis in the DUT because the production data suggests that bridging defects are the primary failure mechanism, followed by the dislocation defects. Therefore it is required to check whether the current, minimal test set (176 tests) is sufficient to detect all the dislocation defects or extra tests are required. In order to achieve this, the minimal test set obtained for the bridging defects was passed as specification test set (T_s) to identify the extra tests needed for detecting all the dislocation defects. The optimal test set detecting all the bridging defects and the dislocation defects is calculated. A greedy algorithm has been applied to obtain the minimal test set.

The greedy algorithm starts with selecting the tests having maximum detection capability and proceeds iteratively. The tests which detect unique defects are added towards the end. Another variant of this algorithm can also be used to minimize the extra tests. This variant of the algorithm starts with adding the tests with unique detection capability. When all the tests with unique detection capability are added to the test set, a greedy algorithm can be applied to cover the remaining defects. This variant is presented in the form of algorithm 5. Amongst the extra tests added for the dislocation defects, many tests are found to be overlapping for different sets of resistance values.

The comparison of the performance of *greedy* and *unique detects first* algorithm for the extra tests needed to cover the dislocation defects on top of the test set obtained for bridging defects are shown in Table 4.1. As can be seen from Table 4.1, the algorithm 5 does not lead to significant improvement over the greedy test selection algorithm. One of the reasons for not achieving significant improvement is: there are very few tests that need to be added on top of the already existing test set. Hence, there is very less room to further optimize the test set obtained with greedy test selection algorithm.

Table 4.1: Comparison of Greedy and Unique detects first algorithm to obtain minimal test set

	Greedy	Unique detects first
1K Resistance	176 + 25 = **201**	176 + 25 = **201**
10K Resistance	176 + 26 = **202**	176 + 26 = **202**
10K Resistance	176 + 27 = **203**	176 + 26 = **202**

In table 4.1, the minimal test set is obtained by finding the extra tests to detect

Data: Detection matrix and spec tests
Result: Minimal test set
$T \longleftarrow$ Tests ; `// original tests`
$D \longleftarrow$ Defects ; `// detectable defects`
$T_s \longleftarrow$ Spec Tests ; `//` $T_s \subset T$
$S \longleftarrow \emptyset$; `// minimal test set, initially empty`
$T \longleftarrow T - T_s$;
while $T \neq \emptyset$; `// remove defects detectable by spec tests`
do
  $t \longleftarrow$ any test of T_s;
  $T \longleftarrow T - \{t\}$;
  $D \longleftarrow D-$ defects detected by t;
end
while *there exists a test with unique detection capability* **do**
  $t \longleftarrow$ the test that detects unique defects;
  $S \longleftarrow$ S $\cup$ {t};
  $T \longleftarrow T - \{t\}$;
  $D \longleftarrow$ D $-$ defects detected by t;
end
$c \longleftarrow$ supply condition appearing most in S;
for $t \in T$ **do**
  if *no condition of* $t \in S$ **then**
    $S \longleftarrow$ S $\cup$ {t_c} ; `// select condition c of t`
  end
end

Algorithm 5: Select the minimal test set starting with the tests with unique detection capability

dislocation defects on top of the existing test set for bridging defects. Since the overall goal is to detect all the defects (dislocations and bridges) present in the DUT, a reverse approach can also be applied, where the test set needed to detect dislocation defects is obtained first and then the extra tests are obtained to detect all the bridging defects. In this approach too, both the greedy and unique detect first algorithms are applied and the results for the minimal test set are shown in Table 4.2

Table 4.2: Comparison of Greedy and Unique detects first algorithm to obtain minimal test set using the reverse approach

	Greedy	Unique detects first
1K Resistance	132 + 68 = **200**	132 + 67 = **199**
10K Resistance	133 + 66 = **199**	133 + 66 = **199**
10K Resistance	134 + 68 = **202**	133 + 67 = **201**

As can be seen from 4.2, there is a slight improvement in the number of final tests

obtained by using the reverse approach. The minimal test set obtained using this approach is used to validate the production data. The production data set contains 1.3 million ICs and the test set obtained is used to catch all the faulty ICs. The details about the whole validation process are presented in Chapter 5.

5 Silicon validation

The previous chapter presented the details about the fault simulation and test optimization process. To validate the selected test set, production data set of 1.3 million dies is analyzed. The details about the validation process are presented and the issues of marginal failures, site dependency and test process errors concerning the test data are addressed. Diagnosis procedure for the escape dies found in the previous chapter is presented using a fault dictionary approach. For an effective diagnosis scheme an impact factor based analysis to match the silicon signature with the simulation signature is presented. Finally, a deeper analysis of the escaped dies is presented and ways are suggested to reach the goal of zero PPM requirements.

This chapter is organized as follows. Section 5.1 presents the details of the input production data and the screening process used to identify the escape dies. Section 5.2 introduces the fault diagnosis procedure and the various issues concerning the analog fault diagnosis. Section 5.3 describes the signature matching procedure used to confirm the presence of dislocation defects in the escaped 11 ICs. Section 5.4 studies the characteristics of the missed devices.

5.1 Validation with production test data

The basic steps involved in the Defect Oriented Testing (DOT) flow are presented in Figure 5.1. Details about the defect extraction were presented in chapter 3. Defect simulation of the extracted defects and the selection of optimized test program were described in chapter 4. This chapter presents the details about the validation process using the production data for 1.3 Million dies.

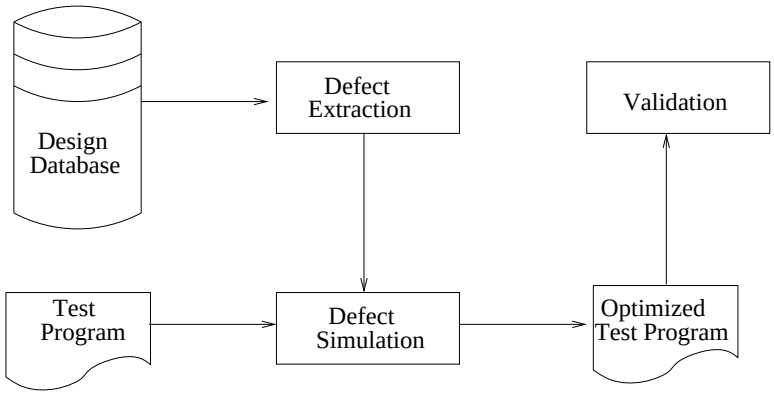


Figure 5.1: Basic steps in the DOT flow

As discussed in chapter 4, the test optimization process has two parts. The first part

consists of selecting the minimal test set for all the 38K bridging defects extracted from the DUT (Device under Test). An optimal test set of 176 tests was obtained (out of 399) to detect all the bridging defects. This test set is used to validate the production data set of 1.3 Million dies. In the validation process, 11 ICs were found as escapes while applying the reduced test set obtained for the bridging defects. The second part of the optimization process includes selecting the extra tests needed to detect all the dislocation defects along with the bridging defects. An optimal test set of 200 tests was obtained across different sets of resistance values. This optimal test set is then used to validate the whole production data, especially focusing on the escaped ICs found in the first part.

This section describes the analysis performed on production test data (wafer test) from 10 different diffusion lots to validate the optimal test set obtained in the test selection process. The goal of the analysis is to verify if the reduced set covers all the dies that were rejected during wafer test.

5.1.1 Input data

In the validation process, 10 diffusion lots (233 wafers) with 1.3 Million dies are analyzed. Only the wafers that have full datalogs were considered for analysis. A full datalog is able to determine all the tests that would reject a particular die. This data is also called as continue-on-fail data. In a typical testing environment a die is thrown away as soon as it fails any test on the ATE. In such a case, rigorous analysis of the failing signature would not be possible. Hence full datalogs, can contribute to a wealth of information in such analysis. These datalogs are stored in a SQL (Sequential Query Language) database. In a typical production testing environment, a group of tests is performed, where if any test is failed a failure bin number is assigned to the die. The number of dies present in various bins could provide useful information about common failure modes of a chip. A typical datalog contains the following information about the die:

- Lot number
- Wafer Number
- X,Y coordinates of a die on a wafer
- Measurement results of all the tests
- Failing bin number
- Site number (the number of site which the die has failed on a multisite ATE)

In total there are more than 1000 tests used in the production testing environment. Out of these only 399 tests are modeled and considered for test optimization purposes. The remaining tests constitute packaging tests, ESD (Electro Static Discharge) protection tests, digital tests, etc., and have not been considered.

The first step in the validation process is to include the ICs failing for only the tests present in the considered test set (399 tests). All the ICs failing the tests other than the original 399 tests are not considered in the analysis, because they will be anyways

detected by the reduced test set also. The second step of the validation process consists of rejecting the ICs which are detected by the reduced test set of 176 tests. All the other ICs which are failing one of the 399 tests and not detected by 176 tests are need to be checked further, because the test data is in general not 'perfect'. It is not uncommon to have some good ICs which are rejected. This can have several reasons such as marginal fails, site dependency and test process issues. Measures are taken to identify these anomalies and correct them, but in case of doubt, anomalies result in rejection if the number of such cases is small and have a very small impact on the overall yield. These issues resulting in anomalies are discussed below in more detail:

- **Marginal fails:** The dies that are included in this category have the measured value just (marginal) outside the test limits. These dies are good dies and part of the main population, but sometimes due to the stringent test limits for automotive products, the test limits are cutting into the distribution of good ICs. These dies do not indicate faulty behavior and are certainly not outliers, because they are well within the six sigma (99.9999998% of population values in a normal distribution curve) limits. These sigma limits are set according to the PPM numbers required for the quality of the product. Figure 5.2 shows one example of a marginal die. In this case, the ICs may be fully functional and passing all the spec tests, but might result into marginal failures for few production tests resulting in overkill. Figure 5.3 shows the wafermaps containing the marginal dies observed in the analysis. These figures are generated with the help of an internal tool at NXP which can generate wafer maps according to different input conditions such as lot number, wafer number, test number, etc.

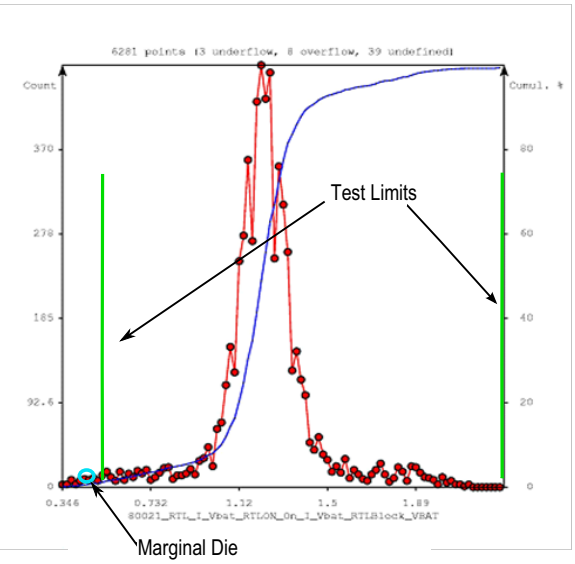


Figure 5.2: Example of a marginal die with the applied test limits

- **Site dependency:** The current production testing environment uses multisite testing. In a multisite testing environment several devices can be tested in parallel.

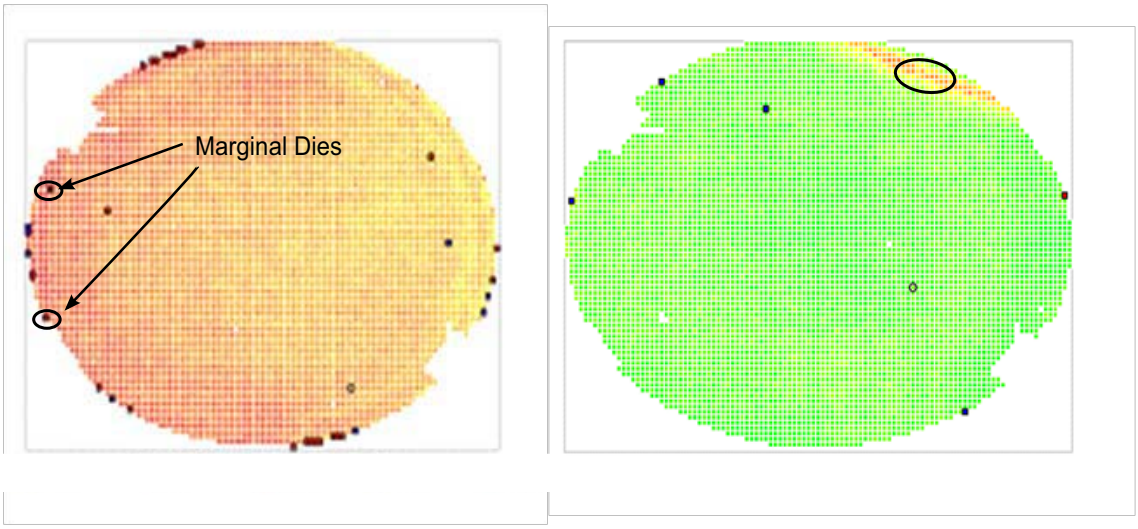


Figure 5.3: Wafermaps with two marginal dies (left) and a scratched wafer with marginal dies (right).

This increases the throughput and decreases the production cost. The current DUT (Device Under Test) is tested in quad-site ATE, where four devices can be tested in parallel. Site dependency is a problem associated with multi-site testing in an ATE. Site dependency usually occurs when one or more sites on a probe card performs differently as compared to the other sites. Since the site number is also present in the datalogs provided, the dies in different bins can be checked for site dependency issues. The 399 simulated tests correspond to the 17 failing bins out of the 25 considered bins. The site dependency issues have been observed for four bins out of 25. Figure 5.4 indicates the site dependency issue observed on one of the wafermaps where the yellow dies indicate slightly deviated measurements compared to the green ones.

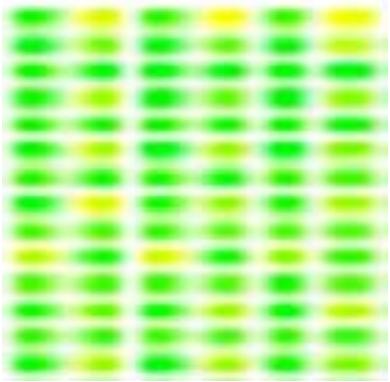


Figure 5.4: Portion of a wafermap where the yellow dies between the green ones indicate site dependency.

- **Test process issues:** Dies that fail due to test process are part of a cluster of 4, 3, 2 failing dies, striping etc. These types of failures are shown in Figure 5.5 with (2,3 or 4) sites failing, and can be caused by insufficient supply decoupling on the probe card. In such cases a hard fail on one site can cause deviating measurements on other sites.

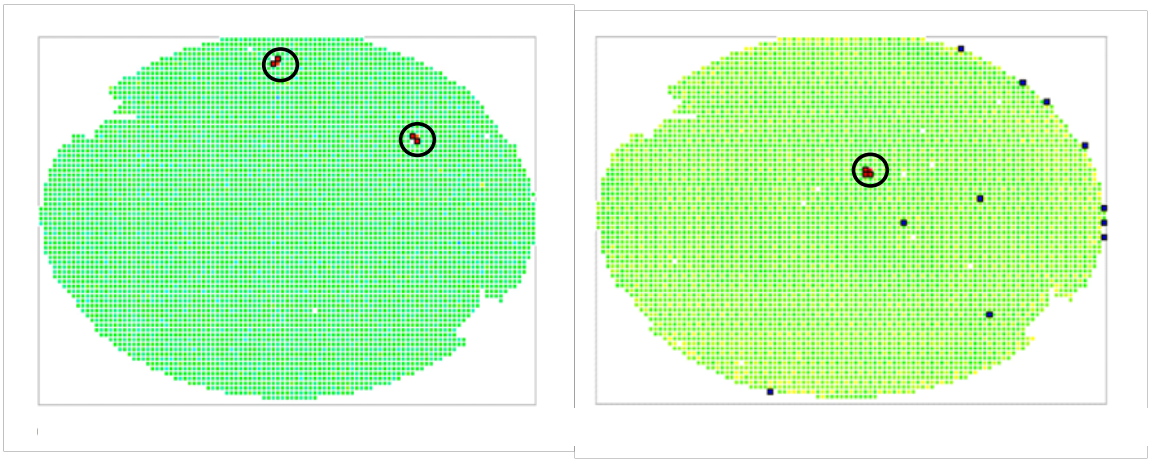


Figure 5.5: Example of dies that fail due to test process

- **Real escapes:** After checking all the above mentioned issues only, a die can be confirmed as a real test escape. Hence a real test escape can be termed as a die which is not caught by one of the 176 tests, fails at least one of the tests (other than 176 tests) in the original test set of 399 tests and does not falls in any of the above mentioned category.

  In the analysis, 11 escape dies were found with the reduced test set obtained by simulating just the bridging defects. The main goal of the further analysis includes to check if the escape dies can be caught by the test set obtained after including dislocation defects. This includes detailed diagnosis of these 11 ICs to confirm if they are suffering from the dislocation defects or not. The diagnosis procedure for these ICs is described in the next section.

5.2 Introduction to fault diagnosis

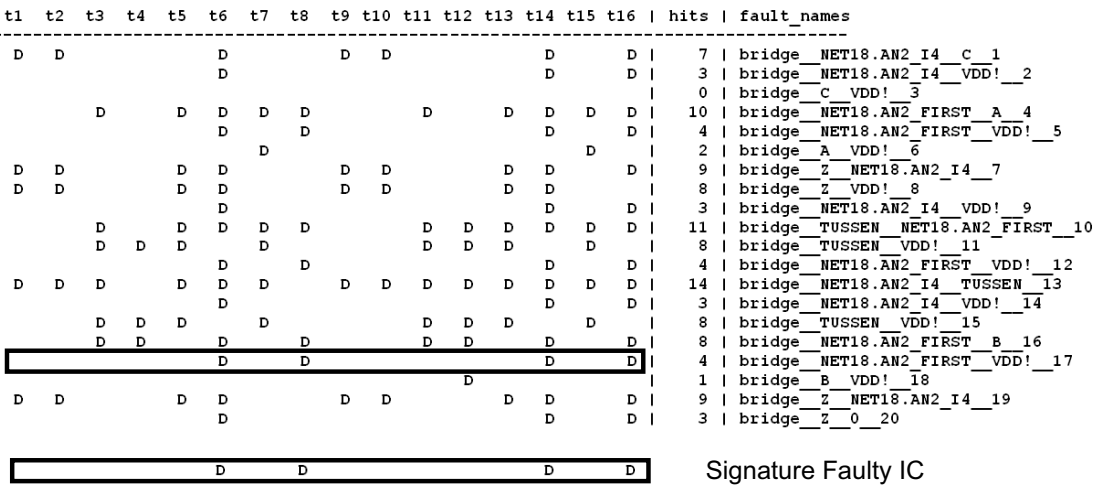
Fault diagnosis in digital ICs using Automatic Test-Pattern Generation (ATPG) tools speed up the failure analysis task to a great extent [36]. But in the arena of analog circuits, nothing comparable exists yet. For the past few decades, the subject of fault diagnosis in analog circuits has been of interest to researchers in circuits and systems. There are two main issues concerned with fault diagnosis: fault location and fault identification. The analog circuit fault location is an extremely challenging problem [37]. This is because of the less controllability and observability of the internal analog nodes, lack of good fault models for analog circuits similar to the stuck at fault models for digital circuits and the nonlinear nature of the problem [38]. For example, in an analog circuit

if a parameter value changes by a certain factor, the circuit responses may not change by the same factor even though the circuit is linear.

A fault dictionary based approach is used to diagnose the faulty ICs in this work. Fault dictionary based technique has been considered very effective to diagnose the catastrophic faults [37], which is the main focus of this study, since the parametric yield is close to 100%. The fault dictionary method can be understood easily with the help of an example. Long before the advent of digital computers, service manuals accompanying the electronic equipments usually contained a section on 'trouble-shooting' where a step by step testing procedure is explained, together with the table of symptoms and the possible causes, which in essence is a fault-dictionary approach. The first step in creating a fault dictionary is identifying the faults which are most likely to occur in a circuit [38]. This is a very important aspect of the entire methodology since only those faults can be identified. Since the main objective is to identify whether the missing ICs are suffering from dislocation defects, an extensive list for dislocation defects has been used in constructing the dictionary. Although the initial effort to generate a fault dictionary is quite demanding, but it can be very beneficial to the prediction accuracy of fault diagnosis once the dictionary is created.

An effective analog test stimuli is an essential component of the fault detection and diagnosis of the analog circuits. For example for the detection of defects that cause leakage related failures, current tests form an important part of the test stimuli to analyze the impact of defect. The Device Under Test (DUT) is simulated for the extracted defects in order to develop sets of circuit responses which can detect and isolate the faults. A simulation signature is defined as the observed response (pass or fail) obtained while simulating the defect for a particular set of tests. The signatures of the simulated defects are stored in a dictionary for use in the identification of faults. The signatures obtained at the time of production testing for the faulty ICs are compared with the simulation signatures. On finding an appropriate match, the fault can be diagnosed to identify the appropriate location of the fault. The defect list contains the net-names constituting the defect in a hierarchical fashion. In a hierarchical netlist, blocks are listed in a top-down fashion, so the precise location of a fault can be obtained. This information is very useful for diagnosing the customer returns and has been successfully applied at NXP semiconductors. When the test limits are applied to the simulation results stored in a fault dictionary, a detection matrix can be obtained. Figure 5.6 shows an example of the signature matching procedure of the simulation results with a faulty IC using a detection matrix. The signature of the faulty IC is available by observing the tests failed in the production environment.

Several diagnosis techniques have been proposed in the literature. The idea to rank simulated candidates based on the size of intersection of simulated signature and the observed behavior of faulty IC is presented in [39]. Three metrics for fault diagnosis have been proposed in the work of [40] - *intersections, mispredictions, and nonpredictions.* The metrics are obtained by computing the observed behavior of the faulty IC with the simulated candidate's behavior. Failures observed on both the ATE (Automatic test equipment) and predicted by a simulated candidate are termed as intersections. Mispredictions are the ones which are predicted by candidate fault but not observed at the ATE. Failures observed at the ATE but not predicted by the fault are called



t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15	t16	hits	fault_names
D	D				D			D	D				D		D	7	bridge__NET18.AN2_I4__C__1
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__2
																0	bridge__C__VDD!__3
		D		D	D	D	D			D		D	D	D	D	10	bridge__NET18.AN2_FIRST__A__4
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__5
						D								D		2	bridge__A__VDD!__6
D	D			D	D			D	D			D	D		D	9	bridge__Z__NET18.AN2_I4__7
D	D			D	D			D	D			D	D			8	bridge__Z__VDD!__8
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__9
		D		D	D	D	D			D	D	D	D	D	D	11	bridge__TUSSEN__NET18.AN2_FIRST__10
		D	D	D		D				D	D	D		D		8	bridge__TUSSEN__VDD!__11
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__12
D	D	D		D	D	D		D	D	D	D	D	D	D	D	14	bridge__NET18.AN2_I4__TUSSEN__13
					D								D		D	3	bridge__NET18.AN2_I4__VDD!__14
		D	D	D		D				D	D	D		D		8	bridge__TUSSEN__VDD!__15
		D	D		D		D			D	D		D		D	8	bridge__NET18.AN2_FIRST__B__16
					D		D						D		D	4	bridge__NET18.AN2_FIRST__VDD!__17
											D					1	bridge__B__VDD!__18
D	D			D	D			D	D			D	D		D	9	bridge__Z__NET18.AN2_I4__19
					D								D		D	3	bridge__Z__0__20
					D		D						D		D		Signature Faulty IC

Figure 5.6: Example of signature matching with the help of detection matrix

nonpredictions. A signature matching method based on impact factor is used in this work which is presented in the next section.

5.3 Fault diagnosis using effective signature matching

For diagnosing the 11 faulty ICs, the first step involves obtaining the signature for the failed tests. The production data for all the ICs is present in a SQL database. The measurement values for all the simulated tests (399) are obtained from the database using the lot number, wafer number and, x and y coordinates of the dies. The pass/fail information for different tests is obtained by applying the test limits and thus the signature is obtained for the faulty IC. The signature for each of the faulty ICs is compared with the signatures present in the simulation database. For the initial part, signature matching was done manually utilizing only the pass fail information in a spreadsheet like analysis. A signature match was found for an IC failing for two tests. To be sure about the signature match, further investigations were required. A deeper investigation revealed that the IC was just outside the limits for the two failing tests, and was just inside the limit for two other tests. All these four tests were big outliers (hugely deviated from the main population of ICs in the same wafer) for the IC under investigation. These four tests have huge impact on the IC, although for two tests it is visible directly, since it is just outside the test limit. These cases can also be observed by tightening the limits to modify the detection status or a simpler method such as an impact factor based analysis can be used. Figure 5.7 presents the concept of impact factor graphically and Equation 5.1 shows how the impact factor is calculated for the simulation. An impact factor of 100 signifies the simulated value lies exactly on the test limits.

$$Impact factor(simulation) = \frac{(\text{Simulated test value} - \text{Mean measurement})}{\frac{\text{Limit window}}{2}} \times 100 \quad (5.1)$$

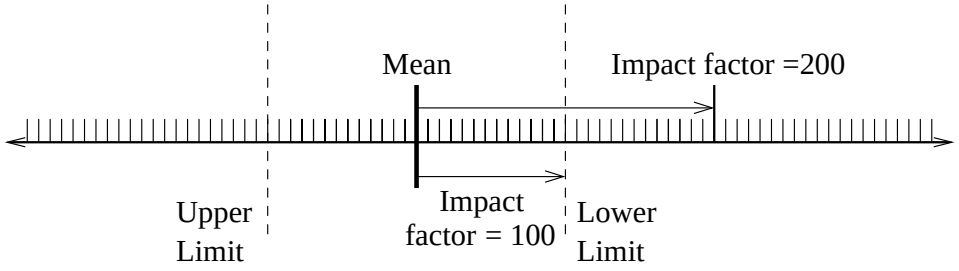


Figure 5.7: Calculaton of impact factor

where *Limit window = Upper Limit - Lower Limit* and *Mean measurement = (Upper Limit + Lower Limit)/2*.

Equation 5.2 shows the calculation of impact factor for the measured values of the faulty IC. In case of calculating the impact factor for the faulty ICs, a median value is used instead of the average value of the limits. A median value indicates where maximum population of the good dies are located. Average value of the measurements over the whole wafer might be shifted, because of some hard failures (strong deviations) in some of the IC and might not solve the purpose of calculating the impact factor based on the measurement of good ICs.

$$Impactfactor(measurement) = \frac{(\text{Measured test value} - \text{Median measurement})}{\frac{\text{Limit window}}{2}} \times 100 \tag{5.2}$$

where median is calculated for the measurements over the wafer for that particular test

The impact factor for test T1 & T2 found for the IC under consideration was found to be 106% & 110%, while the impact factor for T3 & T4 is 98% & 95% (just undetect). Although the impact was marginally less than the impact percentage required for detection (impact factor of more than 100% signifies detection), the IC was still an outlier for the test T3 & T4. Therefore a significant impact was expected for the test T3 & T4 in the case of simulations. But no such impact was found in the simulation signature for tests T3 & T4. Hence, it was discarded having suffering from dislocation faults.

In the analysis of dislocation defects in Chapter 4, we saw that the detectability of a defect decreases with the increase in resistance, therefore it is an appropriate assumption that the detection status of a defect is also affected by the resistance values. Table 5.2 shows with an example how the signature of a defect can be affected by different resistance values. The same defect is detected by four tests in the 1K resistive range and is detected by only one test in the 100K resistive range. Since the defect is simulated across three resistance values, an impact factor based analysis can provide much more depth in the diagnosis of these defects. Hence, the further diagnosis procedure is carried out with the help of impact factor.

In this analysis, the signature matching procedure is based on the impact factor. This method takes into account the modeling issues in simulating defects discussed in Chapter 4. Impact factors are calculated for all the test responses for the faulty ICs and

Table 5.1: Variation of the detection status of a defect across various resistance values

	T1	T2	T3	T4	T5
1K Resistance	D	D	D		D
10K Resistance	D	D			D
100K Resistance	D				

are matched with the calculated impact factors obtained from the simulation database of dislocation defects. In order to effectively diagnose the faulty ICs based on the different impact factor, the automation of the signature matching task is done with the help of a perl script (Figure 5.8).

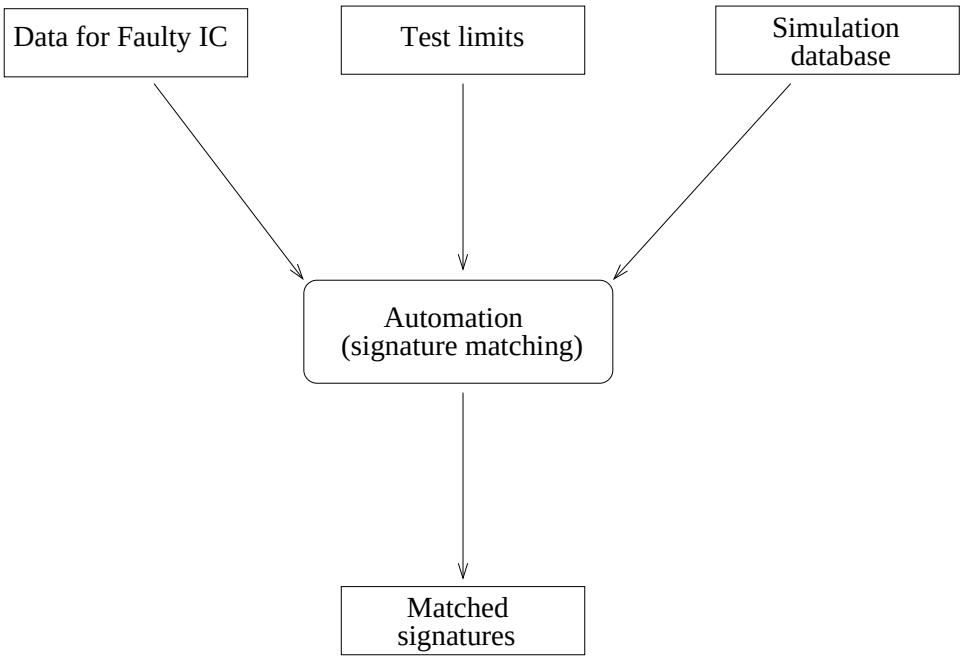


Figure 5.8: Automation of signature matching

The automation script takes the measurement values of the faulty IC, test limits and simulation database of dislocation defects as input. The measurement values of the faulty IC are obtained from the available production data. In the initial phase, all the impact factors for the measurement values corresponding to different tests in a faulty IC are calculated and stored. In the second phase simulation database is parsed. Each row of the simulation database contains the simulation values for the single dislocation defect. The information available in the simulation database is parsed row by row and the impact factor of different tests corresponding to each defect is calculated. The script has a provision in which a predetermined impact factor can be set in the script. The script then matches the signature from the silicon results with the simulation based on the supplied impact factor. The match (if found) for a particular test between the

signature of a faulty IC and a simulated defect is presented in the final output of the script. Table 5.2 shows the output (sample) of the script for the impact factor 50. The script outputs the matches found in the faulty IC with the simulated defects along with the tests matched (last column). For example, the faulty IC has 7 tests having an impact factor greater than 50, the defect D1236 has 11 tests with the same impact factor and the number of tests matching in both the signatures is 4, which makes defect D1236 the best candidate according to other matches. The number in column 3 (faulty IC) always remains constant because the results correspond to a single faulty IC.

It can be seen that the less matches are found for a higher value of the impact factor (90) for the same faulty IC (Table 5.3). It is because the higher value of impact factor implies that the measurement results (signature and silicon) are more deviated from the mean value. For defect D1236, the matches become half and the impact seen on silicon and simulation does not reduce considerably, which indicates its not a high ohmic defect nor a low ohmic defect.

Table 5.2: Sample output of the script for impact factor 50

Defect	Matches	Faulty IC	Simulation	Tests
D1236	4	7	11	T3, T9, T57, T231
D245	3	7	13	T13, T173, T189
D798	2	7	17	T145, T312
D564	2	7	19	T27, T138
.	.	.	.	.....
.	.	.	.	.....

Table 5.3: Sample output of the script for the impact factor 90

Defect	Matches	Faulty IC	Simulation	Tests
D1236	2	4	7	T3, T57
D245	2	4	9	T173, T189
D798	1	4	10	T312
D564	1	4	11	T27
.	.	.	.	.....
.	.	.	.	.....

After a thorough analysis of the script results for all the faulty ICs, it was found that no satisfactory signature match was found with the simulation database of the dislocation defects. An important conclusion that can be drawn at this stage is that there is not sufficient evidence to show that the current production data set under analysis is suffering from dislocation faults. However, the dislocation faults are stress-induced and greatly depend on the process variations. Hence if these defects show up in future in the production testing, the test set obtained for dislocation defects can be used.

5.4 Characteristics of undetected devices

Out of the 11 faulty ICs considered for analysis, 8 were detected when the constraint to include at least one supply condition for each production test was implemented. The remaining 3 ICs were closely investigated for the failing tests. Closer investigation revealed that in all cases the devices are marginal fails for a non-selected test and marginal passes for a selected test. Figure 5.9 shows the example of one the missed devices. The figure shows a density plot for two analog test parameters. The central distribution indicates the region where most of the good devices are located, the dot in the lower left corner represents the missed device and the two lines represent the pass/fail limits of the two tests. The IC under investigation will fail the non-selected test and will just pass the selected test. The same situation was observed for the other two ICs.

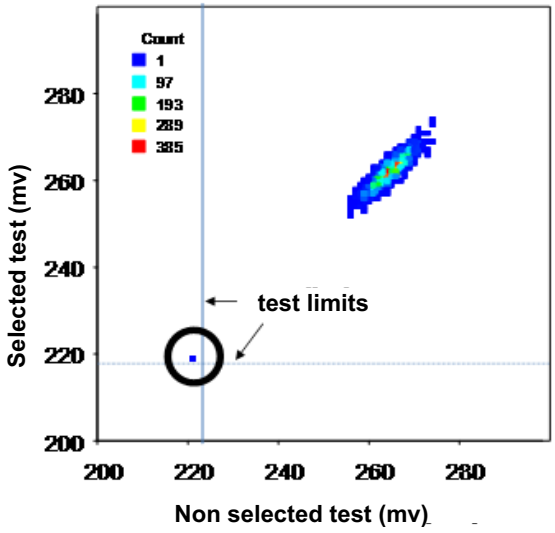


Figure 5.9: Example of a device missed by a selected test (y-axis) and detected by a non-selected test (x-axis), pass fail limits are marked by thin lines

In Table 5.4 the deviation of the three ICs in terms of the impact factor (impact factor of 100 being exactly at the pass/fail limit) is shown. For the selected test, the device is just missed, i.e, <100, while the non-selected, detection test just detect the device, i.e. >100. Scaling the deviation to the specification limit, shows that in all three cases the test results are still well inside the specification limits (last column of Table 5.4). For IC1 it shows that the test limits are seven times more stringent than the specification requirements. For IC2 it is around four times and around two times for IC2. This indicates that the IC may be meeting functional requirements, but for high quality standards in automotive, ICs hugely deviated from the main population are generally thrown away, so that they do not pose reliability risks in the future.

In general the usage of greedy algorithm helps to select the more sensitive tests, however, sometimes the impact of the defect will be close to the pass/fail limit and the result will depend on the 'chance' of selecting/rejecting the test that just detects or misses the failing IC. In the examples of Table 5.4, small shifts from process variations

Table 5.4: Characteristics of undetected devices

Device	Selected test	Detection test	Spec
IC1	99	108	13
IC2	97	106	23
IC3	87	112	55

will determine if a specific test can detect an IC or not. However, the detectability of these ICs is ensured by using adaptive tests. In adaptive tests the pass/fail result depends on more information than the test results of a single IC [41]. The adaptive test method used in this design is the so-called moving limits method in which the limits depend on the results of previous DUTs [42]. This method is capable of detecting devices which deviate strongly from the main population as is the case for the three missed ICs (see also Figure 5.9). The test time overhead of a moving limit test is small. Hence, by adding the selected test to the moving limit set the detection of all anomalies without an increase in the test time and therefore meet the test time reduction goals in combination with zero defect requirements.

6 Conclusion and Future Work

This thesis presents a Defect Oriented Testing (DOT) flow for an automotive Analog/Mixed-Signal (AMS) IC. DOT has been proposed as a structural test method for AMS ICs. The basic steps involved in the DOT flow, such as defect extraction, defect simulation, test optimization and validation are discussed in detail. The main focus of this research work is the analysis of dislocation defects for the IC under consideration. A schematic based flow is developed to extract the dislocation defects and the behaviour of these defects across various resistance values is analyzed. Various test selection approaches are compared to obtain the optimal test set required for detecting dislocation defects. Finally, the validation results with production data are presented.

This chapter summarizes the overall investigation and achievements. Section 6.1 briefly discusses the overall conclusions. Section 6.2 proposes some further research topics.

6.1 Conclusion

The primary failure mechanisms in the IC under consideration are known from the production data. The bridging defects (shorts) and the dislocation defects are the major yield-limiting factors. For extracting the bridging defects an Inductive Failure Analysis (IFA) like approach is utilized. The IC layout is passed through a parasitic capacitor extractor and the bridging defects are extracted. The probability of the relative likelihood of occurrence of the bridging faults can also be calculated based on the capacitance value between the two conducting layers.

Dislocation defects are induced by stress during various IC fabrication steps and cause leakage related failures. An extensive literature survey has been presented to understand the root cause of these defects and the associated failure mechanisms. A novel schematic-based methodology has been proposed to extract these defects by studying the various cross-sections of the devices susceptible to dislocations. By performing the dislocation defect extraction as proposed, the defect list can be *limited to only 8% of the total active devices present in the IC.*

In the DOT flow, defect extraction is followed by simulating the defects. Results of the defect simulation for bridges are discussed. Dislocation defects disrupt the regular crystalline structure of silicon and tend to show a high resistive behavior. Hence, these defects are simulated for four different sets of resistance values (in high resistive range) to observe the detectability status across various resistance values. An important observation that has been made during the analysis of these defects is: *the detectability of a dislocation defect decreases as the resistance value increases.*

Simulation of dislocation defects is followed by the generation of a detection matrix. A detection matrix contains the detection status of a defect across various tests. This

detection matrix can be used for the purpose of test optimization and failure analysis. Test optimization is the process of selecting a minimal test set to cover all the (detectable) defects. An optimal test set of 176 tests (out of 399) is required to detect all the bridging defects. However, during the validation process with production data some ICs got escaped. Since, dislocation defects are the second-most important failure mechanism (after bridging defects) for the considered IC, an extra test set is required to detect all the dislocation defects. Algorithms such as 'greedy' and 'unique detects first', have been used to obtain the optimal test set covering both the bridging defects and the dislocation defects. Various industrial constraints are also described and have been incorporated in the optimal test selection flow. Since the amount of extra tests required to detect the dislocation defects is small, the results obtained from both the algorithms have almost the same number of tests. A reverse approach has also been used, to first obtain the tests for detecting the dislocation defects, and then derive extra tests for detecting the bridging defects. The test set obtained with the reverse approach is slightly smaller than the previous approach. An important conclusion that can be drawn from the test selection process is: *the dislocation defects do require extra tests for detection.*

The optimal test set obtained is then used to validate the production test data for 1.3 million dies. The test data in general is not 'perfect' and needs to be checked for the good ICs which are rejected due to the issues of site dependency, marginal fails and issues associated with the tester. Hence, these anomalies need to be identified in the validation process. While validating the test data with the reduced test set (176 tests) obtained only for bridging defects, some ICs escaped. A fault diagnosis procedure was used to check if the escaped ICs can be explained by dislocation defects. A fault dictionary based approach is used for the diagnosis purpose. The simulation signatures obtained for dislocation defects are matched with the signature of the faulty IC. An analysis based on impact factors is used to effectively match the signatures. The results of the signature matching procedure reveal that the current production test set does not suffer from dislocations. If these defects show up in the future, the extra test set obtained for the dislocation defects can be used. However, *currently no additional tests are required for the detection of dislocation defects.*

6.2 Future work

The dislocation defects for this research work have been extracted by the schematic-based approach. A realistic extraction approach to extract these defects based on layout can also be developed. The performance comparison of both the approaches can be done by simulating the defects and validating the results with available silicon data. The case of study for this research work is an automotive product with zero defects quality requirement. This thesis presents the results for bridging defects and the dislocation defects. Other failure mechanisms such as opens can also be analyzed by appying the whole DOT flow.

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A Schematic-Based Extraction Methodology for Dislocation Defects in Analog/Mixed-Signal Devices

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Abstract

This paper presents a defect extraction methodology for dislocation anomalies in analogue-mixed signal (AMS) Integrated Circuits (ICs). Dislocation defects can cross the PN junction of a transistor/diode and contribute to leakage related failures. The extraction of dislocation defects from layout information is very difficult. We propose a methodology that accepts a schematic (netlist) of the AMS design and generates a list of dislocation defects by identifying the hierarchical net names of each defect. The methodology parses the schematic (netlist) and locates dislocation defects according to pre-determined rules. The cross section of different devices from the design manual of a process technology are studied and the possible dislocation spots related to PN junctions are listed in a rule file. This methodology is applied to five AMS IC products and a considerable amount of simulation time can be saved by truncating the defect list to the extracted dislocation susceptible spots.

Keywords

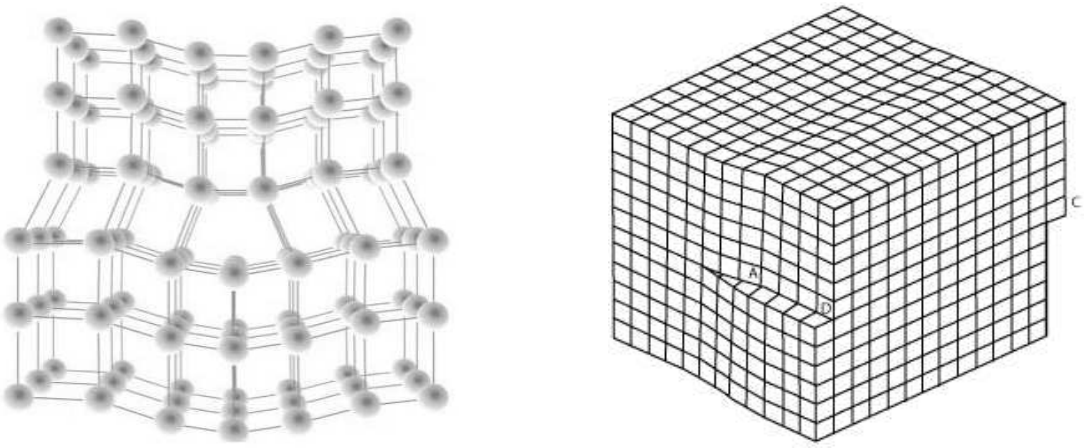
Dislocation Defects, Schematic, Defect Extraction, Defect Oriented Test, Analog Mixed-Signal Testing

I. Introduction

Analogue and Mixed-Signal (AMS) testing takes a considerable portion of the whole test cost of a chip [1]. Mostly, AMS ICs are tested functionally or specification based. Structural testing methods for digital ICs have been around for decades and are very well adopted by the industry. Testing AMS ICs in a structured manner is still in its infancy stage [2]. Defect Oriented Testing (DOT) is an approach in the direction of structural testing for AMS ICs. DOT flow generally consists of defect extraction, fault modeling, fault simulation and test application. This work focuses on the defect extraction of dislocation related faults. Dislocation defects tend to show a high resistive behavior and the observed leakage current is significantly less than the circuit with bridge (short) defects. Dislocations may not result in a complete failure of the IC, but may pose a reliability risk (i.e., the IC fails over time). It is typically very challenging in AMS testing to detect these defects. High stress levels in a substrate are associated with dislocation defects. High accumulation of stress during formation of Shallow Trench Isolation (STI) structures and oxidation steps can extend the effect of dislocations to larger distances. IC fabrication process also involves stress build up, examples are the use of materials having thermal expansion coefficients different than silicon, deposition of films with intrinsic stress and non-planar surface oxidation [3].

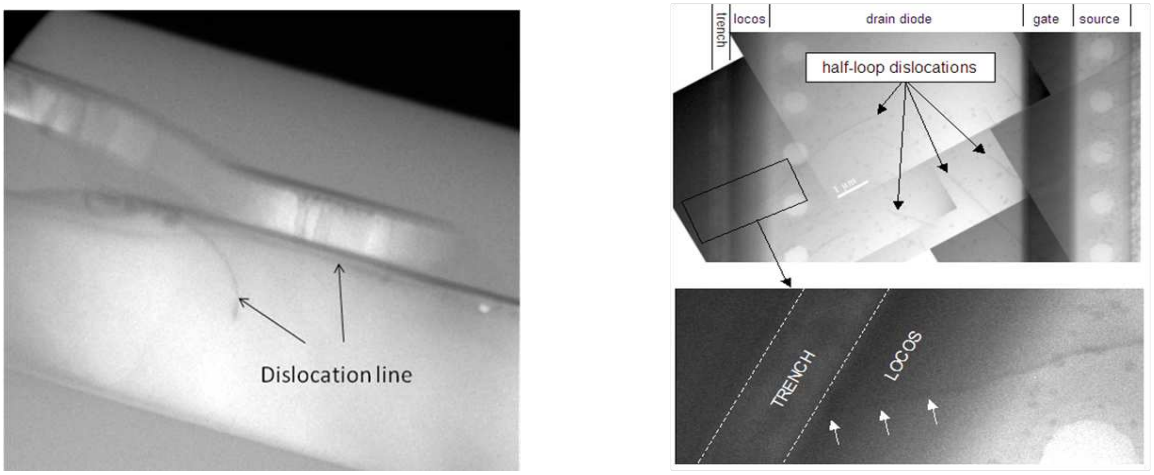
There are two basic types of dislocations, edge dislocations and the screw dislocations. Figure 1(a) shows the edge dislocation defect with an extra plane of atoms in upper crystal lattice, disrupting the regular crystal structure. Screw dislocations are shown in Figure 1(b), where a step or ramp is formed by displaced atoms in a crystal plane. Both edge and screw dislocations belong to the category of line defects. Edge dislocations move in parallel with the direction of the shear stress applied, whereas the defect line movement in a screw dislocation is perpendicular to the shear stress. Dislocation loops are formed if a dislocation containing the extra or missing plane of atoms lie entirely within the crystal. Most of the times, the dislocations are the hybrid combination of edge dislocations and the screw dislocations. Transmission Electron Microscope (TEM) images of some of the observed dislocation defects are shown in Figure 2. Dislocation line defect is shown in Figure 2(a) and the half loop dislocation faults are shown in Figure 2(b). Half loop dislocations are caused by pitting of trench sidewall during trench oxidation and Figure 2(b) reveals their origin from the trench.

Dislocations have been identified as one of the major contributors to the leakage related failures, while crossing PN junction of a device [4][5][6]. Formation of dislocation defects is a two step process: 1) the dislocations should be nucleated and 2) they should grow into areas where they can affect device characteristics [7]. The nucleation of dislocation defects has been attributed to process mechanisms such as ion-implantation and oxidation [8]. Ion-implantation is used in many steps of advanced bipolar and CMOS technologies, it disrupts the regular crystalline structure of silicon and subsequent



(a) (b)

Figure 1. Crystal line defects: (a) Edge dislocations with extra plane of atoms in the lower part of crystal lattice (b) Screw dislocation with screw-like slip of atoms in the upper part of crystal lattice [18].



(a) (b)

Figure 2. TEM image of (a) dislocation line defect and (b) half loop dislocations originating from trench.

annealing steps are required to repair this damage. Even after treating the silicon substrate with annealing steps, some crystal structure residual damages are always left [9]. This residual damage does not alter the device characteristics if it is present in the areas outside the space-charge (critical) regions of the device. However, high stress built up in device structures have a compounding effect on these defects, which can become dislocations and can propagate to larger distances [3]. Much of the work has been performed on the root causes and behavior of dislocations [3][8][10]. Nevertheless - to the best of our knowledge - none of them has addressed the extraction of these defects.

This paper presents a methodology for extracting dislocation defects in AMS products. Extraction of dislocation defects from layout is quite cumbersome, requires much detailed information and is very slow. Mostly, the extraction tools are made for parasitics extraction (e.g., Cadence Assura). Separate rules have to be created to recognize the dislocation susceptible PN junctions based on layout geometry which is a very demanding task. Hence, a schematic-based flow is proposed. The main idea is to identify potential dislocation defects per device (transistors, diodes, etc.) type by studying its PN junctions and the surrounding electrical isolation structures. This is achieved by analyzing the device cross section present in the (process)

design manual. All the possible PN junctions susceptible to dislocation defects are listed in a rule file.

A script written in PERL language parses the product netlist and the rule file as inputs and provides the dislocation defect list as output. The extraction framework developed is generic and can be applied to any product manufactured in the process, whose design manual is implemented in the rule file. The five AMS products considered in this work for dislocation defect extraction belong to the category of transceivers and are manufactured in a BiCMOS-DMOS (BCD) process, supporting very high voltage levels (over 40 V). These are automotive products and have zero defect quality requirements. In many devices, STI structures have been used for performing electrical isolation of the devices.

The rest of this paper is organized as follows. Section II discusses about the prior work done in order to analyze the dislocation defects. Section III presents the details about the different steps involved in the extraction of dislocation defects. Various steps involved such as the analysis of devices from process manual, details about the rule file and the fault extractor are discussed in this section. The results of the extraction are presented in section IV and the conclusion is presented in section V.

II. Related Prior Work

Dislocation defects have attracted the researchers and continuous effort has been put to understand the behavior and the root cause of these defects. [3] provides an excellent study to understand the stress induced dislocation defects. Work in [3] focuses on the effect of different process steps used in IC fabrication process such as oxidation, ion implantation and their role in the formation and promotion of dislocation defects. Stress levels associated with shallow trench isolation structures (STI) are also discussed in detail. Stress induced by gate stack formation also helps in promotion of the dislocation defects [11]. The effect of dislocation velocities in heavily doped silicon substrate is studied in [12]. It was found that in n-type silicon, the dislocations behave as acceptors and a donor like behavior is shown in p-type material. This is the underlying cause for the formation of leakage path in the device junctions affected by dislocations [13].

In a separate work, detailed Transmission Electron Microscope (TEM) imaging of these defects is done to perform the in-depth analysis [8]. Physical information about the defect is related to the observed electrical characteristics, by measuring various leakage currents. Figure 3 shows the measured drain-source current corresponding to the dislocation defect which was observed, spanning from source to drain terminals. The reference transistor curves point to the drain current versus drain voltage of a MOS transistor at different gate voltages while the leaky transistor curves illustrate how the normal behavior of the transistor can be affected due to the dislocation defect.

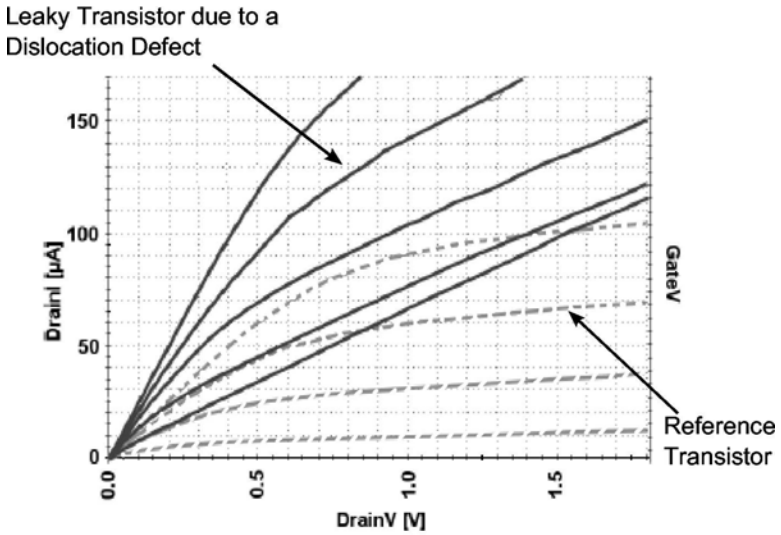


Figure 3. Electrical characteristics of a failing transistor (dark lines) due to source-drain leakage current as compared with a reference transistor (bright lines) [8].

Bipolar analog devices have also been shown to be considerably affected by trench processing conditions resulting in altered device characteristics [14]. It has been shown that stresses and dislocations caused by silicon on insulator (SOI)/trench processing can result in collector-emitter (I_{ceo}) leakage current. In a similar study done in [15], dislocation defects were found in STI/SOI CMOS devices. The dislocation defects found in this study, can become electrically active only if they extend the entire distance for source to drain.

Defects can be extracted at different levels of details. An Inductive Fault Analysis (IFA) like approach utilizes the layout details of a design [16]. This methodology is adopted in [17] to extract the shorts/bridges for an industrial mixed signal chip, where the layout details are passed to a parasitic capacitor extractor and the capacitance values are used to calculate the probability of short between two nets. These nets can be either, two metal tracks, two polysilicon layers or a metal and a polysilicon layer. There, the level of abstraction is layout and the parameter used for defining the set of rules for extraction is parasitic capacitance. A similar analogy can be drawn for the extraction of dislocation defects where the level of abstraction is netlist (or design schematic) and the rules are derived from studying the process design manual of different devices, where the possible dislocation defects can occur.

III. Extraction Framework

Figure 4 shows the main steps involved in the extraction of dislocation defects. The important steps involved in the extraction of dislocation defects include the analysis of design manual, creation of rule file and the implementation of fault extractor. In this section, the details of each step are presented. A device structure obtained from the process design manual is also shown and discussed at the subsequent steps of the flow.

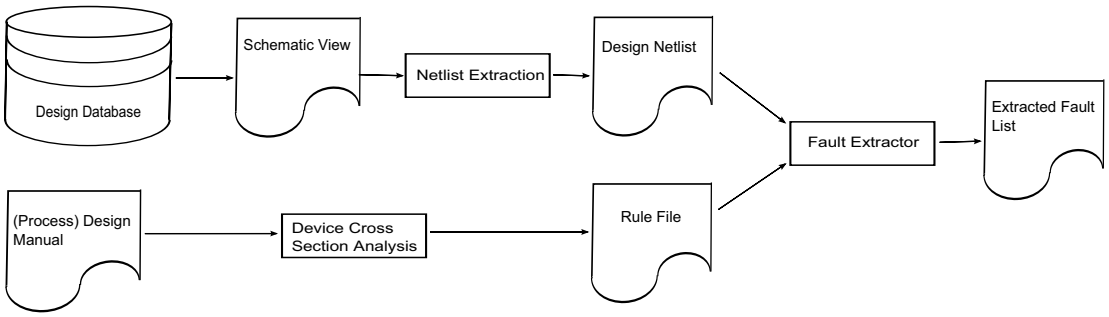


Figure 4. Extraction framework for dislocation defects.

A. Analysis of Design Manual

The DUT has many different types of devices present in the design database. These devices are instances of models present in the design manual. Examples are different types of diodes, capacitors, MOS transistors and Bipolar Junction Transistors (BJTs). These devices are fabricated to operate at different conditions, for example voltage levels can vary in the range of low, medium to very high voltage levels (120 V).

The goal of the design manual analysis is to carefully study the cross-section of all device models to understand the formation of device structures and the PN junctions potentially susceptible to dislocation defects. For example, isolation structures surrounding certain devices play an important role in the formation of dislocation defects and they have a significant contribution while analyzing the process models.

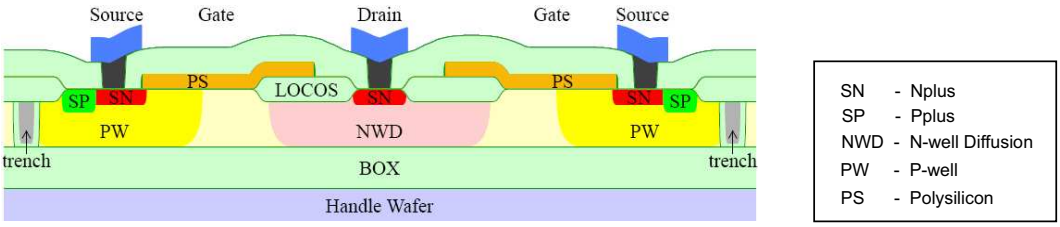


Figure 5. Process Design block of an NMOS transistor with fold=2 (drain centered device).

Figure 5 shows the cross-section of an extended drain N-channel MOS device, with maximum gate voltage as 12V and maximum drain voltage as 60V from the design manual of a BCD process. As can be clearly seen from the figure, the device is surrounded by a trench isolation structure that is filled with oxide and undoped polysilicon down to the buried oxide (BOX). These trenches can aid in the formation of dislocation defects. In such a device, if a dislocation defect is

present which extends in the channel region, then a source-drain leakage current is observed. Many other devices such as BJTs and diodes have also been identified as the potential target for dislocation defects.

B. Rule File Creation

After analyzing the cross-sections of all the device structures in the design manual, a rule file is created. The rule file is a text file that includes an entry for each of the devices where at least one dislocation-susceptible junction can be present. The entry for a device includes its model name from the design manual (which is later matched with the device instances in the netlist), the list of all its pins (contacts), and the potential dislocation defects between its pins.

The pins must be in the same order designer uses when he instantiates devices of that model. For example, the standard order of drain, gate, source, body, (D,G,S,B) is used for a MOS device. The potential dislocations are given by pairs of pins (contacts) along which the leakage current can occur due to dislocation defect. The pin names are separated by whitespace, e.g, a dislocation between source and drain of a MOS device will be written by "S D" in the rule file. Comments are possible in the rule file for the sake of readability. In our implementation, the model name, pins, and dislocation defects must each occur on a separate line. The entry ends with the keyword "end".

For the device shown in Figure 5, the model name is SMNDE and the contacts to this device are Drain (D), Gate (G), Source (S), Body (B) and Handle Wafer (HW). The only potential dislocation defect is between S & D pins. The basic structure of rule file and the corresponding entries are shown in Figure 6. Similarly, many diode structures and BJTs, susceptible to dislocation defects are identified from the design manual and the corresponding rule file entries are created.

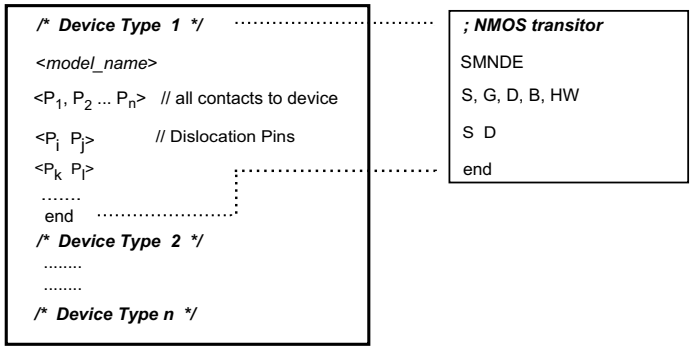


Figure 6. The structure of a rule file (left) and an example (right).

C. Fault Extractor

The fault extractor takes the rule file and the design netlist as input and is written in PERL language. The netlist extracted from design database is in PSTAR[1] format. The fault extractor parses the netlist and flattens the design hierarchy. This is necessary such that the hierarchical net names can be obtained. After flattening, every device instance in the netlist is checked versus all the device models in the rule file. If the model of the device instance matches any of the device models in the rule file, the pins corresponding to the potential dislocation defects of that model are extracted by finding their hierarchical net names. The hierarchical net names are written in the output file as a potential dislocation defect.

For the MOS device shown in Figure 5, the device instance names present in the netlist are matched with model name of the MOS device and the pins (S & D) for the potential dislocation defect are obtained. The hierarchical net names for the corresponding source and drain contacts are then added to the defect list. The basic functionality of the fault extractor is shown in Algorithm 1.

Example: A high voltage N-type DMOS based (HV-NDMOS) diode is shown in Figure 7. This simple device is used to analyze the whole flow. The diode is formed between the drain contact and SPD (body diffusion). The anode is contacted by SP and the drain forms the cathode. PS (polysilicon) is also contacted to anode. The PN junction diode thus formed is susceptible to dislocation defect. There are three contacts to this device, namely, anode (A), cathode (K) and handle wafer (HW). The pins for potential dislocation defect are anode and cathode. Therefore, the information about the contacts and

[1]The in-house analogue simulator of NXP.

Data: Netlist and Rule file
Result: Extracted Defect List for Dislocations
read the netlist and flatten design hierarchy;
read the rule file;
$D \longleftarrow \emptyset$; `// Defect set, initially empty`
foreach *device instance in the netlist* **do**
  get the device instance model;
  foreach *device model in the rule file* **do**
    get the device model;
    if *the device instance model in the netlist = device model in the rule file* **then**
      foreach *dislocation defect in the model* **do**
        get the dislocation defect pins;
        get the hierarchical net names attached to the pins;
        $D \longleftarrow D \cup \{hierarchical\ net\ names\}$;
      end
    end
  end
end

Algorithm 1: Algorithm for fault extractor.

the pins for dislocation defect is to be supplied in the rule file. In the subsequent step, the fault extractor is executed with the design netlist and the rule file as input. After flattening the design hierarchy in the netlist, all device instances in the (flattened) netlist whose model is the HV-NDMOS (diode) are identified. For each instance of HV-NDMOS model, the hierarchical net names corresponding to anode and cathode of the HV-NDMOS diode are added to the defect list.

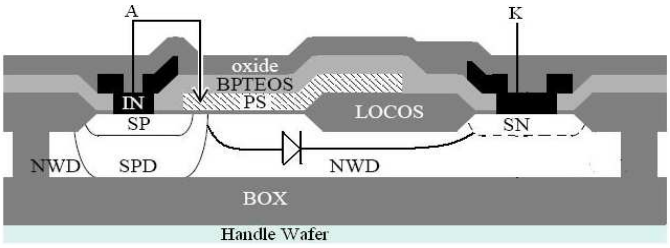


Figure 7. The cross-section of a high voltage N-type DMOS based transistor.

IV. Results

The extraction methodology developed for dislocation defects is applied to five AMS IC products which are all manufactured in the same BCD process technology. The design manual of the BCD process technology is studied to identify the potential dislocations in the device structures and a rule file is made (one time effort for all five ICs). For each product, its netlist and the rule file are passed to the fault extractor to obtain the dislocation fault list of the product. The extraction results for the five AMS ICs are presented in Table I.

Table I
Extraction results

	Product A	Product B	Product C	Product D	Product E
Number of Active Devices	16859	16720	8374	8950	5098
Number of Dislocation Defects	1438	809	2240	2423	1319

Product A and Product B have more active devices and less dislocation defects because they have a larger digital block whose transistors are not considered in the rule file. The defects associated with these transistors are considered to be

detected by digital testing methods, such as IDDQ and stuck-at testing. As shown in Table I, the number of susceptible dislocations is between 5 to 25% of the active number of devices. By performing the dislocation extraction as proposed, we are capable to limit the defect list. This is useful in guiding failure analysis to relevant locations as well as speeding up the DOT process. In DOT, one uses an extensive defect list which is simulated. Truncating the defect list to relevant defect locations reduces the simulation effort considerably.

V. Conclusion

A schematic-based flow is developed to extract the potential dislocation defects in AMS ICs. Device structures present in the design manual are analyzed to identify the potential dislocation defects and the corresponding rules are created in a rule file. A fault extractor script is developed which generates a defect list from the IC netlist according to the extraction rules. The extraction methodology developed is generic and can be applied to any process technology. The extraction flow developed is successfully applied and verified on five AMS products.

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