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An Area-Optimized Digitally-Assisted DAC Employing a Matrix-Based DEM Scheme

Alex CALINESCU[1], Traian ANTONOVICI[2], and Marius ENACHESCU[1,*]

[1]Dept. of Devices, Circuits and Architectures, National University of Science and Technology Politehnica Bucharest, Bucharest, Romania
[2]Electronic Instrumentation Laboratory, Technical University of Delft, Delft, Netherlands
Email: alex.calinescu@stud.etti.upb.ro,
T.Antonovici@student.tudelft.nl, m.enachescu@upb.ro*
* Corresponding author

Abstract. The Dynamic Element Matching (DEM) technique's role is to mitigate mismatch issues in complex, matrix-based systems. Previous work employing a matrix-based random DEM scheme demonstrated enhanced linearity and spectral characteristics in the Digital to Analog Converter's (DAC) thermometric decoded section. This paper presents the design of an area-optimized, DEM-assisted 9-bit segmented DAC. The optimal segmentation level for area-performance is initially established. Subsequently, to mitigate area constraints from the integral nonlinearity (INL) requirement and improve spectral performance, we utilize the matrix-based DEM engine from prior research. The proposed 9-bit DAC, implemented in a commercial 180 nm CMOS process, achieves a total harmonic distortion (THD) of -79 dB and a spurious-free dynamic range (SFDR) of 79 dB, resulting in 8× and 16× improvements in SFDR and THD, respectively, over its non-DEM counterpart.

Key-words: DAC; DEM; digital controller; DNL; INL; mismatch; THD; SFDR.

1. Introduction

High-resolution digital-to-analog converters (DACs) shape the audio systems high-fidelity (hi-fi). Unfortunately, component mismatch introduces nonlinearity, which degrades system performance. As demonstrated in [1], segmentation is an effective approach to reducing differential nonlinearity (DNL) in DACs, though it comes at the expense of increased chip area. This technique involves partitioning the DAC into multiple segments, each encoded in either a binary or thermometric format, with an additional digital decoding step required to convert input data accordingly. A common design approach, such as that described in [2], employs a thermometer-coded most significant bit (MSB) segment alongside a binary-coded least significant bit (LSB) segment. While segmented DACs help mitigate DNL, they require additional area for decoding circuitry and routing, and they do not inherently improve integral nonlinearity (INL).

To further enhance the precision of analog and mixed-signal systems, the Dynamic Element Matching (DEM) technique has been widely adopted [3]. Prior studies [4] have utilized DEM to reduce gain errors in instrumentation amplifiers. Moreover, in [5], a digital control circuit implementing a DEM algorithm was integrated into a 16× programmable-gain amplifier (PGA), reducing gain error to the parts-per-million (ppm) level. It has been shown in [6] that adopting a matrix-based random DEM scheme can improve the linearity and spectral characteristics of the thermometric segment of a DAC. Building on the foundation established in [6], this work presents the design of a DEM-assisted 9-bit segmented DAC. To minimize area usage, the optimum segmentation level will be determined by analyzing the linearity-area tradeoff, adapting the methodology described in [2]. To overcome the area constraints imposed by the integral nonlinearity (INL) requirement and improve spectral perfomance, the matrix-based DEM engine described in [6] is employed. Using the DEM engine leads to an $8\times$ and $16\times$ improvement in spurious-free dynamic range (SFDR) and total harmonic distortion (THD), respectively. As a result, the system achieves a THD of -79 dB and a SFDR of 79 dB.

The rest of the paper is organized as follows. Section 2 presents the background. Section 3 presents a structured methodology for optimizing the DEM-assisted segmented DAC's area and details the proposed digital controller from a system-level perspective. Section 4 presents the system implementation together with a comparative analysis showcassing the DEM techniques advatages. And finally, the paper concludes in Section 5.

2. Background

This section discusses 3 typicall DAC coding schemes (binary, thermometric and segmented) in terms of the area-linearity tradeoff. Next, the dynamic element matching technique is introduced, which enhances linearity at the cost of increased complexity.

2.1. Segmented D/A converters

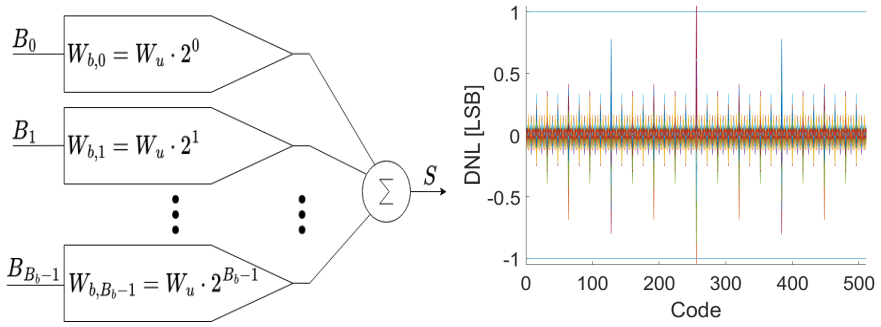
In this subsection, the binary, thermometric, and segmented DAC switching schemes are analyzed with respect to area-linearity tradeoff. The linearity is quantified in terms of the differential non-linearity (DNL) and integral non-linearity (INL). Each DAC cell consists of an analog part, and a digital part. The total analog area (A_{analog}) represents the total current sources area, with each DAC unit current source having an unit area (A_u) and delivering an unit current (I_u). To account for mismatch, the currents are independent random variables that follow a Gaussian distribution with a standard deviation (σ_u) and mean I_u. The total digital area ($A_{digital}$) is comprised of switching logic for each cell (A_{cell}) and the B-to-2^B decoder area, $A_{dcd}(B)$.

2.1.1. Binary coded DAC

Fig. 1a presents a generalized block diagram of a B_b-bit binary coded DAC, consisting of B elements driven directly by the digital input. The DAC output is expressed in (1), where $W_{B,i}$ denotes the i-th binary weight, W_u represents the unit weight, and $\overline{B_{B_b-1}...B_1B_0}$ is the input code.

$$S(\overline{B_{B_b-1}...B_1B_0}) = \sum_{i=0}^{B_b-1} B_i \cdot W_{B,i} = \sum_{i=0}^{B_b-1} B_i \cdot W_u \cdot 2^i \tag{1}$$

The total area of the binary coded DAC, as given by (2), includes 2^{B_b} unit current sources area, and a compact digital area for only B_b cells, lacking a decoder. Given that the weights



(a) (b)

Fig. 1. (a) A binary-coded DAC concept, (b) DNL curves of 100 9-bit binary DACs.

are multiples of a common unit weight ($W_{B,i} = W_u \cdot 2^i$), the binary element's variance is a multiple of the unit variance, ($\sigma^2_{B,i} = \sigma^2_u \cdot 2^i$). Thus, the binary switching scheme experiences significant non-linearity, with the largest error occurring at midcode [2], as indicated in (3), where ($2^{B_b-1} - 1$) sources are turned OFF and (2^{B_b-1}) sources are turned ON, as detailed in (4).

$$A_{total,bin} = A_{analog} + A_{digital} \simeq 2^{B_b} \cdot A_u + B_b \cdot A_{cell} \tag{2}$$

$$\sigma^2_{DNL,mid} = \sigma^2_u \cdot 2^{B_b-1} + \sigma^2_u \cdot (2^{B_b-1} - 1) = \sigma^2_u \cdot (2^{B_b} - 1) \tag{3}$$

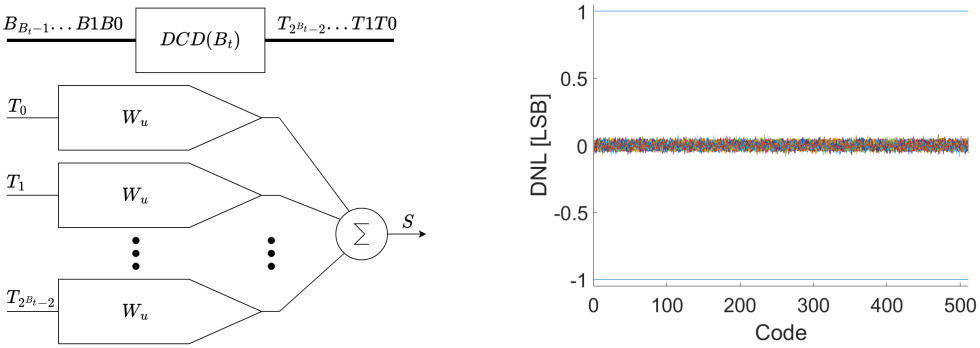
$$DNL, mid = \frac{S(10\ldots0) - S(01\ldots1)}{W_u} - 1 \tag{4}$$

The DNL curves for 100 9-bit DACs, with a σ_u of 0.02, were simulated using MATLAB and are shown in Fig. 1b. Three of the DACs are non-monotonic and the most significant non-linearity, resulting in a $\sigma_{DNL,mid}$ of 0.4, is observed at midcode, as indicated by (3). The theoretical analysis predicts a $\sigma_{DNL,mid}$ of 0.45, implying that approximately 5% of the DACs would be non-monotonic, thereby supporting the consistency between the MATLAB simulation results and theoretical expectations. To meet the industry standard of 0.5 DNL with a yield of 99.7%, a σ_u of 0.007 is necessary. M.J.M. Pelgrom showed in [7] that the mismatch is inversely proportional to the square root of the area. After redesigning the unit elements to reduce the σ_u from 0.02 to 0.007, an $8\times$ increase in the DAC area is expected. Hence, the total area of the binary-weighted DAC is primarily determined by A_{analog}.

2.1.2. Thermometer coded DAC

Fig. 2a presents a generalized block diagram of a B_t-bit thermometer-coded DAC, consisting of $2^{B_t} - 1$ elements, in contrast to only B elements used in the binary version, along with an additional B_t-bit binary-to-thermometric decoder ($A_{dcd}(B)$). Since all elements share the same unit weight, their variances are equal. For each code transition, only one current source is turned ON or OFF, making all transitions equally significant, with $\sigma^2_{DNL} = \sigma^2_u$. Furthermore, since $\sigma_u \ll 1$, the thermometric-coded DAC is always monotonic [2], which mitigates nonlinearity. The DAC output is expressed in (5), where t_i represents the i-th bit of the thermometric code and W_u is the unit weight.

$$S(\overline{B_{B_t-1}...B_1B_0}) = S(\overline{T_{2^{B_t}-2}...T_1T_0}) = \sum_{i=0}^{2^{B_t}-2} T_i \cdot W_u \tag{5}$$



(a) (b)

Fig. 2. (a) A thermometric-coded DAC concept, (b) DNL curves of 100 9-bit thermometric DACs.

Compared to the area of a binary-coded DAC, the footprint of a thermometer-coded DAC, as given by 6, includes an additional $2^{B_t}-1$ cells for extra switches and driving logic, along with a B_t-bit area $A_{dcd}(B)$, which increases more than exponentially with the number of bits [1].

$$A_{total,thermo} = A_{analog} + A_{digital} \simeq 2^{B_t} \cdot (A_u + A_{cell}) + A_{dcd}(B_t) \tag{6}$$

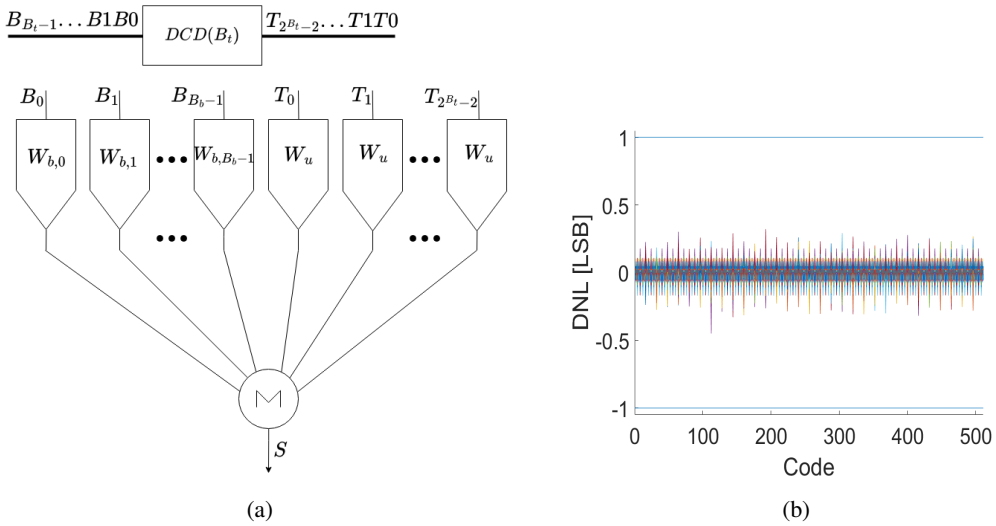
The DNL curves for 100 9-bit DACs, with a σ_u of 0.02, were simulated using MATLAB and are shown in Fig. 2b. The DNL error is uniformly distributed across all codes, and all DACs are monotonic, with $\sigma_{DNL,max}$ of 0.023, aligning with the 0.02 theoretical value. To maintain an industry standard of 0.5DNL with 99.7%, a 0.17 unit element matching is required, making it $24\times$ more relaxed compared to the binary version. According to Pelgrom's law [7], the analog area is $590\times$ smaller. However, the digital area overhead is hefty: the thermometer-coded DAC requires $57\times$ more cell logic and a 9-bit decoder. Therefore, the total area of the thermometer-coded DAC is dominated by $A_{digital}$.

2.1.3. Segmented DAC

To addresses the binary and thermometer coding drawbacks, segmented DACs [2] are proposed. Segmentation involves dividing the DAC into multiple segments, each with binary or thermometric encoding and own weights. Fig. 3a depicts a segmented DAC split into two segments: a binary-coded LSB segment with a unit weight W_u and a thermometric-coded MSB segment with a unit weight $W_u \cdot 2^{B_b}$. The DAC output is expressed in (7).

$$S(\overline{B_{B-1}...B_1B_0}) = S(\overline{T_{2^{B_t}-2}...T_1T_0B_{B_b-1}...B_1B_0}) = \sum_{i=0}^{2^{B_t}-2} T_i \cdot W_u \cdot 2^{B_b} + \sum_{i=0}^{B_b-1} T_i \cdot W_u \cdot 2^i \tag{7}$$

When compared to the pure thermometer-coded DAC, the digital area of a segmented DAC, as covered by 8 and 9, is reduced from $2^B A_{cell}$ to $2^{B-B_b} A_{cell}$, where B is the DAC's total number of bits and B_b is the number of binary coded bits. Furthermore, the decoder's area is



(a) (b)

Fig. 3. (a) A segmented DAC with a themometric-coded MSB segment and a binary-coded LSB segment concept, (b) DNL curves of 30 9-bit segmented DACs with $B_t = 5$.

minimized to the area of the segmented DAC thermometer-coded bits.

$$A_{total} = A_{total,thermo} + A_{total,bin} \simeq 2^{B_t} \cdot (A_u + A_{cell}) + 2^{B_b} \cdot A_u + B_b \cdot A_{cell} + A_{dcd}(B_t) \quad (8)$$

$$A_{total} \simeq 2^B \cdot A_u + 2^{Bt} \cdot A_{cell} + A_{dcd}(B_t) \quad (9)$$

The segmented DAC' DNL is dominated by the binary portion. It peaks when the largest binary-weighted source turns OFF and one of the thermometric sources turns ON. Thus, the maximum DNL of a segmented DAC with B_t thermometric bits and B_b binary bits equals the maximum DNL of a $B_b + 1$ binary-coded DAC [2], as shown in 2.1.3..

$$\sigma^2_{DNL,max} = \sigma^2_u \cdot (2^{B_b+1} - 1) \quad (10)$$

The DNL curves for 100 9-bit DACs, with a σ_u of 0.02 and $B_t = 5$, were simulated using MATLAB and are shown in Fig. 3a. According to (), DNL spikes appear at MSB transitions. All DACs remain monotonic, with $\sigma_{DNL,max}$ at 0.13, closely aligning with the 0.11 theoretical value. To meet the industry standard of 0.5 DNL with a 99.7% yield for the 9-bit DAC batch, a 0.03 unit element matching is required. This results in the analog area of the segmented DAC being 18 times smaller than that of the binary version and 32 times larger than the thermometric version. The required digital area is 16 times smaller than that of the thermometric DAC and 4 times larger, in addition to a 5-bit decoder, compared to the binary DAC.

Kuboki et al. demonstrate in [8] that the DAC's INL is coding scheme independent and depends solely on the number of bits and σ_u, as expressed in (11). Hence, the INL sets a hard limit on the minimum analog area.

$$\sigma_{INL,max} \simeq \frac{1}{2}\sigma_u\sqrt{2^B} \quad (11)$$

2.2. Dynamic element matching

The DEM technique is used to mitigate the effects of mismatch between elements of a system that are intended to be identical [9]. A unit current source mismatch is characterized as the deviation between its actual value and its intended value as a result of fabrication process variations and can be mathematically represented by (12).

$$W_{i,j} = W \cdot (1 + \epsilon_{i,j}), |\epsilon_{i,j}| < 1 \tag{12}$$

In a system composed of multiple elements, $W_{i,j}$, each element deviates from the ideal expected value, W, due to its individual mismatch $\epsilon_{i,j}$. By toggling between various configurations (activating or deactivating elements), the system produces a different output each time. Averaging these output values yields a value closer to the ideal intended output. Let $b_{i,j}$ represent binary values indicating the activation state of the matrix element (0 for inactive, 1 for active). The output S of the $M \times N$ system is determined by (13).

$$S = \sum_{i=1}^{M} \sum_{j=1}^{N} b_{i,j} \cdot W_{i,j} \tag{13}$$

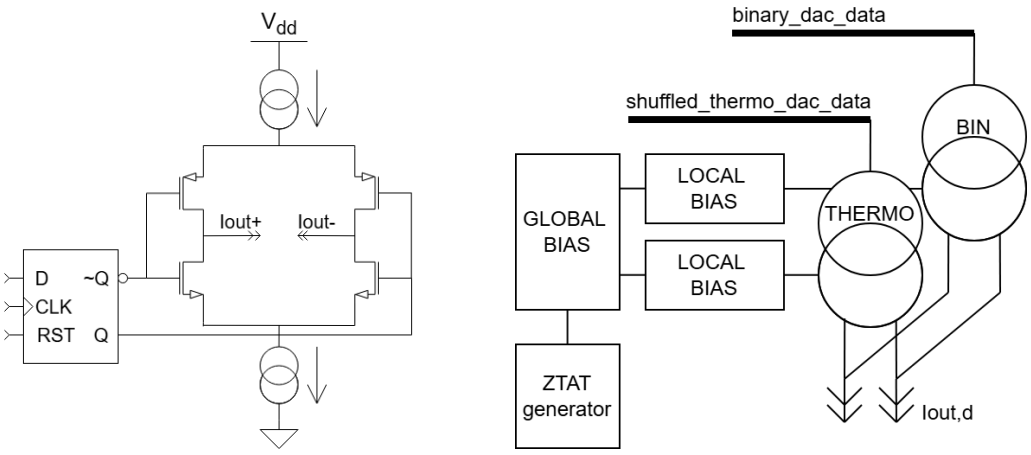
When switching between active elements, a specific configuration is represented by an $M \times N$ matrix constructed using the $b_{i,j}$ values. For instance, a system with only 2 elements can be denoted by the element matrix [$W_{1,1}$ $W_{1,2}$] and configuration matrices [0 1] and [1 0]. Depending on the configuration, either $W_{1,1}$ or $W_{1,2}$ is generated. Three possible cases can be summarized in Eq. 14: i) when both elements' true values are slightly below the ideal value W, the average output falls between the two real outputs, below the ideal output; ii) similarly, if both possible outputs exceed the ideal value, the average output falls between the two real outputs, above the ideal output, and iii) when one output surpasses the ideal value and the other falls short, the average output tends to be closer to the ideal expected output than either individual output.

$$S_{average} = \frac{S_1 + S_2}{2} = W + \frac{\epsilon_1 + \epsilon_2}{2} \tag{14}$$

Scenarios 1 and 2 yield a gain error which can be corrected in the digital domain. For the third scenario, utilizing the DEM technique mitigates the system's output error, hence aligning with the mean value of the mismatch distribution. In thermometric DACs, shuffling randomizes the output characteristic of the DAC, transforming the systematic non-linearity created by mismatch into ideally white noise [10]. This leads to a reduction in INL and an improvement in the system's SFDR and THD [11].

3. Area-Optimized Dynamic Element Matching-Based DAC

In this section, we present the design flow for the DEM-based DAC, aimed at the output of an audio $\Sigma\Delta$ modulator with an OSR of 32 and a 40 kHz bandwidth. The DAC is located between the noise-shaping loop and the reconstruction filter, requiring dual polarity current cells that switch at 1.6 MHz. Due to the low operating frequency ($\ll$ 100 MHz), second-order effects like code-dependent output impedance [12] and inter-symbol interference [13] can be ignored, allowing for sufficient single-cascoding.



(a) (b)

Fig. 4. (a) Dual polarity cell with single cascoding, (b) DAC block diagram.

We derive the cell architecture from the application specifications and use MATLAB modeling to identify the optimal segmentation level that minimizes total area. We also present the architecture and functionality of the digital DEM controller.

3.1. Current source cells

The DAC block diagram is represented in Fig. 4b. A ZTAT generator provides a 1'st order temperature compensated current which is distributed using a network of current mirrors to the thermometric and binary sources. The network was split into GLOBAL BIAS and 2 LOCAL BIAS to lower the noise and diminish the IR drop caused by the parasitic gate currents [13]. The current cell architecture is shown in Fig. 4a, with a retiming latch added to prevent synchronization issues [13]. The current source transistors are sized using the structured approach from [2]. First, the PMOS and NMOS mismatch coefficients ($A_{I,n} = \sigma_{u,n} \cdot \sqrt{WL}$, $A_{I,p} = \sigma_{u,p} \cdot \sqrt{WL}$) and the cell switching logic area (A_{cell}) are determined. Next, the areas of the decoder ($A_{dcd}(B)$), shuffler ($A_{shuff}(B)$), and cell address logic ($A_{add}(B)$) as functions of the number of thermometric bits are extrapolated from [6]. Using 9, the digital area is given by (15).

$$A_{digital} = A_{dcd}(B_t) + A_{shuff}(B_t) + A_{add}(B_t) + A_{cell} \cdot 2^{B_t} \tag{15}$$

Imposing a maximum DNL of 0.5 with 99.7% yield (3σ) and using 2.1.3., the unit current variance as a function of B_t is given by (16). The PMOS and NMOS currents are assumed to be independent, therefore the total variance of the differential current is $\sigma_u^2 = \sigma_{u,p}^2 + \sigma_{u,n}^2$. Assuming the variances are equal and using Pelgrom's law [7], the analog area is given by (17).

$$\sigma_u = \frac{0.5LSB}{3 \cdot \sqrt{2^{B-B_t+1} - 1}} \tag{16}$$

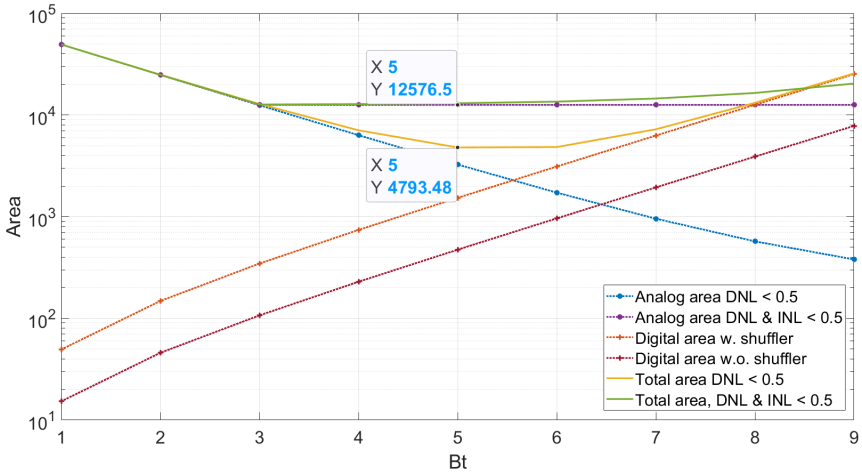


Fig. 5. Required DAC area for different B_t and implementations.

$$A_{analog} = \left[\left(\frac{A_{I,n}}{\sigma_u \cdot \sqrt{2}} \right)^2 + \left(\frac{A_{I,p}}{\sigma_u \cdot \sqrt{2}} \right)^2 \right] \cdot 2^B \tag{17}$$

Using (15), (16), and (17), the area logarithmic characteristics of the segmented DAC with and without shuffling are shown in Fig. 5. At low segmentation levels ($B_t = 1...3$), where $A_{total} \simeq A_{analog}$, the area is dominated by the DNL requirement. For $B_t > 3$, the INL requirement imposes a minimum current source area, as given by (9). At high segmentation levels ($B_t \geq 8$ without shuffling and $B_t \geq 6$ with shuffling), $A_{total} \simeq A_{digital}$. For the DAC without shuffling, there is an optimum region ($3 \leq B_t \leq 8$) where any B_t suffices, but higher B_t reduces DNL. With a shuffler, the INL requirement is alleviated, resulting in a total area decrease until $B_t = 5$ and a $3\times$ reduction in DAC total area compared to the DAC without shuffling.

3.2. DEM digital controller

The design and operation of the proposed digital control circuitry required for the area-optimized DEM-dased DAC is presented. Fig. 6 presents the digital interface, the thermometric encoder that generates the default, initial state of the thermo matrix and the shuffling circuitry.

The shuffling process is achieved by using 2 pseudorandom number generators, one that controls how cells shift their states to one another on the vertical axis, while the other is responsible for the horizontal shifting of the cells' states. The row shuffler decides if a cell will take its value from either the neighbor from above or from the one below. The column shuffler, on the other hand, determines if a cell will take it's next state from the cells from right or left. For the cells placed at the edge of the matrix, the shifting operation is done using a wrap-around method - the bottom row is "above" the top row, while the rightmost column is the left neighbour of the leftmost column. The suffling operations change the state of the cells of the thermo matrix, with a visual example presented in Fig. 7, where white cells are disabled, while blue cells are enabled. The arrows describe where the states of the cells are moving towards.

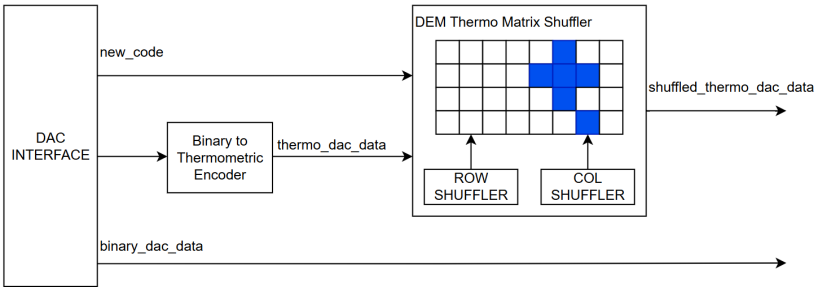


Fig. 6. High-level schematic of the digital control of the thermometric matrix system.

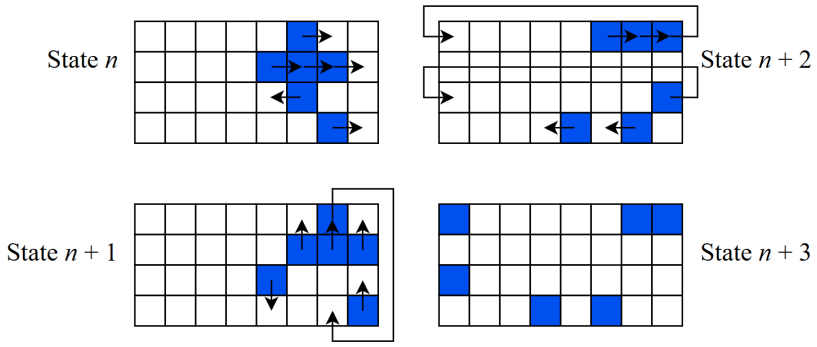


Fig. 7. The shuffling algorithm changing the states of the cells of a 4×8 matrix.

The shufflers are implemented using Galois LFSRs, with parametrized polynomial, initial state and width, as presented in Fig. 8.

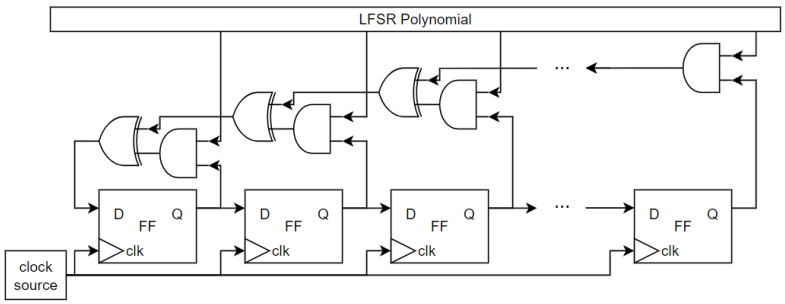


Fig. 8. Galois LFSR implementation of the row and column shufflers.

4. Results

The proposed DAC system was implemented in a commercial 180nm CMOS process. This section details the implementation results, linearity and spectral performance of the system.

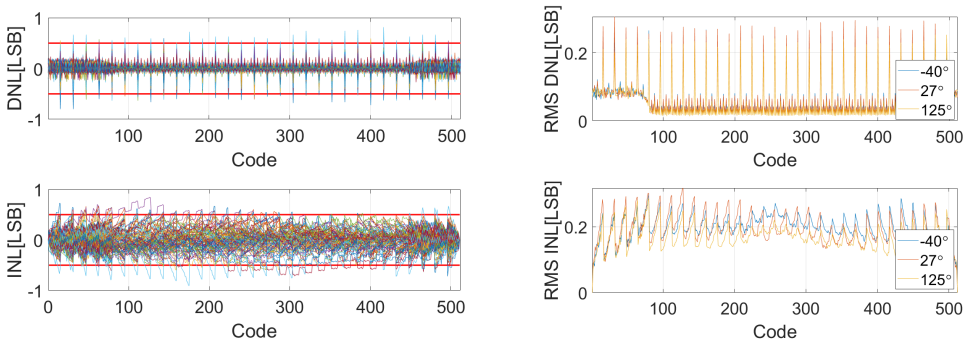
4.1. DEM digital controller implementation

The DEM controller was implemented using RTL description in SystemVerilog and synthesized to logic gates from the standard cell library of the aforementioned process using a commercial synthesis solution for which TCL scripts have been developed. The proposed 4×8 matrix circuit, with 32 cells, is optimized for 400 MHz operation under worst-case conditions (slow process, 125 °C, 1.62 V supply). It occupies 7466 μm^2 and consumes 3.42 mW.

4.2. Segmented DAC simulation results

The DAC current sources were implemented using the sizing data extracted from MATLAB. The DAC current source area is 3469 μm^2 with a σ_u of 0.034, within 6% of the MATLAB estimate of 3261 μm^2 and σ_u of 0.03. The unitary current source produces $400nA$ of differential current, consuming a total of $184\mu W$. The total integrated noise in the [20Hz, 20kHz] bandwidth is 7uV, thus the maximum (thermal-limited) SNR is 105dB. The analog bias circuitry creates an additional overhead of $1908\mu m^2$ active area and $19957\mu m^2$ of passives. The latter can be reduced by placing resistors and capacitors on top of eachother.

Fig. 9a represents INL and DNL curves of a batch of 30 DACs over the $[-40°C, 125°C]$ temperature range. The RMS envelope, which gives a measure of the DNL/INL standard deviation, is represented in Fig. 9b. The maximum RMS DNL is 0.3LSB. All the DACs are monotonic. When binned based on maximum DNL, 16 DACs fall below 0.5 LSB, while 25 remain under 0.6 LSB. When accounting for both DNL and INL, 8 DACs stay below 0.5 LSB, while 20 remain under 0.6 LSB.

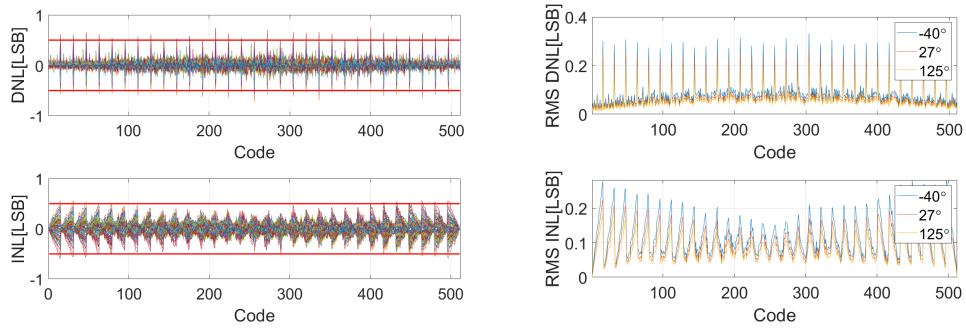


(a) (b)

Fig. 9. (a) DAC linearity characteristics, (b) DAC DNL/INL envelope.

4.3. DEM-based segmented DAC simulation results

The DEM engine shuffles the thermometric sources 256 times per conversion. Since the digital is clocked at 400MHz, this limits the DAC operating frequency to 1.56MHz. Fig. 10a represents the INL and DNL curves of a batch of 30 DEM DACs over full industrial temperature range. The RMS envelope, which gives a measure of the DNL/INL standard deviation, is represented in Fig. 10b. The latter gives the same maximum DNL RMS of ∼0.3, as predicted by 2.1.3.. All the DACs are monotonic. When binned based on maximum DNL, 23 DACs fall below 0.5 LSB, while 27 remain under 0.6 LSB. When accounting for both DNL and INL, 22 DACs stay below 0.5 LSB, while 27 remain under 0.6 LSB.



(a) (b)

Fig. 10. (a) DEM DAC linearity characteristics, (b) DEM DAC DNL/INL envelope.

To assess the improvement in spectral characteristics, the DAC was tested with a 11.23kHz sinewave with the DEM engine turned ON and OFF. For this test, the DAC is driven at 1MHz and the output data was filtered in MATLAB with a digital 2'nd order Butterworth LPF with a corner frequency of 40kHz, to match the reconstruction filter. Fig. 11 shows the averaged PSD of a batch of 10 DACs with the shuffler turned ON and OFF. For clarity, only the [0, 80kHz] band was represented and the maintone, 2nd and 3rd harmonics and largest spur have been marked.

Table 1. Spectral characteristics comparison table

Measurement	SNR[dB]	SNDR[dB]	ENOB[bits]	THD[dB]	SFDR[dB]
DEM OFF	64	61.6	9.9	-67	70
DEM ON	65	65	10.5	-79	79
Improvement	1	3.4	0.6	12	9

Since this is an oversampled system, the ideal ENOB is 11. For the DEM OFF case, the SFDR is limited to 70dB by the 2nd harmonic and the THD is -67dB. Moreover, one full bit is lost. When turning ON the DEM engine, the HD2 and HD3 components are renderd indistinguishable against the noise floor, as expected. Compared to the non-DEM DAC, the SFDR is increased by 9dB, the THD by 12dB and the ENOB loss is halved.

5. Conclusions

The proposed digitally-assisted 9-bit segmented DAC, implemented in a commercial 180nm CMOS process, occupies an active area of 12999μm^2 and consumes up to 3.14mA from a 1.8V power supply at 400MHz. The maximum DNL and INL over 30 MC simulations and $[-40°, 125°]$ temperature range are 0.75LSB and 0.57LSB, respectively, and 27/30 DACs have both their DNL and INL under 0.6LSB. Using the DEM engine renders the harmonics indistinguishable against the noise floor. This leads to an $8\times$ improvement in SFDR and a $16\times$ improvement in THD. As a result, the system achieves a THD of -79 dB and a SFDR of 79 dB.

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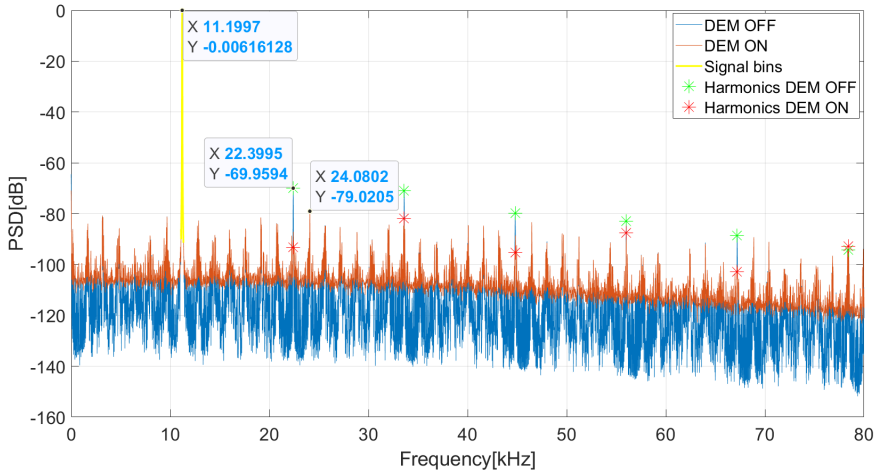

Fig. 11. Average DAC output PSD with DEM turned ON/OFF, 65536 points, Hann window.

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