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van Ginkel, Hendrik Joost; Romijn, Joost; Vollebregt, Sten; Zhang, Guo Qi

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HIGH STEP COVERAGE INTERCONNECTS BY PRINTED NANOPARTICLES

Hendrik Joost van Ginkel, Joost Romijn, Sten Vollebregt and Guo Qi Zhang
Delft University of Technology, Delft, Netherlands
Contact: h.j.vanginkel@tudelft.nl

Abstract — The growing diversity in the used materials in semiconductor packaging provides challenges for achieving good interconnection. Particularly the very soft substrates, such as paper and polymers, and very hard, such as silicon carbide, offer unique challenges to wire-bonding or formation of vertical interconnects. Complementary technologies are therefore needed. Here, a method to direct-write metal tracks on the top and sides of dies is demonstrated. It is based on a spark ablation aerosol printing process entirely performed at room temperature and without any applied force. Therefore, it is suitable for use on soft or temperature-sensitive substrates. The printed metal lines consist of pure Au nanoparticles, without surfactants or contaminants, and do not require any further curing, cleaning, or other processing. The process is demonstrated on Si dies and paper, but is theoretically applicable on a wide variety of substrate materials. It can provide an alternative method to create interconnects or vias on soft materials, temperature sensitive materials, irregularly shaped materials, or curved surfaces.

Keywords — Nanoparticles, flexible electronics, interconnect, thin-film, printing, spark ablation

I. INTRODUCTION

Due to the development of flexible electronics, harsh environment electronics, and bioelectronics, there is a growing need for interconnection technologies compatible with different substrates besides silicon. Traditionally, interconnects are made using flip-chip technology or wire-bonding, which are mature and well-developed technologies but not universally applicable. Wirebonding requires elevated temperatures (>150 °C) or ultrasonic power to make a good weld [1]. Flexible substrates typically do not survive such temperatures and are not rigid enough for ultrasonic bonding. Wirebonding can even induce damaging stress in silicon electronics [1, 2, 3]. New, gentle technologies to work with temperature-sensitive substrates or devices are thus needed. Here, we present a novel process to direct-write an interconnect at room temperature compatible with virtually any substrate that is compatible with a vacuum of 1 mbar. We introduce a method to direct write Au nanoparticle paths by using inertial impaction. It is shown that a conducting line can be printed on the side of a die to create a continuous path from the top to the bottom while maintaining good conductivity. Due to the direct-writing nature of the technique, the step size is limited only by the printing equipment geometry.

The process is based on the synthesis of the nanoparticles by spark discharge generation. This process was first described by Schwyn et al. in 1988 and uses a spark caused by a high potential difference (~1 kV) applied between two opposing electrodes to ablate some material from the electrodes [4]. The vapor is carried away by the carrier gas and rapidly cools down, creating an extremely supersaturated vapor that condenses into nanoparticles. The final mean particle size is typically 4-10 nm [5]. No additional chemicals are required other than the ablated metal and the (inert) carrier gas, removing the need for further processing or cleaning after deposition. The resulting ultra-clean particle surface lowers their sintering temperature to well below 200 °C so they can be sintered at low temperatures if needed. Unfortunately, such ultra-clean surfaces mean there are no surfactants to protect the surface, and the nanoparticles will readily react with any oxygen they encounter and oxidize. Pure metallic particles are in practice only possible with noble metals unless precautions are taken against oxidation [6, 7].

The second advantage of this technology is its material flexibility. Any conducting metal or alloy can be used as parent material, and any combination of two electrodes expands the options even further. Even metals not miscible in bulk can exist as alloys from spark ablation [5]. Mixing several of such aerosols creates even more possibilities. Thirdly, the impaction process can be used with virtually any substrate. Considering the printing process is at room temperature, the only limiting factor is that the substrate can withstand a 1 mbar vacuum. Small, ;ocal variations in substrate height or roughness have no influence on the deposition quality or can be adjusted for by varying the nozzle height. The method has been used to print patterns on polymers [8], paper, glass, and resin packages, as seen in fig. 1. Last, this deposition process is maskless, making the pattern easily customizable.

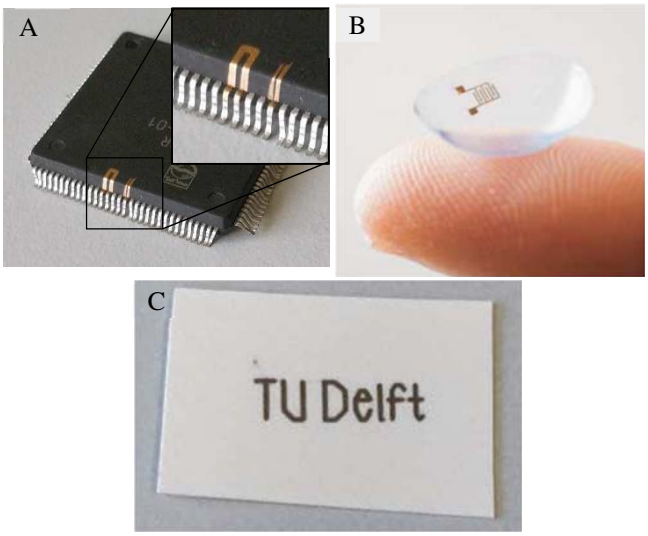

Fig. 1, printed features on various substrates: A) Gold lines on a package connecting to two pins, B) gold pattern on a contact lense [8], C) 'TU Delft' printed in gold on paper. The T is 3 mm high.

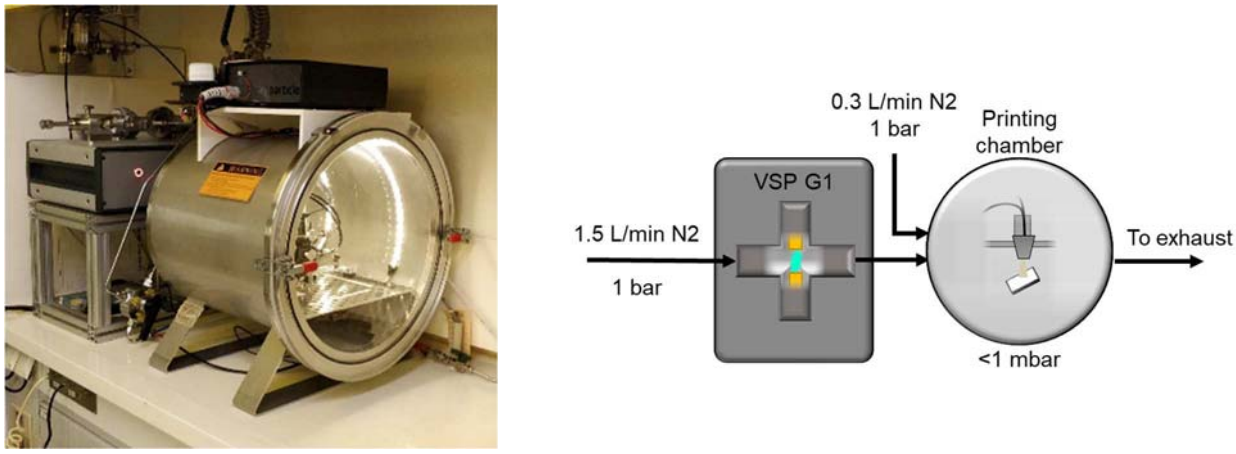

Fig. 2, photograph of the nanomaterial printer (left) and a schematic diagram showing the major components and gas flow (right).

II. Methods & Materials

A. Cleanroom fabrication

Two substrates were used to demonstrate this process: a single side polished 100 mm Si wafer and paper (PowerCoat HD, Arjowiggins Creative Paper). To fabricate the stacked samples, Si wafers were insulated with 300 nm SiO_2 on each side by thermal oxidation. After lithography, 10/100 nm Cr/Au was deposited, and lift-off was performed to finish the patterning. Finally, all wafers were diced into 20x20 or 10x10 mm dies and cleaned with acetone, isopropanol, and demi water.

The 10x10 mm dies were thermocompressively bonded on 20x20 mm dies using SU-8 bonding polymer [9]. These Si on Si (SoS) substrates were cured at 120 °C and 1 kN for 2 hours. The Si on paper (SoP) samples were made by cutting 15x15 mm squares out of the paper sheet, and bonding 10x10 mm top dies using manually applied cyanoacrylate adhesive (3M). No additional curing was needed for this adhesive. The resulting structures are shown in fig. 3. Both substrates have identical Au patterns to connect two sides of the top die. This simplifies probing during 4-point-probe measurements by only having to contact the bottom die.

B. Nanoparticle deposition

The spark discharge generator was a VSP G1 by VSParticle B.V. and 99.999% Au electrodes were used to produce the nanoparticle aerosol. The generator was set to 8 mA and 1 kV. N_2 (99.999%) gas was used as carrier gas at a 1.5 l/min flowrate. After generation, the aerosol is carried to the printing chamber, where they are accelerated by a pressure difference over a nozzle using a <1 mbar vacuum. The diagram in fig. 2 shows the gas connections and the equipment setup. The nozzle is placed at 0.5-2.0 mm distance to the substrate at an angle of 20° or 45°. At supersonic speeds, the NPs cannot adjust fast enough to changes in the flow direction due to their inertia and land on the surface. Combining this with a XYZ-stage allows direct writing of nanoporous deposits. The printer used is a proto-0 Nanomaterial Printer also developed by VSParticle B.V. and was operated at 0.5 mbar using a 0.1 l/min nozzle. Patterns were printed with a writing speed of 1.0 mm/min. To print on the sides of a die, the samples were placed on a tilted holder at 20° or 45° with respect to the stage.

The samples were imaged using A Hitachi Regulus 8230 scanning electron microscope (SEM) and a micro-probestation was used for IV characterization. A Bruker Dektak 150 profilometer was used to determine the height profile and corresponding cross-sectional area.

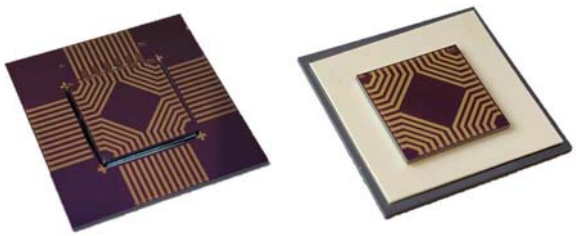

Fig. 3, photographs of the substrates. Left, a SoS sample with a few printed lines (top edge). Right, a SoP sample, taped to a 20x20 mm die for easier handling and mounting.

III. Results

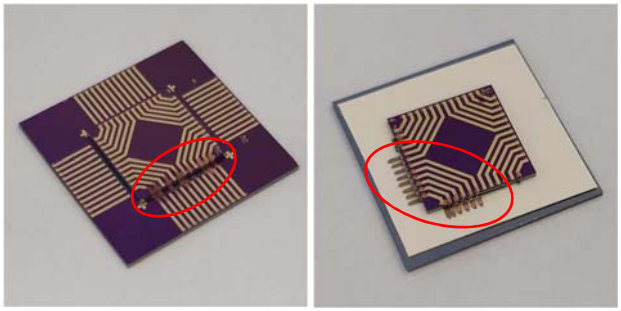

Fig. 4, two printed samples. Left a SoS and right a SoP sample. The encircled areas highlight the location of the printed Au lines.

The final device can be seen in Fig. 4. The tilted SEM images in Fig. 5 show the surface is uniformly coated with a porous film. The deposits show good surface conformity, even on irregular features. Most notably, the film is continuous at the die edge, a 90° corner. Even features on the silicon created during dicing of the wafer only cause minor disturbances in the film. Fig. 5 also shows an excess of SU-8 from the manual glue dispensing and die placement during bonding. Consequently, a rounded corner is formed that fills the gap between the two dies and simultaneously providing a more gradual slope that is easier to conform to for the film. The bottom corner is therefore smooth and transitions gradually to the bottom die. Bonding optimization was not performed and occasionally, cracking was observed at the SU-8 to Si interface, which consequently caused

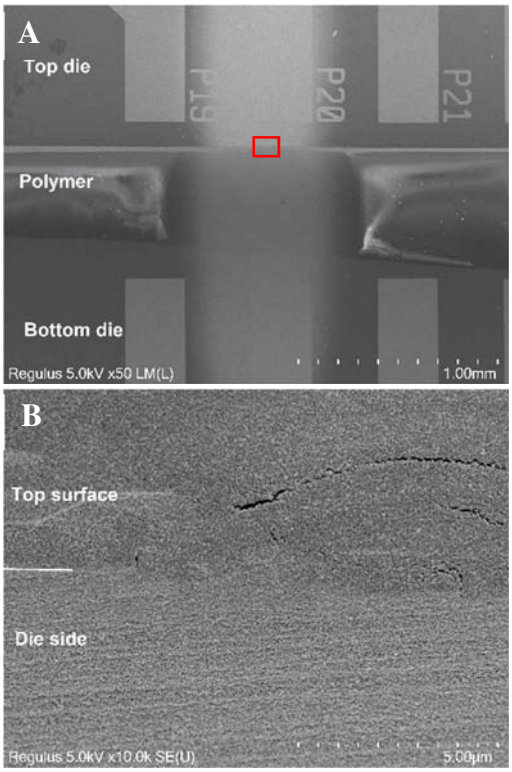

Fig. 5, tilted SEM images taken at a 25° angle of a Si-to-Si connection. A) Showing both top and bottom die with a printed line at "P20" going from the top die surface to the surface of the 20x20 mm die. An excess of bonding polymer (SU-8) can be seen. The red rectangle marks the location of close-up in B. The edge of the top die can be seen in the middle of image B and is marked by the white line on the left.

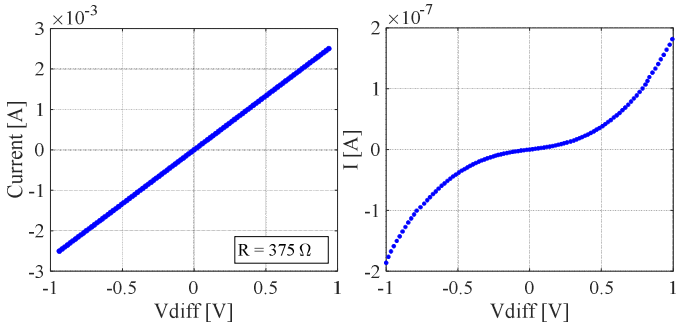

Fig. 6, resistor (left) and varistor (right) IV curves of a SoP sample.

cracks in the NP film.

The yield of the samples was high with 82% of the 18 measured metal tracks showing good Ohmic behavior (fig. 6). The resistance of an interconnect varied with printing settings but was lowest at 0.5 mm printing distance with 2.97±0.72 Ω when printed at 20° nozzle tilt. Broken devices show either an open connection when measured at a single electrode or IV behavior typical for varistors when one measures at two neighboring electrodes. This is likely due to the two opposing Au-Si Schottky diodes that form at a crack on the Si edge. Fig. 6 shows a comparison between a working and broken interconnect.

On SoP samples, the same features can be observed at the top die, since those are identical. One notable feature of printing on paper is that the NP film covers the fibrous structure of the paper while still forming a conductive film, as seen in fig. 7. Again, this shows the high conformity and uniformity of the films. For bonding Si to paper, cyanoacrylate was used, applied

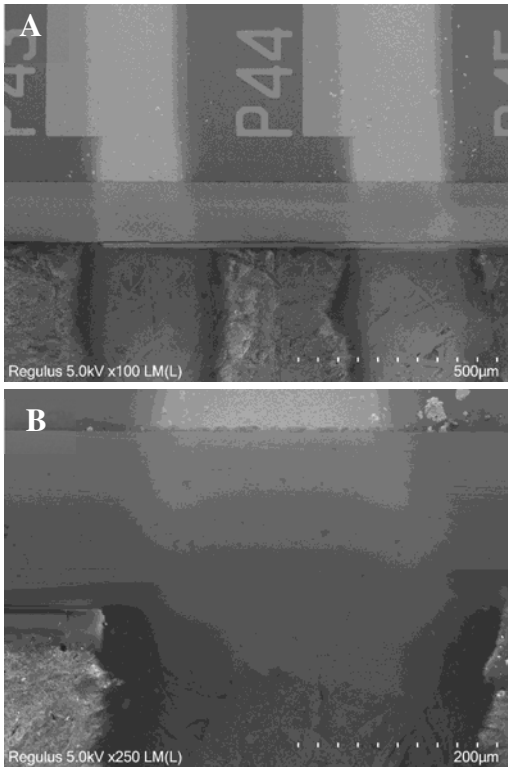

Fig. 7, tilted SEM images of SoP tracks taken at a 25° angle. A) Two lines with cracking at the adhesive and B) a working interconnect. Note the film coats the fibrous structure of the paper while remaining conductive.

at room temperature. Cyanoacrylate appears to be not as good of an adhesive to Si as SU-8 since we observed frequent cracks at the Si interface. This reduced yield drastically. Only 20% of the connections showed Ohmic behavior, the rest showing clear varistor IV curves. Resistance in working connections varied from 250-750 Ohm, indicating that the films vary widely in resistivity. It is not clear if this is caused by the roughness of the paper or the direct probing of the nanoparticle film.

The cross-sectional area of a line was measured using a profilometer at the top die between the Au electrode and the edge of the top surface. A line with a 0.5 mm nozzle distance has a cross-sectional area of 168 μm^2 with a width of ca. 900 µm. Assuming a constant deposition rate, this cross-sectional area is the same on the side of the silicon. From this we can calculate the resistivity of a printed line to be $8.3 \cdot 10^{-5}$ Ω cm for a SoS sample, assuming that the contact resistance between the NP and Au lines is neglectable. This is a factor 34 higher than bulk gold and we can attribute this largely to the porous nature of the film. If one were to sinter the particles, this value would improve due to the reduced particle-to-particle resistance.

IV. Discussion

The major difficulty for this technology appears to be a reliable connection at the Si-Si or Si-paper interface. At that 90 corner, the bonding adhesive needs to fill the gap between the two substrates and ideally create a rounded corner. More accurate and controlled adhesive application is the straightforward solution to solve this.

A second issue is that conducting substrates can short two printed interconnects due to the absence of an insulating layer. In this paper, the edge of a Si die is unoxidized silicon and will make a Schottky contact with the Au film. Although two opposing Schottky diodes have a high resistance, this still results in two lines being connected through the silicon substrate. One proposed solution is to coat the edges after dicing with an insulating material. This might be an oxide, but a polymer such as parylene which is regularly used in packaging would be more appropriate due to the lower deposition temperature. To characterize the electrical performance without any influence of the substrate, future work should use non-conducting substrates like glass or sapphire. Additionally,,. considering there are no patterned thin-film Au electrodes on the paper like on the 20x20 mm Si dies, we had to directly probe the relative fragile nanoparticle film on the paper with the probe needles. Patterning contact pads on the paper using for instance a shadow mask would solve this.

The line width is variable by changing the nozzle distance and nozzle diameter. With the available setup it is currently not possible to go below 100 µm in width, but with continued engineering it could enable smaller feature sizes. Tilting the nozzle to allow printing at a constant angle (i.e. 0°) relative to the sample surface can improve the coverage of the surface and create more homogenous printing on an edge. This would require extensive upgrades to our setup, but this technology is already applied in conventional 3D printing or robotic coating technology. Our setup is a prototype and although fully functional, improvements on the printing accuracy and reproducibility will improve yield. Newer versions of this nanomaterial printer already have significantly higher accuracy and printing speed.

V. Conclusion

A novel process is demonstrated to complement wire-bonding or VIAs on a wide range of substrates. The process is entirely at room temperature, making it especially suitable for temperature-sensitive and soft substrates. Its high conformity and substrate flexibility allow for application on rough or uneven surfaces. The lowest resisitivty measured is still 34 times higher than that f bulk Au, but optimizing printing conditions or using a sintering process if thermal budget allows can improve this.

Future work is to demonstrate this technique on soft polymers or SiC to show application on very hard materials to provide a method to produce front-to-back connections where techniques like through silicon vias are not possible. Making connections on non-conducting substrates should be considered for improving the accuracy of the electrical characterization.

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