Generalized Analysis of the Performance of DAB Converters for Modular Heavy-duty EV Charging Stations

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***Abstract*—The commercialization success of heavy-duty electric vehicles (EVs) is predominantly contingent upon the development of a robust and scalable charging infrastructure. Compared with low-frequency transformers (LFT), modular applications of solid-state transformers (SST) offer a more promising solution for achieving MW-level power scalability in the future. In the DC/DC stage of SSTs, the dual active bridge (DAB) converter is a widely adopted topology. And the optimal modulation plays a crucial role in selecting appropriate switching devices and improving overall efficiency. This paper focuses on the specific case of a 33.3 kW module within the modular charging station for heavy-duty EVs, presenting a generalized approach to optimize the current stress of MOSFETs and soft-switching performance. The switching performance of the candidate devices for this case has also been quantitatively discussed and verified to achieve soft switching over a wide load range in PSIM simulation.**

***Index Terms*—Soft-switching, current stress, dual active bridge (DAB) converters, solid-state transformers (SST), modular charging stations.**

I. Introduction

The global automotive industry is undergoing a major transformation, with approximately 14 million and more than 17 million EVs sold worldwide in 2023 and 2024, respectively. According to the IEA's stated policies scenario, by 2035, every second car sold worldwide is expected to be electric, based on current energy, climate, and industrial policies [1]. While light commercial vehicles (LCVs) are progressing rapidly towards electrification, heavy-duty vehicles (HDVs) are undergoing a more gradual transition. However, their substantial share of operational activity and emissions underscores their critical role in achieving decarbonization goals. Recent studies in the U.S. and Europe suggest that electric trucks may require charging capacities exceeding 350 kW, potentially reaching 1 MW for a full recharge within 30–45 minutes [2], highlighting the urgent need for the development of MW-level heavy-duty EV charging stations to meet these high-power demands.

However, both the research and development of the MW-level charging station remain in their early stages. Compared with traditional LFTs, SSTs offer a technically superior alternative, thanks to improved power quality, enhanced power flow control, and direct connection to the medium-voltage (MV) grid [3]. Furthermore, scholars and industry experts have proposed a diverse range of modular SST topologies, among which the isolated back end (IBE) topology is widely adopted [4], typically implemented as multi-cell input-series output-parallel (ISOP) structure to manage the MV-level connection. Meanwhile, this configuration also enhances the total power capability of the charging station and facilitates the integration of other renewable resources or energy storage.

In the DC/DC stage, DAB converters are particularly well-suited for SST applications due to several advantages [5], [6]. First, they enable self-regulating bidirectional power flow, suitable for SST-based microgrid environments requiring rapid and seamless power direction changes. Second, their inherent zero-voltage switching (ZVS) ability allows for high transmission efficiency, which can be further optimized through proper control strategies. Currently, research on DAB converters is extensive, focusing on topics such as soft-switching performance, current stress on the switching devices and circulating current, etc., especially under gain mismatch or light-load conditions [7]–[13]. However, two key areas still require further exploration. First, most studies address single DAB converters, despite modular designs being essential for MV-level applications. Second, existing research lacks a comprehensive design methodology rooted in modulation strategies, which is essential for practical deployment.

This paper aims to bridge these gaps through case studies, contributing to the modular implementation of the design of heavy-duty electric vehicle charging stations. The remainder of this paper is structured as follows: Section II presents the configuration of the system for the case study. Then, Section III provides a detailed analysis of EPS modulation, along with the methodology to determine the minimum current stress. Finally, Section IV evaluates the corresponding ZVS performance of the obtained phase shift combinations through numerical calculations and simulation validation, while Section V presents the conclusions and provides an outlook on future work.

II. The Cascaded SST Structure and DAB Converters

As mentioned in the previous section, to enable direct connection to the MV grid and enhance power transmission, a cascaded structure is adopted in this study. The overall system architecture is illustrated in Fig. 1. To facilitate subsequent

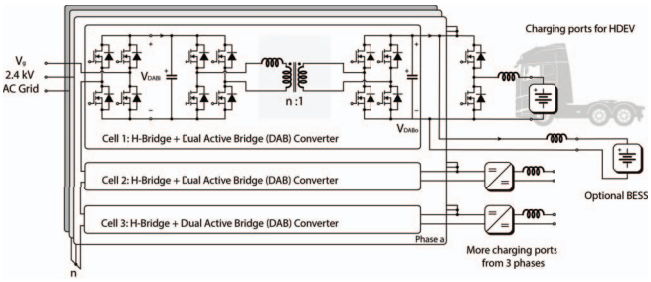


Fig. 1: Overall structure of the modular heavy-duty EV charging station.

research, the system targets connection to a 2.4 kV MV grid and consists of three cascaded modules. With continuous advancements in silicon carbide (SiC) MOSFET technology [14]–[17], research has been increasingly focusing on higher voltage and power levels, improved device performance, reliability, and manufacturing processes. Consequently, a variety of commercially available devices are now capable of handling this voltage level. In terms of power rating, the total power is specified as 100 kW, with each module rated at 33.3 kW. The outputs of these modules will be connected to a 1 kV DC bus, facilitating the integration of additional energy sources or storage systems. Within the broader scope of this research, this paper will specifically focus on the analysis of DAB converters, providing insights into the current stress and soft-switching performance of switching devices.

The fundamental principle of DAB converters can be described as connecting two AC voltage sources across an inductor, with power flow regulated by adjusting the phase shift between them. As a result, single phase shift (SPS) modulation is the most fundamental modulation method for DAB converters. In SPS modulation, the diagonal switches of each full bridge operate with an identical 50% duty cycle, while switches on the same leg operate in a complementary manner. Under this configuration, the power transferred by DAB can be expressed as:

$$P = \frac{nV_iV_oD(1-D)}{2f_{\text{sw}}L_k} \tag{1}$$

Where n is the transformer turns ratio, V_i and V_o are the input and output voltage, f_{sw} is the switching frequency, and L_k is the leakage inductance of the transformer. Notably, the phase shift ratio D is defined as the ratio of the phase shift angle ϕ and half of the switching period π.

However, with continued research progress, the DAB converter encounters significant current stress and difficulties in maintaining soft switching under light-load conditions. To enhance operational flexibility and overall efficiency, a range of advanced modulation techniques have been proposed, and this paper specifically examines EPS modulation as a representative approach.

III. Optimization of the Current Stress

In the DAB converter, current stress is defined as the peak current experienced by the switching devices during stable operation. Excessive current stress necessitates rigorous component selection, potentially increasing costs and exacerbating power losses. Therefore, a thorough investigation into current stress is crucial for improving efficiency and refining converter design.

A. Single Phase Shift (SPS)

From the relationship between the voltage across the leakage inductance L_k and the corresponding current, the expression of current stress i_{max} can be derived as:

$$i_{\text{max}} = \frac{nV_o}{4f_{sw}L_k}(K+2D-1) \tag{2}$$

where the voltage transfer ratio $K = V_i/(nV_o)$.

To facilitate analysis, normalization is performed by selecting the base current as the input current at maximum transmission power $i_N = nV_o/(8f_{sw}L_k)$. The normalized expression of current stress is given by:

$$i_p = \frac{i_{\text{max}}}{i_N} = 2(K+2D-1) \tag{3}$$

This implies that, when P is fixed, an increasing mismatch in the voltage transfer ratio results in higher current stress. However, a more practical consideration is that, for a fixed K, the current stress increases as P rises, as the transformer turns ratio n is typically constant and V_i/V_o will not change significantly.

B. Extended Phase Shift (EPS)

In EPS modulation, an additional phase shift D_1 is applied to the diagonal switches on the primary side, along with the primary-to-secondary phase shift D_2 (denoted as original D in SPS modulation). By classifying two different cases based on the relationship between D_1 and D_2, The expression for the normalized transmission power in EPS can be derived:

$$P_E = \begin{cases} 2\left(-D_1^2+2D_1D_2-D_1-2D_2^2+2D_2\right), & D_1 < D_2 \\ 2\left(2D_2+D_1^2-2D_1D_2-D_1\right), & D_2 < D_1 \end{cases} \tag{4}$$

Based on (4), it can be inferred that when $D_1 < D_2$, the transmission power ranges from 0 to 1. However, for $D_2 < D_1$, the power varies between -0.5 and 0.5. This indicates that, for positive power transfer, the latter mode is limited to half of the maximum achievable power. Furthermore, according to Fig. 2, when $D_1 < D_2$, the peak current is observed at t_4. In contrast, when $D_2 < D_1$, the currents at t_1 and t_3 both present the possibility of reaching the maximum, thus requiring detailed classification analysis. If i_N is also defined as the base current, the normalized current stress can be expressed as:

$$I_{\text{max}} = \begin{cases} 2\left(2D_2-1-K(D_1-1)\right), & D_1 < D_2 \\ \max\left\{ \begin{array}{l} 2(1+K(D_1-1)), \\ 2(2D_2-1+K(1-D_1)) \end{array} \right\}, & D_2 < D_1 \end{cases} \tag{5}$$

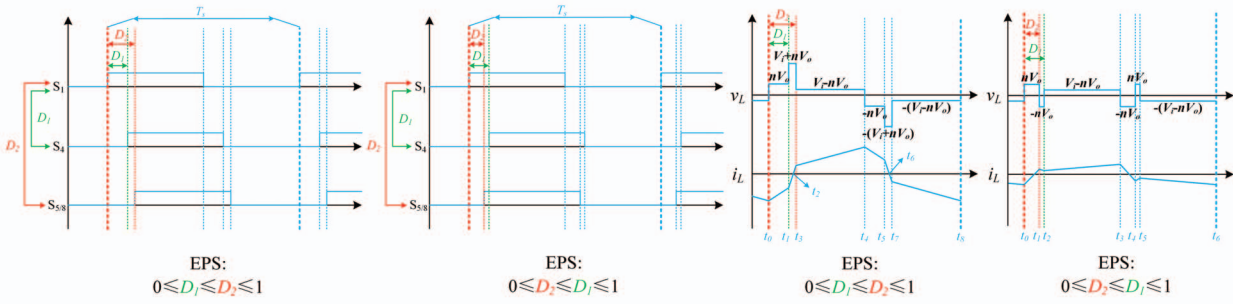


Fig. 2: Voltage and current waveforms when EPS modulation is applying.

a) Analysis for $D_1 < D_2$: To find the optimal combination of phase shift angles and thereby minimize the current stress on switching devices, the Karush-Kuhn-Tucker (KKT) conditional method, which is originally proposed to derive closed-form solutions for the global optimal control parameters, is utilized to optimize the current stress [17]. Mathematically, when the KKT conditions hold, the optimal solution x^* is characterized by the gradient of the objective function $f(x)$ being balanced with the gradients of both the equality constraints $h_i(x)$ and the inequality constraints $g_j(x)$, which can be formally expressed as:

$$\begin{cases} \min f(x) \\ h_i(x) = 0, \quad i = 1, \ldots, l \\ g_j(x) \leq 0, \quad j = 1, \ldots, m \end{cases} \tag{6}$$

where l and m are the number of equality constraints and inequality constraints, respetively.

Based on the previously derived expressions for power transmission and current stress, the standard form of the KKT condition can be formulated as follows:

$$\begin{cases} L_E = I_{max} + \mu\big(P_E - P\big) + \lambda_1(-D_1) + \lambda_2(-D_2) \\ +\lambda_3(D_1 - 1) + \lambda_4(D_2 - 1) + \lambda_5(D_1 - D_2), \\ \dfrac{\partial L_E}{\partial D_1} = 0, \quad \dfrac{\partial L_E}{\partial D_2} = 0, \\ \mu \neq 0, \quad \lambda_1, \lambda_2, \lambda_3, \lambda_4 \geq 0, \\ P_E - P = 0, \\ -D_1 \leq 0, \quad -D_2 \leq 0, \quad D_1 - 1 \leq 0, \quad D_2 - 1 \leq 0 \end{cases} \tag{7}$$

where L_E is the Lagrangian, and μ and λ are both Lagrange multipliers.

The optimal solution under these constraints can be determined as:

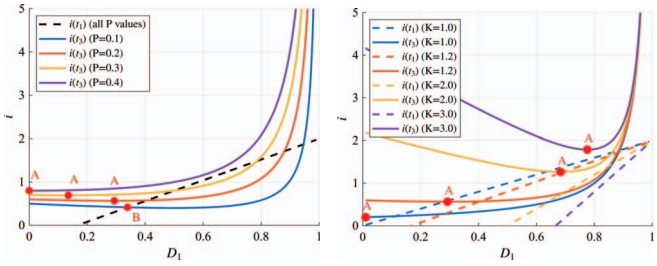
$$\begin{cases} D_1 = \dfrac{(K-1)\sqrt{(1-P_E)(K^2-2K+2)}}{K^2-2K+2} \\ D_2 = \dfrac{(K-2)\sqrt{(1-P_E)(K^2-2K+2)}}{2(K^2-2K+2)} + \dfrac{1}{2} \end{cases} \tag{8}$$

Consequently, under the condition of this phase shift combination, the resulting current stress, i.e., the current at t_4 is:

$$I_{max} = 2K - 2\sqrt{(1-P_E)(K^2-2K+2)} \tag{9}$$

b) Analysis for $D_2 < D_1$: For this scenario, the key point is the comparison of the currents at t_1 and t_3, in order to accurately determine the current stress. As is depicted in Fig. 3, two specific cases are presented: one where P is fixed ($P = 0.2$) and another where K is fixed ($K = 1.2$), allowing a more comprehensive comparison. The corresponding equations are derived as follows:

$$\begin{cases} i(t_1) = 2\left(1 + K(D_1 - 1)\right) \\ i(t_3) = 2\left(2D_2 - 1 + K(1 - D_1)\right) \\ P_E = 2(D_1 - 2D_2)(D_1 - 1) \end{cases} \tag{10}$$



(a) (b)

Fig. 3: Values of $i(t_1)$ and $i(t_3)$ under different conditions: (a) $K = 1.2$, (b) $P = 0.2$.

Generally, when either K or P is fixed, the minimum of $max(i(t_1), i(t_3))$ occurs at $i(t_3)$ where its slope reaches zero. However, if $i(t_1)$ and $i(t_3)$ intersect at a lower horizontal coordinate, the minimum shifts to their intersection instead.

Therefore, the horizontal coordinate at which the derivative of $i(t_3)$ equals zero (denoted as D_a) should be compared with the intersection point of $i(t_1)$ and $i(t_3)$ (denoted as D_b), if it exists. The expressions for the two horizontal coordinates are,

$$\begin{cases} D_a = 1 - \sqrt{\dfrac{P_E}{2(K-1)}} \\ D_b = \dfrac{4K - 3 - \sqrt{1 - (4K-2)P_E}}{4K-2} \end{cases} \tag{11}$$

If $D_a < D_b$, the minimum corresponds to point A in Fig. 3, whereas if $D_b < D_a$, it corresponds to point B.

Accordingly, the boundary condition is given by,

$$P_E = \frac{2(K-1)}{(2-3K)^2} \tag{12}$$

Meanwhile, the derived phase shift combination must additionally satisfy the prerequisite $D_2 > D_1$,

$$P_E < \frac{2(K-1)}{K^2} \tag{13}$$

The corresponding values of D_2 ($D_{2.2}$ corresponded with $D_{1.2}$ and $D_{2.1}$ corresponded with $D_{1.1}$, respectively) and I_{max} can be derived accordingly, as presented in Table I.

IV. Verification of the ZVS Range

To provide a clearer illustration of the ZVS performance under optimized current stress conditions, the voltage transfer ratio K is set to 1.2 in this section.

It is known that achieving ZVS in a DAB converter requires the stored energy in the leakage inductance at the switching instant to exceed the energy stored in the output parasitic capacitances of the switching devices. For EPS modulation, under $D_1 < D_2$, considering the current variation throughout a switching cycle, the required condition is derived as follows:

$$\begin{cases} i_L(t_1) \le 0 \\ i_L(t_3) \ge 0 \end{cases} \Rightarrow \begin{cases} D_2 \ge \dfrac{(K+2)D_1 + 1 - K}{2} \\ D_2 \ge \dfrac{KD_1 - 1 + K}{2K} \end{cases} \tag{14}$$

On the other hand, for the case $D_2 < D_1$,

$$\begin{cases} D_1 \ge \dfrac{K-1}{K} \\ D_2 \ge \dfrac{KD_1 - K + 1}{2} \end{cases} \tag{15}$$

Based on these two constraints, a further analysis can be conducted on the relationship between the previously derived minimum current stress trajectory and the ZVS realization region, as shown in Fig. 4. From the figure, it can be observed that, under ideal conditions, regardless of whether $D_1 < D_2$ or $D_2 < D_1$, the minimum current stress trajectory falls within the feasible phase shift range for (indicated by the gray-shaded region in the figure). The entire analysis process described above can be summarized in the flowchart presented in Fig. 6.

However, it is important to emphasize that the ZVS region determination in this context is based on ideal conditions, excluding the influence of switching device parasitic capacitances when calculating the ZVS criteria. Nevertheless, this factor plays a crucial role in practical applications. Considering the switching device parasitic capacitances, to ensure the achievement of ZVS, it is not enough to merely satisfy the conditions $i_L(t_1) \le 0$ and $i_L(t_3) \ge 0$ under $D_1 < D_2$, instead, a certain sufficient value must be fulfilled. This requirement can be expressed by the following equation,

$$E_{L_K} > E_{C_{eq}} \Rightarrow \frac{1}{2}L_k i_L^2 > 4 \cdot \frac{1}{2}C_{\text{eq}}V_c^2 \Rightarrow i_L > 2V_c\sqrt{\frac{C_{\text{eq}}}{L_k}} \tag{16}$$

Hence, a sufficient criterion for ensuring ZVS under $D_1 < D_2$ can be evaluated using the following expression:

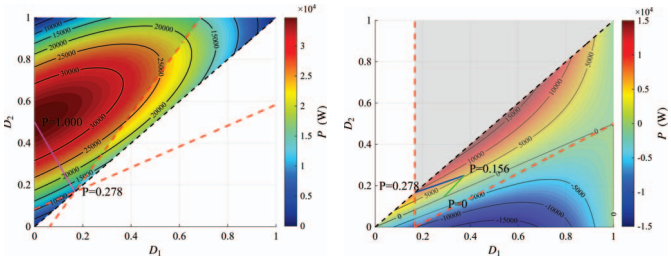
$$\begin{cases} D_2 \ge \dfrac{(K+2)D_1 + 1 - K}{2} + \dfrac{4V_c f_{\text{sw}}}{nV_o}\sqrt{L_k C_{\text{eq}}} \\ D_2 \ge \dfrac{KD_1 - 1 + K}{2K} + \dfrac{4V_c f_{\text{sw}}}{2KnV_o}\sqrt{L_k C_{\text{eq}}} \end{cases} \tag{17}$$

where C_{eq} is the equivalent parasitic capacitances of the MOSFET. In this paper, the equivalent capacitance is defined as the average value of the nonlinear output capacitance [18],

$$C_{\text{eq}} = \int_0^{v_o} C_{\text{oss}}(v)\, dv. \tag{18}$$

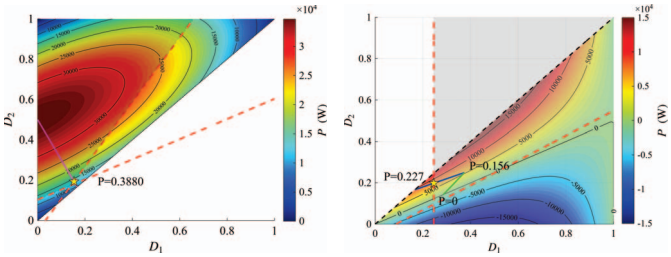
On the other hand, for the case $D_2 < D_1$,

$$\begin{cases} D_1 > \dfrac{K-1}{K} + \dfrac{8f_{\text{sw}}V_c}{KnV_o}\sqrt{C_{\text{eq}}L_k} \\ D_2 > \dfrac{KD_1 - K + 1}{2} + \dfrac{4f_{\text{sw}}V_c}{nV_o}\sqrt{C_{\text{eq}}L_k} \end{cases} \tag{19}$$



(a) (b)

Fig. 4: ZVS performance with EPS modulation when ignoring the switching device parasitic capacitances under different conditions ($K = 1.2$): (a) $D_1 < D_2$, (b) $D_2 < D_1$. The color contours indicates the output power of the DAB converter.



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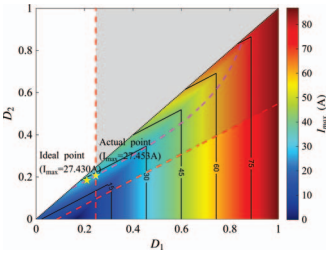


(c)

Fig. 5: ZVS performance with EPS modulation when considering the switching device parasitic capacitances under different conditions ($K = 1.2$): (a) $D_1 < D_2$, (b) $D_2 < D_1$, (c) The current stress trade-off under $P = 0.25$.

From Fig. 5, it can be observed that, when selecting the operating points along the three-segment line corresponding to the minimum current stress, ZVS is only achieved when the output power P is either below 0.227 or above 0.388.

TABLE I: Minimum Current Stress Under Different Modulation and Transmission Power

P_E	D_1	D_2	$I_{\max}$
$0 \le P_E \le \frac{2K-2}{(3K-2)^2}$	$\frac{4K-3-\sqrt{1-(4K-2)P_E}}{4K-2}$ (D$_{1.1}$)	$\frac{3K-2-K\sqrt{1-(4K-2)P_E}}{4K-2}$ (D$_{2.1}$)	$\frac{3K-2-K\sqrt{1+(2-4K)P_E}}{2K-1}$
$\frac{2K-2}{(3K-2)^2} \le P_E \le \frac{2K-2}{K^2}$	$1-\sqrt{\frac{P_E}{2(K-1)}}$ (D$_{1.2}$)	$\frac{1}{2}+\frac{\sqrt{2P_E(K-1)(K-2)}}{4(K-1)}$ (D$_{2.2}$)	$K\sqrt{2P_E(K-1)}$
$\frac{2K-2}{K^2} \le P_E \le 1$	$\frac{(K-1)\sqrt{(1-P_E)(K^2-2K+2)}}{K^2-2K+2}$ (D$_{1.3}$)	$\frac{(K-2)\sqrt{(1-P_E)(K^2-2K+2)}}{2(K^2-2K+2)}+\frac{1}{2}$ (D$_{2.3}$)	$2K-2\sqrt{(1-P_E)(K^2-2K+2)}$

TABLE II: Parameters in the PSIM Simulation

Parameters	**Values**
Input voltage V_i	800 V
Output voltage V_o	1000 V
Rated power P	33.3 kW
Switching frequency f_s	100 kHz
Turns ratio $1:n$	2:3
Leakage Inductance L_k	19.22 μH
Dead Time t_d	150 ns
Primary switches	GeneSiC G3R12MT12K
Secondary side switches	GeneSiC G3R20MT17K

However, by relaxing the strict requirement for minimum current stress, ZVS can still be achieved within this intermediate power range under the case of $D_2 < D_1$. To illustrate this point, the operating condition at $P = 0.25$ is selected as an example, which is depicted by the pink dashed line. As shown in Fig. 5c, when the effects of parasitic capacitances are taken into account, the ideal operating point no longer lies within the ZVS regions. Consequently, a slight increase in current stress is required to shift the operating point into the ZVS-enabled area (Actual point).

It is important to note that the feasibility of ZVS under light-load conditions is also sensitive to the value of the equivalent output capacitance C_{eq}. If C_{eq} is underestimated during the design phase, the required current for charging/discharging the parasitic capacitance may be insufficient in practical scenarios. This is why the impact of device parasitics on the overall converter design will be further investigated in the future work of this project.

To validate whether the aforementioned theoretical calculations achieve the expected results, the model built in PSIM is utilized. Table II lists the main parameters of the DAB converter and the parameters of MOSFETs implemented are based on the datasheet provided by the manufacturers.

To ensure the reliability and generality of the simulation results, three different operating points were selected from three distinct power ranges. Fig. 7 shows the voltage and current waveform of the leakage inductance. Meanwhile, Fig. 8 illustrates the waveforms of V_{ds} and I_{ds} within one switching cycle when $P = 0.8$, $P = 0.2$ and $P = 0.1$, repectively. The left side of the figure presents simulations using the ideal MOSFET model, while the right side employs the non-ideal Level-2 model provided by PSIM, which also have the parasitic capacitance modeled (C_{iss}, C_{oss}, C_{rss}) and

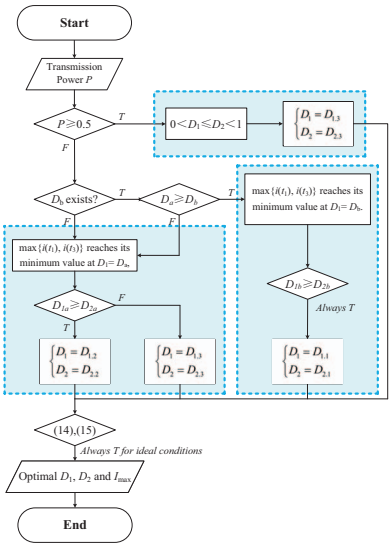


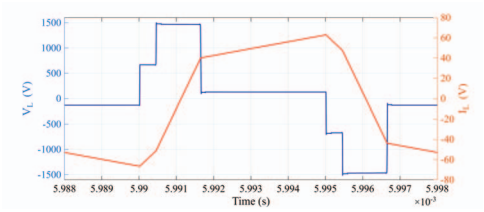
Fig. 6: General workflow of the current stress optimization and ZVS validation for EPS modulation.

will allow for a relatively realistic switching transient.

When using the ideal model, it is evident that ZVS-on is successfully achieved at all three operating points. However, when using the non-ideal model, parasitic effects induce noticeable spikes in the current waveform. Nevertheless, these spikes remain significantly lower than the switching losses caused by hard switching.

V. Conclusion

In this paper, a generalized analysis of DAB converters within modular heavy-duty EV charging stations was conducted. The study focused on optimizing soft-switching performance and minimizing current stress of switching devices within a predefined 33.3 kW module to improve system efficiency. By applying the EPS modulation strategy, analytical expressions for the optimal phase shift combinations were derived. Simulation results in PSIM verified the theoretical findings, demonstrating that under ideal conditions, ZVS-on is successfully achieved across various operating points. Additionally, the impact of parasitic parameters on current waveforms has been observed and preliminarily analyzed, which will also be addressed in our future work to incorporate practical parasitic effects in switching devices. The proposed



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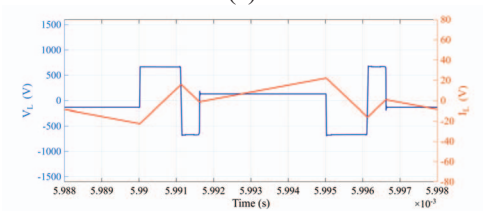

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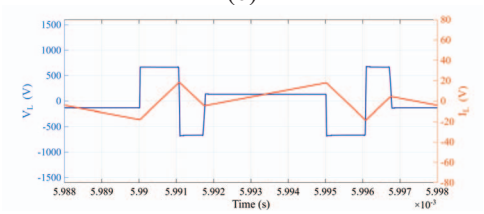
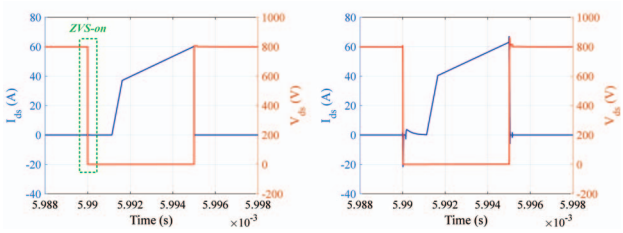


(c)

Fig. 7: Voltage and current waveform of the leakage inductance during switching transient when (a) $P = 0.8$ (b) $P = 0.2$ (c) $P = 0.1$.



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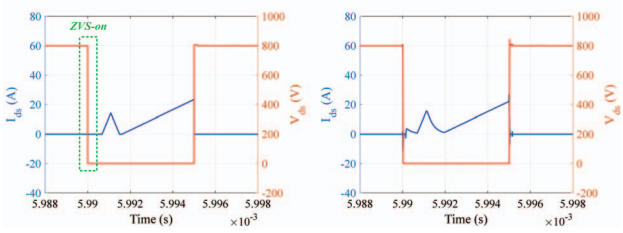

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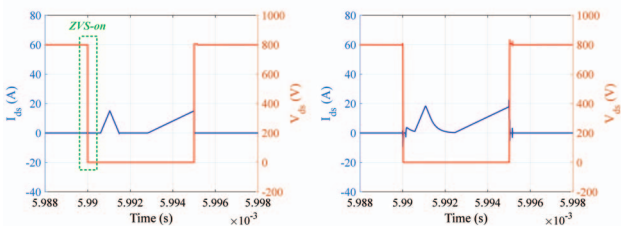

(c)

Fig. 8: Voltage and current waveform of one of the MOSFETs on the primary side during switching transient when (a) $P = 0.8$ (b) $P = 0.2$ (c) $P = 0.1$.

modulation strategy will also be further optimized and validated using a hardware prototype, taking into account various experimental factors such as switching frequency and ambient temperature.

References

[1] IEA (2024), Global EV Outlook 2024, IEA, Paris https://www.iea.org/reports/global-ev-outlook-2024.

[2] CharIN. Megawatt Charging System. Available online: https://www.charin.global/technology/mcs/ (15 January 2025).

[3] S. Rivera, et al., "Charging infrastructure and grid integration for electromobility," Proceedings of the IEEE, vol. 111, no. 4, pp. 371–396, Apr. 2023.

[4] J. E. Huber, et al., "Analysis and design of fixed voltage transfer ratio DC/DC converter cells for phase-modular solid-state transformers," *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015.

[5] R. W. A. A. De Doncker, et al., "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, Jan. 1991.

[6] B. Zhao, et al., "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[7] B. Zhao, et al., "Power characterization of isolated bidirectional Dual-Active-Bridge DC–DC converter with Dual-Phase-Shift control," *IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 4172–4176, Mar. 2012.

[8] T. Hirose, et al., "A power efficiency improvement technique for a bidirectional dual active bridge DC–DC converter at light load," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 4047–4055, May 2014.

[9] B. Zhao, et al., "Universal High-Frequency-Link characterization and practical Fundamental-Optimal strategy for Dual-Active-Bridge DC-DC converter under PWM plus Phase-Shift control," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6488–6494, May 2015.

[10] E. L. Carvalho, et al., "Asymmetrical-PWM DAB converter with extended ZVS/ZCS range and reduced circulating current for ESS applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12990–13001, May 2021.

[11] G. Chen, et al., "Asymmetric phase-shift modulation strategy of DAB converters for improved light-load efficiency," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9104–9113, Aug. 2022.

[12] M. Mahdavifard, et al., "An asymmetrical DAB converter modulation and control systems to extend the ZVS range and improve efficiency," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12774–12792, May 2022.

[13] J. Tian, et al., "Dual-Side asymmetric duty modulation based on accurate Soft-Switching characteristics modeling for DAB-Based DC microgrid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 3, pp. 3146–3160, Jan. 2024.

[14] J. Li, et al., "A review on gate oxide failure mechanisms of silicon carbide semiconductor devices," *IEEE Transactions on Electron Devices*, vol. 71, no. 12, pp. 7230–7243, Dec. 2024.

[15] J. Li, et al., "Temperature dependent trap characterisation and modelling of silicon carbide MOS capacitor." *25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, pp. 1-6. Apr. 2024.

[16] Z. J. Shen, "SIC research beyond power MOSFET: What's next? [happenings]," *IEEE Power Electronics Magazine*, vol. 8, no. 2, pp. 14–23, Jun. 2021.

[17] J. Huang, et al., "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC–DC converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[18] A. Rodríguez, et al., "Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge with Phase-Shift Control." *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 790–804, Feb. 2015.