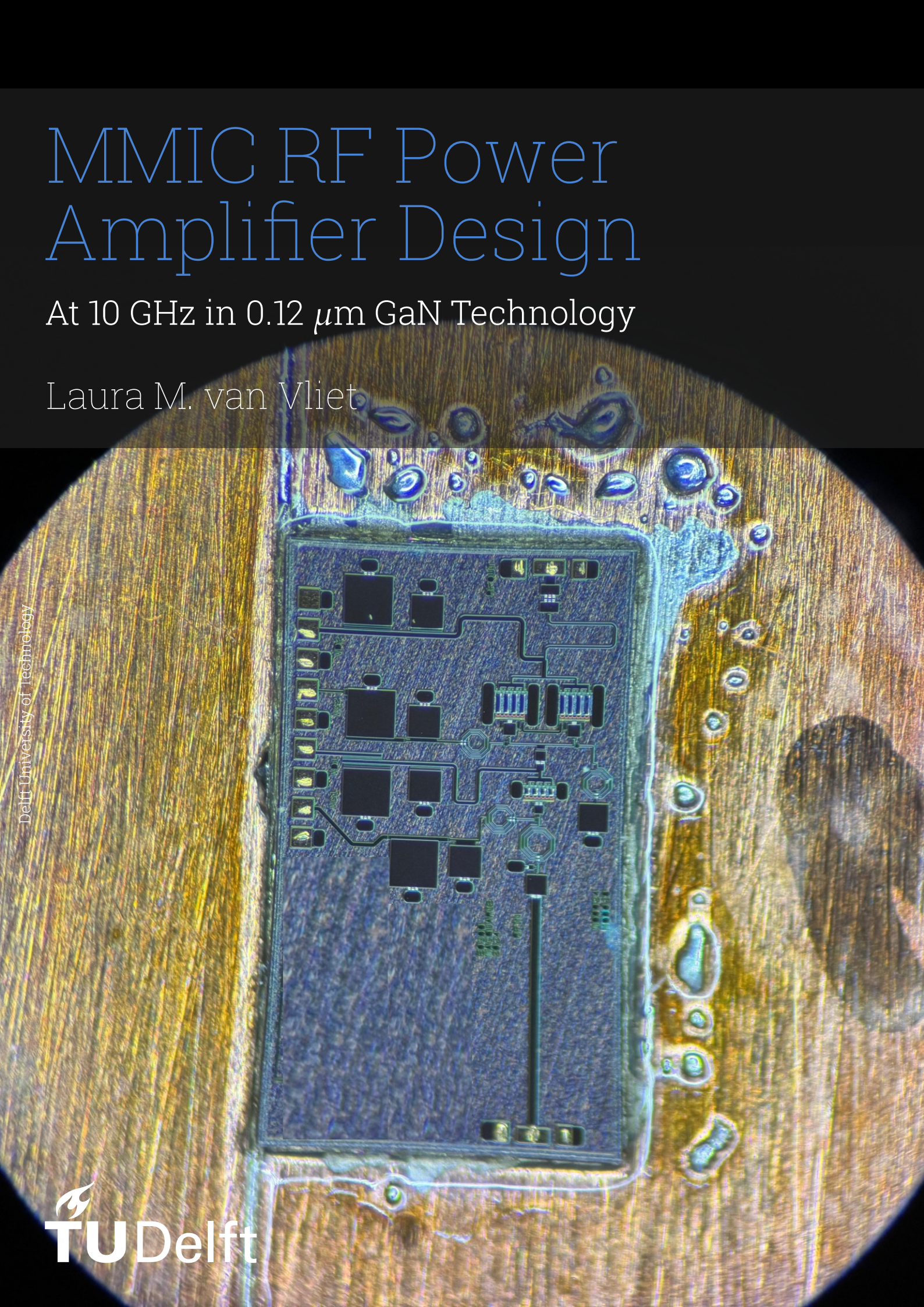
# MMIC RF Power Amplifier Design

## At 10 GHz in 0.12 $\mu$m GaN Technology

Laura M. van Vliet



Delft University of Technology

TU Delft

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by


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*Laura M. van Vliet*
*Sydney, September 2025*

# Abstract

This work investigates whether a power amplifier (PA) designed for a lower operating frequency (10 GHz) can be effectively implemented using a process that has a $f_{max}$ of well above 100 GHz. Operating a process far below its maximum frequency offers potential benefits in gain and efficiency, but also presents challenges. Particularly for the stability of the amplifier, which becomes increasingly critical at high gain levels.

To investegate the potential for such an RF power amplifier, Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) are used. This is a technology that forms the current State-of-Art for microwave high-power high-efficiency MMICs. The circuit is fabricated using WIN Semiconductors NP12-01 GaN-on-SiC technology with 0.12 $\mu$m gates. They offer a technology with one of the shortest gatelengths that are around in the industry.

First a Programme of Requirements was established, before starting the design and four Key Performance Indicators (power, efficiency, stability and size) were defined. A design process was followed that started with transistor measurements, after which an architectural design was made, followed by schematic implementation, electromagnetic (EM) modelling and final layout creation. Continuous refinement between schematic, EM and layout stages where necessary to avoid excessive simulation times. After design rule verification and stability checks, the circuit was submitted for fabrication, with MMIC samples received back approximately four months later, after which, an extensive characterization of MMICs was performed, through both small-signal as well as non-linear measurements.

All this work resulted in the following KPI's:

- For the power, a peak power of over 38 dBm was realized under dedicated measurement conditions and over 35 dBm for nominal measurement conditions (20 V $V_{DS}$) and a bandwidth of more than 2 GHz (-1 dB bandwidth) or 3 GHz (3-dB bandwidth) was obtained.
- For the PAE, 35% was nominally achieved over various bias points and frequencies.
- Unconditional stability was achieved.
- The size of the amplifier was 2x1.75 mm$^2$, resulting in slightly below 2 W/mm.

While amplifiers with higher absolute power at X-band exist, the NP12 process is unlikely to surpass the state-of-the-art in this regard due to its limited maximum drain voltage, which constrains the achievable output power. However, the measured efficiency and gain are promising for a first design iteration. Notably, the implementation of the stability analysis for this power amplifier took a significant effort, but was proved highly effective as no instability was observed at all during the measurements. Two variations of the amplifier were implemented to investigate the possibility of reusing the source via-hole for two adjacent output stage transistors. This variation, with re-used via-holes, worked similar to the baseline design, but exhibited a lower PAE.

In conclusion, the expectation is strengthened that the advantages of a mm-wave process used at X-band frequencies can pay off in a modest increase of the efficiency and a significantly increased gain. Finally, the work resulted in one conference publication, and two tutorial documents for future students (an AWR student guide and MMIC mounting tutorial).

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# Nomenclature

## Abbreviations

| Abbreviation | Definition |
|---|---|
| ADS | Advanced Design System |
| CW | Continuous Wave |
| DC | Direct Current |
| DRC | Design Rule Check |
| DUT | Device Under Test |
| EBL | E-beam lithography |
| EM | Electromagnetic |
| FET | Field Effect Transistor |
| GaAs | Gallium Arsenide, semiconductor material |
| GaN | Gallium Nitride, semiconductor material |
| GDSII | Graphic Design System 2 |
| HBT | Heterojunction Bipolar Transistor |
| HEMT | High Electron Mobility Transistor |
| IC | Integrated Circuit |
| InP | Indium Phosphide, semiconductor material |
| KPI | Key Performance Indicator |
| MAD Lab | Macquarie Analog Devices Laboratory |
| MESFET | Metal Semiconductor Field Effect Transistor |
| MIM | Metal Insulator Metal, capacitor type |
| MMIC | Monolithic Microwave Integrated Circuit |
| PA | Power Amplifier |
| PAE | Power Added Efficiency |
| PCB | Printed Circuit Board |
| PDK | Process Development Kit |
| RF | Radio Frequency |
| S-parameter | Scattering parameter |
| SEM | Scanning Electron Microscope |
| Si | Silicon, here used as substrate material |
| SI | Semi-Insulating |
| SiC | Silicon Carbide, substrate material |
| SiGe | Silicon Germanium, semiconductor material |
| SOLT | Short, Open, Load, Through, calibration standard |

| Abbreviation | Definition |
|---|---|
| TaN | Tantalum Nitride, integrated resistor material |
| TRL | Through, Reflect, Line, calibration standard |
| VNA | Vector Network Analyzer |
| X-Band | 8–12 GHz |

# Symbols

| Symbol | Definition | Unit |
|---|---|---|
| $f$ | Frequency | [GHz] |
| $R$ | Resistor | [Ω] |
| $Z$ | Impedance | [Ω] |
| $C$ | Capacitance | [pF] |
| $L$ | Inductance | [nH] |
| $V$ | Voltage | [V] |
| $I$ | Current | [mA] |
| $l$ | Length | [$\mu$m] |
| $W$ | Width | [$\mu$m] |
| $P$ | Power | [dBm] |

# 1 Introduction

This chapter introduces the application and realization of microwave power amplifiers. The problem that is investigated in this thesis is formulated and the approach that was followed is introduced. Finally, the co-operation with Macquarie University in the frame of this Bachelor Project is described, as it forms the context of this work, and the structure of the thesis is described.

## 1.1. General Introduction

Microwave power amplifiers are all around us. Every cell phone has a small microwave power amplifier that allows the cell phone to connect to the local wifi router and provide connectivity to its user. Every microwave oven has a large microwave power amplifier, a magnetron, that provides the power to heat up our food is a short time. But there are many more microwave power amplifiers that are not so visible to the general public. They fly in space to make radar pictures of the earth, they are in basestations in the top of telecom towers to serve a large amount of users for cell phone coverage, they are in level gauge sensors that determine how full silos are filled with liquids (such as oil) or food (such as grain).

Those microwave power amplifiers essentially convert power from a power source into microwave power. They do so with a finite efficiency, which is never 100%, and the remainder of the energy is wasted in heat. This is problematic in different ways: it is not environmentally friendly to waste energy resources to create heat, the finite efficiency leads to shorter phone use-time (so you have to charge your phone more often), they lead to problems in cooling (how do you get rid of the heat in a satellite?) and many related problems. The problem is even more profound for power amplifiers than for other parts in the system, as usually the power involved is the largest for the power amplifier, so losses are significant at the system level.

By convention the term microwave refers to the frequency range from approximately 1 GHz to 30 GHz, while "millimetre wave" (mm-wave) refers to the 30 GHz to 300 GHz range. Despite this, the terminology is not always used in the most precise sense, as 80 GHz is still often called microwave.

Microwave power amplifiers, in the broadest sense, can be realized with vacuum devices or with semiconductor devices. In the past, vacuum devices were the only available option. They can still be found, for example in microwave ovens, but they are much less used than in the past. They still find use for extremely high power levels (with exotic devices such as klystrons) and in space applications (often using travelling wave tubes). They are increasingly replaced by semiconductor, or solid-state, power amplifiers. This thesis is concerned with solid-state power amplifiers.

## 1.2. Solid-State Microwave Power Amplifiers

A solid-state microwave power amplifier consists of a semiconductor die, the 'chip' that performs the actual amplification. On or around the chip is a matching network that establishes the right performance in view of the source and load impedances. For its actual application, the chip is packaged in for example a plastic or ceramic package. Plastic packages are cheaper, and often found in commercial applications, ceramic packages are more expensive but can provide hermetic properties, amongst others, and are for example found in satellite systems. When the matching network is integrated on the same chip, we speak of a 'Monolithic Microwave Integrated Circuit' (MMIC), as all elements are monolithically (on the same substrate) integrated.

For the semiconductor technology, we distinguish between the material system and the device type. The material system determines the elementary characteristics of the transistor (such as the maximum frequency of operation and the maximum current density). Materials of choice for microwave power ampliers can be SiGe, GaAs, InP and GaN. In this work, GaN (Gallium Nitride) is used for reasons discussed later in this thesis. With that material system, different transistor devices can be made. Choices include MESFET, HEMT, HBT and several other transistor devices. We have been using a GaN HEMT device design as this currently offers the best performance in terms of power density and microwave gain. The GaN HEMT technology used is finally classified by the length of the gate: a short gate leads to a high frequency at which the transistor can operate.

Finally, also the substrate material is of importance. For GaN devices, two substrates are commonly found: Si or SiC. A silicon substrate is more compatible with the large volume IC manufacturing, which is almost always on Si. That can lead to a lower manufacturing cost. For microwave power amplifiers, however, the heat transport is crucial and there is a better choice available: SiC. This diamond-like material (transparent and very strong) outperforms almost all other materials including metals in its heat conductivity performance.

## 1.3. Problem Statement

The research question that was posed at the start of the work is whether we can design a lower frequency (10GHz) power amplifier in a power ampifier process that has an extremely high maximum frequency (well over 100 GHz). Actually, this 10 GHz is not really a low frequency as it is higher than for example wifi frequencies (usually 2.4 or 5 GHz), but it is low in the sense that it is not so close to the frequencies at which the technology is capable of.

Using a process well below its maximum operating frequency offers potential advantages in gain and efficiency, but also poses challenges, in particular for the stability of the amplifier. For power amplifiers, stability is always a critical factor, and is even more an issue at frequencies where there is so much gain. This advantage and the demonstration thereof has been performed at lower frequencies, but was not demonstrated for the class of (state-of-art) technologies (0.12 $\mu$m) that we are using. More common is to use a 0.25 $\mu$m GaN HEMT technology, that has a much lower maximum frequency of operation.

To investigate the potential for such an RF power amplifier, we use Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) with Electron Beam Lithography (EBL) gates. This is a technology that forms the current State-of-Art for microwave high-power high-efficiency MMICs: The circuit is fabricated using the WIN Semiconductors NP12-01 GaN-on-SiC technology with 0.12 $\mu$m gates (that is one of the shortest gatelengths that is around in industry.) and source-coupled field plates for high breakdown and 28 V operation. The process offers two interconnect metals, MIM capacitors, TaN resistors and through wafer vias. Process details can be found in [1].

## 1.4. Approach

The method to investigate the research question is through the design of a power amplifier IC and characterize its performance.

As the models available for specific power transistors is always problematic, the work started with

characterizing dedicated power transistors. This is important for two reasons :

- We need to choose the right size of transistor, that is big enough to support the output power that we want to realize, but not too big (because that sacrifices amplifier efficiency).
- For the right size of the transistor, we need to determine the load impedance at which optimum power and efficiency are available, these measurements are called load-pull measurements. This data is almost never available with the right accuracy.

In that process, test transistors were mounted on a carrier, which is a very delicate activity. Based on transistor data, we then created the amplifier topology (consisting of device sizes and their interconnection). An example is shown in Figure 1.1 below.

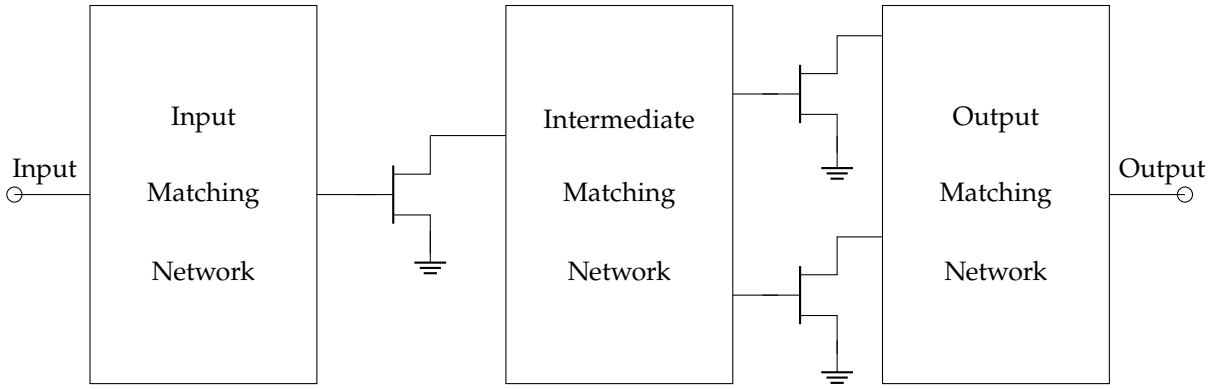



**Figure 1.1:** Example amplifier topology

In this, the transistor sizes need to be chosen such that the required power and gain can be accommodated. The matching networks are now the essential elements that need to be designed in detail and that will define the amplifier performance.

The topology for these three matching networks will then be designed, first with lumped elements to get the right topology and later with electromagnetic analysis to get the details right. Finally, biasing circuits and pad are designed and added. After all this, a layout file will be sent to the manufacturer (Win Semiconductors in Taiwan). They will return, after a processing time of several months, diced amplifier samples. These will be mounted, similar to the transistor samples, on a copper carrier and then be tested for its full functionality.

## 1.5. Collaboration with Macquarie University

The work that is reported in this thesis was performed as part of a bachelor project for the Electrical Engineering study at the Delft University of Technology. In this bachelor project, a co-operation with Macquarie University, Sydney, Australia, was essential. During two internships, first the design and later the measurement of the power amplifier was performed. This took part at the part of Macquarie University that is known as the MAD Lab, the Macquarie Analog Devices Laboratory, that is an integral part of the Macquarie School of Engineering.

## 1.6. Thesis outline

Following this introduction, the entire design and characterization process will be described. In chapter 2, the programme of requirements will be derived. This serves as a reference throughout the document. In chapter 3, the design methodology will be described. Included is the background needed to understand microwave power amplifier design. In chapter 4, the implementation of the design is described. Next to the design discussed, this also includes an experiment to share via-holes between adjacent transistors. The results might be useful for future work. The simulation results are reported in section 4.3. Chapter 5 describes the manufacturing phase. As this was performed by Win Semiconductors, this is only a short chapter. Chapter 6 describes the measurement setup. Specific for microwave measurements

is the elaborate calibration procedure that we need to go through; also this calibration procedure is documented. Chapter 7 reports on the measurement results. In chapter 8 we compare measurements against simulations and discusses the results. Chapter 9 presents the conclusions, including suggestions for future work.

# 2

# Programme of Requirements

In this chapter, the Programme of Requirements is developed. Three distinct parts are distinguished: the Mandatory Requirements, the Objectives (consisting of Functional, Manufacturing and System Requirements) and the Key Performance Indicators. Throughout this report all design design decisions, simulations and measurements are referenced back to these requirements to ensure traceability and compliance.

## 2.1. Introduction

The topic of this thesis is the design of an X-Band Power Amplifier. These power amplifiers are typically used in professional electronics. They are not commonly found in consumer electronics. Applications include sensor systems (in particular radar systems), communication infrastructure (in particular for links between base stations and to drive modulators for optical links) and aerospace systems (such as satellite links). Their prime function is to deliver microwave power at a defined frequency, and the topic of this thesis is to see whether very modern mm-wave technologies can be used at the lower X-Band frequency as well.

For the design of the amplifier, a Programme of Requirements (PoR) is established. The PoR consists of mandatory requirements and objectives. Finally, a set of Key Performance Indicators is outlined. The PoR will be used in the remainder of the thesis to assess the design and results. Throughout the entire report, we will refer back to the items listed in this chapter to assess compliance and to benchmark the achieved results against the initial performance requirements.

## 2.2. Mandatory Requirements

The following requirements arose:

[2.2.1] frequency of operation must be at X-Band (10 GHz).

[2.2.2] The output power of the amplifier must be above than 30 dBm.

[2.2.3] The amplifier must be unconditionally stable.

[2.2.4] The size of the amplifier is smaller than the maximum manufacturing reticle size.

These mandatory requirements reflect widely adopted industry standards for microwave power amplifier design. The choice of the X-band (10 GHz) frequency was made specifically by MAD Lab to align with wafer scheduled for fabrication, making it an ideal platform for both research objectives and for a first MMIC power-amplifier design.

## 2.3. Objectives

Under the objectives we distinguish 1) functional requirements, which are considered requirements that need a careful trade-off against each other, 2) manufacturing requirements, which are a result of the

technology in which the amplifier is manufactured and 3) system requirements, that originate from the environment in which the amplifier is tested or used.

### 2.3.1. Functional Requirements

[2.3.1.1] Frequency: The amplifier shall operate at 10 GHz with a bandwidth targeting 1 GHz.

[2.3.1.2] Output power: The amplifier shall deliver a maximum power targeted at 36 dBm output power at 10 GHz.

[2.3.1.3] Gain: The power gain shall be higher than 10 dB, targeting 15 dB.

[2.3.1.4] Efficiency: The amplifier shall exhibit a maximum PAE, targeting 40 %.

[2.3.1.5] Input reflection: The amplifier shall have an input reflection below -10 dBm.

[2.3.1.6] Sensitivity: The amplifier shall be insensitive to slight variations in external influences, such as a load mismatch or minor supply fluctuations.

### 2.3.2. Manufacturing Requirements

[2.3.2.1] Supply voltage: the PA shall operate at 20 V.

[2.3.2.2] Area: The area of the integrated circuit shall be as small as possible, but not exceed 6 $mm^2$.

[2.3.2.3] Height: The height of the integrated circuit shall be 1.75 mm to allow integration with other designs on the semiconductor reticle.

### 2.3.3. System Requirements

[2.3.3.1] The control interface must digitally control the bias and be able to disable and enable all bias voltages.

[2.3.3.2] The control interface must include current limits as protection feature.

[2.3.3.3] The in- and output impedance of the amplifier must be in line with industry standards (i.e. 50 Ohm).

[2.3.3.4] No DC voltage may be present at the RF in- and output ports, so that connected equipment will not be damaged or disrupted.

## 2.4. Key Performance Indicators

A concise set of Key performance indicators (KPI) is derived from the Objectives above, that facilitate assessment of the results:

[2.4.1] Minimum power over the designed bandwidth. The output power should be as high as possible.

[2.4.2] Minimum Power Added Efficiency over the designed bandwidth. The Power Added Efficiency should be as high as possible.

[2.4.3] Stability, should be absolute.

[2.4.4] Size, should be as small as possible.

# 3

# Design Methodology

In this chapter an extensive design methodology is introduced that briefly describes all aspects of the design phase. Manufacturing and measurement methods are described in the succeeding chapters.

The design methodology described includes the selection of semiconductor technology, a description of some relevant manufacturing and material characteristics of the chosen HEMT transistor, followed by the linear and non-linear transistor behaviour. The design process begins with a description of the load-pull measurements, which forms a critical foundation for determining the optimal operating conditions. Following this, the design and layout of the chip is illustrated. Finally, the check before submission for manufacturing are described. This consists of various stability checks, but also includes the manufacturer's design rule check and connectivity check.

## 3.1. MMIC Semiconductor Technologies

Selecting the right semiconductor technology for a Monolithic Microwave Integrated Circuits (MMICs) power amplifier depends on the output power requirements, operating frequency and frequency range, efficiency, linearity needs, thermal constraints and cost.
An ideal RF power amplifier (PA) must simultaneously deliver high output power, operate efficiently across a large frequency range, have a wide bandwidth, maintain linearity and be robust under varying operating conditions. Each technology, GaN, GaAs and InP, have their advantages and disadvantages that make them suitable for different applications.

Table 3.1 shows the fundamental properties of GaN, GaAs and InP. A larger bandgap allowes the material to withstand higher voltages, high electric breakdown fields ($E_c$), and operate at elevated temperatures. GaN has about two to three times the bandgap energy compared to GaAs and InP.
The saturated electron velocity plays a key role in switching speed and high-frequency performance, higher velocities enable faster device operation. To achieve high currents at these frequencies a high saturated velocity is desirable. GaAs has a very high electron mobility and is often used for that reason for high-frequency performance. GaN has a relative low electron mobility and is not the ideal choice for high frequencies.

The thermal conductivity ($\kappa$) of a semiconductor material is extremely important since it ensures efficient heat dissipation, improving reliability and power handling. Poor thermal conductivity leads to worse results at elevated temperatures, this can be seen with GaAs and InP. The relative permittivity indicates the capacitive loading of a transistor and affects the device terminal impedances [2].

| Property | GaN/ AlGaN | GaAs / AlGaAs | InP / InGaAs |
|---|---|---|---|
| Bandgap energy, $E_g$ (eV) | 3.44 | 1.43 | 1.35 |
| Electric breakdown field, $E_c$ (MV/cm) | 3 | 0.4 | 0.5 |
| Saturated (peak) velocity electrons, $v_{sat}$ ($v_{peak}$) ($\times 10^7$ cm/s) | 2.5 (2.7) | 1.0 (2.1) | 1.0 (2.3) |
| Electron mobility HEMT, $\mu_n$ ($cm^2$/V·s) | 2000 | 10000 | 10000 |
| 2DEG density, $n_s$ ($\times 10^{13}$ $cm^{-2}$) | 1.0 | < 0.2 | < 0.2 |
| Thermal conductivity, $\kappa$ (W/cm·K) | 1.3 - 2.1 | 0.5 | 0.7 |
| Relative permittivity, $\varepsilon_r$ | 9.0 | 12.8 | 12.5 |

**Table 3.1:** Material properties of MMIC Semiconductor Materials at 300 K [2]

## 3.2. High Electron Mobility Transistors (HEMTs)

With the material system of choice, GaN in our case, transistors are formed through a series of illuminations of photo-resist through masks, and a combination of etching and material growth techniques. This is a very complex process that is critical and highly specialized.

The transistor type that will be used is the microwave device that is currently the most popular for microwave power amplifier development: the High Electron Mobility Transistor (HEMT). An example of the cross-section of a GaN HEMT transistor is shown in Figure 3.1. A HEMT is a type of field-effect transistor; its operation is based on the possibility to deplete the region underneath the gate from charge carriers depending on a control voltage.

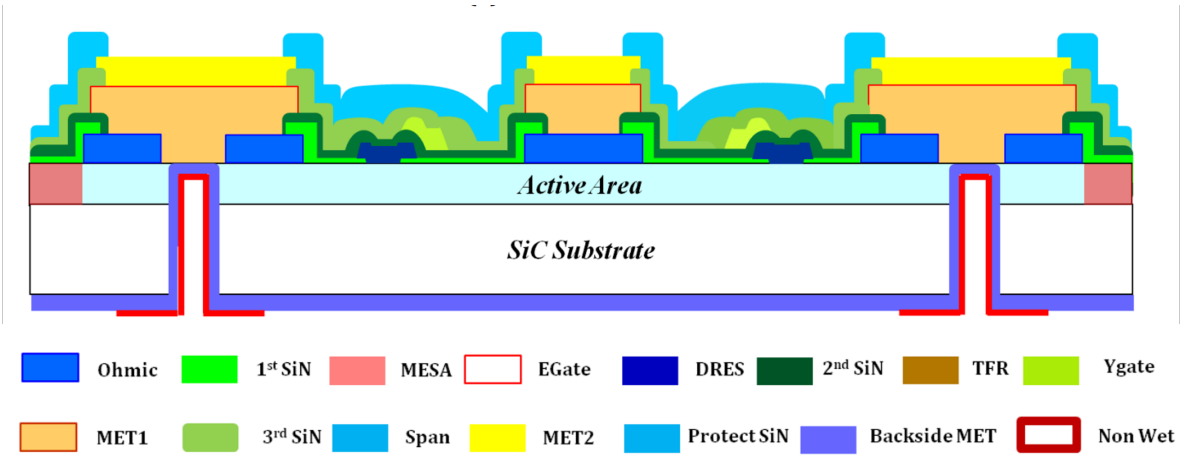



**Figure 3.1:** Cross-sectional view showing material layers of a GaN HEMT structure

There is a clear distinction between the GaN layers and the substrate. In the example, the substrate is semi-insulating (SI) Silicon Carbide (SiC). This is an excellent heat conductor, that largely defines the

good thermal properties.

On top of the substrate, a number of AlGaN and GaN layers are grown. These layers are epitaxially grown and the precise layer stack is a carefully guarded secret by the foundry. On top of the uniform layers, the contacts are present, both for the source and drain, as well as for the gate. The source and drain contacts are so-called ohmic contacts and consist of metal on top of highly doped GaN. They provide access to the active layer underneath with the lowest possible resistance.

The gate contact is a so-called Shottky contact, that depletes the area underneath from electrons depending on the bias voltage between the gate and the source. The gate is the smallest feature of the transistor and the way it is formed is usually through an electron-beam process. The shape of the gate can have different forms. In Figure 3.1, it has a trapezoidal shape, often used at lower frequencies. At mm-wave frequencies, including the process that we will use, the base of the gate is so narrow that it will create a high resistance, and a T-gate (also called a mushroom gate) is created, where the wide hat lowers the resistance of the narrow base. The foot of the T-gate is seen as a tiny detail in Figure 3.2. Sometimes, also field-plates are added. These are extensions to the gate that lower the field strength to avoid breakdown, necessary due to the high voltages encountered. This entire gate structure, including the T-gate and the field plate is illustrated in the SEM picture in Figure 3.2.

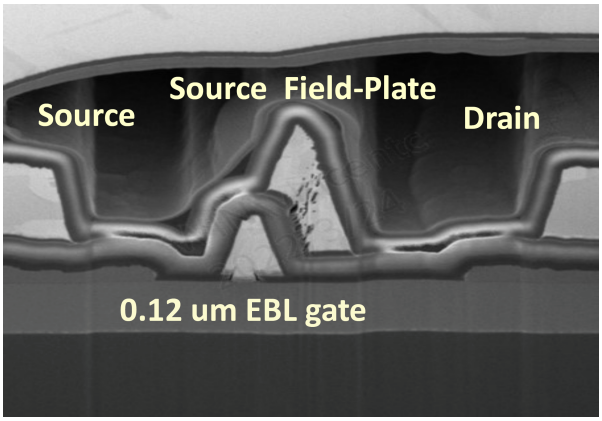



**Figure 3.2:** Overview of EBL gate fabrication and GaN HEMT structure used in the RF power amplifier design

The active layers, that are a more complex stack than shown in Figure 3.1, are essentially needed to create free electrons (from the donor layer, the AlGaN) to form a very thin 2-dimensional sheet charge (called a two-dimensional electron gas, or 2-DEG), which forms the HEMT channel. This is possible because of the special band diagram of the HEMT heterostructure, see Figure 3.3. In this band diagram, the curve for $E_c$ denotes the possible energy states for free electrons (that conduct), and $E_v$ denotes the possible energy states for the valence electrons, that do not move. The sharp dip in the middle of the $E_c$ curve denotes the channel, a very thin layer in which all the free electrons are captured. Note that the horizontal axis in Figure 3.3 corresponds to the vertical axis in Figure 3.1.

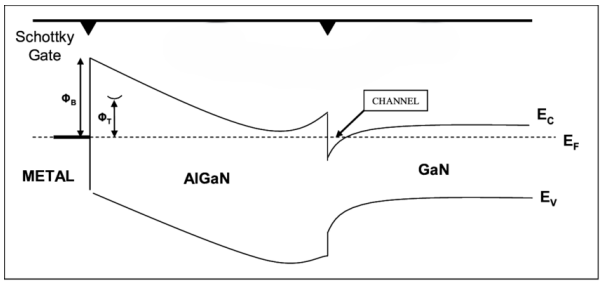



**Figure 3.3:** Energy band diagram of a HEMT structure [3]

For a microwave power amplifier, there are a few relations that are most important to assess its performance. In the first place, the transistor needs to be sufficiently fast. We measure that through the current-gain cutoff frequency (also called the transition frequency, $f_T$, the frequency where the current gain equals one) or the so-called maximum frequency ($f_{max}$, where the power gain equals one).

The current gain cutoff frequency ($f_T$) is given by:

$$f_T = \frac{g_m}{2\pi (C_{GS} + C_{GD})} \tag{3.1}$$

Maximum frequency ($f_{max}$) is given by [4]:

$$f_{max} = \frac{f_T}{\sqrt{4g_{DS}\left(R_{in} + \frac{R_S+R_G}{1+g_m R_s}\right) + 2 \cdot \frac{C_{GD}}{C_{GS}} \left(1 + g_m R_S\right)^2}} \tag{3.2}$$

The low distance between the gate and the 2DEG will lead to a high $g_m$. A small footprint of the gate will lead to a low $C_{GS}$ ($C_{GD}$ is much smaller than $C_{GS}$), and is hence the most important factor for determining the high-frequency capability of a HEMT. From the formula for $f_{max}$, we see that it follows $f_T$, where the term in the denominator will determine how much higher the $f_{max}$ will be than the $f_T$.

The last equation that provides insight in the relation between material parameters and transistor performance is the maximum current:

$$I_{D,sat} = q \cdot n \cdot v_{sat} \cdot W \tag{3.3}$$

This relation states that the maximum current $I_{D,sat}$ is related to the electron charge (q), the electron density (n), the saturated electron velocity ($v_{sat}$) and the width of the transistor finger (W). Together with the high breakdown voltage of GaN (that follows from the high bandgap), these equations explains why GaN is such a good material system for microwave power amplifiers.

## 3.3. Linear Transistor Behaviour

### 3.3.1. Linear Transistor Modeling

Linear (small signal) transistor models play a foundational role in power amplifier design, as they allow circuit designers to predict device behaviour under small-signal excitation. These models are essential for extracting key performance parameters such as: gain, input/output matching, stability. This is essential and widely used in the early stages of RF circuit design.

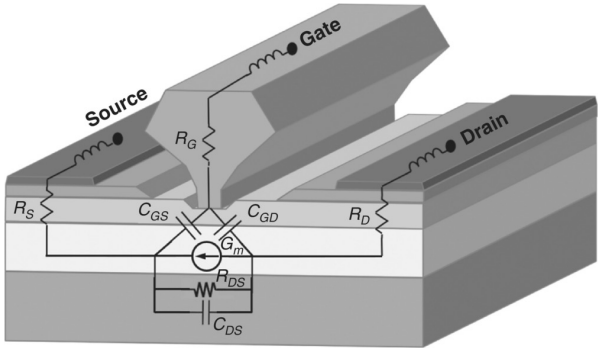



**Figure 3.4:** FET structure with equivalent circuit elements [5]

Figure 3.4 shows the structure of a Field Effect Transistor (FET) along with its equivalent circuit elements. This model separates the transistor into parasitic and intrinsic components. The parasitic elements ($R_G$, $R_S$, $R_D$, $L_G$, $L_S$, $L_D$) are primarily related to device metallisation and interconnects and are

independent of bias conditions. In contrast the intrinsic elements ($C_{GS}$, $C_{GD}$, $C_{DS}$, $R_{GD}$, $R_{GS}$) depend on the transistor's bias voltages and represent its active behaviour.

To develop an accurate linear model, these elements must be extracted reliably, typically through S-parameters measurements performed at a single bias point. This is because small-signal models assume linear operations around a fixed operation point. This makes it unsuitable for large-signal or non-linear analysis.

### 3.3.2. S-Parameters

In microwave-frequency circuit analysis, it is more practical to describe electrical behaviour using waves than voltages and current as this is easier to measure. The foundation of this approach is shown in Figure 3.5 for a two-port network.

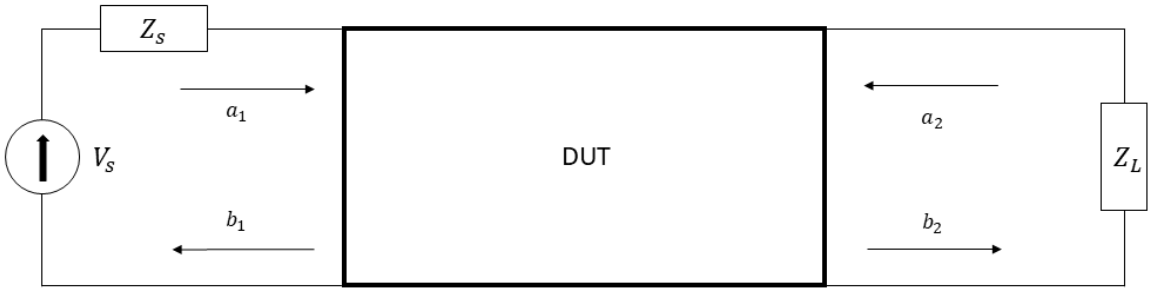



**Figure 3.5:** Two-port network

For a two-port network, the relation between incident waves $a_1$, $a_2$ and reflected waves $b_1$, $b_2$ is given in Equation 3.4.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{3.4}$$

Where:

- $S_{11}$ is the input reflection coefficient
- $S_{21}$ is the forward transmission (gain from port 1 to 2)
- $S_{12}$ is the reverse transmission
- $S_{22}$ is the output reflection coefficient

$$S_{11} = \Gamma = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{Z_L/Z_0 - 1}{Z_L/Z_0 + 1} = \frac{Z}{Z + 2Z_0} \tag{3.5}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{2Z_0}{2Z_0 + Z} \tag{3.6}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \frac{2Z_0}{2Z_0 + Z} \tag{3.7}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = \frac{Z}{Z + 2Z_0} \tag{3.8}$$

These parameters are complex and frequency-dependent and are typically measured using a Vector Network Analyser (VNA). IN RF design $S_{21}$ is also known as the small-signal gain and $S_{11}$, $S_{22}$ help assess input and output matching conditions [6].

### 3.3.3. Gain

At microwave frequencies the gain of a transistor is scarce and an accurate analysis is needed. Therefore, a distinction needs to be made between power gain, available gain and transducer gain. The differences between these definitions is primarily in the way the source and load are matched. In Equation 3.9 - 3.11 the different equations are shown. In Table 3.2 the difference between the equations is shown. The available power refers to the power that is provided by the source, while the delivered power represents the actual power that reaches and is absorbed by the transistor. For an RF power amplifiers, the transducer power gain is used as it also incorporates the effects of matching with the surrounding circuit [7].

The power gain can be expressed as the ratio of power dissipated in the load to the power delivered to the input of the two-port network:

$$G = \frac{P_L}{P_{in}} \tag{3.9}$$

The available power gain can be expressed as the ratio of power available from the two-port network to the power available from the source:

$$G_A = \frac{P_{avn}}{P_{avs}} \tag{3.10}$$

The transducer power gain can be expressed as the ratio of power delivered to the load of the power available from the source:

$$G_T = \frac{P_{\text{Power delivered to the load}}}{P_{\text{Power available from the source}}} \tag{3.11}$$

| | | $P_{out}$ | |
|---|---|---|---|
| | | available power $P_{avs}$ | delivered power $P_L$ |
| $P_{in}$ | avail $P_{avs}$ | available power gain | transducer power gain |
| | delivered power $P_{in}$ | - | power gain |

**Table 3.2:** Overview of gain definitions

## 3.4. Non-linear Transistor Behaviour

### 3.4.1. Non-linear Transistor Modeling

While linear (small-signal) models are highly effective for showing the effects of the transistor in low-power conditions, they fail to accurately predict the behaviour under large-signal conditions. Non-linear transistor modeling becomes necessary when the device is driven into regions where gain compression, harmonic generation or other non-linear behaviour becomes visible.
Accurate modeling of the non-linear transistor behaviour for a 10 GHz power amplifier is essential. Gallium Nitride (GaN) high electron-mobility transistors (HEMTs) exhibit strong non-linearities due to their wide-bandgap material properties and large voltage and current handling capabilities. Non-linear models take over when the response of the transistor no longer behaves linearly as assumed in the small-signal model. When driven to saturation, these non-linear behaviours influence metrics such as PAE, output power and harmonic distortion [8].

Figure 3.6 illustrates the linear transistor model, suitable for small-signal circuit analysis while Figure 3.7 shows the non-linear intrinsic model. The intrinsic model represents the active behaviour of the transistor, while the extrinsic components account for the passive connections of the transistor.

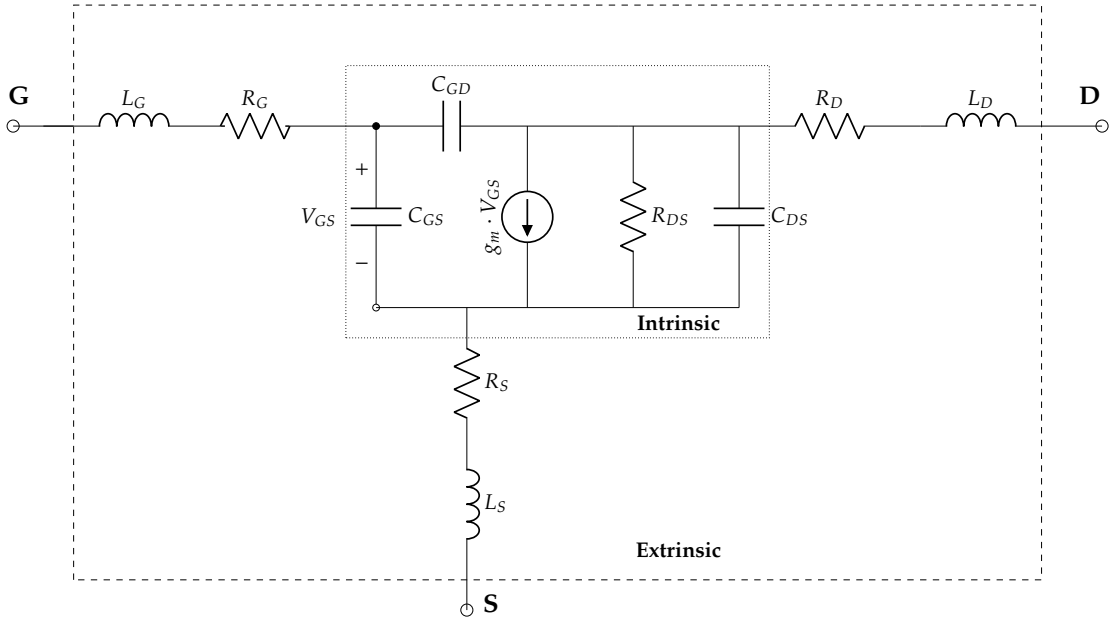



**Figure 3.6:** Linear Transistor Model

Linear models assume a fixed reponse at a defined DC bias point, which are used for impedance matching and stability analysis. In Figure 3.7 the intrinsic transistor elements that responsible for non-linear behaviours are shown, while the extrinsic elements, shown in Figure 3.6, remain linear. These non-linear behaviours of the intrinsic elements depend on the bias voltages and currents (at the bias point), thermal effects, frequency and material properties of GaN and are used to determine the compressed gain, output power and PAE.

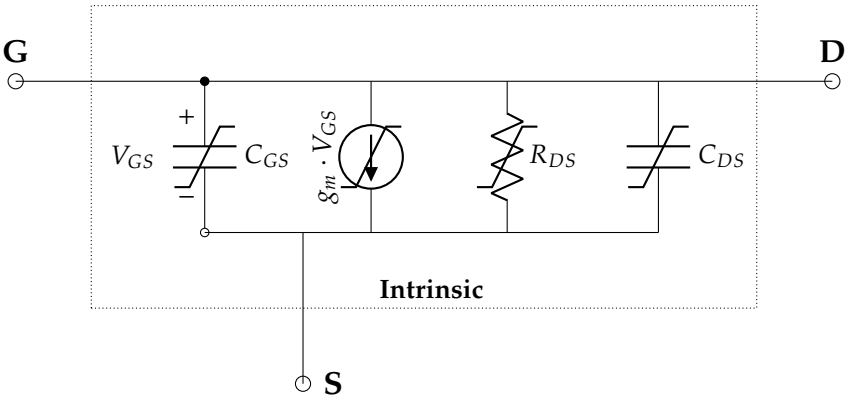



**Figure 3.7:** Non-linear Intrinsic Circuit Model

In Table 3.3 the differences between the linear and non-linear model are shown.

| | **Linear Modeling** | **Non-linear Modeling** |
|---|---|---|
| Operation region | Small-signal conditions, low power | Large-signal conditions, high power |
| Characterization Parameters | Scattering parameters (S-parameters) | large-signal metrics (Gain compression, PAE,$P_{out}$) |
| Operating point | Fixed at bias point | Varies with signal amplitude and bias voltage and currents |
| Behaviour focus | Small-signal gain, input/ouput matching and stability | Gain compression, power saturation, PAE and harmonic generation |
| Harmonics | Not modelled | Harmonic distortion included |
| Common Application | Low-power circuits, early-stage RF design | Load-pull measurements and large signal analysis |

**Table 3.3:** Difference between non- and linear transistor model

### 3.4.2. Large-Signal Metrics

When designing high-power amplifiers at 10 GHz, transistors rarely operate in the small-signal region. They are instead driven with RF power, pushing them into a non-linear region. Large-signal models are specifically developed to predict output power, efficiency and distortion.

#### Gain Compression

Gain compression describes the phenomenon where as the input power to a transistor increases, the output power no longer scales linearly and begins to saturate. This occurs when the device moves into the non-linear operating region.

The 1-dB compression point (P1dB) is a industry standard used for quantifying the gain compression. It is defined as the input power level at which the small-signal gain of the device decreases by 1 dB compared to its ideal linear behaviour.

At the 1-dB compression point, the gain becomes:

$$G_{compressed} = G_{small-signal} - 1dB \tag{3.12}$$

Figure 3.8 illustrates the concept of gain compression and the 1-dB compression point. The horizontal dashed line represents the ideal linear gain, while the solid curve shows the actual gain behavior as the device moves into its non-linear region.

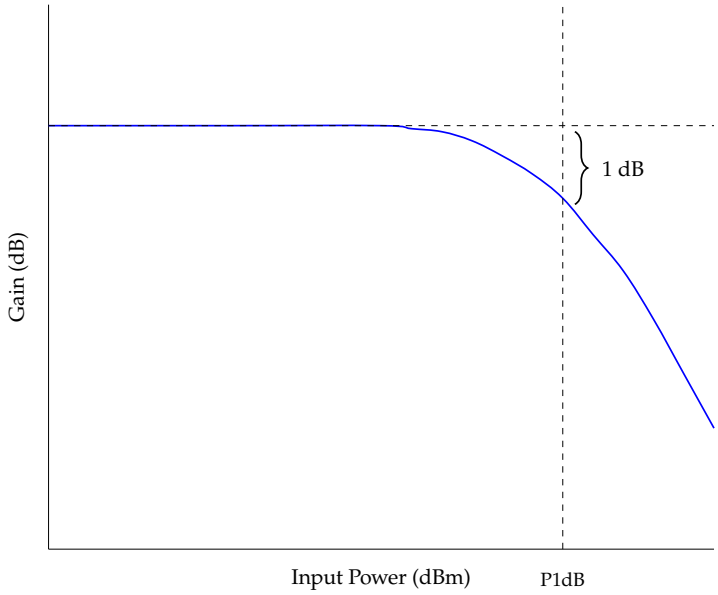



**Figure 3.8:** 1dB compression gain

Physically the gain compression arises from several mechanisms within the transistor:

- **Transconductance roll-off**, where the rate of change of drain current with respect to gate voltage decreases at high drive levels.
- **Voltage-dependent capacitance** ($C_{GS}$,$C_{GD}$) that vary with signal amplitude and bias conditions
- **Thermal effects**, where self-heating reduces the carrier mobility and shifts the threshold voltage
- **Charge trapping effects**, leading to temporary carrier depletion

These non-linear effects collectively reduce the effective gain and limit the amplifiers output power [9].

#### Output Power Saturation

As the input power to the amplifier increases, the output power initially grows linearly with the gain, as seen in Equation 3.13.

$$P_{out} = P_{in} + G_{linear} \tag{3.13}$$

However as the device approaches its physical limits. The transistor gets up to its maximum drain current and gate voltage, the gain then decreases resulting in gain compression subsection 3.4.2. In GaN HEMTs, ouput power saturation is driven by several mechanism:

- **Carrier velocity saturation:** At high electric fields electron velocity reaches a maximum, limiting the drain current.
- **Carrier density:** At high input levels, the channel can run out of available carriers (electrons) restricting further current increase.
- **Knee voltage constraint:** The drain voltage cannot swing below the knee voltage $V_{knee}$, limiting the RF voltage swing.
- **Transconductance reduction:** The channel's charge modulation becomes nonlinear at high gate voltages.
- **Thermal effects:** Self-heating reduces carrier mobility and maximum current.

For a matched load, the optimum resistance can be expressed as:

$$R_{opt} = \frac{V_{dc}}{I_{max}/2} = \frac{V_{dc}}{I_{dc}} = \frac{V_{dc} - V_{knee}}{I_{max}/2} \tag{3.14}$$

where $I_{max}$ is the peak drain current. Under this optimum loading, the maximum deliverable RF output power (saturation power) is:

$$P_{sat} = \frac{1}{2} \cdot (V_{dc} - V_{knee}) \cdot \frac{I_{max}}{2} \tag{3.15}$$

Beyond $P_{sat}$, increasing the input power further results mainly in increased distortion and does not significantly raise the output power [10].

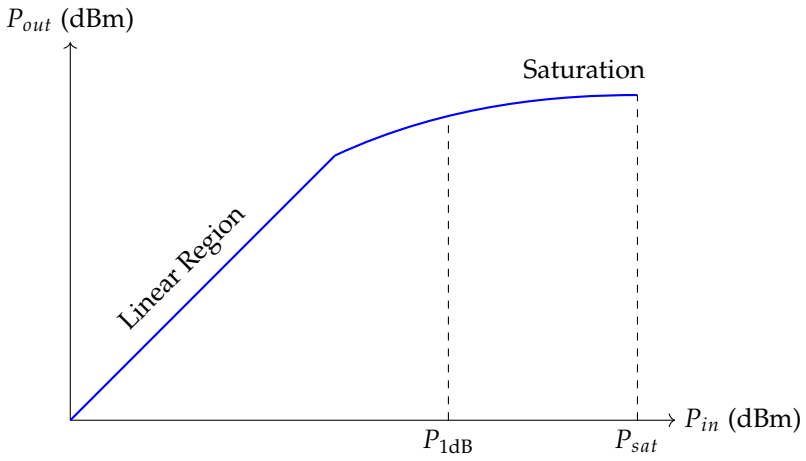



**Figure 3.9:** Typical output power versus input power characteristic of a GaN power amplifier showing the linear region, 1-dB compression point, and saturation region

### Power-Added Efficiency (PAE)

Power-added efficiency (PAE) is a key metric that measures how effectively a power amplifier converts DC power into RF output power:

$$PAE = \frac{|P_{out}| - |P_{in}|}{P_{dc}} \cdot 100\% \tag{3.16}$$

PAE does not simply increase and flatten at saturation. It exhibits a roll-over effect at the high input powers after reaching its maximum. This happens because the gain collapses, increased conduction losses, thermal degradation and breakdown limits seen in Table 3.4.

| Cause | Explanation |
|---|---|
| Gain Collapse | As the amplifier is overdriven, output power saturates while DC consumption continues to rise, reducing PAE as can be calculated with Equation 3.16. |
| Increased conduction losses | At larger powers the conduction losses increase, because more power has to be dissipated as heat instead of being converted to RF output power. |
| Thermal degradation | Self-heating reduces electron mobility and transconductance. |
| Breakdown limits | Approaching device breakdown increases leakage currents and trapping |

**Table 3.4:** Causes of Power-added Efficiency degration in GaN PAs [11, 12, 13, 14, 15]

### Harmonic Generation

RF power amplifiers are non-linear devices, meaning a sinusoidal input will produce output components at multiple frequencies (harmonics) in addition to the fundamental frequency.

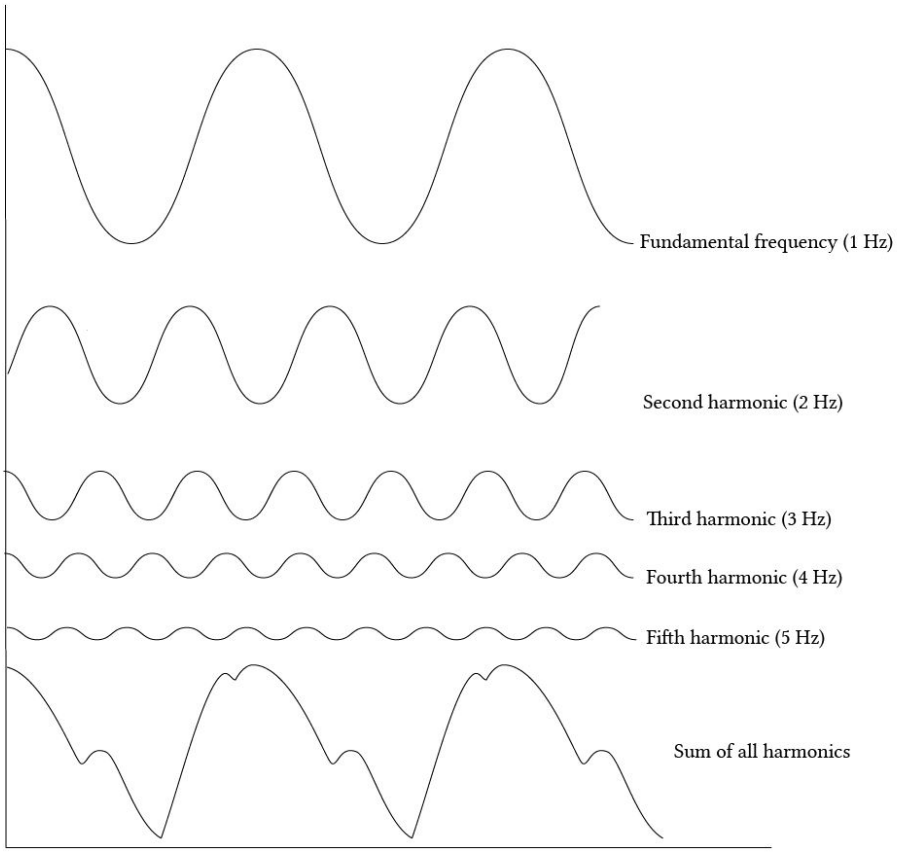



**Figure 3.10:** Illustration of a distorted waveform decomposed into its fundamental and harmonic frequency components [16]

In a transistor PA, the RF output current is a distorted clipped version of the input drive due to the device's non-linear I-V characteristics. This output can be expressed as a Fourier series containing the fundamental and higher-order harmonic components, as shown in Equation 3.17 - 3.20 [10]. The amplitudes of these higher-order harmonics depends on the bias point and input drive level, which together determines the conduction angle (portion of the RF cycle during which current flows). A larger conduction angle (Class A) means the output current waveform is more sinusoidal and thus contains fewer harmonics, whereas a smaller conduction angle (class B, AB or C) produces a more clipped waveform with more harmonics [17].

In class AB, the transistor conducts more than half the full RF cycle. The current waveform is thus partially clipped and asymmetric, leading to both even- and odd-order harmonics. The drain current can be modeled as:

$$i_d(\theta) = \begin{cases} \frac{I_{\max}}{1-\cos(\alpha/2)}\Big[\cos\theta - \cos(\alpha/2)\Big] & for\ \frac{-\alpha}{2} < \theta < \frac{\alpha}{2} \\ 0 & otherwise \end{cases} \tag{3.17}$$

The mean / DC current is:

$$I_{\text{dc}} = \frac{I_{\max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}. \tag{3.18}$$

The fundamental frequency components is:

$$I_1 = \frac{I_{\max}}{2\pi} \cdot \frac{\alpha - \sin(\alpha)}{1-\cos(\alpha/2)}. \tag{3.19}$$

And the n-th harmonic amplitude is:

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}\Big[\cos\theta - \cos(\alpha/2)\Big]\cos(n\theta)\,\theta, \qquad n \geq 2. \tag{3.20}$$

GaN HEMT at X-band generate harmonics primarily through their intrinsic non-linearities (transconductance compression and non-linear conductance) and are secondarily influenced by parasitic non-linear elements (capacitances, resistances). The main implication is accurately controlling and predicting harmonic content that require models that include effect like $g_m$ droop, knee voltage, self-heating and traps. GaN's harmonic behavior around 10 GHz is dominated by its channel physics and how those physics limit the RF waveforms. With load pull you can find the impedances of the fundamental signal and its harmonics (20 GHz, 30 GHz), after you can design to suppress the harmonics or leverage harmonics to enhance efficiency [10].

### 3.4.3. AWR Microwave Office™

Cadence AWR Microwave Office™ is the simulation tool used in this report for the analysis of the small- and large-signal metrics and implement the (non)-linear models. Advanced Design System (ADS) is another widely used industry-standard tool for microwave circuit design, but the choice for AWR in this work reflects the preference of the company and its established workflow. In terms of capabilities both tools are largely equivalent.

## 3.5. Load-pull

Load-pull refers to the process of presenting a known impedance to a Device Under Test (DUT) in order to experimentally determine its optimal performance. In power amplifier design, the best loading conditions depend strongly on the non-linear behaviour and distortion characteristics of the transistor. The load-pull systems aid in identifying the optimum loading conditions experimentally, physically changing load reflection coefficient for extraction of design parameters, such as output power and PAE from transistor devices.

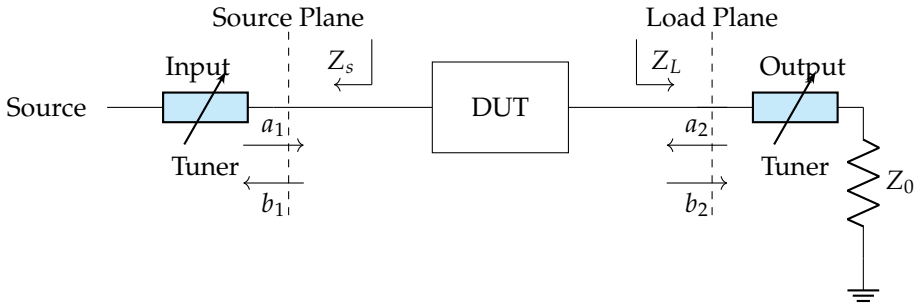



**Figure 3.11:** Schematic diagram of a load-pull measurement setup

A load-pull system consists of a tunable impedance tuner and a control mechanism that allows precise adjustment of the load reflection coefficient presented to the DUT. By varying the impedance, the system maps out the device's performance over a range of loading conditions. These measurements are used by designers as a target for the sign of the ouput matching network [18].

## 3.6. Impedance Matching Networks

Impedance matching is a critical aspect of RF and microwave circuit design for several reasons:

- Maximum power transfer: Proper matching between the source, transmission line and load ensures maximum power delivery while minimizing power losses.
- Improved signal-to-noise ratio: Impedance matching reduces reflections and as a result improve signal-to-noise ratio of the system, which is particularly important in sensitive applications such

as antennas and low-noise receivers.

- Reduced errors: Matching will reduce amplitude and phase errors in a power distribution network, leading to more accurate and stable system performance.

The process of designing a matching network involves several trade-offs. Choices must be made between the simplicity of the design, operational bandwidth, implementation and adjustability [7].

## 3.7. Chip layout

A foundry typically defines a maximum area that a single reticle can occupy. This reticle is shared among multiple designers, thereby constraining the area available for each individual device. During wafer fabrication, the wafer is separated into individual devices using a laser scribing process. For this particular fabrication run, the laser was limited to making only straight cuts spanning the entire reticle. Consequently, adjacent designs must have identical heights or widths, as illustrated in Figure 3.12.

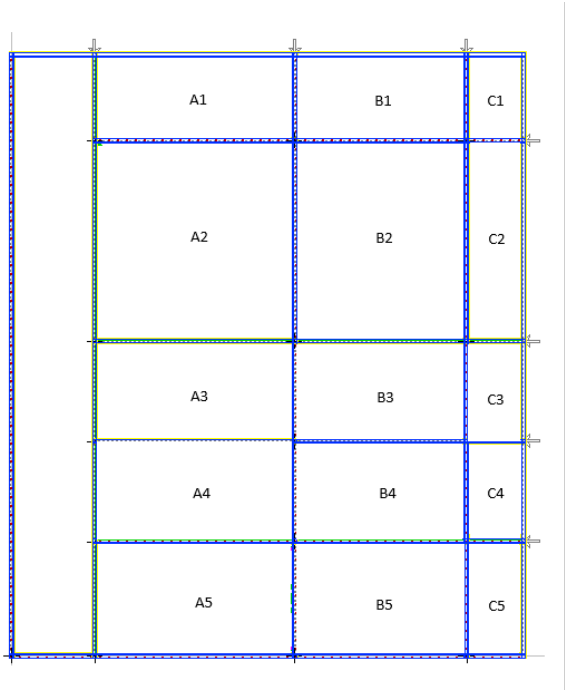



**Figure 3.12:** Reticle Layout with Section Labels

Unlike the schematic design phase, where constraints are largely limited to the capabilities of the simulation software, the physical layout must account for the routing to ensure that all parts fit correctly and maintain proper connectivity. Abnormally sized elements can pose challenges, requiring careful placement and routing to ensure that all parts fit correctly.

In the blank area on the left the left side in Figure 3.12 is used for the Process Control Module (PCM). It contains all the test structures that the foundry monitors to guarantee correct fabrication of the wafer.

## 3.8. Electromagnetic Simulation

Electromagnetic (EM) simulation allows the designers to analyze the internal behaviour of circuit structures in detail. EM solver discretize metal patterns into small elements or cells, also known as meshing. Reducing the cell size improves the accuracy of the simulation, but increases the computational time. Since the EM fields in each cell are described by differential or integral equations, even in linear conditions the simulations can be time-consuming.

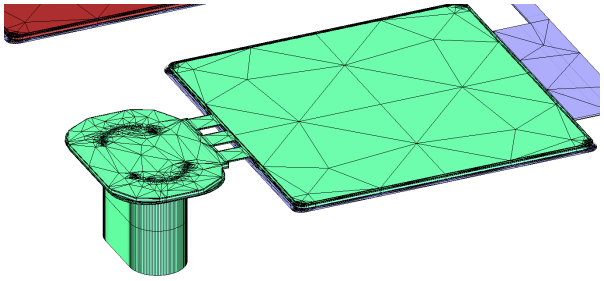


**Figure 3.13:** Via structure in mesh layout using Axiem EM solver

In this report, the Axiem EM solver is used. Axiem is a 2.5D planar solver, capable of handling an arbitrary number of homogeneous dialectric layers with arbitrary shaped metals across multiple planes, including via holes between the layers Figure 3.13. It's referred to as a 2.5D planar solver, because (while primarily planar) it can also simulated vertical via connections.

The main characteristics of the 2.5D planar solver are [4]:

- No fixed grid
- Rectangular and triangular elements
- Numerical Green's funtion
- Symmetry or walls require image theory
- Arbitrary spacial resolution

## 3.9. Stability Checks

As indicated in chapter 2, stability is a mandatory requirement. The analysis of the stability of a microwave power amplifier is not straightforward, due to the architecture of the power amplifier (with both cascaded and parallel transistors), due to the non-linearity and due to the large number of variables to be considered (input power, input frequency, load impedance, source impedance, all bias voltages, temperature, etc.).

The problem is addressed by first establishing stability in the nominal linear case, extending this in a kind of sensitivity analysis to input and output impedances and bias voltages. After satisfying results are obtained, the stability analysis is then extended to a non-linear analysis that also captures the stability in case of parallel transistor branches.

### 3.9.1. K-factor

The theory for assessing the stability of microwave amplifiers in the frequency domain is established when it concerns linear amplifiers of not more than two stages without parallel branches. A linear two-port is unconditionally stable if its characteristic frequencies remain in the left half of the complex frequency plane [19].

$$K = \frac{1 - |S_{11}| - |S_{22}| + |\Delta|^2}{2|S_{12}| \cdot |S_{21}|} \tag{3.21}$$

with

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.22}$$

The circuit is:

- **Unstable** when $K$ is below zero. This is indicating an unacceptable amplifier design that needs to be modified.
- **Unconditional stable** when $K$ is above one. This indicates that regardless of the source and load terminations presented to the amplifier, the amplifiers will be stable.

- Conditionally stable when $K$ is between zero and one. This indicates that depending on the input and output terminations, the design can be stable or unstable. For the complete amplifier this is not acceptable, but for individual amplifier stages it might not be a problem. For example, the source impedance presented to the second stage of a two-stage amplifier is well controlled in the design, it's the output impedance of the first stage. When this well-controlled impedance is in the stable region, the total amplifier will still be unconditionally stable.

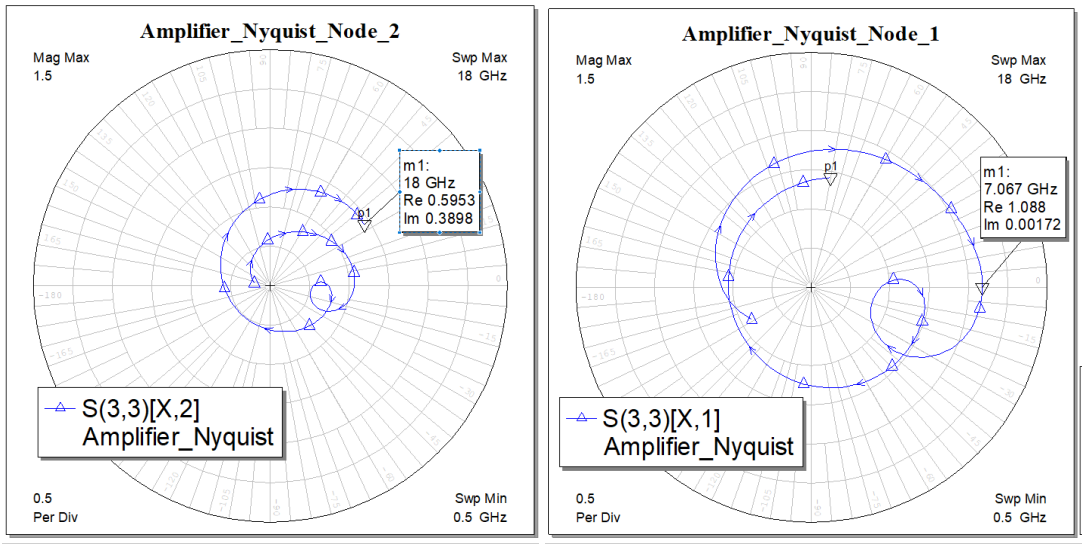
This analysis is then repeated for different drain and gate-voltages through nested drain and gate-voltage sweeps. The argument that drain and gate voltages are fixed and stability does not need to be assessed for variations does not hold. Apart from variations in the setup (tolerances in the supply voltages but also accidental application of the wrong voltage), upon startup the end voltages will never immediately be presented to the amplifier, but appear in a ramp or exponential manner. During all possible combinations of bias voltages at startup, the amplifiers needs to be stable to avoid accidental oscillations that may lead to damage or destruction of the amplifier.

### 3.9.2. Ohtomo Stability Analysis

The analysis at subsection 3.9.1 is easy, fast and powerful, but doesn't cover amplifiers with parallel transistors, non-linear stability and amplifiers with more then three stages. For microwave power amplifiers, particularly the problem of odd-mode oscillations that come in a variety of forms, needs to be solved. They are often triggered under dynamic load conditions such as signal envelope or thermal effects.
Traditionally, designers access stability by plotting stability circles on the Smith chart and ensure that no passive terminations fall in unstable regions. Only this lacks the completeness of multiloop feedback systems, especially those with interdevice coupling or distributed networks.
In these cases the k-factor analysis needs to be complemented with a method that identifies these other stability problems. As an alternative Ohtomo is introduced: generalized and systematic method to analyze the stability of multidevice amplifiers, treading the system as a feedback network compased of two n-port blocks: a active device network with s-matrix S, and a passive enbedding network with S-smatrix S', connected at n interface ports. The overall system behavior is captured by the matrix Equation 3.23 where $I_n$ is the identity matrix.

$$M_n = S'S - I_n \tag{3.23}$$

The Nyquist criterion is then applied to a set of open-loop transfer functions, derived from the signal flow graph of incident and reflected wave at each port. These transfer functions are given in terms of the determinant and co-factors of $M_n$, allowing identification of right-half-plane poles, and hence unstable modes. This method is compatible with AWR by inserting ideal circulators and isolators at the interface ports. These components isolate specific feedback paths, enabling extraction of the required Nyquist plots directly from S-parameter simulations. By observing whether the open-loop transfer functions encircle the critical point 1 + j0 in the complex plane, the presence and severity of potential instability can be determined [20].




**(a)** stable **(b)** unstable

**Figure 3.14:** Nyquist stability analysis of amplifier showing (a) stable and (b) unstable cases

This methodology enables precise, assumption-free analysis of multiloop instabilities in high-power GaN amplifiers, supporting more robust design and validation during the simulations phase.

## 3.10. Design Rule Check

Chip fabrication is subject to strict layout constrains defined by the foundry. To ensure manufacturability, every design must undergo a Design Rule Check (DRC), which verifies compliance with the foundry's specifications. These rules enforce requirements such as minimum spacing between materials, allowable metal angles and other geometric constraints necessary for reliable fabrication. This requires some small adjustments to ensure the design complies with the rules. Only after the design successfully passes DRC can it be placed onto the reticle and exported as a GDSII layout file, which is then submitted to the foundry for fabrication.

## 3.11. Connectivity Check

At the complete end a connectivity check is performed to ensure that all metal layers are properly connected without unintended gaps. This step also verifies that the correct components are interconnected, preventing accidental shorts (e.g. across a capacitor) or misrouted connections. The connectivity check is deliberately carried out at the very end, because even minor adjustments to the layout can unintentionally break connections, making an early check unreliable. In Figure 3.15 an example of a connectivity check is shown.

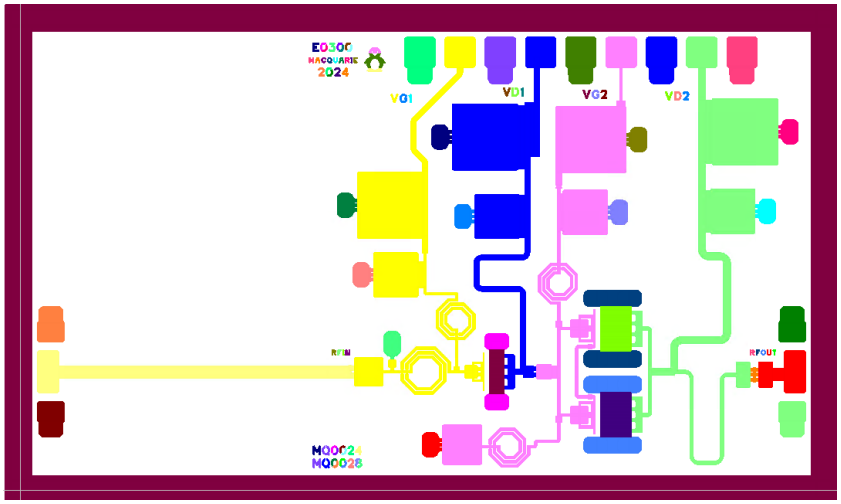



**Figure 3.15:** Connectivity check

# 4

# Design Implementation

In the previous chapter, chapter 3, the theoretical foundations and design principles were presented in detail. This chapter focuses on translating that theory into a practical circuit implementation. The design was made using the NP12-01 GaN process proviced by WIN Semiconductors, which offers high-performance Gallium Nitride technology well-suited for power amplification applications as can be seen in section 3.1.

A step-by-step approach is taken to implement the amplifier, including device selection, matching network design, layout considerations, electromagnetic simulations, while ensuring compatibility with the fabrication process (PDK). The order of this chapter is in the same order as the theoretical chapter chapter 3.

## 4.1. NP12-01 Technology

The key features of the 0.12 $\mu$m depletion-mode GaN HEMT technology are summarized below [21]:

- Manufactured on 100 mm SiC wafers
- 0.12 $\mu$m gate with source-coupled field plate
- 28 V operation, ft = 38.5 GHz
- Typical power density of 3.7 W/mm at 29 GHz
- 215 pF/mm2 capacitor
- Through-wafer vias for grounding

The lines, MLIN and MCTRACE, all are from metal 1, metal 2 or thick metal. These lines can handle a certain amount of current per $\mu$m, as is shown in Table 4.1.

| Material | Current Density Limit |
|---|---|
| Metal 1 | 6.15 mA/$\mu$m |
| Metal 2 | 23.44 mA/$\mu$m |
| Thick metal | 30 mA/$\mu$m |

**Table 4.1:** Current density limits for metal layers [22]

## 4.2. E0300: X-band Power Amplifier

As discussed in chapter 2 the power amplifier has four main functional requirements: the amplifier has to operate at 10 GHz with a minimum bandwidth of 1 GHz, the maximum output power is targeted at 36 dBm, the gain has to be higher than 10 dB and the efficiency has to be around 40%. In the following sections, it is translated into concrete design coices, simulations and verification steps.

### 4.2.1. Architecture

The overall architecture of the E0300 X-band power amplifier is illustrated in Figure 4.1. Both the E0300 X-band power amplifier as the E0302: E0300 with Alternative Transistor use the same structure (input, intermediate and output matching network), only with different values. Each matching network is designed to fulfill two key roles.

First the networks provide the necessary physical interconnection between all circuit elements, including microstrip lines (MLIN and MCTRACE), capacitors and inductors, to ensure proper biasing and connectivity to the transistors. This includes integrating bias feed lines and ensuring that each active device is supplied with the correct gate and drain voltages, as indicated in the highlighted bias subcircuits, red for gate feed lines and blue for drain feed lines.

Second, the matching networks serve the crucial function of impedance transformation between stages and at the interfaces to the system (the pads). This is achieved through a combination of shunt capacitors (capacitors to ground), inductors to ground and series inductors. Long microstrip lines are used deliberately to introduce inductive behaviour.

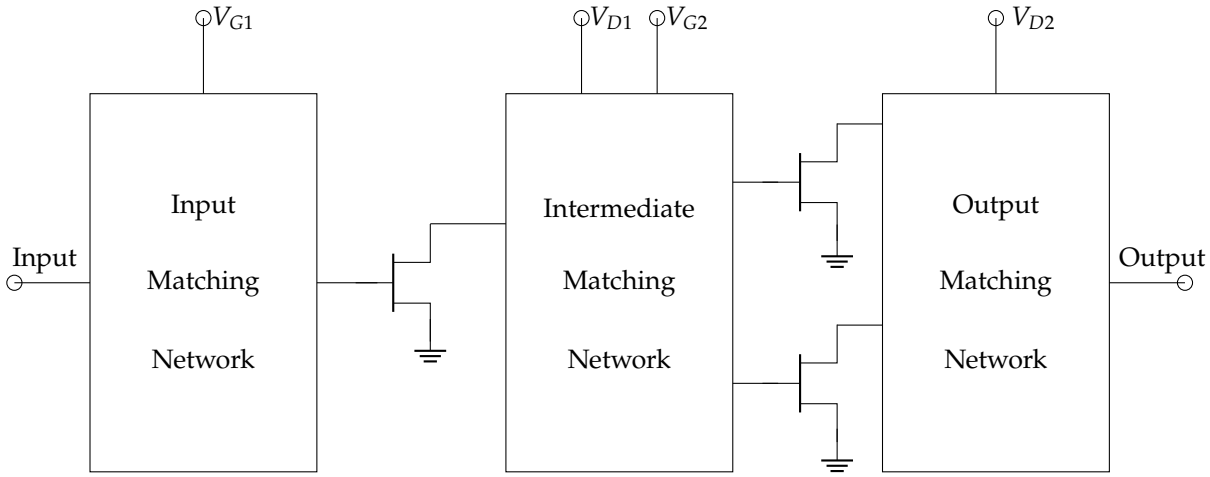



**Figure 4.1:** Block diagram of the two-stage amplifier showing the input, intermediate and output matching networks, along with the associated gate and drain bias connections

The detailed design methodology leading to these specific structures, including the iterative optimization of line lengths, capacitor values and bias network is discussed in subsection 4.2.2.

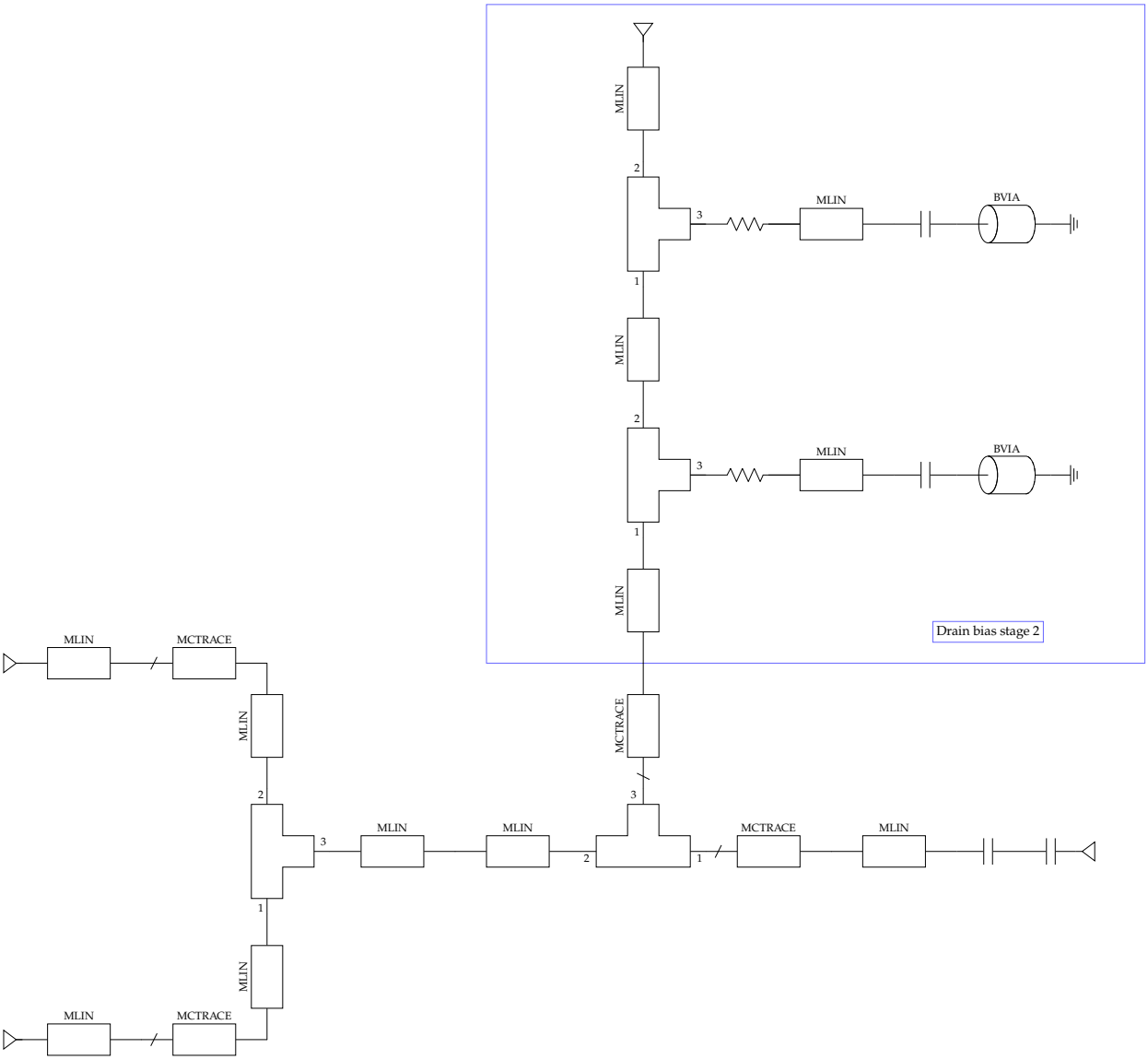



**Figure 4.2:** Detailed schematic of the output matching network, including bias circuitry for the second-stage drain ($V_{D2}$)

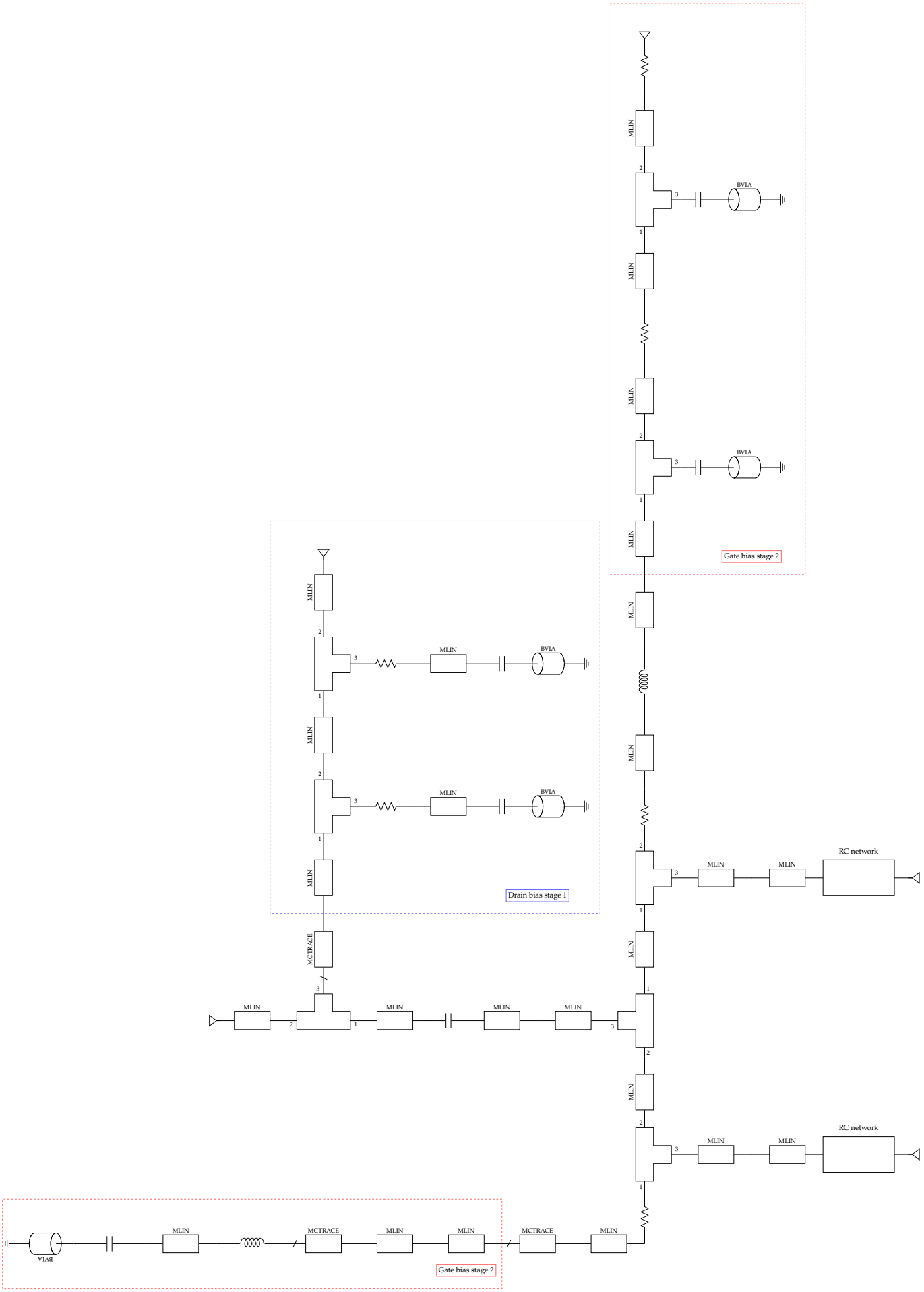



**Figure 4.3:** Detailed schematic of the intermediate matching network, including the associated gate ($V_{G2}$) and drain ($V_{D2}$) bias networks.

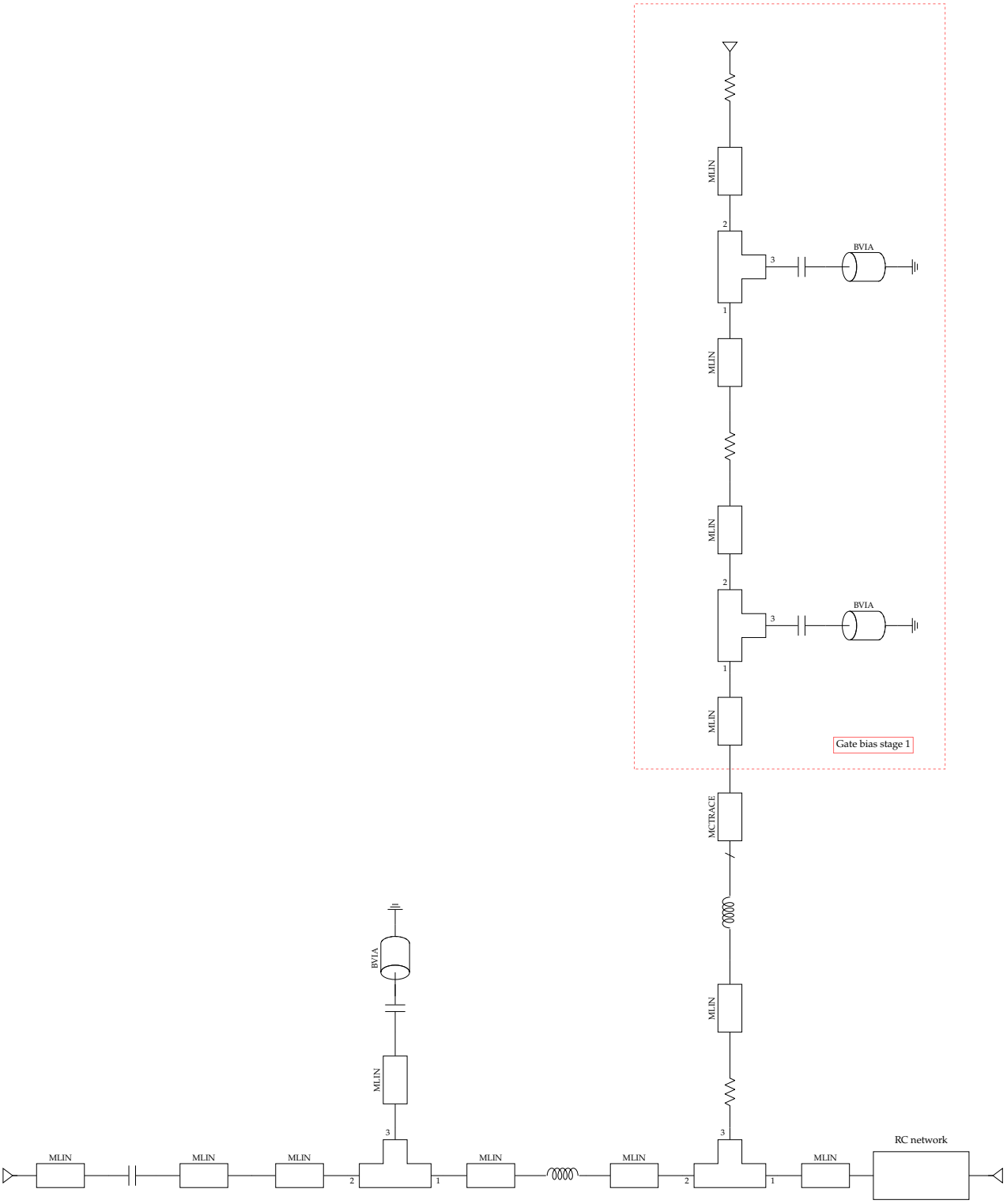



**Figure 4.4:** Detailed schematic of the input matching network, including bias circuitry for the first-stage gate ($V_{G1}$)

## 4.2.2. Implementation

### Load-pull analysis

The first step in the design process is to determine the required number of transistor and the appropriate transistor sizes for the power amplifier, discussed in the programme of requirements chapter under functional requirements item [2.3.1.2]. This analysis is carried out using the load-pull simulation setup

illustrated in Figure 4.5.

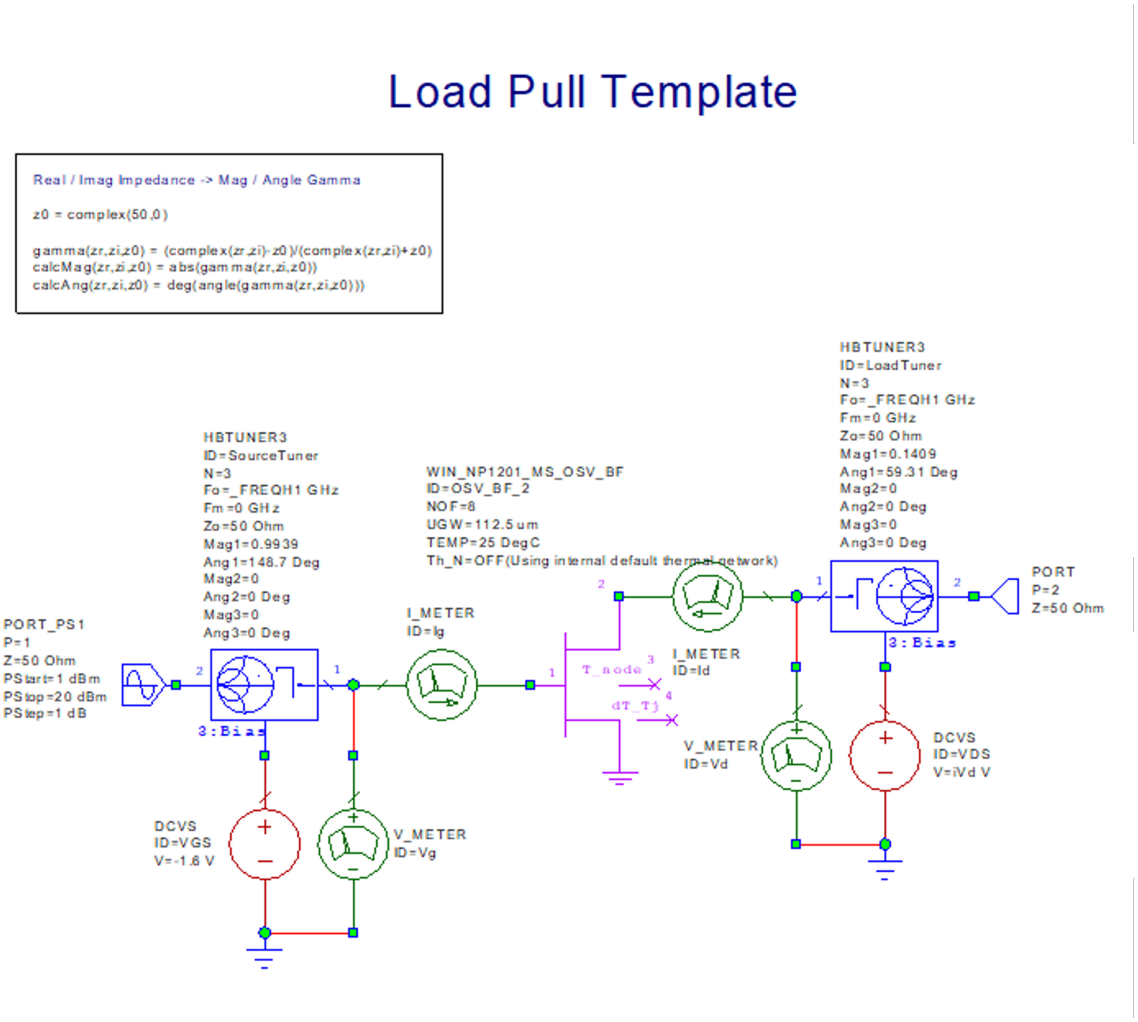



**Figure 4.5:** Load-pull simulation schematic showing the structure and tuning elements

The resulting load-pull simulation contours are presented in Figure 4.6, where the maximum achievable output power ($P_{out}$) and power-added efficiency (PAE) are depicted. These contours provide insight into maximum power that a signle transistor can deliver under optimal impedance conditions. To ensure this, the input impedance is first optimized and set within the HBTUNER element at the input of the transistor, after which the load-pull simulation is performed to obtain the contours shown.

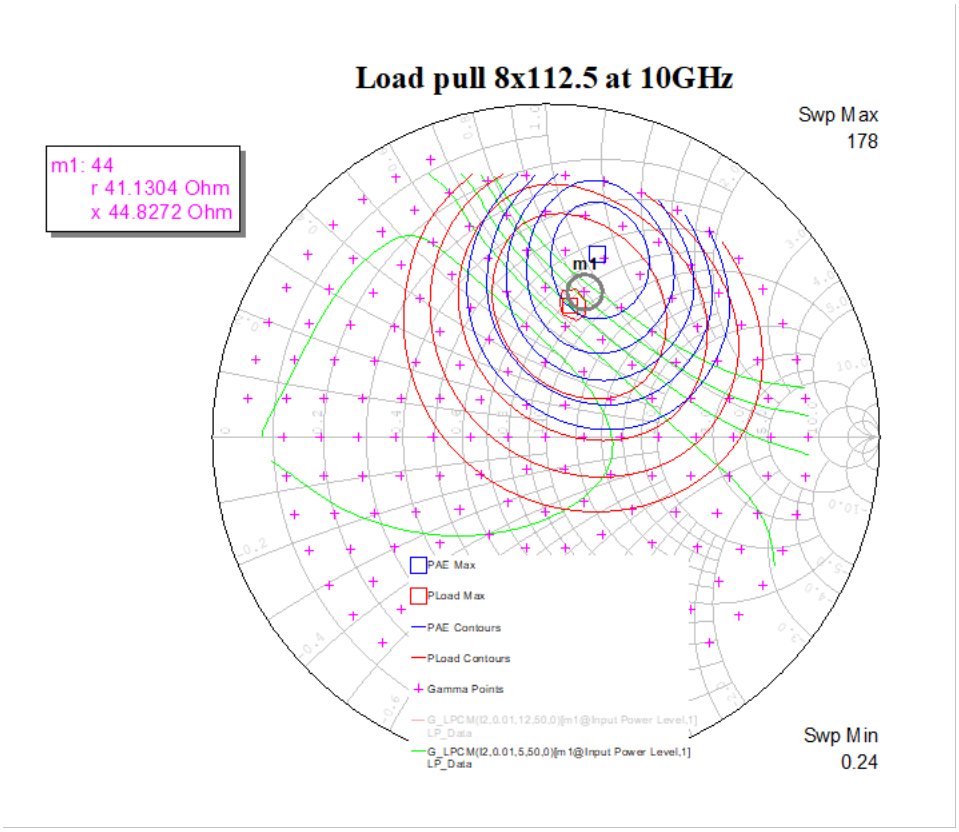



**Figure 4.6:** Load-pull simulation results of a transistor with 8 fingers with a width of 122.5 $\mu$m on a Smith chart showing contours of the output power ($P_{out}$), power-added efficiency (PAE) and drain current at 28 dBm $P_{in}$ and $V_d$ is 20 V

Based on these results at 20 V (Manufacturing requirement item [2.3.2.1]) and the required output power specified in the functional requirements item [2.3.1.2], it was determined that two transistors in parallel before the output stage are needed to meet the power target of 36 dBm. Consequently, the design adopts a two-stage power amplifier architecture, as illustrated in Figure 4.1. Each stage serves a distinct role: the input matching network primarily influences input reflections, the intermediate matching network governs overall gain and bandwidth and the output matching network dominantly impacts the output power and PAE.
For a power amplifier, achieving a high output power and power-added efficiency (PAE) is of primary importance. Consequently, the design is carried out starting from the output stage and progressing toward the input stage. Unlike low-noise amplifiers (LNAs), where minimizing noise is the primary design driver and the process begins at the input stage, noise performance is typically not a critical factor for power amplifiers. While lower noise is generally beneficial to avoid contributing to the overall system noise figure, in most applications the functionality and efficiency of the power amplifier outweighs noise considerations. As a results, noise is not treated as one of the primary design aspects for power amplifiers [23].

### Schematics

**Output Matching Network** To meet the system requirement of matching the output matching network to a 50 Ω load (system requirement item [2.3.3.3]), a load-pull simulation was performed. From the results shown in Figure 4.6, contours indicating the optimal power-added efficiency (PAE) and output power ($P_{out}$) were extracted for the frequencies 9, 10 and 11 GHz. Since both efficiency and output power are critical for this design, the chosen operating point was selected as a compromise between the two maxima. This trade-off typically depends on customer preferences. However, as this work is research-oriented, a balanced midpoint was chosen.

The design targets operation across the 9-11 GHz frequency band (functional requirement item [2.3.1.1]).

Therefore, the optimal load impedance was identified for each frequency within this range and plotted on a Smith chart to guide the design of the output matching network (Figure 4.7 and Figure 4.8).

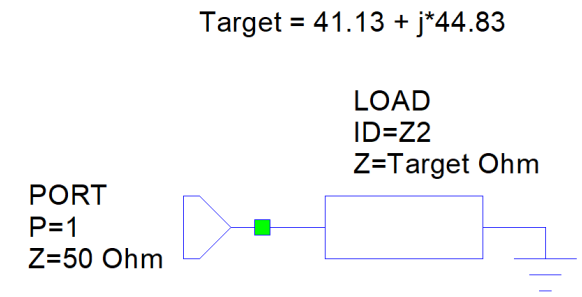
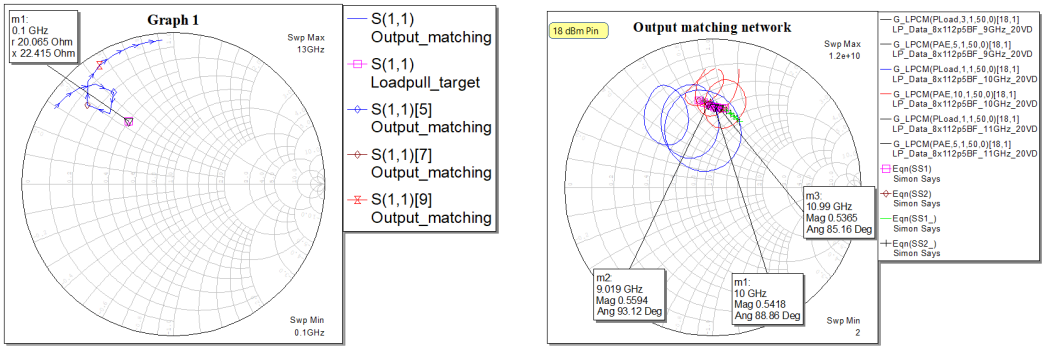



**Figure 4.7:** Circuit representation fo the target impedance (Z = 41.13 + j44.83 Ω) at 10 GHz

On the same chart, the impedance trajectory of the designed output matching network was plotted for a wider 8-12 GHz frequency band, with markers at 9, 10 and 11 GHz. To help with impedance matching, the load-pull contours were also superimposed in Figure 4.8. Achieving an optimal match requires iterative adjustments of the matching network topology, involving trial-and-error experimental steps with different components and line lengths as: adding shunt capacitors or inductors and tuning transmission line segments. In some cases, creating loops on the chart helps bring the frequency-dependent impedance points closer to the optimum region. Thereby improving the overall performance across the entire target bandwidth.

Certain elements in the design are essential in the output matching circuit. For instance, a DC-blocking capacitor is included at the output to isolate the amplifier from external imperfections and prevent them from disturbing the chips operation. Additionally, transmission lines are required to connect the transistor's drain to the DC supply and output. For stability considerations, both sides of the transistor must be symmetrically connected (Key Performance Indicator item [2.4.3]).




**(a)** Smith chart of the output impedance before tuning the output matching network

**(b)** Smith chart of the output impedance after tuning the output matching network

**Figure 4.8:** Smith chart output impedance transformation before and after application of the output matching network tuning

**Intermediate and Input Matching Network** The primary function of the intermediate matching network is to match the output of the first-stage transistor to the input of the second-stage transistor. This network has the biggest effect on the overall gain of the amplifier. If the impedance between these two stages are not well matched, a substantial portion of the power generated by the first stage may be lost rather than transferred, resulting in a notable reduction in total gain. Additionally, this stage is responsible for incorporating the first-stage drain bias and the second-stage gate bias into the circuit.

In contrast, the input matching network has the greatest influence on the input reflection coefficient ($S_{11}$) and the amplifier's bandwidth, as specified in the functional requirements item [2.3.1.5] and item [2.3.1.1]. Ensuring wideband performance and proper input matching is essential to achieving the desired frequency response.

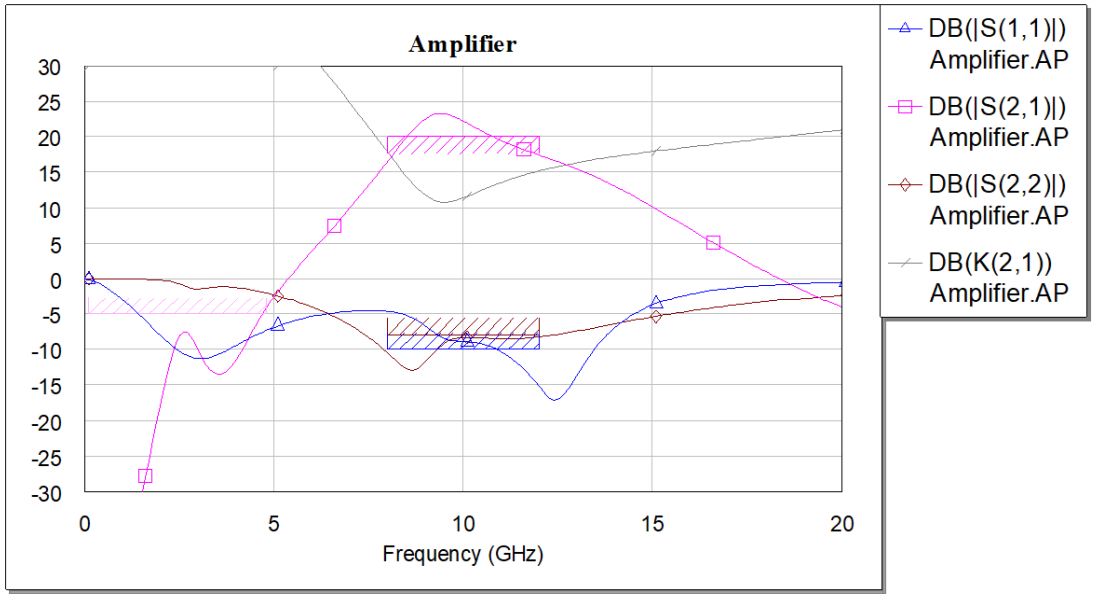



**Figure 4.9:** Simulated S-parameters ($S_{11}$, $S_{21}$, $S_{22}$) and stability factor (K-factor) of the designed amplifier

Stability can be considered the most critical requirement in the entire amplifier design, as outlined in the key performance indicator item [2.4.3]. Without a stable system, performance metrics such as output power ($P_{out}$) and power-added efficiency (PAE) become irrelevant. For this reason, symmetry is often preferred in the design as it can help improve inherent stability as it helps avoid oscillations.

Stability verification during this phase is conducted using the simulation results shown in Figure 4.9. At the target operation frequencies, both $S_{11}$ and $S_{22}$ should be as low as possible, indicating minimal reflection and efficient signal transfer. Across all frequencies these s-parameters should remain below 0 dB. Any value above 0 dB would indicate that more power is being reflected than accepted, which would mean the chip is oscillating.

In the context of both the input ant intermediate matching network, the K-factor is used as a stability metric and should remain greater than 0 dB (or 1 in decimals) across the entire frequency range (item [2.4.3]). Additionally, the gain ($S_{21}$) should be maximized within the desired frequency band while remaining low output it to prevent unwanted amplification. Irregularities or sharp spikes in any of these parameters may suggest potential oscillations and should be avoided at all times.

**Layout**

Once the schematic-level simulation results were deemed satisfactory, the focus is shifted towards the physical layout of the chip. The microstrip lines used to interconnect the various components must be designed to handle the expected current levels without violating reliability constraints. Each metal layer has a maximum allowable current density, as summarized in Table 4.1. In combination with the simulated current at the biases show in Figure 4.10, these limits are used to determine the minimum required line widths throughout the layout.

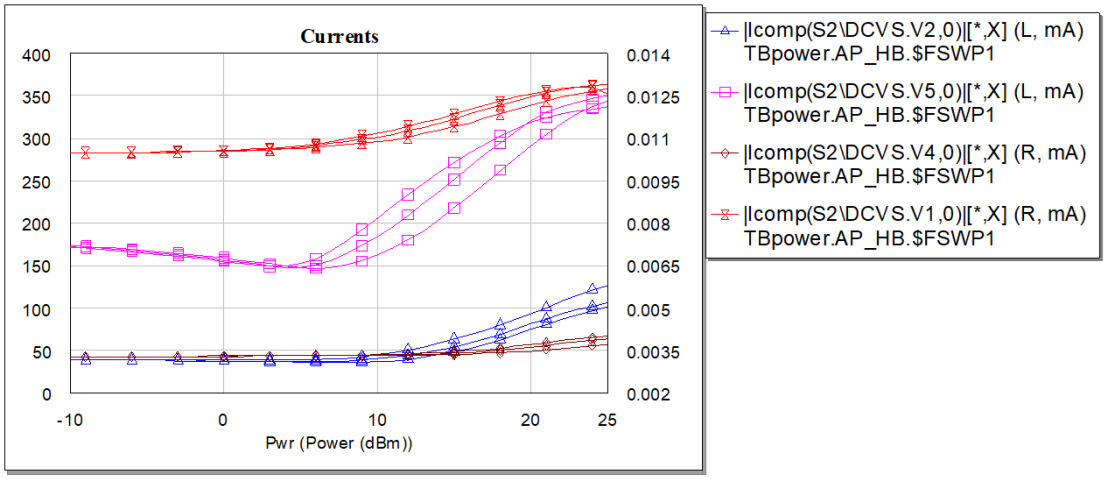



**Figure 4.10:** Simulated bias currents as function of output power ($P_{out}$). Drain currents, pink and blue, are plotted on the left y-axis, while gate currents, orange and brown, are plotted on the right y-axis.

For most high-current paths, thick metal is used due to its superior current-handling capability, in accordance with the robustness requirement defined in item [2.3.1.6]. The minimum required widths for different metal layers are calculated using the following expressions:

$$\text{Minimum width thick line} = \frac{I}{0.03} \tag{4.1}$$

$$\text{Minimum width metal 1 line} = \frac{I}{0.00615} \tag{4.2}$$

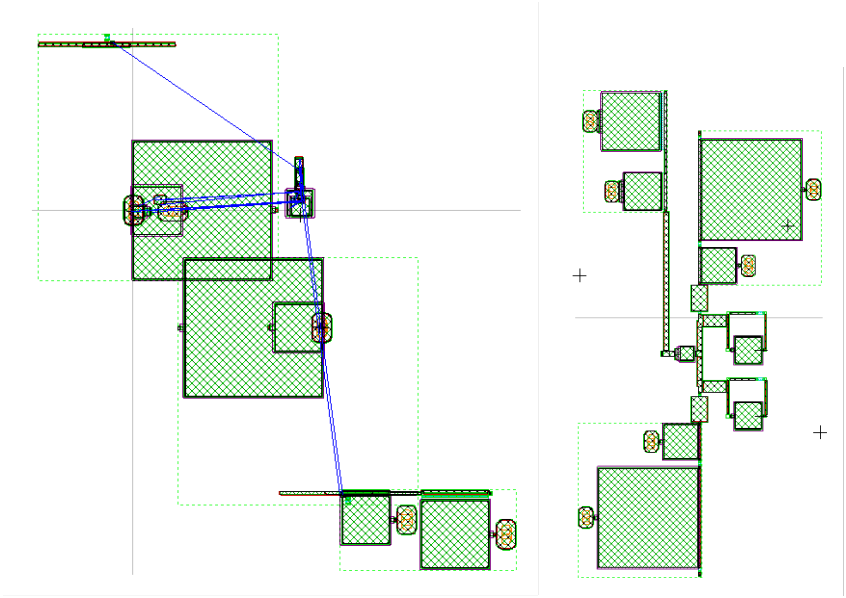
$$\text{Minimum width metal 2 line} = \frac{I}{0.02344} \tag{4.3}$$

Despite its higher current capacity, thick metal is not always the preferred choice in all parts on the circuit. For example, in gate bias lines where current levels are relatively low, it may be more advantageous to use metal 2 to achieve better impedance matching. Especially when the simulation shows narrow lines give the best results. This trade-off is discussed in more detail in Figure 4.2.2. In other situations, thick metal may be avoided to prevent shorting components in the layout, such as capacitors, or to allow for airbridges in the layout.

All the components have been dimensioned to safely handle the expected current levels within the circuit. However, we are not done with the layout yet. The schematic simply represents logical connections between components, assuming ideal interconnects with no physical length, little parasitic or spatial constraints. It implicitly treats all elements as if they are sufficiently spaced apart, without any considerations for overlap.
When transitioning to the layout, it becomes evident that this abstract representation is not directly manufacturable. Components are placed on top of each other, connect cross each other and design rule violations are inevitable as seen in Figure 4.11a. A considerable amount of manual adjustments are required to rearrange the elements, ensure layout design rules are followed and make sure the design fits in the reticle.

At this point all the components should be able to handle all the currents going through this circuit, but this chip can't be produced like this. The schematics will just look at the components and how you connected the ideal components without looking at the layout. If we start looking at the layout

everything is all over the place and on top of eachother, like in Figure 4.11a. After moving everything around to the correct spot and changing the sizes we end up with something like Figure 4.11b.



**(a)** Layout disorganized **(b)** Layout cleaned up

**Figure 4.11:** Example layout

From this point forward, the design process enters an iterative refinement phase. This phase consists of repeated cycles of simulation, analysis of the graphs, tuning, layout modifications and electromagnetic (EM) simulation, Figure 4.12. Each step in this loop affects multiple aspects of the design, making convergence towards a final solution a gradual and interdependent process. The goal of this process is getting back the results found in the schematic circuit.
For example, adjusting the value of a component may change its physical footprint in the layout, potentially causing overlap with neighboring elements. To resolve this, the layout must be updated, which in turn alters the spatial relationships between components. These spatial changes affect the results of the EM simulation, as coupling effects and parasitic effects vary with geometry. Consequently, the updated EM data must be reintegrated into the schematics for a new round of layout-level simulation. The resulting performance metrics, such as gain, output power, PAE and stability, must be re-evaluated every time leading to further tuning.

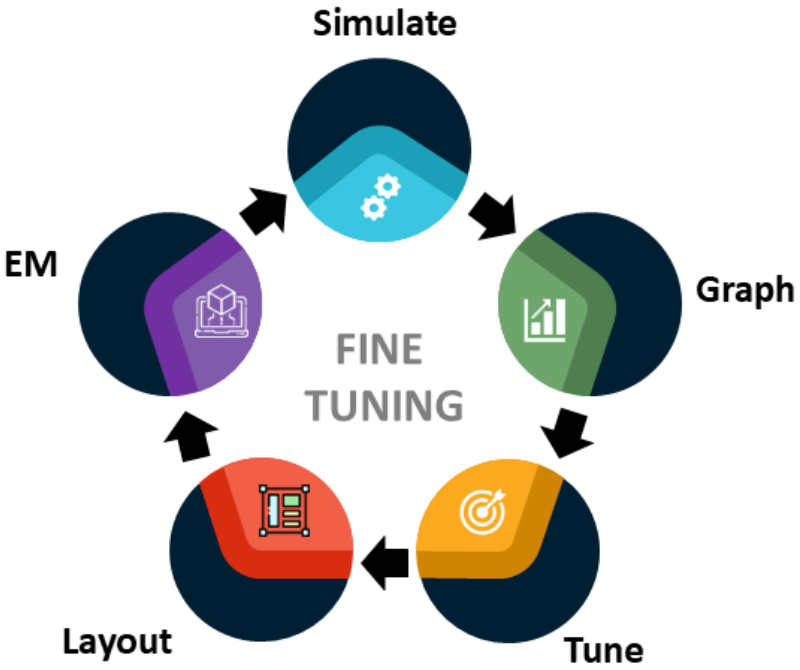
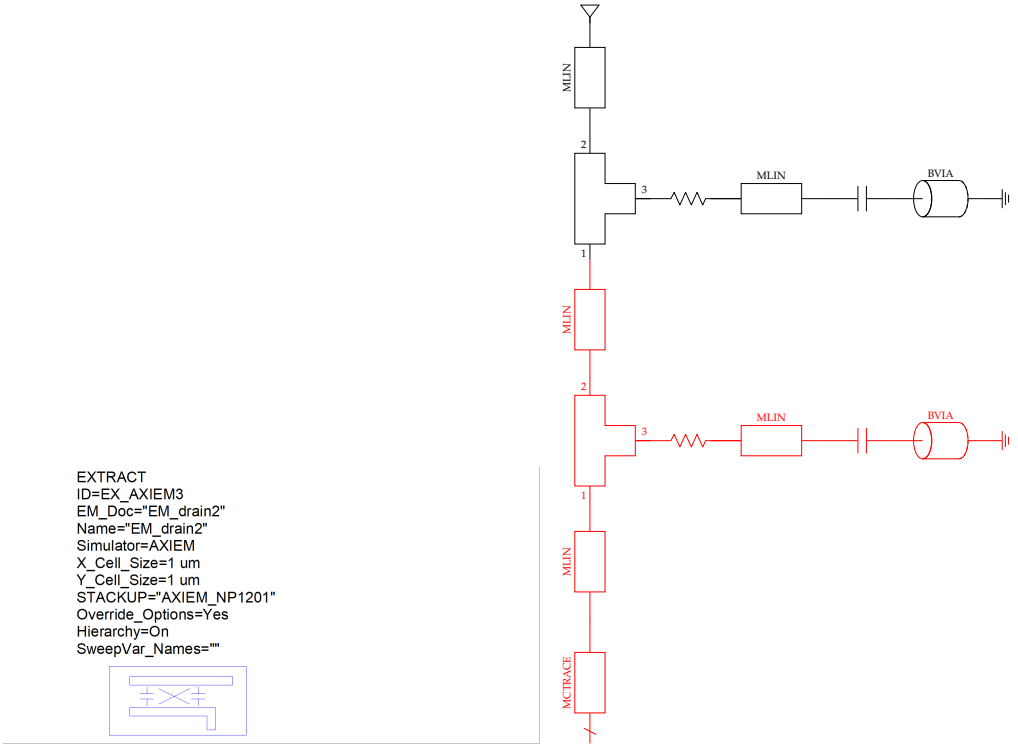



**Figure 4.12:** Iterative fine-tuning cycle of the power amplifier design process, consisting of simulation, result analysis, tuning, layout adjustments and EM simulations

**Electromagnetic Simulation**

To efficiently incorporate the electromagnetic effects into the design, the EM simulations were divided into two stages: partial EM simulation and full EM simulation. During the iterative refinement phase, discussed in Figure 4.2.2, partial EM simulations were used as shown in Figure 4.13.

In this approach, each matching network is subdivided into 2 to 5 EM blocks. Within each block elements are grouped based on proximity, grouping areas where coupling and parasitic effects are most likely to occur. Figure 4.13b shows this approach, with the red-highlighted components representing an example of one EM block.




**(a)** Example EM block in schematics **(b)** Example components in one EM block

**Figure 4.13:** EM where the schematics are directly connected to EM

During the iterative design loop (Figure 4.12) EM block were activated one at a time to evaluate their individual impact. This method simplifies the tuning process. As shown in Figure 4.14, enabling a single EM block initially allows for a more precise adjustment to try to get the performance back to the schematics results.
In the layout phase, Figure 4.2.2, transmission lines are often meandered to fit within the available layout area while preserving their desired electrical length. However, such bends add capacitance at the corners, effectively shortening the effective length of the line. To compensate for this line lengths often need to be increased slightly.

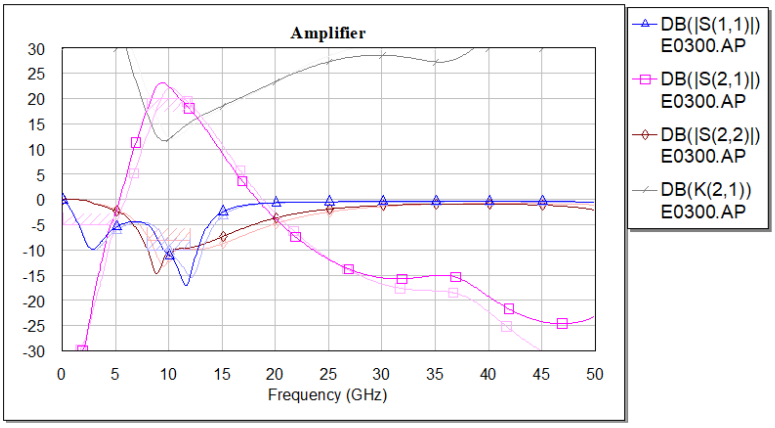



**Figure 4.14:** Example of S-parameter variation before and after electromagnetic (EM) simulation

A practical rule of thumb is that if components are spaced more that the substrate height (50 $\mu$m) apart,

their mutual coupling becomes negligible. Therefore, elements placed closer to each other should be included within the same EM block to accurately capture their interaction.
Once all the partial EM results have been compensated for and the overall circuit performance is restored, a full EM simulation of the entire layout is performed, excluding the transistors Figure 4.15. This simulation is done in several configurations to evaluate the impact of the layout boundaries and port definitions.

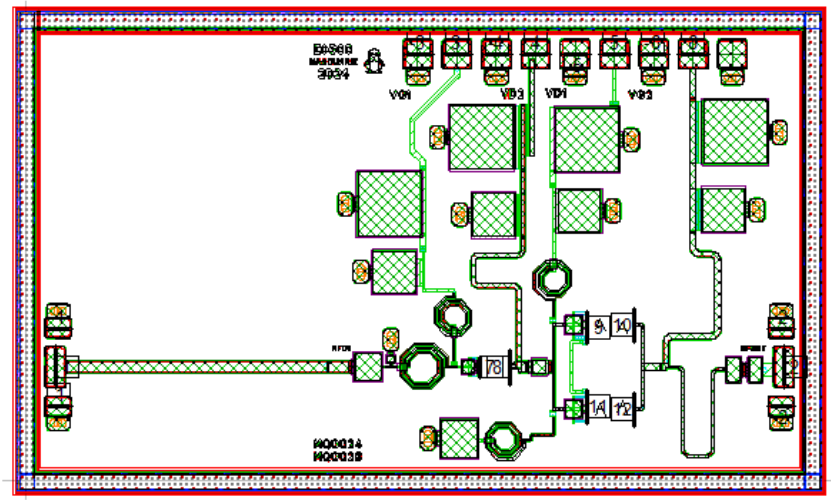
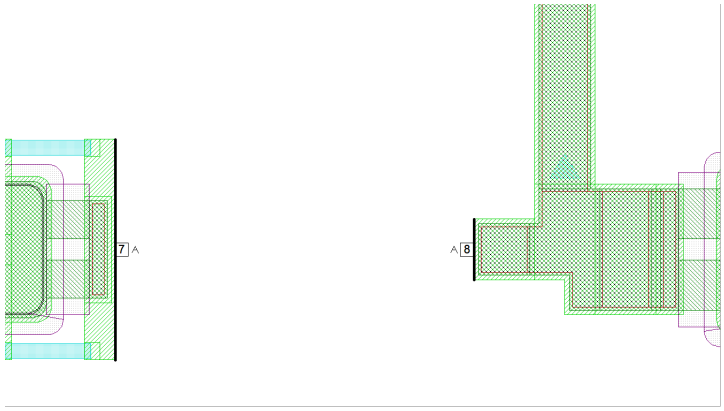



**Figure 4.15:** Electromagnetic (EM) simulation model of the complete circuit excluding active transistors

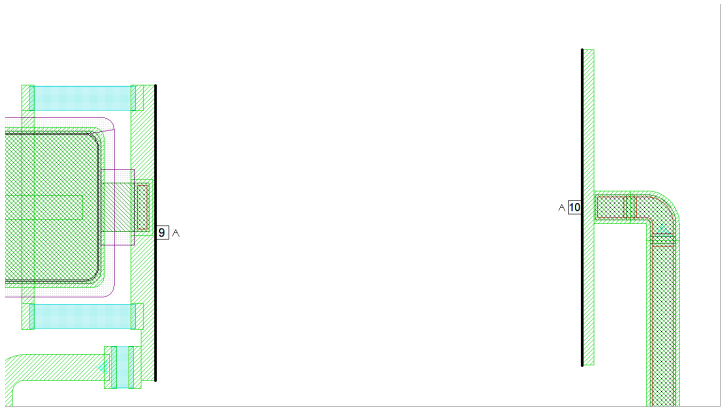
The full simulation was repeated under multiple boundry conditions:

- Entire chip including ring and pads
- Chip without the ring
- Chip without the ring and pads
- Chip with simple ports
- Chip with extended metal 1 lines to replicate realistic port coupling conditions

Figure 4.16a and Figure 4.16b show the difference between transistor EM block with and without extended metal lines. These additional lines help approximate the real connection environment with the amplifier and better capture coupling effects at the in- and output ports.




**(a)** EM simulation of transistor block without extended metal lines




**(b)** EM simulation of transistor block with extended metal lines

**Figure 4.16:** Comparison of port definition strategies in EM simulations

### Stability and Sensitivity Checks

Beyond the standard performance metrics, such as output power ($P_{out}$), power-added effiency (PAE) and S-parameters and K-factor, several additional checks are conducted to ensure the amplifier meets stability and robustness requirements.

The first of these is the gate resistance check. Gate resistors are incorporated into the design to enhance stability by absorbing potential fluctuations (item [2.4.3]). However, excessive resistance in the gate path can cause an undesirable voltage drop which degrade circuit performance. To avoid this, the total resistance in the gate line is evaluated against the maximum allowable value given by Equation 4.4 [24].

$$R_{G_{max}} = \frac{200}{\frac{\text{number of gate fingers} \cdot \text{width fingers}}{1000}} \tag{4.4}$$

Following the gate resistance verification, bias and impedance sensitivity analyses are performed. These involve sweeping the drain voltage, gate voltage and source/load impedances to evaluate the circuit's sensitivity to variations in external conditions and bias conditions. If significant performance changes are observed during these sweeps, further tuning is necessary to improve the robustness of the design (item [2.3.1.6]).

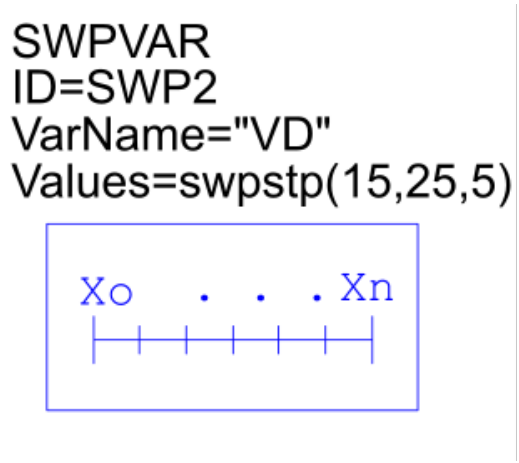



**Figure 4.17:** Schematic setup for gate and drain voltage sweep

Afterwards, drain voltage, gate voltage and impedance sweeps are done to check the sensitivity of the circuit to the outside world and different bias conditions with the structure seen in Figure 4.17 and Figure 4.18. For the voltages sweep, Figure 4.17 the variable $V_D$ or $V_G$ are filled into the supplies at the schematics and then the simulation is ran to see the result. For the impedance the structure seen in Figure 4.18 is added to all the connections at the source and again the simulation is ran. If the performance changes a lot the circuit should be tuned again to help it be more rebuts (item [2.3.1.6]).

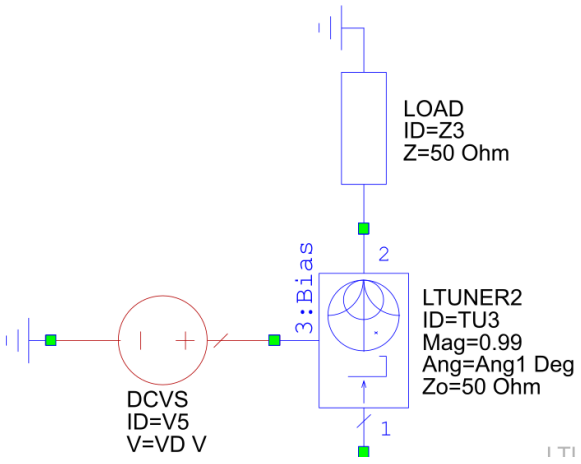



**Figure 4.18:** Schematic setup for impedance sweep

In the design phase bias supplies are typically kept separate to maintain maximum control over each stage of the amplifier. However, when integrated into a complete system, these supplies are often tied together for practical implementation. This can introduce bias loops, which affect stability that can't be seen in the K-factor. Therefore, Ohtomo stability analysis is carried out (Figure 4.19). As well to confirm the unconditional stability of the second-stage transistors under all operating conditions, as is discussed in subsection 3.9.2.

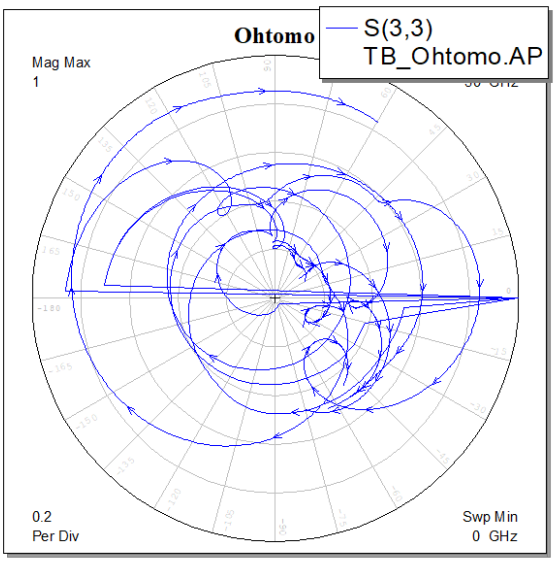



**Figure 4.19:** Ohtomo stability analysis

### Design Rule Check

At last the Design Rule check is done, Table 4.2 shows a couple of the design rules of the different metals.

| Material | Description | Dimension ($\mu$m) |
|---|---|---|
| Ohmic | Minimum width | 5 |
| | Minimum spacing between Ohmic | 2.5 |
| MET1 | Minimum width | 5 |
| | Minimum spacing between MET1 | 5 |
| MET2 | Minimum width out of active region | 6 |
| | Minimum spacing between MET2 | 5 |
| Backvia | Backvia diameter | 30x60 |
| | Minimum spacing between Backvia | 65 |
| | VIA1, MET1, VIA2, MET2 must be present on Backside Via | - |
| | Minimum spacing between Ohmic | 10 |

**Table 4.2:** Examples Layout Design Rules NP12-01 WIN Semiconductors [22]

### Connectivity Check

Just before submitting the design to the foundry a connectivity check is done as a final verification step. In this process, each element in the circuit is systematically selected to confirm that all intended connections are present, no unintended shorts exist and no accidental gaps are present between the metals. This is done for every part of the circuit, step-by-step as can be seen in Figure 4.20.

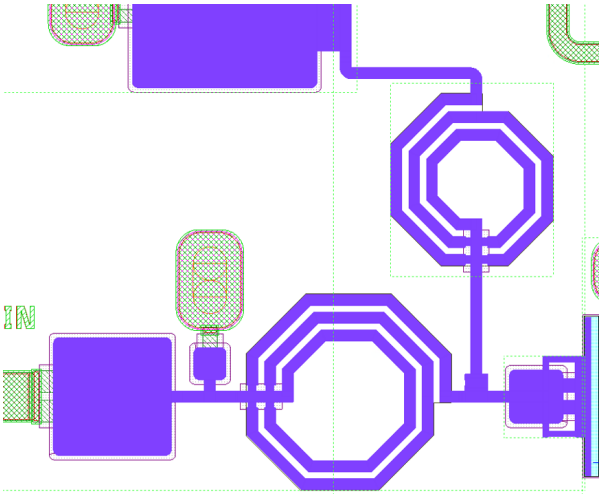



**Figure 4.20:** Connectivity check in parts

## 4.3. Simulation Results

This section presents the simulated performance of the E0300 and its variant E0302 under nominal bias conditions of $V_{DS}$ of 20 V, first stage drain current of 40 mA and second stage drain current of 180 mA for the E0300 and 220 for E0302. The analysis is devided into two parts: small-signals S-parameter and large-signal performance analysis.

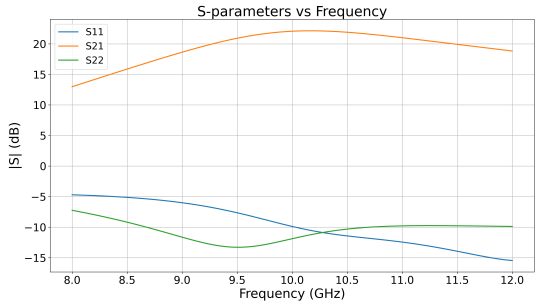
### 4.3.1. S-Parameters

The simulated S-parameters for both the E0300 and E0302 designs are compared to the requirements in the subsections below. At the target operating frequency of 10 GHz (item [2.3.1.1]).

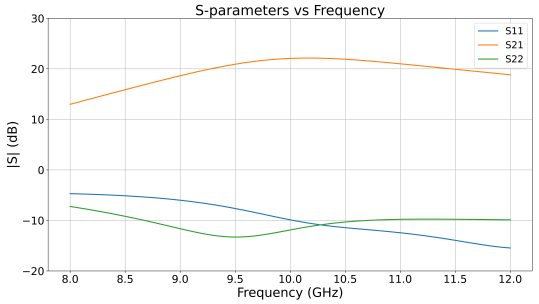
#### E0300: X-band Power Amplifier

The input reflection coefficient ($S_{11}$) remains below -10 dB at the design frequency (item [2.3.1.5]), demonstrating effective input matching and minimal reflected power. The zoomed-in plot (Figure 4.21a) show smooth performance across the 8-12 GHz band, with output reflection ($S_{22}$) also remaining low, confirming good output matching.

Broadband simulations (Figure 4.21b) illustrate the device's response from 0 to 50 GHz, showing all the lines are smooth up to the higher-end frequencies.




**(a)** Zoomed-in view of the S-parameters between 8 and 12 GHz, showing detailed performance around the band of interest



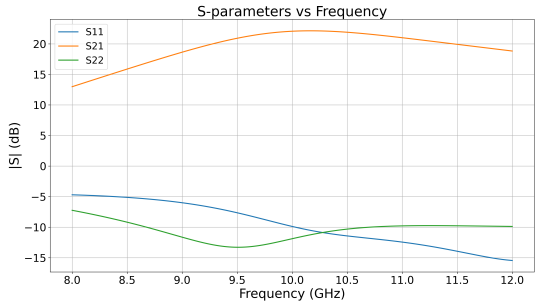

**(b)** Full broadband simulated S-parameters response from 0 to 50 GHz, illustrating overall device behaviour across the full frequency span.

**Figure 4.21:** Simulated S-parameters (S11, S21, S22) of one instance of the E0300 chip measured under nominal bias conditions

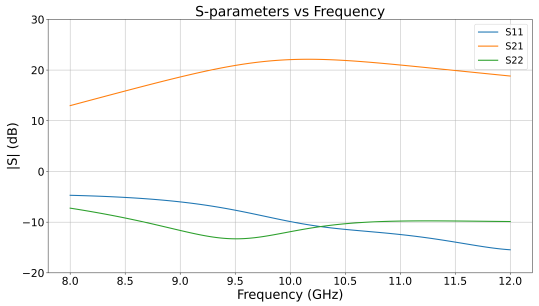
#### E0302: E0300 with Alternative Transistor

The simulated S-parameter results of the E0302 design exhibits a strong resemblance to those obtained for the E0300, as shown in Figure 4.21. In the broadband response of Figure 4.22b a minor deviation is

observed around 4 GHz, where the input reflection coefficient ($S_{11}$) shows a slight peak at approximately 1 dB. This peak is neither pronounced enough in magnitude nor sharp enough in bandwidth to raise concerns regarding stability or performance. Across the intented operating band, the small-signal forward gain ($S_{21}$) remains consistently above 20 dB, thereby fulfilling the gain expectations for the application.




**(a)** Zoomed-in view of the simulated S-parameters between 8 and 12 GHz, showing detailed performance around the band of interest




**(b)** Full broadband simulated S-parameters response from 0 to 50 GHz, illustrating overall device behavior across the full frequency span.

**Figure 4.22:** Simulated S-parameters (S11, S21, S22) and K-factor of one instance of the E0302 chip measured under nominal bias conditions

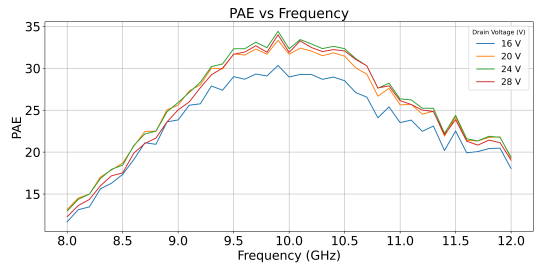
### 4.3.2. Power

These simulations are done under the same bias conditions as the s-parameters simulations.

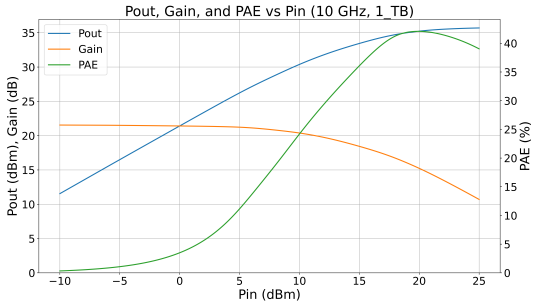
#### E0300: X-band Power Amplifier

The large-signal simulation results for the E0300 design, presented in Figure 4.23 demonstrate compliance with the defined performance targets in chapter 2. At the nominal operating frequency of 10 GHz (item [2.3.1.1]), the output power ($P_{out}$) reaches a maximum of approximately 35 dBm, just below the specifications of item [2.3.1.2]. The corresponding power-added efficiency (PAE) peaks at around 45 %, meeting the PAE requirement item [2.3.1.4].

The power gain remains above the minimum threshold of 10 dB across the operating band (item [2.3.1.3]), it is even surpassing 15 dB.




**(a)** Simulated Pout, Gain, and PAE vs Frequency for E0300 at Pin is 20 dBm



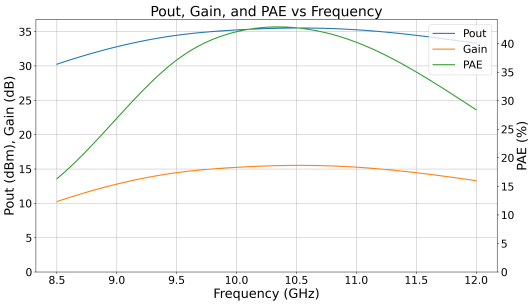

**(b)** Simulated Pout, Gain, and PAE vs Input Power for E0300 at 10 GHz

**Figure 4.23:** Simulated RF Performance of E0300: Pout, Gain, and PAE vs Frequency and Input Power

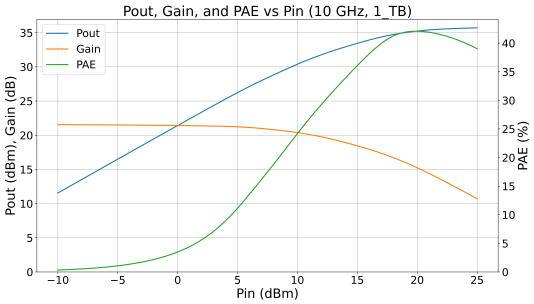
#### E0302: E0300 with Alternative Transistor

The E0302 configuration, shown in Figure 4.24, exhibits similar performance trens, with $P_out$ also achieving approximately 35 dBm at 10 GHz. The output power is a little higher than seen in Figure 4.23, by around 0.2 dBm. The gain characteristic mirrors that of the E0300, again meeting the specifications outlined in item [2.3.1.3]. This demonstrates that the alternative transistor technology is capable of meeting the same large-signal performance requirements while retaining comparable efficiency. The

one difference is that the E0302 compresses a bit later then the E0300, this can be seen at the roll-over of the PAE and the saturation of the output power is at a higher input power then the E0300.




**(a)** Simulated Pout, Gain, and PAE vs Frequency for E0302 at Pin is 20 dBm




**(b)** Simulated Pout, Gain, and PAE vs Input Power for E0302 at 10 GHz

**Figure 4.24:** Simulated RF Performance of E0302: Pout, Gain, and PAE vs Frequency and Input Power

# 5

# Fabrication

The design created in chapter 4 is manufactured by WIN Semiconductors Corp. This chapter describes that process, including the design of the pad ring required for on-chip measurements, together with pictures of the fabricated MMICs.

## 5.1. Probe Pad Layout

Special structures need to be included around the chip to be able to measure its microwave performance. They are called the probe pads. These structures facilitate the probing of the MMIC, very small needles are pushed onto the metal pads to contact the circuit. These pads have three functions:

- Providing the electrical ground (zero potential), connecting to the back of the wafer through via holes (ground pads).
- Providing the DC voltages to the transistors so that they can be biased at the right bias point (DC pads).
- Providing the microwave interconnections (RF pads).

The same pads can be used at a later moment to bond tiny gold wires from the chip to the electrical contacts of the chip package (if the chip is packaged). The size of all pads is the same (100x100 $\mu m^2$). This size is big enough that they can accommodate the needles and small enough to not take too much space.

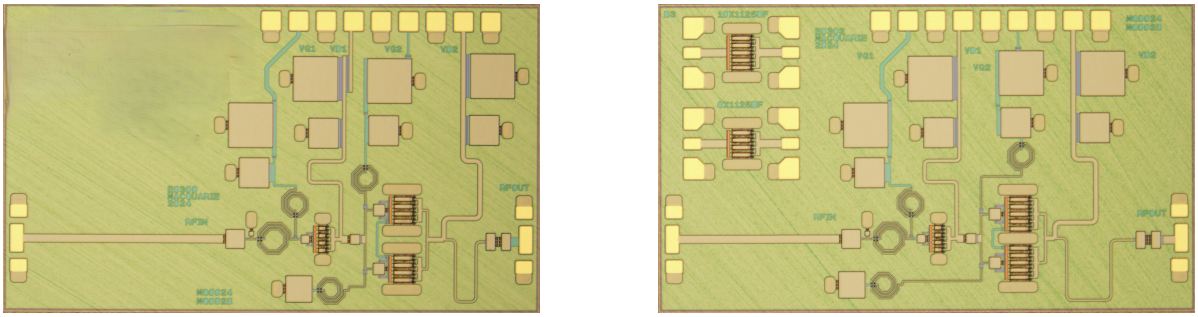
The RF pads are on the input- and output side of the chip, all the DC pads are on the top and bottom of the chip. Around the chip an empty ring where no components can be placed. This is the 'scribe area', that is used to cut the chips into separate components. The position of the pads and the scribe area can be found in Figure 6.1. The function of the pads is indicated with text in the figure as well.

## 5.2. Manufacturing

The designed MMIC is exported from the design software into a GDSII file. This GDSII file encodes the entire layout. Coupling the designed layout to the mask layers that the manufacturer will use to fabricate the circuit.
The layout was submitted to WIN Semiconductors Corp. at the end of December 2024, together with other designs from MAD Lab and a quarter-wafer, in diced condition, was received back on film at the start of May 2025.

Upon receipt of the fabricated samples, an initial visual inspection was conducted using an optical microscope to verify the absence of mechanical defects or fabrication abnormalities. No defects were observed and high-resolution photographs of the MMICs were taken, as shown in Figure 5.1. The reflective gold region correspond to the probe pads, which appear highly polished due to the absence of

a protective passivation layer. In contrast, all the other gold metallisation layers are covered by this protective coating.



**(a)** E0300 **(b)** E0302

**Figure 5.1:** High-magnification microscope images of the fabricated MMICs after delivery from the foundry

In Figure 5.2 a magnified view of a single transistor is presented, where the individual device elements can be clearly distinguished: the yellow region is the gate metals, the purple are the resistors and green-greyish colour is the thick gold layer.

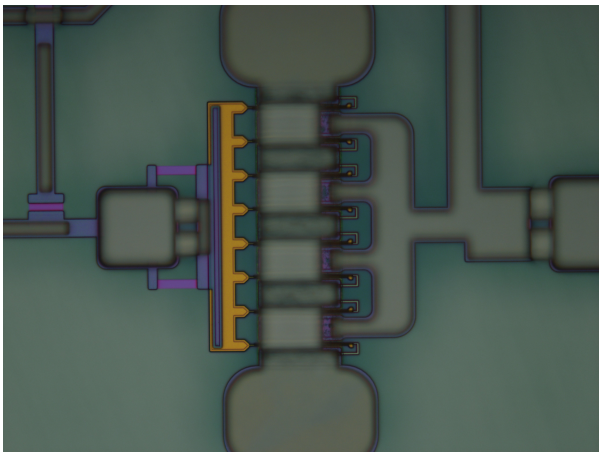


**Figure 5.2:** Microscope image of a single transistor, showing the gate metallization (yellow), resistors (purple), and thick gold interconnects (green-grey)

In Figure 5.3, shows the imperfections of the fabrications on the edge. Because this chip was made at the edge of the wafer, you can see edge-processing effects. The outer 2 mm of the wafer cannot be used for working circuits because the manufacturing is less accurate there.

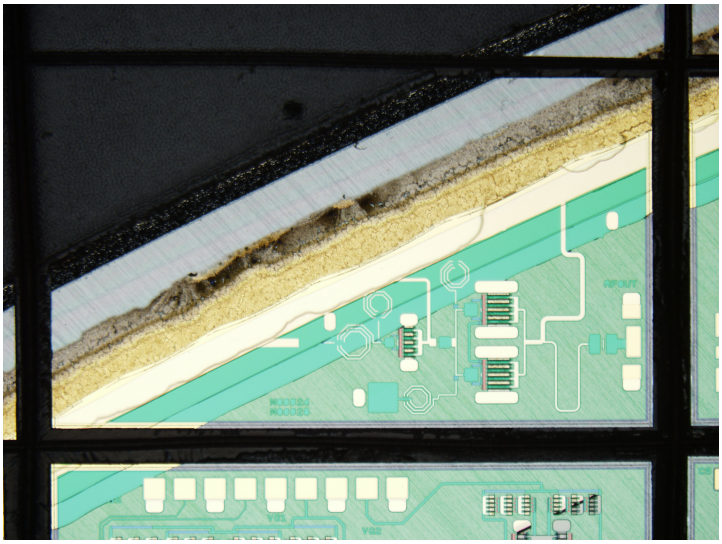


**Figure 5.3:** Microscope image of an MMIC fabricated at the wafer edge, showing imperfections

# 6

# Measurement Setup

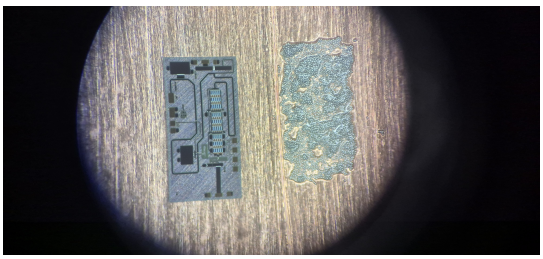
The MMICs that resulted from the manufacturing phase will be extensively characterized. This chapter describes the measurement setup, together with the limits of the setup.

## 6.1. Mounting MMICs

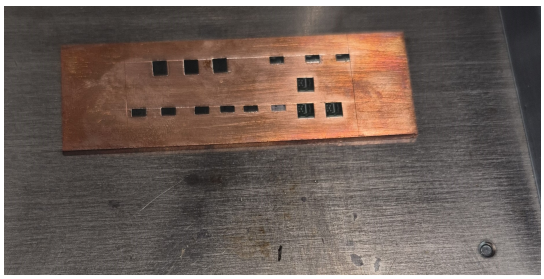
The quarter wafer returned from the foundry was diced and mounted on sticky film. For the measurements, each chip required proper heat sink to dissipate the heat generated by the limited efficiency of the power amplifier [25].

For this, a copper block was prepared. Copper is an excellent thermal conductor with a thermal conductivity of 5.8 x $10^7$ S/m [7]. The chips were then hand-picked and soldered onto the copper. A step-by-step MMIC mounting procedure was documented as a tutorial to assist future engineers in performing this task (Figure 6.1).

In Figure 6.1a, a microscope zoom is shown of an MMIC placed next to the applied solder paste prior to soldering. Figure 6.1b presents the completed copper block with all MMICs.



**(a)** Applying solder with dimensions matching the chip footprint



**(b)** Copper block with all chips mounted on copper block

**Figure 6.1:** Mounting chips on copper block

## 6.2. S-Parameters measurement setup

A standard measurement setup was emplyed for determining the scattering parameters utilizing an Keysight PNA-X vector network analyser (VNA), shown in Figure 6.2. The network analyzer connects to the input and output of the DUT and through its internal switching is able to measure all four S-parameters ($S_{11}$, $S_{12}$, $S_{21}$ and $S_{22}$) without the need for cable reconnections.

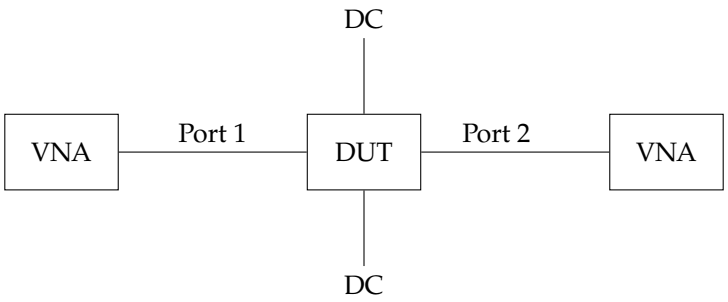



**Figure 6.2:** Setup scattering parameter measurement

## 6.3. Power measurement setup

The scattering parameter measurement setup offers high accuracy for small-signal characterization. However, it is not suitable for non-linear measurements. To fully characterize the power amplifier, additional large-signal measurements are required to determine both the absolute output power and the power-added efficiency (PAE).

A dedicated measurement setup was constructed specifically for this device, as the target frequency range and output power level impose strict requirements on what the laboratory equipment can handle. The measurement configuration shown in Figure 6.3. From left to right, a signal generator provides the input signal and is followed by a driver amplifier. This driver amplifier ensures that the right input power level can be delivered to the Device-Under-Test (DUT). The input power level is then partially coupled out to make accurate input power level measurements. The power is then provided to the DUT, which is embedded by two bias tees that are not needed (as there are also bias blocking capacitors on the MMIC) but provide an extra protection for the measurement equipment. After an attenuator, the output power is measured. The most important specifications for the measurement equipment are summarized in Table 6.1.

One problem occurred during the measurements resulted in less accurate, 'noisy', measurements. After a lot of trial and error it turned out that the input and output matching of one of the bias tees was insufficient and needed to be replaced.

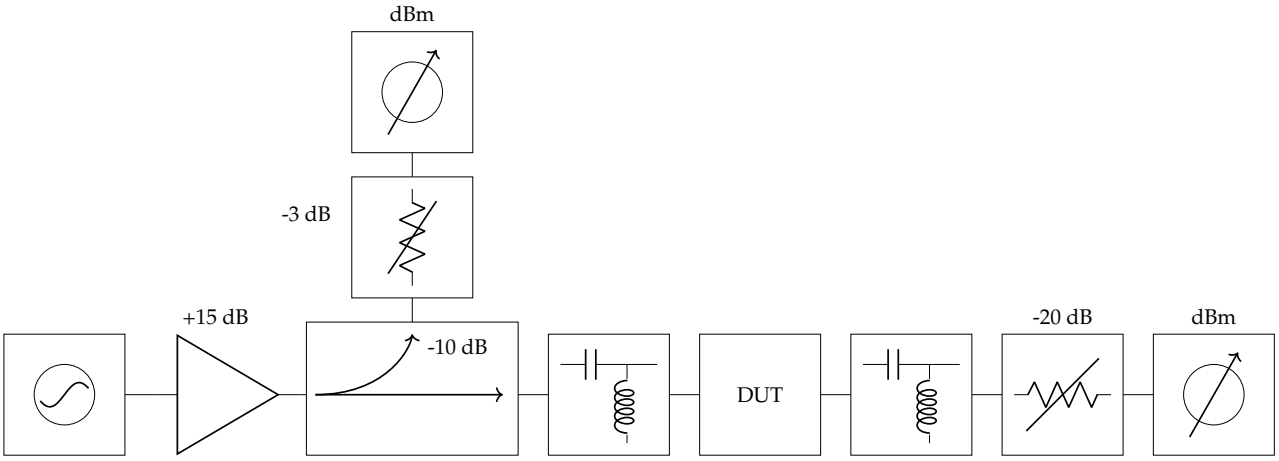



**Figure 6.3:** Setup large-signal measurement

| Equipment | Model | Frequency Range | Power Range |
|---|---|---|---|
| Signal Generator (SG) | Rohde & Schwarz SMA100B | 1-40 GHz | -80 - 20 dBm |
| Driver Amplifier (DA) | In house development | 2-18 GHz | 42dBm max |
| Directional Coupler (RFDC) | Fairview Microwave FM2CP1129-10 | 6-26 GHz | 45dBm |
| Attenuator Top (AT) | Mini-Circuits BW-K3-2W44+ | 0 - 40GHz | 33dBm |
| Power Meter Top (PMT) | Keysight N1912A | 50MHz - 40GHz | -40 - 20 dBm |
| Bias Tee 1 (BT1) | Auriga BT1026-10 | 1 - 26.5GHz | 40dBm |
| Device Under Test (DUT) | - | - | - |
| Bias Tee 2 (BT2) | Auriga BT1018-50-P | 1 - 18GHz | 47dBm |
| Bias Tee 3 (BT2) | Auriga BT1018-50-P | 1 - 18GHz | 47dBm |
| Attenuator Bottom 1 (AB1) | Pasternack PE7363-20 | 0 - 18GHz | 44dBm |
| Attenuator Bottom 2 (AB2) | Pasternack PE7363-20 | 0 - 18GHz | 44dBm |
| Power Meter Bottom (PMB) | Keysight N1912A | 50MHz - 40GHz | -40 - 20 dBm |

**Table 6.1:** Performance Limits of Measurement Setup Components

The bias supplies used to power the DUT are shown in Table 6.2. These include independent sources for the drain and gate voltages of each stage, allowing precise control of the operating conditions during testing.

| Equipment | Model |
|---|---|
| Gate Supplies | Keysight N6784A |
| Drain Supplies | Keysight N6751A |
| Switch Supplies | Keysight B2902A |

**Table 6.2:** Bias supplies

## 6.4. Calibration

Calibration of microwave measurements is critical and difficult. Due to the high frequencies every little disturbance in the microwave measurement path causes inaccuracies. For example, the exact layout of the probe-pad, the influence of RF probes and the force which microwave connectors are tightened all affect the accuracy of the measurements. This problem is usually solved by fixing the measurement setup and then measuring known standards, both for linear and non-linear measurement setups. This is a laborious work that involves probing multiple standards. Common reference standard choices are through-reflect-line standards (TRL calibration) and short-open-load-through standards (SOLT calibration) [26].

Some modern vector network analysers have an automated way to calibrate, using eCAL (electronic calibration) standards, where the changing of standards is automated and does not need reconnecting to standards. This method still requires for example SOLT standards, but they are now inside the eCAL module.

In this report, the reference plane is after the probe-pads (at the side of the chip). Accurate SOLT standards were on the wafer and eCAL calibration is useful mainly for a connector reference-plane. That's why SOLT calibration was chosen.

# 7

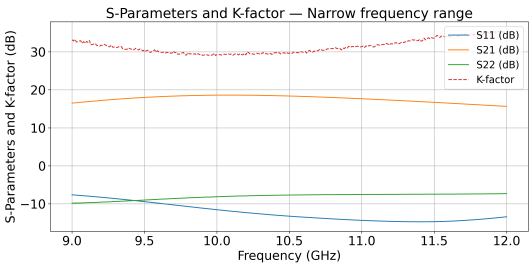
# Measurement Results

This chapter presents the measurements on the MMICs manufactured as described in chapter 5. The measurements are performed with the setups described in chapter 6. Both linear (S-parameters) and non-linear measurements (power measurements) are discussed, for both the baseline design (E0300) and the design with alternative transistors (E0300).

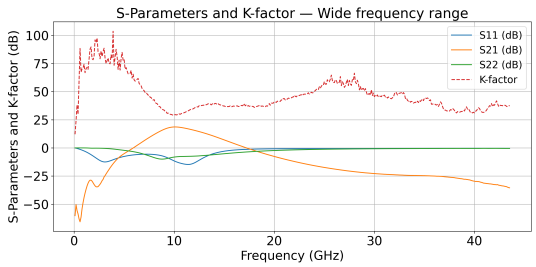
## 7.1. S-Parameters

### 7.1.1. E0300: X-band Power Amplifier

Figure 7.1 presents the measured S-parameters ($S_{11}$, $S_{21}$, $S_{22}$) and the stability factor (K-factor) of the E0300 X-band power amplifier. The left plot, Figure 7.1a shows a zoomed-in view of the frequency range between 9 and 12 GHz, corresponding to the target operating band. This detailed view highlights the in-band performance, including gain, input matching and stability margin. The right plot, Figure 7.1b displays the broadband response from 0 to 43.5 GHz. This wider frequency sweep is performed to verify unconditional stability across the entire accessible spectrum ensuring no risk of oscillation at out-of-band frequencies. In both cases, the K-factor remains well above zero, satisfying the stability requirement defined in item [2.4.3].




**(a)** Zoomed-in view of the S-parameters and K-factor between 9 and 12 GHz, showing detailed performance around the band of interest



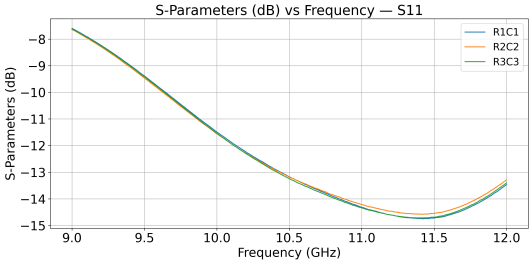

**(b)** Full broadband S-parameters and K-factor response from 0 to 43.5 GHz, illustrating overall device behavior across the full frequency span.

**Figure 7.1:** Measured S-parameters (S11, S21, S22) and K-factor of one instance of the E0300 chip measured under nominal bias conditions

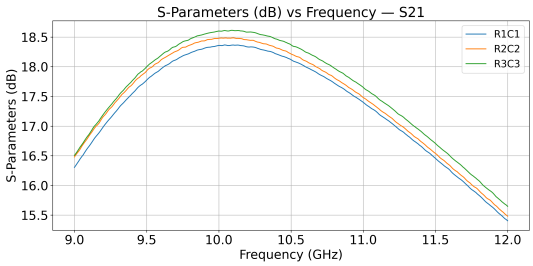
Figure 7.2 presents a comparison of three separate instances of the E0300 X-band power amplifier (R1C1, R2C2, R3C3), all measured under nominal bias conditions: 40 mA for $I_{d1}$, 180 mA for $I_{d2}$ and 20 V $V_{ds}$. The intent of this comparison is to assess the consistency of the fabrication process, as well as the robustness of the design to process variations.

The measured input reflection coefficient ($S_{11}$), shown in Figure 7.2a, demonstrates close agreement among the three instances. With the minimum near -11.5 dB at 10 GHz. Similarly, the measured

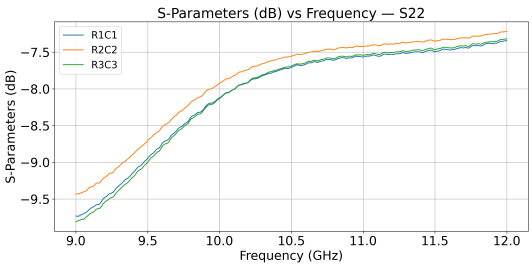
small-signal gain ($S_{21}$) in Figure 7.2b exhibits consistent performance, peaking at approximately 18.5 dB at near 10 GHz.



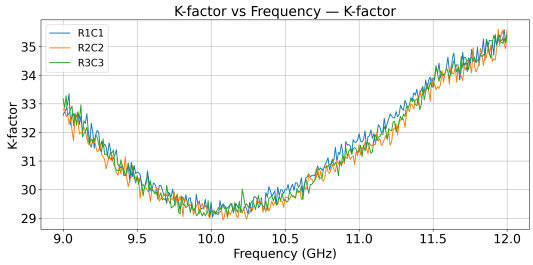

**(a)** Measured input reflection coefficient (S11) for all three chip samples




**(b)** Measured small-signal gain (S21) for all three chip samples

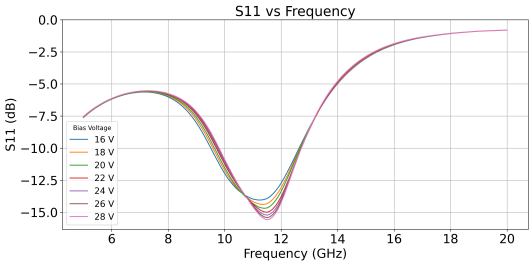



**(c)** Measured output reflection coefficient (S22) for all three chip samples

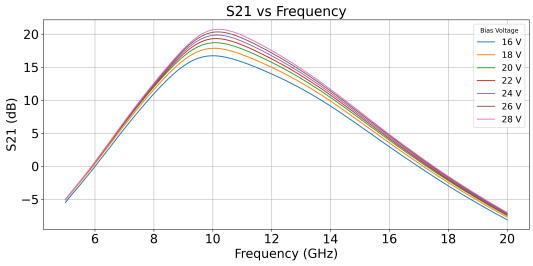



**(d)** Measured stability factor (K) for all three chip samples

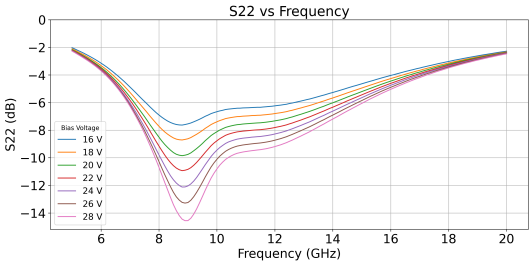
**Figure 7.2:** Comparison of measured S-parameters and K-factor for three instances of the E0300 chip across 9-12 GHz under nominal bias conditions



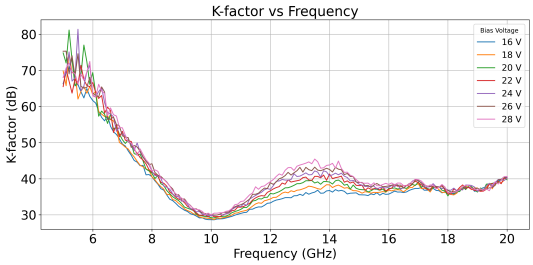

**(a)** Measured input reflection (S11) under drain voltage sweep




**(b)** Measured small-signal gain (S21) under drain voltage sweep




**(c)** Measured output reflection (S22) under drain voltage sweep



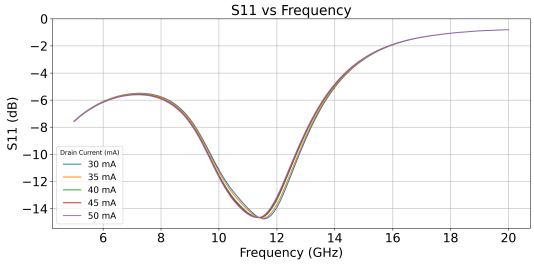

**(d)** Measured stability factor (K) under drain voltage sweep

**Figure 7.3:** Measured S-parameters and K-factor of the E0300 chip under drain voltage sweep of the two stages tied together from 16 $V$ to 28 $V$ in 4 $V$ steps

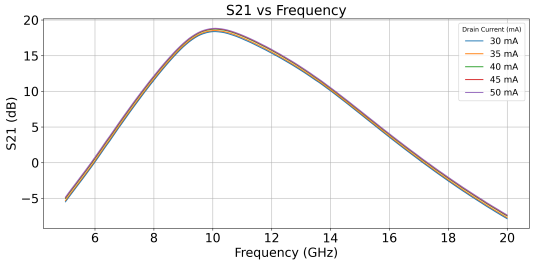
Figure 7.3 shows the S-parameters and stability factor (K-factor) of the E0300 power amplifier under a drain voltage sweep of the two stages tied together, ranging from 16 V to 28 V in 4 V increments. The nominal supply operating voltage was selected as 20 V at the drain bias (item [2.3.2.1]), which represents a safe and reliable operating point within the process specifications. While the sweep was extended up to 28 V for characterization purposes, this is the maximum voltage allowed by the NP12-01 GaN

process and designing at the edge of this limit would be considered risky from a reliability standpoint (item [2.4.3]).

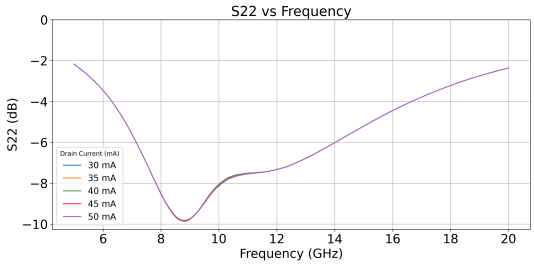
The measured $S_{21}$, representing the small-signal gain, increases with higher drain bias voltages. Similarly, $S_{22}$, the output reflection coefficient, improves as the drain voltage is increased.
The input reflection coefficient $S_{11}$ also decreases in magnitude with increasing voltage. However, its shifts from being centered around 10.5 GHz towards above 11.5 GHz. This frequency shift is not ideal, as the power amplifier is designed for operation around 10 GHz (item [2.3.1.1]). Nevertheless, at 10 GHz the value of $S_{11}$ remains below -10 dB, thereby meeting the functional requirement specified in item [2.3.1.5].



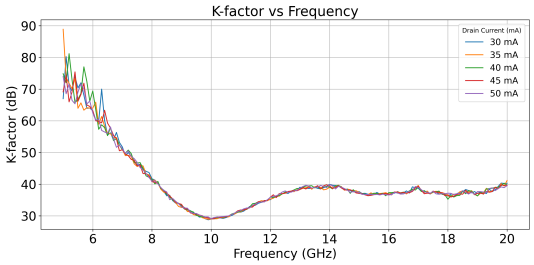

**(a)** Measured input reflection coefficient (S11) under first stage drain current sweep




**(b)** Measured small-signal gain (S21) under first stage drain current sweep



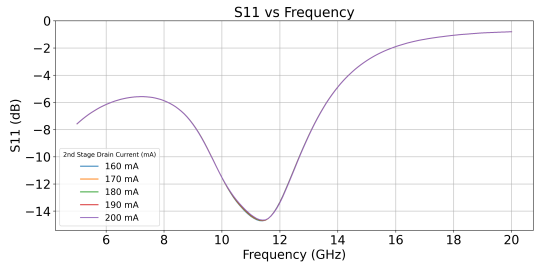

**(c)** Measured output reflection coefficient (S22) under first stage drain current sweep



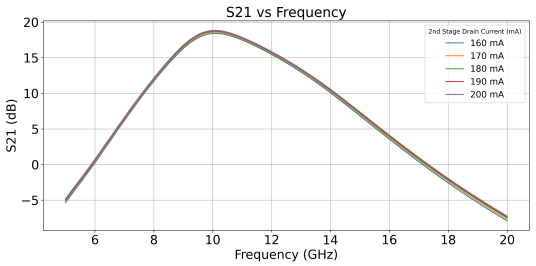

**(d)** Measured stability factor (K) under first stage drain current sweep

**Figure 7.4:** Measured S-parameters and K-factor of the E0300 chip under drain current sweep of the first stage transistor from 30 m$A$ to 50 m$A$ in 5 m$A$ steps

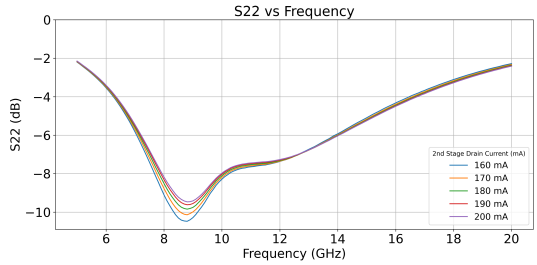
In Figure 7.4 and Figure 7.5 the results are presented of the E0300 chip under drain current sweeps for the first and second stage transistors respectively. For the first stage (Figure 7.4), the drain current is varied from 30 mA to 50 mA in steps of 5 mA, while for the second stage (Figure 7.5) the drain current ranged from 160 mA to 200 mA in steps of 10 mA. In both cases variations in the drain current have only a marginal effect on all the S-parameters and the stability factor. The most notable change is observed in $S_{22}$, where higher drain currents slightly improve the output matching.



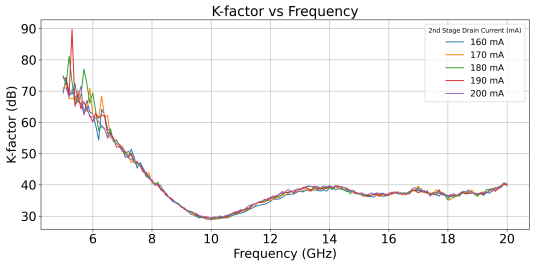

**(a)** Measured input reflection coefficient (S11) under second stage drain current sweep




**(b)** Measured small-signal gain (S21) under second stage drain current sweep




**(c)** Measured output reflection coefficient (S22) under second stage drain current sweep




**(d)** Measured stability factor (K) under second stage drain current sweep

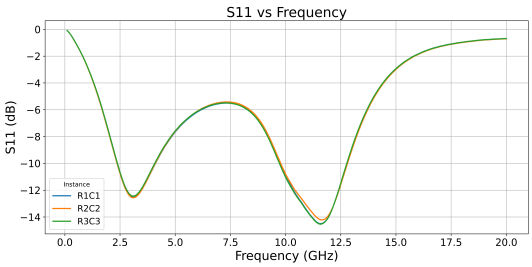
**Figure 7.5:** Measured S-parameters and K-factor of the E0300 chip under drain voltage sweep and drain current sweep of the second stage transistors from 160 m$A$ to 200 m$A$ in 10 m$A$ steps

### 7.1.2. E0302: E0300 with Alternative Transistor

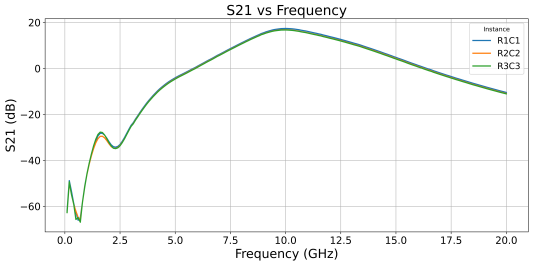
In the simulated analysis in subsection 4.3.1, it was observed that the S-parameters of the E0300 and E0302 chip where highly similar. Based on this observation, it was decided to extend the investigation by comparing the measured values of the two chips variants in order to identify and quantify any performance differences under real-world conditions.

Figure 7.6 presents the measured S-parameters and stability factor for three different samples of the E0302 chip, recorded over the 0-20 GHz frequency range at nominal bias conditions. The input reflection coefficient ($S_{11}$) in Figure 7.6a exhibits two minima, one around 3 GHz and another close to 11 GHz, both falling below the -10 dB threshold specified in item [2.3.1.5] at the design frequency of 10 GHz.

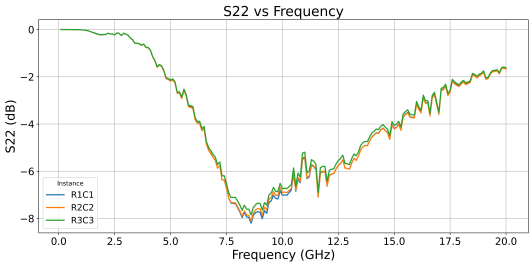
The output reflection coefficient ($S_{22}$) in Figure 7.6c remains below -5 dB over most of the band of interest, with its lowest value occurring near 9 GHz. Finally, the stability (K-factor) illustrated in Figure 7.6d remains well above zero across the full measured range. The close alignment between the three measured samples further supports the repeatability and robustness of the E0302 design and provides a solid basis for direct comparison with the measured performance of the E0300 chip.



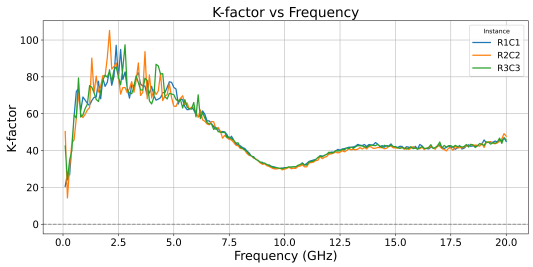

**(a)** Measured input reflection coefficient (S11) for all three chip samples




**(b)** Measured small-signal gain (S21) for all three chip samples




**(c)** Measured output reflection coefficient (S22) for all three chip samples




**(d)** Measured stability factor (K) for all three chip samples

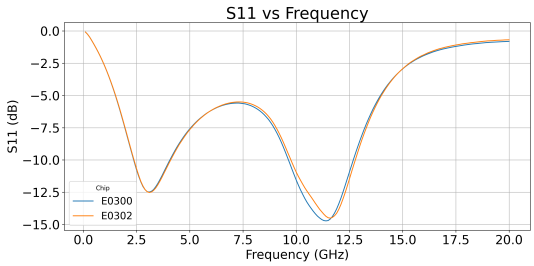
**Figure 7.6:** Comparison of measured S-parameters and K-factor for three instances of the E0302 chip across 0-20 GHz under nominal bias conditions

Figure 7.7 presents the measured input and output reflection coefficients, small-signal gain and stability factor for both designs over the 0-20 GHz range under nominal bias conditions.

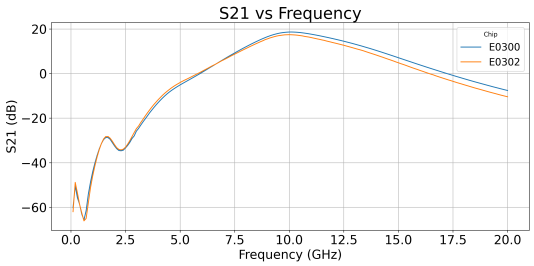
The input reflection coefficient ($S_{11}$), shown in Figure 7.7a, displays nearly identical behaviour for the two devices. The small-signal gain ($S_{21}$), Figure 7.7b, also follows a closely matched trend. E0300 demonstrates a slight better performance within the target frequency. However, the difference is not significant to conclusively favour one design over the other with just the gain.

For the output reflection coefficient ($S_{22}$) illustrated in Figure 7.7c, the E0302 shows slightly higher values beyond 12 GHz, though the difference remains small within the band of interest. The stability k-factor are indicating stability for both design with a significant margin from the 0 dB instability line.

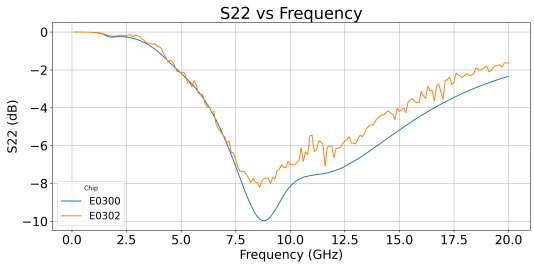
Overall, the measured data confirms that the E0300 and E0302 exhibit nearly identical RF performance across the examined small-signal metrics, validating the earlier simulation-based conclusion.



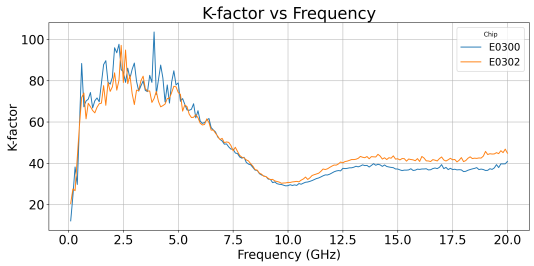

**(a)** Measured input reflection coefficient (S11)




**(b)** Measured small-signal gain (S21) for all three chip samples




**(c)** Measured output reflection coefficient (S22)




**(d)** Measured stability factor (K)

**Figure 7.7:** Comparison of measured S-parameters and K-factor for E0300 versus E0302 Chips across 0-20 GHz under nominal bias conditions

## 7.2. Power

The measured results in this section present the output ($P_{out}$), gain and power-added efficiency (PAE) of the fabricated amplifier under various operating conditions, evaluated against the requirements defined in item [2.3.1.1], item [2.3.1.2], item [2.3.1.3] and item [2.4.3].

### 7.2.1. E0300: X-band Power Amplifier

In Figure 7.8 the performance of three fabricated instances is plotted as $P_{out}$, gain and PAE versus input power. Across all devices the measured maximum $P_{out}$ approaches 36 dBm, while the gain remains well above the minimum threshold of 10 dB. The PAE peaks around 35% for all the instances, indicating consistent behaviour and good reproducibility. Minor differences between devices is expected due to manufacturing tolerances, but no device shows significantly different results.

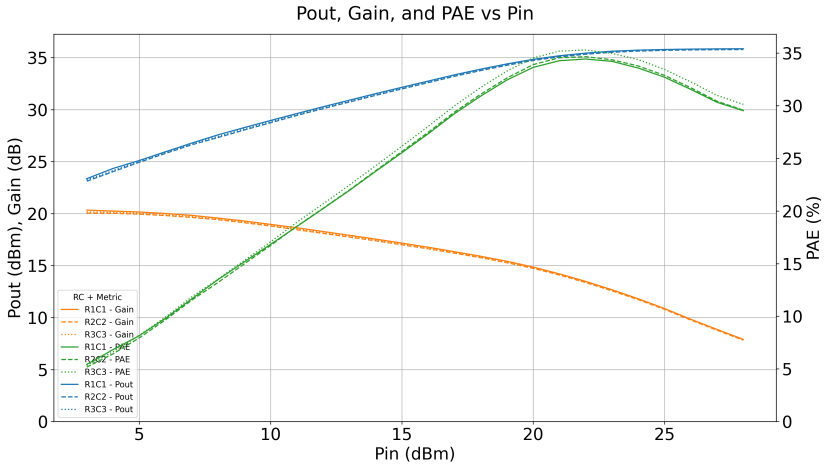



**Figure 7.8:** Measured $P_out$, gain and PAE versus input power for three E0300 instances at 10 GHz under nominal conditions

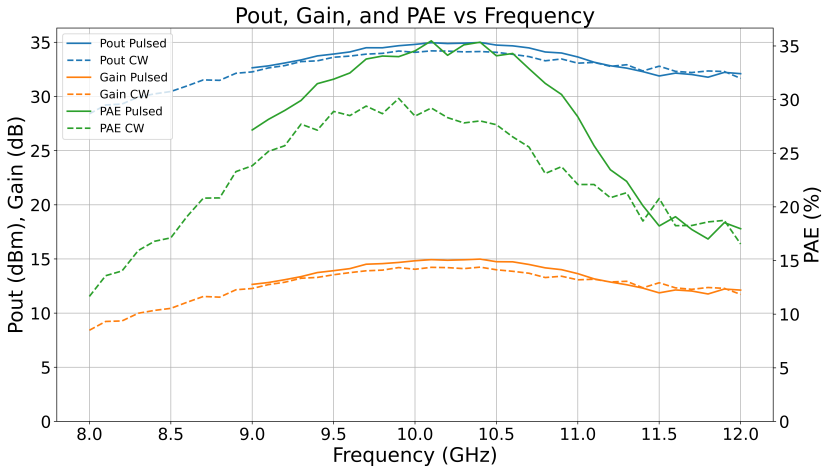



**Figure 7.9:** Measured $P_{out}$, gain and PAE versus frequency for pulsed and CW operation at 20 dBm input power

To investigate thermal effects, both pulsed and continuous-wave (CW) measurements were performed under identical conditions. In Figure 7.9 and Figure 7.10 the pulsed and continuous-wave (CW) measurement are plotted. At the design frequency of 10 GHz the difference in $P_{out}$ and gain are minimal: under 1 dB(m). PAE differs a bit more around 5%, this is expected as the warmth of the power amplifier effects the current. With the pulsed measurement the amplifier turns the amplifier on and off, that makes the overall temperature of the chip less and as a result the current doesn't increase as much as the continuous wave measurement.

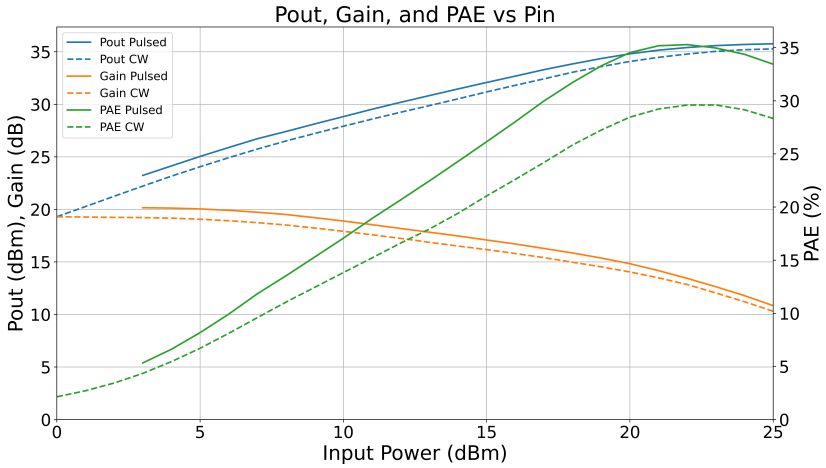
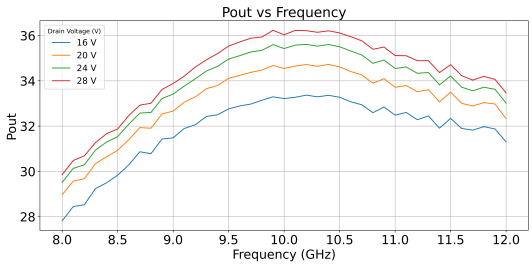
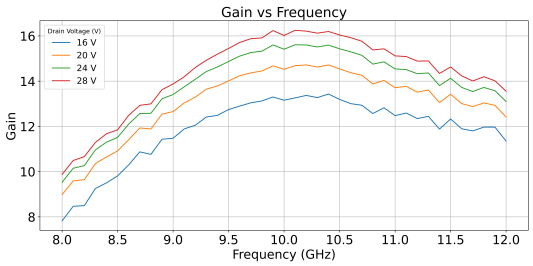



**Figure 7.10:** Measured $P_{out}$, gain and PAE versus input power for pulsed and CW operation at 10 GHz

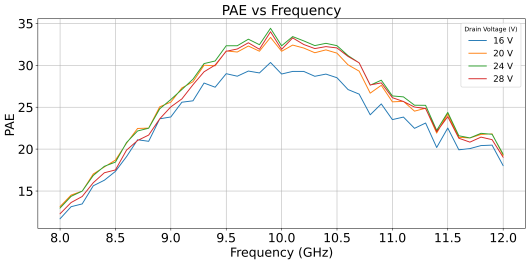
Figure 7.11a presents a zoomed-in view of the drain-voltage sweep, showing that higher drain voltage increases both $P_{out}$ and gain significantly. The PAE remains relatively constant across most drain-voltage values.




**(a)** $P_{out}$ versus frequency




**(b)** Gain versus frequency




**(c)** PAE versus frequency

**Figure 7.11:** Measured large-signal performance at varying drain voltages

### 7.2.2. E0302: E0300 with Alternative Transistor

For the E0302 chip, the measured large-signal performance is presented in Figure 7.12 and 7.13 for both pulsed and continuous-wave operation condition.

In Figure 7.12 again $P_{out}$, gain and PAE are plotted versus frequency for 20 dBm input power. Across 8-12 GHz band, $P_{out}$ remains above 30 dBm complying with requirement item [2.2.2]. Only not close to the desired power of 36 dBm. The gain is above 10 dB aligning with the target. The PAE peaks near 30% under pulsed conditions and is sightly lower in CW performance, due to self-heating effects as observed in the E0300 measurements.

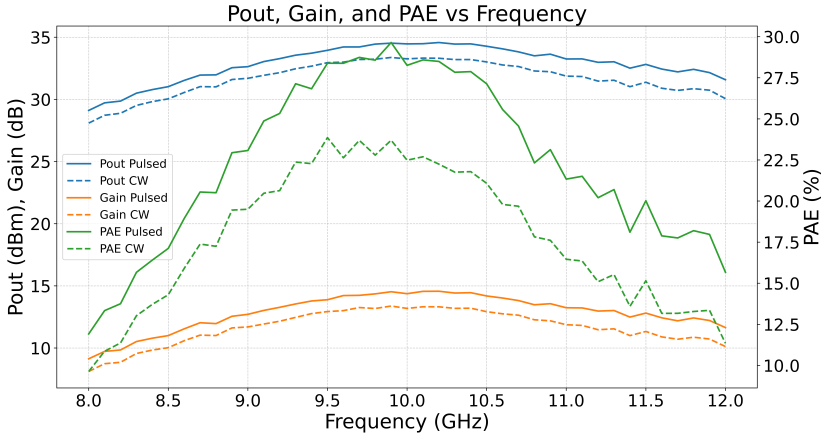



**Figure 7.12:** Measured output power, power gain, and PAE of the E0302 MMIC as a function of frequency at 20 dBm input power under CW and pulsed conditions

In Figure 7.13 the same parameters are plotted against input power at 10 GHz. For this graph, it could be determined that at higher input powers the PAE would be better. Getting closer to 35%. Overall, the E0302 achieves the mandatory requirement for output power (item [2.2.2]) and gain. While the PAE is a little below the requirement of 40%.

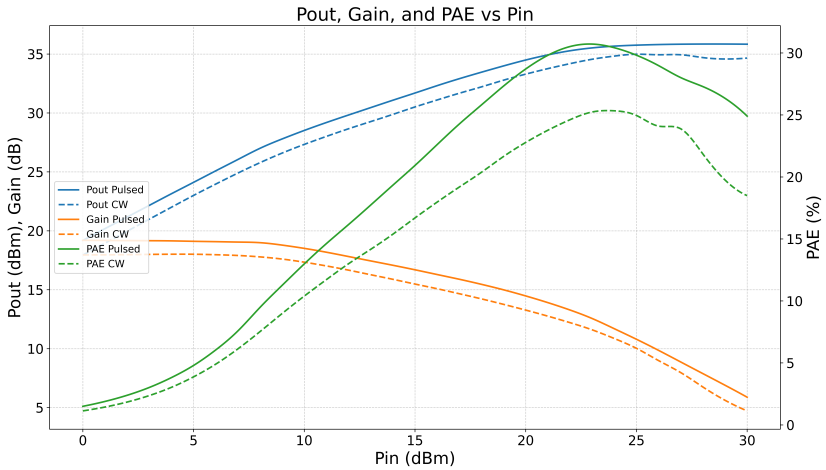



**Figure 7.13:** Measured output power, power gain, and PAE of the E0302 MMIC as a function of input power at 10 GHz under CW and pulsed conditions

# 8

# Discussion

This chapter discusses the results from chapter 4 and chapter 7 and discusses the results by presenting simulations versus measurements.

## 8.1. S-Parameters

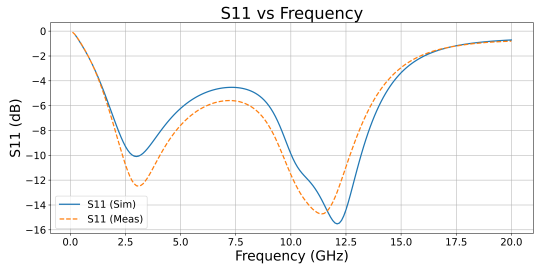
### 8.1.1. E0300: X-band Power Amplifier

Figure 8.1 presents the simulated and measured small-signal S-parameters and stability k-factor for the E0300 power amplifier over the 0-20 GHz range, obtained under nominal bias conditions. This comparison serves to verify the accuracy of the simulation models and see if the chip still meets the requirements after identifying any discrepancies.

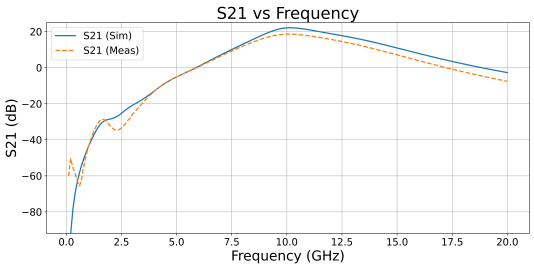
In Figure 8.1a, the measured reflection loss ($S_{11}$) is a bit worse as it has a slightly higher value then the simulation. This suggests minor differences in either the input matching network realization or in the transistor realization. The forward gain ($S_{21}$), shown in Figure 8.1b, peaks roughly at 20 dB in both measurement and simulation. The measured gain rolls off slightly faster at the upper end of the band.The output reflection coefficient ($S_{22}$), presented in Figure 8.1c shows the same shape, although the measured values are 3 dB higher. This is likely caused by fabrication tolerances in the output matching network or transistor realization This parameter is one of the least important parameter, as it will largely change under non-linear conditions. Further, the PA assumes a 50 Ω load for proper operation and in that case $S_{22}$ is not relevant.

Finally, the k-factor is shown in Figure 8.1d. At the lower frequencies (<6 GHz) the measured k-factor is much higher than the simulated value, which is good. It should be noted that in simulation the k-factor could only computed up to 30 dB, whereas in the measurement significantly higher values were observed.

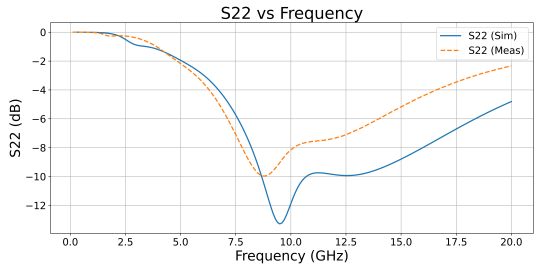
Overall, a good agreement for the small-signal parameters is found



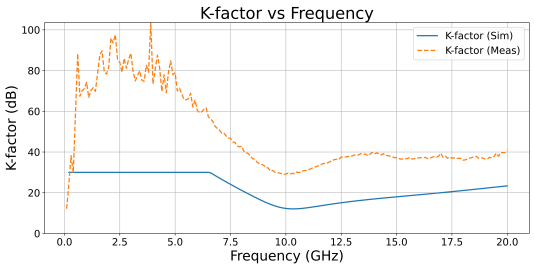

**(a)** Measured input reflection coefficient (S11)




**(b)** Measured small-signal gain (S21)




**(c)** Measured output reflection coefficient (S22)




**(d)** Measured stability factor (K)

**Figure 8.1:** Comparison of simulated and measured S-parameters and K-factor for the E0300 chip under nominal bias conditions

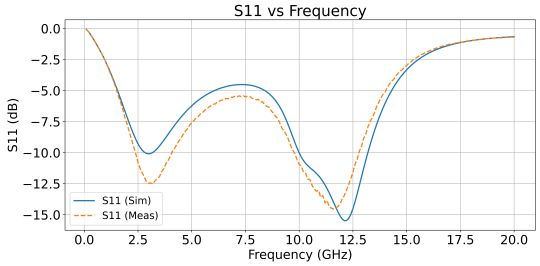
### 8.1.2. E0302: E0300 with Alternative Transistor

Figure 8.2 compares the simulated and measured S-parameters and k-factor of the E0302 design under nominal bias conditions. The results are much in line with the results for E0300.

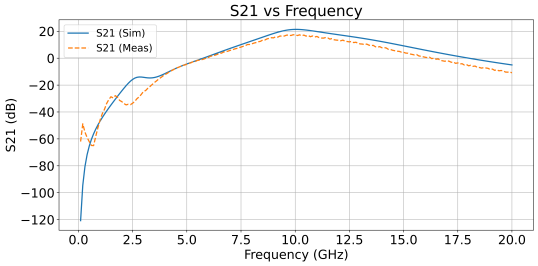
In Figure 8.2a, the measured reflection coefficient ($S_{11}$) is a bit worse as it has a slightly higher value then in the simulation. This suggests minor differences in either the input matching network realization or in the transistor realization. The forward gain ($S_{21}$), shown in Figure 8.2b, peaks roughly at 20 dB in both measurement and simulation. The measured gain rolls off slightly faster at the upper end of the band. The output reflection coefficient ($S_{22}$), presented in Figure 8.2c shows the same shape, but the optimum match occurs at a frequency that is a little bit too low. This frequency difference is smaller than for the E0300 design; apparently part of the downshift from E0300 is compensated by the inappropriate use of the shared via hole between the two output transistors. Again, however, this parameter is one of the least important parameters, as it will largely change under non-linear conditions and the PA assumes a 50 Ω load for proper operation and in which case the $S_{22}$ is not relevant.

Finally, the k-factor shown in Figure 8.2d. Almost identical to the E0300 design, at the lower frequencies (<6 GHz) the measured k-factor is much higher than the simulated value, which is good. It should be noted that during simulation the k-factor could only be computed up to 30 dB, whereas in the measurement significantly higher values were observed.

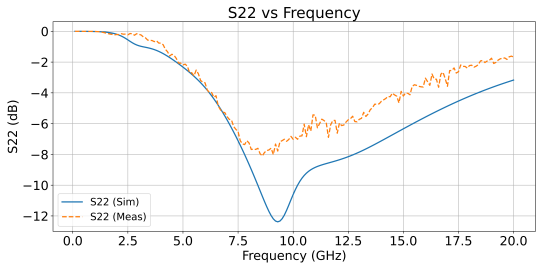
Overall, just like for the E0300 design, a very satisfying agreement for the small-signal parameters is found.



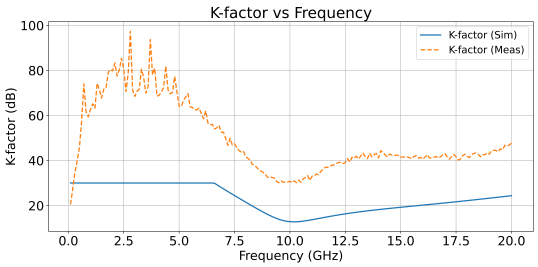

**(a)** Measured input reflection coefficient (S11)




**(b)** Measured small-signal gain (S21)




**(c)** Measured output reflection coefficient (S22)




**(d)** Measured k-factor

**Figure 8.2:** Comparison of simulated and measured S-parameters and K-factor for the E0302 chip under nominal bias conditions

# 8.2. Power

## 8.2.1. E0300: X-band Power Amplifier

The simulated and measured large signal metrics are compared in the three figures below. In Figure 8.3 the output power, PAE and power gain are plotted as a function of frequency at 20 dBm input power. Both continuous-wave (CW) and pulsed measurement results are included. The pulsed measurements (pulse length of 100 $\mu$s with a duty cycle of 10 %) were conducted to evaluate the influence of self-heating in the MMIC. All measurements were performed with a fixed input power of 20 dBm to ensure consistent and comparable dataset.

For both output power and gain, the agreement between measured and simulated results is really good, with deviations generally below 1 dB. At the upper end of the frequency band, the discrepancy increases slightly, which may indicate minor inaccuracies in the device modelling. The largest deviation is observed in the power-added efficiency (PAE). This parameter is inherently more sensitive to both design and measurement uncertainties, as well as to temperature variations.

The difference between pulsed and CW measurements is relatively small for the output power and the gain. At 10 GHz the gain difference between the two measurements is approximately 0.6 dB. From theory, the gain exhibits a temperature dependence of approximately -0.015 dB/K [27]. This suggests that the transition from pulsed to CW operation corresponds to an approximate temperature increase of 40 ° C. While this is significant, it indicates that improved cooling or shorter pulse durations could further enhance the efficiency.

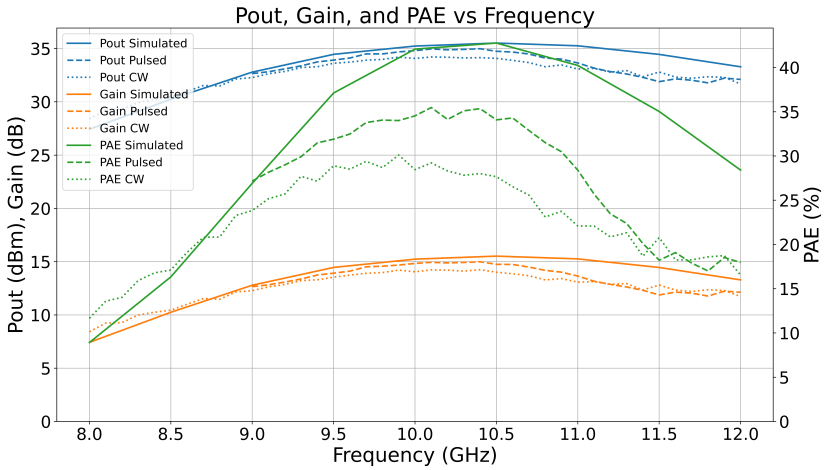



**Figure 8.3:** Comparison of simulated and measured output power, power gain, and PAE of the E0300 MMIC as a function of frequency at 20 dBm input power under CW and pulsed conditions

In Figure 8.4 the output power, PAE and gain are plotted as a function of input power at 10 GHz. It turns out that the maximum efficiency occurs at a slightly higher, at 22 dBm, input power than predicted by the simulation (20 dBm). This shift may be attributed to a slightly reduced gain in the first amplifier stage in the fabricated device compared to the model.

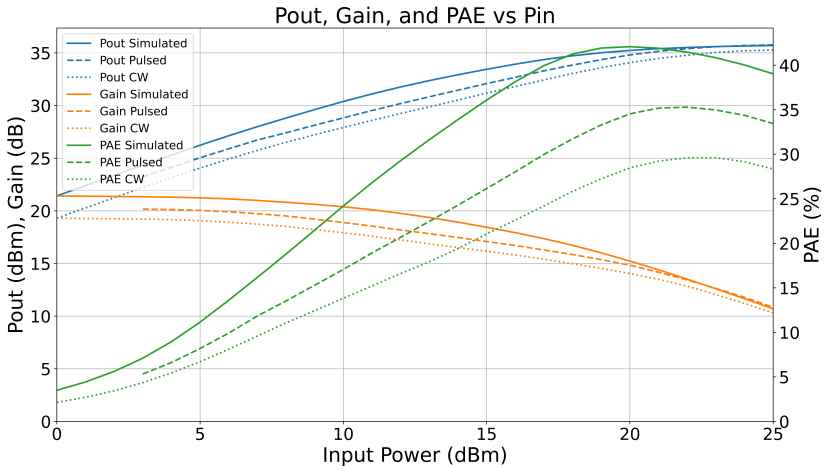



**Figure 8.4:** Comparison of simulated and measured output power, power gain, and PAE of the E0300 MMIC as a function of input power at 10 GHz under CW and pulsed conditions

Finally, Figure 8.5 shows the drain current as a function of input power at 10 GHz. In compression, both the first-stage as second-stage drain currents are higher than predicted. This may be caused by difference in the two-dimensional electron gas (2DEG) properties between the simulated model and the fabricated devices. The increased DC current explains the lower measured PAE observed in the previous figure, as can be seen in Equation 3.16. The difference between pulsed and CW drain current is minimal.

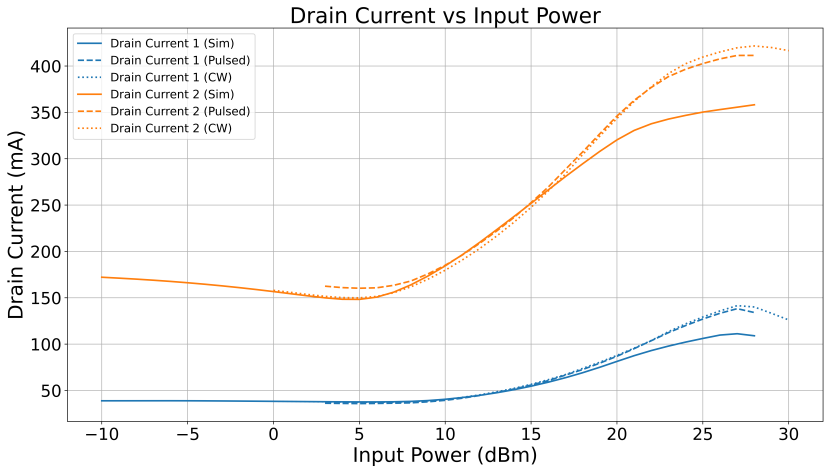



**Figure 8.5:** Comparison of simulated and measured drain currents of the E0300 MMIC versus input power at 10 GHz for the first and second amplifier stages, under CW and pulsed operation

### 8.2.2. E0302: E0300 with Alternative Transistor

The simulated and measured large-signal performance of the E0302 design is compared in Figure 8.6 and 8.7. The measurement details are identical to those described in the previous section for E0300. Also the measurements to a large extent follow the same behaviour. For minimizing device self-heating, pulsed measurements (100$\mu$s pulse length, 10% duty cycle) were again performed.

In Figure 8.6 the output power, gain and PAE are plotted as a function of input power at 10 GHz. At the measurements the peak PAE occurs at a slightly higher about drive level, similar to what was observed for the E0300 design. This shift may be linked to a slightly lower gain in the first stage of the realised amplifier compared to the model. Both continuous-wave (CW) and pulsed measurement results are included. In general, the agreement between measured and simulated results is really good, with deviations in output power and gain generally below 1 dB. The largest deviation is observed in the power-added efficiency (PAE). The PAE values are a bit lower than expected, and also lower than for the E0300 design. This parameter is inherently more sensitive to both design and measurement uncertainties, as well as to temperature variations.

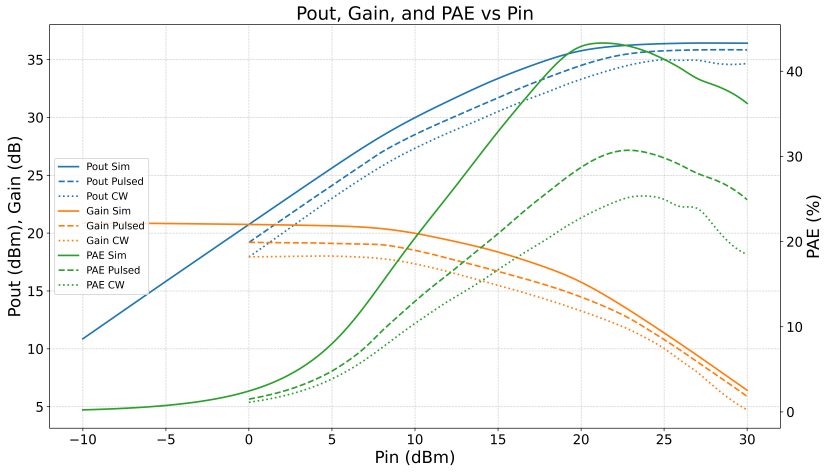



**Figure 8.6:** Measured and simulated output power, gain and PAE versus input power at 10 GHz input power for the E0302 design, under CW and pulsed conditions

Figure 8.7 shows the same metrics plotted against frequency for a fixed 20 dBm input power. Both the measured gain and output power track the simulated predictions well, with deviations typically below

1 dB at the desired frequencies. At the upper end of the frequency band, the discrepancy increases slightly, which may indicate minor inaccuracies in the device modelling. As with the E0300, the PAE shows the largest discrepancy, being more sensitive to both modelling and temperature effects.

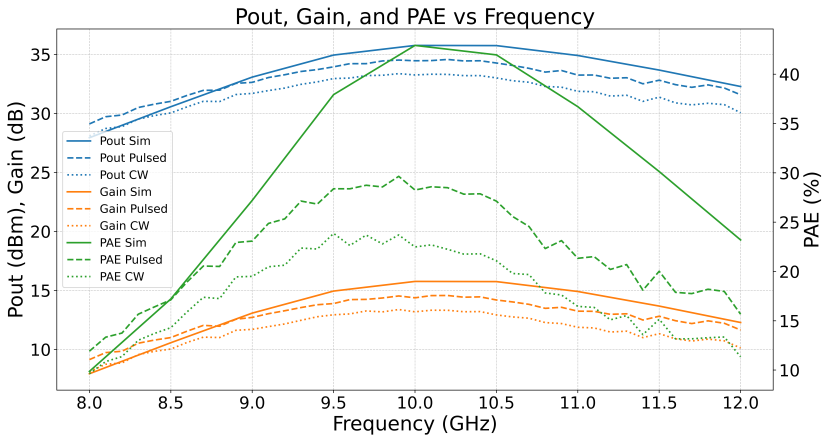



**Figure 8.7:** Measured and simulated output power, gain and PAE versus frequency at 20 dBm input power for the E0302 design, under CW and pulsed conditions

An explanation for the lower PAE in comparison to the E0300 design could be in the transistor model, but could also be in an increased thermal coupling between the two neighbouring transistors. Overall, the E0302 design matches the simulated behaviour closely and meets the key requirements for gain, stability and output power.

## 8.3. General Discussion

Based on the good agreement between simulation and measurement results, the design methodology turns out to be valid for this frequency and power range. The results, both small-signal and large-signal, follow the simulation closely.

No stability problems occurred during the measurements, indicating that also in this respect the extensive simulation philosophy worked out well. This is a really good result, as this problem deals with very large gains and is difficult to simulate due to its non-linear and thermally sensitive behaviour as well as the large amount of variables. This stability verified an important part of the research question.

There is only one parameter that is lagging in performance during the measurements: the PAE. This parameter is notably the most difficult to predict, as it combines all the critical modelling parts: the DC behaviour, the microwave characteristics, the non-linear modelling and the thermal accuracy. As it lags behind the simulation only a few percent point, it justifies the conclusion that a second iteration of the design would allow to get also this value on par with the simulations. The high sensitivity of the PAE for duty cycle also suggests that for even shorter pulses and duty cycles the measured PAE would even be closer to simulations.

From the comparison between the E0300 and the E0302 designs, it is found that from a small-signal perspective the sharing of a via hole is acceptable. The differences between the two designs are only very small. From a large-signal perspective, this is not the case. Although the output power is virtually identical, the PAE is significantly lower. A most likely cause for this is that the optimum load for a transistor with shared via holes is different than for a transistor without shared via holes. As a consequence, the design would have needed a differently tuned output matching circuit. This could be solved by performing dedicated load-pull transistor measurements for the shared-via hole transistor and then incorporating the results in a different design. An alternative explanation could be the thermal

coupling between the two output transistors, that are now more closely separated and are even directly coupled thermally through a via hole. This could be evaluated through thermal measurements.

# 9

# Conclusion and Future Work

This chapter concludes the thesis. It reports in a concise way the conclusions of the work and presents some possibilities to extend the work further.

## 9.1. Conclusion

The research question that was posed at the start of the work is whether we can design a lower frequency (10 GHz) power amplifier in a power ampifier process that is capable of operating at very high frequencies (well over 100 GHz).

### 9.1.1. Overview

For the design in NP12 technology, a design process was followed that started with transistor measurements, after which an architectural design was made. This design was detailed into a schematic design and then refined into a design in which all interconnections were electromagnetically modelled. In parallel, a layout of the power amplifier was designed, the detail of which followed the schematic and electromagnetic design.

This way of continuous refinement and optimization of power amplifier parts was the only way to deal with the extensive simulation times. After careful checks for compliance with the integrated circuit manufacturing rules, the design was submitted to the foundry, and manufactured IC samples returned back after approximately four months. After this, an extensive characterization of the MMIC was performed, through both small-signal as well as non-linear measurements.

### 9.1.2. Key Performance Indicators

The four KPI's that we identified in section 2.4 (power, efficiency, stability and size) were linked to the Programme of Requirements. For the power, a peak power of over 38 dBm was realized under dedicated measurement conditions and over 35 dBm for nominal measurement conditions (20 V $V_{ds}$), and a bandwidth of more than 2 GHz (1-dB bandwidth) or 3 GHz (3-dB bandwidth) was obtained. For the PAE, 35 % was nominally achieved (over various bias points and frequencies), which was a few percent point below the 40 % target value. Several ways to improve on this were identified, and will be reported under future work. Unconditional stability was achieved, which answered an important part of the research question. The size of the amplifier was 2x1.75 $mm^2$, extended to 3x1.75 $mm^2$ for multi-project wafer manufacturing reasons. This resulted in a peak value of slightly below 2 W/mm, a value that could be improved by optimizing the design on this aspect.

A detailed answer of the entire Programme of Requirements is included Appendix A.

### 9.1.3. Evaluation

For the absolute power level, power amplifiers with a higher output power at X-Band can be found in literature, the same holds for the power per square $mm^2$. Although power amplifiers with much more

power could be made in NP12 through parallelling more transistors in the output stage, NP12 is not likely to improve the state-of-the-art in this respect. The basic limitation is the maximum drain voltage. This translates directly into the maximum power, and dedicated lower-frequency processes can have higher maximum drain voltages, and hence higher absolute maximum powers.

For the efficiency and gain of the amplifier, the results of this amplifier are a little below the state-of-art, but very encouraging. It is quite an achievement that a first design-effort comes so close to the best reported performance. The expectation is strengthened that the advantages of a mm-wave process used at X-Band frequencies can pay off in somewhat increased efficiency and significantly increased gain.

It was shown that the main boundary condition, an unconditional stability of the power amplifier, can be achieved. Many small measures were taken, including placing small stabilizing resistors at well-chosen positions in the circuit, for example the resistors that are in series with the bias decoupling capacitors. The implementation of the stability analysis for this power amplifier took a significant effort, but paid off very much as no instability was observed at all during the measurements.

Two variations of the amplifier were implemented to investigate the possibility of reusing the source via-hole for two adjacent output stage transistors. This would save area (and hence cost) in an amplifier product, or increase the maximum output power for a given amplifier height. This variation, with re-used via-holes, worked similar to the baseline design, with one exception. The measured PAE was lower than for the baseline design. The cause for this is thought to be in a slightly incorrectly modelled transistor (as effectively the transistor now has only half of the source via-holes). This could be solved by creating dedicated test-transistors for load-pull analysis and modelling.

## 9.2. Future Work

Creating a state-of-art implementation of an MMIC power amplifier, a topic where so much research and development effort has been spent, is a large and demanding task. Several options for future work are hence still open, and briefly summarized below.

### 9.2.1. Design Optimization

The design can be optimized further for either of the KPIs, depending on the KPI that is prioritized:

- If maximum power is of premium concern, an output stage with more and larger transistors can be performed. This will affect also the earlier stages. It is expected that a slight reduction in efficiency will occur, as the output combiner network will be more complex and hence a little lossier.
- If maximum power is of premium concern, an output stage with more and larger transistors can be performed. This will affect also the earlier stages. It is expected that a slight reduction in efficiency will occur, as the output combiner network will be more complex and hence a little lossier.
- If minimum size is of premium concern, shrinking the passive bias elements would be possible. A optimization of the layout of that part could be done, part of the decoupling could be off-chip (increasing risk of oscillation, but reducing the chip size), or a re-use of bias elements for both transistors could be investigated.
- If maximum efficiency is of premium concern, a second optimization of the design, incorporating all the little things that were learned in this first iteration would be the first step. A second step could be to reduce the stability measures: during the design we did not yet dare to do so, but confidence on the stability was gained. A third option would be to introduce specialized amplifier classes and change the entire amplifier architecture. One of the easier options would be to spend extra time on for example harmonic termination. If we do so for the second and third harmonic, we need to be aware that the (non-linear) modelling of transistors and all passives needs to be accurate up to at least 36 GHz (third harmonic of upper design frequency), which is not easy.

### 9.2.2. Design Application

Many MMIC designs implement multiple functions, and the PA that was designed in this thesis could form a part of such a larger design. Front-end chips, that implement the receiver and transmitter components that connect to an antenna are one of these [28].

There are many opportunities to integrate this PA in such a multi-function chip and explore advantages of e.g. the very good noise figure of NP12 for X-Band applications.

Finally, the application of the MMIC to demonstrate a real application would be very interesting. If we solve the packaging problem for the MMIC (possibly through an air-cavity QFN package), it could be straightforward to realize an X-Band transmitter on a small PCB board that integrates the power amplifier, control electronics and potentially even the antenna element.

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# A

# Requirements Implementation

In chapter 2, the Programme of Requirements was defined. In this appendix we return to the Programme of Requirements to ensure that the requirements set at the beginning were met to the extent possible. We revisit the Mandatory Requirements and the Objectives.

## A.1. Mandatory Requirements

- [2.2.1] The frequency of operation must be at X-Band (10 GHz)
  This requirements was met during the design phase
- [2.2.2] The output power of the amplifier must be larger than 30 dBm.
  This requirement was met during the design phase and confirmed with measurements.
- [2.2.3] The amplifier must be unconditionally stable.
  This requirements was ensured through extensive simulation and confirmed during them measurement
- [2.2.4] The size of the amplifier is smaller than the maximum manufacturing reticle size.
  This requirement was ensured during the maximum manufacturing reticle size.

## A.2. Objectives

### A.2.1. Functional Requirements

- [2.3.1.1] **Frequency:** The amplifier shall operate at 10 GHz with a bandwidth targeting 1 GHz.
  This requirement was met during the design phase and confirmed with the measurements. The 1-dB gain bandwidth exceeds 20% and commonly used 3dB gain bandwidth even exceeds 30% relative bandwidth. THis corresponds to 2 GHz and 3 GHz absolute bandwidth respectively.
- [2.3.1.2] **Output power:** The amplifier shall deliver a maximum power targeted at 36 dBm output power at 10 GHz.
  This requirement was met during the design phase and confirmed with measurements. Peak powers measured were exceeding 38 dBm and even at only 20 V $V_{ds}$ more then 35 dBm was measured.
- [2.3.1.3] **Gain:** The power gain shall be higher than 10 dB, targeting 15 dB.
  This requirement was met during the design phase and confirmed with measurements. The small-signal gain was around 20 dB and at the maximum efficiency, the most likely operating point, the compression gain was still approximately 15 dB.
- [2.3.1.4] **PAE:** The amplifier shall exhibit a maximum PAE, targeting 40%.
  This requirement was the toughest to meet. The requirement was met during simulation, but was not fully met during measurements. Many efforts were directed at this challanging requirement, the peak efficiency measured is 35%.

- [2.3.1.5] Input reflection: The amplifier shall have an input reflection below -10 dBm.
  This requirement was met during the design phase and confirmed with the measurements.
- [2.3.1.6] The amplifier must be insensitive to slight variations in external influences, such as a load mismatch or minor supply fluctuations.
  This requirement was ensured in the design phase.

### A.2.2. Manufacturing Requirements

- [2.3.2.1] **Supply voltage:** the PA shall operate at 20 V.
  This requirement was ensured during the design phase.
- [2.3.2.2] **Area:** The area of the integrated circuit shall be as small as possible, but not exceed 6 $mm^2$.
  This requirement was met during the design phase. The designed power amplifier was 1.75x2 $mm^2$ and was extented with an extension line and blank space to 1.75x3 $mm^2$ to meet other reticle requirements.
- [2.3.2.3] **Height:** The height of the integrated circuit shall be 1.75 mm to allow integration with other designs on the semiconductor reticle.
  This requirement was ensured during the design phase.

### A.2.3. System Requirements

- [2.3.3.1] The control interface must digitally control the bias and be able to disable and enable all bias voltages.
  This requirement was met during the design of the measurement setup.
- [2.3.3.2] The control interface must include current limits as protection feature.
  This requirement was met during the design of the measurement setup.
- [2.3.3.3] The in- and output impedance of the amplifier must be in line with industry standards (i.e. 50 Ohm).

- [2.3.3.4] No DC voltage may be present at the RF in- and output ports, so that connected equipment will not be damaged or disrupted.
  This requirement was ensured during the design phase through the introduction of DC blocking capacitors at the input and output of the MMIC.