Frequency References Based on the Thermal Diffusivity of Silicon and Silicon Dioxide

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To My Parents

and Tripti.

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TU Delft

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1 Introduction

Conventional methods of generating accurate on-chip frequencies are based on electrical components such as resistors, capacitors, and inductors. Recently, a new type of frequency reference based on the thermal diffusivity (TD) of silicon has been introduced. Such TD frequency references rely on the well-defined thermal-domain properties of silicon, rather than on the stability of electrical components. This thesis explores various ways of improving the performance of TD frequency references. This chapter provides an introduction to the thesis. Section 1.1 provides a brief introduction to integrated frequency references. Section 1.2 gives an overview of the prior work on TD frequency references. Section 1.3 presents the motivation for this thesis and finally, Section 1.4 describes the structure of the thesis.

1.1 Integrated Frequency References

Today, the majority of electronic systems are synchronous, i.e. they require clock signals for proper operation. The level of stability and noise of the clock signals used in systems such as radios and analog-to-digital converters is an important determinant of their performance. To generate clock signals, some kind of frequency reference is required. In the last few decades, the dominant frequency control and generation block has been the quartz-crystal oscillator [1]. Although crystal oscillators can be used to realize very accurate clocks, they cannot be integrated due to their specific manufacturing process.

Due to the trend towards more and more integration, it is natural that there is a trend to realize integrated frequency references. Compared to crystal oscillators, the advantages of integrated frequency references include their reduced cost and form factor, and their increased reliability and ease of testing [2]. In recent years, there have been several efforts to integrate frequency references, with the main focus being on LC oscillators, MEMS oscillators, RC oscillators and TD frequency references [2][3][8][9].

Although the ultimate goal of any integrated frequency reference is to achieve the accuracy of crystal oscillators, however, this is not necessary for all applications. A remote sensor node, for instance, can tolerate inaccuracies of up to a few percent, but its power consumption should only be a few tens of micro-Watts [3]. On the other hand, HS-USB (High-Speed USB), S-ATA (Serial Advanced Technology Attachment) applications require inaccuracies of less than ±500ppm [4] and ±350ppm [5], respectively. Fig. 1.1 shows the accuracy vs. power trade-off for different types of frequency references.

As can be seen from Fig. 1.1, although *LC oscillators* [6] have sufficient stability for HS-USB applications, their power consumption is quite high (~3.5mW) and they are thus not suitable for low-power applications such as wireless sensor nodes. An LC oscillator consists of an LC tank in parallel with a circuit that generates a negative resistance to compensate for the losses in the tank. An additional temperature compensation circuit is required to provide sufficient stability over temperature. LC oscillators can be integrated in standard CMOS.

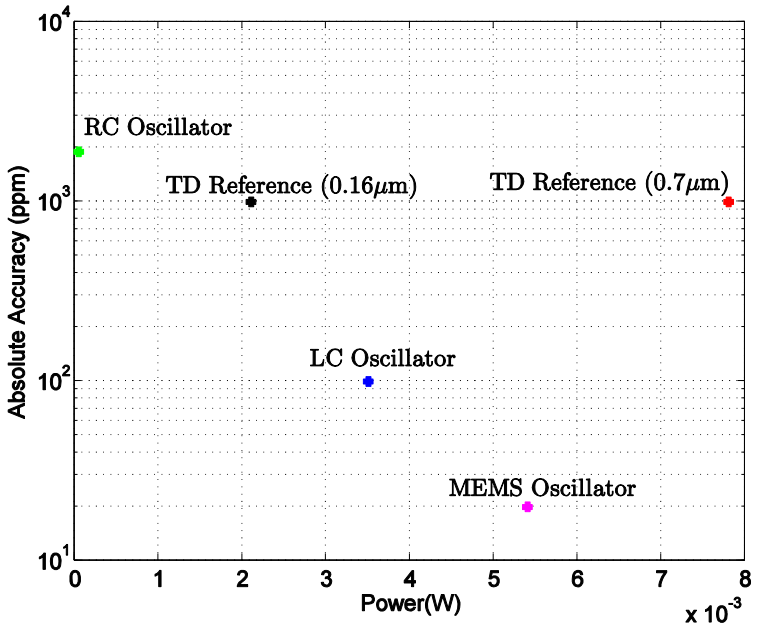

Fig 1.1- Absolute accuracy vs. power consumption of various frequency references

MEMS oscillators are the closest rivals of crystal oscillators. This is mainly because of the very high quality factors (Q > 100000) that can be achieved by MEMS resonators [7]. After temperature compensation, such oscillators can achieve sub-ppm stability, which is comparable to that of crystal oscillators [7]. Due to the special process technology required for the manufacture of MEMS resonators, MEMS oscillators typically consist of two chips, one containing the resonator and the other containing CMOS circuitry.

RC oscillators are based on time constants established by resistors and capacitors. Among the various possible topologies, the Wienbridge and relaxation oscillators are the most common. Due to the process and temperature drift of on-chip resistors and capacitors, such oscillators need to be carefully designed in order to achieve inaccuracies in the order of a few percent. The benefit of such oscillators is their very low power consumption (in tens of μW). This makes them suitable for use in low-power applications with relaxed stability requirements, such as in biomedical implants or wireless sensor networks [8].

All the above-mentioned frequency references are based on either the electrical or mechanical properties of silicon. Recently, however the *thermal* properties of silicon have also been used to create frequency references [9][10]. The design of thermal frequency references will be the main focus of this thesis. Their operation will be described next.

1.2 Thermal frequency references

Most on-chip oscillators depend on a time constant (delay) or resonance frequency generated by an electrical circuit. However, delays can also be created in the thermal domain. A thermal oscillator can then be realized by incorporating such a delay into an oscillator. Thermal oscillators have been around for quite some time. The first thermal oscillator was created by Bosch, in 1972, with structures that could realize a thermal delay and perform a thermal to electrical conversion [11]. In 1995, Szekely [12] investigated the use of such oscillators for temperature-to-frequency conversion. This work was

further advanced by Makinwa [13], who used a thermal oscillator to create an accurate temperature-to-frequency converter.

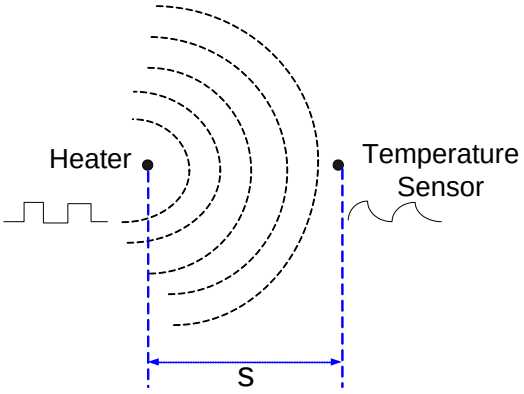

Fig 1.2- Top view of a thermal delay line. Both the heater and temperature sensor are realized in the same silicon substrate

Central to the concept of thermal oscillators is the thermal delay line. Fig 1.2 shows a simplified top view of a thermal delay line. It consists of a point-heater in the vicinity of a point-temperature sensor in a silicon substrate. The point heater generates heat pulses as a function of an AC electrical signal applied to it. These then travel through the silicon substrate, arriving at the temperature sensor after a certain delay. This delay is governed by the distance between the heater and the temperature sensor, and by the well-defined thermal diffusivity of silicon [13]. The latter is the rate at which heat diffuses through silicon. A temperature sensor then converts the delayed heat pulses back into an AC electrical signal.

For the highly pure epitaxial silicon used in ICs the thermal diffusivity D of silicon is quite well-defined [14]. However, the distance between the heater and the temperature sensor, s, is only as accurate as the lithography of the fabrication process. Thus, variations in s will cause the thermal delay to vary from device to device. However, this should be less of a problem in more advanced process technologies that support smaller feature lengths, i.e. thermal delay lines should benefit from Moore's law [15].

The heater and the temperature sensor of a thermal delay line can be realized in standard IC technology. For instance, a resistor can be used as the heater, while a thermocouple can be used as the temperature sensor. (A thermocouple[1] is a relative temperature sensor based on the Seebeck effect.) A thermal delay line can be regarded as an Electrothermal Filter (ETF) [13]. This is because it behaves like a thermal low-pass filter, in the sense that there is a phase shift (delay) between the AC signal applied to its heater and the AC signal produced by the temperature sensor. This phase-shift is determined by D and by the ETF's geometry. Since D is temperature dependent, the phase characteristic of an ETF will be a function of temperature [13][16].

The phase shift of an ETF can be extracted by synchronous demodulation (see Fig.1.3). This is done by multiplying its output signal by a replica of its input signal. The resulting DC term will then be proportional to the phase difference between the two signals. In [13], a frequency-locked-loop (FLL) was created by embedding an ETF and a synchronous demodulator in a feedback loop together with an integrator and a VCO (Fig.1.3). The integrator drives the VCO, whose output drives the heater of the ETF. Feedback ensures that the VCO output frequency creates a 90^0 phase shift in the ETF, since the

[1] Thermocouples are described in detail in Chapter 2.

DC term at the output of the synchronous demodulator then goes to zero, resulting in a stable integrator output. Thus, the FLL's output frequency will be locked to the ETF's thermal delay. The work of [13] demonstrated this in practice and showed that the output frequency has the same temperature dependence as *D*. This concept was used to create a temperature-to-frequency converter.

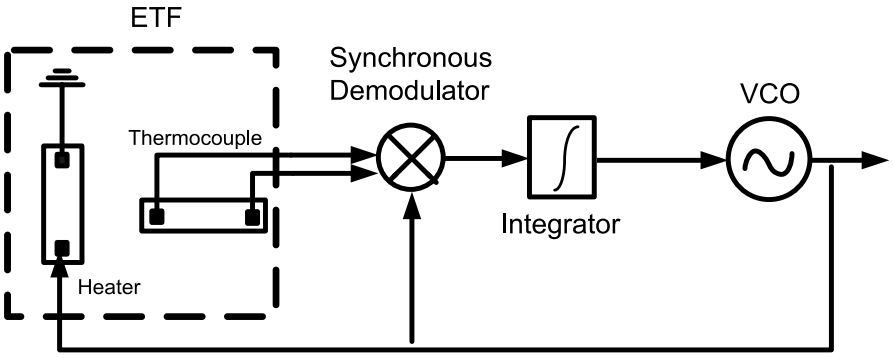

Fig 1.3- Simplified diagram of a FLL with ETF within the loop

If the temperature dependence of the thermal delay can be compensated, the same FLL can be used as a frequency reference. Instead of operating the ETF at a fixed phase-shift of 90^0, this reference phase-shift can be varied with temperature such that the output frequency becomes temperature independent. In [9][10], this principle has been used to create a Thermal Diffusivity (TD) based frequency reference. Fig. 1.4 shows a simplified block diagram of such a TD reference. An on-chip band-gap temperature sensor is used to measure die temperature. This is then mapped to a reference phase that compensates for the temperature dependence of the thermal delay (Fig. 1.5 and Fig. 1.6). Thus, a temperature-stable output frequency can be obtained.

The first TD reference was designed in a 0.7µm CMOS process [10]. It achieved less than 1000ppm inaccuracy over the military temperature range (-55^0C – 125^0C), while dissipating 7.8mW of power from a 5V supply. Another TD reference was designed in a 0.16µm CMOS process with a much smaller ETF (*s*=4.7µm compared to *s*=24µm in the previous design) [9]. The reduction in *s* improved the SNR at the output of the ETF, thus resulting in lower power consumption while achieving similar inaccuracy (1000ppm).

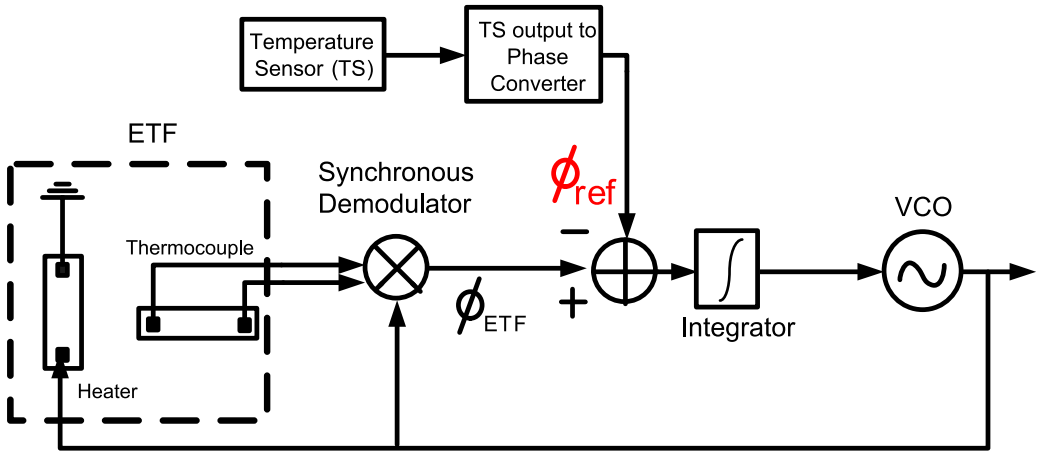

Fig 1.4- Simplified diagram of the FLL with temperature compensation

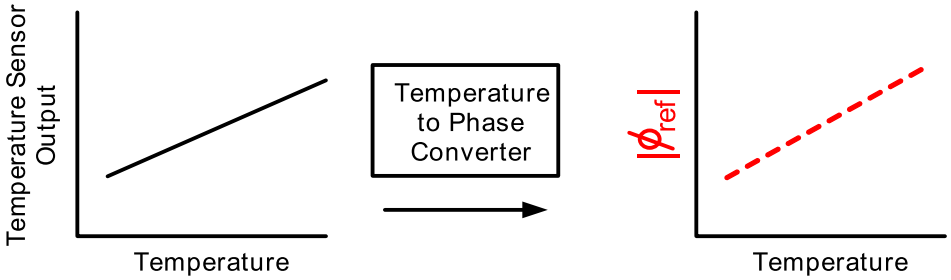

Fig 1.5- Temperature compensation scheme

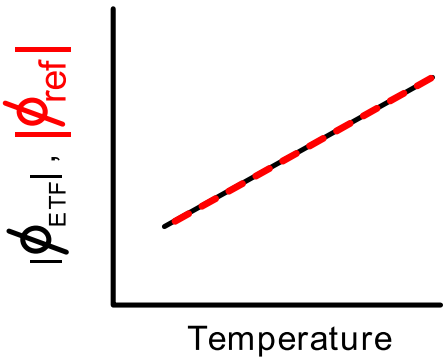

Fig 1.6- Ideal temperature compensation of thermal delay, ϕ_{ETF} , by ϕ_{ref}

1.3 Motivation

The earlier designs [9][10], have shown that it is feasible to build frequency references based on the thermal diffusivity of silicon. One of the aims of this work is to achieve improved performance by optimizing the silicon ETF. The limit to their accuracy is studied by characterizing a few silicon ETF which were fabricated earlier.

In [9][10], the combined process spread of the temperature sensor and the ETF was corrected by a single room-temperature trim applied to the temperature sensor. As a result, the compensation is only perfect at the trimming temperature (Fig. 1.7). In this work, a two temperature trim, albeit more expensive, is likely to result in better accuracy (Fig. 1.8) and is therefore investigated. A comparison of slope trim, offset trim and two temperature trim is also done to find out which of the three trims results in best temperature calibration.

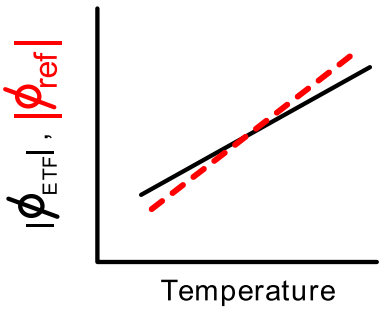

Fig 1.7- : Temperature compensation of thermal delay, ϕ_{ETF} , using PTAT trim

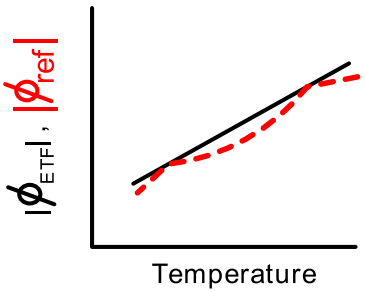

Fig 1.8- Temperature compensation of thermal delay, ϕ_{ETF} , using 2 temperature trim

In [9][10], it was stated that the main limitation on frequency accuracy was the inaccuracy of the Temperature Sensor (TS). As mentioned earlier, the output of the TS is used to create a reference phase for the FLL. Since the TS is outside the loop, any error in its output creates a frequency error. This means that the accuracy of a TD frequency references is not only governed by the tolerance of the ETF, but is also a function of its temperature compensation scheme. The sensitivity of output frequency to errors in the temperature compensation scheme is determined by the temperature dependence of *D*. In [9], it is shown that even a state-of-the-art temperature sensor [21] with an inaccuracy of 0.1^{o}C will limit frequency inaccuracy to about 800ppm.

The thermal diffusivity of a material is given by the thermal conductivity divided by the density and specific heat capacity. The temperature dependence of the diffusivity of silicon is mainly due to its thermal conductivity k. As it turns out, the temperature dependence of the thermal conductivity of silicon dioxide is much lower than that of silicon [22][23]. Thus, an ETF realized in silicon-dioxide should have much lower temperature dependence than that of an ETF realized in silicon. A TD frequency reference based on such ETF would potentially be more resilient to the inaccuracy of its TS. One of the major aims of this research is to fabricate and test an ETF structure in which a significant part of the delay comes from oxide.

With better accuracy expected from oxide based ETF, it is imperative to look at other sources of errors in the FLL loop. The TD frequency references proposed in [9][10] incorporate a digitally-assisted FLL which uses a Digitally Controlled Oscillator (DCO) instead of the VCO (shown in Fig 1.4). A DCO is a digital-to-frequency converter and thus introduces quantization noise determined by its resolution. In this work, the effect of limited DCO resolution on the frequency accuracy will be explored. Previous implementations had a DCO resolution of 200ppm. Limited DCO resolution can not only cause frequency errors at a particular measurement point but also affect the trimming accuracy. Thus, one of the motivations for this work is to reduce the frequency errors due to limited DCO resolution. Another performance metric of interest is the jitter of the frequency reference. In previous designs, this was limited by the DCO. Thus, the noise of the DCO should be reduced to be in line with the expected improvement in the accuracy.

1.4 Structure of Thesis

The organization of the thesis is as follows:

Chapter 2 describes the Electrothermal Filter along with the equations that govern its operation. Previous implementations of TD frequency references and their performance limitations are also discussed in more detail.

Chapter 3 investigates the performance limitations of silicon ETFs. Three different sized ETF are compared with respect to their SNR and accuracy. Further, comparison based on different types of trim, for the three ETFs, is discussed. Based on the result of these comparisons a more accurate frequency reference is presented.

Chapter 4 introduces Oxide ETF as a solution to the accuracy limitation due to temperature coefficient of the Silicon ETFs. Structure and various properties of the Oxide ETF are discussed. A frequency reference based on the proposed Oxide ETF is described and measurement results are presented.

Chapter 5 provides the details of the improvement in DCO resolution. Specifications for an improved DCO are derived and a complete circuit design is presented. Various components of the DCO are optimized for jitter. Oversampling and noise shaping are used to improve the resolution of the DCO.

Chapter 6 presents some conclusions and some recommendations for future work.

2 TD Frequency References

In this chapter, a detailed discussion of earlier work on TD frequency references is presented. Electrothermal filters are described in detail as they are at the heart of such references; an understanding of what they are and how they work is an essential requirement for any meaningful discussion on this topic. Section 2.1 describes the theory and design of electrothermal filters (ETF). Section 2.2 describes electrothermal frequency-locked loops (FLL) while Section 2.3 discusses the design of TD frequency references. Section 2.4 concludes the chapter.

2.1 Electrothermal Filters: Theory

As mentioned in the previous chapter, TD frequency references use electrothermal filters (ETFs) to generate accurate delays (or phase-shifts). By means of an electrothermal frequency-locked loop (FLL), the output frequency of an oscillator can be locked to the phase shift of an ETF. The accuracy of the output frequency is determined by the accuracy of the ETF's phase shift. This section delves more into the theory of operation of ETFs and explains the factors that affect their operation and performance.

2.1.1 Electrothermal Filters

An ETF is an electrothermal structure that is capable of producing accurate phase shifts [13]. It has electrical input and output signals; however, its phase shift is generated in the thermal domain. The top view of an ETF is shown in Fig.2.1. It consists of a heater which converts an AC electrical signal into heat. A relative temperature sensor is then implemented in close proximity to the heater and in the same silicon substrate. To realize an ETF in a standard IC process, a resistor may be used as the heater, while a thermopile (series connection of thermocouples) may be used as the temperature sensor.

The electrical signal applied to the heater generates heat pulses which travel through the silicon substrate. This acts as a low-pass thermal filter and delays the heat pulse. The heat pulses eventually reach the thermopile, which then converts them back to an AC electrical signal. The phase shift between the heater's power dissipation and the thermopile's output signal will be denoted by ϕ_{ETF} .

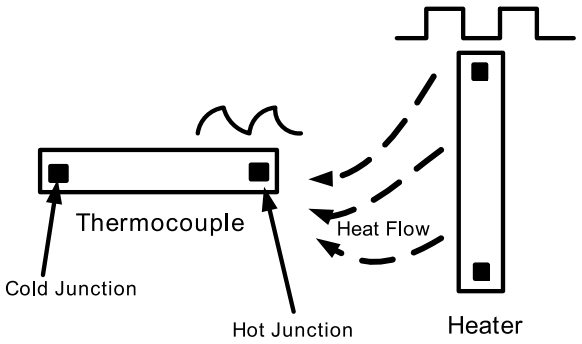

Fig 2.1- : Top View of an ETF

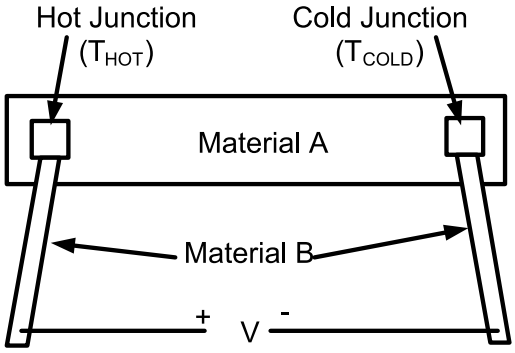

Fig 2.2- Operation of a thermocouple

The operation of a thermopile is based on the *Seebeck effect*, i.e. the fact that if two junctions between two dissimilar conductive materials are at different temperatures, a voltage will be generated across them. This is illustrated in Fig. 2.2. If the temperature difference between the hot and cold junctions is ΔT then the potential developed across the thermocouple, V_{TC} is given by

$$V_{TC} = (\alpha_1 - \alpha_2)(\Delta T) \tag{2.1.1}$$

Where α_1 and α_2 are the Seebeck coefficients of the two materials.

In a practical ETF, a number of thermocouples are connected in series such that the potential across the thermocouples accumulates. The result is a thermopile with a differential output, as shown in Fig. 2.3.

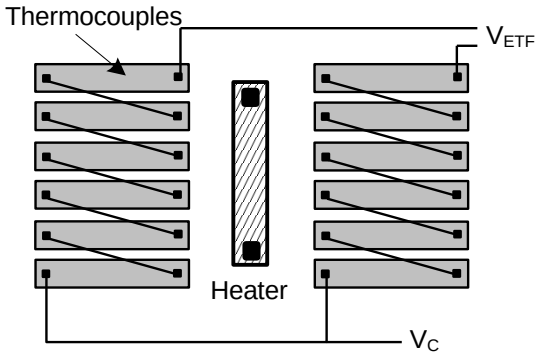

Fig 2.3- Traditional ETF bar structure

2.1.2 **ETF Thermal Delay Modelling**

The phase vs. frequency characteristic of an ETF is a function of its geometry and the thermal properties of silicon. This can be modelled in the thermal domain and the results transferred to the electrical domain by exploiting the analogies between the two domains. In [16][18] a detailed description of the modelling of ETFs is presented. A brief explanation and a summary of the main results are given below.

In the thermal domain, if Q watts of heat is dissipated by a point-heater, the temperature at any given point, *i*, and at a distance *s* from the heater is given by

$$T_i = QZ_{th,i} \tag{2.1.2}$$

Where $Z_{th,i}$ is the thermal impedance between the point-heater and the given point *i*. Thus, $Z_{th,i}$ determines the characteristic of the thermal domain filter, because it models the temperature fluctuations at the point *i* as a function of the heat dissipated in the heater. For an AC heat dissipation, this thermal impedance is a complex function of frequency and is given by [16][18]

$$Z_{th}(s,\omega) = \frac{1}{2\pi ks}.\exp\left(-s\sqrt{\frac{\omega}{2D}}\right)\exp\left(-js\sqrt{\frac{\omega}{2D}}\right) \tag{2.1.3}$$

Where *s* is the distance between the heater and the point *i*, ω is the frequency at which heater is driven and *D* is the thermal diffusivity of the bulk material. The magnitude of Z_{th} is given by

$$\left|Z_{th}(s,\omega)\right| \propto \frac{1}{s}.\exp\left(-s\sqrt{\frac{\omega}{2D}}\right) \tag{2.1.4}$$

And its phase shift is given by

$$\phi = -s\sqrt{\frac{\omega}{2D}} \tag{2.1.5}$$

The thermal diffusivity *D* of lightly-doped mono-crystalline silicon is essentially process independent [19]. Thus, the accuracy of the thermal phase shift in Eq. 2.1.5 should be, to first order, mainly determined by the accuracy of *s*. Furthermore, it should be noted that the thermal diffusivity of silicon is a strong function of temperature and can be approximated by the following power law [14],

$$D \propto \frac{1}{T^n}, n \approx 1.8 \tag{2.1.6}$$

Thus, from Eq. 2.1.5 the temperature dependence of a point-heater point-temperature sensor electrothermal system can be approximated as

$$\phi \propto -T^{0.9} \tag{2.1.7}$$

Previous ETFs, have used a thermocouple as their temperature sensor [16][18]. Since a thermocouple measures temperature differences, the location of its cold junction should also be considered in determining the thermal impedance of an ETF. It can be shown that the effective thermal impedance is a vector sum of the thermal impedances of the thermocouple's *Hot* and *Cold* junctions [16] [18]. The temperature difference between these two junctions is then given by,

$$T_{hot} - T_{cold} = Q(Z_{th,hot}(s,\omega) - Z_{th,cold}(s+l,\omega)) \tag{2.1.8}$$

In this equation, l is the distance between the hot and cold junctions. Thus, the thermocouple's output voltage is given by (Eq. 2.1.1),

$$V_{ETF} = (\alpha_1 - \alpha_2)(T_{hot} - T_{cold}) \tag{2.1.9}$$

The above equations are for a single thermocouple. However, an ETF will employ many thermocouples whose thermal impedances will each contribute to the complete structure's characteristic. The output of the thermopile shown in Fig. 2.1 is a vector sum of all the thermocouple outputs given by Eq. 2.1.8 and Eq. 2.1.9.

2.1.3 **Effect of Scaling on ETFs**

A major source of inaccuracy in ϕ_{ETF} is the inaccuracy in *s*, which is determined by the lithography. At a given temperature and excitation frequency, this relation can be represented by

$$\frac{d\phi_{ETF}}{\phi_{ETF}} = -\frac{ds}{s} \tag{2.1.10}$$

Eq. 2.1.10 shows that for a fixed s, the percentage inaccuracy in ϕ_{ETF} reduces for smaller lithography since *ds* becomes smaller, i.e. processes with smaller feature sizes have more accurate lithography and thus, ϕ_{ETF} should become more accurate in scaled processes. This feature of ETFs was used in [15] to realize a temperature sensor with an inaccuracy of 0.2°C.

2.1.4 **ETF Design**

In this section, practical aspects of ETF design are discussed. Fig. 2.4 shows the cross section of an ETF. The heater is an n^+ diffusion resistor and the thermocouples are made from the ohmic contact between a p^+ diffusion resistors and metal interconnect. We will call such an ETF a silicon ETF, because its main heat diffusion path is through the silicon substrate.

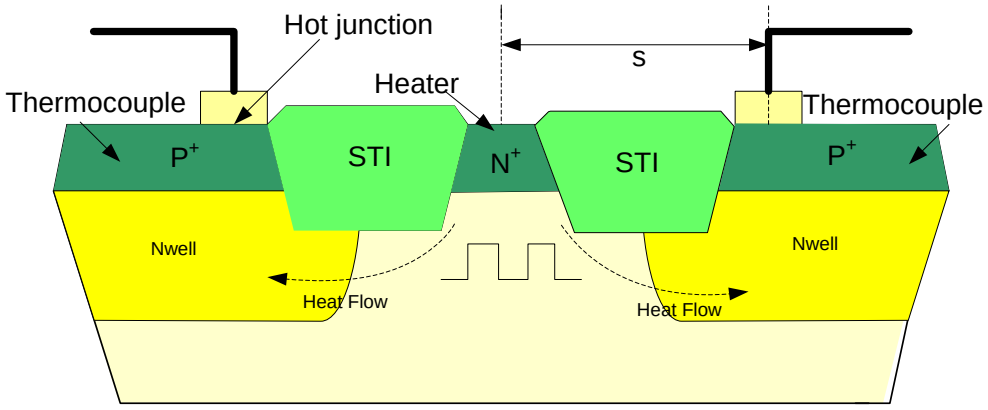

Fig 2.4- Cross-section of a silicon ETF

The top view of a silicon ETF is shown in Fig. 2.5. A 'U' shaped heater is used for better thermal efficiency [20]. Further, the thermocouples are placed on equi-phase contours around the heater such that their outputs contribute equally to the ETF output [20]. This configuration leads to greater SNR than the traditional bar structure used in [20] (shown in Fig. 2.3). An optimum length of the thermocouple arms can be determined since larger lengths lead to a larger signal (because the cold junctions are farther away) but also to more noise due to the increased resistance of the p^+ diffusion arms.

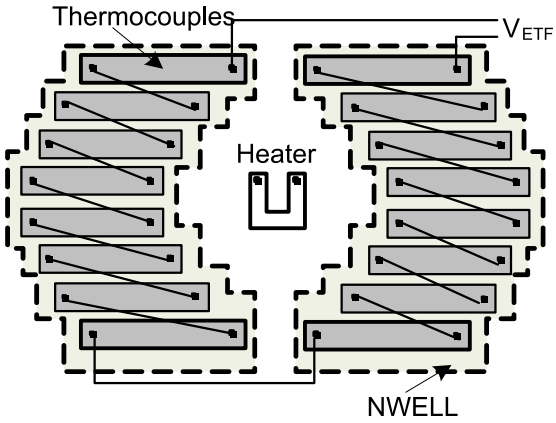

Fig 2.5- Top view of the ETF

In [9], a similar, but smaller, silicon ETF, with $\underline{s}$ = 4.7μm, has been used in a frequency reference. Fig. 2.6 shows the actual layout of the ETF. This ETF creates a phase shift of 54^0 at room temperature when driven by a square-wave at f_{drive} =1MHz.

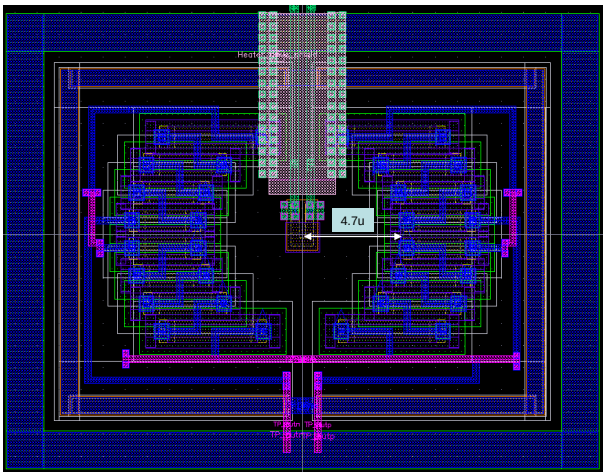

Fig 2.6- ETF Layout

2.2 **Electrothermal FLL**

As described in Chapter 1, an FLL can be created by locking the output frequency of a voltage-controlled oscillator (VCO) to the thermal delay of an ETF. Fig 2.7 shows a simplified block diagram of such an electrothermal FLL. It consists of an ETF in a feedback loop that comprises a synchronous demodulator, an integrator and a VCO. The output of the synchronous demodulator is proportional to the cosine of the ETF's phase shift. The FLL locks to the frequency at which the input of the integrator is zero i.e. thermal phase shift is equal to 90^0. Thus the frequency of the FLL is governed by the properties of the ETF alone and not those of the VCO. Any error in the ETF phase will cause an error in the output frequency given by (differentiating Eq. 2.1.5)

$$\frac{df}{f} = 2\frac{d\phi_{ETF}}{\phi_{ETF}} \tag{2.1.11}$$

In an ETF, the heat pulses have to travel through the silicon bulk which is a good conductor of heat. Therefore a lot of heat is dissipated in the silicon bulk before reaching the thermopile. For a few milli-Watts of heater power only a few hundred micro-Volts of signal is obtained at the temperature sensor output [10]. Further, the thermopile creates jitter as it is implemented using resistors (source of wide band thermal noise). This jitter is determined by the loop noise-bandwidth and the ETF's thermal noise contribution.

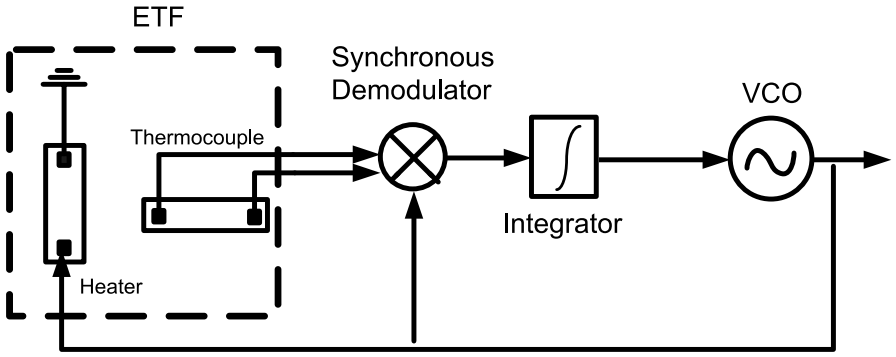

Fig 2.7- A simplified block diagram of an electrothermal FLL

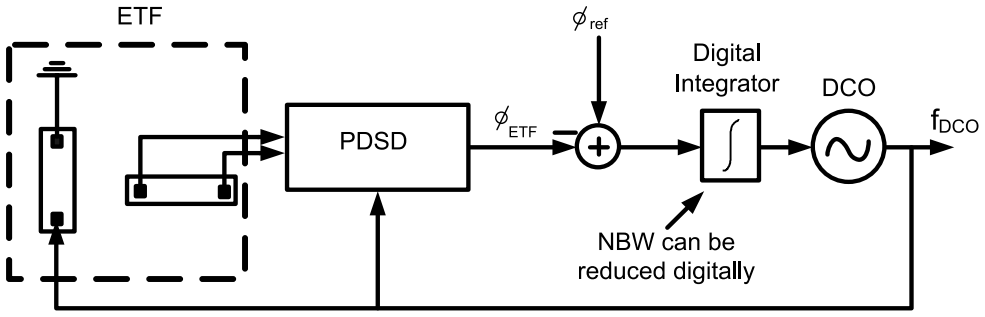

Fig 2.8- Block Diagram of a digitally assisted FLL loop

The loop bandwidth should be reduced to limit the thermal noise contribution of the ETF. If an analog integrator is used (as in Fig. 2.7) it would require a capacitor greater than 1μF to decrease the loop bandwidth to less than 0.5Hz [10]. Such a big capacitor cannot be integrated. To realize this loop bandwidth, in a more reasonable manner, a digital assisted loop is implemented (shown

in Fig. 2.8). The phase shift of the ETF is digitized using a ***Phase Domain Sigma Delta (PDSD)*** modulator. A PDSD is a 1st order sigma-delta ADC whose references are phase shifted versions of ETF driving frequency f_d (shown in Fig. 2.9).

The block diagram of the PDSD is shown in Fig.2.9. The ETF is driven at a frequency f_d and the output of the ETF is converted into current by a transconductor stage, g_m. This current is multiplied by either one of the phase shifted references $f_d(\phi_1)$ or $f_d(\phi_0)$ using a chopper demodulator. The output of the demodulator is either $\propto \cos(\phi_{ETF} - \phi_1)$ or $\propto \cos(\phi_{ETF} - \phi_0)$. The result is integrated and then quantized by a single bit quantizer running at f_S. At every clock cycle, the output of the quantizer decides whether $f_d(\phi_1)$ or $f_d(\phi_0)$ is used as the demodulating signal. The output of the PDSD is a bit stream whose average is equivalent to ϕ_{ETF}.

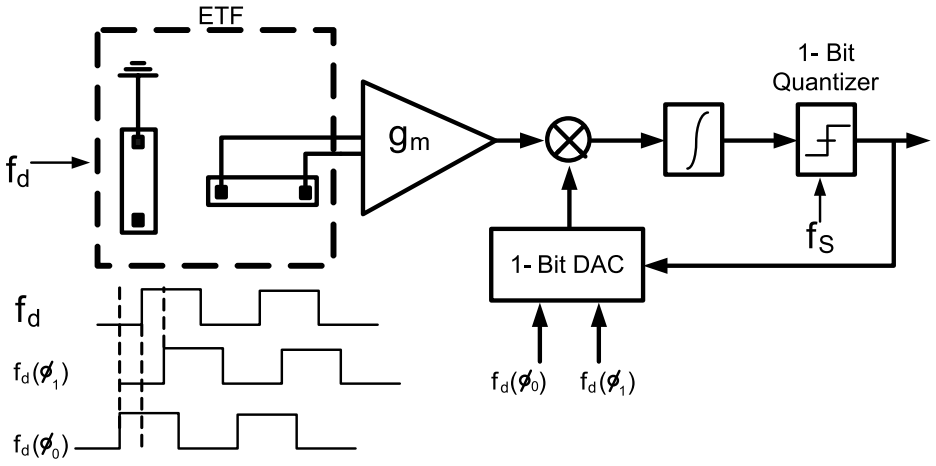

Fig 2.9- Block diagram of the PDSD [18]

In the digitally-assisted FLL, the output of the PDSD is compared to ϕ_{ref} and the result is integrated as shown in Fig 2.8. Since, ϕ_{ETF} is in digital domain, the loop phase reference and phase summation node are also implemented in digital domain. The output of the summation node is integrated by a digital integrator implemented by an up-down counter whose output then drives a digitally-controlled oscillator (DCO). Since the integrator is now implemented digitally therefore the loop bandwidth can be reduced to less than 0.5Hz without using an external capacitor.

2.3 TD frequency reference

It was noted in Section 2.1.2, that ϕ_{ETF} is a strong function of temperature (Eq. 2.1.7). Thus, temperature compensation is needed to create a stable frequency reference. Since, the difference of ϕ_{ETF} and ϕ_{ref} is integrated (Fig. 2.8), therefore the FLL locks to the frequency at which ϕ_{ETF} is equal to ϕ_{ref}. Now, it can be seen from Eq. 2.1.7 that for a constant driving frequency,

$\phi_{ETF} \propto -T^{0.9}$. Thus, ϕ_{ref} should also have exactly the same temperature dependence as ϕ_{ETF} for the loop to lock to a constant output frequency.

An on-chip ***PNP based temperature sensor*** is used to measure the temperature of the die. Two diode connected PNPs are biased at a current ratio of n:1. The difference between the base-emitter voltages of the two PNPs is equal to,

$$\Delta V_{BE} = \frac{kT}{q}\ln(n) \tag{2.1.12}$$

Where k is the Boltzmann's constant, q is the electron charge and T is the absolute temperature. This voltage is directly proportional to the absolute temperature and depends only on the current ratio of the diodes. Thus, it is an accurate measure of temperature. Further, ΔV_{BE} (PTAT) combined with V_{BE} (CTAT) can be used to create a temperature independent reference. Using these results, a temperature sensor can be created as shown in Fig. 2.10.

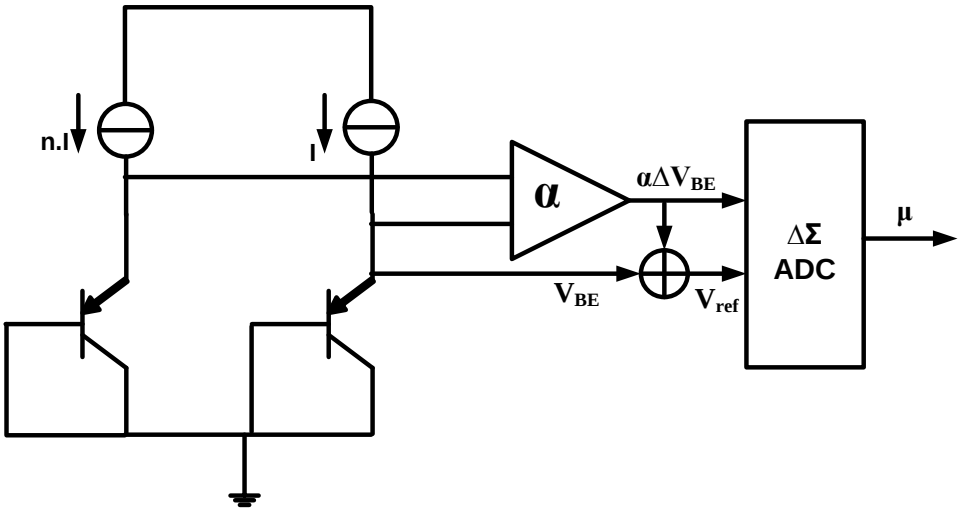

Fig 2.10- Block diagram of the TS [21].

The output μ of the charge balancing delta-sigma ADC is equal to:

$$\mu = \frac{\alpha\Delta V_{BE}}{\alpha\Delta V_{BE} + V_{BE}} \tag{2.1.13}$$

This is a digital representation of the die temperature. The major source of inaccuracy of the TS is due to the process spread of V_{BE} [21]. This can be corrected by a single PTAT trim [21] which is done by varying the bias currents of the diode connected PNP transistors (this is also called the fine trim in [21]).

Once the temperature information is obtained, it is mapped to a digital ϕ_{ref} .To begin with, a compensating polynomial is extracted which maps the die temperature to the phase reference

$\phi_{ref}(T)$. First, values of $\phi_{ref}(T)$ are experimentally determined such that the output frequency is exactly 16MHz. Then the Temperature Sensor (TS) is also characterized i.e. values of its output (μ) are measured at different temperatures. Based on these two sets of data, master curves (best fit lines) for the FLL and the TS are obtained. A fifth order polynomial is then derived from these master curves that maps μ to $\phi_{ref}(T)$, which is represented by a 15-bit number called a Frequency Control Word (FCW).

Without trimming, the spread of ϕ_{ETF} is in the order of ±1500ppm. This spread causes a frequency inaccuracy of ~±3000ppm (Eq. 2.1.11). Thus, the spread of ϕ_{ETF} is not tight enough to obtain reasonable frequency inaccuracy (<1000ppm), and must be trimmed. Furthermore, the spread in TS output also needs to be trimmed. As stated on the previous page, TS spread can be compensated by a single PTAT trim. Since the spread of ϕ_{ref} is also PTAT in nature, (Fig. 2.11), both sources of error can be effectively compensated by the same trimming knob.

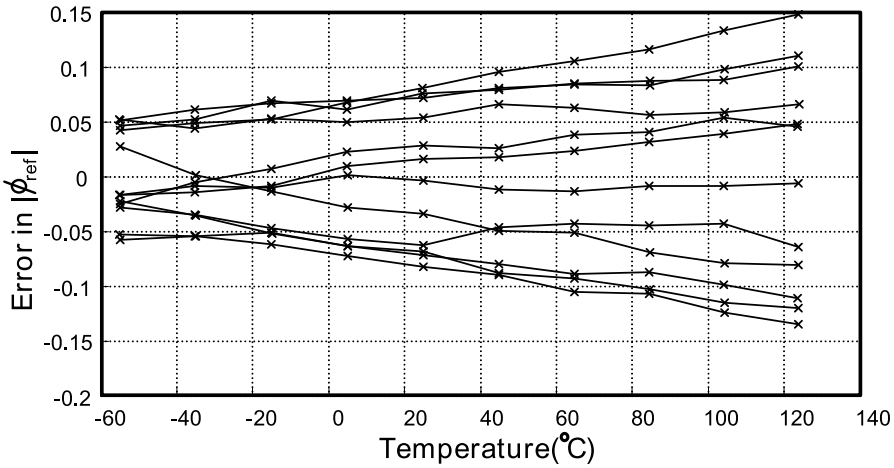

Fig 2.11- Untrimmed ϕ_{ref} error (Figure taken from [])

Fig. 2.12 shows the trimming algorithm. For each device, a fine trim word is applied to the TS. The output of the TS goes through the fifth order polynomial to give $\phi_{ref}(T)$. The FLL locks to a frequency corresponding to this $\phi_{ref}(T)$. The fine trim word applied to the TS is adjusted till the output frequency becomes 16MHz. The final fine trim word is stored and used for all temperatures for that particular device.

To prove the feasibility of TD frequency references, a first prototype was realized in a *0.7μm* CMOS process [10]. The area and power dissipation of the reference were 6.75mm^2 and 7.8mW respectively. The *s* (the distance between the heater and the temperature sensor) of the ETF was chosen to be ~24μm. A relatively large *s* is used to ensure that reasonable accuracy can be obtained albeit with larger jitter. This design achieved an absolute frequency inaccuracy of 1000ppm, with 1.6MHz output frequency, using a single temperature trim. Moreover, the cycle to cycle jitter of the reference was 400ps (rms).

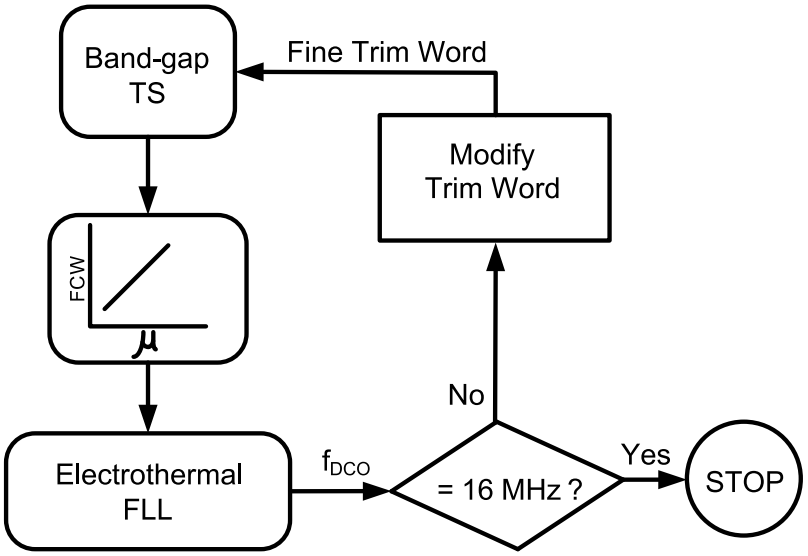

Fig 2.12- Algorithm for trimming the frequency reference

To see the effect of scaling a new reference was designed in a *0.16μm* standard CMOS process [9]. This employs a more accurate lithography. Thus, the ETF dimensions can be reduced while maintaining the same accuracy. Smaller ETF dimensions not only mean smaller *s* but also smaller thermopile sizes. These reductions lead to an increase in SNR which in turn leads to lower heater power and lower jitter. In comparison to the 0.7μm design, there was significant reduction in power, area and jitter of the reference, while the accuracy remained the same. Table 2.1 summarizes the performance of the two designs.

Technology	**0.16μm**	**0.7μm**
Frequency	16MHz	1.6MHz
Supply Voltage	1.8V	5V
Power consumption	2.1mW	7.8mW
Area	0.5mm2	6.75mm2
Inaccuracy	±1000	±1000
Period jitter	45ps	312ps

Table 2.1- Performance comparison of the two designs

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2.4 **Conclusion**

In this chapter, the system architecture of TD frequency references has been described in detail. Furthermore, a brief overview of the important components of the system such as the Electrothermal Filter (ETF, the Phase Domain Sigma Delta Modulator (PDSDM) and the Temperature Sensor (TS) was provided. It was shown that a previous design gained significant performance improvements by shifting to a more accurate lithography. Although many of the performance metrics improved in this 0.16 μm design, its inaccuracy remained at 1000 ppm. In the rest of this thesis, an attempt is made to improve accuracy and other performance metrics.

3 Characterization and Optimization of Silicon ETFs for TD Frequency References

This chapter discusses the performance limitations of TD frequency references based on silicon ETFs. Three different sized silicon ETF structures are compared to determine the one with the best performance in terms of accuracy and SNR. Section 3.1 provides an introduction to various parameters of silicon ETFs and their effect on the reference's output frequency. Section 3.2 discusses the increased spread of silicon ETFs and proposes various trimming strategies. Section 3.3 describes the implementation details of an improved TD frequency reference. The chapter is concluded in Section 3.4.

3.1 Introduction

In the previous chapter, the design of TD frequency references was outlined. Their accuracy is limited by the accuracy of the temperature compensation scheme, the resolution of the DCO and the initial accuracy of the ETF itself. In this chapter, an attempt is made to determine the ultimate accuracy of silicon ETFs. Moreover, the SNR at the ETF output is also of interest as it determines the reference's output jitter.

The behavior of an ETF was described as a function of its geometry, driving frequency and thermal diffusivity of silicon, under the assumption of single point heater and single point sensor. This description must be expanded to incorporate the complex geometry of a real ETF and to model its behavior over a wide temperature range.

The main cause of inaccuracy in a silicon ETF is limited lithographic accuracy. The resulting error decreases as the distance between the heater and TS (denoted by *s*) is increased. However, increasing *s* reduces the amplitude of the ETF's output voltage (V_{ETF}), since more of the heat will be lost to the silicon substrate (Eq. 2.1.4). This makes the reference more susceptible to errors from the readout circuit. Fig. 3.1 shows the effect of increasing *s*. Thus, there is an optimum value for *s* at which minimum system inaccuracy is obtained.

Similarly, as the ETF driving frequency, f_{drive}, increases, ϕ_{ETF} also increases (Eq. 2.1.5). But at the same time, V_{ETF} decreases due to the ETF's low pass characteristic (Eq. 2.1.4). Furthermore, the electrical phase-shift of the ETF and the readout circuit will also increase. Thus, there is an optimum value of f_{drive} such that the ETF accuracy is optimized.

From the above discussion, it is clear that the study of the performance of fabricated silicon ETFs with different values of *s* and f_{drive} is of interest. Therefore, the performance of three silicon ETFs with s=24μm, s=10μm and s=4.7μm has been evaluated at different driving frequencies. All three ETFs were fabricated on a single chip implemented in a 0.16μm CMOS process [9] (the chip was

designed by Mahdi). The ETFs are embedded in a TD frequency reference based on the design proposed in [9]. The design procedure for the three ETFs is the same as that described in Section 2.1.4.

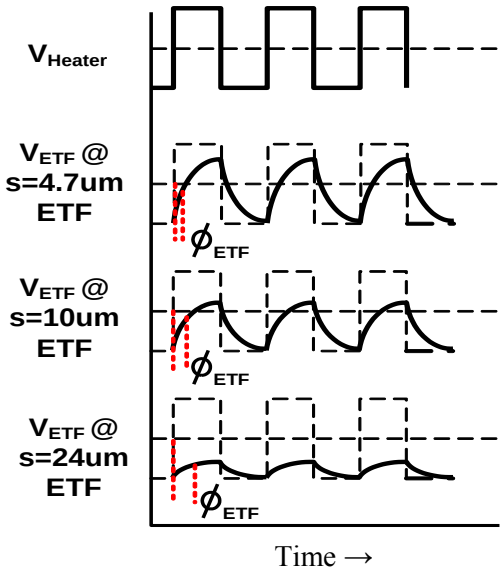

Fig 3.1- Effect of increasing s on V_{ETF}

3.2 Limits to the Performance of silicon ETFs

To evaluate the performance of the three ETFs, several measurements were performed over a wide temperature range. In this section, the measurement setup and the various results obtained from the measurements are described. The aim of the experiments was to find the values of *s* and f_{drive} that give the best performance in terms of accuracy and SNR. Further, the behavior of the silicon ETFs with temperature was measured in order to select the most suitable trimming scheme for the TD frequency reference.

3.2.1 Measurement Setup

The setup shown in Fig. 3.2 is used to measure ϕ_{ETF} . The ETF is driven at an excitation frequency of f_{drive} which is derived from a 16MHz crystal oscillator clock (XTAL). The XTAL oscillator output clock is divided down to ETF driving frequency using a FPGA. The FPGA also provides the lead (ϕ_0) and lag (ϕ_1) phase references for the Phase Domain Sigma Delta Modulator (PDSDM). Care is taken to ensure that the phase range ($\phi_1 - \phi_0$) is sufficient to cover the variation of ϕ_{ETF} over the entire temperature range. The setup is placed inside an oven for measurements across temperature. The output frequency is measured in steps of 20^0C starting from -55^0C up to 125^0C. Inside the oven, the chip is placed in good thermal contact with an aluminum block to prevent temperature fluctuations. Further, the temperature of the aluminum block is monitored using a calibrated platinum resistor temperature sensor known as PT100. This is calibrated to within 20 mK at the Dutch Institute of Metrology. ϕ_{ETF} is measured when the rate of change of temperature of the aluminium block has stabilized to below 0.005^0C/measurement

cycle. Along with the ϕ_{ETF} measurement, the corresponding temperature is also stored for calibration.

The post-processing on ϕ_{ETF} data is done using Labview program. To ensure that thermal noise has minimal effect on the final result, the stored value of ϕ_{ETF} is the average of 130768 samples[2]. This corresponds to a measurement time of approx. 3 sec.

The same setup can also be used to measure the noise in ϕ_{ETF} . A number of samples of ϕ_{ETF} are measured at a particular temperature. The variance of ϕ_{ETF} can be calculated from this data and is equal to

(3.1.1)

$$\langle \emptyset_{ETF} \rangle = \emptyset_n \sqrt{Bw}$$

where ϕ_n is the thermal phase noise floor and Bw is the noise bandwidth of the filter.

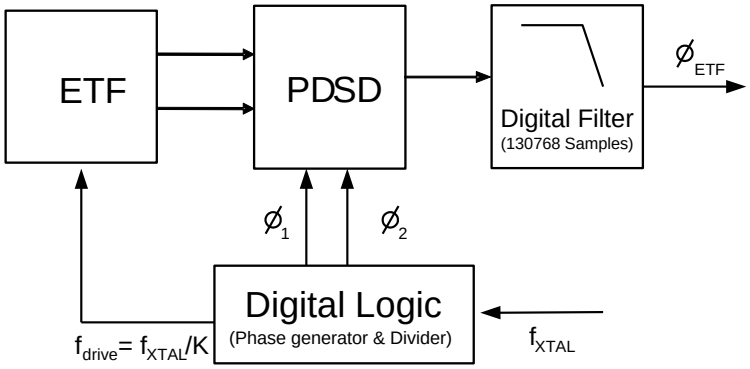

Fig 3.2- Measurement setup for ϕ_{ETF}

3.2.2 **Limit to accuracy due silicon ETFs and the readout**

The data obtained from the measurement setup is used to investigate the limits of the accuracy of the resulting TD frequency reference. In Chapters 1 and 2, it was mentioned that the inaccuracy of a TD frequency reference is limited by the accuracy of temperature compensation. But even if the temperature sensor was ideal, there would be inaccuracy due to the ETF itself. This section examines error sources inherent to the silicon ETF.

The spread of ϕ_{ETF} is mainly determined by the following factors:

a) *Inaccuracy of lithography*.

b) *Electrical phase shift* due to the limited bandwidth of the ETF's parasitic electrical filtering and the demodulator.

[2] Ideally more samples would give more accurate results. But it was not possible to increase the number of samples as the software crashes on increasing the number of samples beyond 130768.

c) *Residual offset and leakage currents* are DC errors which directly add to the output of the synchronous demodulator.

The errors due to elements (b) and (c) mentioned above have been reduced by proper design of the readout circuit [9]. Thus, most of the remaining error comes from lithographic inaccuracy.

To study the spread of the error in ϕ_{ETF} , the three ETFs were measured at 10 equi-spaced temperature points from -55^{0}C to 125^{0}C. The ETFs are driven at the corresponding optimum drive frequencies (at which maximum SNR is obtained as shown in Appendix A). The drive frequencies are as follows: 85 KHz for s=24μm, 256 KHz for s=10μm and 512 KHz for s=4.7μm.

Fig. 3.3 (a) shows the ϕ_{ETF} variation with temperature for the three ETFs. Figs. 3.3 b, c and d show the untrimmed error in ϕ_{ETF} for the three ETFs. It should be noted that the ϕ_{ETF} errors in these figures show considerable temperature dependence (except for s=4.7μm). However, the error due to lithography is given by Eq. 2.1.10 ($\frac{d\phi_{ETF}}{\phi_{ETF}} = -\frac{ds}{s}$) and therefore should show no temperature dependence. The reason for this behavior has not been established.

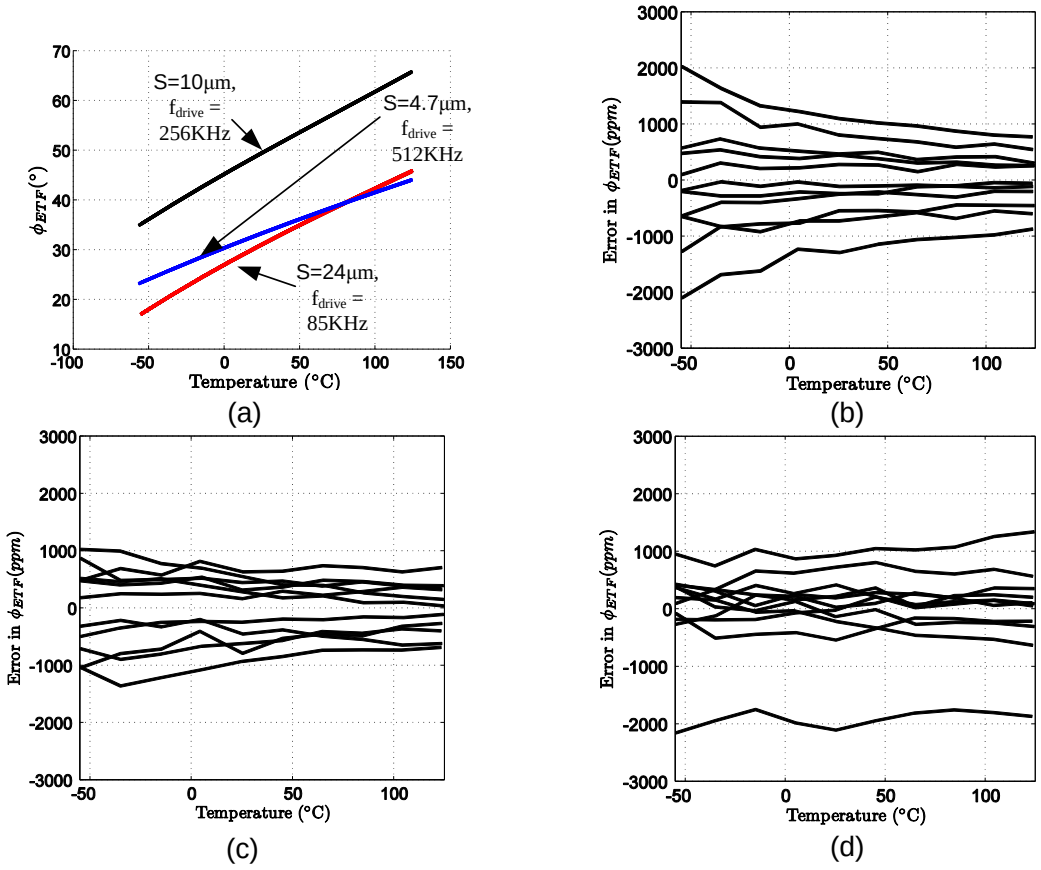

Fig 3.3- Untrimmed error in ϕ_{ETF} (in ppm) for (a) ϕ_{ETF} vs. Temperature for the three ETFs

(b) s=24 μm (c) s=10 μm (d) s=4.7 μm

As discussed in chapter 2, ϕ_{ETF} should be trimmed to obtain final frequency accuracy. To emphasize this point, consider the ϕ_{ETF} error shown in Fig.3.3 a. The error at -55^{0}C is ~2000ppm. This error translates to ~4000ppm error in frequency output ($\frac{df}{f} = 2\frac{d\phi_{ETF}}{\phi_{ETF}}$). Thus, the limit to the frequency accuracy is determined by how well the error in ϕ_{ETF} can be trimmed. If the error has a well defined temperature characteristic then it would be possible to trim it out completely. But as can be seen from Fig 3.3, the ϕ_{ETF} error shows temperature dependence which limits the effectiveness of trimming. Nevertheless, different trimming strategies can be used to compensate for different types of errors (this point will be elaborated later in this section).

To see the effectiveness of trimming strategies and hence investigate the performance of silicon ETF, three trimming strategies are compared. They are a) *Slope trim* b) *Offset trim* c) *Two temperature trim*. These are explained in the following sub-sections and the performance of the three ETFs vis-à-vis the trimming strategies is compared.

3.2.2.1 Slope Trim[3]

This is a single temperature trim. For each device, the ϕ_{ETF} curve is multiplied by a trim factor *m* such that the error becomes zero at the trim temperature.

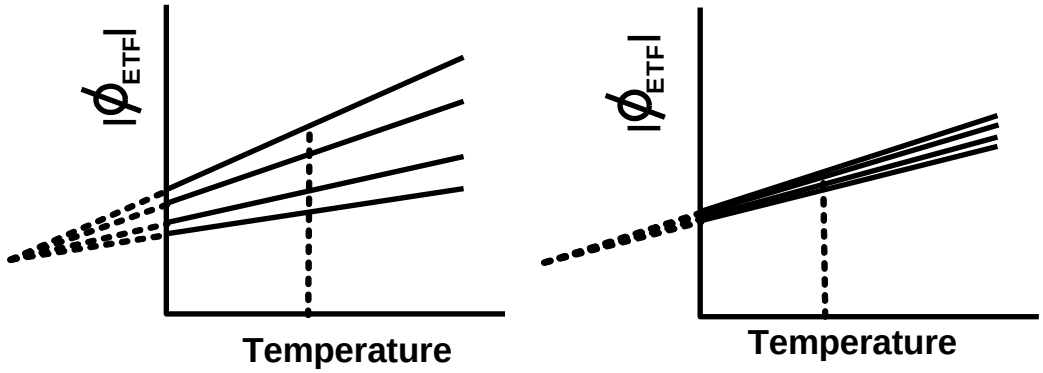

Fig 3.4- The principle of slope trim

A graphical representation of the principle of slope trim is shown in Fig 3.8. The slope trim works perfectly if the all the ϕ_{ETF} curves intersect at absolute zero. In this case, limited trimming resolution is the only remaining error as shown in Fig 3.4. The slope trim is performed on the three ETFs. The residual error after trimming is shown in Fig. 3.5. The maximum residual errors over temperature are summarized in Table 3.1. As can be seen from the table even if an electrothermal FLL is built around the ETF with s=10μm, no better than ±600ppm (1σ) ($\frac{df}{f} = 2\frac{d\phi_{ETF}}{\phi_{ETF}}$) frequency inaccuracy can be obtained with the slope trim. Here it is assumed that the TS and the DCO are ideal

[3] This is same as PTAT trim used in [10]

S	Maximum error in ϕ_{ETF} (1σ) over temperature
24 µm	±1000ppm
10µm	±300ppm
4.7µm	±500ppm

Table 3.1 - Maximum error in ϕ_{ETF} over temperature for the three ETF.

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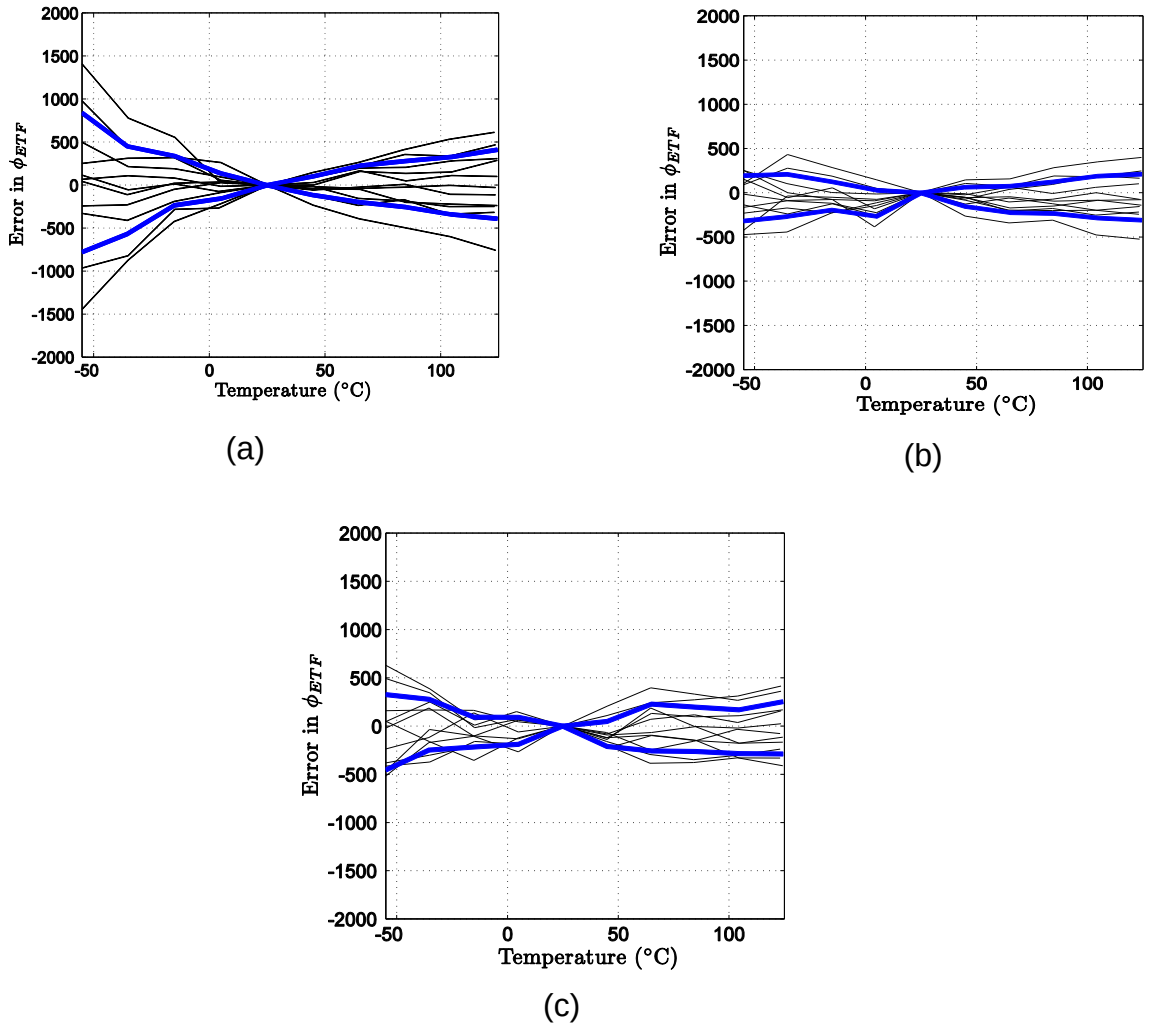

Fig 3.5- Residual error in (in ppm), after slope trim, for (a) s=24 µm (b) s=10 µm (c) s=4.7 µm

One of the advantages of slope trim is that it can be simply implemented via the TS. A PTAT trim mechanism has been implemented in the TS of previous TD frequency references [9][10]. This technique has been used to trim both the silicon ETF and the TS using the same trimming knob

3.2.2.2 Offset trim

This is also a single temperature trim. In this trim, an offset *C* is added to the ϕ_{ETF} curve of each device such that the error becomes zero at the trim temperature.

A graphical representation of the offset trim is shown in Fig 3.6. The residual error after trimming is shown in Fig. 3.7. The maximum residual errors over temperature are summarized in Table 3.2. Thus, if an electrothermal FLL is built around the ETF with s=10μm then, no better than ±600ppm inaccuracy (1σ) can be obtained with offset trim.

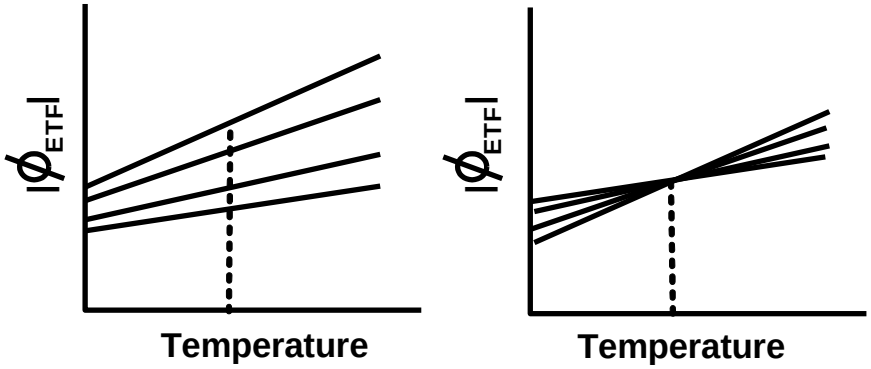

Fig 3.6- Principle of offset trim

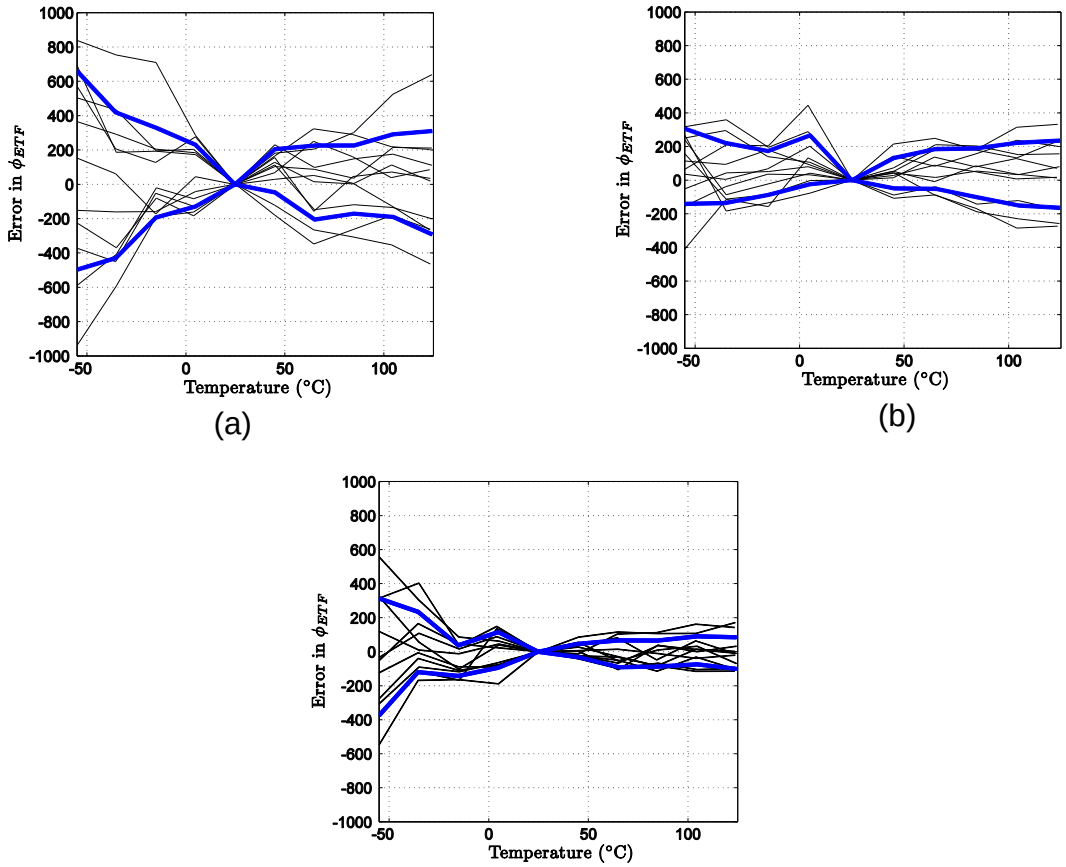

Fig 3.7- Residual error in (in ppm), after offset trim, for (a) s=24 μm (b) s=10 μm (c) s=4.7 μm

S	Maximum error in ϕ_{ETF} (1σ) over temperature
24 μm	±800ppm
10μm	±300ppm
4.7μm	±400ppm

Table 3.2- Maximum error in ϕ_{ETF} over temperature for the three ETF.

These conclusions about frequency spread assume an ideal temperature sensor. In reality the TS has additional error due to its residual non-idealities compared to the inherent PTAT spread expected from a band-gap TS [21]. Thus, to obtain lower levels of inaccuracy, trim applied to a TD frequency reference will be more effective if it is performed in two steps. First, a multiplicative trim/PTAT trim (described in Chapter 2 Section 2.3) should be applied to the TS output. This is equivalent to the slope trim. Now, with the TS trimmed, an offset trim can be applied to compensate for ϕ_{ETF} error as described in this section

3.2.2.3 Two temperature trim

As seen from the previous two sections, the frequency inaccuracy (only due to the silicon ETF) is limited to ±600ppm if a single temperature trim is used. It would be interesting to see if better accuracy can be achieved with a two temperature trim.

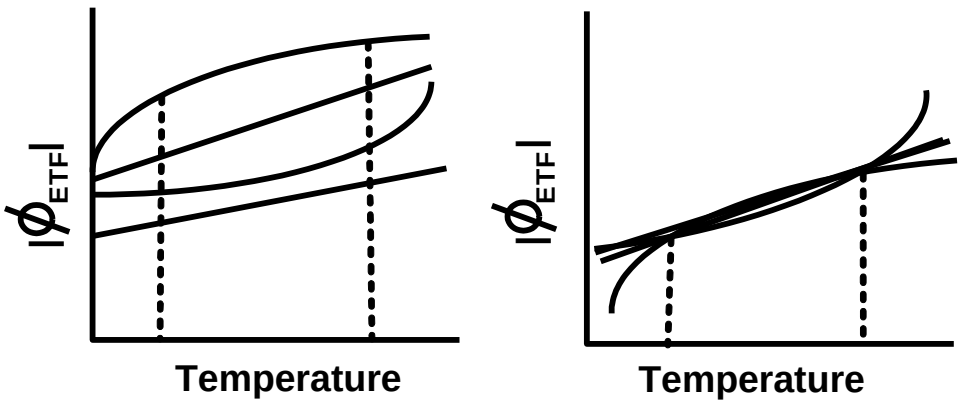

Fig 3.8- Principle of two temperature trim

A two temperature trim is a combination of a slope and an offset trim. A multiplying factor *m* and an offset *C* are applied to ϕ_{ETF} curve of each device such that the error becomes zero at the two trim temperatures.

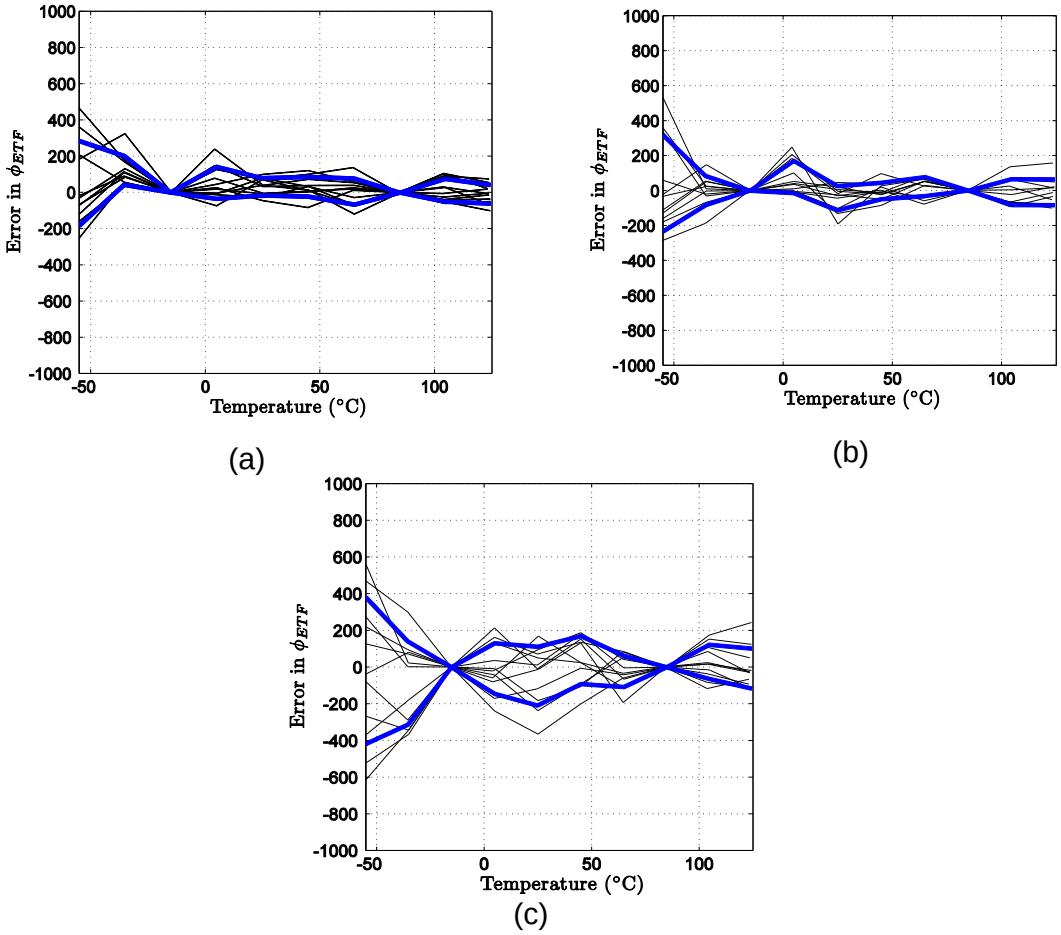

Fig 3.9- Residual error in (in ppm), after two temperature trim, for (a) s=24 μm (b) s=10 μm (c) s=4.7 μm

A graphical representation of the two temperature trim is shown in Fig 3.8 and the residual error after trimming is shown in Fig. 3.9. The maximum residual errors over temperature summarized in Table 3.3. Thus, it would be only possible to achieve ±400ppm (-35^{0}C to 125^{0}C) of frequency inaccuracy with the silicon ETFs (s=10μm ETF) even after a two temperature trim. This results shows that it is possible to build a more accurate frequency reference (in comparison to ±1000ppm accuracy achieved in [9][10]) using this trim.

s	Maximum error in ϕ_{ETF} (1σ) over temperature
24 μm	±300ppm
10μm	±300ppm (±200ppm for all temperatures except -55^{0}C)
4.7μm	±400ppm

Table 3.3- Maximum error in ϕ_{ETF} over temperature for the three ETF.

The reason for the large error at -55^{0}C was not established at the time of measurements. Later, it was found that this oven needed maintenance and so was rather unstable at -55^{0}C

3.3 A more accurate frequency reference

In the previous sections, it is established that a silicon ETF with s=10μm gives the best accuracy after trimming. Further, a two temperature trim results in less inaccuracy. In this section, this result is used to implement a more accurate silicon ETF based frequency reference.

The aim of the experiment, described in this section, is to find the limit to which the frequency inaccuracy of silicon-ETF-based references can be reduced in practice.

The ETF with s=10μm was embedded in an electrothermal frequency-locked-loop, described in Section 2.2 and shown in Fig 2.8. The digital integrator block and digital logic are implemented in a FPGA. The DCO is implemented on chip and resembles the one in [9]. The FLL must be calibrated for temperature compensation using the procedure described in Section 2.2.

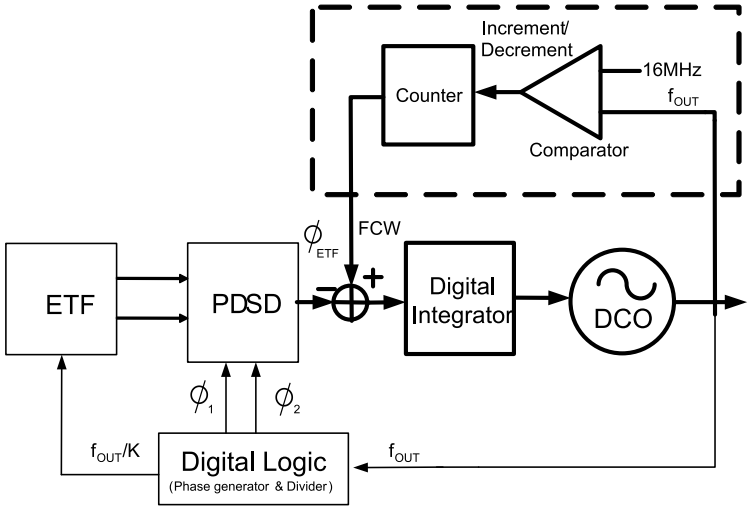

Fig 3.10- Measurement setup for characterizing ϕ_{ref} . The portion enclosed in the dotted line is implemented in software (Labview)

Measurements of 12 devices, over the military temperature range, are used for calibration. For each device, ϕ_{ref} (FCW) is measured such that the DCO output frequency is equal to 16MHz. The temperature is also recorded, at this point, using a PT100 temperature sensor. The characterization set-up is implemented in Labview (shown in Fig 3.10). The output frequency is measured using a keithley and the result is compared to 16MHz which is the desired output frequency. Depending on the outcome of the comparison, the FCW is either incremented or decremented using a counter. It should be ensured that the gain of the characterization loop (enclosed within the dotted lines), at the measurement frequency, is enough so that the gain error in the measured FCW is less than 100ppm. An integrator gain of 16 was found to be enough for this system.

The on-chip Band-Gap TS is also characterized for 12 devices. From this data, a 5th order polynomial is extracted that maps μ (output of TS) to ϕ_{ref} . Once this mapping is obtained, the devices can be trimmed with respect to the PT100.

The two-temperature trimming procedure used in this work is shown in Fig. 3.11. Since a two temperature trim is being applied to the silicon ETF, the temperature sensor is also trimmed at two temperatures. To trim a particular device, ϕ_{ref} and μ (TS output) are measured at around -15^{0}C and 85^{0}C (here again, ϕ_{ref} is measured such that the DCO frequency is 16MHz). First, the TS is trimmed with respect to PT100 using the two data points. Parameters a and b (Fig. 3.12) are calculated to correct for the slope and offset error of the TS. These parameters are applied to the temperature sensor output to obtain μ'.

Further, ϕ_{ref} is also trimmed with respect to PT100. But in this case the trim is applied through the TS output using the mapping from μ (TS output) to ϕ_{ref}. Parameters m and c are calculated such that ϕ_{ref} error becomes zero at the two temperature points. These parameters are applied to μ' to obtain μ'' (Fig.3.12).

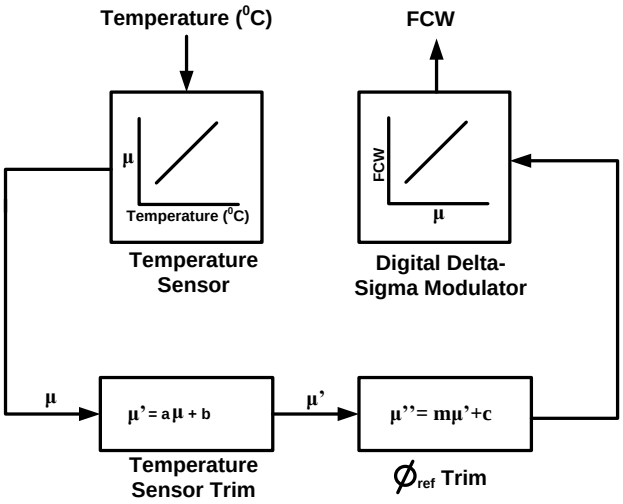

Fig 3.11- Trimming strategy for two temperature trim

Instead of the above trimming procedure, ϕ_{ref} can be directly trimmed with respect to μ without involving PT100. However, in this thesis, the TS output μ is trimmed with respect to PT100 to obtain useful information about the absolute accuracy of the TS.

Once the trimming parameters are defined, the devices are put inside an oven for measurements across temperature. The output frequency is measured in steps of 20^{0}C starting from -55^{0}C up to 125^{0}C. Fig. 3.12 shows the frequency errors from the desired 16MHz for 16 devices. An absolute frequency inaccuracy of ±600ppm is obtained except at -55^{0}C. As stated earlier, the reason for the large error at -55^{0}C was not established at the time of measurements. Later, it was found that this oven needed maintenance and so was rather unstable at -55^{0}C. Fig. 3.13 also shows the TS error for reference.

The limitation on accuracy in this implementation comes from the following:

a) Error in TS output (shown in Fig. 3.13)

b) Limited DCO resolution: The DCO resolution was measured to be 1LSB ~ 250ppm. Thus, it can cause a frequency error of ½LSB = 125ppm at each measurement point.
c) The DCO used is similar to the one used in [9]. The jitter reported for that DCO is 45pS (720ppm). The frequency is measured 65 times and the average is used for determining the frequency accuracy. Thus, a 720ppm of jitter can cause $720/\sqrt{65}$ ~ 90ppm of frequency error.
d) As established in Section 3.2.2.3, the silicon ETF can itself cause ±400ppm (-35^{0}C to 125^{0}C) of error in frequency.

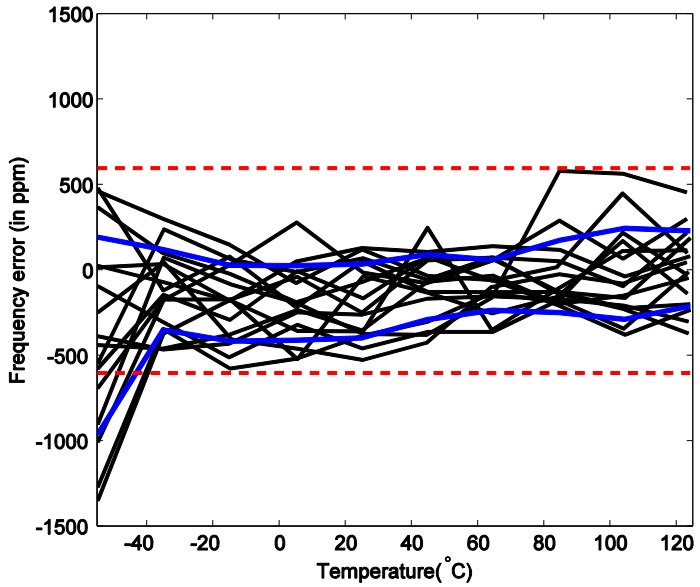

Fig 3.12- Frequency inaccuracy for silicon ETF with s=10μm. Blue lines are lines. Red lines denote ±600ppm limit

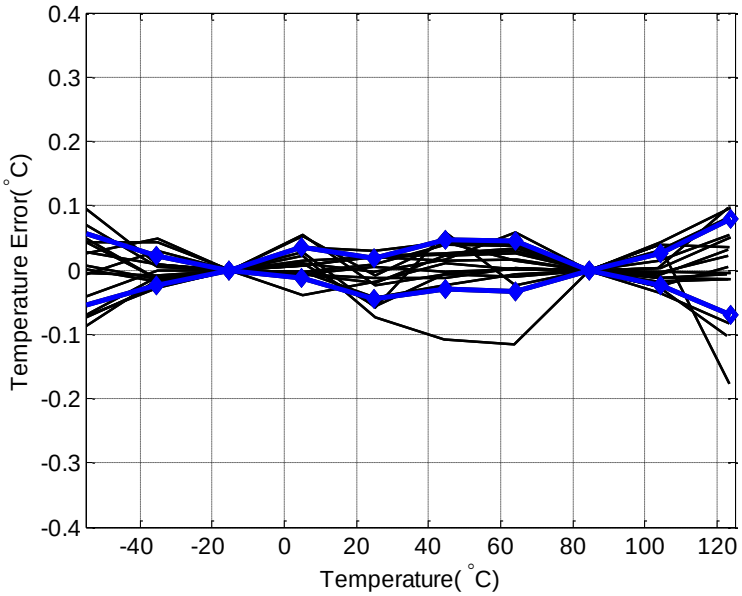

Fig 3.13- Two temperature trimmed TS error. Blue lines with diamond point makers are lines

3.4 **Conclusion**

In this chapter, the accuracy limits of the silicon ETF are studied. Measurements are performed on silicon ETF to find the optimum *s* and f_{drive} for maximum accuracy. Furthermore, various trim strategies are implemented to get the best possible accuracy. It was found that a silicon ETF can achieve an accuracy of ±400ppm (-35^0C to 125^0C) with a two temperature trim.

An electrothermal FLL was implemented using the ETF with s=10μm and driven at 256 KHz and a two-temperature trim strategy was applied. An absolute accuracy of ±600ppm was achieved over the temperature range of -35^0C to 125^0C. In comparison, earlier work [9][10] achieved absolute inaccuracy of ±1000ppm over the temperature range from -55^0C to 125^0C.

4 A Frequency Reference Based on an Oxide ETF

One of the major contributors to the inaccuracy of TD frequency references is the temperature sensor. The inaccuracy of the sensors used in the previous works was about 0.1^{o}C which limits the frequency accuracy to 800ppm. This work intends to improve the frequency accuracy to less than 500ppm. To achieve this goal, a new ETF structure based on silicon-dioxide (will be referred to as oxide ETF) is presented. Such an oxide ETF makes the phase shift of the ETF, and thus the frequency error of the reference, less sensitive to temperature. Section 3.1 describes the effect of limited TS accuracy. Section 3.2 describes the structure, properties and advantages of the oxide ETF. Section 3.3 presents the implementation details such as the layout and various issues related to it. The chapter is concluded with measurement results presented in Section 3.4

4.1 Introduction

As discussed in the earlier chapters, the output frequency of an electrothermal FLL is strongly temperature dependent. To build a frequency reference, an on-chip Temperature Sensor (TS) is used to compensate for this temperature dependence. This can be done by translating the temperature information at the output of the TS to a temperature dependent phase reference for the FLL. Any temperature sensing inaccuracy will directly translate to a phase error and hence contribute to the inaccuracy of the output frequency. As can be seen from Fig. 4.1, an inaccuracy of less than 0.05^{0}C is required to obtain better than 400ppm of frequency inaccuracy.

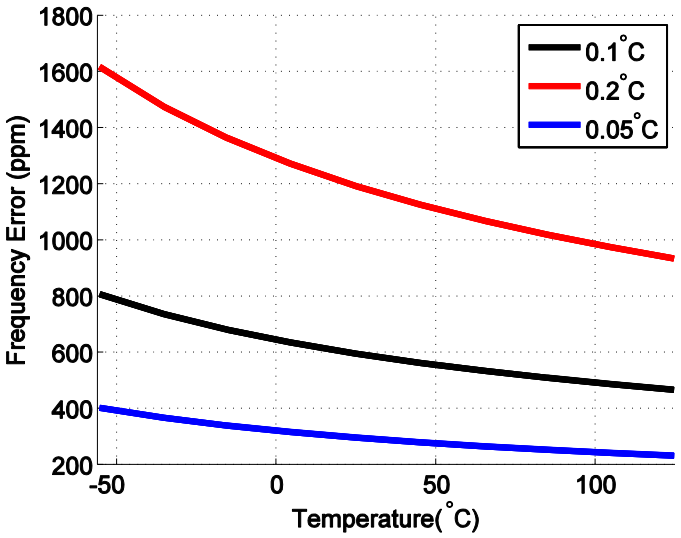

Fig 4.1- Frequency error for various temperature sensor inaccuracies

Thus, to obtain a more accurate frequency reference, either the temperature sensor should be improved or the temperature sensitivity of ϕ_{ETF} has to be reduced. The state-of-the-art integrated temperature sensors available in literature have accuracy greater than 0.05^0C [24] (achieved by means of a two temperature trim). Improving the accuracy of integrated temperature sensors is an area of active research that falls out of the scope of this thesis. Here, the second option i.e. to reduce the temperature sensitivity of ϕ_{ETF} has been explored.

4.2 Structure of an Oxide ETF

As explained in the first chapter, the thermal diffusivity of a material is given by,

$$D = \frac{k}{\rho c_p} \tag{4.1.1}$$

Where k is the thermal conductivity, ρ is the density and c_p is the specific heat capacity of the material. The temperature sensitivity of ϕ_{ETF} is mainly due to the temperature dependence of thermal conductivity of silicon. The thermal conductivity of silicon-dioxide has a much lower temperature coefficient than that of a bulk silicon [22][23]. Therefore, an ETF that uses silicon dioxide for creating thermal delay should have a lower temperature coefficient. The following subsections discuss two possibilities for building such an ETF.

4.2.1 ETF: Dual heater - p^+ diffusion thermocouple

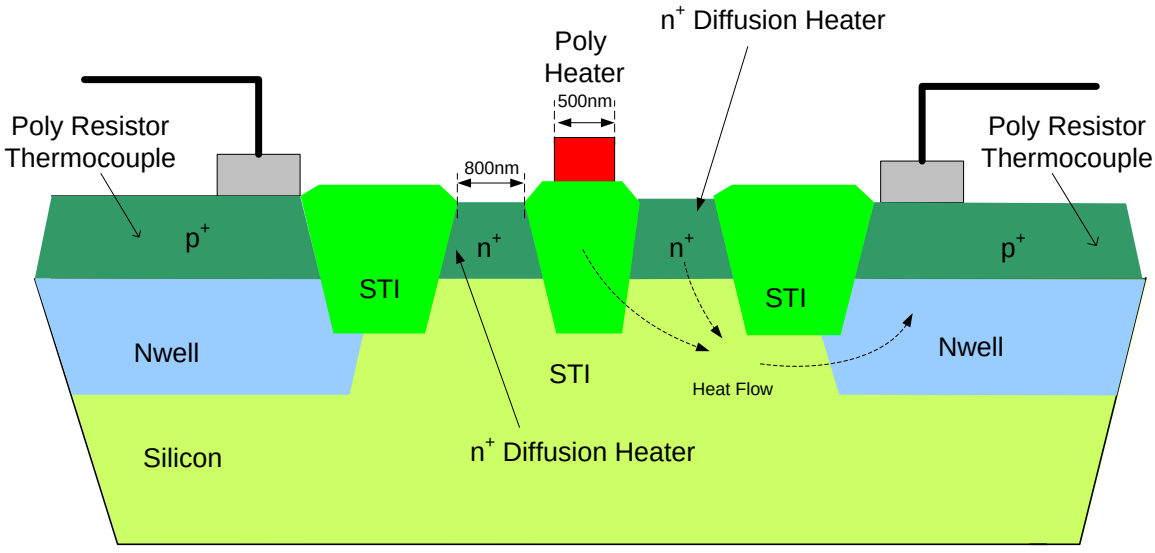

Fig 4.2- Cross-section of the ETF comprising of dual heater (polysilicon heater and p+ diffusion heater) – p+ diffusion thermocouple.

This structure, shown in Fig. 4.2, consists of a dual heater i.e. one polysilicon (resistor) heater and one n^+ diffusion heater [9]. The thermocouples are the same as in silicon ETF (p^+ diffusion resistors). In the first cycle, a voltage pulse is applied only to the polysilicon heater. The heat

pulse travels through both STI (Shallow Trench Insulator) and silicon to reach the thermocouples. Thus the phase delay obtained at the output is due to both silicon dioxide and silicon. In the second cycle, a voltage pulse is applied only to n^+ diffusion heater. Now, the phase delay at the output is only due to silicon. As can be seen from the cross-section, the silicon path is nearly the same for both cycles. Therefore, the difference between the phase delays, obtained from the two cycles, gives the phase delay associated with the oxide. A major drawback of this structure is the added complexity in realization of the frequency locked loop due to the two cycles of operation. Moreover, the division of thermal delay between silicon and oxide will vary from device to device because the temperature characteristics of both the materials are different due to lack of correlation between their physical properties. This could potentially result in *untrimmable* errors. Furthermore, the power consumption will remain similar to silicon ETF.

4.2.2 **ETF: Poly silicon heater - p+ diffusion thermocouple**

Fig. 4.3 shows a detailed structure of this ETF with annotated dimensions. This structure has a polysilicon heater and p^+ diffusion thermocouples. A pulse is applied to the terminals of the poly silicon (resistor) heater. The heat pulse travels through STI to reach the hot junction of the thermocouple. To minimize the thermal path through the silicon, it is ensured that thermocouples are as close to the heater as possible. As will be seen from the measurement results in Section 3.5.1, the thermal path is not purely through the oxide. The pulse that reaches the cold junction has to traverse through the silicon bulk and has a significant impact on the final temperature coefficient of the ETF phase output.

Another advantage of this ETF is its lower power consumption. Since silicon is a good conductor of heat, the silicon bulk acts as a heat sink. In the silicon ETF, shown in Fig. 2.1, a significant portion of the heat is lost in the silicon bulk before it reaches the thermocouples. Whereas, the ETF shown in Fig. 4.4 is a 'packed' structure i.e. the thermocouples are very close to the heater.

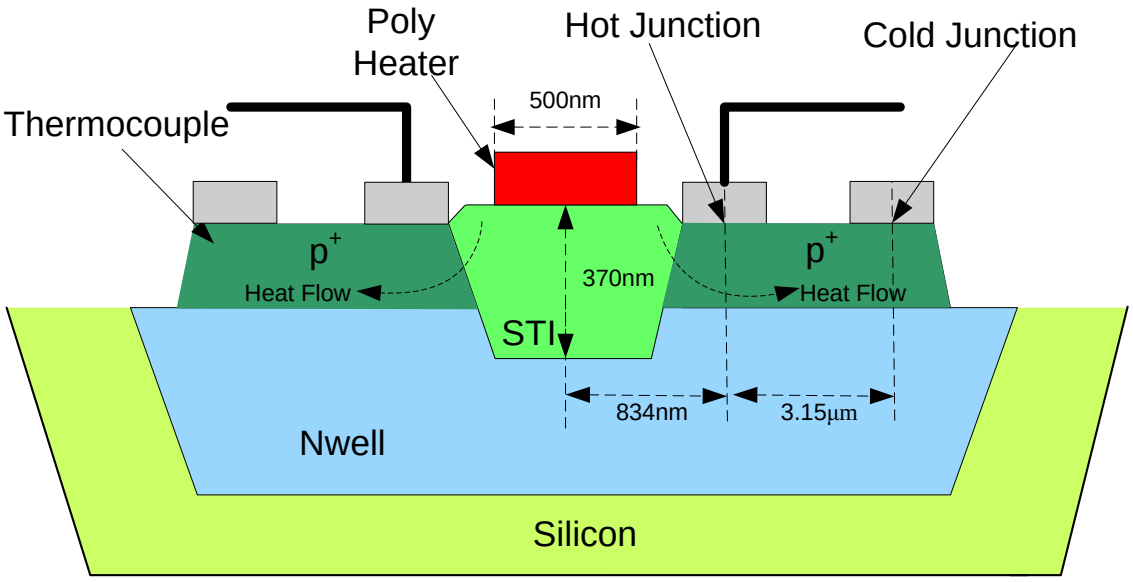

Fig 4.3- Cross-section of oxide ETF comprising of poly silicon heater – p+ diffusion thermocouple

Thus, a much larger portion of the heater power (in comparison to silicon ETFs) reaches the thermocouples. It is therefore expected that much lower power would be required for same SNR as silicon ETF.

Since, the ETF described in this section has a thermal delay that is due to both oxide and silicon therefore its temperature coefficient is expected to be lower than that of a silicon ETF. Furthermore, due to the lower level of power consumption expected from it, this has become the oxide ETF[4] structure of choice for this work.

4.3 Implementation Details

4.3.1 Layout: Placement and Routing Strategy

In an ETF, it is intended that most of the signal travels, in the form of heat, through the silicon/oxide to reach the thermocouples. But some of the signal, at the heater, is also coupled directly to the thermocouples, due to capacitive coupling or through the substrate. The direct coupling of the signal causes errors in phase output as it is demodulated to DC by the synchronous demodulator.

In [15], a heater drive inversion mechanism (HDI) has been proposed, which periodically reverses the polarity of the heat generating pulse across the heater resistor. This will have no effect on the generated heat, however results in alternatively changing polarity of the capacitively coupled spikes to the thermopile. As a result the net average effect of the spikes will be cancelled. Although the HDI technique does mitigate this problem yet it is beneficial to reduce the initial amplitude of the spikes.

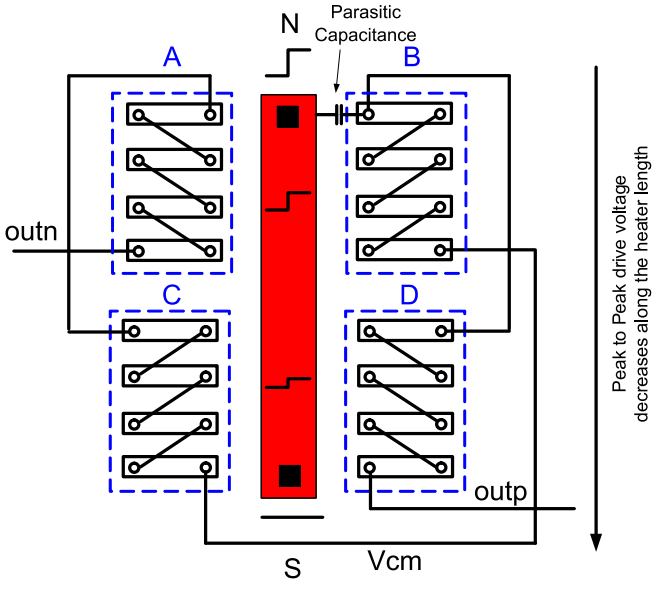

Fig 4.4- Standard layout strategy for silicon ETF

[4] The name oxide ETF is a misnomer as the thermal delay is due to the oxide path as well as the silicon path.

The coupling issue is particularly severe in case of an oxide ETF, since the thermocouples and the heater are placed close to each other (0.834µm in comparison to > 4.7µm in the previous silicon ETFs). Fig. 4.4 shows the layout strategy of the previous silicon ETFs. This layout leads to a symmetric routing which reduces its capacitive coupling with the heater. In the case of the oxide ETF, the thermocouples are placed close to the heater. The parasitic capacitance between the heater and the p^+-metal1 contact at the hot junction of the thermocouple is relatively large and leads to differential spikes of greater than 200µV (in comparison the silicon ETF used in [9] shows less than 50µV spikes).

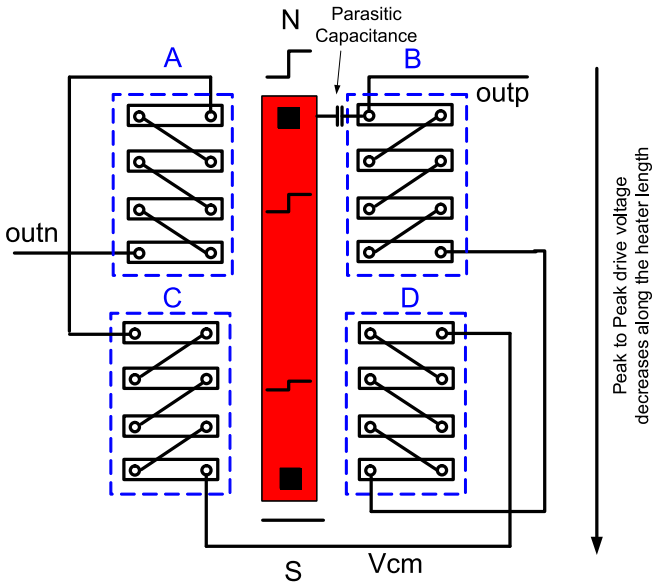

Fig 4.5- Revised layout strategy for silicon ETF

Symmetric routing cannot reduce this coupling as can be seen in Fig. 4.4. Let us assume that the heat signal is applied at N side of the heater. The peak to peak voltage of the signal decreases along the heater length until finally it becomes zero at the S side. Now, *outn* is taken out from quadrant A whereas *outp* is derived from quadrant D. Since, quad A is closer to side N than quad D, therefore *outn* suffers much more coupling, to the heater drive signal, than *outp*. It should be noted that the ETF used in previous works had a U-shaped heater and therefore the standard layout strategy works well in that case. Fig. 4.6 shows the differential spike voltage at the output

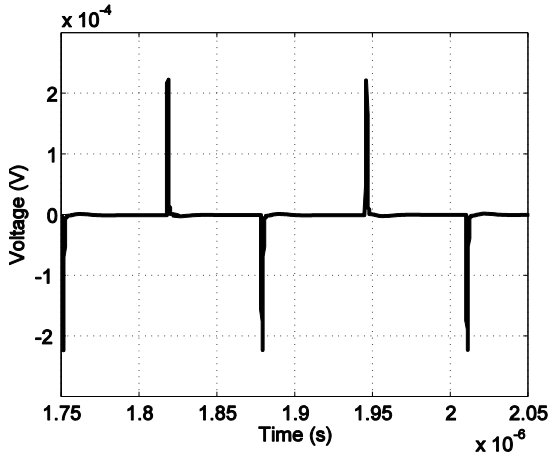

Fig 4.6- Differential spike voltage at the ETF output for layout strategy given in Fig. 4.4

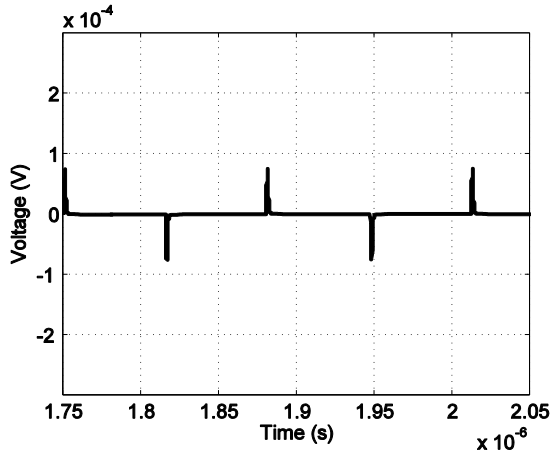

Fig 4.7- Differential spike voltage at the ETF output for layout strategy given in Fig. 4.5

To counter this issue, the placement is done as shown in the Fig.4.5. Now, both *outn* and *outp* are closer to side N as they come out of quad A and quad B respectively. The differential spike voltage is now reduced as shown in Fig. 4.7 (an reduction of around 3X is obtained).

4.3.2 **Electrical Phase Shift**

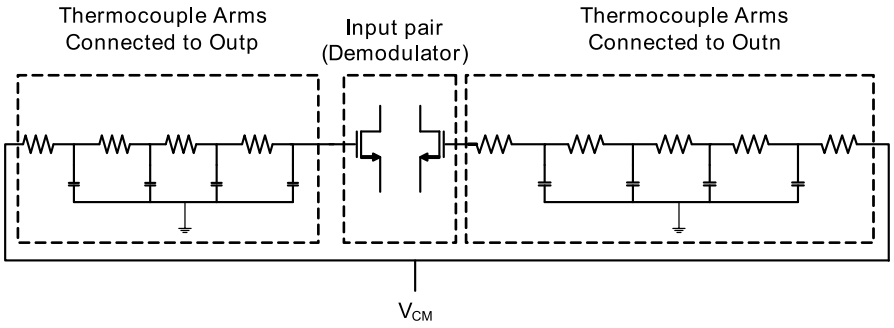

Fig 4.8- Electrical model of ETF

Although an ETF is used as a thermal filter, but it also acts as an electrical filter adding excess phase shift to the thermal phase of the filter. This is mainly because of the parasitic coupling of the thermopile to the substrate in conjunction with its electrical resistance. A simplified electrical model of ETF can be seen in Fig 4.8. This coupling adds an electrical phase shift directly to the thermally filtered heater drive signal. It has to be ensured that this is not significant in comparison to the thermal phase shift. Simulations are done on back annotated layout of the ETF for two drive frequencies 1MHz and 500 KHz.

The results are shown in Fig 4.10. The phase spread, across temperature, at fdrive of 1MHz is 24mdeg or 400ppm. It should be noted that for each batch a separate polynomial (mapping from temperature to ϕ_{ETF}) is used to calibrate the devices. This calibration will already reduce this error by an order of magnitude and will also compensate for the temperature dependency of the electrical phase shift. Further, ϕ_{ETF} is trimmed at two temperatures for obtaining the desired

frequency accuracy (Section 3.5). Therefore, this phase spread is also trimmed at two temperatures. Fig 4.10 shows that the phase spread after two temperature trim becomes negligible.

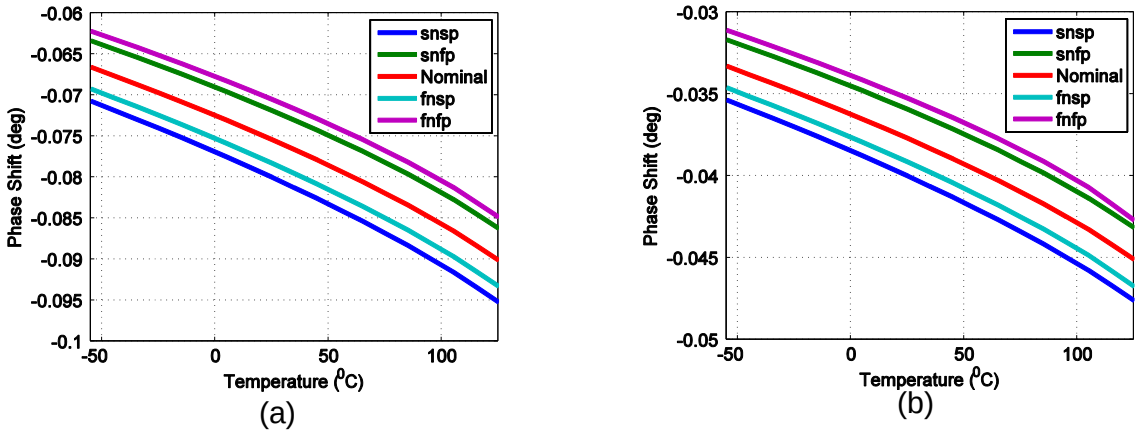

Fig 4.9- Electrical phase shift in ETF when (a) fdrive = 1MHz (b) fdrive = 500KHz

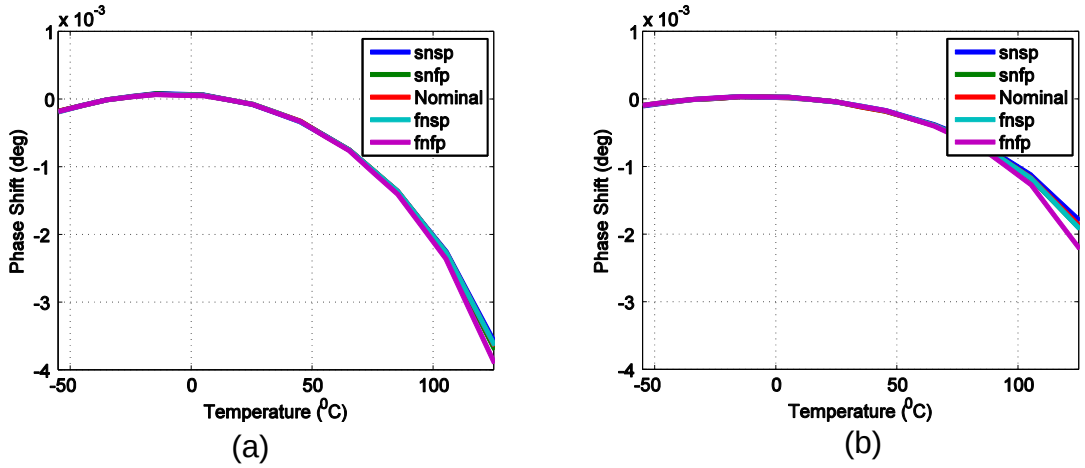

Fig 4.10 - Electrical phase shift in ETF after two temperature trim when (a) fdrive = 1MHz (b) fdrive = 500KHz

4.4 Measurement Results

It must be realized that an oxide ETF is composed of two materials and modeling its phase characteristics is quite difficult. Therefore, measurements are used to analyze the oxide ETF and verify its functionality. The following sections provide and discuss these measurement results.

4.4.1 Characteristics of Oxide ETF

The oxide ETF was fabricated in a 0.16μm CMOS 1.8V process. This section presents the characterizations of the phase of this ETF as a function of temperature and excitation frequency. The measurement setup is same as used for the silicon ETF and is shown again here in Fig 4.11. The Phase Domain Sigma-Delta modulator (PDSD) resembles the one used in the previous chip [9]. The output of the PDSD is filtered by a 130768 sample average. As it was expected that the oxide ETF would be more power efficient than silicon ETF, therefore it was designed to dissipate a maximum of 0.6mW of heater power. All the measurements are done at this power level.

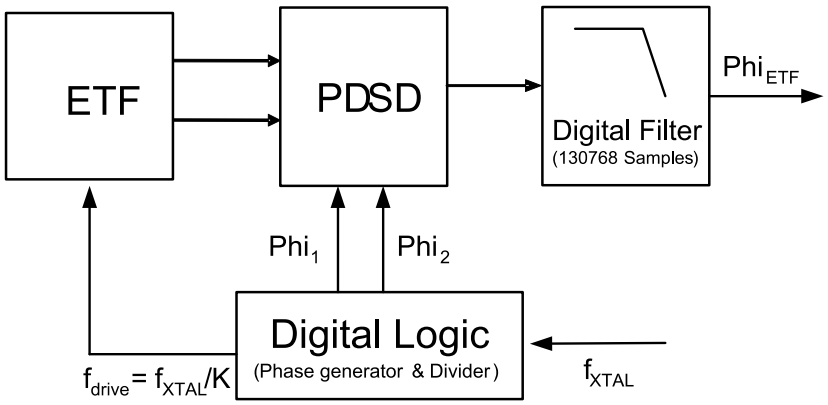

Fig 4.11- Measurement setup for ϕ_{ETF}

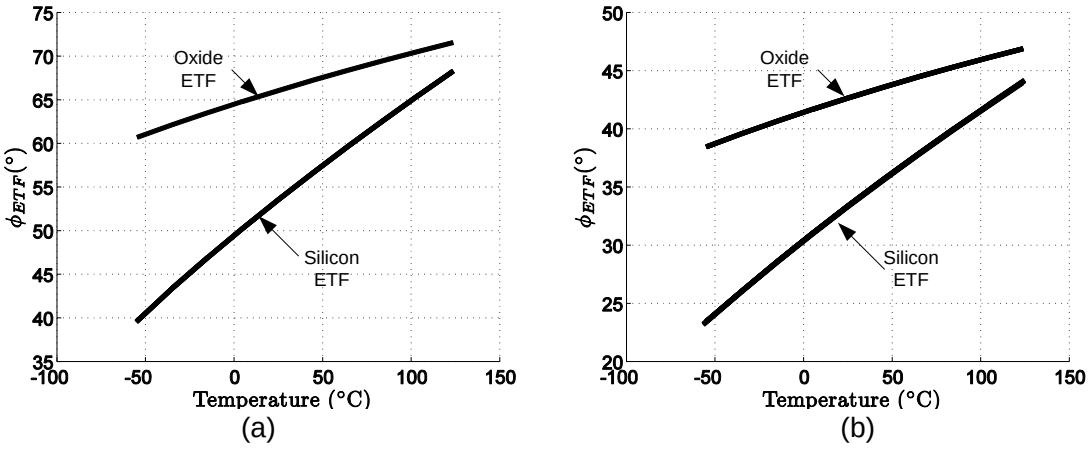

Fig 4.12- Phase delay due to Silicon (4.7µm) and Oxide ETF at (a) fdrive =1MHz (b) fdrive = 500KHz

Fig 4.12 shows ϕ_{ETF} variation across temperature. The phase variation across temperature (from -55^{0}C to 125^{0}C) is 11^0 for fdrive = 1MHz and 8^0 for fdrive = 500 KHz. This is about 2-3 times smaller than that of the silicon ETF used in the previous chip (Silicon ETF phase shift = 30^0 for fdrive = 1 MHz and 20^0 for fdrive = 500 KHz) (Fig 4.12). Thus the temperature sensitivity of the FLL that embeds such an oxide ETF should also be reduced by about the same factor. Although the oxide itself has much less temperature sensitivity, however, as discussed earlier in Section 3.2.2, the phase delay of the ETF is not only associated with the oxide. The heat pulse has to travel through silicon to reach the cold end of the thermocouple resulting in higher temperature sensitivity (in comparison to phase delay purely due to oxide).

One of the basic equations used to model an ETF is $\phi_{ETF} \propto \sqrt{f_{drive}}$ (2.1.5). This equation was derived for a uniform material such as silicon. For an oxide ETF, the heat pulse has to travel through two materials i.e. silicon dioxide and silicon. Thus, the validity of this equation should be verified for an oxide ETF, before it can be used in any further analysis. Fig 4.13 shows the plot of ϕ_{ETF} as a function of the driving frequency, f_{drive}. From this figure, it can be observed that for

high driving frequencies (f_{drive} > 512 KHz), the phase-frequency characteristic of an oxide ETF is close to $\phi_{ETF} \propto \sqrt{f_{drive}}$ curve. Further, for low driving frequencies (f_{drive} <100 KHz), the phase-frequency characteristic of an oxide ETF is close to $\phi_{ETF} \propto f_{drive}$ line. Thus, if an oxide ETF is driven at f_{drive} > 500 KHz, then the relation $\phi_{ETF} \propto \sqrt{f_{drive}}$ can be used for first order calculations.

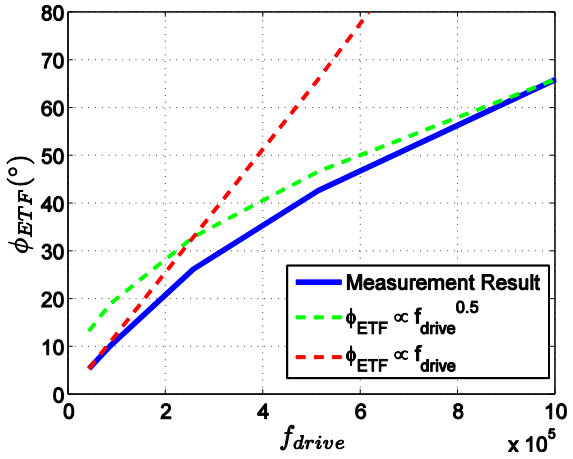

Fig 4.13- Phase-frequency characteristic of Oxide ETF

4.4.2 Limit to the accuracy due to Oxide ETF and the readout

In Chapter 3 (Section 3.3.2) limits to the frequency accuracy due to a silicon ETF were analyzed. The limit to the frequency accuracy due to the oxide ETF can be analyzed in a similar fashion. To study the spread of error in ϕ_{ETF} , the oxide ETF is driven at 1MHz and the error is plotted in Fig 4.14 (b).

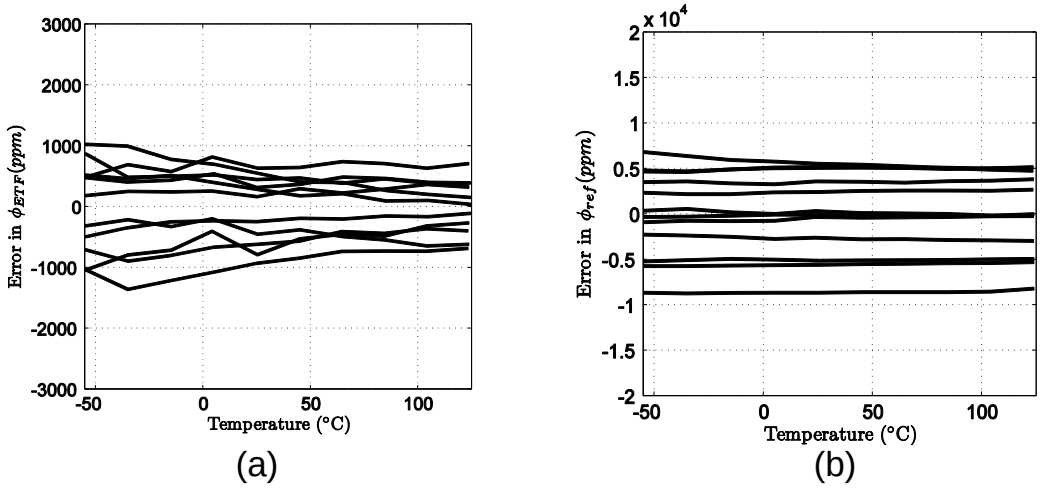

Fig 4.14- Untrimmed error spread of ϕ_{ref} for (a) s=10µm Silicon ETF (b) Oxide ETF

It can be observed from Fig 4.14 that the phase spread across the devices is much more in the case of the oxide ETF in comparison to the silicon ETF. The phase spread for the oxide ETF across devices at 25^0C is ~5000 ppm. In comparison, the phase spread for 10µm silicon ETF is less than 1000 ppm. More spread is due to variability of STI thickness with process. Thus, for obtaining an accurate frequency reference, trimming is necessary.

Different trimming strategies are implemented on the oxide ETF (trimming procedures for different strategies are described in detail in Chapter 3, Section 3.2.2). It was found that the two temperature trim gives the best accuracy performance. Fig 4.15 shows the ϕ_{ETF} error curves after two temperature trim. The two temperature trim is implemented by making the error zero at -15^0C and 85^0C. As can be observed from Fig.4.15 (a), the residual noise in ϕ_{ETF} (due to the thermal noise of the ETF and the readout) is limiting the trimming accuracy. If there was no noise the error curves would be smoother without abrupt jumps across temperature points. To reduce the effect of noise, the trim is applied to a linear approximation (best fit line) of the ϕ_{ETF} error curves. This results in a more realistic estimate of the accuracy of the frequency reference.

It can be seen from Fig. 4.15 (b) that the absolute phase error is ~ ±200ppm. Therefore, it is expected that frequency accuracy error, only due to ϕ_{ETF} error, would be around ±400ppm ($\frac{df}{f} = 2\frac{d\phi_{ETF}}{\phi_{ETF}}$).

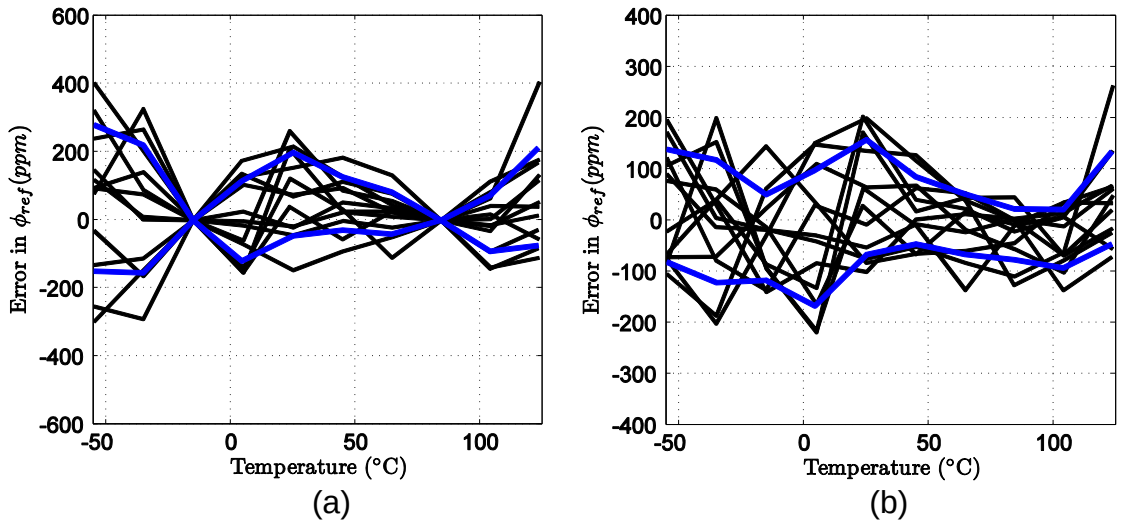

Fig 4.15 - ϕ_{ETF} error after two temperature trim on (a) Measurement data (b) Linear fit on the measurement data. Blue lines are $\pm 1\sigma$ lines.

4.5 An improved frequency reference based on Oxide ETF

To create a frequency reference, a digital integrator and a DCO are added to the block diagram in Fig. 4.14. The feedback loop is closed by driving the ETF with the output of the DCO (Fig. 4.24). To temperature compensate the FLL, a temperature dependent ϕ_{ref} is injected at the phase summation node of the loop.

The characterization setup used to calibrate the FLL is shown in Figure 4.25 and is the same as the one discussed in Chapter 3 (Section 3.3). In this figure, the parameter FCW is a 15-bit digital number that represents ϕ_{ref} .

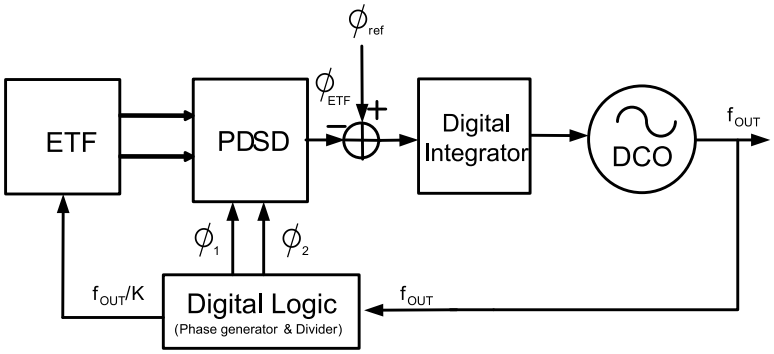

Fig 4.16- Block diagram of the FLL

For the purpose of calibration, ϕ_{ref} (FCW) is measured for 12 devices. A master curve (best fit to the over temperature characteristic) is extracted for these devices and is shown in Fig 4.18.

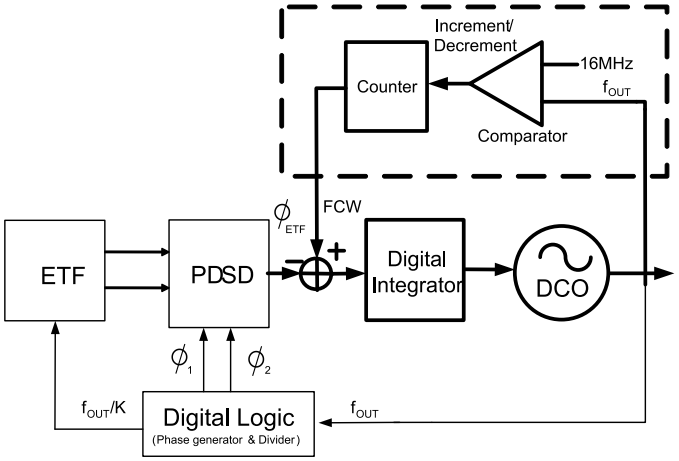

Fig 4.17- Measurement setup for characterizing ϕ_{ref} . The portion enclosed in the dotted line is implemented in software (Labview)

As in [9], a BG Temperature Sensor (TS) is present on the same chip. This TS is also characterized for 12 devices. Since, a two temperature trim is already planned for ϕ_{ref} , therefore TS is also two temperature trimmed. Fig 4.19 (a) and (b) show the untrimmed temperature error and the two temperature trimmed error respectively.

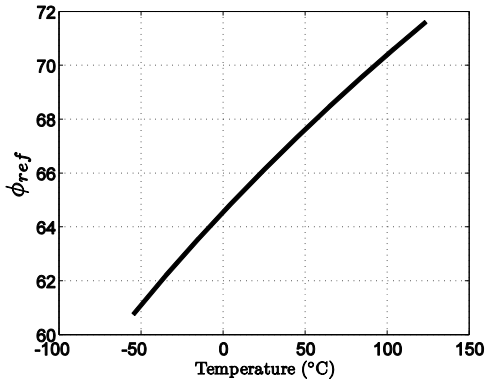

Fig 4.18 - Master curve for ϕ_{ref} vs. temperature for the oxide ETF. The ETF drive frequency is 1MHz.

To trim the devices, a strategy similar to the one used for silicon ETF is used (Section 3.3) and is shown here again in Fig 4.20. A 5th order polynomial is derived for mapping between ϕ_{ref} and μ. To trim a particular device, ϕ_{ref} and μ (TS output) are measured at around -15^{0}C and 85^{0}C. First, the TS is trimmed with respect to PT100 and trim parameters a & b are found using the two data points. Next, ϕ_{ref} is also trimmed again with respect to PT100. The trim in this case is applied though the TS output using the mapping between ϕ_{ref} and μ. Trim parameters m & c are calculated such that ϕ_{ref} is trimmed.

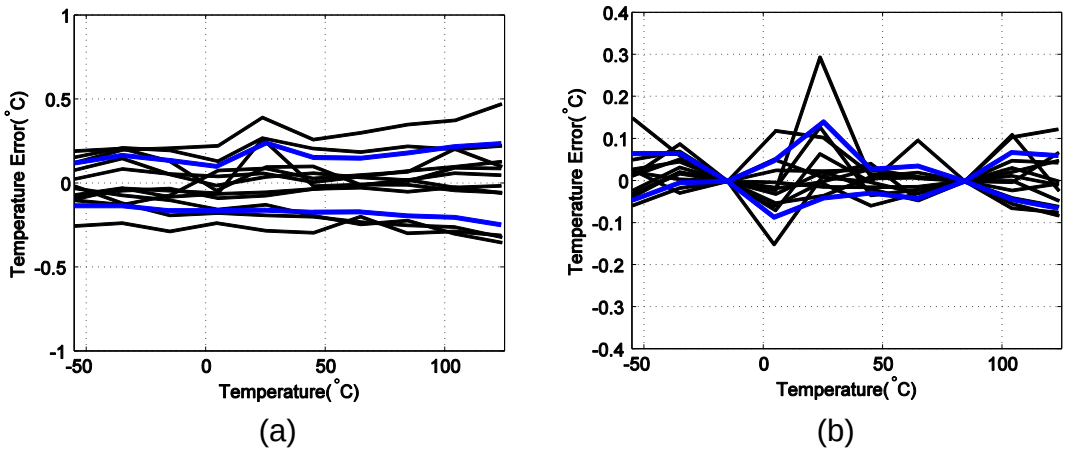

Fig 4.19- Temperature error (a) Untrimmed (b) Two temperature trimmed. Blue lines are $\pm 1\sigma$ lines.

Once trimming parameters are defined, the devices are put inside an oven for accuracy measurement across temperature. The output frequency is measured at steps of 20^{0}C starting from -55^{0}C up to 125^{0}C. Fig 4.21 shows the frequency errors from the desired 16MHz for 16 devices. As can be seen from the figure, an absolute inaccuracy of ~ ±500ppm is obtained over the complete military temperature range.

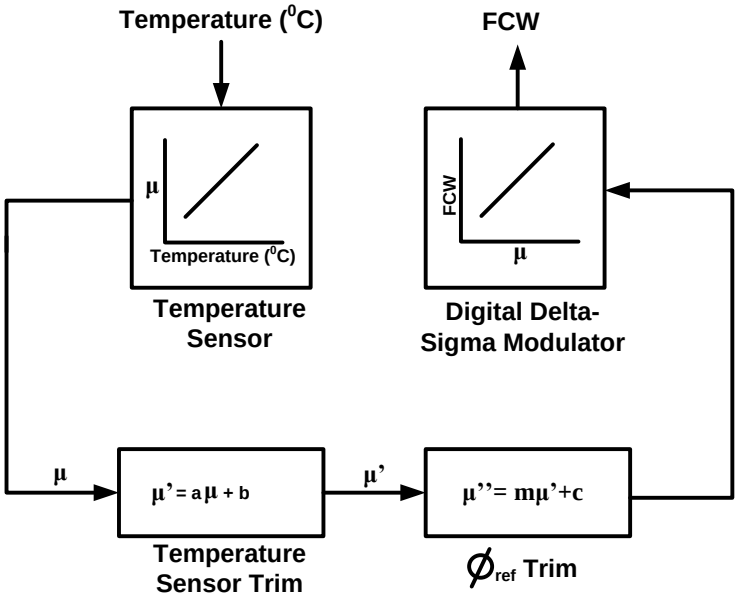

Fig 4.20- Trimming strategy for two temperature trim

The TS in this chip has a poorer accuracy than the one used for silicon ETF compensation (Chapter 3). The 1σ accuracy of this TS is close to $\pm 0.1^0$C (Fig 4.19) whereas 1σ accuracy of the earlier TS is less than $\pm 0.05^0$C (Fig. 3.19) for temperatures less than 105^0C. Even with higher TS inaccuracy, the oxide ETF produces a more accurate frequency output than the silicon ETF.

Since, the DCO is similar to the one used for silicon ETF therefore, the errors contributed by it are also of the same order.

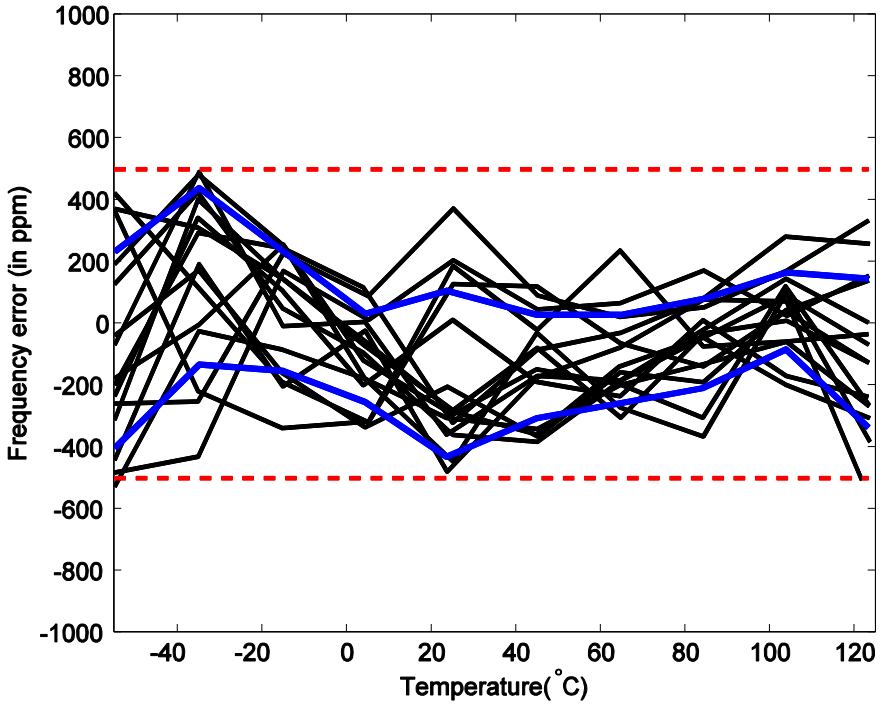

Fig 4.21- Frequency inaccuracy for Oxide ETF. Blue lines are lines $\pm 1\sigma$ lines.

4.6 **Conclusion**

In this chapter, a new ETF structure is proposed. The structure uses Silicon dioxide to generate thermal delay. Since the temperature coefficient of thermal conductivity of silicon dioxide is much lower than silicon, the phase characteristic of the resulting oxide ETF is less temperature dependent than the previously used silicon ETFs; this relaxes the accuracy requirements of the temperature compensation scheme, i.e. the on-chip temperature sensor, of the thermal diffusivity based frequency reference, built around the oxide ETF. Therefore frequency errors due to the inaccuracy of TS are reduced. Measurements on the characteristics of the oxide ETD over temperature show a 2-3x lower temperature sensitivity with respect to 4.7um Silicon ETF. As a function of variations in the thickness of the oxide layer, the oxide ETF has an initial process spread of 5X times larger than the silicon ETF. The oxide ETF has been embedded in an electrothermal frequency locked loop (FLL) with an output frequency of 16MHz. The FLL's output frequency is temperature compensated by means of a band-gap temperature sensor. A two temperature trim was applied to reduce the output frequency inaccuracy. Finally, an absolute output frequency inaccuracy of ±500ppm was obtained. This inaccuracy is due to the residual temperature sensitivity of the ETF, limited trimming resolution, limited DCO resolution and jitter. With an improved DCO resolution and jitter performance, inaccuracy of ~ ±300ppm should be achievable.

5 Digitally Controlled Oscillator

In the previous chapter, it was shown that limited DCO resolution was one of the factors limiting the frequency accuracy. To obtain better frequency accuracy, the DCO resolution should be improved. As a consequence, the jitter should also be reduced. In many applications, such as synchronous data transfer, jitter performance of the DCO is critical.

Based on these requirements, the design of an improved DCO is presented in this chapter. Section 5.1 provides an introduction to the chapter. Section 5.2 lists and derives the important specifications of the DCO. Section 5.3 describes the circuit design of the various DCO blocks and finally the chapter is concluded in Section 5.4

5.1 Introduction

In Chapters 3 and 4 it was concluded that the trimming accuracy was limited by the DCO resolution. This leads to inaccurate frequency output. In this section, further motivation for better DCO resolution and jitter is provided.

The frequency of a TD frequency reference can change only in discrete steps defined by the LSB of the DCO. Therefore, the frequency accuracy of the reference is limited to half the LSB of the DCO e.g. if the DCO LSB size is 250ppm then the worst case frequency error could be 125ppm.

Further, the DCO resolution will also limit the trimming resolution. The effect of limited trimming resolution becomes worse at temperatures farther away from the trim temperature.

Apart from the resolution, the inherent jitter of the DCO directly affects the jitter performance of the frequency reference. The FLL used to implement the frequency reference is a first order loop. The transfer function of the output phase noise to the DCO phase noise is given by [9],

$$\frac{\phi_{OUT}}{\phi_{n,DCO}} = \frac{s}{s+K} \tag{5.1.1}$$

where K is the loop gain of the electrothermal loop. As can be seen from Eq.5.1.1, the noise of the DCO is high pass filtered by the loop. Further, the loop bandwidth is in tens of Hz [9]. Therefore, most of the phase noise from the DCO will end up as jitter at the reference output.

In the following sections, specifications for the DCO are derived for a more accurate and low noise frequency reference. Further, a DCO design is presented which meets these specifications.

5.2 Specifications

In this section, all the important specifications of the DCO are discussed. Specifications are derived based on the requirements of a 500ppm accurate frequency reference.

5.2.1 **Resolution**

Any real DCO will have a frequency spread due to temperature, process and other variables. The tuning range of the DCO should be enough to compensate for this spread. Tuning is done using a DAC which has a limited resolution.

To obtain 500ppm of frequency accuracy (at a centre frequency of 16MHz), the DCO resolution should be at least 5 times better (100ppm) so as not to have an effect on the overall accuracy. A very accurate DAC is required to obtain this level of resolution (assuming a DCO output range of 1MHz centred at 16MHz, the DAC should be more than 10bits).

5.2.2 **Jitter**

As mentioned earlier, the jitter is a critical specification for a frequency reference. The standard jitter metric used in digital systems is *period jitter*. Period jitter is defined as the standard deviation of the difference between two consecutive rising edges of the clock or in other words, as the standard deviation of a single period of the clock [27].

$$\sigma(k) = \sqrt{Var(t_{k+1} - t_k)} = \sqrt{Var(T_k)} \tag{5.1.2}$$

where t_k and t_{k+1} are k^{th} and $k+1^{th}$ rising edges of the clock respectively and T_k is the k^{th} period of the clock.

The jitter of the DCO should be in-line with the expected resolution. Thus, the DCO is designed for a period jitter of 100ppm (6.25ps) with respect to 16MHz centre frequency which is the same as the specification for the resolution.

To make a comparison, crystal-oscillator based frequency references (which are used for application such as USB, S-ATA etc) have 6.1ps of period jitter at 16MHz centre frequency[2]. Thus, the period jitter specification of 6.25ps is also close to the period jitter of a crystal oscillator (6.1ps). This shows that a period jitter of 6.25ps is not unrealistically high and is comparable to commercially available frequency references[5].

5.3 **DCO Design**

In this section, the factors limiting the performance of the previous DCO are discussed. With the help of these factors, an architecture is selected which can satisfy the specifications discussed in the previous section. Finally, a detailed design of all the blocks of the DCO will be provided.

5.3.1 **Previous DCO**

The DCO used in the previous chip [9] is a relaxation oscillator driven by a resistor string DAC (see Fig 5.1). The center frequency of the DCO is 16MHz. The oscillator consists of two capacitors which are charged and discharged in complementary half cycles. The capacitors are charged to V_{DD} through R_{ch} and discharged through a constant current source I_{ref}. When either of

[5] It should be noted that LC oscillator based references have achieved better period jitter performance (<3ps)

the capacitor voltages V_1 and V_2 reaches the comparator threshold voltage V_{ref}, the corresponding comparator sets the SR latch. Once the latch is set, the other capacitor starts to discharge.

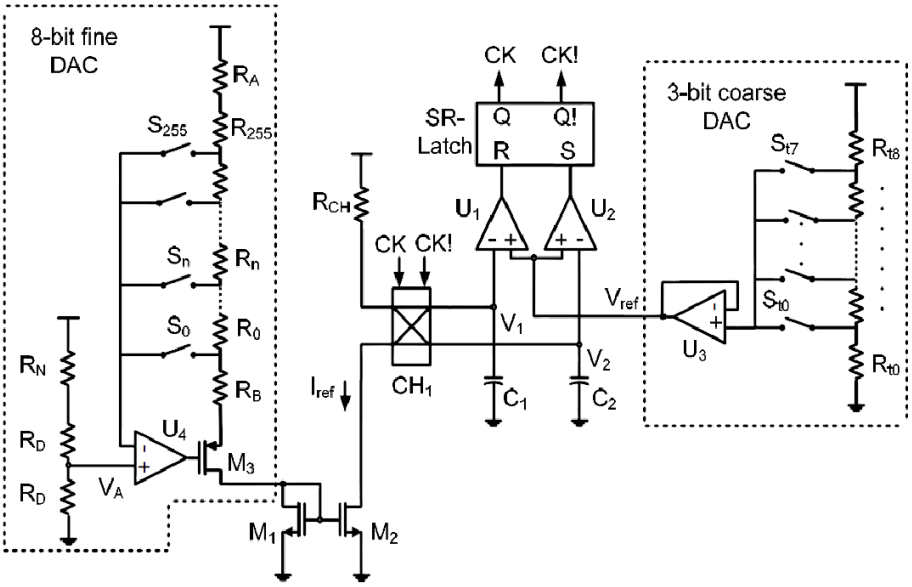

Fig 5.1- Block diagram of DCO used in the previous chip (Figure taken from [9]).

Measurements on the previous chip show that the free-running DCO has a jitter of about 40ps. From simulations, only 16ps of jitter was due to the inherent noise of the circuit. As shown in the next paragraph, the rest of the jitter is probably due to power supply noise.

VDDA supply noise couples into the VCO via resistor R_{ch} and reference current I_{ref} while VSSA supply noise is coupled in via capacitors C_1 and C_2. Fig 5.2 shows the simulated jitter at the DCO output as the supply noise is increased. It can be seen that jitter is strongly affected by supply noise. Thus, it is probable that high noise on the supply in addition to poor AC PSRR of the previous DCO causes an increase in the jitter.

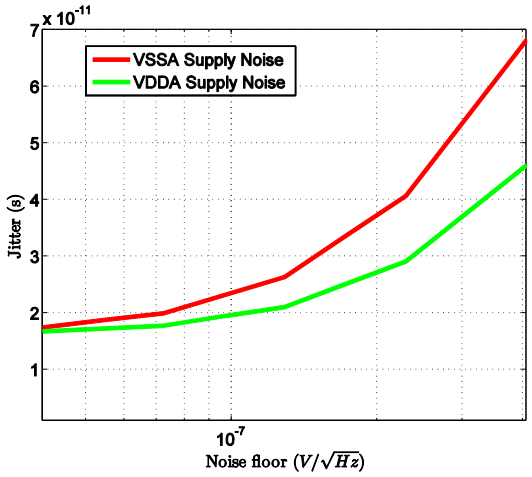

Fig 5.2- Jitter of the previous DCO due to the VDDA and VSSA supply noise

5.3.2 **DCO architecture**

In this section, various possible architectures of the DCO are discussed which can satisfy the requirements listed in the previous sections. Among these the most widely used are LC oscillators, ring oscillators and relaxation oscillators. Due to area constraints, LC oscillators were not considered as an option for this DCO. Moreover, the center frequency of this reference is 16MHz which is rather low for LC oscillators.

To compare the different architectures with respect to power and noise a widely used Figure of Merit (FOM) is used [32].

$$FOM = \gamma(f)\left(\frac{f_m}{f_{OSC}}\right).P.10^3 \qquad (5.1.3)$$

Where $\gamma(f)$ is the phase noise at a frequency f_m, f_{OSC} is the oscillation frequency and P is the power dissipation in the oscillator core.

Theoretically, relaxation oscillators have a better FOM than ring oscillators. But in practice, relaxation oscillators perform worse due to the noise contribution of their comparators [28]. Typical values of FOM for ring oscillators are around -165dB, while for relaxation oscillators they are around -155dB [28][29].

Since, susceptibility to supply noise is high; therefore supply rejection is a major consideration while designing the DCO. Single ended ring oscillators have poor supply rejection. Differential ring oscillators have excellent supply rejection but their FOM is typically 10-13 dB lower ([29] lists several inverter chain ring oscillators, current starved ring oscillators and differential ring oscillators. Their FOM was determined with the data provided and it was found that differential ring oscillators have 10-13dB lower FOM than single ended ring oscillators). Thus, the FOM of differential ring oscillators is similar, if not worse, than that of relaxation oscillators. This implies that relaxation oscillators would have similar performance as differential ring oscillators if they could be designed to have good Power Supply Rejection (PSR).

In this chapter a noise cancellation technique for relaxation oscillators is proposed which reduces the effect of supply noise on the output jitter (this technique is described in detail in Section 5.3.4). Since the effect of supply noise can be reduced, a relaxation-oscillator based DCO will again be used for the frequency reference.

In the previous DCO, shown in Fig 5.1, the capacitors C_1 and C_2 are discharged by I_{ref}. Therefore, I_{ref} and the current mirror transistors M1-M2 contribute considerable thermal and 1/*f* noise when referred to the phase or frequency output. One way to reduce this noise is to degenerate the current mirror transistors M1-M2. Since limited voltage headroom is available in 0.16µm CMOS process (1.8V) therefore this option is not considered. Another way to reduce this noise is to replace these current sources by resistors [8]. Poly resistors do not show 1/*f* noise and therefore contribute less to jitter.

The schematic of the improved oscillator is shown in Fig 5.3. The oscillator comprises two complementary circuits. In the first half cycle, the capacitor C_1 is charged by the resistance R_1. When V_{OSC} reaches V_C, the comparator output sets the set-reset latch.

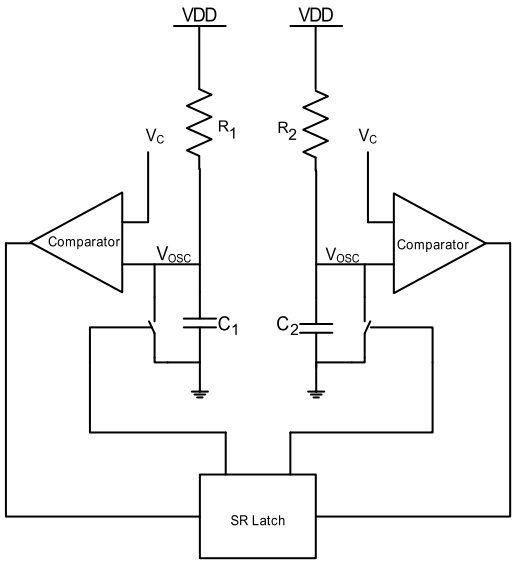

Fig 5.3- Block diagram of the DCO

Once the FF is set, the other capacitor C_2 starts to charge and C_1 is discharged to ground. The waveform of V_{OSC} is shown in Fig 5.35. The time constant of the oscillator is given by:

.

$$T_{OSC} = 2\left[t_d + RC \ln\left(\frac{V_{DD}}{V_{DD} - V_C} \right) \right] \tag{5.1.4}$$

Where t_d is the comparator delay and V_C is the reference voltage at the positive terminal of the comparators.

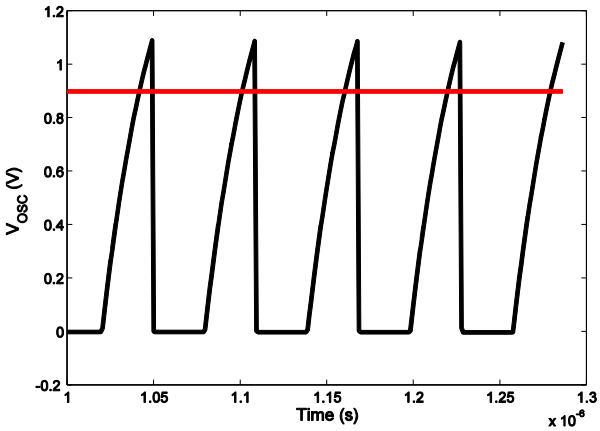

Fig 5.4- Voltage waveform at V_{OSC} (Input of the comparator). The red line denotes the reference voltage V_C

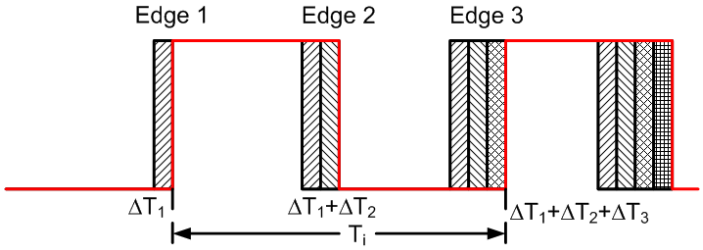

Fig 5.5- Clock Output of the Oscillator

To aid the design of this oscillator, *a guideline for jitter* needs to be established. Fig 5.5 shows the clock output with additional jitter. ΔT_1 is the timing jitter at Edge 1 and so on. Abidi[31] defines timing jitter for relaxation oscillators as:

$$\sigma_{rms} = \frac{\alpha V_n}{S} \tag{5.1.5}$$

Where V_n is the rms noise voltage in series with the timing waveform, i.e. V_{OSC} in Fig 5.4 and S is the slope of the timing waveform at the triggering point and α is a proportionality constant which depends on whether the noise power is concentrated at high or low frequencies. The noise gets accumulated as it is generated within the oscillator (see Fig 5.5). Therefore the period jitter is given by,

$$\sigma_{Ti} = \sqrt{Var(\Delta T_2 - \Delta T_3)} = \sqrt{2.Var(\Delta T_{2,3})} \tag{5.1.6}$$

$$\sigma_{Ti} = \frac{\sqrt{2}\alpha\sigma_V}{S} \tag{5.1.7}$$

The above equation is used to calculate period jitter in rest of the chapter. From this equation it can be seen that slope of the timing waveform should be maximized to reduce noise.

5.3.3 Optimum Values of $C_{1,2}$, $R_{1,2}$ and V_C

The optimum values are determined so as to minimize jitter. In this oscillator, $R_{1,2}$ is the major source of jitter apart of the comparator. A detailed noise analysis is done in Appendix B to find a relation between these design parameters and jitter.

Since the oscillator switches alternatively from one half to another, the resistor noise is integrated on the timing capacitance $C_{1,2}$ over half the oscillation cycle. This integrated noise causes a variation in V_{OSC} which in turn results in jitter (since the oscillator changes state when $V_{OSC}=V_C$ therefore any variation in V_{OSC} causes variation in the triggering point). As the integrated noise voltage will be smaller for a larger capacitor therefore jitter is expected to decrease for larger capacitor values. To verify this, the oscillator is simulated with all the components as noiseless except the timing resistors $R_{1,2}$. Fig 5.7 shows jitter for varying capacitor $C_{1,2}$ values. Although, $C_{1,2}$ should be kept as large as possible but area constrains limit $C_{1,2}$ to lower values. To ensure

that $C_{1,2}$ does not contribute significantly to jitter and area specification, $C_{1,2}$ = 1pF is chosen for this design.

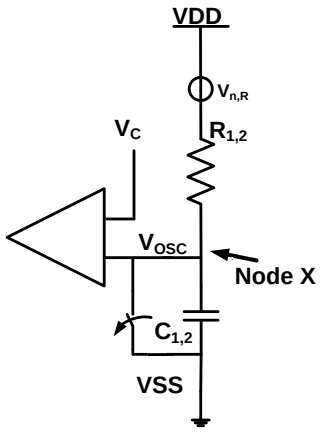

Fig 5.6- Half circuit of the oscillator for noise analysis.

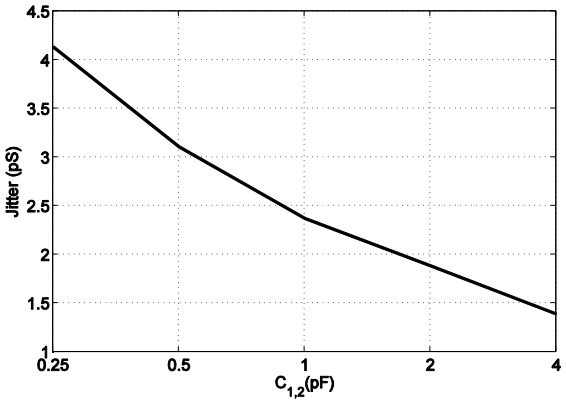

Fig 5.7- Jitter variation across Capacitance

Once C1,2 is fixed, the value of R1,2 can be determined from the RC product (RC is fixed for a given oscillation frequency – Eq. 5.1.4).

The find the optimum value of V_C, the oscillator jitter is simulated for a fixed oscillator frequency. The result is shown in Fig.5.8. The minimum jitter is obtained at $V_{C,opt}$ = 1V (same result is also obtained from the analysis done in Appendix B).

In the above simulation the comparator has been assumed ideal. To make sure there is enough biasing margin for all the transistors in the comparator, V_C = 0.9V has been taken for this design (comparator design is discussed in Sec. 5.2.3.4). It can be observed from Fig. 5.8 that a lower value for V_C (=0.9V) results only in a marginal increase in jitter.

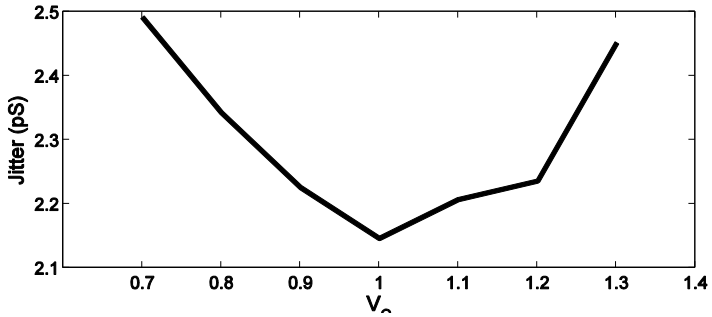

Fig 5.8- Jitter variation across V_C

5.3.4 **Comparator**

In this section the design of the comparator is presented. A continuous time comparator is required for this oscillator. Further, the noise of the comparator should be low as it affects the jitter. Apart from being low noise, the delay of the comparator should not be significant when compared to the whole period of the oscillator. This is because variations in the comparator delay, t_d, results in a variation in the frequency over PVT (process-voltage-temperature). Frequency variations are not desirable in order to relax the dynamic range requirement on the DAC. But decreasing the comparator delay leads to an increase in jitter as shown by Gierkink [30]. As the delay decreases, the input referred noise of the comparator increases due to expansion of its noise bandwidth (NBW). Therefore there is a trade-off between total frequency variation, jitter and power.

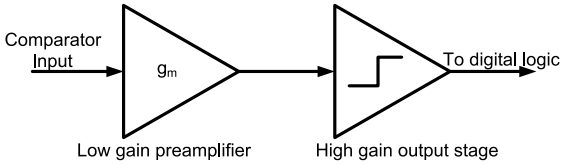

Fig 5.9- Block diagram of the comparator.

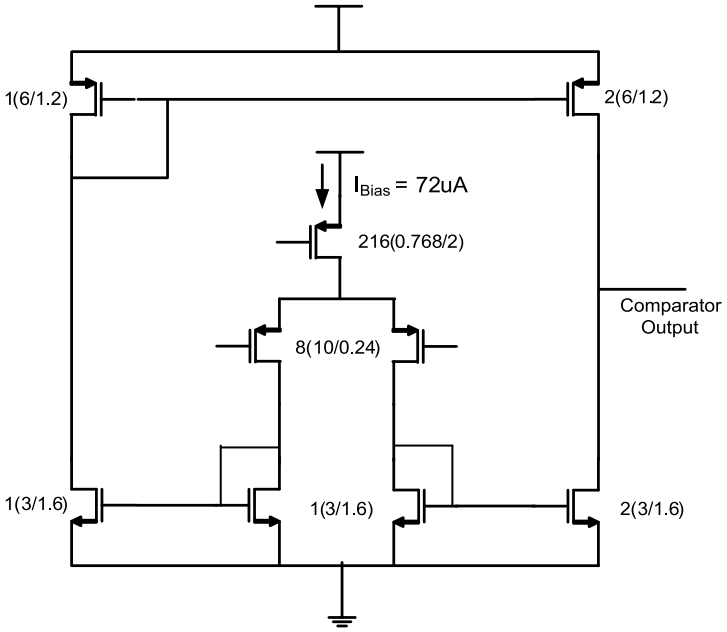

Fig 5.10- Schematic of the comparator.

A simple two-stage architecture is chosen for the comparator as shown in Fig 5.9. The first stage acts like a buffer and reduces kickbacks, to the input, due to comparator output switching. It has a low gain of around 5. The second stage is fast and has high gain (>35) to provide rail to rail swing to the proceeding stages. The schematic of the comparator is shown in Fig 5.10.

The input pair is operated in sub-threshold for better power efficiency and sized to reduce 1/f noise. PMOS transistors are used for the input pair as they have lower 1/f noise than NMOS transistors. The load current mirrors are sized to minimize noise i.e. they are biased at maximum possible V_{GST} for a given current. The maximum V_{GST} is limited by maximum drain voltage, of the input pair, such that the input pair always remains in saturation at the quiescent point.

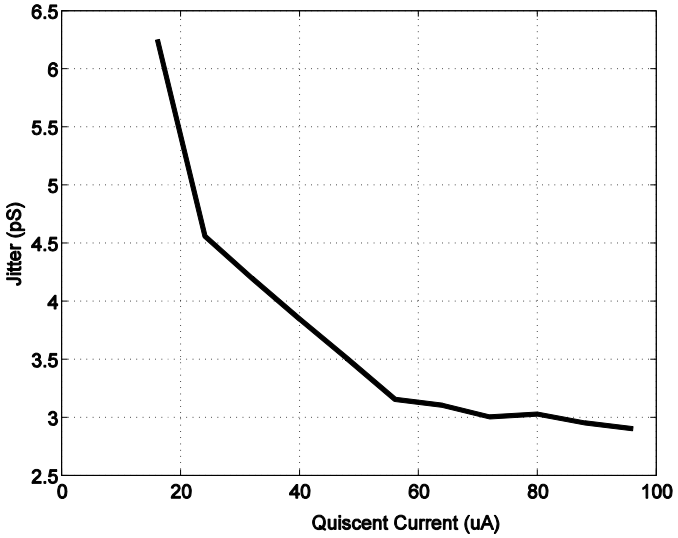

Fig 5.11- Jitter variation with quiescent current in the first stage of the comparator.

Fig 5.11 shows the plot of jitter vs. the current in first stage of the comparator. The jitter will increase in other process corners as shown in the final simulation results in Section 5.3.9. To ensure that jitter specification is met in all the corners, a relatively high quiescent current of 72μA is used in the first stage. It can be seen, from Fig 5.11, that 72μA of current gives 3pS of jitter in the nominal corner. Fig 5.11 is obtained by increasing the current in the comparator while keeping the biasing voltages constant. The rate of change of jitter with current slows down at around 60 μA as the jitter due to the timing resistance $R_{1,2}$ starts to have an effect on the overall jitter performance.

It should be noted that the current in the output arm of the D2S stage (output stage) flows only when the comparator is in linear mode i.e. the output is neither high nor low. Therefore, the average current consumption in the comparator is only 94μA.

5.3.5 **DAC**

As stated in Section 5.2.1, a frequency resolution of 100ppm is required in line with the frequency accuracy of the reference. Building a Nyquist DAC is not trivial at such resolutions. Recently, some authors have used a delta-sigma DAC for increasing the resolution of a DCO [25][26]. The

advantage of using a delta-sigma DAC is that it can be implemented easily in digital with the existing analog hardware. To have some margin, a resolution of around 50-75ppm is targeted. This can be achieved by implementing a 200-300ppm resolution Nyquist DAC and obtaining an extra 2-bit resolution using a delta-sigma modulator.

5.3.5.1 Nyquist DAC

For this DCO, a coarse Nyquist DAC is used to compensate for frequency variations due to process corners. At a particular process corner, a separate fine Nyquist DAC is used to compensate for frequency variations, across parameters such as temperature, supply voltage etc. Fig 5.12 shows the variation of frequency, across temperature, at various process corners. The maximum variation is ~300KHz and occurs at snfp process corner. To ensure enough margins, the DCO should be able to tune up to ±500KHz around the center frequency.

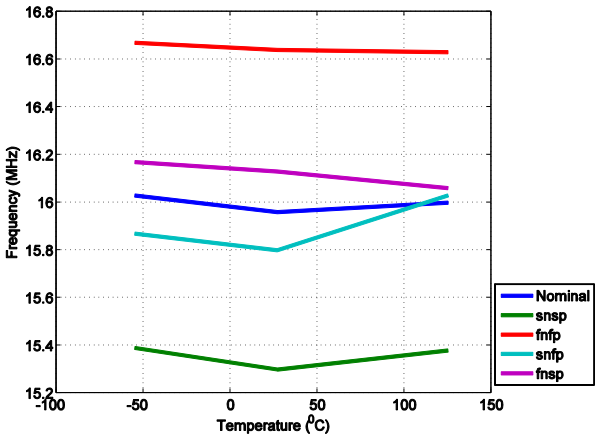

Fig 5.12- DCO frequency variation across temperature and process.

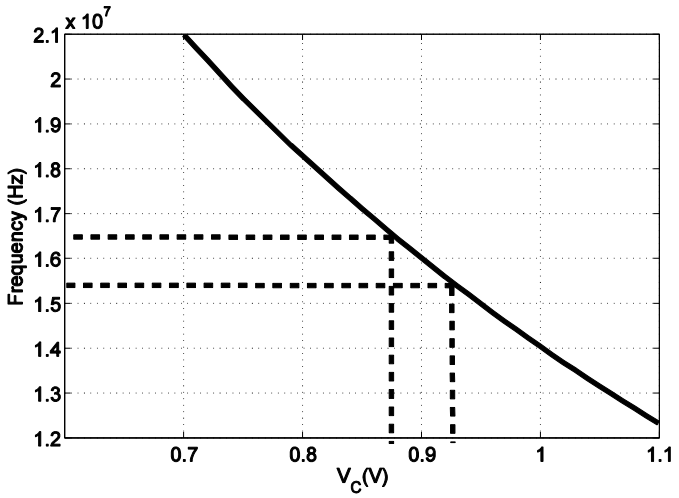

Fig 5.13- DCO frequency variation with V_C (analog control voltage)

Fig 5.13 shows the plot of the DCO output frequency F_{DCO} vs. V_C , where V_C is the analog frequency control voltage for the oscillator. From this figure it can be seen that the DAC output should be ±25mV to enable ±500kHz tuning of the frequency output. An 8-bit resistor array DAC was designed for the previous chip and is re-used here with some modifications. An 8-bit DAC would give ~244ppm frequency resolution over a ±500kHz tuning range. This DAC resolution is enough for meeting the required specifications[6].

The top level diagram of the DAC is shown in Fig 5.14. The output of the DAC is connected to the appropriate point on the resistor array depending on the digital input. To compensate for the temperature variations, an Nwell resistor (positive TC) is added in series with the Npoly resistor array (negative TC) [9]. (The filter at the DAC output is described later in this section)

The coarse DAC is implemented using the timing resistor. The schematic of the coarse DAC is shown in Fig 5.15. The timing resistor R_1 in Fig 5.3 is divided into the coarse DAC and a resistor R1'. One of the switches, S1-S8, is switched-on depending on the coarse trim value. Plot of DCO frequency output, F_{DCO} , at various trim values is shown in Fig 5.16. F_{DCO} can be varied from 19.2MHz to 13MHz and is large enough to cover all possible process corners.

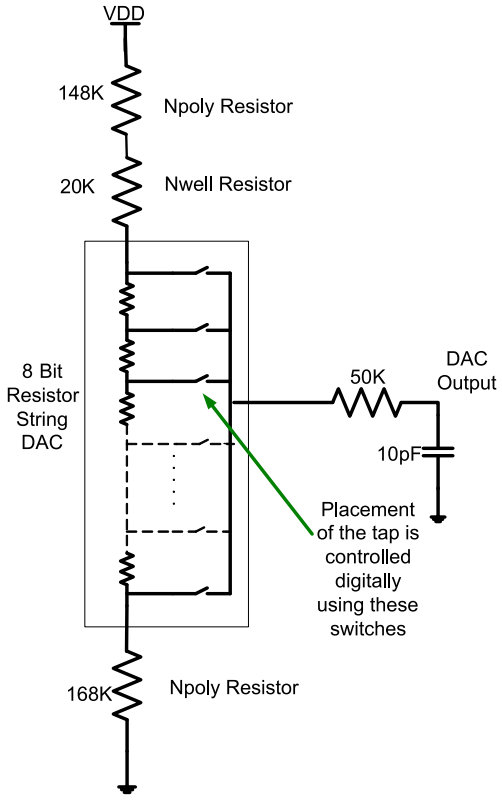

Fig 5.14- Top level diagram of resistor string DAC.

[6] It should be kept in mind that this resolution is only for the Nyquist DAC. An extra 2 bits of resolution is obtained from the delta-sigma DAC.

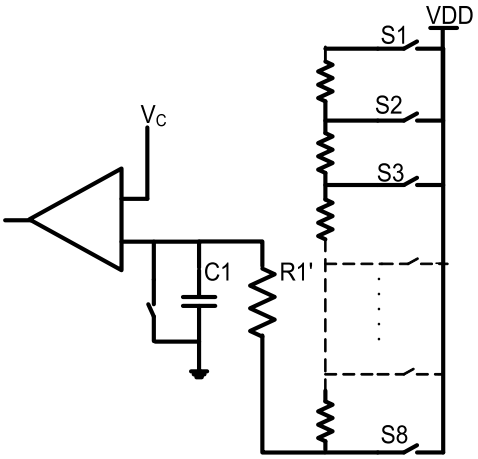

Fig 5.15- Left half cell of the oscillator. The coarse trim DAC is also shown

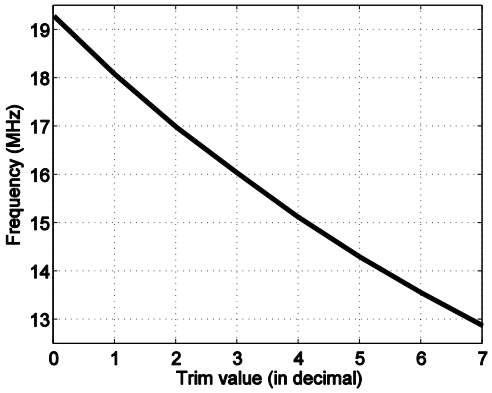

Fig 5.16- DCO frequency output vs. coarse trim

5.3.5.2 Delta Sigma DAC

In the previous system, the DCO resolution is limited by the DAC resolution i.e. to one DAC LSB. The DCO input is updated at Fs = 42 kHz. Since, the highest frequency in the system is F_{DCO} = 16MHz, therefore there is a possibility to drive the DAC at a higher frequency and use oversampling to obtain better resolution. To see how this works, consider two values of reference voltage V_C which are one DAC LSB apart (V_X and $V_X + V_{LSB}$). These are alternatively applied to the oscillator at twice the present update rate of Fs=42 kHz (Fig 5.17). The oscillation period changes with the applied V_C as,

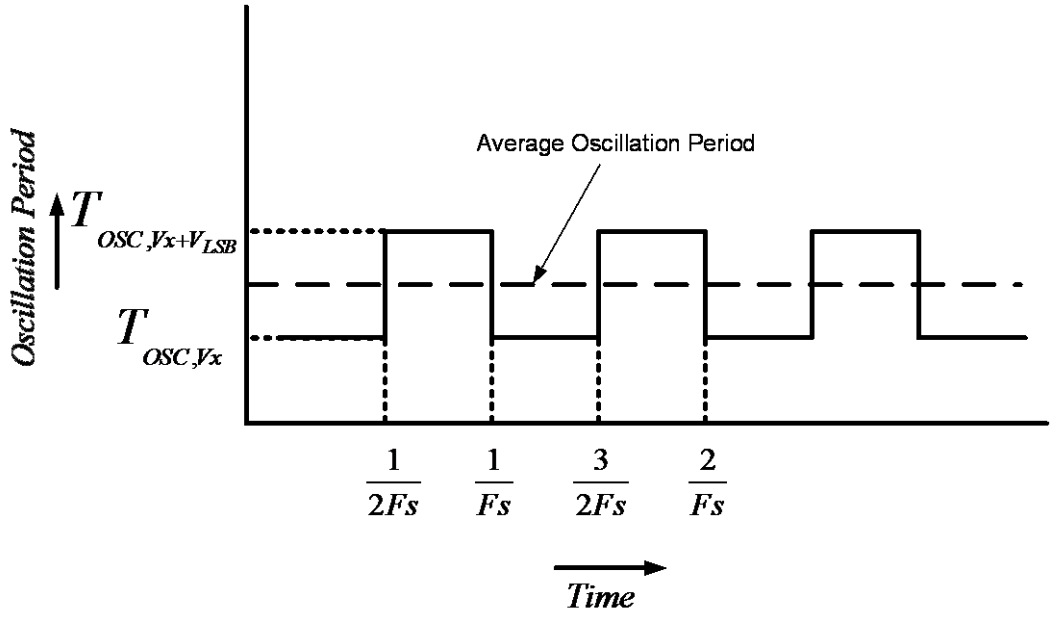

Fig 5.17- Oscillation period changes alternatively according to the applied V_C .

For $V_C = V_x$: $$T_{OSC,V_x} = 2\left[t_d + RC\ln\left(\frac{V_{DD}}{V_{DD} - V_x} \right) \right]$$

For $V_C = V_x + V_{LSB}$: $$T_{OSC,V_x+V_{LSB}} = 2\left[t_d + RC\ln\left(\frac{V_{DD}}{V_{DD} - V_x - V_{LSB}} \right) \right]$$

$$\begin{aligned} &= 2\left[t_d + RC\ln\left(\frac{V_{DD}}{V_{DD} - V_x} \right) + RC\ln\left(1 - \frac{V_{LSB}}{V_{DD} - V_x} \right) \right] \\ &\approx 2\left[t_d + RC\ln\left(\frac{V_{DD}}{V_{DD} - V_x} \right) + RC\left(\frac{V_{LSB}}{V_{DD} - V_x} \right) \right] \end{aligned} \tag{5.1.8}$$

Thus, for a V_{LSB} change in V_C, the time period changes by $RC\left(\frac{V_{LSB}}{V_{DD} - V_x} \right)$.

From the above equations, the average period can be calculated as,

$$\frac{T_{OSC,V_x+V_{LSB}} + T_{OSC,V_x}}{2} = 2\left[t_d + RC\ln\left(\frac{V_{DD}}{V_{DD} - V_x} \right) + \frac{RC}{2} . \frac{V_{LSB}}{V_{DD} - V_x} \right] \tag{5.1.9}$$

As can be seen from Eq.5.1.9, the resolution improves by a factor of two by the use of oversampling. The resolution can be improved further by updating the DAC at even higher frequencies and also using noise shaping.

The update pattern shown in Fig 5.17 is not random and results in a tone at Fs. To spread this energy, over a wider band, a higher order delta-sigma modulator can be used.

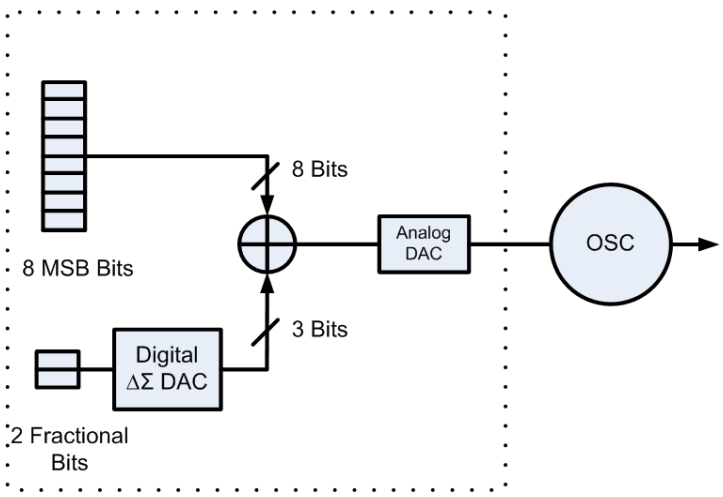

Fig 5.18- Block Diagram of the DAC. The area enclosed within the dotted lines is the DAC.

Block diagram of the complete DAC is shown in Fig 5.18. The basic principle of the DAC is same as used in [25]. The input to the delta-sigma modulator is a 2 bit number that represents the fractional bits for obtaining extra resolution. The 3rd order delta-sigma modulator is driven at $F_{MOD} = \frac{F_{OUT}}{2}$ i.e. 8MHz. The output of the modulator is a 3 bit number. This high frequency 3 bit output (updating at F_{MOD}) is added to the slowly varying 3 integer LSBs (updating at Fs). The combined 8 bits then drive the oscillator.

The architecture of the digital modulator is same as in [25]. The block diagram of the digital modulator is shown in Fig 5.19. It is a third-order MASH type structure. The LSB of the first modulator output is randomized using a 1-bit pseudorandom dithering sequence. This helps to randomize the input further (Fig 5.20).

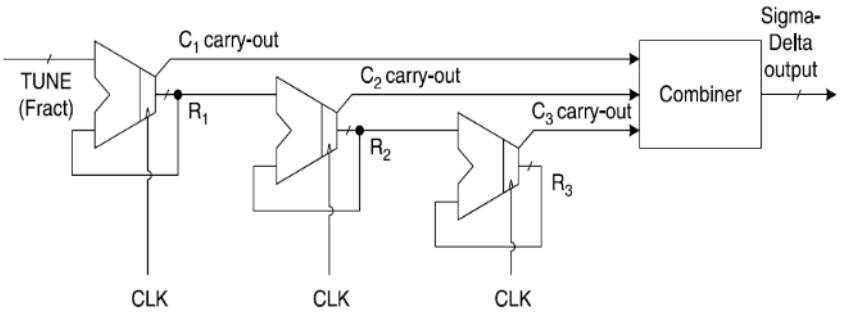

Fig 5.19- Diagram of the digital delta-sigma modulator [25].

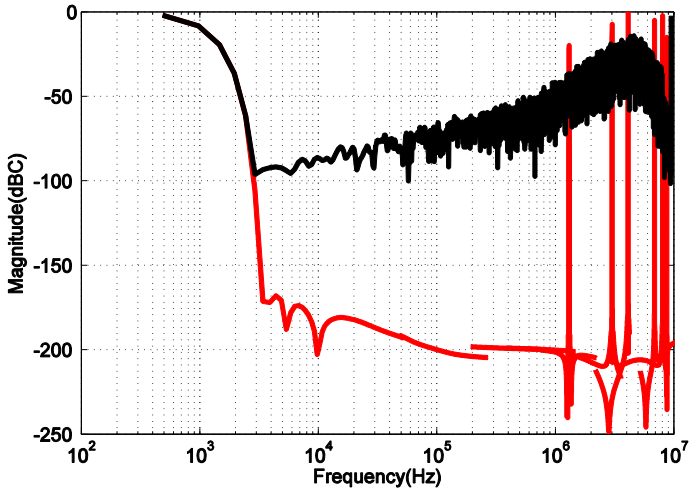

Fig 5.20- Spectrum of the modulator before (red) and after (black) randomization of the input.

The combiner circuit takes the three carry outs as inputs and produces 3 bit third-order modulator output using the following formula [25]:

$$Out_{\Delta\Sigma} = C_1 D^3 + C_2(D^2 - D^3) + C_3(D_1 - 2D^2 + D^3) \qquad (5.1.10)$$

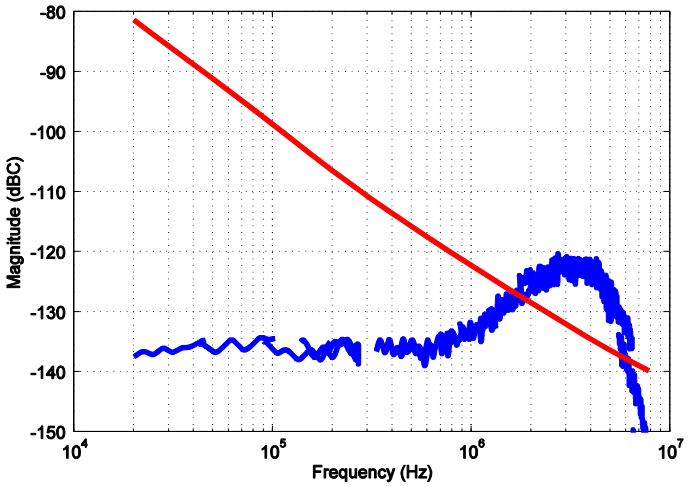

Fig 5.21- Phase noise plots of the DCO. Red curve is the phase noise plot of the DCO without delta-sigma modulator. Blue curve is the phase noise plot of the DCO with noise contribution only due to the delta-sigma modulator.

The 3rd order modulator shifts the quantization noise to higher frequencies. This quantization noise increases the phase noise at higher frequencies. The phase noise plot for *fractional input 2* is shown in Fig 5.21. To suppress noise at higher frequencies, the output of the DAC should be low pass filtered. From Fig 5.21, it can be observed that a first order filter of bandwidth <100 kHz would be sufficient to suppress the quantization noise[7]. A first order passive filter is implemented using Poly resistors and MIM caps. The phase noise plots, after filtering, for the fractional inputs 0, 1, 2 and 3 are shown in Fig 5.22, 5.22, 5.23 and 5.24. In all the phase noise plots below, the red curve is the phase noise plot of the DCO without the delta-sigma modulator and the black curve is the phase noise plot of the DCO with noise contribution only due to the delta-sigma modulator. The additional jitter, due to the quantization noise of the delta-sigma modulator, is less than 2.5pS.

Further, the loop updates the input of the DCO at Fs. Thus, the average frequency is calculated over a sampling period of $\frac{1}{F_S}$. Fig 5.26 shows the average output frequency for all the four possible fractional inputs (DCO output frequency is averaged over $\frac{F_{MOD}}{F_S}$ = 192 samples). It should be noted that these frequencies are above the 16MHz output. The following output frequencies are obtained over the centre frequency: 100Hz, 1100Hz, 2100Hz and 3100Hz corresponding to the fractional inputs of 0, 1, 2 and 3 respectively. Thus, the resolution obtained is ~ 1000Hz or 62.5ppm.

[7] The maximum attenuation needed to suppress the quantization noise, below the inherent phase noise of the DCO, is <20dB even beyond 1MHz. Since a first order filter with a bandwidth of 100 kHz would have attenuation greater than 20dB beyond 1MHz (1 decade) therefore it is sufficient to suppress the quantization noise.

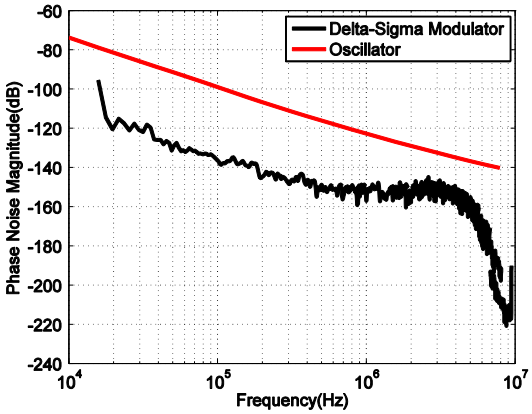

Fig 5.22- Phase noise plots of the DCO for fractional Input=0.

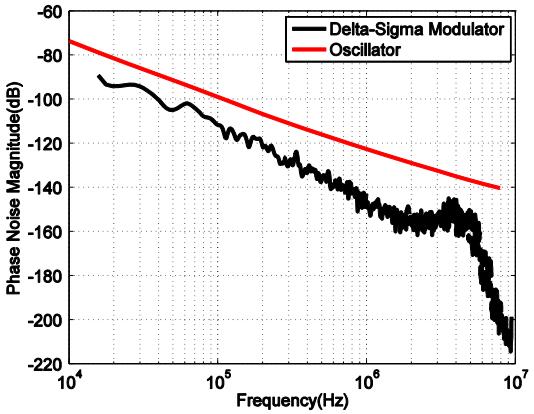

Fig 5.23- Phase noise plots of the DCO for fractional Input=1.

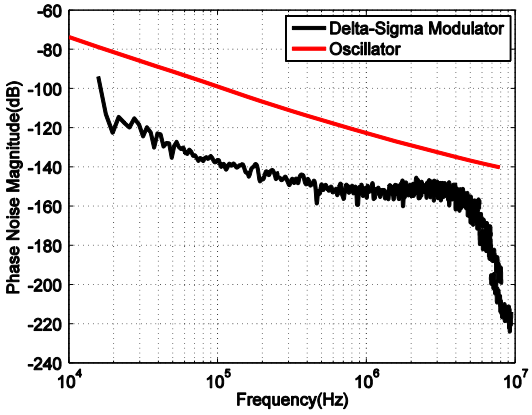

Fig 5.25- Phase noise plots of the DCO for fractional Input=2.

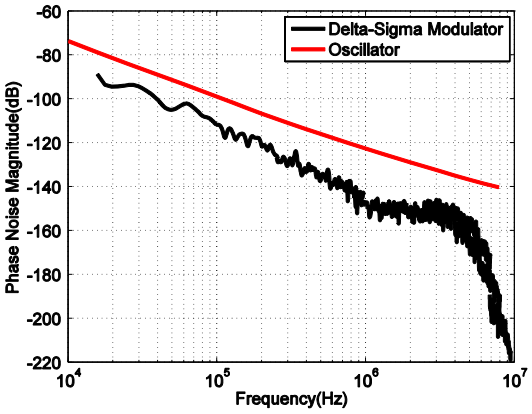

Fig 5.24- Phase noise plots of the DCO for fractional Input=3.

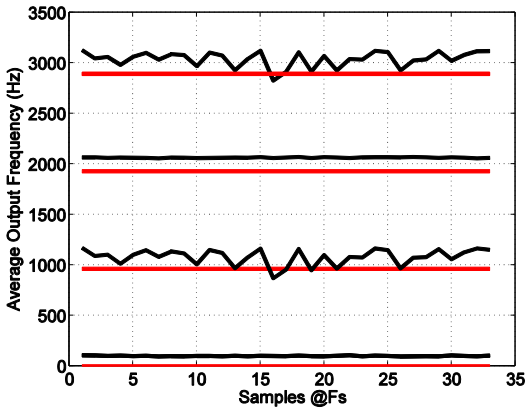

Fig 5.26- Average output frequency of the DCO. Red line is the target frequency for each fractional input.

5.3.6 **Supply Noise Cancellation**

As mentioned in Section 5.2.2, one of the major causes of jitter in the previous design was supply noise coupling. This section investigates how supply noise causes jitter. For the analysis, a band-limited white noise is assumed at the supply. After the cause of jitter is investigated, a cancellation scheme is proposed. Finally, simulation results are shown.

Fig. 5.27 shows the left half cell of the oscillator with V_{DD} supply noise. Since the noise is in series with R therefore its transfer function to the output jitter is similar to the resistor noise.

Fig. 5.28 shows the left half cell of the oscillator with V_{SS} supply noise. Since the noise is still in series with R therefore its transfer function to the output jitter will also be similar to the resistor noise. Apart from this there is a high frequency path though the capacitor C.

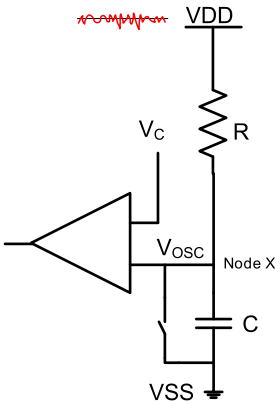

Fig 5.28- Left half cell of the oscillator with V_{DD} noise.

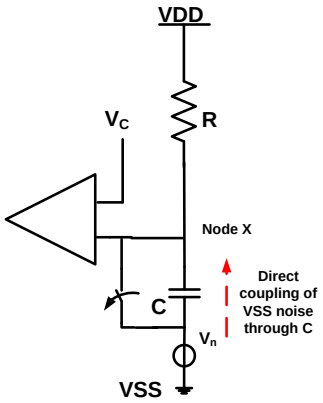

Fig 5.27- VSS supply noise.

Transfer functions for both the supply noise are calculated in Appendix C. One way to cancel the supply noise is to ensure that the transfer function of the supply noise to the Node X is same as its transfer function to V_C. A filter is designed with such a transfer function and placed before the V_C node. The complete circuit is shown in Fig. 5.29 (design of the filter is discussed in Appendix C).

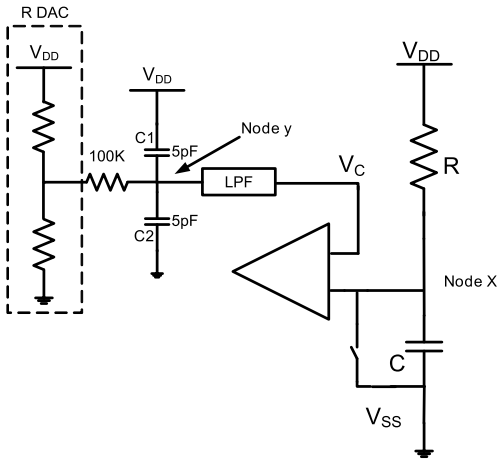

Fig 5.29- Noise cancellation for low frequency supply noise.

To see the effectiveness of supply noise cancellation, jitter was simulated for various supply noise floors at fixed NBW (Noise BandWidth) =16MHz. Fig.30 and Fig.31 show the jitter due to V_{DD} and V_{SS} supply noise respectively. As can be seen from the figures, a ≈ 4X/6X improvement in jitter performance is obtained, with respect to the previous DCO, for supply V_{DD}/V_{SS} noise (noise floor of $400nV/\sqrt{Hz}$).

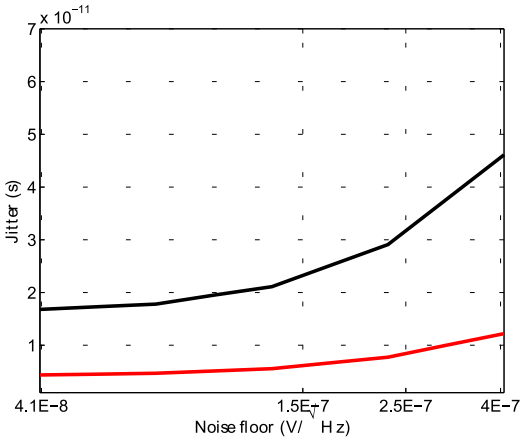

Fig 5.30- Jitter vs. the V_{DD} supply noise floor level. The dashed line is the jitter of the previous design and red line is the jitter of the new design.

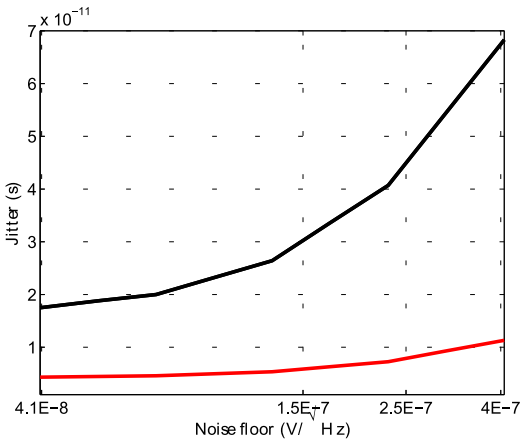

Fig 5.31- Jitter vs. the V_{SS} supply noise floor level. The dashed line is the jitter of the previous design and red line is the jitter of the new design.

5.3.7 Jitter simulations across process

Simulations are done to ensure that the jitter specification is met across the process corners/temperatures. Table 5.1 shows the jitter values for different process and temperatures. Here the jitter is only due to the noise inherent to the circuit. The worst case jitter is 5.32pS. In addition to this, 2.5pS of jitter is contributed by the residual quantization noise of the delta-sigma DAC. Thus, total jitter is ~5.9pS. In comparison, the worst case jitter of the previous design was 24pS.

Temp	Nominal	snsp	fnfp	snfp	fnsp
-55^{0}C	3.96	3.76	4.11	3.8	4.11
27^{0}C	4.19	4.06	4.38	4.03	4.28
125^{0}C	5.03	4.92	5.25	5.32	5.04

Table 5.1- Period Jitter across temperature and process

5.3.8 **Frequency variation with supply voltage**

In this section, frequency variation with supply voltage is determined. This is important as it is one of the factors that determine the fine DAC's full scale range. From Eq. 5.1.3, the variation of time period with V_{DD} can be derived. It should be noted that V_C is derived from V_{DD} using a resistor divider (DAC). Thus, V_C can be given by,

$$V_C = \alpha V_{DD} \tag{5.1.11}$$

Where α is determined by the resistor ratio in the DAC. Substituting Eq. 5.1.11 in Eq. 5.1.3, the following relation is obtained.

$$T_{OSC} = 2\left[t_d + RC\ln\left(\frac{V_{DD}}{V_{DD} - \alpha V_{DD}} \right) \right] = 2\left[t_d + RC\ln\left(\frac{1}{1-\alpha} \right) \right] \tag{5.1.12}$$

Thus, frequency is, to the first order, independent of V_{DD} voltage. Simulations are done to see the variation of frequency with supply voltage V_{DD}. For a supply voltage variation from 1.7V-1.9V, the frequency varies by 180 KHz which is ~1% of the output frequency.

5.4 **DCO Results**

Table 5.2 below shows a comparison of this DCO with the DCO in the previous chip. A ~4X improvement in period jitter and resolution are obtained. The current consumption has increased to 255µA. This is not a major issue as the DCO contributes < 15% to the total power of the frequency reference. The FOM of the new DCO is 150dB ($FOM = \gamma(f)\left(\frac{f_m}{f_{OSC}} \right).P.10^3$ [7]). This FOM can be further improved by using a lower supply voltage. Moreover, only one comparator is active every half cycle. Thus, the other comparator can be put in to sleep mode i.e. its bias current can be switched off, hence, improving its FOM even further.

The FOM of the current state of the art relaxation oscillator is 162dB [32]. This is achieved by cancelling the noise of the comparator and using a faster process (65nm CMOS). Although, this design has an excellent phase noise performance but has poor supply noise rejection. There are several paths through which noise can couple to the output. In comparison, the DCO described in this chapter, has a good supply noise rejection (refer to Fig 5.30 and Fig 5.31 for a comparison with the previous DCO).

	New DCO	Previous DCO
Center Frequency	16MHz	16MHz
Resolution	60ppm	200ppm
Period jitter (circuit) nom-worst	4.9ps-5.9ps	16ps-24ps
Period jitter (V_{DD} noise)	12ps (407 nV/√Hz), 5.2ps (128 nV/√Hz)	45ps (407 nV/√Hz), 21ps (128 nV/√Hz)
Period jitter (V_{SS} noise)	11ps (407 nV/√Hz), 5.2ps (128 nV/√Hz)	68ps (407 nV/√Hz), 28ps (128 nV/√Hz)
Frequency variation (across supply 1.7V – 1.9V)	180KHz	170KHz
Frequency variation (across temperature) -55^0C – 125^0C	230KHz	300KHz

Table 5.2- Comparison between the new DCO and the previous DCO

5.5 Conclusion

In this chapter, a DCO was presented with an improved resolution and jitter performance. A new architecture is used to reduce the noise contributed by the current reference of the previous DCO. Optimum values of various parameters such as the control voltage V_C, timing resistor $R_{1,2}$ and $C_{1,2}$ are calculated to minimize noise. To improve the resolution of the DCO, oversampling and noise shaping are used. Also, a supply noise cancellation circuit is proposed which improves the jitter by 4-6X in comparison to the previous DCO.

6 Conclusion

This chapter summarizes the results obtained during this thesis and provides few recommendations for future work.

Section 6.1 gives an overview of the conclusions that can be made based on the measurements, analysis and simulations done in this thesis. Subsequently, recommendations for future work are provided in Section 6.2.

6.1 Conclusions

In the context of TD based frequency reference, the following conclusions can be made.

1) It is found that a maximum accuracy of ±400ppm (-35^0C to 125^0C) can be achieved using silicon ETFs even with a two temperature trim. An electrothermal FLL implemented using a silicon ETF with s=10µm and driven at 256 KHz achieves an absolute accuracy of ±600ppm over the temperature range of -35^0C to 125^0C.
2) An oxide ETF over temperature shows a reduction of temperature sensitivity by 2-3 times with respect to 4.7µm Silicon ETF.
3) As a function of variations in the thickness of the oxide layer, the oxide ETF has an initial process spread of five times larger than the silicon ETF.
4) An electrothermal FLL based on oxide ETF achieves an absolute output frequency inaccuracy of ±500ppm. This inaccuracy is due to the residual temperature sensitivity of the ETF, limited trimming resolution, limited DCO resolution and jitter. With an improved DCO resolution and jitter performance, an inaccuracy of ~ ±300ppm should be achievable.
5) The DCO resolution is improved by 4X using oversampling and noise shaping in the DAC.
6) Period jitter of the DCO has been reduced by more than 3X. This is achieved by eliminating the major sources of noise, using optimum values of control voltage, timing resistances and capacitors.
7) A supply noise cancellation circuit is proposed which improves period jitter by 6X (VDDA supply noise)/4X(VSSA supply noise). The circuit is verified using simulations.

6.2 Future Work

Based on the work done in this thesis few recommendations can be made for future work.

1) Only one possible structure was fabricated for oxide ETF. There are several other possibilities which can potentially give better results. These structures can be fabricated and measured.
2) The modeling for oxide ETF is difficult and hence a more empirical approach is followed in this thesis. If a model can be developed then it would be useful for making more

informed decisions on various parameters of an oxide ETF (such as the thermopile length etc).

3) DCO designed in this thesis has not been fabricated. A natural step would be to fabricate the DCO and verify its performance in silicon.

Appendix A

In this appendix, a transfer function of the ETF noise to the output frequency is calculated (the analysis done here follows a similar approach as in [9]).

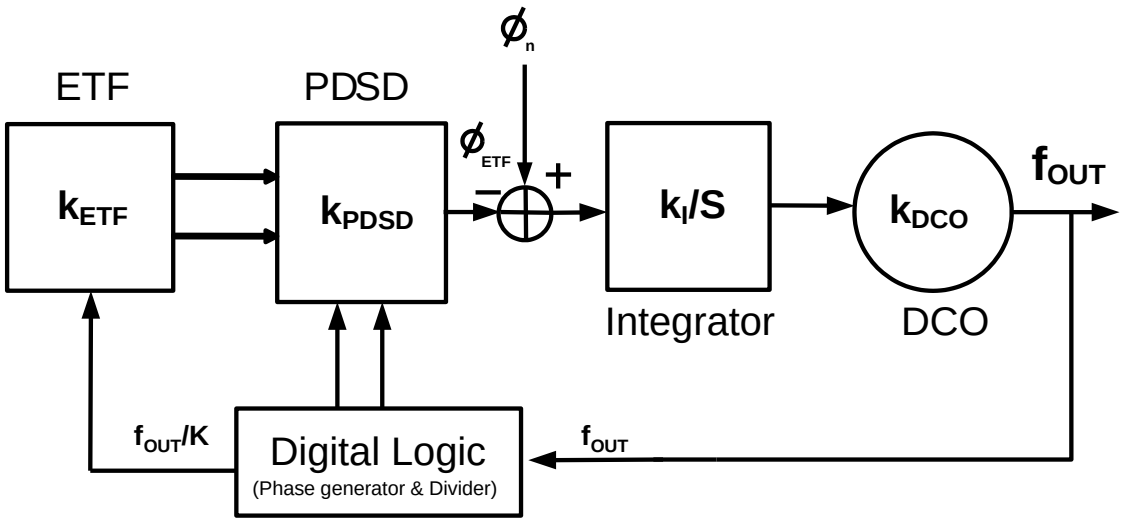

Fig. A.1 - An s-domain model of the digital electrothermal FLL

An s-domain model of an electrothermal FLL is seen in Fig.A.1. ϕ_n models the thermal noise floor of the ETF and PDSD modulator together. The ETF is replaced with a small signal gain of k_{ETF}. Since, this gain is for a small signal around the steady state point on the phase-frequency curve; it can be calculated by differentiating Eq. 2.1.5 which relates the phase shift and driving frequency of an ETF. Therefore, k_{ETF} is given by;

$$k_{ETF} = \frac{d\phi}{df} = \frac{\phi}{2 f_{drive}} \tag{A.1}$$

In Eq.A.1, the ETF is driven at $f_{drive} = \frac{f_{OUT}}{K}$. In the model, k_{PDSD} is the gain of the PDSD which converts the analog phase into a 15-bit digital number. This gain is equal to 32768/90 (15 bits ,2^{15}=32768, are used to represent a phase range of 90^0). Therefore, ϕ_{ETF} is given by,

$$\phi_{ETF} = 2k_{ETF} \frac{f_{OUT}}{K} . k_{PDSD} \tag{A.2}$$

Further, k_I is the integrator gain which is equal to the sampling frequency multiplied by a programmable digital number. Thus, $k_I = F_S \times d$ where F_S =42 KHz and d=1/16 are same as in [9]. k_{DCO} is the DCO gain and is equal to ~4 KHz/LSB (the DCO resembles the one used in [9]).

Thus, the noise transfer function can be calculated as;

$$Tf = \frac{f_{OUT}}{\phi_n} = \frac{1}{2\pi}\left[\frac{\frac{K}{k_{ETF}k_{PDSD}}}{1+\frac{sK}{k_{ETF}k_{PDSD}k_I k_{DCO}}}\right] \tag{A.3}$$

From Eq. A.1, the closed loop DC gain is equal to $\frac{K}{2\pi k_{ETF}k_{PDSD}}$ and the loop bandwidth is equal to $\frac{k_{ETF}k_{PDSD}k_I k_{DCO}}{K}$. Since this is a first order system, the noise bandwidth is equal to;

$$NBW = \frac{\pi}{2}\frac{k_{ETF}k_{PDSD}k_I k_{DCO}}{K} \tag{A.4}$$

From these equations, total noise in the output frequency is given by;

$$f^2_{OUT,noise} = \phi_n^2 \cdot \left|\frac{K}{2\pi k_{ETF}k_{PDSD}}\right|^2 .NBW$$

$$f^2_{OUT,noise} = \phi_n^2 \cdot \left|\frac{K}{2\pi k_{ETF}k_{PDSD}}\right|^2 \cdot \frac{\pi}{2}\frac{k_{ETF}k_{PDSD}k_I k_{DCO}}{K}$$

$$f^2_{OUT,noise} = \phi_n^2 \cdot \frac{K.k_I k_{DCO}}{8\pi k_{ETF}k_{PDSD}} = \phi_n^2 \cdot \frac{f_{OUT}k_I k_{DCO}}{4\pi\phi_{ETF}} \tag{A.5}$$

Where k_{ETF} has been replaced by $\frac{\phi_{ETF}K}{2f_{OUT}}$ from Eq. A.2.

From Eq. A.5, the jitter in ppm is given by;

$$\frac{f_{OUT,noise}}{f_{OUT}} = \frac{\phi_n}{\sqrt{\phi_{ETF}}} \cdot \sqrt{\frac{k_I k_{DCO}}{4\pi f_{OUT}}} \tag{A.6}$$

The second term on the right hand side is a constant for a given DCO and output frequency (although k_I can be varied, as it is programmable, but it is assumed as constant in this section). The first term on the right hand side is the noise floor divided by the ETF phase. This term will vary with the ETF size and driving frequency. For a constant bandwidth Bw, $\frac{\phi_n B}{\sqrt{\phi_{ETF}}}$ ($B = \sqrt{Bw}$) is plotted in Fig.A.2, for the three ETFs at different driving frequencies, to find their optimum values.

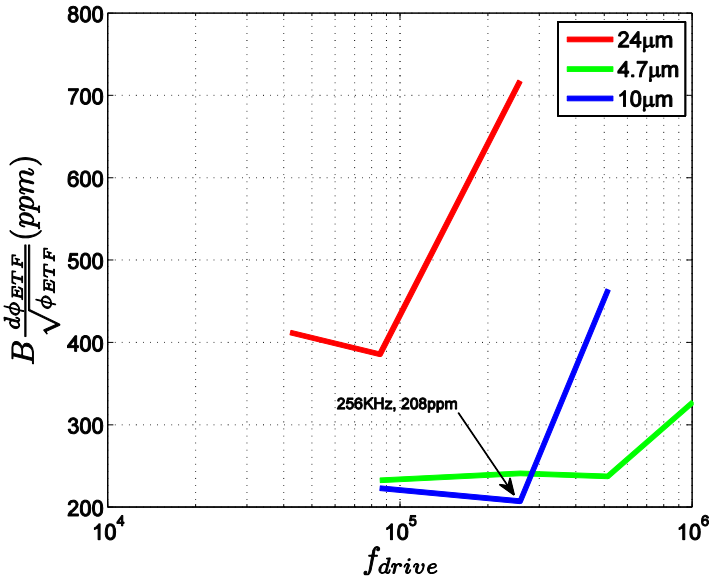

Fig. A.2 - $B\frac{d\phi_{ETF}}{\sqrt{\phi_{ETF}}}$ **vs. driving frequency for the three ETFs**

For all the three ETFs, the sampling frequency of PDSD is kept the same. Also, the measurements are done at room temperature. As can be seen from the above figure, the minimum $\frac{\phi_n B}{\sqrt{\phi_{ETF}}}$ is obtained for s=10µm ETF at f_{drive} of 256 KHz. Thus, the jitter at the frequency output, due to the ETF, is minimal at this point.

Appendix B

In this appendix, a relation between timing resistor noise and jitter is derived. Using this relation, optimum values of $R_{1,2}$, $C_{1,2}$ and V_C are derived analytically for minimum jitter and compared with simulation results.

Resistor Noise

The thermal noise of resistors $R_{1,2}$ causes timing jitter at the output of the comparator. The noise analysis is done on half circuit of the oscillator for simplicity.

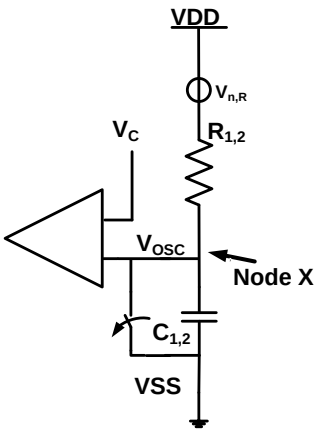

Fig B.1 - Half circuit of the oscillator for noise analysis.

The Thevenin equivalent of the $R_{1,2}$ resistor noise is a voltage source in series with the supply voltage V_{DD}. The supply voltage that the timing elements ($R_{1,2}$ and $C_{1,2}$) see is then equal to equivalent supply voltage $V_{DD}^{'} = V_{DD} + V_{n,R}$. It can be seen from Eq.5.1.4 that the time period of oscillation will change with the change in equivalent supply voltage. This is depicted in Fig. B.2.

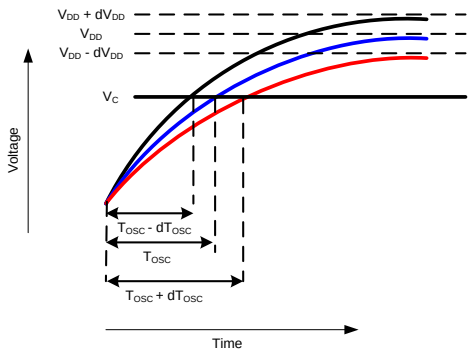

Fig B.2 – Change in oscillation period with change in V_{DD}.

The linear approximation of the change in time period with the change in $V_{DD}^{'}$ is given by (obtained by differentiating Eq. 5.1.4),

$$dT_{OSC} = \frac{RC}{V_{DD} - V_C} \frac{V_C}{V_{DD}} dV_{DD}^{'} \tag{B.1}$$

This equation can be used to predict the statistics of dT_{OSC} for an *average* change in $V_{DD}^{'}$ [8] .The average change in $V_{DD}^{'}$ is due to the white noise of the resistor. This noise is averaged over a time window of half the oscillation period (Fig. B.3).

$$dV_{DD}^{'} = \frac{1}{\left(\frac{T_{OSC}}{2}\right)} \int_0^{\frac{T_{OSC}}{2}} V_{n,R}.dt \tag{B.2}$$

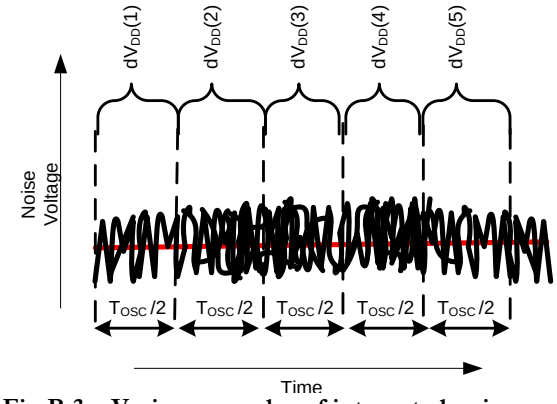

Fig B.3 – Various samples of integrated noise are calculated by shifting the integration window

But this is just one sample. To find the RMS value of $dV_{DD}^{'}$ several samples are needed. This can be done by convolving the noise voltage with a rectangular time window $w_{\frac{T_{OSC}}{2}}$ of width $\frac{T_{OSC}}{2}$ (This is similar to the analysis done in [34]).

$$dV_{DD}^{'}(t) = \frac{1}{\left(\frac{T_{OSC}}{2}\right)} \int_0^{\infty} V_{n,R}(t) \times w_{\frac{T_{OSC}}{2}}(t-x)dx \tag{B.3}$$

where each value of *t* gives a different sample. The convolution can be replaced by multiplication in the frequency domain. This is given by

$$S_{dV_{DD}}(f) = \frac{4}{T_{OSC}^2} |W_{\frac{T_{OSC}}{2}}(f)|^2 \times S_{V_{n,R}}(f) \tag{B.4}$$

[8] Although white noise has zero mean but its variance is non zero. This implies that noise integrated over finite time will also have non zero variance. The noise integrated over finite time will have zero mean over several samples but the value of each sample may not be zero.

In the above equation, $S_{v_{n,R}}(f)$ is the single sided power spectral density of the resistor noise. Magnitude of the Laplace transform of a rectangular window is

$$|W_{\frac{T_{OSC}}{2}}(s)| = \frac{T_{OSC}}{2}\text{sinc}(f\frac{T_{OSC}}{2}) \tag{B.5}$$

This is a low pass sinc filter with notches at multiples of $f = \frac{2}{T_{OSC}}$. Further, it is already known that $S_{v_{n,R}}(f)$ has white Gaussian spectrum. Therefore, the mean square value of dV_{DD} can be calculated as follows.

$$\langle dV_{DD}^2 \rangle = \sigma_{V_{DD}}^2 = \int_0^\infty S_{dV_{DD}}(f)df = \frac{4}{T_{OSC}^2}\int_0^\infty |W_{\frac{T_{OSC}}{2}}(f)|^2 \times S_{v_{n,R}}(f)df \tag{B.6}$$

Substituting $W_{\frac{T_{OSC}}{2}}(s)$ and $S_{v_{n,R}}(f)$ in the above equation and solving,

$$\sigma_{V_{DD}}^2 = \frac{4}{T_{OSC}^2}S_{v_{n,R}}(f).\frac{T_{OSC}}{4} = \frac{4KTR}{T_{OSC}} \tag{B.7}$$

Thus jitter can be found by substituting the RMS value of $dV_{DD}^{'}$ in Eq. B.1.

$$\sigma_{\frac{T_{OSC}}{2}} = \frac{\frac{V_C}{V_{DD}}}{\frac{V_{DD}-V_C}{RC}}\sigma_{V_{DD}} = \frac{\frac{V_C}{V_{DD}}}{\frac{V_{DD}-V_C}{RC}}\sqrt{\frac{4KTR}{T_{OSC}}} \tag{B.8}$$

This equation gives the jitter for one of the half cycles. Therefore, the period jitter is given by.

$$\sigma_{T_{OSC}} = \sqrt{2}\,\frac{\frac{V_C}{V_{DD}}}{\frac{V_{DD}-V_C}{RC}}\sqrt{\frac{4KTR}{T_{OSC}}} \tag{B.9}$$

Increasing R while keeping other variables constant will have an adverse effect on jitter performance. Thus, R should be kept at minimum value. Further, V_C needs to be optimized as it appears in both the numerator and the denominator.

It can also be argued that $V_{n,R}$ will be low pass filtered by the RC network and thus will cause a change in voltage at Node X. This effect has been neglected in this derivation as $RC < \frac{T_{OSC}}{8}$.

In the next few paragraphs, optimum values of reference voltage V_C, $R_{1,2}$ and $C_{1,2}$ are calculated.

Optimum V_C, $R_{1,2}$ & $C_{1,2}$

Optimum value of V_C can be derived by minimizing Eq. B.9 for a given oscillation frequency. To perform this minimization all the other variables should be written in terms of V_C. $(RC)_{1,2}$ and V_C are related by Eq. 5.1.4 as,

$$\frac{T_{OSC}}{2\ln\left(\frac{V_{DD}}{V_{DD}-V_C}\right)} = RC \tag{B.10}$$

$(RC)_{1,2}$, as defined above, can be substituted in Eq. B.9 to obtain jitter in terms of V_C, σ_R and constants such as the oscillation frequency and V_{DD}. Further, $\sigma_{V_{DD}} = \sqrt{\frac{4KTR_{1,2}}{T_{OSC}}}$ can be expressed in terms of V_C and $C_{1,2}$ using Eq. B.7. For a given $C_{1,2}$ =1pF, V_{DD} =1.8V and f_{OSC} =16MHz, Eq. B. 9 is minimized with respect to V_C to obtain $V_{C,opt}$ =1.05V.

In order to confirm this derivation, the oscillator circuit is simulated for various V_C and the jitter is plotted in Fig.B.4. In the simulations, $R_{1,2}$ and V_C are varied for a given f_{OSC}, $C_{1,2}$ and V_{DD}.

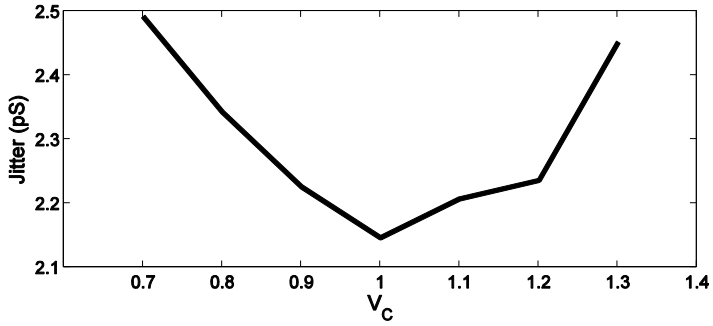

Fig B.4 - Jitter variation across V_C

Fig.B.4 shows that $V_{C,opt}$ =1V which is close to the result obtained from calculations. In the above derivation and simulation the comparator has been assumed ideal. To make sure there is enough biasing margin for all the transistors in the comparator, V_C = 0.9V has been taken for this design (comparator design is discussed in Sec. 5.2.3.4). It can be observed from Fig B.2 that a lower value for V_C (=0.9V) results only in a marginal increase in jitter.

As discussed earlier, $R_{1,2}$ should be kept at minimum value to reduce jitter. Since $(RC)_{1,2}$ is fixed therefore $C_{1,2}$ should be kept as large as possible to reduce jitter. But area constrains limit

$C_{1,2}$ to lower values. To ensure that $C_{1,2}$ does not contribute significantly to jitter (indirectly through $R_{1,2}$) and area specification, $C_{1,2}$ = 1pF is chosen for this design.

Appendix C

In this appendix, relations between V_{DD}/V_{SS} supply noise to oscillator jitter are derived. Using these relations, a supply noise cancellation technique is described.

V_{DD} Supply Noise

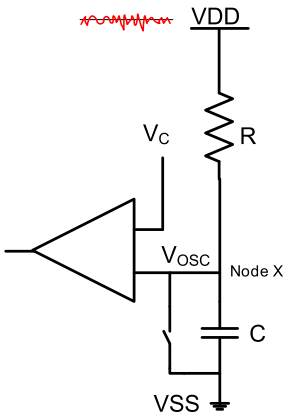

Fig C.1 - Left half cell of the oscillator with V_{DD} noise.

Noise on V_{DD} has a similar effect on jitter as the timing resistor noise (Appendix B). Therefore, the jitter due to the V_{DD} supply noise can be defined as,

$$\sigma_{T_{OSC},V_{DD}} = \sqrt{2}\,\frac{\frac{V_C}{V_{DD}}}{\frac{V_{DD}-V_C}{RC}}\,\sigma_{V_{DD}} \qquad \text{(C.1)}$$

Where $\sigma_{V_{DD}}$ is the rms noise voltage on V_{DD}. As in the case of timing resistor noise, the supply noise is low pass filtered by a sinc filter with the first notch at $f = \frac{2}{T_{OSC}}$.

V_{SS} Supply Noise

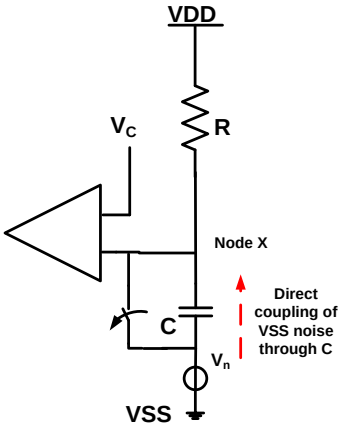

Fig C.2- VSS supply noise.

The effect of V_{SS} supply noise is similar to V_{DD} supply noise apart from the fact that noise at frequency $f > \frac{1}{2\pi RC}$ directly couples to the node X through the capacitor C (as shown in Fig.C.2). Although the noise at higher frequencies does not affect the charging of node x but it now effects the triggering point. Therefore, jitter due to V_{SS} noise at $f < \frac{1}{2\pi RC}$ is given by,

$$\sigma_{T_{OSC},V_{SS}} = \sqrt{2}\frac{\frac{V_C}{V_{DD}}}{\frac{V_{DD}-V_C}{RC}}\sigma_{V_{SS}} \tag{C.2}$$

where $\sigma_{V_{SS}}$ is rms noise at V_{SS} within $0 < f < \frac{1}{2\pi RC}$. And jitter due to V_{SS} noise at $f > \frac{1}{2\pi RC}$ is given by (refer to Eq. 5.1.6),

$$\sigma_{T_{OSC},V_{SS}} = \sqrt{2}\frac{\sigma_{V_{SS}}}{\frac{V_{DD}-V_C}{RC}} \tag{C.3}$$

where $\sigma_{V_{SS}}$ is rms noise at V_{SS} for $f > \frac{1}{2\pi RC}$ and $\frac{V_{DD}-V_C}{RC}$ is the slope of the charging waveform at the triggering point.

Supply Noise Cancellation Circuit

One way to cancel the supply noise is to ensure that the transfer function of the supply noise to the Node X is same as its transfer function to V_C. A filter is designed with such a transfer function and placed before the V_C node.

The transfer functions of the supply noise to output jitter are summarized below:

1) V_{DD} supply noise – In Eq. C.1, it can be noted that $\frac{V_{DD}-V_C}{RC}$ is the slope of the timing waveform at the triggering point. Therefore this jitter can also be expressed as

$$\sigma_{T_{OSC},V_{DD}} = \sqrt{2}\frac{1}{S}\frac{\sigma_{V_{DD}}}{2} \tag{C.4}$$

for V_C =0.9V, V_{DD} =1.8V and $S = \frac{V_{DD}-V_C}{RC}$.

2) V_{SS} supply noise – As in the previous case, jitter due to noise at $f < \frac{1}{2\pi RC}$ can be expressed as

$$\sigma_{T_{OSC},V_{SS}} = \sqrt{2}\frac{1}{S}\frac{\sigma_{V_{SS}}}{2} \tag{C.5}$$

3) V_{SS} supply noise – Jitter due to noise at $f > \frac{1}{2\pi RC}$ can be expressed as $\sigma_{T_{OSC},V_{SS}} = \sqrt{2}\frac{1}{S}\sigma_{V_{SS}}$.

$$\sigma_{T_{OSC},V_{SS}} = \sqrt{2}\frac{1}{S}\sigma_{V_{SS}} \tag{C.6}$$

The jitter due to supply noise can be compensated by adding equivalent amount of noise to reference voltage V_C. Jitter due to noise in V_C would be equal to (Eq. 5.1.5)

$$\sigma_{T_{OSC},V_C} = \sqrt{2}\frac{\sigma_{V_C}}{S} \tag{C.7}$$

Comparing the above equation with Eq. C.4 and Eq. C.5, it can be observed that the jitter can be compensated by adding half the noise in supplies to V_C.

The voltage V_C is supplied by the DAC followed by a low pass filter (Fig 5.14). Thus, a 10pF cap is already connected between V_C and V_{SS}. Jitter mentioned in points 1 and 2, above, can be compensated as shown in Fig. C.3.

Any noise on either V_{DD} or V_{SS} appears at node y after attenuation by a factor of 2 (determined by capacitor ratio $\frac{C_1}{C_2}$). This noise is low pass filtered (by the LPF) so that cancellation can be obtained for points 1 and 2 stated above (contribution of high frequency noise to $\sigma_{V_{DD}}$ is limited by the sinc filter). The LPF is implemented using an Npoly resistor and a MIM capacitor. The value of MIM cap is chosen as 2pF (> 10 times the C_{GD} of comparator input transistor) so that any kickback from the comparator, on the reference node (V_C), is reduced. The MIM capacitor also provides a path, to the node V_C, for the high frequency noise on V_{SS} supply resulting in cancellation for point 3 above.

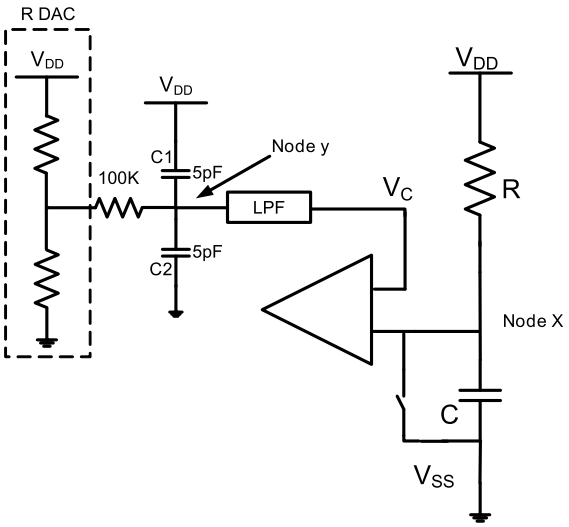

Fig C.3 - Noise cancellation for low frequency supply noise.

Simulations are performed for determining an optimum cut-off frequency for the LPF. To get a starting point for the simulation, the rms noise at V_C (σ_{V_C}) due to the V_{DD} supply noise is equated to $\frac{\sigma_{V_{DD}}}{2}$ (refer to Eq. C.4 and Eq. C.7),

$$\sigma_{V_C} = \frac{\sigma_{V_{DD}}}{2} = \sqrt{\left(\frac{v_{n,V_{DD}}}{2}\right)^2 B\frac{\pi}{2}} = \frac{1}{2}\sqrt{\int_0^{NBW}\left(v_{n,V_{DD}}\,\mathrm{sinc}(\frac{\pi}{2}fT_{OSC})\right)^2 df} \qquad \text{(C.8)}$$

where B is the bandwidth of the 1st order low pass filter, NBW is the noise bandwidth of the band-limited white noise on the V_{DD} supply. From the above equation, $B \approx 9MHz$ is obtained for NBW of the white noise equal to $16MHz \times \frac{\pi}{2}$.

The supply noise can be simulated as shown in Fig C.4 [35]. Wide band thermal noise is added using a resistor R_0. A low pass filter is used to band limit the supply noise.

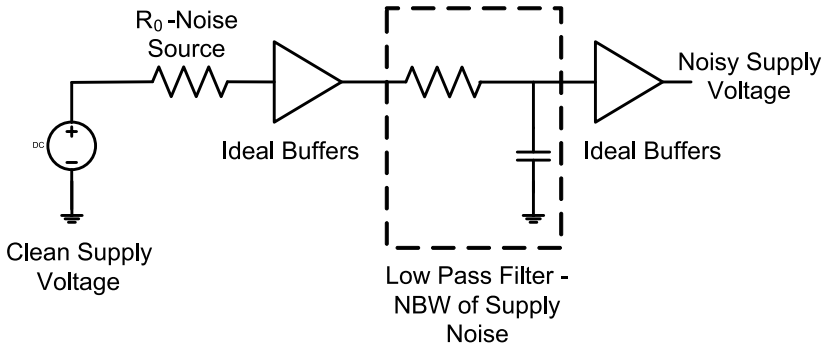

Fig C.4- Circuit for adding noise to supply.

To find the optimum bandwidth of the LPF in the noise cancellation circuit, jitter is simulated for different NBW of supply noise. Fig C.5 and Fig C.6 show the jitter due to V_{DD} and V_{SS} supply noise respectively, for varying bandwidth of the LPF. It can be observed, from these figures, that around the LPF bandwidth of around 10MHz, jitter is less for all the four simulated NBW. Thus, R=8K is chosen corresponding to the bandwidth of 10MHz. Nevertheless, this resistance can be made *trimmable* in the actual implementation.

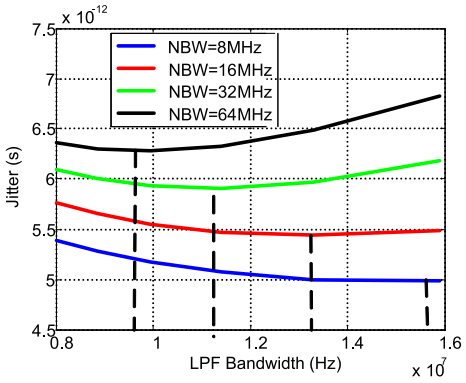

Fig C.5 -Jitter due to V_{DD} supply noise vs. Bandwidth of the LPF for different NBW.

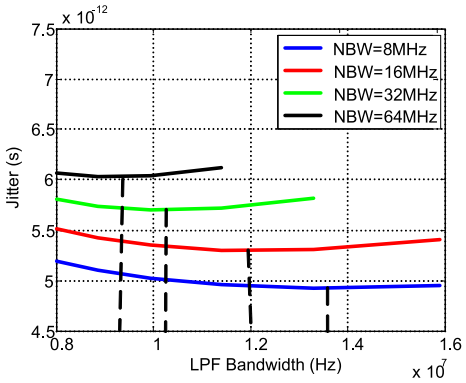

Fig C.6- Jitter due to V_{SS} supply noise vs. Bandwidth of the LPF for different NBW.

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