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***Abstract*—Identifying faulty lines and their accurate location is key for rapidly restoring distribution systems. This will become a greater challenge as the penetration of power electronics increases, and contingencies are seen across larger areas. This paper proposes a single terminal methodology (i.e., no communication involved) that is robust to variations of key parameters (e.g., sampling frequency, system parameters, etc.) and performs particularly well for low resistance faults that constitute the majority of faults in low voltage DC systems. The proposed method uses local measurements to estimate the current caused by the other terminals affected by the contingency. This mimics the strategy followed by double terminal methods that require communications and decouples the accuracy of the methodology from the fault resistance. The algorithm takes consecutive voltage and current samples, including the estimated current of the other terminal, into the analysis. This mathematical methodology results in a better accuracy than other single-terminal approaches found in the literature. The robustness of the proposed strategy against different fault resistances and locations is demonstrated using MATLAB simulations.**

***Index Terms*—Power system protection, microgrids, Power distribution faults, fault location.**

I. Introduction

Low voltage DC (LVDC) will play a vital role in future low-carbon electrical energy systems with solar photovoltaics, electric vehicles, etc. [1]. Potentially, LVDC will enable the use of power-denser hardware and bring less stand-by losses, more control flexibility, and higher power quality [2]–[4]. The protection of DC systems requires reliability, security, dependability, and selectivity [4] to identify and locate a fault. Therefore, fault identification techniques help reduce the impact of contingencies, whereas location methods allow a timely restoration of the system. Fault location methods are divided into two categories in the literature: offline and online methods. Offline methods calculate the fault location after the fault has been cleared. In contrast, online methods evaluate the fault distance after the fault has been identified but before it is cleared.

Discussing the offline methods in the literature, the authors in [5]–[7] use a probe power unit (PPU) as an active external injection unit. The authors in [5] neglect the damping coefficient in the second-order RLC discharging circuit, taking the damped frequency to be equal to the natural frequency. This results in a loss of accuracy of the fault distance location. Authors in [6] use a least squares algorithm to evaluate the damping i.e., attenuation constant. However, the method's accuracy is compromised when the attenuation constant is high. Paper [7] uses a modified PPU to calculate a high value for the attenuation constant and, therefore, evaluate the fault distance with higher accuracy compared to [5]–[8]. The authors in [9] use a fault location module consisting of an inductor, two switches, and two thyristors to achieve an accuracy of 98.4% for low resistance faults in an LVDC system. However, the method in [9] is prone to white Gaussian noise (WGN) in measurement as it uses a differential term (*di/dt*) in the analysis of the fault location. Authors in [10] propose an iterative method to evaluate the fault location for pole-to-ground (PTG) faults without any external modification. However, this method has a dead zone for faults closer to the bus and for pole-to-pole (PTP) faults [11]. Additionally, it is desirable to have a robust online method over its offline counterpart. Regarding online methods, the authors in [11] propose using a current limiting reactor (CLR) in single and double terminal fault location methods. The analysis is robust and convincing based on the ratio of transient voltages (ROTV). The authors in [13] use an improved solid-state circuit breaker (SSCB) to propose a curve-fitting method. However, the parameter extraction method presents low accuracy when the fault occurs close to the bus [18]. Paper [14] uses multiple capacitive earthing points as an external modification that can be used to locate faults. The authors in [16], [17] use current and voltage measurements from both ends to formulate a fault location method without any external modification. The method from [16] uses a Moore–Penrose pseudo-inverse, whereas the authors in [17] use an iterative approach for fault location. However, the performance in [16], [17] and [14] is affected by WGN. Moreover, papers [16], [17] require synchronized double terminal data for accurate fault location. The authors in [12] propose a Newton-Raphson-based fault detection and location method for low-resistance faults and a ground current

TABLE I: FAULT LOCATION METHODS IN LITERATURE

Fault Location Methods	Location Sequence/Differential Term	Other Terminal Considered?	Degree of External Modification Required?
[11], [12]	Online/No	No	low, current limiting reactor
[13]	Online/No	No	high, improved solid-state circuit breaker
[14]	Online/Yes, prone to WGN	No	high, multiple capacitance earthing
[15]	Online/No	Yes, estimates other terminal current	Not required, high sampling frequency
[9]	Offline/Yes, prone to WGN	No	high, Fault location module
[16]- [17]	Online/Yes, prone to WGN	Yes, require synchronous data	Not required
[10]	Offline/Yes, prone to WGN	No	Not required
[5]- [7]	Offline/No	No	high, Probe power unit
[18]	Online/No	Yes, requires asynchronous data	high, modified T-source circuit breaker
[Proposed method]	Online/No	Yes, estimates other terminal current	low, current limiting reactor

relay to locate high-resistance faults (up to 25Ω). However, this method assumes an overdamped response of current and voltages in the analysis, even for low-resistance faults. This reduces the accuracy of the fault location strategy under low fault resistance scenarios. The authors in [18] use a modified T-source circuit breaker in a method that is robust to WGN and effective to high fault resistance. However, the method requires double terminal asynchronous data to eliminate the influence of fault resistance.

This paper presents an online single-terminal fault location method for flexible (point-to-point or multi-terminal) LVDC systems. The novelty of this method lies in improving the fault location accuracy for low resistance faults up to 1 Ω, which constitute the majority of faults in LVDC systems (usually with low resistive earthing [14], [19]). Low voltage systems have a high possibility of experiencing low resistance pole-to-ground faults. Likewise, short circuit pole-to-pole faults are less likely to occur, and high resistance pole-to-ground faults are rare [5], [13].

The proposed approach is based on estimating the current of other terminals that are being directly affected during a fault using only local measurements. Including the estimated current in the single terminal iterative fault location method improves fault location accuracy. However, as the fault resistance increases, the fault current contribution in the analysis reduces. As a result, the merit of using estimated current reduces for high fault resistances. The proposed method shows similar accuracy to conventional single terminal methods [5]–[7], [11] for higher fault resistances up to 5 Ω. Therefore, the fault location method is accurate and applicable for a conventional LVDC system with a fault resistance ranging from 0-5 Ω. Briefly, the proposed location method has the following key attributes:

- Single-terminal. The proposed method does not require information from other terminals to locate the fault. This reduces its cost and complexity. However, single-terminal methods are dependent on fault resistance. The proposed work estimates other terminals' current to mimic the double terminal methods' methodology. This eliminates the dependence of fault location accuracy on fault resistance, improving the accuracy of fault location.
- No differential term. The method is robust against WGN in measurements as it replaces the differential current term with the voltage across CLRs since the use of differential terms (*di/dt* and *dv/dt*) in the mathematical analysis make these approaches prone to the loss of accuracy in the presence of WGN in measurements.
- Minimum external modification. To optimise the cost of the LVDC systems, it is important to do minimum changes to the existing systems for the purpose of control, operation and protection. The proposed method requires a low degree of external modification in the form of CLRs [11], [12], which is widely suggested and used in literature for the protection of DC systems. This reduces the cost and complexity of the fault location method compared to other strategies such as [13] (improved solid-state circuit breakers), [14] (multiple capacitive earthing points), [9] (fault location module), [18] (modified T-source circuit breaker).

The rest of the paper is organized as follows. Section II describes the test system. Section III presents the fault location algorithm using the estimation of the current experienced by other terminals and the related validation in MATLAB/Simulink. Finally, section IV brings the conclusions of the work.

II. TEST SYSTEM CONFIGURATION

The fault location algorithm is developed to be used either in a point-to-point or multi-terminal distribution system. Therefore, two systems with identical elements but different configurations (i.e. one as a multi-terminal and the other as a point-to-point) are considered in Fig. 1. These systems operate at ±380V and are formed by 6 buses. The LVDC system consists of a fuel cell on Bus 1, an AC grid on Bus 2, a photovoltaic system on Bus 3, and an energy storage system on Bus 6. Buses 4-5 have AC loads, DC loads, and constant power loads [20]. Benchmark controllers used in conventional LVDC system applications have been implemented to validate the analysis [21].

The system needs the addition of CLRs to limit the rate of change of the current during faults. For the point-to-point configuration, CLRs are present at both cable terminals. However, for a multi-terminal configuration, CLRs may not be present at both cable terminals (see Fig. 1(b)). As a

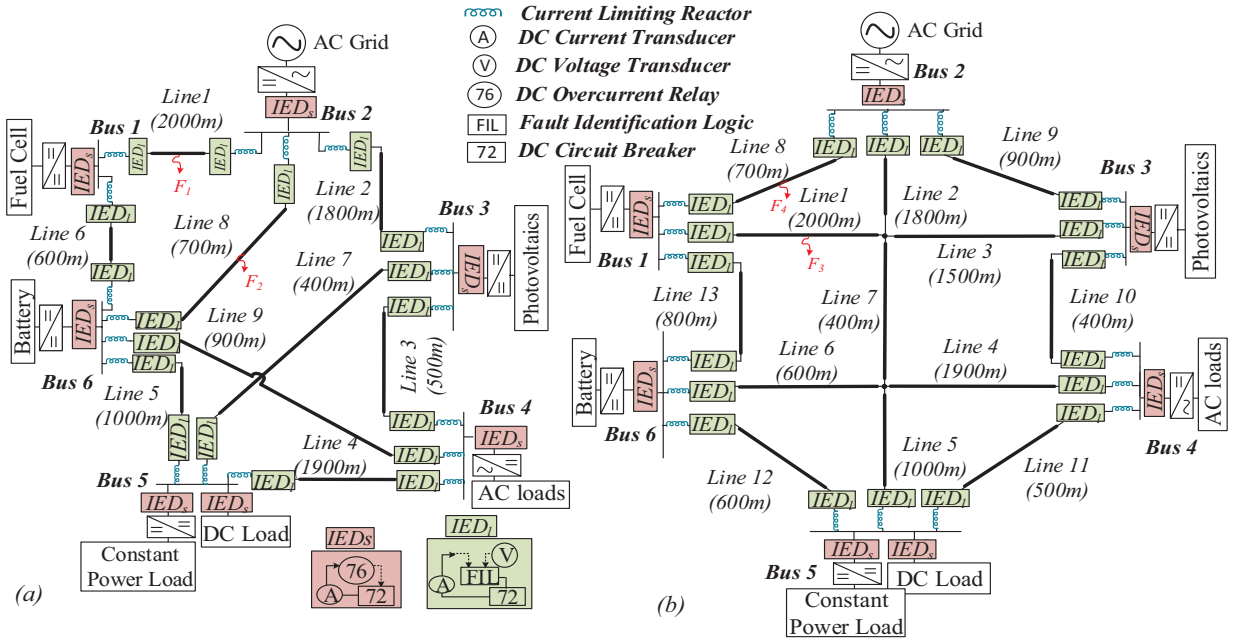


Fig. 1: LVDC Test System formed by (a) point-to-point, (b) multi-terminal configuration

result, the fault location method is independently analyzed for point-to-point and multi-terminal systems. For the point-to-point system, the fault contribution from other buses is neglected since the converter´s controllers' slow bandwidth and the path´s high inductance would limit the current from other buses [16], [17]. This permits simplifying the faulty point-to-point network as shown in Fig. 2. Similarly, for the multi-terminal system, the contribution from other buses is neglected, but the contribution from other nodes is considered (see Fig. 3). This makes the analysis of fault location slightly tedious for the multi-terminal system compared to the point-to-point system. Fig. 3 is used as the effective and simplified single-line network for a multi-terminal system.

A bipolar line configuration with a frequency-dependent transmission model (FDTL) of an underground cable (UGC) is considered. The LVDC system consists of different cables modeled as single-core cables with copper conductor, XLPE insulation (2.8 mm thick), and PVC sheathing (2.5 mm thick). The grounding capacitance of the UGC is 0.5μF/km while the equivalent DC capacitor of the converter is around 10^3-10^4 μF. Hence, the fault contribution from the grounding capacitance of cables and lines can be ignored for short to medium cables. As a result, the $R-L$ representation of UGC is used for the fault location analysis. The grounding scheme considered is TN-S, which provides mid-point grounding at each converter terminal. The fault contingencies considered in the test system are of different types, i.e., PTP, P-PTG, and N-PTG. The sources and loads in the setup are protected using an intelligent electronic device on the source side (IED_s) which is a combination of DC current transducer and DC over-current relays and DC circuit breakers as shown in Fig. 1. The cables in the system are protected using intelligent electronic devices of load side (IED_l) [4], [22]. The fault

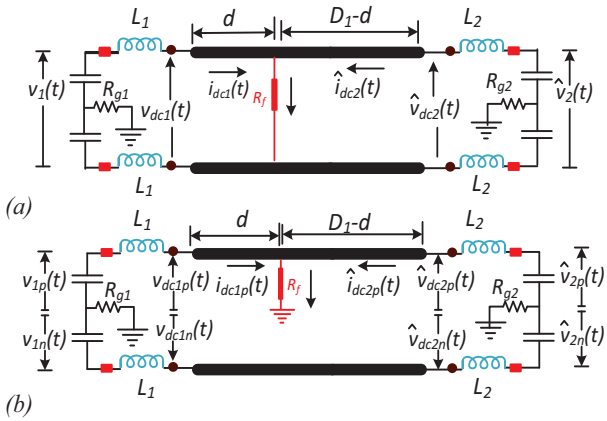


Fig. 2: Simplified network for point-to-point configuration under (a) PTP fault, (b) P-PTG fault

current used in the analysis is supplied by the discharging DC bus capacitance, not the inverters and converters upon fault inception. The converters should trip as soon as overcurrent hits. This is indicated in Fig. 1 using DC circuit breakers in IED_s and IED_l.

III. Fault Location Algorithm

A. Estimation of other terminal current, $\hat{i}_{dc2}(t)$

Fig. 1(a) shows the point-to-point system with a fault between bus 1 and bus 2 (shown as F_1 in Fig. 1(a)). Fig. 2(a) shows the simplified network under a PTP fault, whereas Fig. 2(b) shows the simplified network under a P-PTG fault. Since the method is single terminal, $\hat{v}_{dc2}(t)$ and $\hat{i}_{dc2}(t)$ are unknowns [23]. The analysis assumes $v_1(t) \approx \hat{v}_2(t)$ as voltage collapses slowly due to the energy dynamics of the DC bus as

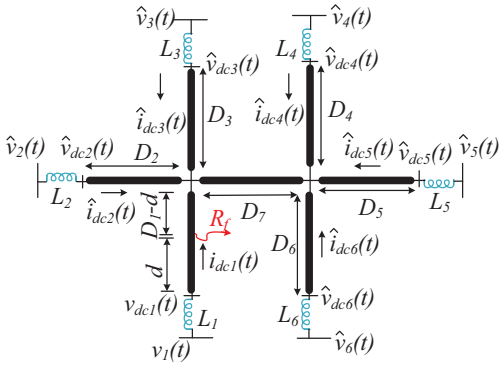


Fig. 3: Simplified multi-terminal test system

a result of its equivalent capacitance. Applying KVL in Fig. 1(a), following equations are obtained [24]:

$$v_{dc1}(t) = 2rdi_{dc1}(t) + 2ld\frac{di_{dc1}(t)}{dt} + R_f[i_{dc1}(t) + \hat{i}_{dc2}(t)], \quad (1)$$

$$\hat{v}_{dc2}(t) = 2r(D_1-d)\hat{i}_{dc2}(t) + 2l(D_1-d)\frac{d\hat{i}_{dc2}(t)}{dt} + R_f[i_{dc1}(t) + \hat{i}_{dc2}(t)], \quad (2)$$

where $v_{dc1}(t)$ and $\hat{v}_{dc2}(t)$ are the terminal voltages at each side of the cable, $i_{dc1}(t)$ and $\hat{i}_{dc2}(t)$ are the currents fed into the fault by the terminals on each side. r and l are the unit resistance and inductance of UGC. L_n is defined as the value of the CLR, and R_f is defined as the fault resistance. D_1 is the cable length whereas d is the fault distance from bus terminal. Considering the voltage drop across the CLR, the current derivative terms can be obtained, avoiding substitution errors due to differential calculations [2]. This improves the algorithm's performance in the presence of WGN. These terms are given as $\frac{di_{dc1}(t)}{dt} = \frac{v_1(t)-v_{dc1}(t)}{2L_1}$ and $\frac{d\hat{i}_{dc2}(t)}{dt} = \frac{\hat{v}_2(t)-\hat{v}_{dc2}(t)}{2L_2}$. Dividing (1) with $v_1(t)$ and (2) with $\hat{v}_2(t)$, (3)-(4) are obtained, where the ratio of transient voltages is defined as, $\gamma_1(t) = \frac{v_{dc1}(t)}{v_1(t)}$ and $\hat{\gamma}_2(t)$=$\frac{\hat{v}_{dc2}(t)}{\hat{v}_2(t)}$.

$$\gamma_1(t) = \frac{L_1}{L_1+ld}\left[\frac{2rdi_{dc1}(t)}{v_1(t)} + \frac{ld}{L_1} + R_f\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{v_1(t)}\right] \quad (3)$$

$$\hat{\gamma}_2(t) = \frac{L_2}{L_2+l(D_1-d)}\left[\frac{2r(D_1-d)\hat{i}_{dc2}(t)}{\hat{v}_2(t)} + \frac{l(D_1-d)}{L_2} + R_f\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{\hat{v}_2(t)}\right] \quad (4)$$

Considering (3) and discussing $\frac{2rdi_{dc1}(t)}{v_1(t)}$, generally $2rd < 1$ for LVDC systems and $\frac{i_{dc1}(t)}{v_1(t)}$ is at its minima right after the fault inception. During the fault transient, $i_{dc1}(t)$ rises and $v_1(t)$ drops which cumulatively increase the value of $\frac{i_{dc1}(t)}{v_1(t)}$.

Similarly, $\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{v_1(t)}$ in $R_f\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{v_1(t)}$ is at its minima right after the fault inception. During the fault transient, $i_{dc1}(t)$ and $\hat{i}_{dc2}(t)$ rise and $v_1(t)$ drops which cumulatively increase the value of $\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{v_1(t)}$. High resistance faults (HRFs) can increase the value of the time-varying term, but the effect is not dominant enough to compensate low $\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{v_1(t)}$ right after the fault. Further, as the maximum value of a fault resistance under the analysis is limited to 5Ω (considering an LVDC system), the effect of this term is fairly limited. Additionally, the total sum of time-varying terms is $R_f\frac{i_{dc1}(t)+\hat{i}_{dc2}(t)}{v_1(t)} + \frac{2rdi_{dc1}(t)}{v_1(t)} \ll \frac{ld}{L_1}$ right after a fault. This results from a low CLR (L_1) value used in LVDC systems. As a result, the time-varying terms in (3)-(4) are neglected immediately after the inception of a fault, as they increase gradually (see Fig. 3). Therefore, for $t = 0^+$ in (3)-(4), time-varying terms are neglected to give, $\gamma_1(0^+) = \frac{ld}{L_1+ld}$ and $\hat{\gamma}_2(0^+) = \frac{l(D_1-d)}{L_2+l(D_1-d)}$. A similar analysis can be carried out

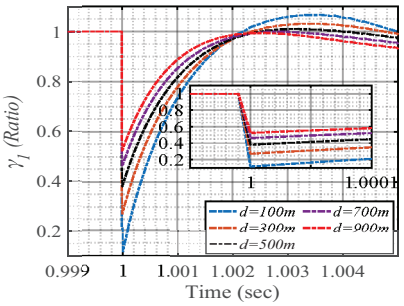


Fig. 4: Variation of ratio of transient voltages, γ_1 vs time for different fault distances.

for a PTG fault using the voltage and current measurements of the faulty pole. By subtracting (3) and (4) and using (5) and (6), the estimated value of other terminal currents for $t = 0^+$ is defined as (7a) for a PTP fault and (7b) for a P-PTG fault.

$$\hat{i}_{dc2}(t) = \frac{d}{D_1-d}i_{dc1}(t) : PTP \quad (5a)$$

$$\hat{i}_{dc2}(t) = \frac{rd+R_{g1}}{r(D_1-d)+R_{g2}}i_{dc1}(t) : P\text{-}PTG \quad (5b)$$

The analysis is valid for a point-to-point configuration, but multiple node currents are involved in the analysis for a multi-terminal configuration. As a result, the estimation gets complex. Fig. 1(b) shows a multi-terminal LVDC system, whereas Fig. 3 shows its simplified configuration. The objective of the analysis is to find the relation between $\hat{i}_{dck}(t)|_{k=2}^{6}$ and $i_{dc1}(t)$. The application of KVL considering buses 1-6, simplifying the ratio of transient voltages, gives the relationships between $\hat{i}_{dck}(t)|_{k=2}^{6}$ and $i_{dc1}(t)$. The identities $\hat{i}_{dc3}(t) = \frac{D_2}{D_3}\hat{i}_{dc2}(t)$, $\hat{i}_{dc4}(t) = \frac{D_2}{D_4+D_7}\hat{i}_{dc2}(t)$, $\hat{i}_{dc5}(t) = \frac{D_2}{D_5+D_7}\hat{i}_{dc2}(t)$ and $\hat{i}_{dc6}(t) = \frac{D_2}{D_6+D_7}\hat{i}_{dc2}(t)$ are used to define $\hat{i}_{dc2}(t)$ in terms of $i_{dc1}(t)$ for $t = 0^+$ as in (6).

$$\hat{i}_{dc2}(t) = \frac{d}{D_2 + (D_1-d)\left[1 + \frac{D_2}{D_3} + \sum_{k=4}^{6}\frac{D_2}{D_k+D_7}\right]}i_{dc1}(t) \quad (6)$$

For a P-PTG fault (F_1 in Fig. 1(a)), Fig. 4 shows the time variation of error (ε_i) (defined as the difference between estimated other terminal current ($\hat{i}_{dc2}$) and actual current (i_{dc2})). Fig. 5(a)-(c) show ε_i, i_{dc2}, i_{dc1} and $\hat{i}_{dc2}$ for a fault

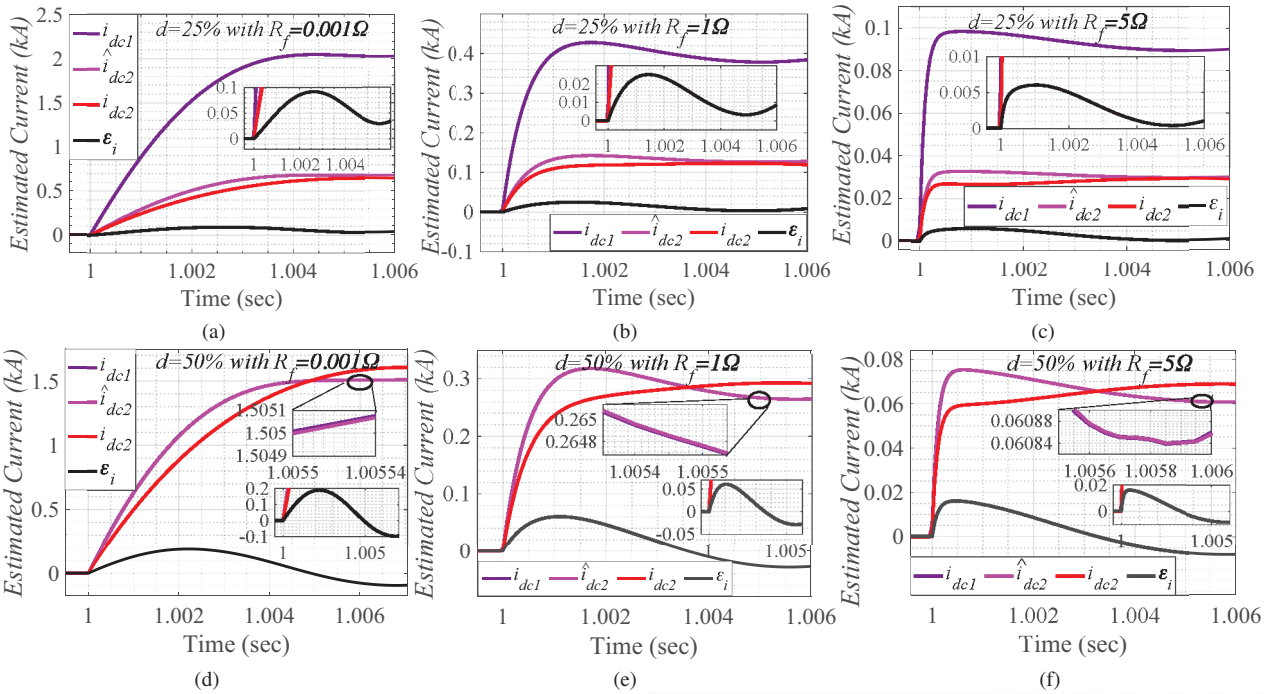


Fig. 5: Estimated terminal current (kA) vs time (sec) for a P-PTG fault at $t = 1$

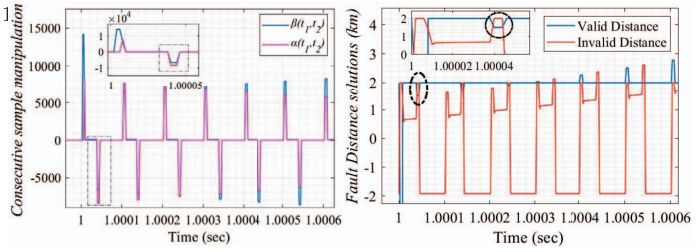


Fig. 6: (a) $\alpha(t_1, t_2)$ and $\beta(t_1, t_2)$ vs time (sec), (b) Fault distance solutions (km) vs Time (sec) for a line of total length 2 km.

distance of 25% with a fault resistance of 1mΩ (Fig. 5(a)), 1Ω (Fig. 5(b)) and 5Ω (Fig. 5(c)). Similarly, Fig. 5(d)-(f) show ε_i, i_{dc2}, i_{dc1} and $\hat{i}_{dc2}$ for a fault distance of 50% with fault resistance of 1 mΩ (Fig. 5(d)), 1Ω (Fig. 5(e)) and 5Ω (Fig. 5(f)). For a fault distance at 50%, $\hat{i}_{dc2} = i_{dc1}$ and the plots in Fig. 5(b),(e),(f) coincide. As the fault resistance increases, fault current reduces, and the merit of using estimated current in the calculation is reduced. Therefore, even if the defined estimated current closely resembles the actual measured current for fault resistance up to 5 Ω, the proposed method shows the merit of better fault location accuracy for fault resistance up to around 1 Ω.

B. Consecutive sample manipulation for fault location

Due to space constraints, the evaluation of fault location is explained for a point-to-point PTP fault in line with total length, $D_1 = 2$ km. Including the above conclusion in eq. (1), we can redefine $v_{dc1}(t)$ as:

$$v_{dc1}(t) = d\left(ri_{dc1}(t) + l\frac{di_{dc1}(t)}{dt}\right) + R_f\frac{D_1}{D_1 - d}i_{dc1}(t). \quad (7)$$

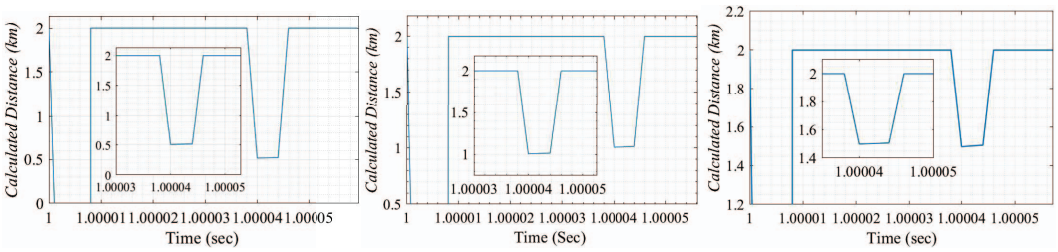
Rearranging for the calculated fault location, *d*, we can write the following quadratic polynomial:

$$d^2\left[r + \frac{l}{L_m}\frac{u_1(t_1)}{i_1(t_1)}\right] - d\left[\frac{v_{dc_1}(t_1)}{i_1(t_1)} + rD_1 + \frac{lD_1}{L_m}\frac{u_1(t_1)}{i_1(t_1)}\right] + D_1\frac{v_{dc_1}(t_1)}{i_1(t_1)} = D_1R_f. \quad (8)$$

Evaluating eq. (8) at $t = t_2$ can give us another equation with the constant D_1R_f on the RHS. Subtracting eq. (8) and the equation at $t = t_2$ would give us eq. (9).

$$d^2\frac{l}{L_m}\alpha(t_1, t_2) - d\left[\beta(t_1, t_2) + \frac{lD_1}{L_m}\alpha(t_1, t_2)\right] + D_1\beta(t_1, t_2) = 0 \quad (9)$$

where $\alpha(t_1, t_2) = [u_1(t_1)i_1(t_2) - u_1(t_2)i_1(t_1)]$ and $\beta(t_1, t_2) = [v_{dc1}(t_1)i_1(t_2) - v_{dc1}(t_2)i_1(t_1)]$. Continuous subsequent current and voltage measurements [23] are used to solve the quadratic expression. Fig. 6(a) shows the plots for $\alpha(t_1, t_2)$ and $\beta(t_1, t_2)$ with a window of 3 samples i.e., $t_2 = t_1 + 3\Delta T_s$. A window with fewer samples gives a triangular distance behavior (instead of a trapezoidal behavior) solution, while a window of abruptly high samples, such as 20 samples, gives an erroneous fault distance solution. A window of 3-10 samples is recommended to implement consecutive sample manipulation where ΔT_s=60μs for the given case. The fault information is packed within the black dotted rectangle in Fig. 6(a) and the black dotted ellipse in Fig. 6(b). The quadratic polynomial gives two solutions for the fault distance. One of the solutions is negative for the most part and is defined as the invalid distance (shown with red line) in Fig. 6(b). The valid distance (shown with a blue line) in Fig. 6(b) gives valuable information on accurate fault distance for nearly 4μs. Fig. 7 shows the presence of the DC fault at different locations i.e., $d = 0.5$ km, $d = 1$ km and $d = 1.5$ km. The algorithm gives accurate fault location for faults at different locations, as evident from Fig. 7, where the second transient of the valid solution gives the accurate fault distance. In each case, the



(a) (b) (c)

Fig. 7: Calculated fault distance (km) vs time (sec) for a fault at a distance of (a) $d = 0.5$ km, (b) $d = 1$ km, (c) $d = 1.5$ km.

fault distance lingers around its true value for nearly 4μs. This time can be increased with an increase in the window size of consecutive sample manipulation. However, increasing it to a very high value may jeopardize the method's accuracy. The future scope of the work includes generalizing the algorithm for a low-voltage system irrespective of its configuration. Further, the proposed method can be validated in the real-time digital simulator (RTDS).

IV. Conclusion

The proposed method estimates the adjacent terminal current using local current measurement and mimics double terminal fault location analysis methods. This eliminates the dependence of accuracy on the resistance of the fault. The simple algorithm accurately determines the distance using a consecutive sample manipulation. The proposed methodology presents highly accurate performance for low resistance faults, but as the fault resistance increases, the fault current contribution reduces, and the performance of the approach decreases. Nevertheless, the accuracy for high fault resistances is still comparable to other single terminal methods discussed in the literature.

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