Integration of the Battery Energy Storage System in a 450 kW EV Charger

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TUDelft

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by

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Acknowledgements

Abstract

Despite the Covid-19 pandemic and supply chain challenges, including shortages of semiconductor chips, the electric vehicle (EV) market is expanding rapidly. Automobile manufacturers have been progressively developing business plans, considering electrification as an opportunity to acquire market share and preserve competitive advantages. The main barriers to EV adoption are high vehicle costs, range issues, and charging infrastructure. Installing a comprehensive EV fast charging network will help alleviate range and charging problems on long intercity drives. However, fast and ultra-fast charging directly from the grid will place a huge and unpredictable load on the power system. Therefore, energy storage systems (ESS) appear as a promising solution to prevent grid overload during charging and help reduce infrastructure costs.

In this dissertation, the integration of the battery energy storage system (BESS) in a 450 kW EV charger is designed and validated via modeling, simulation and experiment. For the front end of the DC fast charger, the 3-phase 3-level T-type converter is selected as the PFC converter linked to the grid for its superior performance, especially for applications with low voltage and medium switching frequencies. An appropriate modulation method based on space vector modulation (SVPWM) and closed loop control will be illuminated and simulated via PLECS. Based on the comparison of several types of state-of-the-art cylindrical 18650 batteries, the battery energy storage system is designed from thermal issues and integration impact on the DC bus. In order to explore the heat dissipation and the temperature distribution across the pack, the thermal model based on the sub-model technique is developed via COMSOL, and a preliminary layout and cooling strategy are determined.

Finally, the proposed structure of the EV charger integrated with the battery energy storage system is validated based on a 6 kW rated lab-scaled hardware test bench. In conjunction with the actual scenario, both the prospective steady states and transitions have been implemented. Hence, the feasibility of the concept of directly connecting the BESS to the DC bus is also verified by observing the response of the front-end AC/DC converter with the modulation and control strategies utilized.

Key Words: Fast charging, 3-phase 3-level T-type converter, BESS, System integration

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Introduction

1.1. Background

The electric vehicle market is one of the most dynamic clean energy sectors worldwide. In recent years, countries all over the world have proposed related policies to realize environmental sustainability by reducing carbon emissions. Among the most crucial steps is the rapid expansion of electric vehicles as a viable alternative to those powered by conventional fuels. Price subsidies or tax reductions by the governments significantly stimulated the whole EV industry to a brand new level.

According to Global Electric Vehicle Outlook 2022 [1], in 2021, over 16.5 million electric cars were on the road, which is three times as three years ago. Despite the Covid-19 epidemic and supply chain issues, like semiconductor chip shortages, sales of electric automobiles hit another record high in 2021. Sales of EVs including battery electric vehicles (BEVs) and plug-in hybrid electric vehicles (PHEVs) was 6.6 million, which is almost twice of the last year. For specific regions shown in Fig 1.1, in 2021, 3.3 million electric cars were sold in China, surpassing the total worldwide sales in 2020. Meanwhile, sales of EVs in Europe reached 2.3 million in 2021, which increased by 65% compared with the last year. Despite two years of consecutive decline, the EV market in the United States also ushered in a rebound in 2021, and about 630000 electric cars were sold, which is more than in 2019 and 2020 combined. From a global perspective, the global EV sales share increased from 4% to 8.6%.
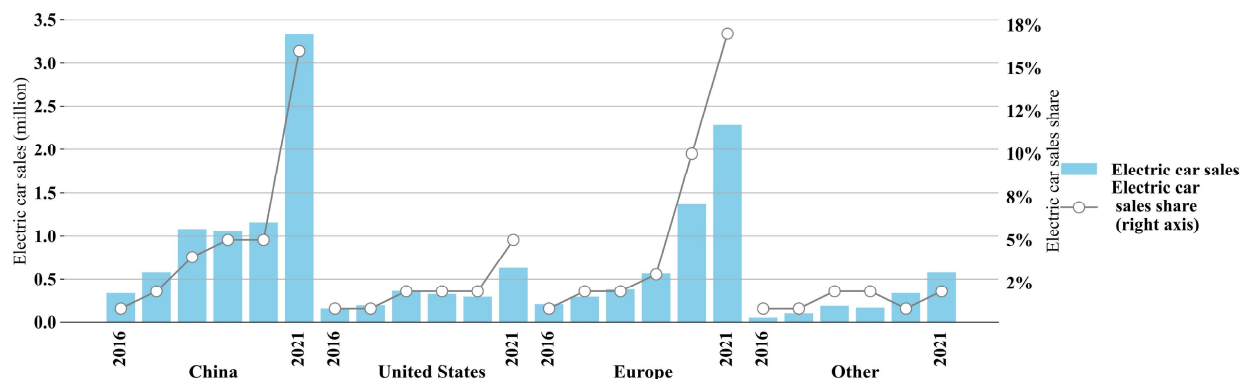
Figure 1.1: Electric car registrations and sales share in selected countries/regions, 2016-2021[1]

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However, because of the range anxiety, charging infrastructure construction has become a key focus. Therefore, it can be seen that the publicly available chargers are also expanding significantly, especially the DC fast chargers. Electricity from the grid is always AC, and EV batteries only accept DC electricity. The distinction between AC and DC charging stations is whether the power converter is positioned on or off the car. DC charging typically has a higher power level compared with AC charging, which can facilitate longer journeys and tackle range anxiety more efficiently. A sizable preliminary expenditure for grid reinforcement may be needed for DC fast chargers, especially those offering charging power over 100 kW. In the case of a weak grid connection, for instance, the utility upgrade needed for a 350 kW charger would be far higher than that needed for a 50 kW charger [2].

To achieve higher charging power and avoid large impacts on the grid especially during peak periods, the DC fast charger integrated with a battery energy storage system (BESS) is a quite promising option. Typically, AC/DC rectification, power factor correction (PFC), voltage regulation and isolation between the battery and grid ought to be included in such a system [3]. There are two mainstream structures of DC fast chargers with energy storage, which are depicted in Fig 1.2. The key distinction here is the use of a DC/DC converter between the DC bus and the BESS. On the one hand, the DC/DC converter in the first structure is responsible for regulating the DC bus voltage. Meanwhile, due to the existence of the additional converter, a larger loss will also be generated. On the other hand, for the second arrangement, the DC bus varies with the battery state of charge (SOC), and the battery terminal voltage fluctuates with charging and discharging events due to the direct connection. Therefore, the design of the BESS should comply with the operating conditions of the AC/DC PFC converter. In addition, stationary BESS can usually be grounded, so isolation can be ignored to avoid a larger budget for the volume and cost of the overall system.
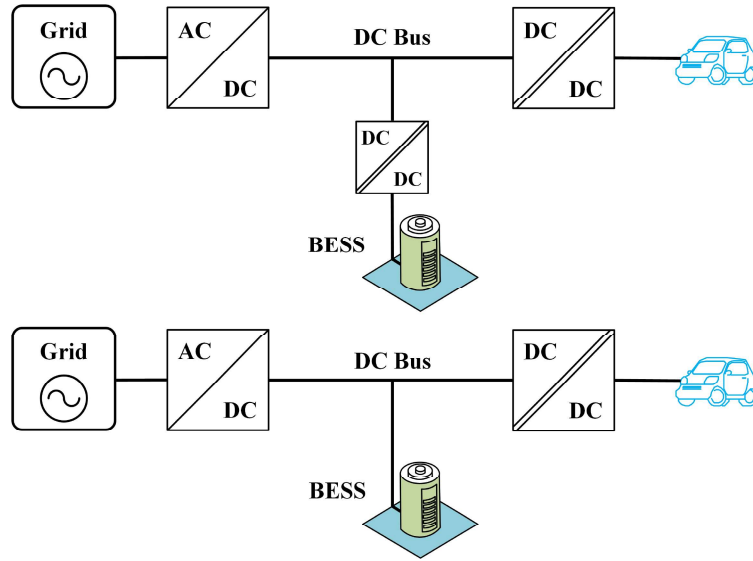
Figure 1.2: Architectures of DC fast charging stations with energy storage

1.2. Problem Definition

As an important part of DC fast chargers, for the high power grid connection requiring potential bidirectional power flow between the grid and the BESS, 3-phase front-end converters are utilized so that the BESS also has the opportunity to provide grid services such as voltage support or peak power [4]. In addition to providing AC/DC rectification and an appropriate DC bus voltage level for the EV connections, they also provide power factor correction to enhance power quality at the AC mains and decrease losses. One of the most commonly used topologies is the 3-phase 3-level T-type converter, which is mainly applied for low voltage and medium switching frequency applications. Compared with

other popular AC/DC PFC converters such as 2-level converters or neutral point clamped (NPC) 3-level converters, the T-type converters are superior in terms of switching loss, switching noise, and conduction loss. However, the neutral point balancing problem of the 3-level converter is inherent and needs to be taken into consideration.

In this system, the selection and design of energy storage technologies are equally important. As depicted in Fig 1.3, A typical BESS structure consists of a number of battery cells, a battery management system (BMS), and a thermal management system (TMS). Nowadays, batteries, flywheels, and hydrogen are three promising and prominent energy storage technologies, especially for the DC fast charging field. And electrochemical cells, such as Li-ion batteries, are the primary rivals in this field and also the research object of this dissertation. A well-designed BESS with Li-ion batteries can normally achieve 94% to 98% efficiency [5]. Meanwhile, the series or parallel connection will also impact the overall efficiency and the fluctuation of DC bus voltage. Furthermore, the thermal management of the battery pack will have a significant effect on the battery's lifespan, consequently influencing its one-cycle investment cost. Hence, it is essential to investigate and optimize the heat dissipation of both one single pack and the entire rack.

Considering the auxiliary role of BESS for ultra-fast DC charging, which can offer up to 450 kW output power without incurring a significant influence on the grid, the holistic system integration is also essential. This includes the effect of the drop in SOC, which also leads to a drop in the terminal voltage of the BESS, on the functioning of the AC/DC PFC converter and the effect of the charging and discharging mode transition on the DC bus, etc.
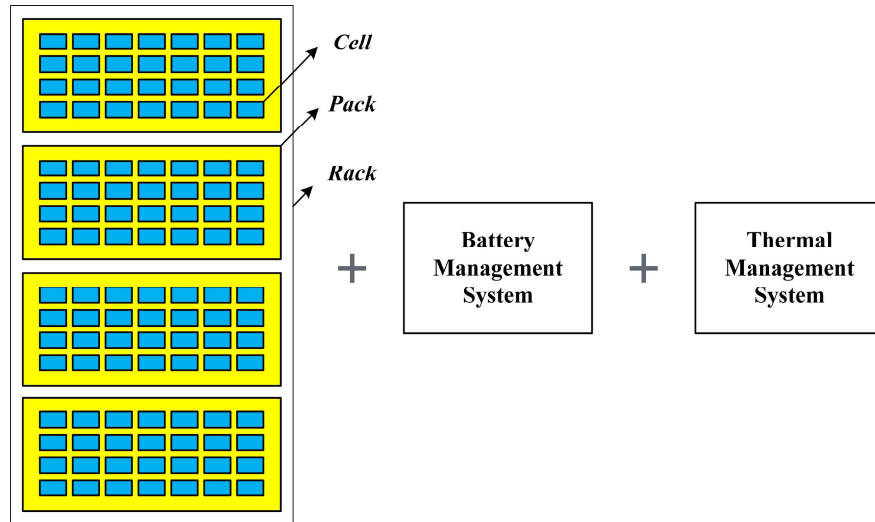
Figure 1.3: Typical structure of a BESS

1.3. Research Objective

Although some companies have industrial products, they are mostly inaccessible and the related academic research is limited. Therefore, this thesis project aims to design the front-end AC/DC PFC converter of a 450 kW DC fast charger with the integrated BESS system. The specific objectives are as follows:

1. Investigate and implement appropriate modulation and control strategies of the AC/DC PFC converter.

2. Complete the design of BESS based on Li-ion battery including model selection, sizing, and connection method design.

3. Investigate the preliminary design of the thermal management of the BESS by comparing different layouts of battery packs under unidirectional airflow.

4. Validate the integration concept of a BESS in a DC fast charger in both simulations and experiments combined with practical scenarios.

1.4. Research Plan

According to the research objectives, the detailed research plan is as follows:

1. Perform a literature review on the AC/DC PFC converters and implement suitable modulation and control methods via PLECS.

2. Collect relevant battery data and compare various cutting-edge cylindrical Li-ion batteries to complete the design of overall battery sizing and connection.

3. Perform a literature review on the thermal issues of BESS and complete a preliminary design of layout and cooling method via COMSOL thermal simulation.

4. Simulate the charging and discharging mode from a system integration aspect via PLECS and build a lab-scaled experimental test bench to conduct the experimental validation.

1.5. Thesis Outline

Chapter 1: Introduction

This chapter explains the background, motivation, and demands of this thesis project, which is the integration of BESS in a DC fast charger satisfying the demands of development. Hence, the front-end stage design from the system level is necessary also because of the inaccessibility of commercial industrial products.

Chapter 2: Literature Review

In this chapter, a literature review on the commonly used AC/DC PFC converters including the 2-level converter, the neutral point clamped (NPC) converter and the T-type converter is performed. After selecting the T-type converter as the active front-end converter, a literature review on the neutral point balancing issue for the 3-level converter is also investigated. In addition, reference to the literature on Li-ion batteries, promising energy storage options and also related thermal dissipation issues are also included in this part for the follow-up design of the BESS.

Chapter 3: AC/DC PFC Converter of the EV Charger

Based on the literature review in Chapter 2, Chapter 3 provides an appropriate modulation method based on the space vector modulation (SVPWM) and a control strategy based on closed loop control. Furthermore, active damping by capacitor-current feedback and the neutral point balance control approach are also implemented to form an overall control method.

Chapter 4: Design of Battery Energy Storage System

In this chapter, based on the selection of the battery equivalent model and collection of battery data, several cutting-edge 18650 cylindrical Li-ion batteries are compared from a number of crucial aspects, namely capacity, nominal voltage, Max C-rate, specific energy, price, losses, etc. Hereafter, the optimal model is selected and the overall battery packs, especially with respect to heat dissipation according to the thermal simulation via COMSOL, are determined.

Chapter 5: Simulation and Experiment Validation

Considering the improvement in simulation speed, in Chapter 5, the average model simulations are performed to replace the switched model and the simulation results are also compared to verify the feasibility of the method. Besides, from a system-level point of view, the simulation of potential steady states and transitions is also performed via PLECS. Finally, a 6 kW lab-scaled experimental test bench is built to conduct the experimental validation for the proposed integration structure combined with actual scenarios.

Chapter 6: Conclusion and Future Work

In the final chapter, the conclusion and summary of the whole dissertation are given. At last, combined with the current conclusion and judgment, potential future directions for research are discussed.

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Literature Review

2.1. Three-Phase PFC Converters

2.1.1. 2-Level Converters

Prior to the advent of multi-level voltage-sourced converters (VSC), the 2-level converters are widely used in a number of fields, such as transportation, industrial automation, etc. The output voltage of 2-level converters presents two voltage levels, specifically $+V_{dc}/2$ and $-V_{dc}/2$. The circuit of the 2-level VSC is depicted in Fig 2.1. There are 2 switches on each leg and the upper and lower switch are complementary to each other. The switching action is typically performed using Pulse Width Modulation (PWM) techniques such as carrier-based PWM approaches by comparing a triangular carrier signal with a sinusoidal reference signal to generate the appropriate pulse that regulates the operation of power electronic switches, which is shown in Fig 2.2a. Pulse generation and distribution to switches occur when the reference signal is greater than the carrier signal. Besides, a digital modulating technique named Space Vector Modulation (SVM) is also a widely used method for the 2-level converters. The switch states are integrated by the vectors placed in a hexagonal structure for representing the magnitudes and phases, which is depicted in Fig 2.2b. The switch states marked in the hexagon correspond with whether the upper or lower switch is activated in one phase, which will be transformed into the six gate drive signals delivered to switches in three phases subsequently.
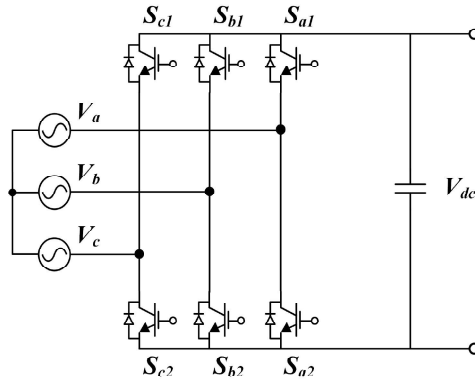
Figure 2.1: The schematic of 2-level converters

(a) Carrier-based modulation for 2-level converters   **(b)** Space vector modulation for 2-level converters
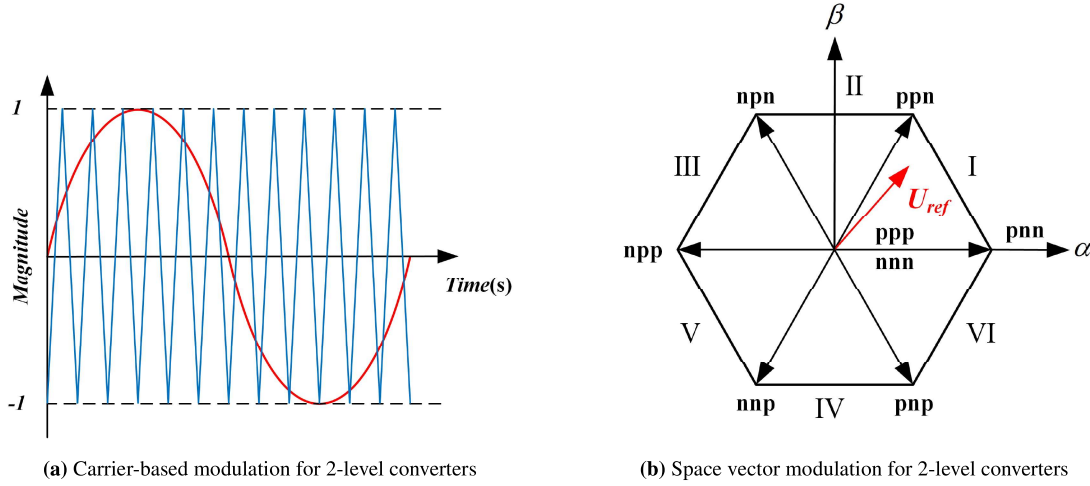
Figure 2.2: Modulation methods for 2-level converters

2.1.2. 3-Level Converters

Compared with 2-level converters, 3-level converters have multiple advantages. First of all, when disconnecting the half-bridge switches (S_{x1} and S_{x4}), the bidirectional switches (S_{x2} and S_{x3}) will only block half of the DC link voltage [6]. Therefore, the requirement for the voltage rating of the devices is possible to be lower. Switching losses and switching noise are also decreased since the devices operate at half the dc-link voltage in comparison to the 2-level converter. In addition, multi-level converters offer lower electromagnetic interference, lower harmonic contents, and lower common mode voltage (CMV) [7]. The most common multi-level converters are the 3-phase 3-level neutral point clamped converter (NPC) and the 3-phase 3-level T-type converter, of which schematics are shown in Fig 2.3. The former is widely applied in distributed renewable energy systems or other industrial applications requiring medium voltage and high power[8, 9, 10], while the latter is intended for low voltage applications [11]. Since the current is conducted through a single switch, the T-type converter incurs less conduction loss than the NPC converter [12]. In medium switching frequencies, especially 4 to 30 kHz, the overall loss of a T-type converter is thus the lowest.
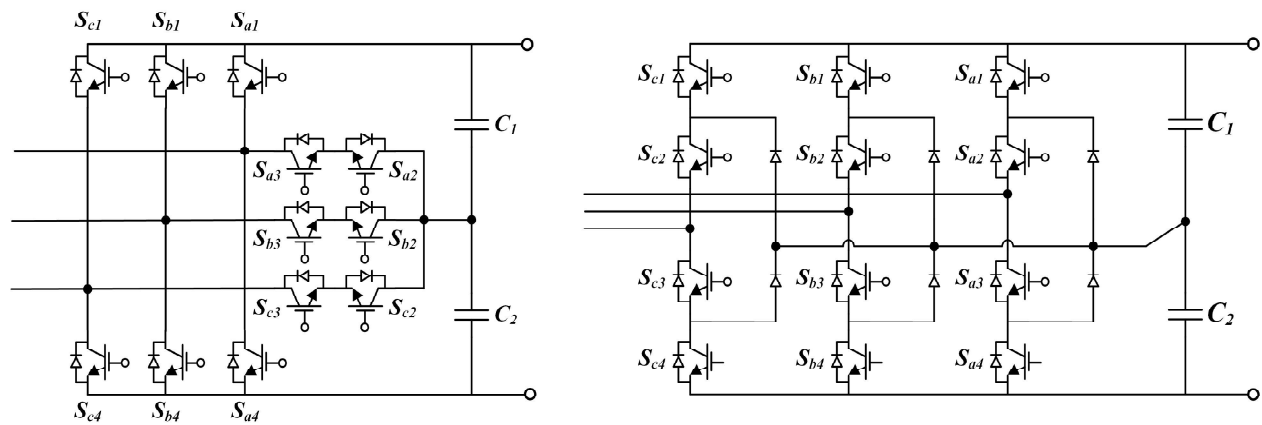
Figure 2.3: Circuit diagram of NPC and T-type converter

There are various PWM strategies are available for multi-level converter applications, and the two most commonly used categories are still carrier-based PWM (CBPWM) and space vector PWM (SVPWM). Initially, CBPWM could be divided into three mainstream methods according to different carriers utilized, namely Phase Disposition (PD) PWM,

Phase Opposition Disposition (POD) PWM and Alternate Phase Opposite Disposition (APOD) PWM. In subsequent research, many other carriers were also developed, such as Phase Shifting Carrier (PSC), Interleaved Carrier (IC) and Variable Frequency Carrier (VFC). The Arrangements of reference and carrier signals are shown in Fig 2.4. It should be noted that, in CBPWM, $N - 1$ carrier signals are required, where N is denoted as the line-to-line number of levels. Specifically, for the 3-level converters, the carrier signals needed is 2.

(a) Phase Disposition (PD) PWM

(b) Phase Opposition Disposition (POD) PWM

(c) Alternate Phase Opposite Disposition (APOD) PWM

(d) Interleaved Carrier (IC) PWM

(e) Phase Shifting Carrier (PSC) PWM

(f) Variable Frequency Carrier (VFC) PWM
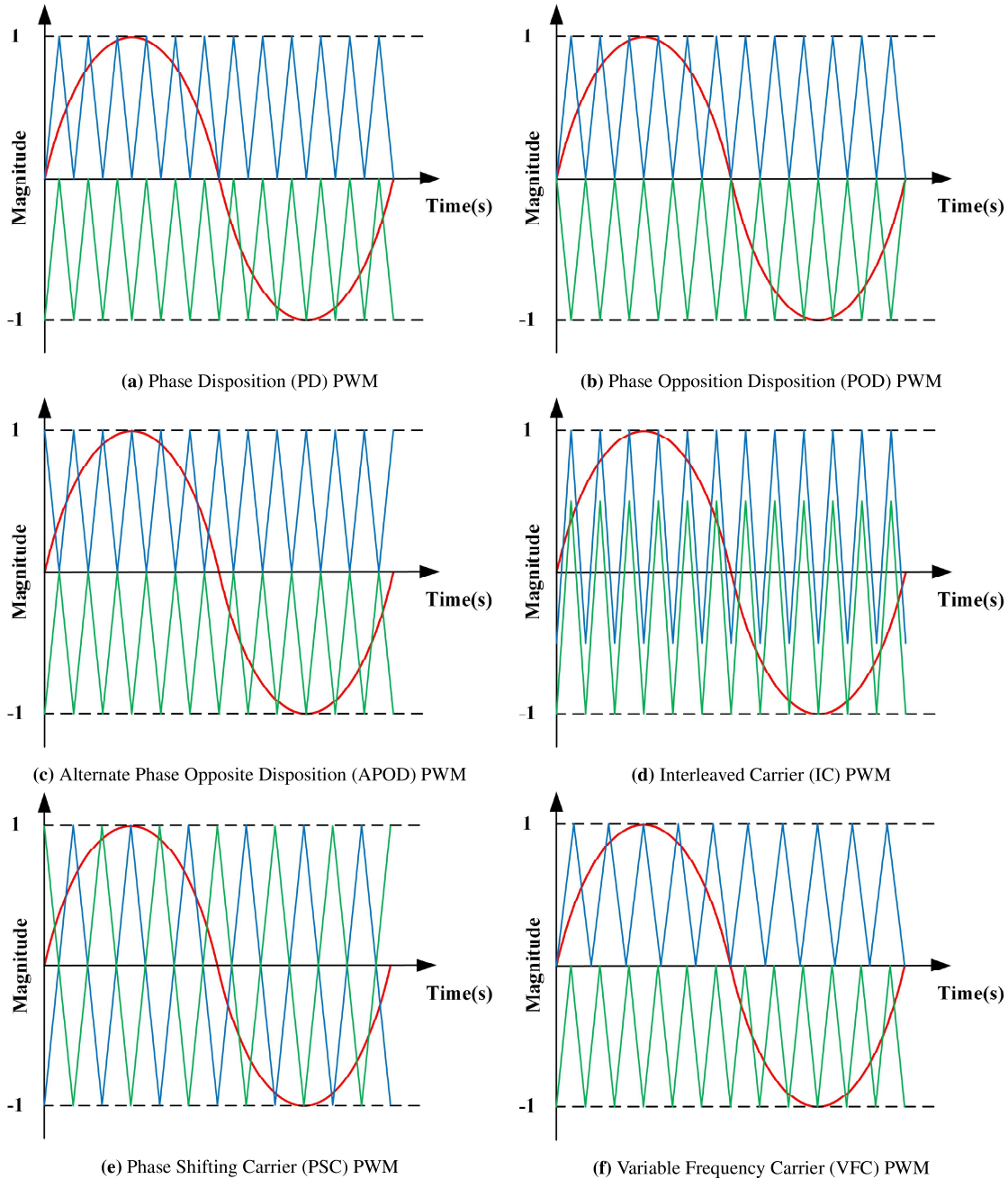
Figure 2.4: Arrangements of reference and carrier signals for the 3-level converter

In the PD PWM technique (Fig 2.4a), the upper and lower carrier signals are placed without phase shifting and they are compared with a sinusoidal reference waveform to generate pulses for switches [13]. While in the POD PWM

technique (Fig 2.4b), the vertical position of carriers is the same as the PD one, but they have a 180-degree phase shift [14]. For the APOD PWM, the carriers alternate in their phase displacement from one another by 180 degrees, but it is similar to POD PWM when there are only two carriers used. But for converters with output levels more than three, the implementation is much different [15]. In the IC PWM technique (Fig 2.4d), both carriers have the same amplitude, frequency and phase, but they will have offset with each other [16]. In the PSC PWM technique (Fig 2.4e), a phase shift is added between each carrier signal rather than a level shift, leading to a stepped output waveform with low harmonic content. The carrier signals will have a certain phase shift depending on the number of carriers and the phase shift between the carriers is calculated as 180/N [17]. The last mentioned CBPWM is the VFC PWM technique where the frequencies of the two carriers in (Fig 2.4f) are different, leading to the harmonic spectrum distributed over a wide range of frequency [18, 19].

Meanwhile, SVPWM can also be applied to 3-level converters. Conventionally, the SVPWM technique is implemented in the $\alpha - \beta$ frame. In Fig 2.5, the composition of the space vector in the $\alpha - \beta$ frame is represented. As is commonly known, the α axis is along 0° and β axis is along 90°. Besides, SVPWM can also be carried out in $g - h$ and $K - L$ frames, which are discussed in [20]. The g axis and L axis are overlapped with the α axis, but the h axis and K axis are shifted from the α axis by 60° and 120° respectively. Actually, they are essentially the same but utilize different coordinate systems to synthesize necessary space vectors. And these algorithms are generic and applicable to converters of all levels.
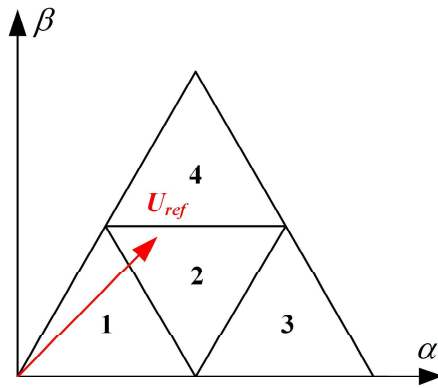
Figure 2.5: The composition of space vector in the $\alpha - \beta$ frame

2.1.3. Neutral Point Balancing of 3-Level Converters

When it comes to 3-level converters, the neutral point balancing is an essential issue since this these topologies are composed of two DC link capacitors connected in series. Low-order harmonics will occur in the output voltage if the neutral-point is not balanced, which might shorten the life of the switching devices and increase the THD of the output current [6]. In order to minimize the impact of unbalanced neutral point voltages, a number of different methods were proposed. Some of these approaches, which are based on CBPWM, improve the performance of the two capacitors' midpoint balance by introducing a zero-sequence voltage into the modulation reference signal. [21] proposed a zero-sequence voltage injection to force the specific voltage modulation reference signal clamped to 0, -1 or 1 according to the voltage difference between two capacitors and then achieve the effect of midpoint balance. Another kind of methods are based on the SVPWM modulation. The balance of midpoint voltage is achieved by adjusting the distribution sequence and time of different switching states. [6] proposed a method to adjust the distribution of P-type and N-type small vectors within one switching cycle by properly adding or subtracting a minimum gate-on time, thereby affecting the flow of the midpoint current to stabilize the two capacitor voltages. This solution does not require additional hardware, but complicated calculations to realize balance. [22] proposed a technique to modify the

angle of reference current vectors using the error voltage of the two capacitors. As a result, the number of sampling periods are decreased or increased in respective sectors and the capacitor voltages tend to be balanced. In [23] and [24], according to the judgment of the voltage of the two capacitors, two different finely designed switching sequences are allocated to each small sector. In essence, this is still a change on the direction of the midpoint current, so as to charge or discharge the capacitors. Based on the basic space vectors, there is also a derivative method named Virtual Space Vector PWM (VSVPWM) proposed. In [25], the original positive and negative redundant voltage states are used to synthesize the corresponding virtual space vectors. And then, the zero vectors, large vectors, and virtual vectors are utilized to synthesize the required reference vectors to suppress the neutral point potential fluctuation at any time because of the opposite effect of redundant vectors. Besides, there are also some methods proposed based on control theory. For instance, [26] and [27] put forward methods based on parameters self-tuning fuzzy logic control. This algorithm has enough robustness and adaptability for time-varying nonlinear systems. However, they are both difficult to implement because of the high computational effort.

2.2. Energy Storage System (ESS)

2.2.1. Energy Storage Options

Due to the continuous increase of the charging power of the DC fast charger, fast charging or even ultra-fast charging directly from the grid would place enormous and unpredictable strains on the power grid infrastructure [28, 29]. Much of the demand for DC fast chargers stems from long-distance driving, but the electrical infrastructure along some highways is usually located far from the main distribution grid and, therefore has high impedance with low short-circuit power. In some areas, (ultra) fast charging from the grid is even not feasible. Therefore, the energy storage system can operate as a buffer between the grid and the vehicles to avoid the expensive cost of large-scale upgrades of electric services.

Nowadays, mainstream energy storage technologies for DC fast chargers include batteries, flywheels, and hydrogen. Due to their high efficiency, high energy density, and low cost, electrochemical cells are currently the most predominant of these alternatives. The two most common types of battery chemistries are lithium-ion and lead-acid batteries. Despite using different materials, both types of batteries are able to store and release electrical charge and electrons through an electrochemical process. The key metric for assessing batteries is their capacity, and research has proven that lithium-ion battery technology has a substantially better energy density than lead-acid batteries, meaning it requires much less physical space to store the same amount of energy. In addition, the permissible depth of discharge (DoD) has an effect on the battery's life and the size of the battery pack required to meet energy demands. Most modern lithium-ion batteries have a DoD ranging from 80% to 95%, compared to a recommended DoD of only about 50% for lead-acid batteries. Most importantly, the efficiency of lithium-ion batteries also shows great advantages, usually reaching 94%-98% [30]. In conclusion, lithium-ion batteries are preferable to lead-acid batteries in the majority of cases, while lead-acid batteries are usually used for infrequently used backup batteries to avoid their technical shortcomings.

As an alternative to batteries for energy storage, flywheels generally have higher power density and lower energy density than batteries [31]. The flywheel energy storage system (FESS) is fundamentally a mechanical device that uses electricity to rotate at high speed and set the flywheel at the operating speed to create kinetic energy storage. When energy is needed, the flywheel sends the rotating energy to the electric machine, which works as a generator, completing the cycle of electrical energy. The main advantage of FESS is high cycle life and high power density, combined with long service life, typically 175,000 to 200,000 cycles over a 20-year lifespan [32]. However, FESS is not broadly applied on DC fast chargers in the real world due to the factors such as the high cost of low-loss magnetic bearings, smaller energy density, lower power output capability, especially compared with battery energy storage systems, etc [33]. Besides, hydrogen storage has the advantage of high energy density, which is a critical enabler for

the development of hydrogen and fuel cell technologies for both stationary power and portable power. Energy storage for DC fast chargers is still uncommon, even though hydrogen storage projects are being developed worldwide to provide for the storage of surplus renewable energy.

Table 2.1 summarizes the advantages and disadvantages of mainstream energy storage systems for DC fast charging stations in light of the preceding statement.

Table 2.1: Comparison of mainstream ESS for DCFC stations

	Advantages	Disadvantages
Batteries	1. High efficiency; - up to 94%-98% [30]. 2. High energy density; - up to 100-150kWh/m^3 [34]. 3. Rapidly reduced cost [35].	1. Short cycle life; - up to 10-15 years [30]. 2. Potential replacement cost.
Flywheels	1. Higher power density than batteries; - 264.71kW/m^3 for Beacon Power Model 450 XP [36]. 2. High cycle lifetimes; - up to 175,000-200,000 cycles over 20 years [32]. 3. Less maintenance over lifetime [30].	1. Lower energy density than batteries; - 26.47kWh/m^3 for Beacon Power Model 450 XP [36]. 2. High self-discharge rate; - up to 20% per hour [37]. 3. Low power output capacity.
Hydrogen	1. High energy density. - up to 1300 kWh/m^3 for commpressed hydrogen at 700 bar [38].	1. Lower round-trip efficiency than batteries; - only around 30% [39].

2.2.2. Thermal Effect in Lithium-ion Batteries

As mainstream energy storage and the most prevalent alternative for the DC fast chargers, lithium-ion batteries demonstrate excellent performance in a variety of respects including high energy density and high power density. However, temperature impacts continue to hinder its performance. Normal operating temperatures for lithium-ion batteries range between -20 and $60°C$ [40]. Too high or too low temperatures will lead to performance degradation or even irreversible damage. In general, there are two broad classes of temperature-related effects on Li-ion batteries, namely the low-temperature effect and the high-temperature effect [41]. On the one hand, the low-temperature effect occurs mainly in high latitudes and spacecraft in outer space. According to the study cited in [42], the diffusivity of lithium ions in graphite decreases at low temperatures, putting a restriction on the material's power and energy storage capacities. High-temperature circumstances, on the other hand, are more common than low-temperature ones. The high-temperature effect is frequently caused by the capacity and power loss of Li-ion batteries during high current states, such as rapid charging or discharging. The primary cause of capacity degradation is the accumulation of the solid electrolyte interphase layer (SEI) of lithium, while other mechanisms include side reactions that result in lithium loss inside the electrolyte [43]. Repeated layer deposition on the anode surface causes a faster rate of lithium loss and a significant rise in anode resistance with cycling, both of which contribute to the battery's greater capacity fading at higher temperatures [44]. And the higher internal resistance in a battery is correlated with a faster power loss rate [45]. In extreme situations, thermal runaway can potentially result in spontaneous combustion or explosion. Therefore, the thermal management is crucial to the performance and safety of batteries.

3

AC/DC PFC Converter of the EV Charger

3.1. Introduction

The grid-tied PFC AC/DC converter provides the interface between the grid and the regulated DC bus in the DC fast chargers, as shown in Fig 3.1. Typically, several differences should be considered in the design of the AC/DC converter for a DC fast charging station with energy storage compared to the ones without energy storage. First, for small DC fast charging stations with only one charging port, a high power rating could be provided by BESS instead of the grid side, which can reduce the size and cost of this stage. Second, a bidirectional converter is worthwhile due to the potential economic return of the grid services by the BESS. Based on Chapter 2, the 3-phase 3-level T-type converter is selected as the AC/DC PFC converter of the DC fast charger for its superior performance, especially for applications with low voltage and medium switching frequencies. In this chapter, an appropriate modulation method based on the SVPWM and control strategy based on the closed loop control will be provided and illuminated.
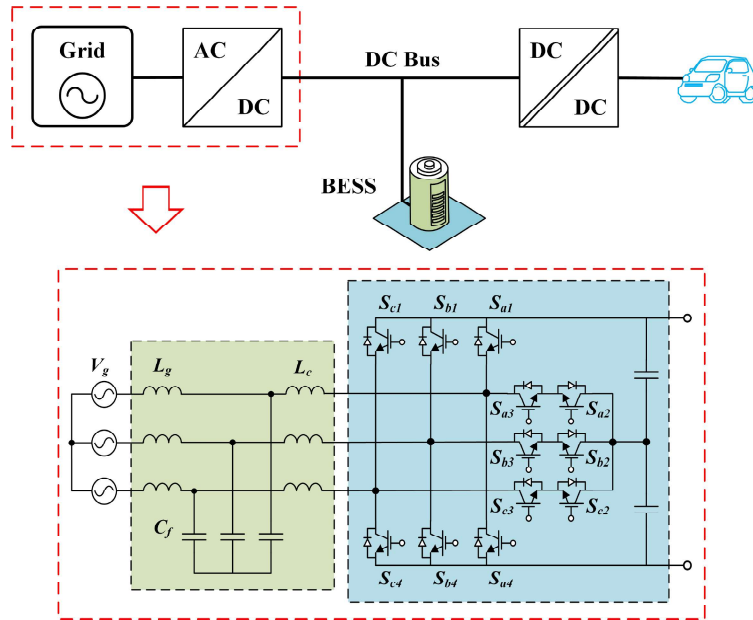
Figure 3.1: The overall scope of chapter 3

3.2. Working Principle and Mathematical Model of T-type Converter

The output of the T-type converter has three states namely the positive (P), neutral (O) and negative (N). One phase is selected to demonstrate the switch commutation of the 3-phase T-type converter. The neutral point between two capacitors is set as a reference point, and the current direction flowing out of the bridge arm is defined as the positive direction. The switch commutations under different current directions are depicted in Fig 3.2.

When the current direction is positive:

- If S_1 is turned on, meanwhile, S_2, S_3 and S_4 are turned off, the current flows through S_1. The output voltage of this phase is $U_{dc}/2$, which indicates the P state.
- If S_2 and S_3 are turned on, meanwhile, S_1, S_4 are turned off, the current flows through D_3 and S_2. The output voltage of this phase is 0, which indicates the O state.
- If S_4 is turned on, meanwhile, S_1, S_2 and S_3 are turned off, the current flows through D_4. The output voltage of this phase is $-U_{dc}/2$, which indicates the N state.

When the current direction is negative:

- If S_1 is turned on, meanwhile, S_2, S_3 and S_4 are turned off, the current flows through D_1. The output voltage of this phase is $U_{dc}/2$, which indicates the P state.
- If S_2 and S_3 are turned on, meanwhile, S_1, S_4 are turned off, the current flows through S_3 and D_2. The output voltage of this phase is 0, which indicates the O state.
- If S_4 is turned on, meanwhile, S_1, S_2 and S_3 are turned off, the current flows through S_4. The output voltage of this phase is $-U_{dc}/2$, which indicates the N state.
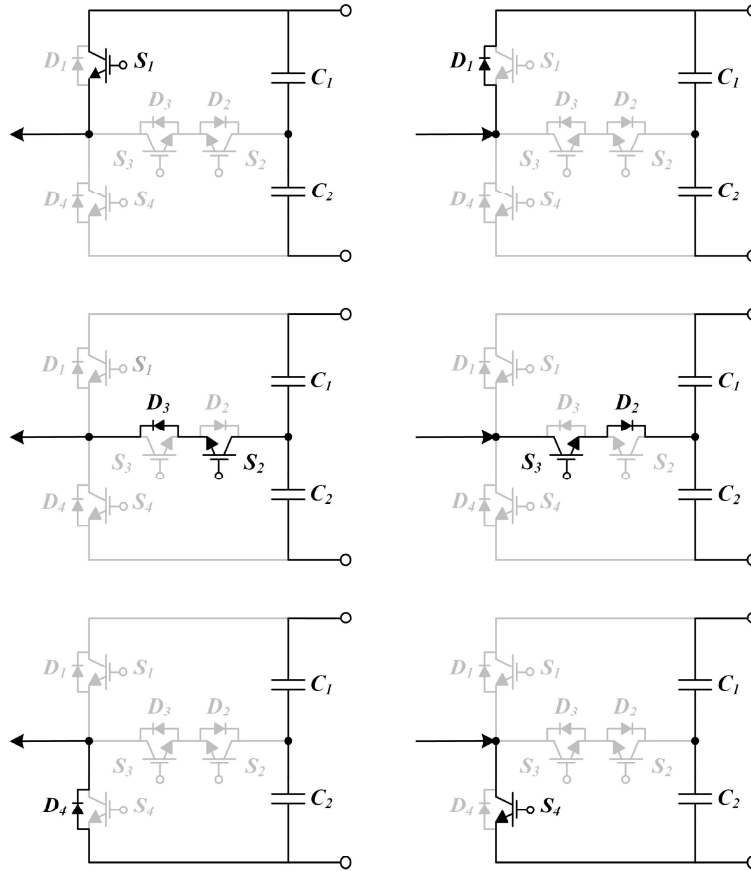
Figure 3.2: The switch commutations under different current directions in one phase

Based on the analysis above, the characteristics of the 3-phase 3-level T-type converter are as follows:

- When the output of one phase is P state or N state, only one of S_1 and S_4 is turned on and all the other switches are turned off. In this way, the conduction losses only depend on one switch for each phase.

- Unlike the half-bridge switches (S_1 and S_4), the bidirectional switches (S_2 and S_3) have to block only half of the DC link voltage, which means it is possible to use the devices having a lower voltage rating.

- The sign of the output voltage is not affected by the direction of the current.

Table 3.1: Relationship between the output voltage and states of the 3-phase 3-level T-type converter.

S_1	S_2	S_3	S_4	Output	States
ON	OFF	OFF	OFF	$U_{dc}/2$	P
OFF	ON	ON	OFF	0	O
OFF	OFF	OFF	ON	$-U_{dc}/2$	N

As is summarized in Table 3.1, when S_1 is turned on, the output voltage is high level; when S_2 and S_3 are turned on, the output voltage is 0; when S_4 is turned on, the output voltage is low level. However, three of the switches in one phase need to be changed during the transition between P state and O state or O state and N state, which increase the switching losses. Therefore, the switch commutation can be optimized in the following manner, which is shown in Table 3.2. Based on the analysis, there will be no influence, if S_2 is turned on during the P state. In the same way, turning on S_3 during the N state is also feasible. Therefore, only one switch in one phase needs to be changed during the transition mentioned, which will significantly improve converter efficiency.

Table 3.2: Optimized switch commutation of the 3-phase 3-level T-type converter.

S_1	S_2	S_3	S_4	Output	States
ON	ON	OFF	OFF	$U_{dc}/2$	P
OFF	ON	ON	OFF	0	O
OFF	OFF	ON	ON	$-U_{dc}/2$	N

For further mathematical model analysis, S_a, S_b and S_c are defined to be the output states of the 3-phase 3-level T-type converter for each phase. The value of S_i (i = a, b, or c) is -1, 0 or 1. Then the phase voltage relative to the mid-point O can be expressed as follows:

$$\begin{cases} U_{AO} = \dfrac{S_a}{2} U_{dc} \\[2mm] U_{BO} = \dfrac{S_b}{2} U_{dc} \\[2mm] U_{CO} = \dfrac{S_c}{2} U_{dc} \end{cases} \tag{3.1}$$

For an ideal switching model of the 3-phase 3-level T-type converter, the bridge arm of each phase could be considered as a single pole three-throw switch connecting the mid-point of the two capacitors. And then the 3-phase 3-level T-type converter can be simplified as the diagram shown in Fig 3.3, where the S_i is divided into S_a, S_b and S_c.
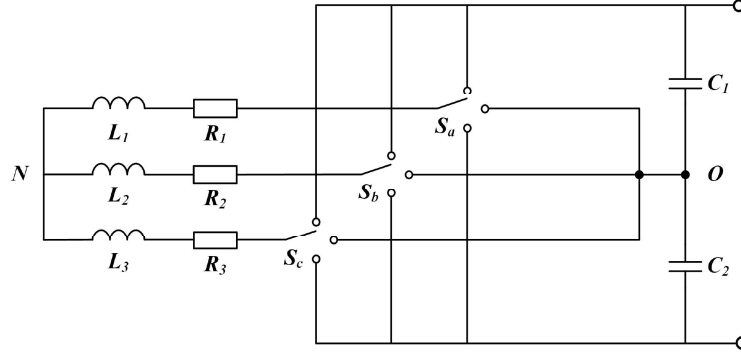
Figure 3.3: Simplified diagram of the 3-phase 3-level T-type converter

So the line voltage of the 3-phase 3-level T-type converter can be expressed as:

$$
\begin{cases}
U_{AB} = U_{AO} - U_{BO} = \dfrac{U_{dc}}{2}(S_a - S_b) \\[2mm]
U_{BC} = U_{BO} - U_{CO} = \dfrac{U_{dc}}{2}(S_b - S_c) \\[2mm]
U_{CA} = U_{CO} - U_{AO} = \dfrac{U_{dc}}{2}(S_c - S_a)
\end{cases}
\tag{3.2}
$$

And rewrite Eq 3.3 in matrix representation:

$$
\begin{bmatrix} U_{AB} \\ U_{BC} \\ U_{CA} \end{bmatrix}
= \frac{U_{dc}}{2}
\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}
\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}
\tag{3.3}
$$

For symmetrical three phase system:

$$
U_{AN} + U_{BN} + U_{CN} = 0
\tag{3.4}
$$

And also,

$$
\begin{cases}
U_{AN} = U_{AO} + U_{ON} \\[2mm]
U_{BN} = U_{BO} + U_{ON} \\[2mm]
U_{CN} = U_{CO} + U_{ON}
\end{cases}
\tag{3.5}
$$

By considering Eq 3.1, 3.4 and 3.5, it can be derived as:

$$
U_{ON} = -\frac{1}{3}\left(U_{AO} + U_{BO} + U_{CO}\right) = -\frac{1}{6}U_{dc}\left(S_a + S_b + S_c\right)
\tag{3.6}
$$

By considering Eq 3.1, 3.5 and 3.6, the relationship between the phase voltage and switching functions can be derived:

$$
\begin{bmatrix} U_{AN} \\ U_{BN} \\ U_{CN} \end{bmatrix}
= \frac{U_{dc}}{6}
\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}
\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}
\tag{3.7}
$$

3.3. Space Vector Pulse Width Modulation (SVPWM)

The Space Vector PWM (SVPWM) is widely used in 3-phase converters for its lower switching losses, lower THD and better utilization of DC bus voltage [46]. It is a digital modulation method that generates the required pulses based on the reference space vectors. The SVPWM is implemented under $\alpha - \beta$ frame and the vectors are placed in a hexagonal structure to represent magnitudes and phases, which will be demonstrated in detail in the following contents.
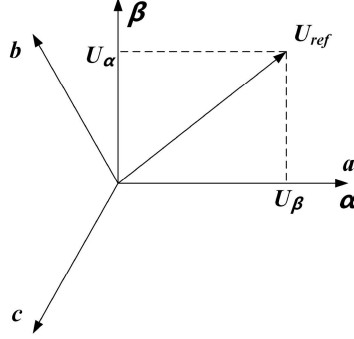
Figure 3.4: The reference vector under $\alpha - \beta$ frame

As is shown in Fig 3.4, $a - b - c$ is a 3-phase stationary coordinate system and $\alpha - \beta$ is a 2-phase stationary coordinate system. In order to convert variables under a 3-phase stationary coordinate system into the ones under a 2-phase stationary coordinate system, the principle to be followed is: the projection of the space vector on the a, b and c is exactly the instantaneous quantity of the a, b and c phases in the 3-phase stationary coordinate system. The voltage of each phase of the 3-phase AC system is:

$$
\begin{cases}
U_{AN} = U_m \cos(\omega t) \\[2mm]
U_{BN} = U_m \cos(\omega t - \dfrac{2}{3}\pi) \\[2mm]
U_{CN} = U_m \cos(\omega t + \dfrac{2}{3}\pi)
\end{cases}
\tag{3.8}
$$

where ω is the AC angular frequency and U_m is the voltage amplitude.

The voltage of each phase in the above formula represents the instantaneous value on the three axes of the space coordinate system, so the composite reference vector in the $a - b - c$ 3-phase coordinate system is:

$$
\begin{aligned}
V_{ref} &= U_{AN} + U_{BN}e^{j\frac{2\pi}{3}} + U_{CN}e^{j\frac{4\pi}{3}} \\[2mm]
&= U_{AN} + U_{BN}(\cos\frac{2\pi}{3} + j\sin\frac{2\pi}{3}) + U_{CN}(\cos\frac{4\pi}{3} + j\sin\frac{4\pi}{3}) \\[2mm]
&= U_{AN} + U_{BN}(-\frac{1}{2} + j\frac{\sqrt{3}}{2}) + U_{CN}(-\frac{1}{2} - j\frac{\sqrt{3}}{2}) \\[2mm]
&= (U_{AN} - \frac{1}{2}U_{BN} - \frac{1}{2}U_{CN}) + j(\frac{\sqrt{3}}{2}U_{BN} - \frac{\sqrt{3}}{2}U_{CN})
\end{aligned}
\tag{3.9}
$$

Meanwhile, under the 2-phase stationary coordinate system:

$$
\begin{cases}
V_{ref} = V_\alpha + jV_\beta \\[2mm]
V_\alpha = U_{AN} - U_{BN}/2 - U_{CN}/2 \\[2mm]
V_\beta = \sqrt{3}U_{BN}/2 - \sqrt{3}U_{CN}/2
\end{cases}
\tag{3.10}
$$

Substitute Eq 3.8 into Eq 3.10 to obtain:

$$
\begin{cases}
V_\alpha = U_m \cos \omega t + \dfrac{1}{2} U_m (-\dfrac{1}{2} \cos \omega t + \dfrac{\sqrt{3}}{2} \sin \omega t) + \dfrac{1}{2} U_m (-\dfrac{1}{2} \cos \omega t - \dfrac{\sqrt{3}}{2} \sin \omega t) \\[2mm]
\quad = \dfrac{3}{2} U_m \cos \omega t \\[2mm]
V_\beta = \dfrac{\sqrt{3}}{2} U_m (-\dfrac{1}{2} \cos \omega t + \dfrac{\sqrt{3}}{2} \sin \omega t) - \dfrac{\sqrt{3}}{2} U_m (-\dfrac{1}{2} \cos \omega t - \dfrac{\sqrt{3}}{2} \sin \omega t) \\[2mm]
\quad = \dfrac{3}{2} U_m \sin \omega t
\end{cases} \tag{3.11}
$$
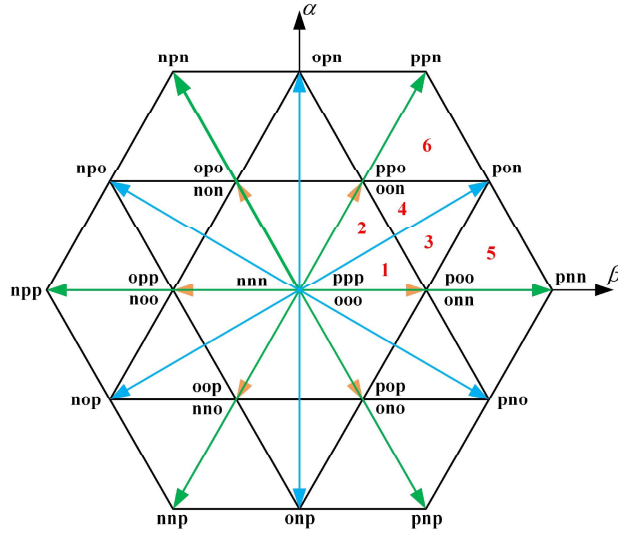
Figure 3.5: The reference vector under $\alpha - \beta$ frame

It can be found in the formula above that the amplitude of the voltage signal on the 2-phase coordinate system is 3/2 times the original. If the equal-amplitude transformation is used, the original vector expression needs to be multiplied by 2/3.

$$
V_{ref} = \frac{2}{3} (U_{AN} + U_{BN} e^{j\frac{2\pi}{3}} + U_{CN} e^{j\frac{4\pi}{3}}) \tag{3.12}
$$

Then Eq 3.11 can be transformed into:

$$
\begin{cases}
V_\alpha = U_m \cos(\omega t) \\[2mm]
V_\beta = U_m \sin(\omega t)
\end{cases} \tag{3.13}
$$

The magnitude of the composite vector is:

$$
V_{refm} = \sqrt{V_\alpha^2 + V_\beta^2} = U_m \tag{3.14}
$$

The angle of the composite vector is ωt. In this way, the process of obtaining the composite vector from the 3-phase given voltage is realized.

Based on the mathematical model (Eq 3.7) of the T-type converter under the 3-phase stationary coordinate system, there would be 27 output statuses because there are three possibilities for each value of S_a, S_b and S_c, which are 1, 0 and -1. It should be noted that the actual voltage in Table 3.3 should be multiplied by the DC link voltage U_{DC}, but here the DC link voltage is omitted in the table for simplicity of demonstration.

Table 3.3: Voltage states corresponding to 27 switch states

Switch States			AC Side Line Voltage			AC Side Phase Voltage		
S_a	S_b	S_c	U_{AB}	U_{BC}	U_{CA}	U_{AN}	U_{BN}	U_{CN}
P	P	P	0	0	0	0	0	0
O	O	O	0	0	0	0	0	0
N	N	N	0	0	0	0	0	0
P	O	O	1/2	0	-1/2	1/3	-1/6	-1/6
O	N	N						
P	P	O	0	1/2	-1/2	1/6	1/6	-1/3
O	O	N						
O	P	O	-1/2	1/2	0	-1/6	1/3	-1/6
N	O	N						
O	P	P	-1/2	0	1/2	-1/3	1/6	1/6
N	O	O						
O	O	P	0	-1/2	1/2	-1/6	-1/6	1/3
N	N	O						
P	O	P	1/2	-1/2	0	1/6	-1/3	1/6
O	N	O						
P	O	N	1/2	1/2	-1	1/2	0	-1/2
O	P	N	-1/2	1	-1/2	0	1/2	-1/2
N	P	O	-1	1/2	1/2	-1/2	1/2	0
N	O	P	-1/2	-1/2	1	-1/2	0	1/2
O	N	P	1/2	-1	1/2	0	-1/2	1/2
P	N	O	1	-1/2	-1/2	1/2	-1/2	0
P	N	N	1	0	-1	2/3	-1/3	-1/3
P	P	N	0	1	-1	1/3	1/3	-2/3
N	P	N	-1	1	0	-1/3	2/3	-1/3
N	P	P	-1	0	1	-2/3	1/3	1/3
N	N	P	0	-1	1	-1/3	-1/3	2/3
P	N	P	1	-1	0	1/3	-2/3	1/3

Table 3.4: Voltage space vectors under the $\alpha - \beta$ coordinate system

		$S_aS_bS_c$	U_α	U_β
Zero vectors	V_0	P P P	0	0
		O O O	0	0
		N N N	0	0
Small Vectors	V_1	P O O	1/3	0
		O N N		
	V_2	P P O	1/6	$\sqrt{3}/6$
		O O N		
	V_3	O P O	-1/6	$\sqrt{3}/6$
		N O N		
	V_4	O P P	-1/3	0
		N O O		
	V_5	O O P	-1/6	$-\sqrt{3}/6$
		N N O		
	V_6	P O P	1/6	$-\sqrt{3}/6$
		O N O		
Medium Vectors	V_7	P O N	1/2	$\sqrt{3}/6$
	V_8	O P N	0	$\sqrt{3}/3$
	V_9	N P O	-1/2	$\sqrt{3}/6$
	V_{10}	N O P	-1/2	$-\sqrt{3}/6$
	V_{11}	O N P	0	$-\sqrt{3}/3$
	V_{12}	P N O	1/2	$\sqrt{3}/6$
Large Vectors	V_{13}	P N N	2/3	0
	V_{14}	P P N	1/3	$\sqrt{3}/3$
	V_{15}	N P N	-1/3	$\sqrt{3}/3$
	V_{16}	N P P	-2/3	0
	V_{17}	N N P	-1/3	$-\sqrt{3}/3$
	V_{18}	P N P	1/3	$-\sqrt{3}/3$

According to Table 3.4, the vector distribution could be obtained under the $\alpha - \beta$ coordinate system, which is shown in Fig 3.6. It can be seen from the vector diagram that there are actually only 19 independent vectors, which are called basic space vectors, and the remaining eight vectors are the redundant vectors. The basic space vectors are divided into zero, small, medium and large vectors. The six large vectors divide the diagram into six large sectors, and each large sector is further divided into six regions by the medium and small sectors. In Fig 3.6, the first large sector is taken as an example, and the six small sectors are numbered for the following analysis.

Assuming that the basic voltage vectors are selected as V_1, V_2 and V_3, the basic space vectors and the voltage reference vector have the following relationship:

$$T_1 V_1 + T_2 V_2 + T_3 V_3 = T_s V_{ref} \tag{3.15}$$

$$T_s = T_1 + T_2 + T_3 \tag{3.16}$$

T_1, T_2 and T_3 are the corresponding action times of three basic vectors, and T_s is the sampling time. At each sampling time, there is a corresponding given reference voltage space vector. And the appropriate basic voltage vectors need to be selected to integrate it. The time required for each basic vector in one sampling period is calculated and then the pulse signal for each switch is generated through a specific algorithm to obtain the required equivalent vector. The position of the given voltage vector is different in each sampling period, so the accumulation of the vectors during multiple sampling periods will be equivalent to a vector circle. For example, for a 3-phase sine wave with a frequency of 50Hz, the rotation frequency of the final integrated voltage vector is also 50 Hz, so the time for rotation is 0.02s. If the sampling time is 0.0001s, there will be 200 space vectors in one cycle, which are evenly distributed over the entire circumference. The shorter the sampling time, the more space vectors will be integrated, and the closer the rotation trajectory of the integrated voltage vector is to a circle.
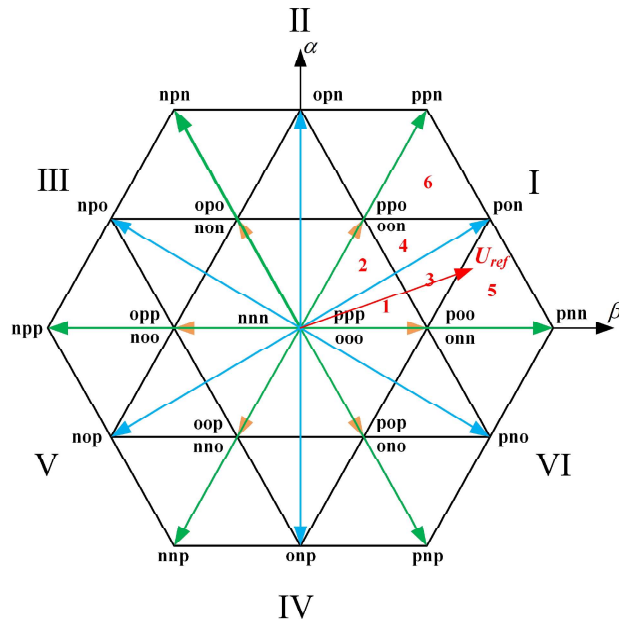
Figure 3.6: The reference vector under $\alpha - \beta$ frame

Based on the above analysis, the space vector diagram can be divided into six large sectors by 60 degrees. The first priority is to judge in which large sector the reference space vector is. All the corresponding action times of basic

vectors can be calculated based on the analysis in the first large sector. The specific judgment is as follows:

$$S = \text{ceil}\left(\frac{\theta}{60}\right)$$
$$\gamma = \theta - 60(S - 1)$$

(3.17)

where ceil is the round-up function, S represents the location of the large sector, θ represents the angle of the reference voltage vector, and γ represents the angle of the reference voltage vector in the large sector I. For example, if $\theta = 90$, then $S = 2$, $\gamma = 30$. In this way, the operation of the second large sector is transferred to the first large sector, and the same method can be applied to all the other sectors. Therefore, the action time of each vector in the other large sectors can be obtained by only calculating the action time of vectors in different positions in the first large sector. It is worth noting that the order of the action should correspond to the time instant, which will be analyzed in detail below.

After the judgment of large sectors, the small sectors in one single large sector also need to be judged. The main purpose is to figure out the three basic vectors used to integrate the reference vector. In the 3-level SVPWM method, one large sector would be divided into six regions, which is demonstrated in Fig. 3.7a. v_α and v_β are the coordinate components of the reference voltage vector on the α-axis and β-axis, respectively. From Table 3.4, the coordinates of A,B,C,D and E are:

$$O(0,0), A\left(\frac{1}{3}U_{DC}, 0\right), B\left(\frac{1}{6}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right), C\left(\frac{2}{3}U_{DC}, 0\right), D\left(\frac{1}{2}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right), E\left(\frac{1}{3}U_{DC}, \frac{\sqrt{3}}{3}U_{DC}\right)$$

Based on the coordinates, the equations of AB, BD and DA can be obtained:

$$AB : V_\beta = \frac{\sqrt{3}}{3}U_{DC} - \sqrt{3}V_\alpha$$
$$BD : V_\beta = \frac{\sqrt{3}}{6}U_{DC}$$
$$DA : V_\beta = -\frac{\sqrt{3}}{3}U_{DC} + \sqrt{3}V_\alpha$$

(3.18)

(a) The coordinate components of the reference vector

(b) Nearest Three Vectors Principle
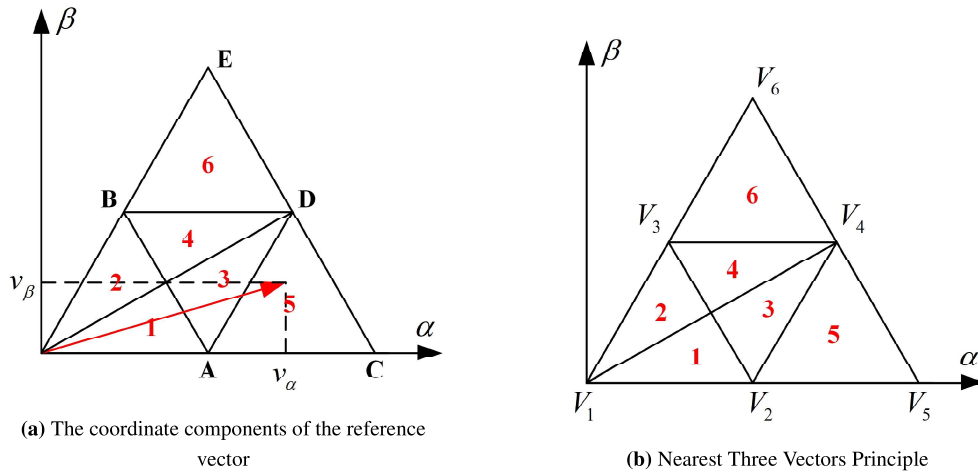
Figure 3.7: Geometry in Large Sector 1

The following part is the judgment of small sectors,

1. When $\theta \leq 30°$, V_{ref} is in the region 1, 3 or 5.

   If $V_\beta \leq \sqrt{3}V_{dc}/3 - \sqrt{3}V_\alpha$, then V_{ref} is below the line AB, which means that V_{ref} is in the region 1 ($n = 1$);

   If $V_\beta \leq -\sqrt{3}V_{dc}/3 + \sqrt{3}V_\alpha$, then V_{ref} is below the line DA, which means that V_{ref} is in the region 5 ($n = 5$);

   Otherwise, V_{ref} is in the region 3 ($n = 3$).

2. When $\theta \geq 30°$, V_{ref} is in the region 2, 4 or 6.

   If $V_\beta \leq \sqrt{3}V_{dc}/3 - \sqrt{3}V_\alpha$, then V_{ref} is below the line AB, which means that V_{ref} is in the region 2 ($n = 2$);

   If $V_\beta \geq \sqrt{3}V_{dc}/6$, then V_{ref} is above the line BD, which means that V_{ref} is in the region 6 ($n = 6$);

   Otherwise, V_{ref} is in the region 4 ($n = 4$).

After the judgment of small sectors, three basic vectors can be found according to the Nearest Three Vectors (NTV) Principle. The basic vectors selected from Fig 3.9b for each region are shown in Table 3.5.

Table 3.5: The basic vectors selected for each small sectors

Position of the reference vector	1	2	3	4	5	6
	V_1	V_1	V_2	V_2	V_2	V_3
Basic voltage vectors	V_2	V_2	V_3	V_3	V_4	V_4
	V_3	V_3	V_4	V_4	V_5	V_6

Once the basic vectors are selected, it is necessary to determine the action time of each vector. Assuming that the three vectors selected are V_1, V_2 and V_3, the reference vector is V_{ref}, and then one can obtain:

$$\begin{cases} T_1 V_{1\alpha} + T_2 V_{2\alpha} + T_3 V_{3\alpha} = T_s V_{\text{ref}\,\alpha} \\ T_1 V_{1\beta} + T_2 V_{2\beta} + T_3 V_{3\beta} = T_s V_{\text{ref}\,\beta} \\ T_1 + T_2 + T_3 = T_s \end{cases} \tag{3.19}$$

where T_1, T_2 and T_3 are the action times of the three basic vectors, respectively, and the subscripts α and β represent the components of the vector on the α and β axes. Based on the formula above, the solutions of T_1, T_2 and T_3 to the linear equation can be obtained. Since the six large sectors can be equivalent to each other through rotation, their time calculations are the same. It is just required to adjust the order of the corresponding action time in accordance with the action order of the respective vectors in different large sectors. For further clarification, the first large sector will be used as an illustration in the following.

First, set the three basic vectors in small sectors 1 and 2 as a, b and c, as shown in Fig 3.8a. Therefore, the coordinates of these three points are calculated as:

$$V_{12\_a} = \left(\frac{1}{6}U_{DC}, \frac{\sqrt{3}}{6}U_{DC} \right), V_{12\_b} = (0, 0), V_{12\_c} = \left(\frac{1}{3}U_{DC}, 0 \right)$$

The reference voltage vector can be decomposed as:

$$V_{\text{ref}} = (V_m \cdot \cos\theta, V_m \cdot \sin\theta)$$

(a) Small sector 1 and 2   (b) Small sector 3 and 4
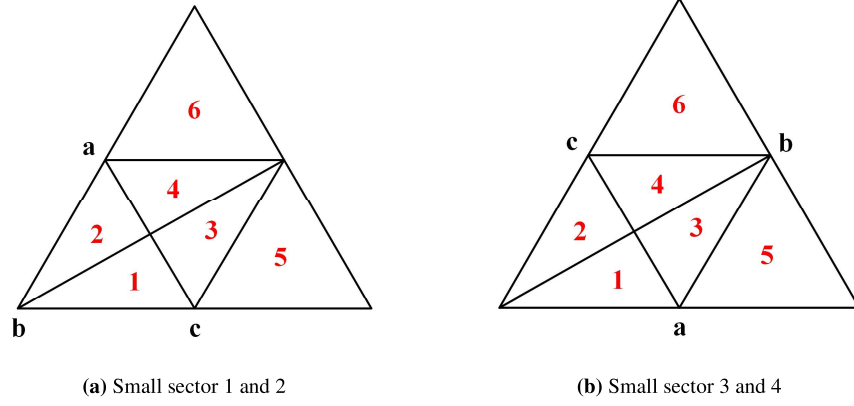
Figure 3.8: The vector action in small sectors 1, 2, 3 and 4

Substitute them into the time calculation Eq 3.19, and then one can obtain:

$$
\begin{cases}
\dfrac{1}{6}U_{DC}T_{12\_a} + \dfrac{1}{3}U_{DC}T_{12\_c} = V_m \cos\theta T_s \\[2mm]
\dfrac{\sqrt{3}}{6}U_{DC}T_{12\_a} = V_m \sin\theta T_s \\[2mm]
T_{12\_a} + T_{12\_b} + T_{12\_c} = T_s
\end{cases}
\tag{3.20}
$$

The solution to Eq 3.20 is given as:

$$
\begin{cases}
T_{12\_a} = 2mT_s \sin\theta \\[1mm]
T_{12\_b} = T_s - 2mT_s \sin(\pi/3 + \theta) \\[1mm]
T_{12\_c} = 2mT_s \sin(\pi/3 - \theta)
\end{cases}
\tag{3.21}
$$

where m is the modulation ratio of the three-level SVPWM control strategy, which is expressed as:

$$
m = \frac{\sqrt{3}V_m}{U_{DC}}
\tag{3.22}
$$

Three basic vectors in small sector 3 and 4 are also defined as a, b and c as shown in Fig 3.20. The coordinates of these three points are:

$$
V_{34\_a} = \left(\frac{1}{3}U_{DC}, 0\right), V_{34\_b} = \left(\frac{1}{2}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right), V_{34\_c} = \left(\frac{1}{6}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right)
$$

Substitute them into the time calculation Eq 3.19, and then one can obtain:

$$
\begin{cases}
\dfrac{1}{3}U_{DC}T_{34\_a} + \dfrac{1}{2}U_{DC}T_{34\_b} + \dfrac{1}{6}U_{DC}T_{34\_c} = V_m \cos\theta T_s \\[2mm]
\dfrac{\sqrt{3}}{6}U_{DC}T_{34\_b} + \dfrac{\sqrt{3}}{6}U_{DC}T_{34\_c} = V_m \sin\theta T_s \\[2mm]
T_{34\_a} + T_{34\_b} + T_{34\_c} = T_s
\end{cases}
\tag{3.23}
$$

The solution to Eq 3.23 is given as:

$$
\begin{cases}
T_{34\_a} = T_s - 2mT_s\sin\theta \\[2mm]
T_{34\_b} = -T_s + 2mT_s\sin(\pi/3 + \theta) \\[2mm]
T_{34\_c} = T_s - 2mT_s\sin(\pi/3 - \theta)
\end{cases}
\tag{3.24}
$$

(a) Small sector 5   (b) Small sector 6
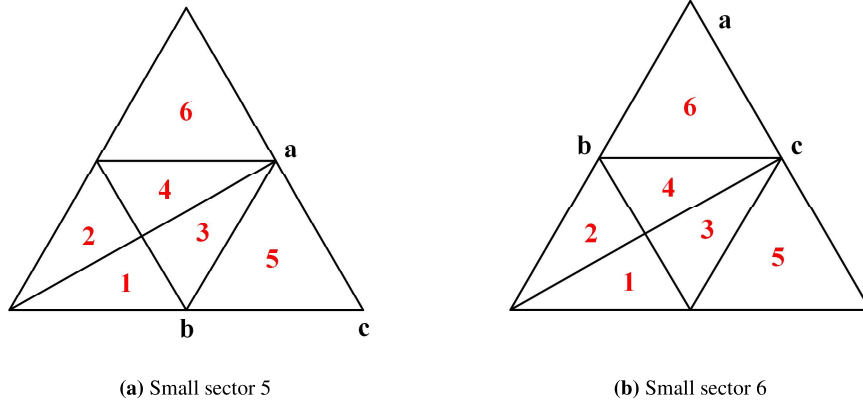
Figure 3.9: The vector action in small sector 5 and 6

As illustrated in Fig 3.9a, three basic vectors in small sector 5 are also specified as a, b, and c. The coordinates of these three points are:

$$
V_{5\_a} = \left(\frac{1}{2}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right), V_{5\_b} = \left(\frac{1}{3}U_{DC}, 0\right), V_{5\_c} = \left(\frac{2}{3}U_{DC}, 0\right)
$$

Substitute them into the time calculation Eq 3.19, and then one can obtain:

$$
\begin{cases}
\dfrac{1}{2}U_{DC}T_{5\_a} + \dfrac{1}{3}U_{DC}T_{5\_b} + \dfrac{2}{3}U_{DC}T_{5\_c} = V_m\cos\theta T_s \\[3mm]
\dfrac{\sqrt{3}}{6}U_{DC}T_{5\_a} = V_m\sin\theta T_s \\[3mm]
T_{5\_a} + T_{5\_b} + T_{5\_c} = T_s
\end{cases}
\tag{3.25}
$$

The solution to Eq 3.25 is given as:

$$
\begin{cases}
T_{5\_a} = 2mT_1\sin\theta \\[2mm]
T_{5\_b} = 2T_s - 2mT_s\sin(\pi/3 + \theta) \\[2mm]
T_{5\_a} = -T_s + 2mT_s\sin(\pi/3 - \theta)
\end{cases}
\tag{3.26}
$$

Likewise, small sector 6 is depicted in Fig 3.9, and the coordinates of these three points are:

$$
V_{6\_a} = \left(\frac{1}{3}U_{DC}, \frac{\sqrt{3}}{3}U_{DC}\right), V_{6\_b} = \left(\frac{1}{6}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right), V_{6\_c} = \left(\frac{1}{2}U_{DC}, \frac{\sqrt{3}}{6}U_{DC}\right)
$$

Substitute them into the time calculation Eq 3.19, and then one can obtain:

$$
\begin{cases}
\dfrac{1}{3}U_{DC}T_{6\_a} + \dfrac{1}{6}U_{DC}T_{6\_b} + \dfrac{1}{2}U_{DC}T_{6_{c}c} = V_m \cos\theta T_s \\[2mm]
\dfrac{\sqrt{3}}{3}U_{DC}T_{6\_a} + \dfrac{\sqrt{3}}{6}U_{DC}T_{6\_b} + \dfrac{\sqrt{3}}{6}U_{DC}T_{6\_c} = V_m \sin\theta T_s \\[2mm]
T_{6\_a} + T_{6\_b} + T_{6\_c} = T_s
\end{cases}
\tag{3.27}
$$

The solution to Eq 3.27 is given as:

$$
\begin{cases}
T_{6\_a} = -T_s + 2mT_s \sin\theta \\[2mm]
T_{6\_b} = 2T_s - 2mT_s \sin(\pi/3 + \theta) \\[2mm]
T_{6\_c} = 2mT_s \sin(\pi/3 - \theta)
\end{cases}
\tag{3.28}
$$

The calculation process and formula of the first large sector are discussed above, and the corresponding switching time for the next five large sectors can be determined by substituting different θ values. When the reference voltage vector is rotated clockwise or counterclockwise, the space vector will transit from one valid state to another valid state, and then a continuous three-phase voltage can be generated, whose frequency is consistent with the rotation frequency of the reference vector.

After judging the sector and calculating the action time of the basic vectors, it is necessary to arrange the action sequence of the basic vectors of each sector. For the time allocation in the three-level SVPWM algorithm, the following points are mainly considered:

1. In order to facilitate the balance control of the mid-point voltage of two capacitors and to reduce the common-mode voltage of the output terminal, the seven-segment switching sequence is used, and the action time of the zero vector is evenly distributed. It can be also used as a transition state to comply with the minimum switching principle.

2. In order to reduce the harmonics at the output terminal and also the switching losses, it is preferred to alter the switching state of only one phase bridge arm at one time while switching from one switching state to another. If the switches of two or three bridge arms act simultaneously for one single switching state transition, electromagnetic noise or greater pulsations may occur.

3. In the two-level topology, the zero vector is utilized as the initial vector, while in the three-level topology, the problem of vector changes in the process of mutual conversion between different regions needs to be considered. Typically, the vertex of the small regular hexagon is chosen as the starting vector, which means that 12 small vectors are used as the starting vectors.

4. In order to avoid the detrimental effects of small vectors on the neutral point voltage imbalance, the action time of redundant vectors in one single switching period should be evenly distributed. For example, POO and ONN are a pair of redundant vectors.

Combined with the preceding principles, the action sequence of basic vectors in all small sectors is presented in Table 3.6. It can be seen from Table 1 that the first, fourth and seventh segments in the seven-segment switching sequence represent vectors at the same position, and thus they share the same period of time. According to the symmetry, the remaining four segments each account for half of the corresponding time period. And the time allocation methods for the corresponding vectors of all small sectors are the same, namely $T_{x1}/4$, $T_{x2}/2$, $T_{x3}/2$, $T_{x1}/2$, $T_{x3}/2$, $T_{x2}/2$, $T_{x1}/4$. In addition, the preceding table demonstrates that the time allocation order of the small sectors corresponding to the large sector I, III and V is identical. Therefore, it is sufficient to obtain the allocation of each small sector in the

large sector I, and then the time allocation of the vector in the large sector III and V can be subsequently obtained. The same holds valid for the large sector II, IV and VI. The division and time calculation of the small sectors also reveal that the time allocation of the small sector 1 and 2 is only in a different order, but the value is the same. And the same holds for the small sectors 3 and 4.
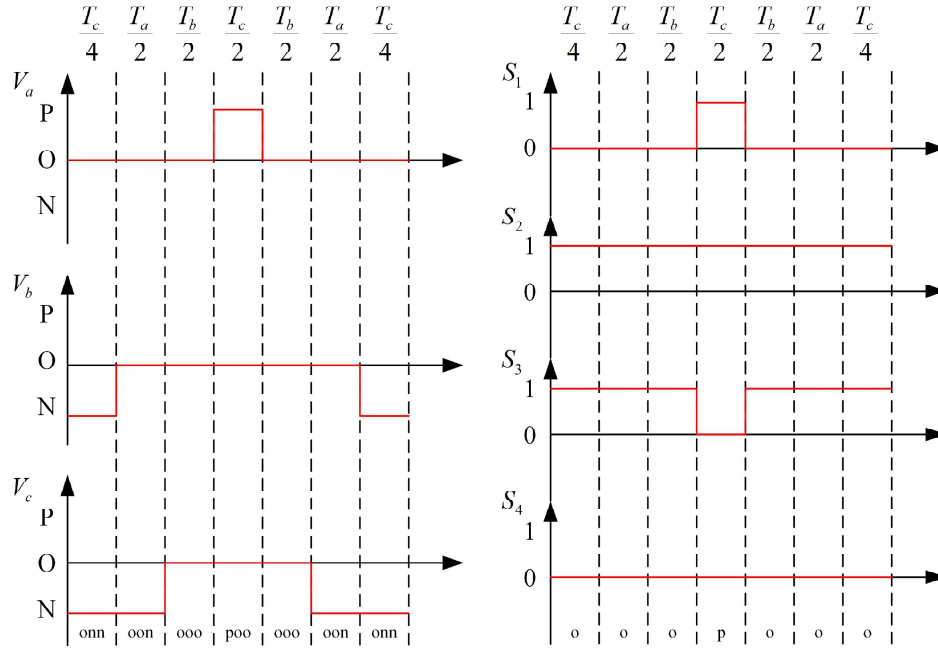
Figure 3.10: Generation of 12 drive pulses

As depicted in Figure 3.10, the generation of the drive pulses of the switches will be described using the small sector 1 of the large sector I as an example. In the left figure, V_a, V_b, and V_c represent the switch states corresponding to the a, b, and c bridge arm, while the right figure represents the switch states corresponding to the four switches of phase A during the sampling period. Before generating the drive pulses, it is necessary to first determine the switch states of the three bridge arms based on the calculated time and then assign the appropriate drive pulse to each switch based on the switch state so that the required 12 switch pulse signals can be obtained.

As shown in Figure 3.11, the overall block diagram of the SVPWM algorithm can be obtained.
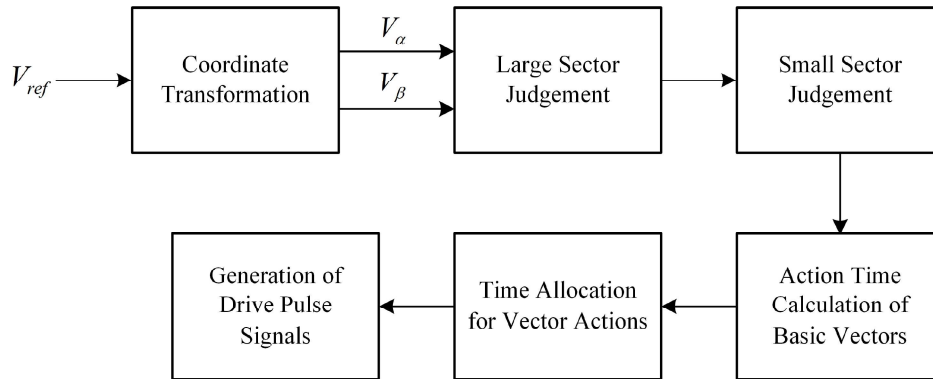
Figure 3.11: The overall block diagram of the SVPWM algorithm

Table 3.6: The action sequence of basic vectors in all small sectors

Region	The action order of basic vectors	Region	The action order of basic vectors
1-1	onn(c)-oon(a)-ooo(b)-poo-ooo-oon-onn	4-1	noo(c)-ooo(b)-oop(a)-opp-oop-ooo-noo
1-2	oon(a)-ooo(b)-poo(c)-ppo-poo-ooo-oon	4-2	nno(a)-noo(c)-ooo(b)-oop-ooo-noo-nno
1-3	onn(a)-oon(c)-pon(b)-poo-pon-oon-onn	4-3	noo(a)-nop(b)-oop(c)-opp-oop-nop-noo
1-4	oon(c)-pon(b)-poo(a)-ppo-poo-pon-oon	4-4	nno(c)-noo(a)-nop(b)-oop-nop-noo-nno
1-5	onn(b)-pnn(c)-pon(a)-poo-pon-pnn-onn	4-5	noo(b)-nop(a)-npp(c)-opp-npp-nop-noo
1-6	oon(b)-pon(c)-ppn(a)-ppo-ppn-pon-oon	4-6	nno(b)-nnp(a)-nop(c)-oop-nop-nnp-nno
2-1	oon(c)-ooo(b)-opo(a)-ppo-opo-ooo-oon	5-1	nno(c)-ono(a)-ooo(b)-oop-ooo-ono-nno
2-2	non(a)-oon(c)-ooo(b)-opo-ooo-oon-non	5-2	ono(a)-ooo(b)-oop(c)-pop-oop-ooo-ono
2-3	oon(a)-opn(b)-opo(c)-ppo-opo-opn-oon	5-3	nno(a)-ono(c)-onp(b)-oop-onp-ono-nno
2-4	non(c)-oon(a)-opn(b)-opo-opn-oon-non	5-4	ono(c)-onp(b)-oop(a)-pop-oop-onp-ono
2-5	oon(b)-opn(a)-ppn(c)-ppo-ppn-opn-oon	5-5	nno(b)-nnp(c)-onp(a)-oop-onp-nnp-nno
2-6	non(b)-npn(a)-opn(c)-opo-opn-npn-non	5-6	ono(b)-onp(c)-pnp(a)-pop-pnp-onp-ono
3-1	non(c)-noo(a)-ooo(b)-opo-ooo-noo-non	6-1	ono(c)-ooo(b)-poo(a)-pop-poo-ooo-ono
3-2	noo(a)-ooo(b)-opo(c)-opp-opo-ooo-noo	6-2	onn(a)-ono(c)-ooo(b)-poo-ooo-ono-onn
3-3	non(a)-noo(c)-npo(b)-opo-npo-noo-non	6-3	ono(a)-pno(b)-poo(c)-pop-poo-pno-ono
3-4	noo(c)-npo(b)-opo(a)-opp-opo-npo-noo	6-4	onn(c)-ono(a)-pno(b)-poo-pno-ono-onn
3-5	non(b)-npn(c)-npo(a)-opo-npo-npn-non	6-5	ono(b)-pno(a)-pnp(c)-pop-pnp-pno-ono
3-6	noo(b)-npo(c)-npp(a)-opp-npp-npo-noo	6-6	onn(b)-pnn(a)-pno(c)-poo-pno-pnn-onn

3.4. Control Strategy of T-type Converter

The overall control diagram of the three-phase T-type converter is shown in Fig 3.12. Due to the design of the overall system structure, the voltage of the DC bus will be determined by the BESS to a relatively stable level to ensure the normal operation of the T-type converter. As a result, the T-type converter control design in this system primarily consists of current loop control, capacitor current feedback, and neutral point balance control.

3.4.1. Current Loop Control

Primarily, the current is measured in the $a - b - c$ frame, which is sinusoidal. But mostly, the current controls are implemented in the $d - q$ frame because the ProportionalIntegral (PI) controller is typically used to achieve zero error tracking. However, the PI controller has an infinite gain only at zero frequency. So if the PI controller is chosen to be implemented, the AC currents should be transformed from the $a - b - c$ frame to the $d - q$ frame. Besides, the control can be also implemented under $\alpha - \beta$ frame. As previously stated, in order to realize zero error tracking, the infinite gain is needed at the critical frequency, which is the fundamental frequency of grid voltage (50Hz). The

Proportional-Resonant (PR) controller has an infinite gain at the resonant frequency, so what is required is to set the resonant frequency equal to the fundamental frequency of the grid voltage, and then an infinite gain is obtained here. In this manner, the $d - q$ frame is not necessary to realize zero error tracking of AC current.
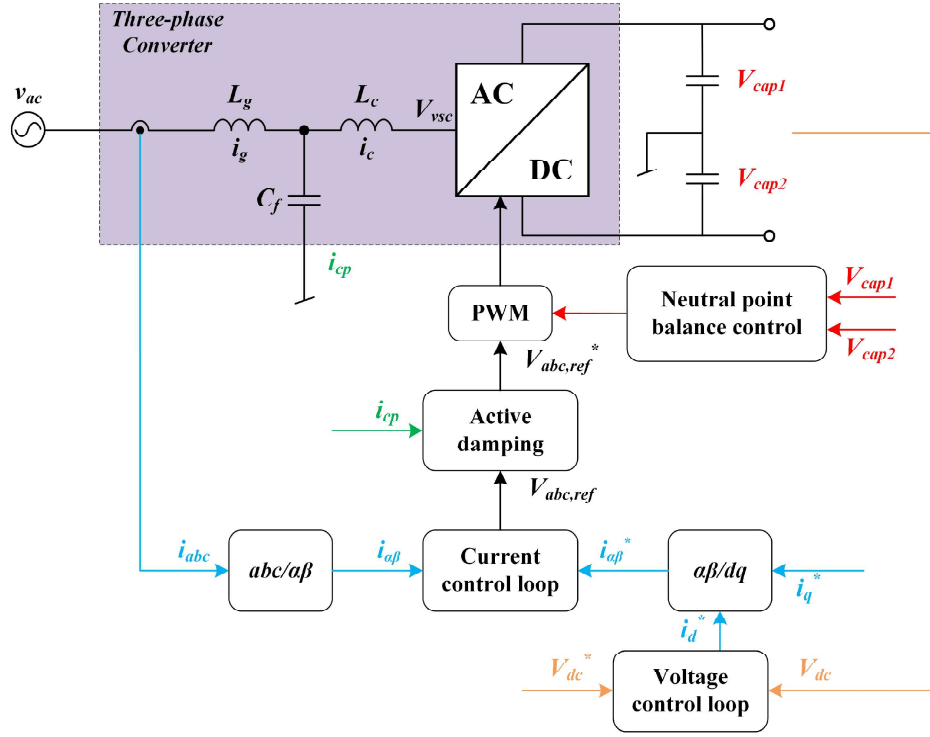
Figure 3.12: The overall control diagram of three-phase T-type converter

The transfer function of the grid-side current can be expressed as:

$$i_{\mathrm{g}} = \frac{1}{s^3 L_{\mathrm{g}} L_{\mathrm{c}} C_{\mathrm{f}} + s L_{\mathrm{g}} + s L_{\mathrm{c}}} v_{\mathrm{vsc}} - \frac{s^2 L_{\mathrm{c}} C_{\mathrm{f}} + 1}{s^3 L_{\mathrm{g}} L_{\mathrm{c}} C_{\mathrm{f}} + s L_{\mathrm{g}} + s L_{\mathrm{c}}} v_{\mathrm{ac}} \qquad (3.29)$$

where L_g is the grid-side filter, L_c is the converter-side filter, and C_f is the filter capacitor.

And the dynamic of the AC-side LCL filter is expressed as Eq 3.30. In order to implement respective control, it can also be expressed in $\alpha\beta$ frame as Eq 3.31 and Eq 3.32.

$$L_{\mathrm{c}} L_{\mathrm{g}} C_{\mathrm{f}} \frac{d^3 i_{\mathrm{ac}}}{dt^3} + L_{\mathrm{c}} \frac{di_{\mathrm{ac}}}{dt} + L_{\mathrm{g}} \frac{di_{\mathrm{ac}}}{dt} - L_{\mathrm{c}} C_{\mathrm{f}} \frac{d^2 v_{\mathrm{ac}}}{dt^2} = v_{\mathrm{ac}} - v_{\mathrm{vsc}} \qquad (3.30)$$

$$L_{\mathrm{c}} L_{\mathrm{g}} C_{\mathrm{f}} \frac{d^3 i_{\mathrm{ac},\alpha}}{dt^3} + L_{\mathrm{c}} \frac{di_{\mathrm{ac},\alpha}}{dt} + L_{\mathrm{g}} \frac{di_{\mathrm{ac},\alpha}}{dt} - L_{\mathrm{c}} C_{\mathrm{f}} \frac{d^2 v_{\mathrm{ac},\alpha}}{dt^2} = v_{\mathrm{ac},\alpha} - v_{\mathrm{vsc},\alpha} \qquad (3.31)$$

$$L_{\mathrm{c}} L_{\mathrm{g}} C_{\mathrm{f}} \frac{d^3 i_{\mathrm{ac},\beta}}{dt^3} + L_{\mathrm{c}} \frac{di_{\mathrm{ac},\beta}}{dt} + L_{\mathrm{g}} \frac{di_{\mathrm{ac},\beta}}{dt} - L_{\mathrm{c}} C_{\mathrm{f}} \frac{d^2 v_{\mathrm{ac}}}{dt^2} = v_{\mathrm{ac},\beta} - v_{\mathrm{vsc},\beta} \qquad (3.32)$$

As mentioned before, the $\alpha\beta$ frame is essentially the same as the $a - b - c$ frame, and the only difference is that there are two axes other than three. Since v_{ac} is sinusoidal, $v_{ac,}$, $v_{ac,}$, $i_{\alpha,ref}$ and $i_{\beta,ref}$ are also sinusoidal. Therefore, in this system, the PR controller is implemented to track the sinusoidal signal, and the transfer function $G_{\mathrm{c}}(s)$ is shown as Eq 3.33. Because this transfer function will have an infinite gain at ω_0, a more practical controller is introduced as Eq 3.34.

$$G_c(s) = K_p + \frac{2K_i s}{s^2 + \omega_0^2} \tag{3.33}$$

$$G_c(s) = K_p + \frac{2K_i \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{3.34}$$

where K_p, K_i are the coefficients of PR controller, ω_0 is the angular frequency of grid, and ω_c is the cutting-off frequency.

The overall block diagram of the current controller is shown in Fig 3.13.
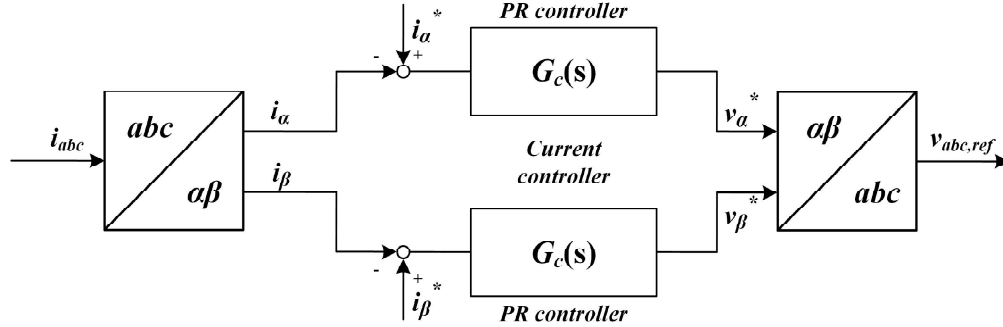
Figure 3.13: The control block diagram of the current controller

3.4.2. Voltage Loop Control

Typically, the closed loop control for a three-phase T-type converter comprises an outer voltage loop and an inner current loop. Although in the final system integration, the DC bus is directly connected to the BESS, the outer voltage loop is still necessary for the separate simulation for the 3-phase T-type converter. As is derived in [47], Eq 3.35 describes dynamics of V_{DC}^2.

$$\frac{dV_{DC}^2}{dt} = \frac{2}{C}P_{ext} - \frac{2}{C}P_{\text{loss}} - \frac{2}{C}\left[P_s + \left(\frac{2LP_s}{3\widehat{V}_s^2}\right)\frac{dP_s}{dt}\right] + \frac{2}{C}\left[\left(\frac{2LQ_s}{3\widehat{V}_s^2}\right)\frac{dQ_s}{dt}\right]. \tag{3.35}$$

where C is the total DC link capacitor, P_{ext} is a time-varying power on the DC side, P_s and Q_s is the real power and the reactive power on the AC side, P_{loss} is the power of the converter. Therefore, in order to control V_{DC}^2, it should be compared with the reference $V_{DC,ref}^2$ by an outer loop. The error will be processed by a compensator, and also $P_{s,ref}$ will be delivered into the inner current loop, which regulates P_s at $P_{s,ref}$.

A transfer function from P_s to V_{DC}^2 can be derived as Eq 3.36 if transformed to Laplacian domain.

$$G_v(s) = -\left(\frac{2}{C}\right)\frac{\tau s + 1}{s} \tag{3.36}$$

where the time constant τ is

$$\tau = \frac{2LP_{s0}}{3\widehat{V}_s^2} = \frac{2LP_{ext0}}{3\widehat{V}_s^2} \tag{3.37}$$

Finally, the block diagram of the DC bus voltage control is described in Fig 3.14
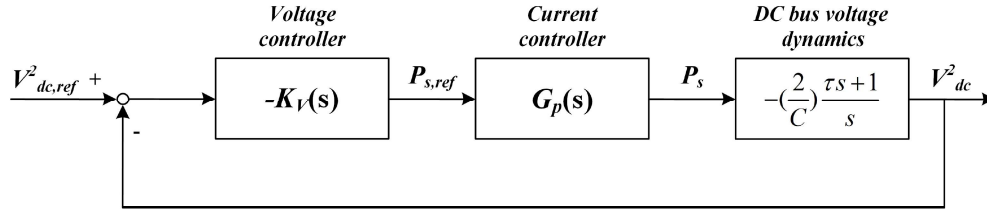
Figure 3.14: The control block diagram of the voltage controller

where $K_v(s)$ is a PI controller and the transfer function is expressed as:

$$K_V(s) = K_{pv} + \frac{K_{iv}}{s} \tag{3.38}$$

where K_{pv}, K_{iv} are the PI controller coefficients.

3.4.3. Capacitor Current Feedback

The LCL filter is widely adopted for grid-connected voltage source converters (VSCs). Compared with the L filter, the LCL filter is a third-order filter. Therefore, to achieve the same attenuation, the LCL filter requires less total inductance, and thereby less weight and volume of the filter. However, the influence on the system stability is the major concern of the implementation of the LCL filter when providing effective damping of the filter resonances [46],[48],[49].

In the digitally controlled system, there will be delays associated with computation and pulse width modulation (PWM). In synchronous sampling, the computation delay is the time period between the sampling and the PWM reference update instant, which means one sampling period [50]. If the symmetric sampled PWM with the single update is implemented here, the computation delay is one sampling period T_s. For example, the current is sampled at t_1. But the PWM reference will be updated at t_2, which means one sampling time period T_s. And the computation delay $G_d(s)$ can be expressed as:

$$G_d(s) = e^{-sT_s} \tag{3.39}$$

Besides, the PWM delay should also be considered during this process. The PWM delay is the result of the zero-order hold (ZOH) effect, which maintains the PWM reference after it has been updated, and it is definitely half sampling period [51], which can be expressed as $G_h(s)$:

$$G_h(s) = \frac{1 - e^{-sT_s}}{s} = e^{-0.5sT_s} \tag{3.40}$$

Combining Eq 3.39 and Eq 3.40, the total delay of the digital control can be expressed as $G_{td}(s)$:

$$G_{td}(s) = G_d(s) + G_h(s) = T_s e^{-1.5sT_s} \tag{3.41}$$

Fig 3.16 depicts the equivalent circuit of the LCL filter with capacitor current i_c, and the feedback of i_c is equivalent to adding a parallel impedance Z_{ad} to the filter capacitor, which is expressed as Eq 3.43 [52].

As shown in Fig 3.17, the current control loop is modified by i_c feedback via gain $G_a(s)$, and the relationship between Z_a and $G_a(s)$ can be described by:

$$Z_a(s) = \frac{L_c}{G_a(s)G_{td}(s)C_f} \tag{3.42}$$
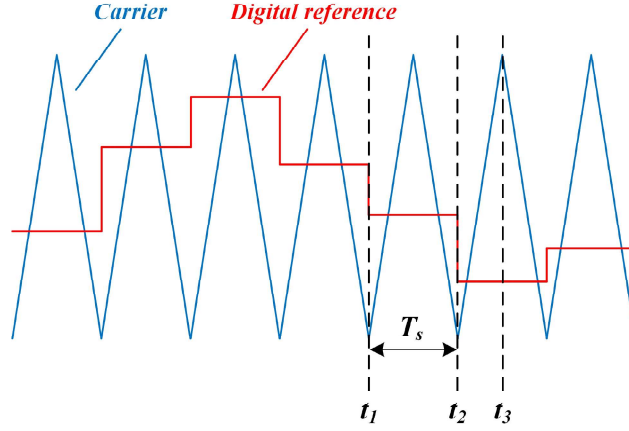
Figure 3.15: The total delay of the digital control

$$Z_{\mathrm{ad}} = R_{\mathrm{ad}} + jX_{\mathrm{ad}} \tag{3.43}$$
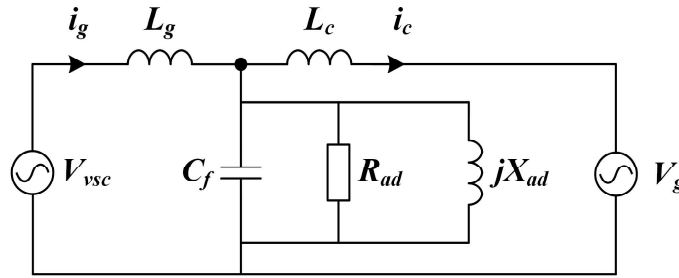
Figure 3.16: The equivalent circuit of capacitor current feedback

Here, the transfer function of active damping is chosen as a constant K_a:

$$G_{\mathrm{a}}(s) = K_{\mathrm{a}} \tag{3.44}$$

The equivalent impedance behaves like a virtual resistor the system delay G_{td} is not considered. Nevertheless, the proportional feedback results in the virtual impedance if the delay is included, and the impedance can be calculated as follows:

$$Z_a(s) = \frac{L_c}{K_a C_f} e^{1.5 s T_s} = R_a e^{1.5 s T_s} \tag{3.45}$$

And the virtual resistor can be expressed as:

$$R_{\mathrm{a}} = \frac{L_c}{K_{\mathrm{a}} C_f} \tag{3.46}$$

Substituting $s = j\omega$ into Eq 3.45:

$$Z_{\mathrm{a}}(j\omega) = R_{\mathrm{a}} \left[\cos\left(\frac{3}{2}\omega T_{\mathrm{s}} \right) + j \sin\left(\frac{3}{2}\omega T_{\mathrm{s}} \right) \right] \tag{3.47}$$
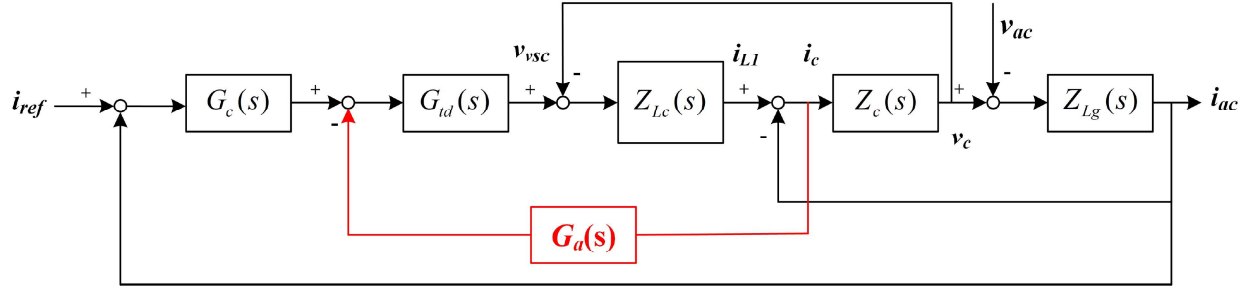
Figure 3.17: Block diagram of using active damping

According to Eq 3.47, Both the resistive and inductive (or capacitive) components will be affected by the system delay. In the meantime, it has been demonstrated that the resistive component becomes negative when the resonance frequency is above $1/6f_s$ [52]. Therefore, the proportional feedback gain of the capacitor's current must be designed properly for a well-tuned controller.

3.4.4. Neutral Point Balancing Control

For three-level converters, another inherent issue is the balancing of DC link capacitance voltage. It is assumed that the two capacitors have identical initial voltages. The voltage imbalance of DC link capacitors will occur only when the mid-point current is not zero. And this is related to the space vector switching state implemented over a period of time. Specifically, both the zero vectors and the large vectors do not contribute to the unbalanced voltage of the capacitors, as shown in Fig 3.18. In addition, for the small vectors in Fig 3.19a, they can be generated by two conduction states, thus redundant vectors, namely positive commutation state and negative commutation state, are obtained. As mentioned in the previous passages, in the optimal space vector sequence, the action time of redundant vectors in one single switching period would be evenly distributed, which means that they are implemented with the same duty cycle, but at different instants in time. Therefore, the balance of capacitor voltages will be affected during this process. Moreover, Fig 3.19b reveals that the medium vectors are also responsible for the unbalance because of the presence of the mid-point current [22].

To alleviate these capacitance unbalance issues, three primary methods have been proposed:

1. Implement external hardware to compensate for the mid-point current.

2. Adjust sequence of vectors (Only small/medium vectors are responsible for the unbalance).

3. Use control strategy and zero sequence injection.

(a) Zero vector PPP   **(b)** Large vector PNN
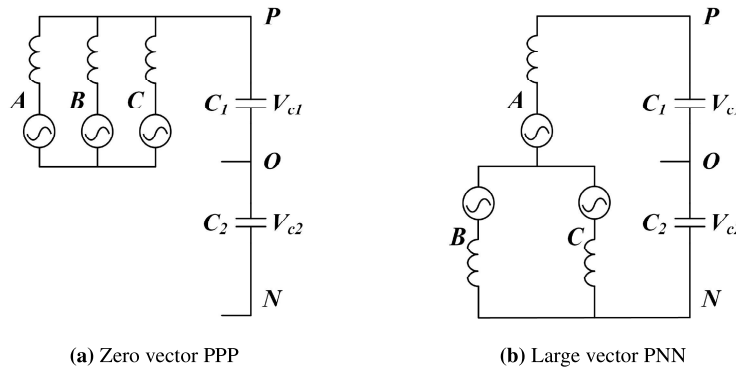
Figure 3.18: Examples of different switching states (1)

(a) Small vector POO   **(b)** Medium vector PNO
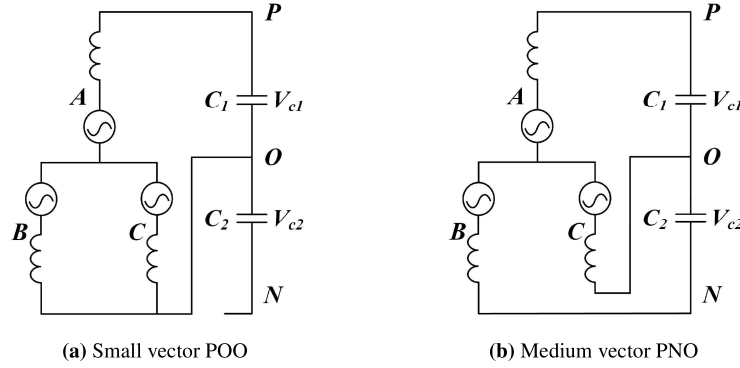
Figure 3.19: Examples of different switching states (2)

(a) Positive commutation state   **(b)** Negative commutation state
(POO)   (ONN)
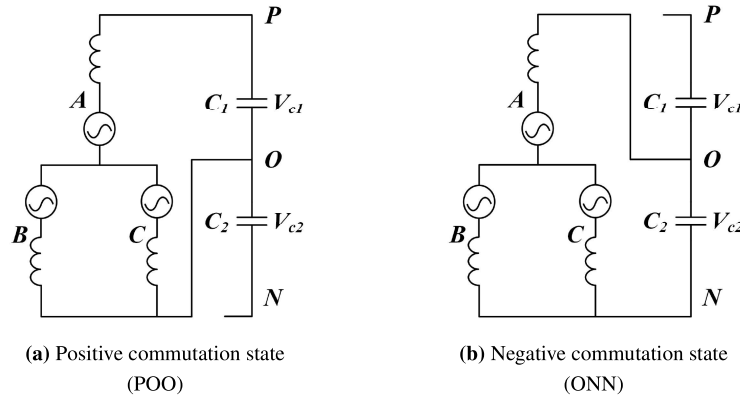
Figure 3.20: Different commutation states of the small vector

Here, a capacitor-voltage loop with a proportional-resonant (PR) controller is implemented, and the block diagram of the neutral point balancing control is depicted in Fig 3.21. It is known that the injected third-harmonic PWM method not only improves the utilization of the dc link voltage of the 3-phase inverters but also causes an average pulse neutral point current [53]. If a variable zero sequence component is added to make the final actual neutral point current close to zero, the unbalance issue would be suppressed. Actually, the voltage difference between two capacitors Δu_{12} reflects the essence of the neural point voltage fluctuation, which means a component that alternates with the triple fundamental frequency. Therefore, Δu_{12} could be utilized as a zero-sequence component that efficiently suppresses the voltage unbalance, necessitating the use of a capacitor-voltage loop control method with a PR controller.
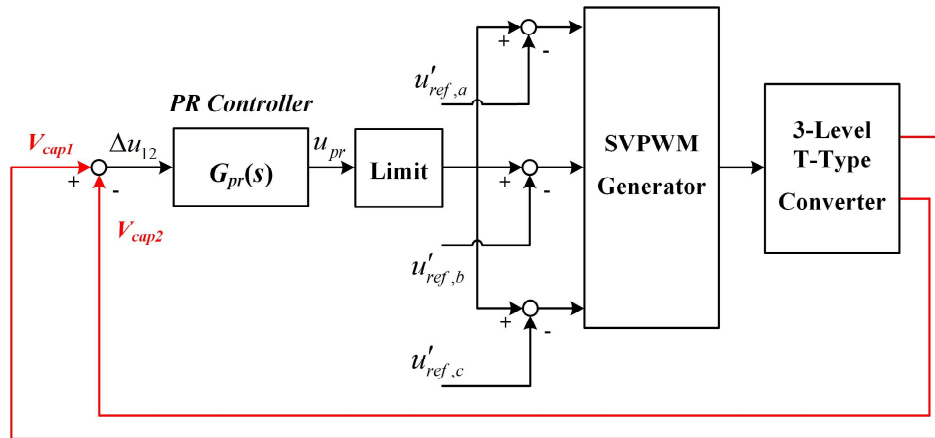
Figure 3.21: Block diagram of NP balance

The second zero-sequence component u_{pr} can be obtained by Eq 3.48:

$$u_{pr} = \Delta u_{12} \cdot G_{pr}(s) \tag{3.48}$$

$G_{pr}(s)$ is the transfer function of the PR controller, which can be written as Eq 3.49:

$$G_1(s) = k_p + k_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{3.49}$$

where k_p is the proportional coefficient, k_r is the resonant coefficient, ω_0 is the resonant angular frequency and ω_c is the cutoff angular frequency.

<div style="text-align: right; font-size: 4em;">4</div>

Design of Battery Energy Storage System

4.1. Introduction

The integration of energy storage as part of the charging station is an effective way to alleviate the high demand generated during peak electricity consumption hours. In order to obtain a practical design of a Battery Energy Storage System (BESS), some basic factors including capacity, terminal voltage, maximum C-rate, specific energy, price, losses, etc. should be considered. In this chapter, several different types of state-of-the-art cylindrical 18650 battery cells are calculated and compared, and the most suitable battery cell is chosen, all in accordance with the design requirements and the availability of relevant data. This result informs the design of battery packs made from this battery cell, which is then thermally simulated using a sub-model technique to ensure accuracy in spite of computational constraints, which accounts for factors such as the layout of battery packs, the impact of airflow direction on heat dissipation, and the temperature distribution across the pack. Most importantly, the interaction of the design of the AC/DC conversion stage and the BESS is also analyzed and summarized. The overall scope for Chapter 4 is depicted in Fig 4.1.
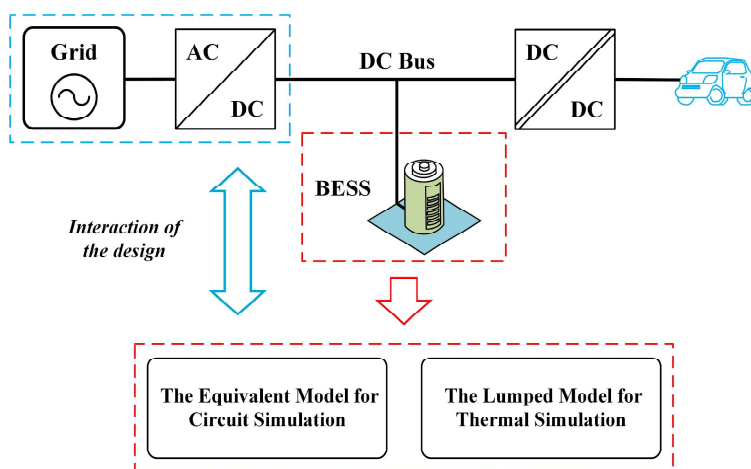
Figure 4.1: The overall scope for Chapter 4

4.2. The Equivalent Model of Lithium-ion Battery

Based on the state-of-the-art research, it is difficult to directly measure the microscopic physical parameters of lithium batteries using measurement techniques [54, 55, 56]. Therefore, developing suitable equivalent models according to specific analysis is quite critical. Considering its various building mechanisms, the battery model can be classified as the equivalent circuit model, electrochemical model and black box model [57]. Numerous studies employ the equivalent circuit model because its parameters have a clear physical meaning and it strikes a good balance between computational complexity and accuracy [58]. When attempting to describe the dynamic behavior of a battery, it is the widespread procedure to use a dynamic battery model that contains multiple RC parallel circuits, such as the Thevenin model, the dual polarization model [57, 59], which are depicted in Fig 4.2. The fundamental concept behind it is to use ohm internal resistance to describe the instantaneous change in terminal voltage and use RC-links to characterize the polarization effect of the battery [60]. The analysis of ch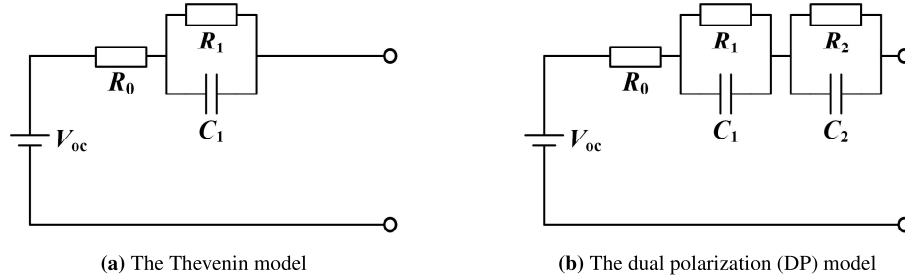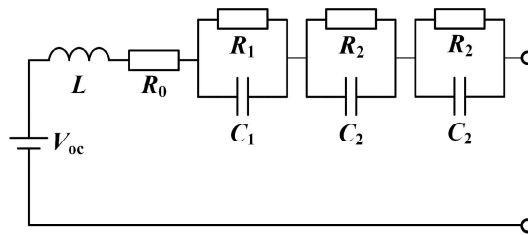emical reactions within the battery forms the basis for the electrochemical model, and the partial differential equation is established to characterize the behavior of the electrodes and electrolyte [61]. Furthermore, the response characteristics of battery voltage can also be described by a linear or non-linear function known as the black-box model [62, 63]. A black-box model allows for versatile model structure establishment and parameter optimization, but it is devoid of physical significance. The selection of the model relies on the features of the models. For instance, the electrochemical model is suitable for the optimization design of batteries and the safety analysis of these designs. On the other hand, the equivalent circuit model is suitable for the simulation of engineering practices and systems.

The equivalent circuit model is the best option because it could be used throughout the system-level discussion in subsequent simulations. And it appears that the three RC-link models, as shown in Fig 4.3, adequately describe battery dynamics and ohmic battery losses. On the one hand, the equivalent circuit model consists of a series inductor denoted by L_R and a series resistor denoted by R_0. On the other hand, the transient behavior of a battery can be described using the three-time constants, represented by R_1C_1 to R_3C_3.

$$Z_{\text{Cell,3RC}} = j\omega L_\text{R} + R_0 + \sum_{n=1}^{3} \frac{R_n}{1 + j\omega R_n C_n} \tag{4.1}$$

(a) The Thevenin model   (b) The dual polarization (DP) model

Figure 4.2: Common used equivalent circuit models of battery

Figure 4.3: The three RC-link model

The dynamic behavior of the battery cell is captured by this model over a range of frequencies from a few hertz to a few kilohertz. However, the accuracy of the model is determined by the battery cell and the desired battery behavior, both of which are largely subject to the intended use.

4.3. Comparison of Different Cylindrical 18650 Battery Cells

In this section, the key battery parameters of several different types of cutting-edge cylindrical 18650 battery cells are compared comprehensively. In addition, the estimated impedance parameters are also provided for subsequent analysis, according to [64]. The battery cells presented in Table 4.1 are the ones that are compared in this thesis. [65] and [66] are the primary sources for the characteristic parameters of battery cells. In general, all of the listed cells have a cylindrical 18650 geometry and the typical range of cell capacities Q is between 2600 mAh and 3500 mAh, with nominal battery voltage V_N around 3.7 V. The C-rate is a measurement of the rate at which a battery is fully charged or discharged. For instance, a C-rate of 1C indicates that the battery is charged from 0% to 100% in one hour. Likewise, a C-rate higher or lower than 1C results in faster or slower charging, respectively. The Max C-rate in Table 4.1 indicates the maximum permissible C-rate at discharge for the candidate batteries, which essentially means the maximum permissible current at discharge. Another important parameter derived from datasheets is the specific energy e_{Cell}, which is the proportion of energy contained in a battery in relation to its weight (Eq 4.2). Since the price of the batteries is also a key design criterion, it is also considered in this comparison.

$$e_{Cell} = \frac{V_N Q}{m_{Cell}} \tag{4.2}$$

Table 4.1: Parameters of candidate battery cells

Model	Capacity Q(mAh)	Voltage V_N(V)	Max C-rate	Specific energy e_{Cell}(Wh/kg)	Price (EUR)
LG Chem INR18650MJ1	3500	3.7	3.3	264.28	7.95
LG Chem INR18650HG2	3000	3.7	6.7	226.53	8.95
LG Chem INR18650M26	2600	3.7	4	225.29	2.99
Sony Murata Konion US18650VTC6	3120	3.7	10	247.73	10.49
Sony Murata Konion US18650VTC5A	2600	3.7	13.5	213.78	8.94
KeepPower P1834J	3400	3.7	2	262.08	11.9
Nitecore 18650 NL1835HP	3500	3.7	2.3	239.81	20.95
Samsung INR18650-30Q	3000	3.7	5	231.25	9.9

The parameters of the three RC-link model has also been listed in Table 4.2. LG Chem INR18650MJ1 and Nitecore 18650 NL183 have the highest capacity (3500mAh). Therefore, they can be classified as high-energy cells. Sony Murata Konion US18650V has the highest Max C-rate, which means that the maximum current allowed during the discharge process is the highest. However, as the C-rate increases, so does the actual energy loss converted to heat, which may result in a reduction in the actual available energy of the batteries. The comparison of the impedance is primarily based on the internal resistance R_0. As shown in Table 4.2, the KeepPower P1834J represents the maximum resistance of 101.01 mΩ, while the minimum internal resistance of the Sony Murata Konion US18650VTC6 is 12.82 mΩ. The loss of BESS during charging and discharging is also affected by the internal resistance of batteries. In addition to the aforementioned factors, LG Chem INR18650M has a significant price advantage, costing only 2.99 EUR per cell. Overall, the studied batteries exhibit various characteristics in different aspects. To illustrate the given battery cell comparisons, Fig 4.4 shows a five-axis radar chart considering the cells capacity, max C-rate, specific

energy, price, and impedance. It should be noted that all the absolute value are normalized by dividing the greatest value for each metric because of the different magnitudes. Therefore, the radar chat is only used to present the relative value of the same parameters for different batteries.

Table 4.2: Battery parameters for the three RC-pair model

Model	$L_R(nH)$	$R_0(m\Omega)$	$R_1(m\Omega)$	$C_1(mF)$	$R_2(m\Omega)$	$C_2(mF)$	$R_3(m\Omega)$	$C_3(mF)$
LG Chem INR18650MJ1	358.75	43.10	1.77	768.68	2.30	906.10	2.26	1290
LG Chem INR18650HG2	98.01	17.82	1.19	569.54	1.32	1087.72	1.42	1190
LG Chem INR18650M26	372.23	40.08	2.68	659.19	3.67	943.75	3.55	1270
Sony Murata Konion US18650VTC6	83.57	12.82	1.56	430.08	1.80	1190.20	2.40	810
Sony Murata Konion US18650VTC5A	98.62	73.64	1.55	908.24	2.04	1132.24	1.99	1110
KeepPower P1834J	153.03	101.01	4.43	509.48	5.42	965.03	6.84	1670
Nitecore 18650 NL1835HP	153.46	54.30	4.27	586.53	5.36	1064.61	5.92	1460
Samsung INR18650-30Q	72.95	13.15	1.16	434.11	1.23	1017.04	1.47	1210

Based on the adaptation to the entire system, the following basic requirements for BESS are proposed:

1. The ratio of BESS to grid-side power supply is set to 1:2 for grid assistance and easy implementation.

2. Given the available information on electric vehicles nowadays, it is assumed that the capacity of EV battery is 100 kWh. Thus, the BESS is designed to provide at least 2/3 of its capacity, or 67 kWh, during one charging cycle.

3. Due to the structure of the overall EV charger, the terminal voltage of the BESS must be stable for the AC/DC converter to function properly, which means to prevent over-modulation. The DC link should have a minimum voltage of 700V to leave enough margin.

4. Since the total power required to be provided is 450 kW, the power that the BESS can provide is at least 300 kW. Therefore, the system demands should also be met by the maximum allowable C-rate at discharge.

5. In addition, considering the actual energy loss converted to heat, the efficiency of BESS needs to be controlled at around 95%

In a BESS, the individual battery cells can be connected either in series or in parallel, depending on the specific requirement. On the one hand, the number of series connections has the most significant impact on the terminal voltage of the entire battery pack. This, in turn, has an effect on the voltage of the DC bus and determines whether or not the T-type converter functions normally. On the other hand, assuming that the number of connections in series has already been determined, the number of connections in parallel (or the total number) will mainly affect the loss of the battery pack. Based on the above analysis, it can be summarized as the following formula:

$$N_s V_N I - \frac{R_i N_s}{N_p} I^2 = P_o \tag{4.3}$$

$$V_t = \frac{P_o}{I} \tag{4.4}$$

$$\eta = \frac{P_o}{N_s V_N I} \tag{4.5}$$
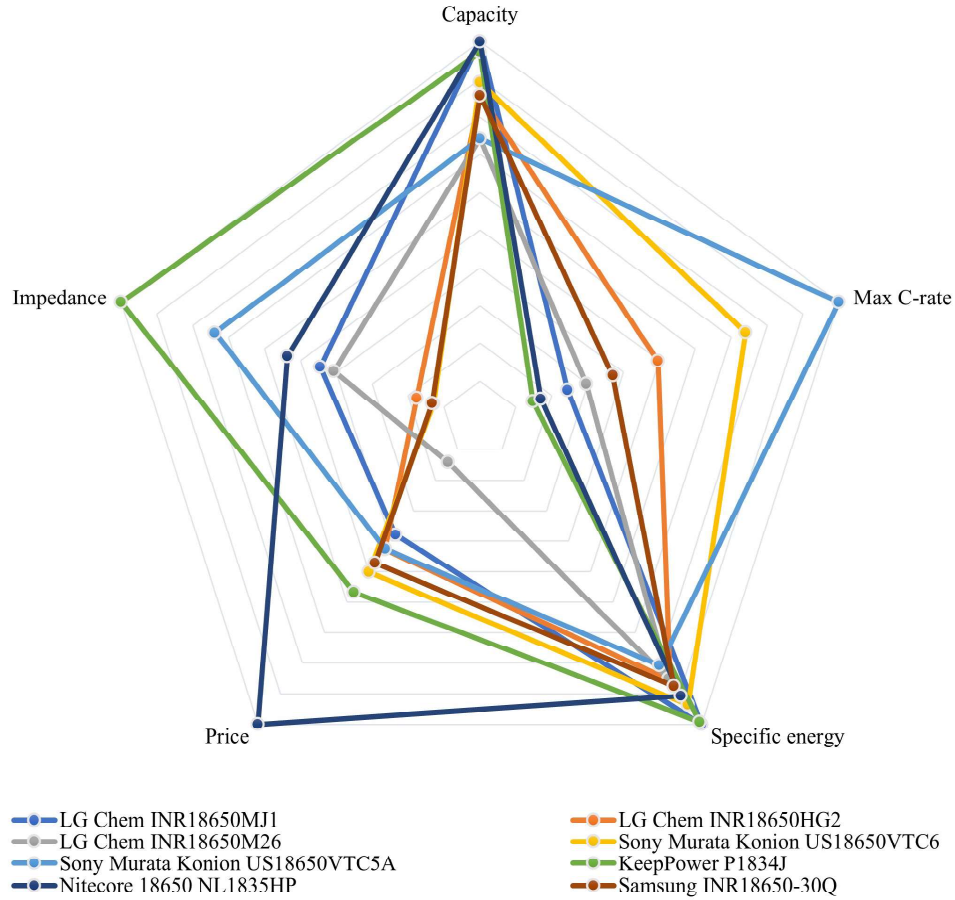
**Figure 4.4:** Multiple-criteria evaluation of the selected batteries

where N_s is the number of series connection, N_p is the number of parallel connection, I is the current flowing through the BESS, R_i is the internal impedance of one single battery cell, P_o is the output power of the BESS, V_t is the terminal voltage of the BESS, and η is the efficiency of the BESS.

Based on the formula above, the minimum serial number of each battery is obtained through the requirements for the DC bus voltage, and then the minimum parallel number is obtained through the requirements for the BESS loss. As shown in Table 4.3, Sony Murata Konion US18650VTC6 and Samsung INR18650-30Q require the least number of battery cells at 8610 and 7917, respectively. At the same time, when both weight and price are taken into account, the Samsung INR18650-30Q is the superior option to the Sony Murata Konion US18650VTC6.

Taking Samsung INR18650-30Q as an example, the total number in Fig 4.5a is first set to a minimum value, which is based on the required battery capacity. The terminal voltage gradually rises as the number of series increases, eventually reaching the predetermined level of 700V. Fig 4.5b shows the process by which the minimum value of the number of parallels can be determined. After the selection of the minimum series number, the number of parallels is increased while the losses of BESS are decreased until they reach 5%. Furthermore, it can be seen from Fig 4.6 that if the losses other than those caused by the internal impedance of the battery are ignored, and the total number of the battery remains unchanged, then the losses of BESS also remains the same. Besides, in the case of the non-integer number of parallel in Fig 4.5a and 4.6, this is due solely to the consideration of the numerical relationship and will be adjusted to an integer in the actual number design.

Table 4.3: The number of series and parallel connection of different batteries

Model	Minimum number of series	Minimum number of parallel	Minimum total number
LG Chem INR18650MJ1	270	86	23220
LG Chem INR18650HG2	208	49	10192
LG Chem INR18650M26	236	98	23128
Sony Murata Konion US18650VTC6	205	42	8610
Sony Murata Konion US18650VTC5A	359	102	36618
KeepPower P1834J	379	144	54576
Nitecore 18650 NL1835HP	379	86	32594
Samsung INR18650-30Q	203	39	7917
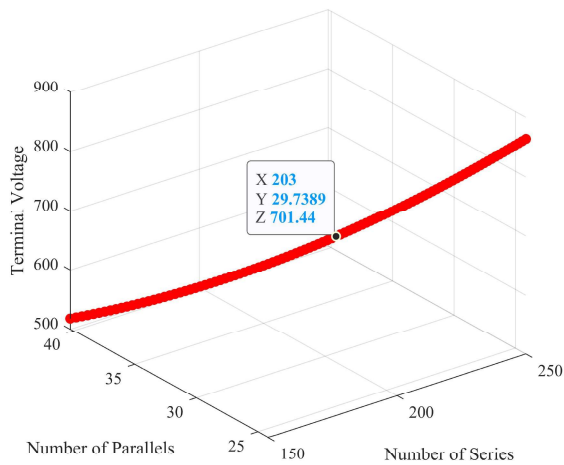
(a) The number of batteries in series   **(b)** The number of batteries in parallel
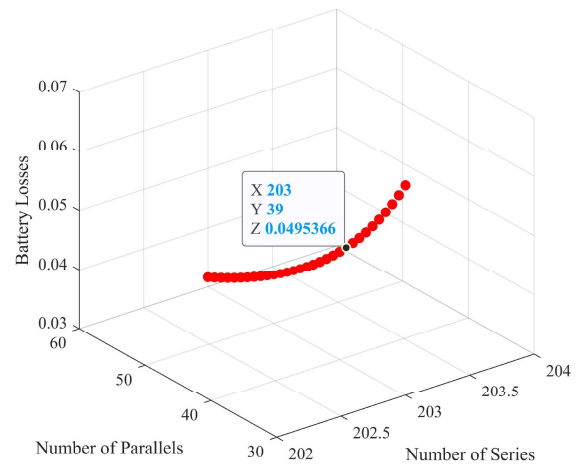
Figure 4.5: The number of batteries
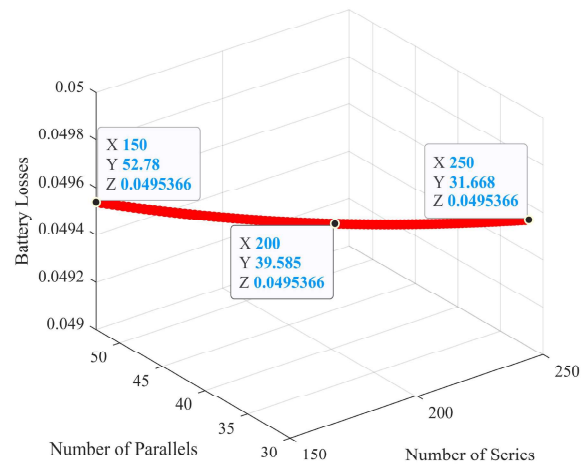
Figure 4.6: Losses while keeping the total number constant

4.4. Thermal studies with different geometric configuration

Li-ion batteries are superior to alternative energy storage technologies in terms of specific energy and energy density, making them ideal for the adoption in electric vehicles and related BESS systems. However, Li-ion cells are extremely delicate when exposed to heat, making thermal management of Li-ion cells and battery packs an important area of research [67]. The electrical, electrochemical, and thermal phenomena that occur in Li-ion batteries interact through well-known processes, such as species diffusion, charge transport, chemical kinetics, heat transport etc [68]. Therefore, heat generation is an inevitable result of the energy conversion and storage process of Li-ion batteries. Li-ion battery internal properties are typically strong functions of battery temperature and electrochemical state. Overheating a battery can initiate an internal decomposition reaction, which can eventually result in fires and explosions due to thermal runaways. To avoid the scenario described above, it is prudent to conduct thermal analyses of the battery packs.

Some articles have performed relevant thermal simulations for smaller scale battery packs [69, 70, 71], but for larger battery packs consisting of thousands of cells, the efficient and quick simulation remains a challenge. This is due to the existence of multiple length scales, which can make meshing and computation time-consuming. Thermal simulations were also performed on only a small portion of the package rather than the entire package in some articles [72, 73]. However, it is also essential to have an understanding of the non-uniformity of the temperature distribution throughout the battery pack, which can only be achieved by the entire simulation. Therefore, this thesis makes a trade-off between computation time and accuracy and adopts the method of sub-modeling, which was originally developed for mechanical stress simulation. The same principle applies to thermal simulations [74, 75], but limited research has been done on thermal simulations of Li-ion battery packs. The fundamental concept behind sub-modeling is to initially model and simulate the global model of the entire geometry without taking details into consideration. The results of the global model are then utilized to obtain the boundary condition for the refined local model. In this manner, the global model is used to study the temperature distribution of the whole system, but the calculation speed is much faster compared with the full-scale simulation model. By isolating the areas that are predicted to cause the highest temperature increase, it can avoid simulating the entire geometry in intricate details. The basic idea of sub-modeling is depicted in Fig 4.7.

Global Model

Boundary

Full-scale Model
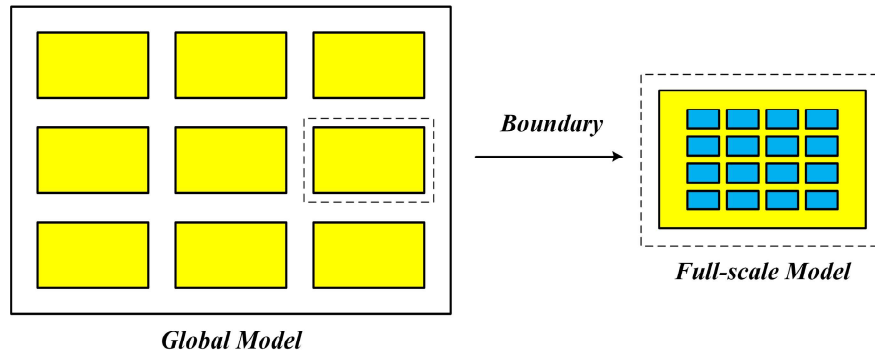
Figure 4.7: The basic idea of sub-modeling

The general sub-modeling process mentioned earlier will be applied to the thermal simulation of Li-ion battery packs in COMSOL. According to the calculation of the number of series and parallels, a BESS system consisting of 8000 Samsung INR18650-30Q cells in total (the number of series is 200 and the number of parallels is 40) will be modeled. And each pack will contain 400 cells. Thermal modeling of batteries with COMSOL is typically realized by using two approaches: high-fidelity modeling or lumped modeling. While high-fidelity modeling can provide insight into the concentration and transport of lithium ions or current and potential distributions for individual cells, it is

computationally expensive for the thermal simulation of large battery packs. In addition, it is often difficult to obtain the input parameters required for high-fidelity models. With fewer input parameters and lower computational costs, the lumped model can achieve acceptable simulation accuracy. Transport and reaction processes in electrodes can be described with a single-particle model, which significantly reduces computational resources in comparison to more detailed models. The lumped model employs a small number of lumped parameters to describe how mass transport, charge transfer, and ohmic processes affect the battery's potential loss.

In general, the battery cell voltage E_{cell} is described as follows:

$$E_{\text{cell}} = E_{\text{OCV}}(\text{SOC}, T) + \eta_{\text{IR}} + \eta_{\text{act}} + \eta_{\text{conc}} \tag{4.6}$$

where η_{IR} is the ohmic overpotential, η_{act} is the activation overpotential, and η_{conc} is the concentration overpotential. E_{ocv} is the open-circuit voltage of the cell, which is influenced by the state of charge SOC and the temperature T, as stated in:

$$E_{\text{OCV}}(\text{SOC}, T) = E_{\text{OCV,ref}}(\text{SOC}) + (T - T_{\text{ref}}) \frac{\partial E_{\text{OCV}}(\text{SOC})}{\partial T} \tag{4.7}$$

where $E_{\text{OCV,ref}}$ is the E_{ocv} at the reference temperature T_{ref}. And the time evolution of SOC is defined as:

$$\frac{\partial \text{SOC}}{\partial t} = \frac{I_{\text{cell}}}{Q_{\text{cell},0}} \tag{4.8}$$

where I_{cell} is the applied current and $Q_{\text{cell},0}$ is the capacity of the battery cell.

The equation for calculating the lumped voltage loss associated with the ohmic process in the electrolyte and electrodes is as follows:

$$\eta_{\text{IR}} = \eta_{\text{IR,1C}} \frac{I_{\text{cell}}}{I_{\text{1C}}} \tag{4.9}$$

where I_{1C} is the ohmic overpotential at 1C, and

$$I_{\text{1C}} = \frac{Q_{\text{cell},0}}{3600\text{s}} \tag{4.10}$$

Overpotential activation voltage loss, which occurs on both the positive and negative electrode surfaces, is defined as:

$$\eta_{\text{act}} = \frac{2RT}{F} \text{asinh}\left(\frac{I_{\text{cell}}}{2J_0 I_{\text{1C}}}\right) \tag{4.11}$$

where R denotes the molar gas constant, T is the temperature, F is the Faraday's constant, and J_0 is the dimensionless charge exchange current.

In order to take the influence of temperature on ohmic overpotential at 1C, dimensionless charge exchange current and diffusion constant, a impact factor k_{arrh} could be defined by Arrhenius equation:

$$k_{\text{arrh}} = e^{\frac{E_a}{R_{\text{const}}} \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)} \tag{4.12}$$

where E_a is the activation energy for the reaction, R_{const} is the universal gas constant, T is the actual temperature and T_0 is the reference temperature.

Finally, the battery heat source is defined as follows:

$$Q_{\text{h}} = \left(\eta_{\text{IR}} + \eta_{\text{act}} + T \frac{\partial E_{\text{OCV}}(\text{SOC}, T)}{\partial T}\right) I_{\text{cell}} \tag{4.13}$$

The detailed geometry of one single battery pack is shown in Fig 4.8, which consists of 400 Samsung INR18650-30Q cells in total. Specifically, the number of series is 10 and the number of parallels is 40. In order to achieve the tightest arrangement between cells, the cells are staggered and connected by copper connectors. At the same time, every two rows of batteries are tightly wrapped by a copper heat sink to aid in heat dissipation.
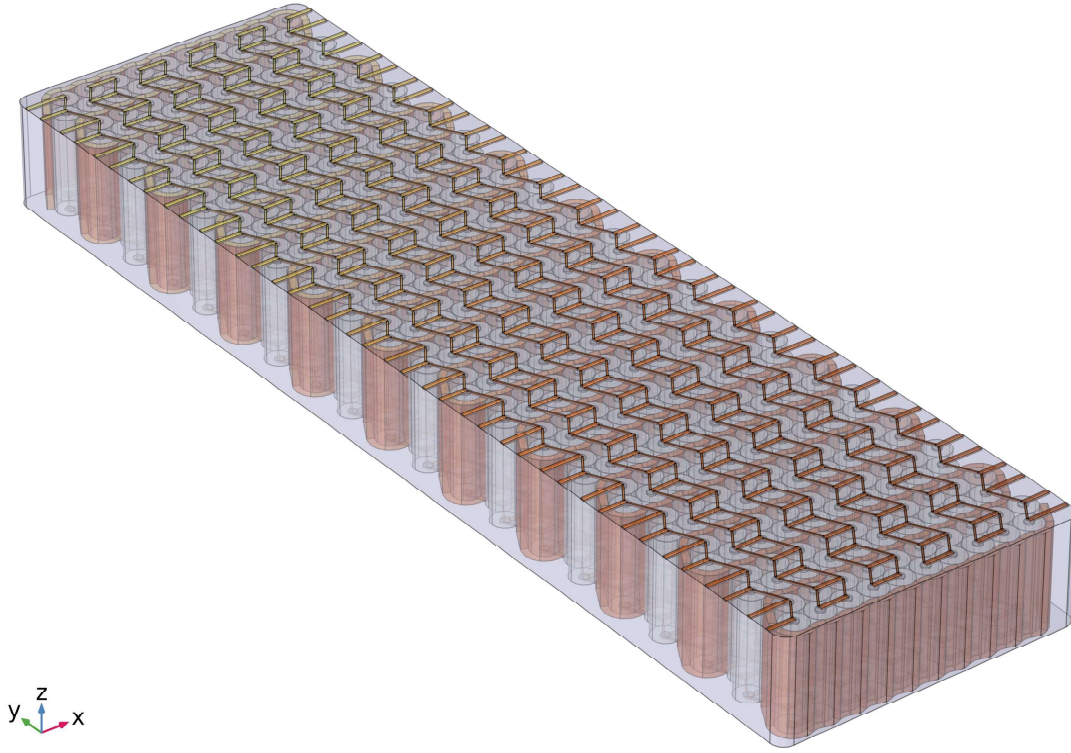
Figure 4.8: The geometry of one single battery pack

The required input parameters of the battery for the thermal simulation are listed in Table 4.4 [76].

Table 4.4: List of parameters used in the model

Parameter	Value	Unit	Description
d_{cell}	0.018	m	Diameter of the cells
h_{cell}	0.065	m	Height of the cells
Q_{cell}	10800	C	Cell capacity as rated by the supplier
I_{1C}	3	A	Current corresponding to 1C
T_{ref}	303.15	K	Reference temperature
$Ea_{\text{eta,1C}}$	24000	J/mol	Ohmic overpotential at 1C activation energy
$J_{0,\text{ref}}$	0.1	-	Dimensionless charge exchange current pre-exponential factor

Ea_{J0}	-14000	J/mol	Dimensionless charge exchange current activation energy
Ea_{τ}	12000	J/mol	Diffusion time-constant activation energy
τ_{ref}	1000	s	Diffusion time-constant pre-exponential factor
SOC_{initial}	1	-	Initial state of charge
SOC_{final}	0.2	-	Final state of charge
h_{hs}	0.0044696	m	Thickness of the heat sink
$kT_{\text{batt,ang}}$	20	W/(m·K)	Axial cell thermal conductivity
$kT_{\text{batt,r}}$	3.4	W/(m·K)	Radial cell thermal conductivity
ρ_{cell}	2700	kg/m^3	Density of the cells
Cp_{batt}	1280	J/(kg·K)	Heat capacity of the cells
I_{app}	-10.8	A	Appied constant current for one cell

In order to explore the impact of the layout of battery packs on the overall heat dissipation at the system level, a single battery pack is first simplified as a cube of the same size to complete the related thermal simulation. As is shown in Fig 4.9, there are 5 different layouts for 20 battery packs. Generally, this is a top view of different layouts, each square represents a vertical column of battery packs, and the numbers marked on the square indicate the number of packs in one column. Air cooling, obviously, is to utilize the convection of working fluid to cool down the batteries. Therefore, each configuration is evaluated for two different airflow directions by setting the velocity field of fluid in the simulation, namely along the x-axis direction and along the y-axis direction. Most importantly, in order to capture the hysteresis of temperature changes, there is also a period of rest to allow the temperature of the battery pack to change sufficiently after the discharge from 100% SOC to 20% SOC.
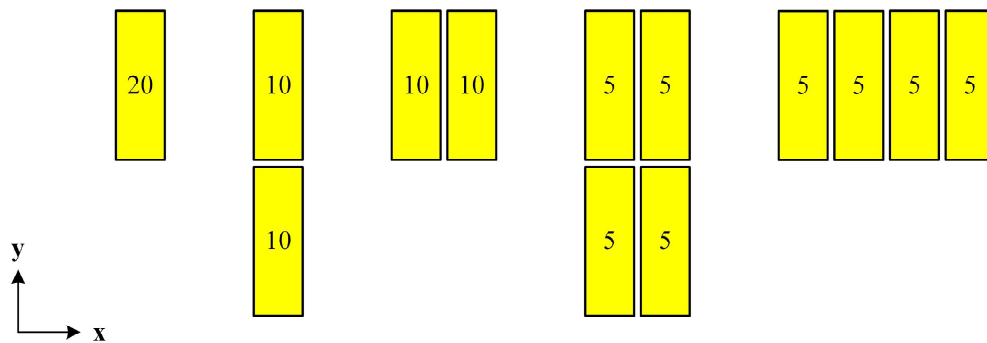
Figure 4.9: 5 different layouts of battery packs

(a) Temperature distribution

(b) Maximum temperature
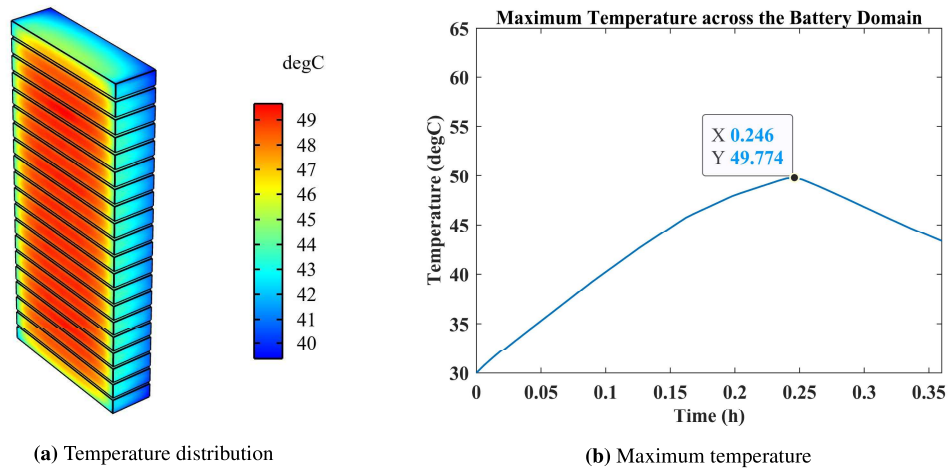
Figure 4.10: Air cooling in x-axis for Layout 1

(a) Temperature distribution

(b) Maximum temperature
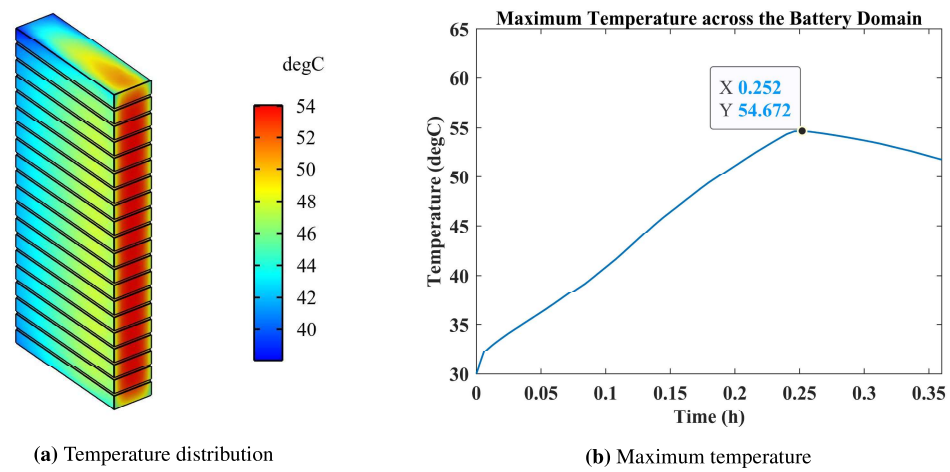
Figure 4.11: Air cooling in y-axis for Layout 1

(a) Temperature distribution

(b) Maximum temperature
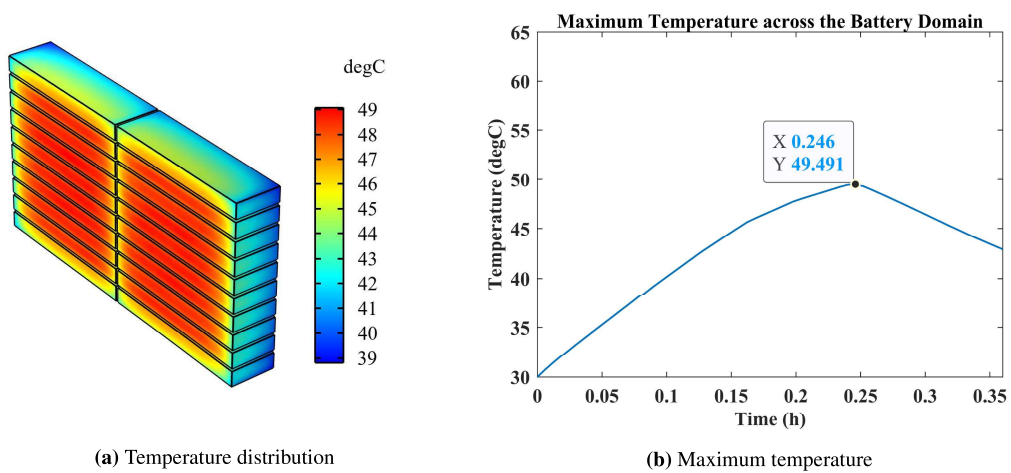
Figure 4.12: Air cooling in x-axis for Layout 2

(a) Temperature distribution

(b) Maximum temperature
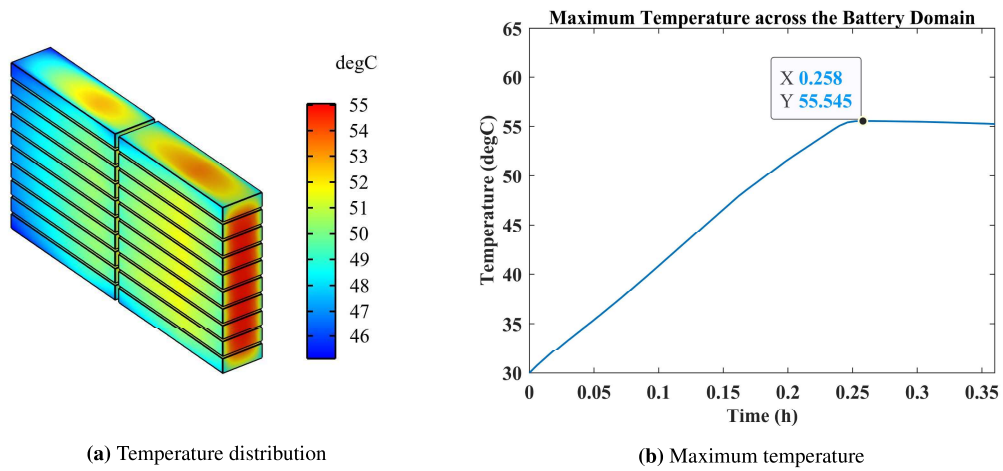
Figure 4.13: Air cooling in y-axis for Layout 2

(a) Temperature distribution

(b) Maximum temperature
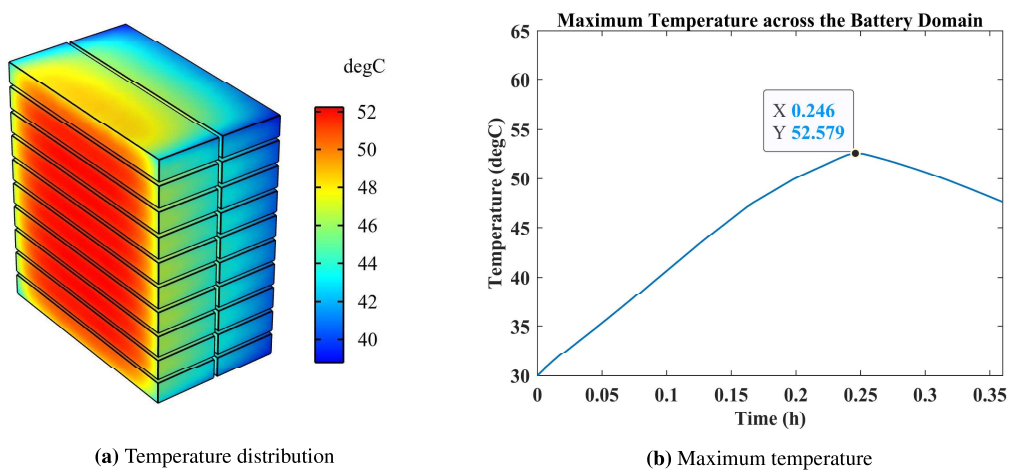
Figure 4.14: Air cooling in x-axis for Layout 3

(a) Temperature distribution

(b) Maximum temperature
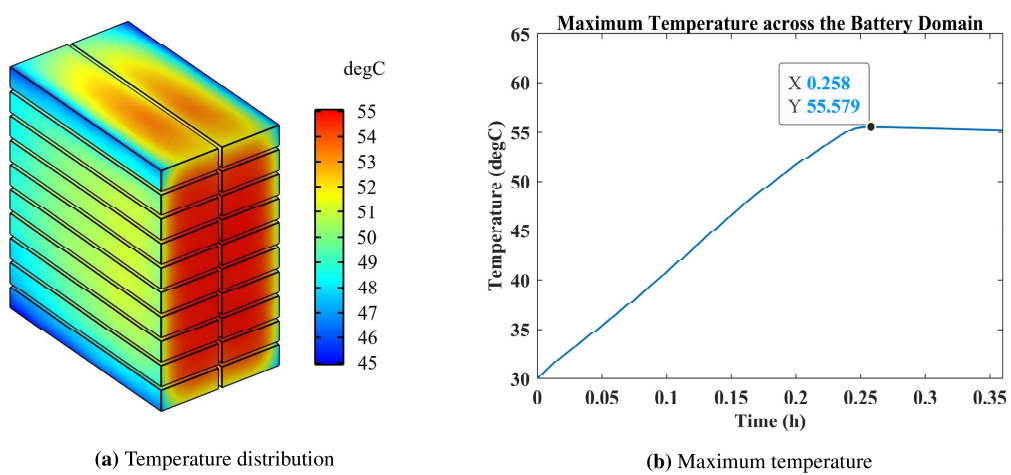
Figure 4.15: Air cooling in y-axis for Layout 3

(a) Temperature distribution

(b) Maximum temperature
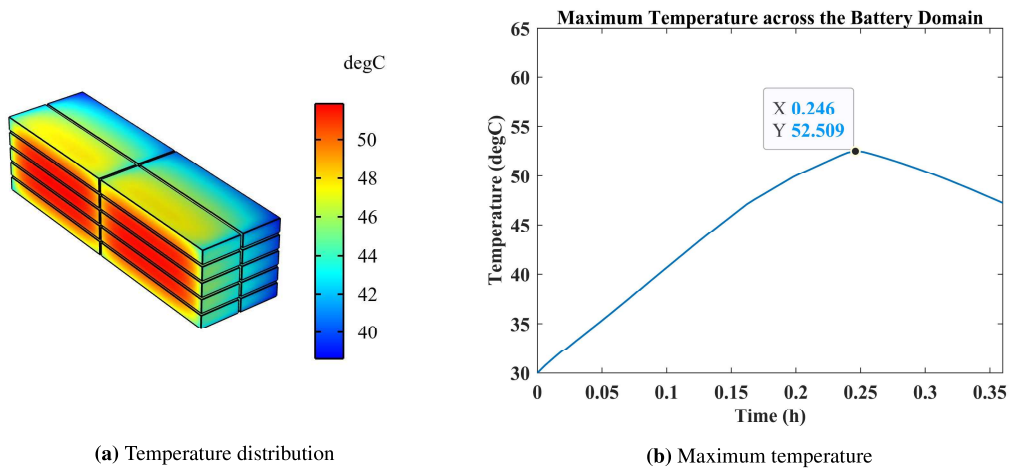
Figure 4.16: Air cooling in x-axis for Layout 4

(a) Temperature distribution

(b) Maximum temperature
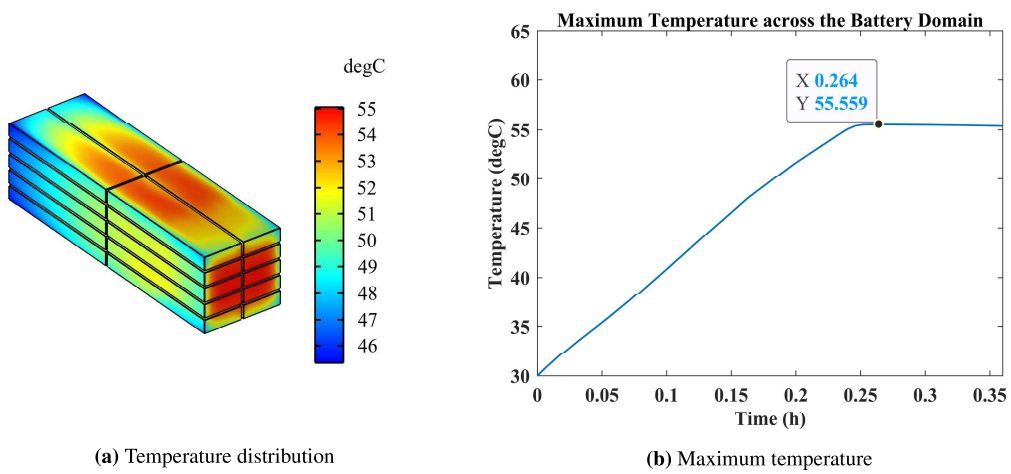
Figure 4.17: Air cooling in y-axis for Layout 4

(a) Temperature distribution

(b) Maximum temperature
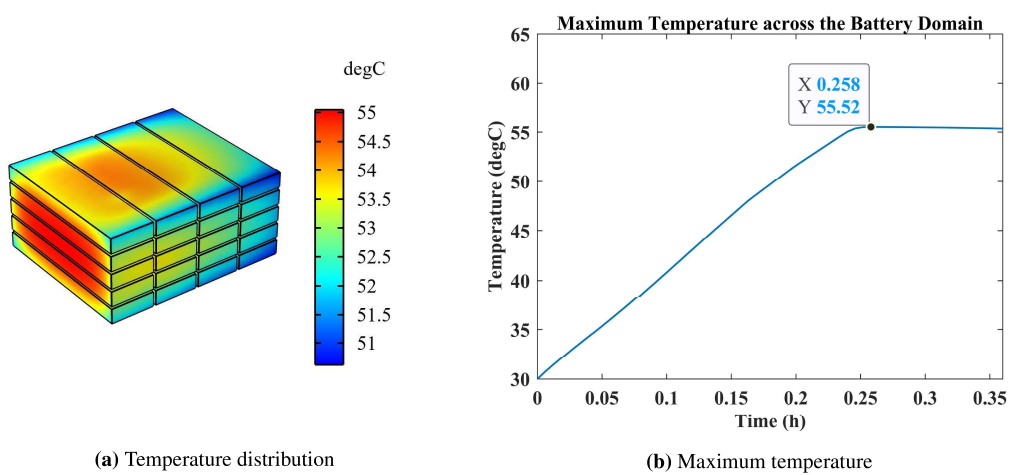
Figure 4.18: Air cooling in x-axis for Layout 5

(a) Temperature distribution   (b) Maximum temperature
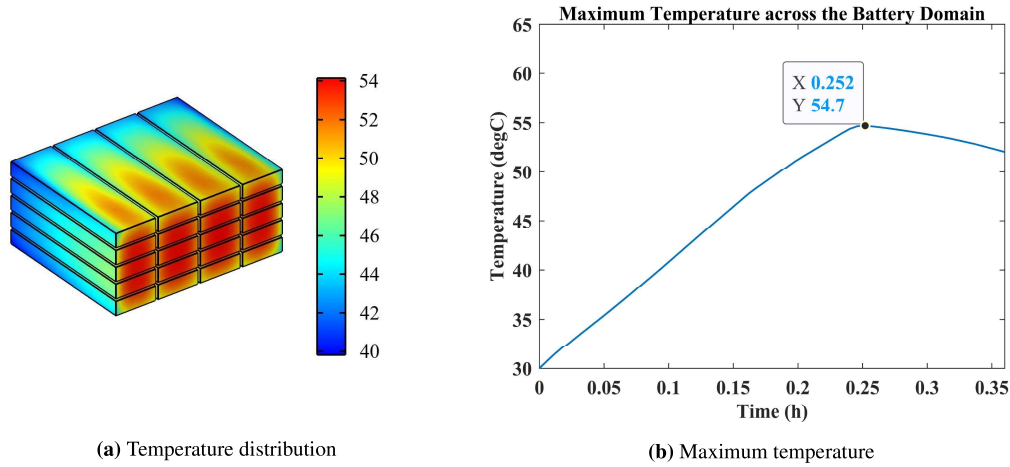
Figure 4.19: Air cooling in y-axis for Layout 5

The maximum temperature and the distribution of temperatures across all battery packs are shown in Fig 4.10 - Fig 4.19. At each setting, the maximum temperature of the battery pack keeps rising because the battery pack discharges at a constant current from 0 to 0.24h. On the other hand, after 0.24h, the battery pack stopped discharging, so the maximum temperature of the battery pack showed different levels of temperature drop due to airflow. From the results of the simulations, it is clear that the cooling for Layout 1 and 2 (especially using the airflow in the x-axis) has the best heat dissipation performance, and that the maximum temperature can be kept below $50°C$ even at the end of the discharge period. In addition, it can also be seen that the overall heat dissipation effect and the temperature distribution both improve when the airflow is directed to follow a path with a shorter geometric length.

After completing the investigation of the system-level battery pack layout and air cooling, the focus will return back to a single battery pack. In this section, Layout 1 will be selected as an example due to its superior cooling effect. According to Fig 4.7, the full-scale model of the target single pack will be included in the global model for simulation, meanwhile maintaining the same air cooling conditions. Because of the limitation of simulation time, this part only selects the global model consisting of 3, 5, and 7 packs, which are depicted in Fig 4.20. Finally, in Fig 4.21, as the number of packs contained in the global model increases, the maximum temperature of the target pack increases to a certain extent but is limited. Therefore, it can be inferred that the upper and lower two packs next to the target battery pack have the greatest influence on the maximum temperature of the target pack. Even if only these two packs are considered, it can significantly reflect the influence of the Global model on the target pack. In addition, it can be noticed that there is a certain difference between the absolute value of the maximum temperature of the target pack and the temperature shown in Fig 4.10, which is also in line with the prediction, because of the differences from details of geometry and specific heat capacity. The former simulation is more concerned with the comparison between the overall effect of heat dissipation, while the latter is more concerned with the details in one single battery pack.

(a) The full-scale model included in a global mode of 3.

(b) The temperature distribution in the full-scale model.

(c) The full-scale model included in a global model of 5.

(d) The full-scale model included in a global model of 7.
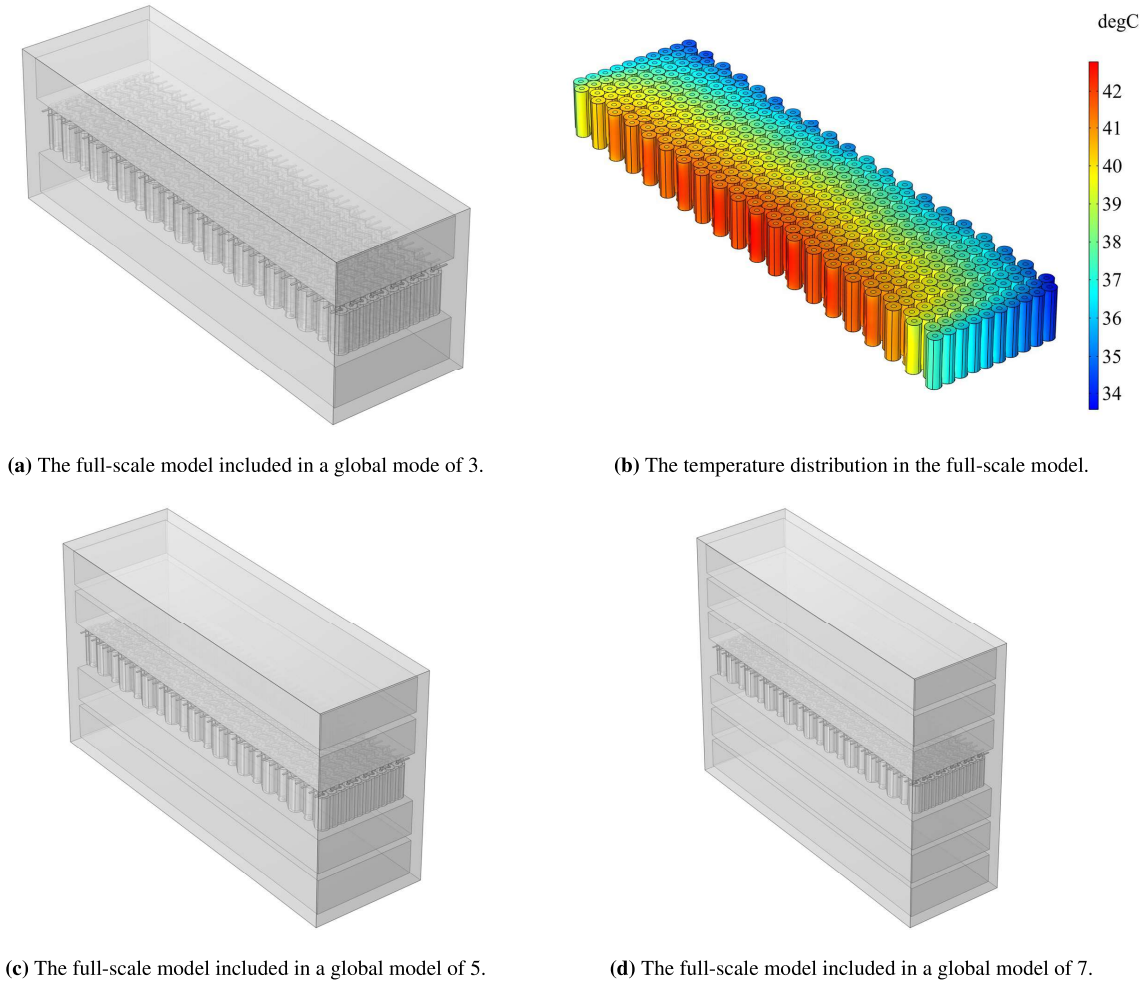
Figure 4.20: The full-scale model included in a global model of more packs.
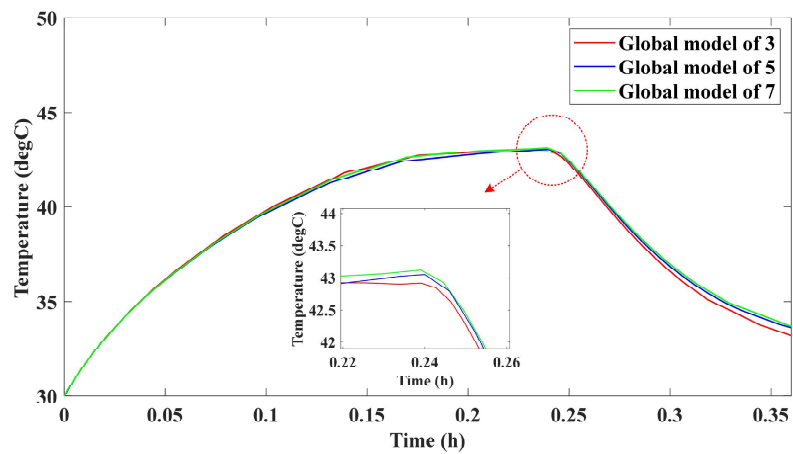

Figure 4.21: The maximum temperature for full-scale models included in a global mode of 3, 5 and 7 packs respectively

4.5. Interaction between the AC/DC PFC Converter and BESS

The DC fast charging station relies on three inputs — charging demand from EV load, battery status, and grid condition — to function appropriately. For charging demand, the settings in this system can be divided into 450kW demand from load in total or no load, which depends on whether there is an electric vehicle to charge. For battery status, the main consideration is the state of charge (SOC) of the battery. For example, if the battery depth of discharge (DoD) reaches a certain value, the DC bus voltage will not be able to be controlled within the required range, then the discharge of BESS will be stopped. Additionally, the total output power will also be reduced to the maximum output power of the grid side. On the contrary, if the SOC of the battery reaches 100%, it will stop charging the BESS. Furthermore, the primary consideration for the grid is the temporal unavailability of the grid. Based on the above description, the output of the system is also obvious, which is essentially the control and distribution of the grid-side and BESS-side power flow. The following diagram (Fig 4.22) summarizes the inputs and outputs of the system in light of the aforementioned factors.
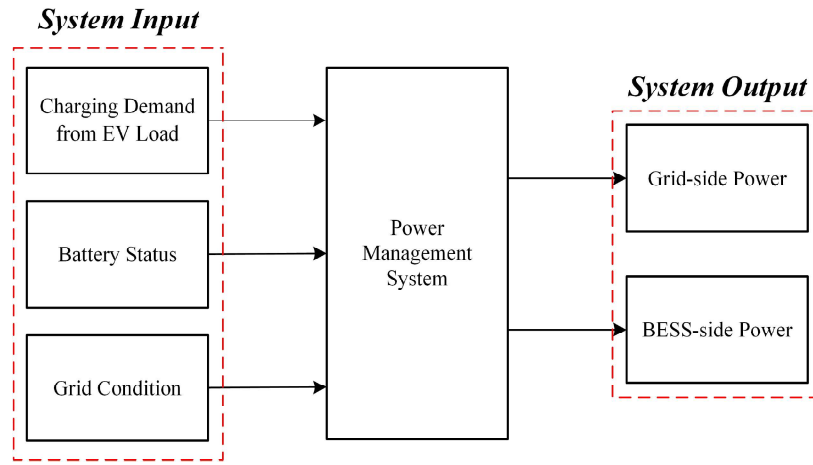
Figure 4.22: The inputs and outputs of the power management system for a DC fast charging station

In addition, for system integration and design, the interaction between the grid side and the BESS side needs to be considered:

1. First, as was previously indicated, the fluctuation range of the voltage level of the DC bus will be decided by the sizing and connection design. Additionally, the SOC of the BESS will have an impact on the DC bus voltage. In the case of SVPWM, the peak value of the grid-side phase voltage and the DC bus voltage should meet Eq 4.14, which means the DC bus voltage must be at least 565.6V to avoid over-modulation. This will ensure the 3-phase 3-level T-type converter continues to function normally.

$$V_{dc} \geq \frac{2V_{\mathrm{m}}}{M_{max}} \tag{4.14}$$

where V_{dc} is the DC bus voltage, V_{m} is the peak value of the grid-side phase voltage, and M_{max} is the maximum value of the modulation index, which is 1.15 for SVPWM in this case.

2. In terms of power flow distribution, the power provided by the grid side is set to 150kW, which is also due to the fact that the cost of providing access to the grid rises alongside the power level. As a result, 300kW of power will be supplied from the BESS side to the load to meet the power requirement. This in turn affects how the battery packs are connected inside the BESS.

3. In addition, system integration also affects the consideration of AC/DC converter selection. In conventional DC charging stations, there are typically two AC/DC converter selection options: unidirectional AC/DC converters (such as the Vienna rectifier) and bidirectional converters (such as the 3-phase 2-level converters, 3-phase 3-level NPC converters, and T-type converters). Considering the potential ancillary services supplied by Storage to Grid (S2G) or Vehicle to Grid (V2G), such as frequency regulation, reactive power support, voltage regulation, etc., the T-type converter with bidirectional power flow capability is utilized in this system.

<div style="text-align: right; font-size: 4em;">5</div>

Simulation and Experiment Validation

5.1. Simulation Validation

5.1.1. Three-Phase T-type Converter

This part of the simulation is to verify the modulation and control techniques for the three-phase T-type converter that were previously discussed, including the current loop control, the voltage loop control, and the midpoint balance control of the two capacitors. It should be noted that, the voltage loop control of the T-type converter will be removed in the subsequent system integration since the DC bus will be constrained by the terminal voltage of the BESS.

In general, to ensure the filtering performance of the LCL filter and minimize the stability problem brought on by harmonic pollution to a large extent, the parameters of the LCL filter ought to be determined based on the initial conditions, namely the RMS of fundamental line-to-line grid voltage U_{rms}, the rated active power of the converter P_n, the fundamental frequency of grid voltage f_{sw}, and the rated current of the converter f_0, etc. And the step-by-step design process could be followed as [77]:

1. Calculate the maximum total inductance $L_{T,max}$:

$$L_T \leq 10\% \frac{U_{rms}^2}{2\pi f_0 P_n} \tag{5.1}$$

2. Determine the minimum inductance on the converter side $L_{c,min}$:

$$L_1 \geq \frac{\sqrt{3}}{12} \frac{U_{dc}}{30\% I_{\text{rated}} f_{sw}} \tag{5.2}$$

3. Identify the maximum capacitor C_{max}:
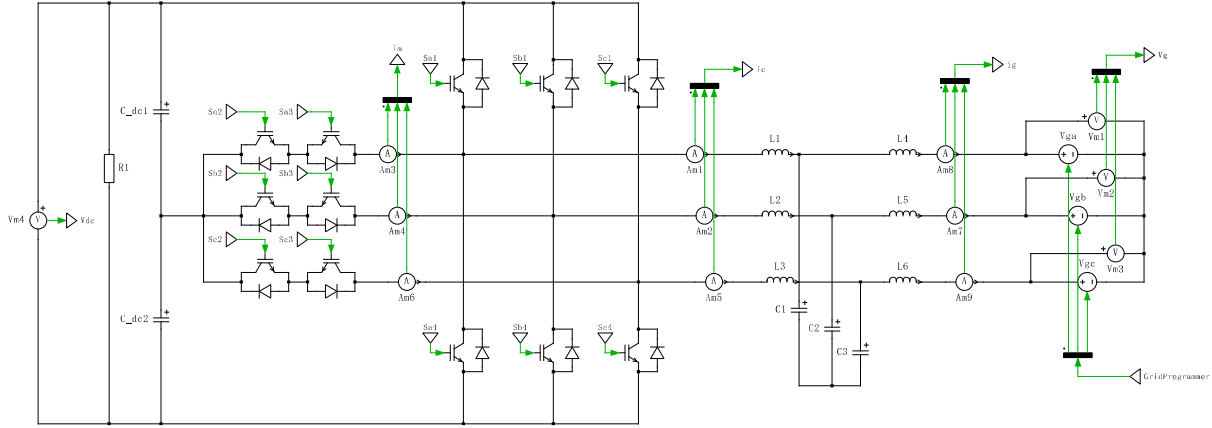
$$C < 5\% \frac{P_n}{2\pi f_0 U_{rms}^2} \tag{5.3}$$

4. Verify the resonance frequency f_r is within the reasonable range, typically between $10 f_0$ and $0.5 f_{sw}$.

$$2\pi f_r = \sqrt{(L_1 + L_2)/L_1 L_2 C} \tag{5.4}$$

After calculation, the relevant parameters are selected as shown in the Table 5.1:

Table 5.1: Parameter selection for the LCL filter

$L_1(\mu H)$	$L_2(\mu H)$	$C_f(\mu F)$	$C_{dc,1}(\mu F)$	$C_{dc,2}(\mu F)$
150	150	10	3000	3000

Figure 5.1: The simulation circuit of the three-phase T-type converter in PLECS (switched model)

Basically, there are two simulation models for converter, namely the switched model and the average model. On the one hand, the switched model provides detailed analysis of cycle to cycle variants in the circuits, which has advantages on transient analysis. On the other hand, the purpose of the average model is to provide less complexity and faster time domain simulation studies of converters by representing the switches using the average behaviour, while still maintaining sufficient converter dynamic accuracy. Therefore, the average model of three phase T-type converter is also developed for the simulation of subsequent system integration.
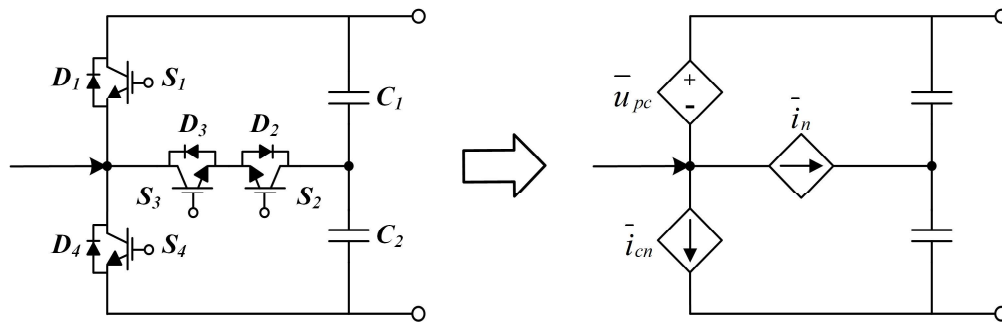
Figure 5.2: The average model of T-type converter in one phase

As is depicted in Fig 5.2, the average behaviour of switches in one phase of T-type converter can be substituted by one controlled voltage source and two controlled current sources [78]. u_{pc} is the voltage across the switch on the upper arm, i_{cn} is the current flowing through the switch on the lower arm, and i_n is the current on the middle arm. According to the description in Chapter 3, it can be known that there are only three switch states for the T-type converter, specifically P, O and N state. And the relation between the switch states and the value of u_{pc}, i_{cn} and i_n could be concluded as Table 5.2

Table 5.2: Current and voltage in different switch states

Switch states	i_{cn}	i_n	u_{pc}
P	0	0	0
O	0	i_o	$U_{dc}/2$
N	i_o	0	U_{dc}

Assume the duty of the switch states P, O and N are p_1, p_2 and p_3, then we have:

$$\begin{cases} \bar{i}_{cn} = p_3 \bar{i}_o \\ \bar{i}_n = p_2 \bar{i}_o \\ \bar{u}_{pc} = p_3 U_{dc} + p_2 U_{dc}/2 \end{cases} \tag{5.5}$$

And the there is a relation between the duty of the switch states p_1, p_2, p_3 and the duty of each single switch d_1, d_2, d_3, d_4.

$$\begin{cases} p_1 = d_1 \\ p_2 = d_2 - d_1 \\ p_3 = 1 - d_2 \end{cases} \tag{5.6}$$

Substituting 5.6 into 5.5, the controlled current source and voltage source can be derived as Fig 5.7. It is worth noting that, the expression of controlled sources only depends on the duty of S_1 and S_2.

$$\begin{cases} \bar{i}_{cn} = (1 - d_2) \bar{i}_o \\ \bar{i}_n = (d_2 - d_1) \bar{i}_o \\ \bar{u}_{pc} = (1 - d_2) U_{dc} + (d_2 - d_1) U_{dc}/2 \end{cases} \tag{5.7}$$
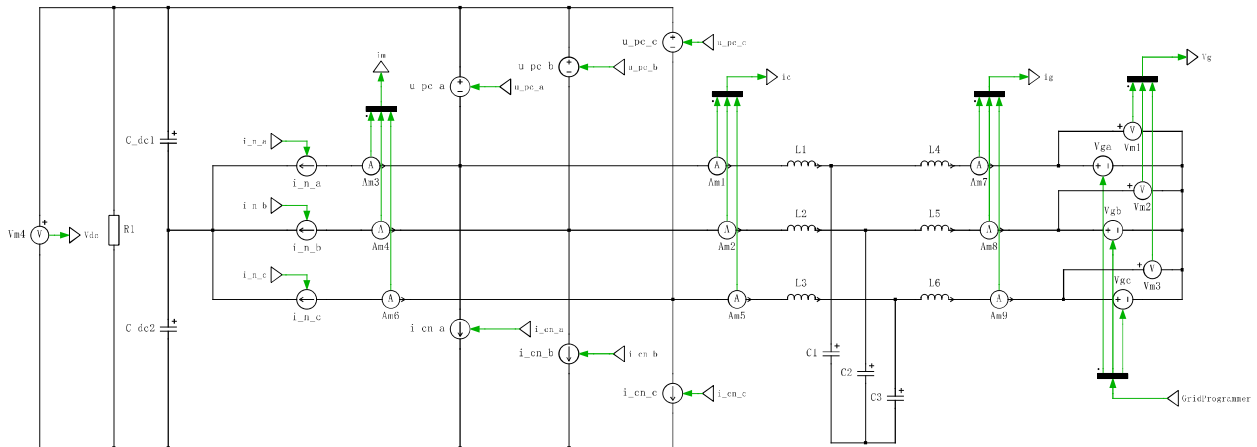
Figure 5.3: The simulation circuit of the three-phase T-type converter in PLECS (average model)

The results of the simulation are shown as follows:
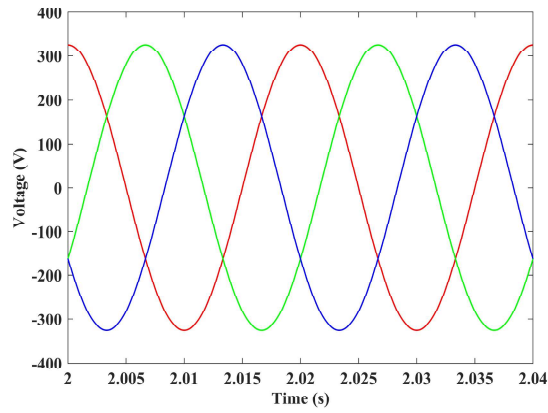
Figure 5.4: Three phase voltages of the grid
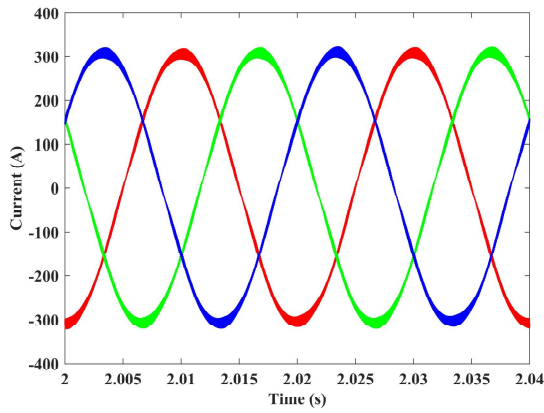
(a) Switching model
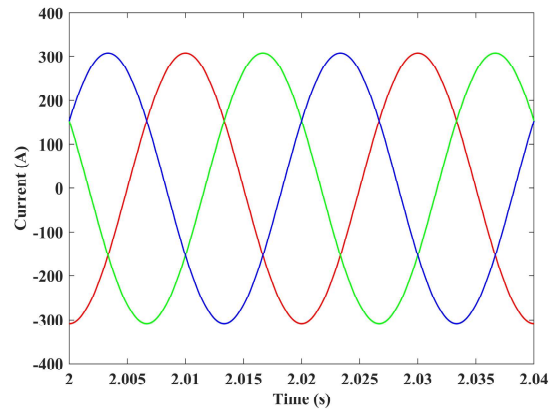
(b) Average model

Figure 5.5: The converter-side currents
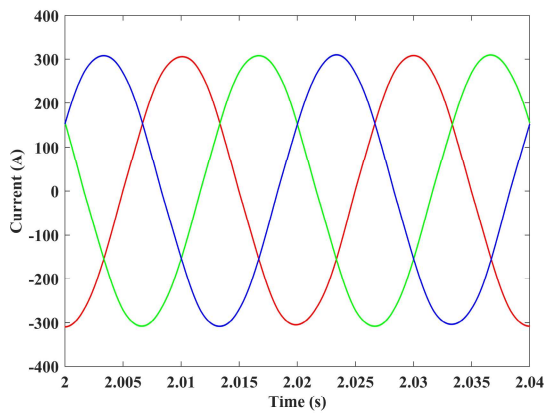
(a) Switching model
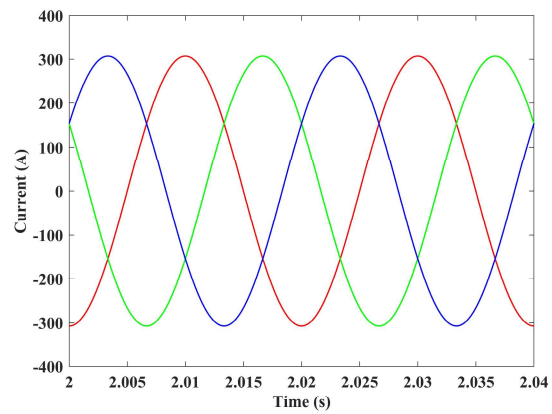
(b) Average model

Figure 5.6: The grid-side currents

(a) Switching model

(b) Average model
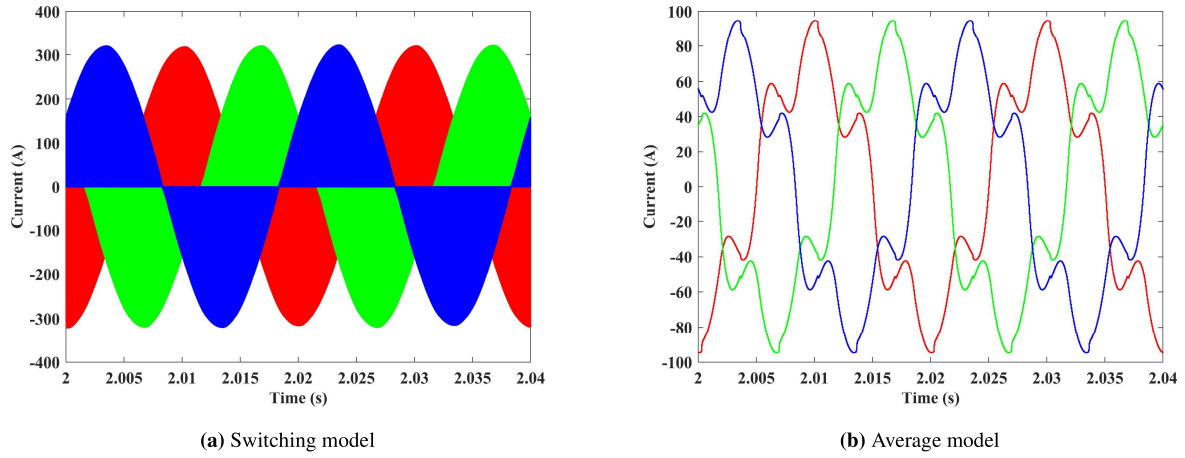
Figure 5.7: The middle leg currents

(a) Switching model

(b) Average model
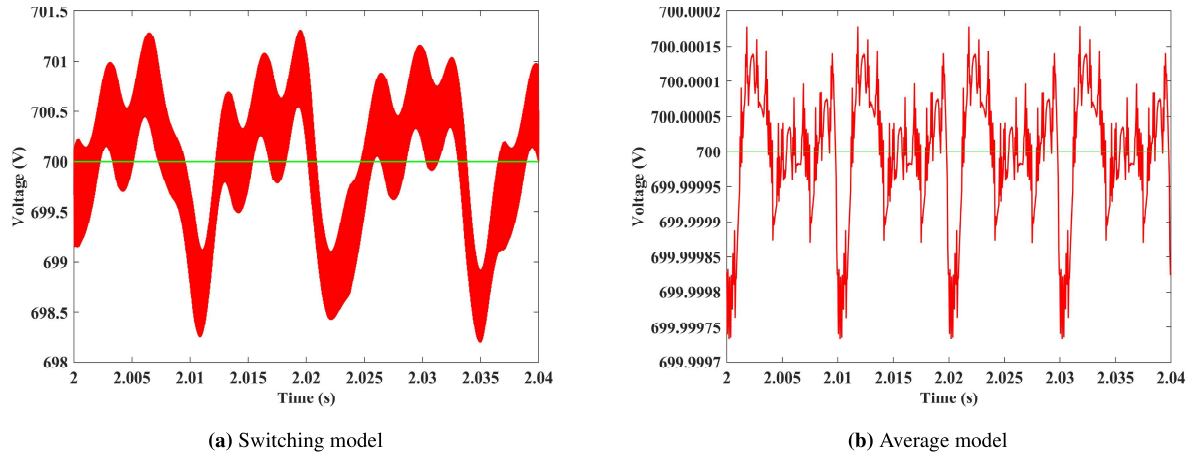
Figure 5.8: The DC bus voltage

(a) Switching model

(b) Average model
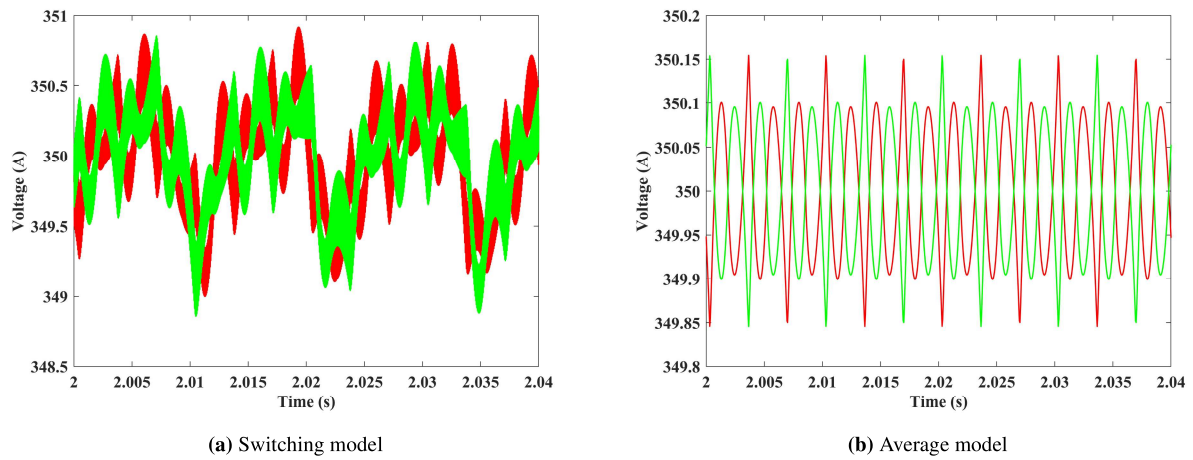
Figure 5.9: The voltages of two capacitors with the neutral point balance control

(a) Switching model
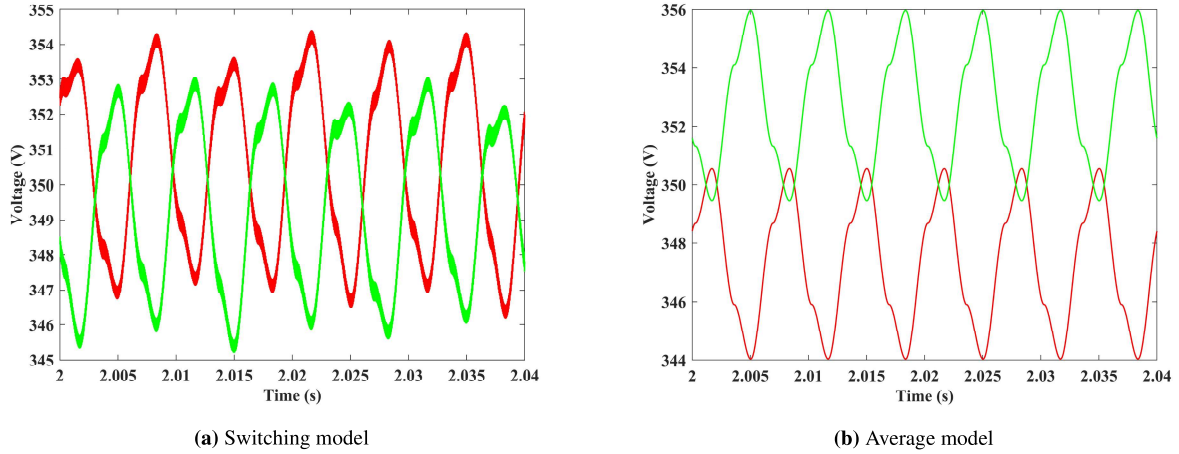
(b) Average model

Figure 5.10: The voltages of two capacitors without the neutral point balance control

(a) Switching model
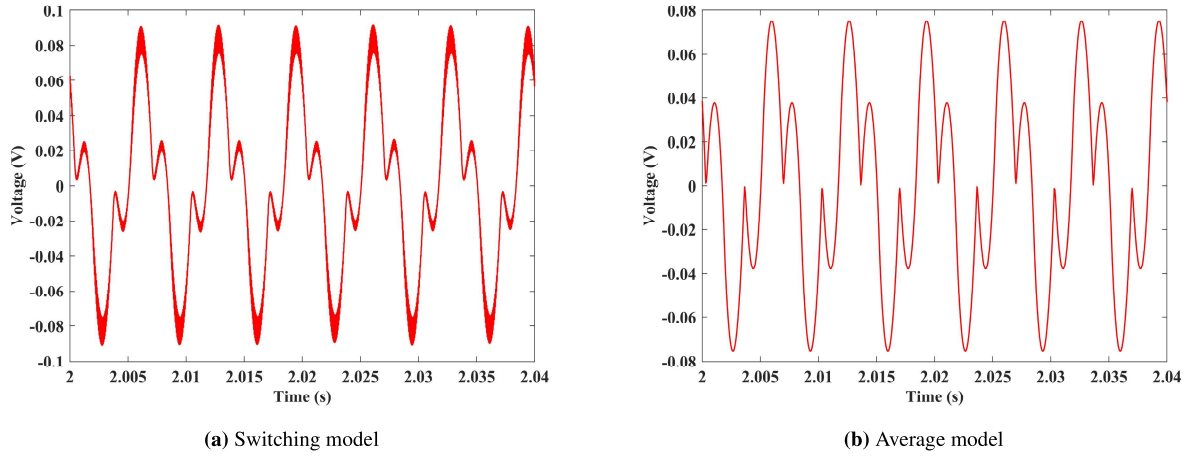
(b) Average model

Figure 5.11: The second zero sequence injected to the reference voltage

It can be seen from Fig 5.4-5.11 that, the average modeling method used realizes the unified modeling of three-phase T-type converters while maintaining the parameters set in the circuit including inductors, capacitors, resistors, and power supplies. Most importantly, it will provide a much faster time domain simulation when it comes to the system-level operation.

5.1.2. System Integration

In general, the simulation of the system integration is separated primarily into two parts, namely steady states and transitions. The fundamental classification criteria for steady states is the direction of power flow, and the details are shown in Table 5.3. For Steady State 1 (shown in Fig 5.12), the direction of power flow is from Grid to BESS, indicating that there is no charging demand on the load side and that the grid is charging the BESS. It is recommended that the total charging current for BESS be limited to 60A, based on the standard charging current of the aforementioned Samsung INR18650-30Q. Therefore, the overall charging power of the BESS will fluctuate as the SOC of the BESS itself varies. The power delivered by the BESS to the grid in Steady State 2 (shown in Fig 5.14) is determined by the rated power of the AC/DC converter linked to the grid, therefore, the maximum is 150kW. For Steady State 3 and

Steady State 4, there is a charging demand on the load side. Steady State 3 (shown in Fig 5.16) is a standard power charging mode, in which the grid and the BESS deliver a total power of 450kW to the load side. In comparison, considering that the grid may be unexpectedly unavailable in some circumstances, the BESS can also provide electricity to the load side alone. In other words, Steady State 4 (shown in Fig 5.18) is a lower power charging mode accomplished only by the BESS and outputs a total power of 300kW to the load side.

Table 5.3: Steady states for simulations of system integration

States	Staedy State 1	Staedy State 2	Staedy State 3	Staedy State 4
Direction of Power Flow	From Grid to BESS	From BESS to Grid	From Grid and BESS to Load	From BESS to Load
Output Power of Grid Side (kW)	40-50	-150	150	0
Output Power of BESS Side (kW)	40-50	150	300	300
Total Output Power of Load Side (kW)	0	0	450	300

In the simulation via PLECS, the T-type converter is selected as the validated average model and the aforementioned 3 RC link model of the Li-ion battery serves as the BESS. Considering the connection of the battery cells, the number of series connections and parallel connections are inherited from the previous design, which is 200 and 40 respectively. Since the focus of this design is on the front end rather than the back end of the DC fast charging station, the load side is simplified as a current source in the simulation to provide a constant power demand when necessary. In order to investigate the system integration under different SOC conditions of the BESS, three representative operating points of 20% SOC, 50% SOC and 80% SOC are selected.
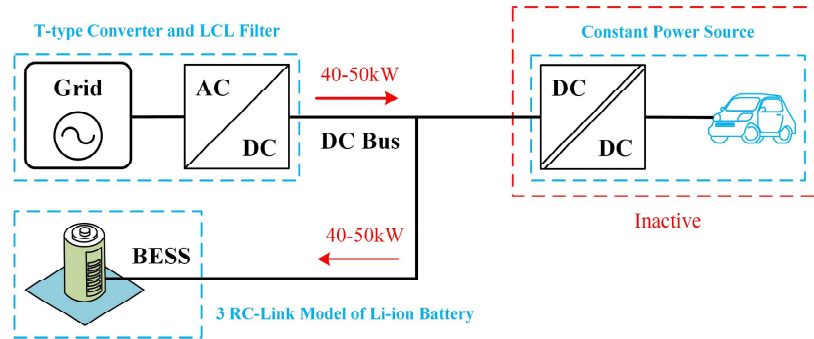
Figure 5.12: The schematic diagram of Steady State 1

Table 5.4: Simulation results of Steady State 1

	$I_{\text{PFC}}(A)$	$I_{\text{BESS}}(A)$	$I_{\text{Load}}(A)$	$P_{\text{PFC}}(W)$	$P_{\text{BESS}}(W)$	$P_{\text{Load}}(W)$	$V_{\text{dc}}(V)$
20% SOC	59.99	-59.99	0	43257.7	-43257.7	0	721.08
50% SOC	59.99	-59.99	0	44645.1	-44645.1	0	744.18
80% SOC	59.99	-59.99	0	47306.0	-47306.0	0	788.47

The simulation results of Steady State 1 are shown in Table 5.4 and Fig 5.13. I_{PFC}, I_{BESS}, and I_{Load} represent the DC current flow on the PFC converter, BESS, and load branches, meanwhile, P_{PFC}, P_{BESS}, and P_{Load} represent the Power Flow on the three branches, respectively. In order to distinguish the flow direction, both the current and power are configured based on the principle that the output is positive and the input is negative on each branch. It can

be observed that, in Steady State 1, since the charging current from the grid to the BESS is limited to the standard charging current, the charging power fluctuates between 43-47kW as the DC bus voltage changes, which is the same as expected. In addition, because the T-type converter selected in the simulation is the average model, the grid-side current and the converter-side current are identical, only the grid-side current is represented in Fig 5.13.
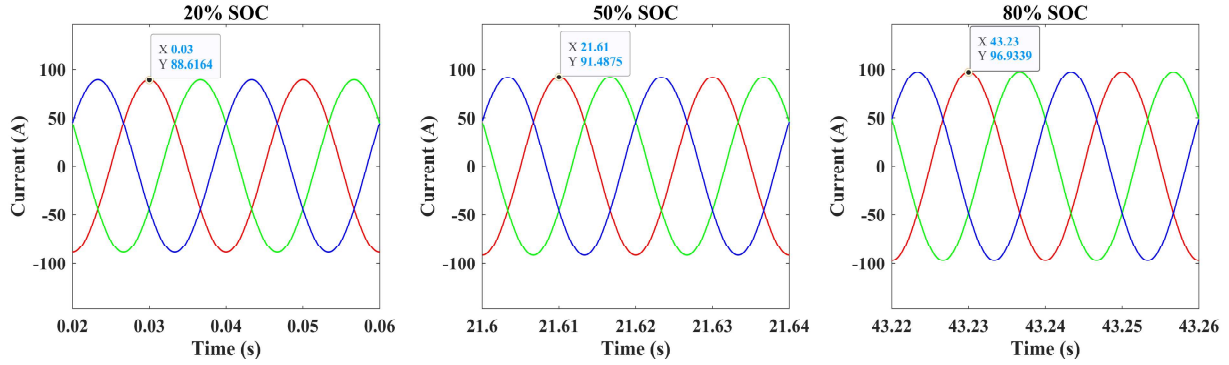
Figure 5.13: Grid-side current for the PFC converter during Steady State 1

The simulation results of Steady State 2 are shown in Table 5.5 and Fig 5.15. In Steady State 2, the power delivered by the BESS to the grid in Steady State 2 is limited by the T-type converter linked to the grid, which is 150kW. Besides, as the BESS feeds power back to the grid, the SOC and the terminal voltage of the BESS decrease accordingly. Therefore, as the DC bus voltage of the system drops, the DC current on the branch of the T-type converter will increase in order to keep the power constant. However, the grid-side current will not be affected because the power level supplied by the grid remains the same. The two steady states simulated above are both the power exchange between the power grid and the BESS without the EV load, thus the bidirectional power flow capability of the system is validated.
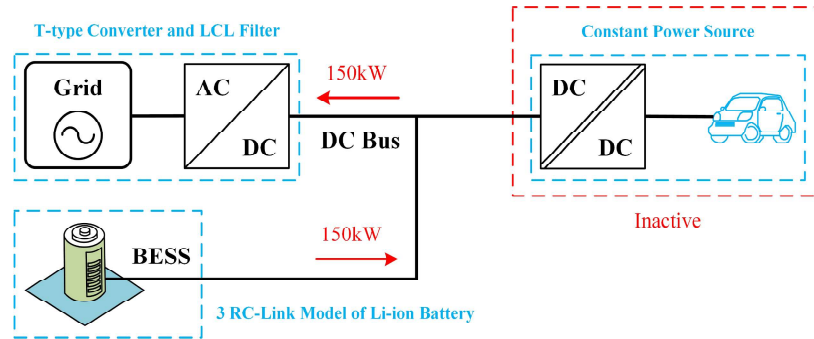
Figure 5.14: The schematic diagram of steady state 2

Table 5.5: Simulation results of Steady State 2

|	$I_{\text{PFC}}(A)$	$I_{\text{BESS}}(A)$	$I_{\text{Load}}(A)$	$P_{\text{PFC}}(W)$	$P_{\text{BESS}}(W)$	$P_{\text{Load}}(W)$	$V_{\text{dc}}(V)$
20%SOC	-214.92	214.92	0	-149954	149954	0	697.73
50%SOC	-207.88	207.88	0	-149953	149953	0	721.34
80%SOC	-195.58	195.58	0	-149951	149951	0	766.68
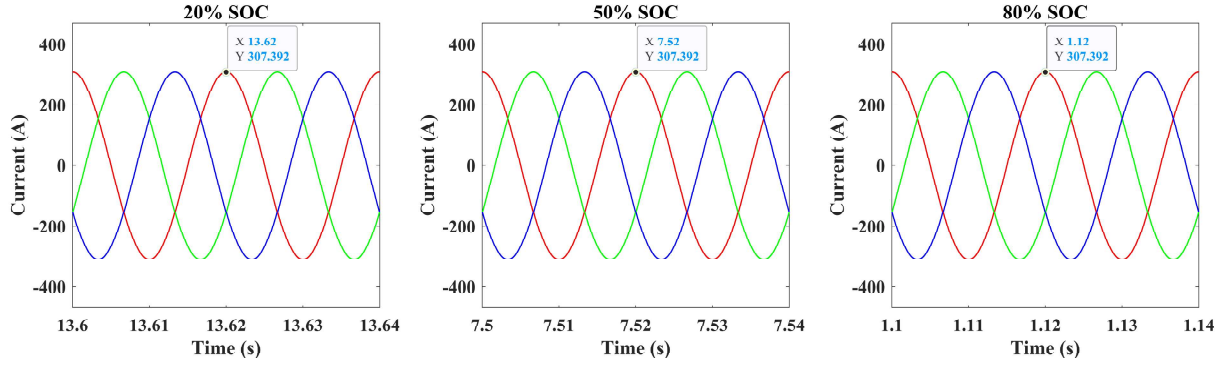
Figure 5.15: Grid-side current for the PFC converter during steady state 2

The simulation results of Steady State 3 are shown in Table 5.6 and Fig 5.17. As mentioned previously, in Steady State 3, the entire system will charge the EV in standard charging power mode at the load side. The grid and BESS will provide 150kW and 300kW of power respectively. Similar to Steady State 2, it is apparent that as the charging process progresses and the SOC of BESS decreases, the terminal voltage of the BESS inevitably decreases. Therefore, the DC current output by the T-type converter will also increase. When it comes to Steady State 4, as a lower charging power mode, the load side will receive 300kW power provided by BESS alone, as shown in Table 5.7. In fact, for the design of the BESS, a SOC greater than 20% is taken as a prerequisite. Hence, when the SOC of the BESS is less than 20%, it is not recommended to enter Steady State 2, Steady State 3 and Steady State 4. Otherwise, it will cause the over-modulation of the AC/DC PFC converter.
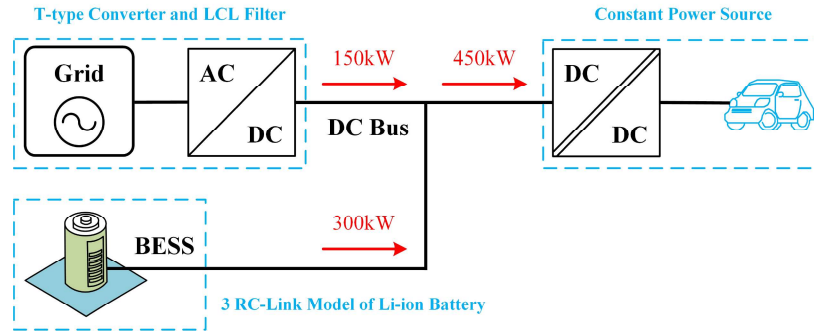
Figure 5.16: The schematic diagram of steady state 3

Table 5.6: Simulation results of Steady State 3

	$I_{\text{PFC}}(A)$	$I_{\text{BESS}}(A)$	$I_{\text{Load}}(A)$	$P_{\text{PFC}}(W)$	$P_{\text{BESS}}(W)$	$P_{\text{Load}}(W)$	$V_{\text{dc}}(V)$
20%SOC	221.11	442.20	663.31	150003	299997	450000	678.41
50%SOC	213.45	426.88	640.33	150004	299996	450000	702.76
80%SOC	200.22	400.40	600.62	150008	299992	450000	749.23

Figure 5.17: Grid-side current for the PFC converter during steady state 3

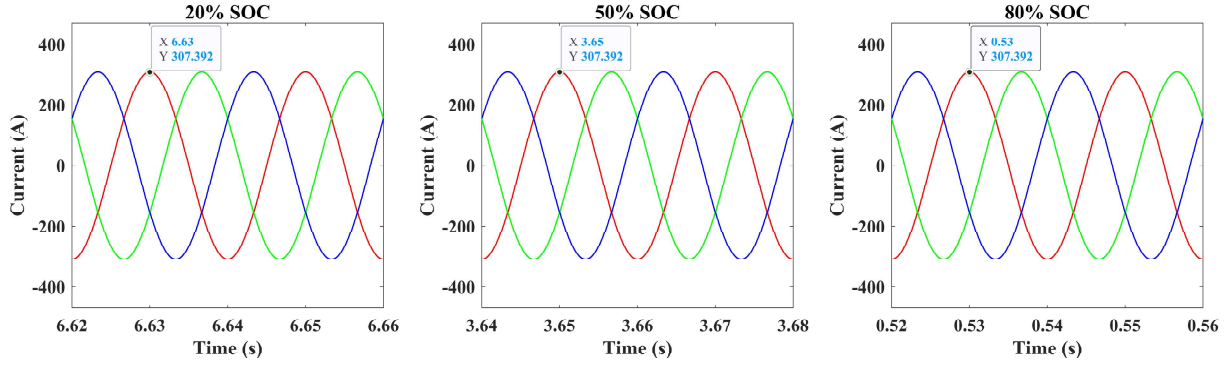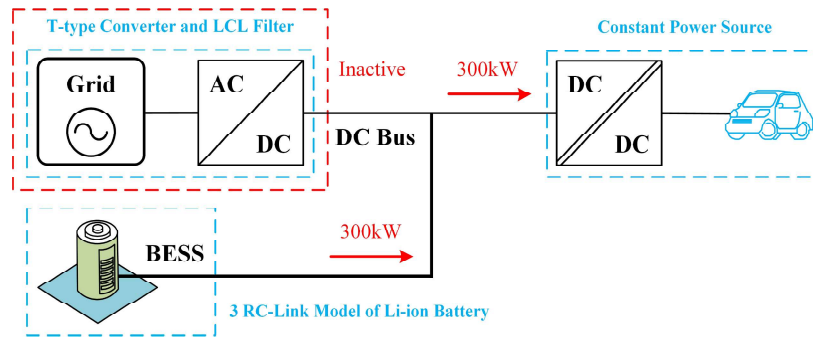**Figure 5.18:** The schematic diagram of steady state 4

Table 5.7: Simulation results of Steady State 4

	$I_{\text{PFC}}(A)$	$I_{\text{BESS}}(A)$	$I_{\text{Load}}(A)$	$P_{\text{PFC}}(W)$	$P_{\text{BESS}}(W)$	$P_{\text{Load}}(W)$	$V_{\text{dc}}(V)$
20%SOC	0.0043	442.20	442.20	2.90	299997	300000	678.41
50%SOC	0.0062	426.89	426.90	4.30	299996	300000	702.76
80%SOC	0.0105	400.41	400.41	7.80	299992	300000	749.24

Based on an assessment of the actual circumstances, there are primarily two situations for transitions in this simulation. The first transition to consider is from Steady State 1 to Steady State 3. This transition describes the case when the grid charges the BESS while no charging demand comes from the load side, and then the grid and BESS jointly charge the EV in the standard power charging mode when the charging demand arrives at a specific time. Another scenario to consider is the transition from Steady State 4 to Steady State 3. In this case, the grid is unavailable during the initial phase, so the EV can only be charged in the lower power mode by the BESS alone. The grid then becomes available at a particular time, at which point the grid and BESS begin to charge the EV simultaneously in the standard power charging mode.

The simulation results of Transition 1 are shown in Fig 5.19. In this simulation, it is set that before 3.6s, the grid will charge the BESS. Immediately afterward, there will be a charging demand on the load side at 3.6s, and the grid and BESS will provide 450kW of power to the load jointly. It should be noted that, in order to select a representative situation, when Transition 1 occurs, the SOC of the BESS is at 50%. First of all, it can be observed that, with sudden variations in power demand, the currents on the three branches would also shift abruptly. In addition, due to the change in the current flowing through the BESS, the divided voltage on the equivalent circuit model inside the BESS

will inevitably change, thereby affecting the DC bus voltage. However, it can be found that at the moment when Transition 1 occurs, the DC bus voltage drops from 745V to around 700V, which does not impair the normal operation of the T-type converter with the proper control and modulation method. And this is also confirmed by the simulation result of the grid-side current of the T-type converter.
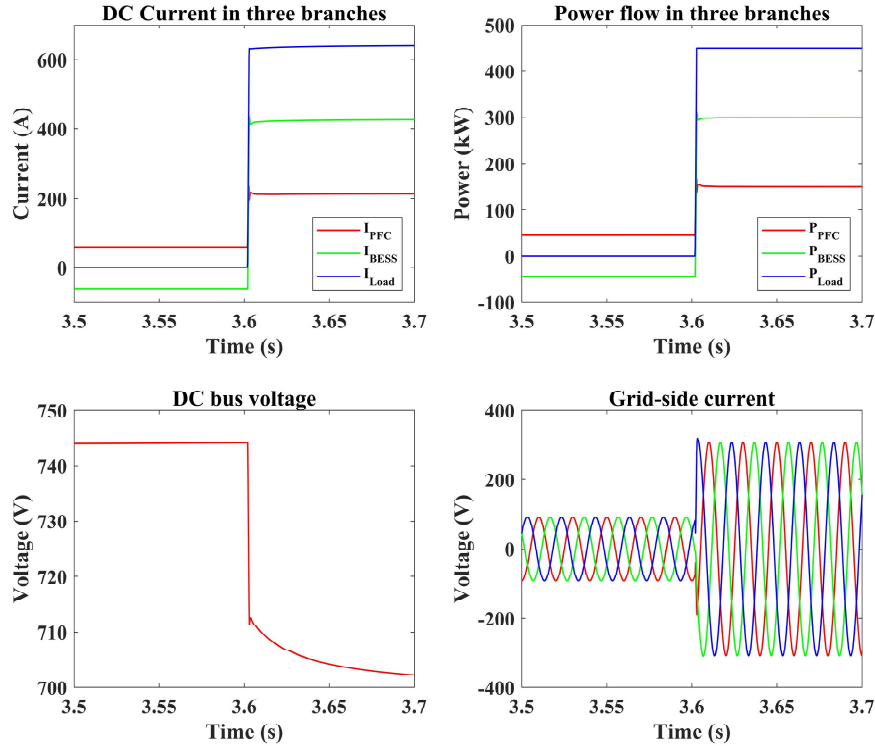

Figure 5.19: The simulation results of transition 1

The simulation results of Transition 2 are shown in Fig 5.20. In this simulation, Transition 2 is divided into two steps: Initially, when the power grid recovers from an unavailable state to a usable state, the charging power under the previous lower charging power mode is maintained and is equally divided by the grid and BESS, that is, 150kW of power is provided to the load side respectively. Subsequently, the charging power is converted from lower charging power mode to standard charging power mode. The power supplied by BESS rises from 150kW to 300kW while the power supplied by the grid remains constant at 150kW, allowing the system to switch from Steady State 4 to Steady State 3. To maintain consistency with Transition 1, the moment when Transition 2 occurs is still set at the situation when the SOC of the BESS is around 50%. Similar to Transition 1, when the power supplied to the load side changes, the current on the three branches also changes, which is in line with expectations. It is important to note that during the first step of Transition 2, the DC bus voltage climbs from 705V to about 720V, and then decreases back to 705V during the second step of Transition 2. This is still due to the change in the divided voltage caused by the current change on the BESS branch. Nonetheless, the simulation result for the grid-side current of the T-type converter indicates that this is an acceptable range for normal operation.

For Transition 1 and Transition 2, since they are both transitions to the standard charging power mode, there are some common prerequisites. The first one is that the SOC of the BESS should be under an appropriate state (at least higher than 20% in this case). Otherwise, it will not be suitable for charging the load. Additionally, the power grid must be in an appropriate state, meaning that its frequency and voltage must be maintained within a particular range. In other words, it is in an available state. As a comparison of the two transitions, the difference is that the former is triggered by the appearance of power demand at the load side, whereas the latter is triggered by a change in grid
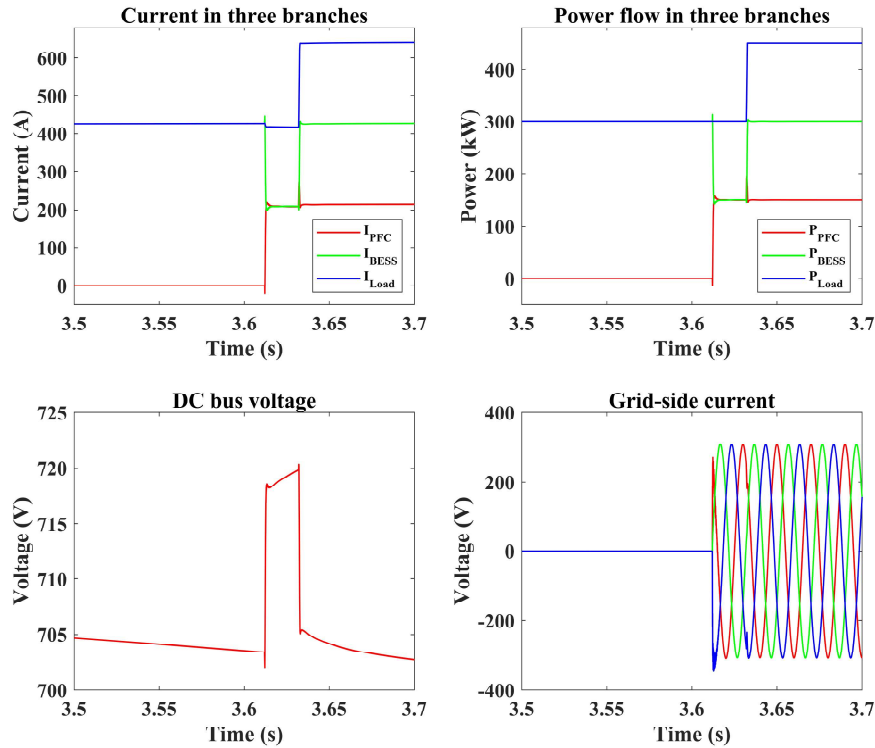
availability.

Figure 5.20: The simulation results of transition 2

5.2. Experiment Validation

For the purpose of validating the proposed system structure and operating modes provided in the simulation section, the experiment setup is depicted in Fig 5.22. In this experiment setup, the Cinergia Grid Emulator is linked to the three-phase damping resistor on the grid branch. Besides, due to power level restrictions, the power rating is chosen as 2kw instead of 150kW for the existing 3-phase 3-level T-type converter prototype in the laboratory. And the digital signal processor (DSP)-TMS320F28379D is used to send signals to the gate drivers of the T-type converter. For the BESS branch, the Cinergia Battery Emulator was chosen as a substitute for a real battery pack. The mathematical model is stored and executed in the firmware of the DSP in Cinergia equipment to ensure accurate and deterministic behavior, but the model cannot be changed. The user can emulate different batteries by adjusting the parameters of the model in the interface. Similar to the PFC branch, the maximum output power of the BESS is also reduced to about 4kW instead of 300kW in the experiment. For the load branch, the DELTA Electronika SM1500-CP-30 bi-directional power supply is selected to act as a constant current source. In order to ensure the recording of experimental data and waveform, the YOKOGAWA DLM4058 mixed signal oscilloscope and Fluke 289 digital multimeter are also used in the experiment. The experiment setup schematic is depicted in Fig 5.21. It should be noticed that all these power supplies share the same input source from the mains in the ESP lab, but both DELTA and Cinergia have isolation internally.

Comparable to the simulation section, the experimental verification of system integration continues to be divided into two sections, namely steady states and transitions. In terms of experimental operation, both Steady State 1 and 2 were conducted with the DELTA power supply turned off. The only difference lies in the positive and negative of the grid-side reference current of the current loop control for the T-type converter, which is reflected in the direction of power flow. The experiment results of Steady State 1 and 2 are shown in Fig 5.23. In the experiment, measurement

values are as follows: DC bus voltage V_{dc}, grid-side line voltage V_{ab}, grid-side current for T-type converter I_{ga}, converter-side current for T-type converter I_{ca}, and the DC currents on three branches I_{PFC}, I_{BESS}, I_{Load}. For measurement of DC current, still, the direction from current branch to other branches is defined as positive and vice versa. In Steady State 1, at three different operating points, the power output on the PFC branch is calculated to be 1777.88W, 1771.14W, and 1753.57W, respectively, based on the measurement results. In contrast, in Steady State 2, at the corresponding operating point, the PFC branch absorbs 2153.97W, 2155.24W, and 2163.98W accordingly. The difference in power between the two steady states is due to the fact that the control of the grid-side reference current, namely the current loop control for the T-type converter is essentially the control of the output or absorption power of the grid emulator in the experiment. In Steady State 1, the output power of the grid emulator is set to 2kW, however a portion of the output power is consumed by the 3-phase damping resistors, therefore, the measured output power on the PFC branch will be lower than the set value. Likewise, in Steady State 2, the grid emulator absorbs power is set to 2kW, but the BESS will deliver more than 2kW of power to cover its internal loss.
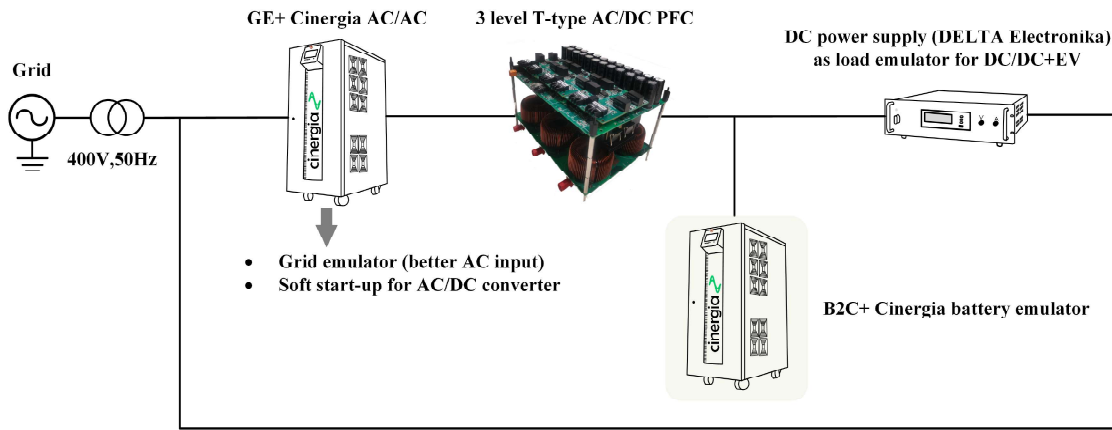
Figure 5.21: Experiment setup schematic
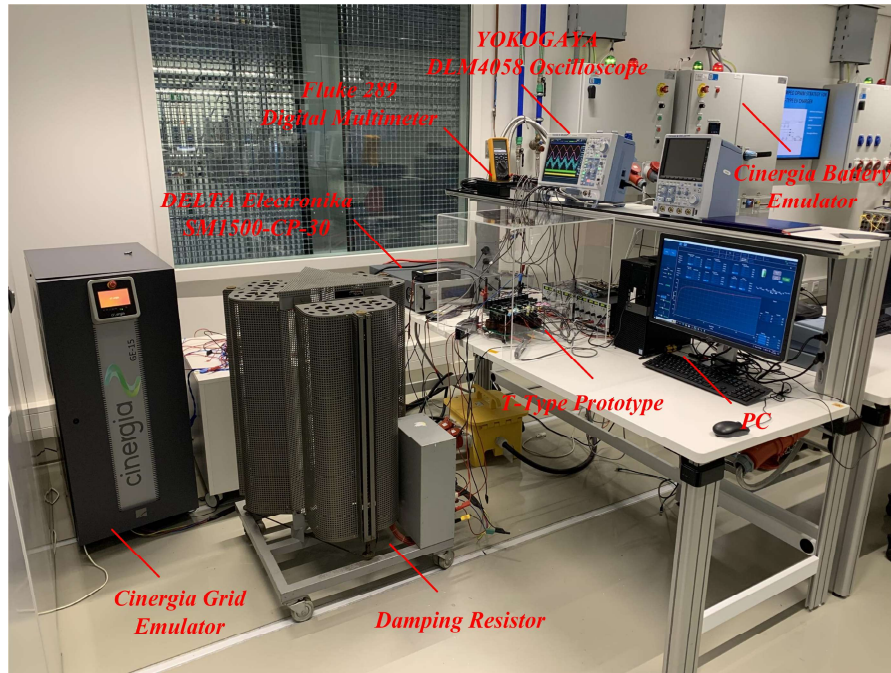
Figure 5.22: Experiment setup
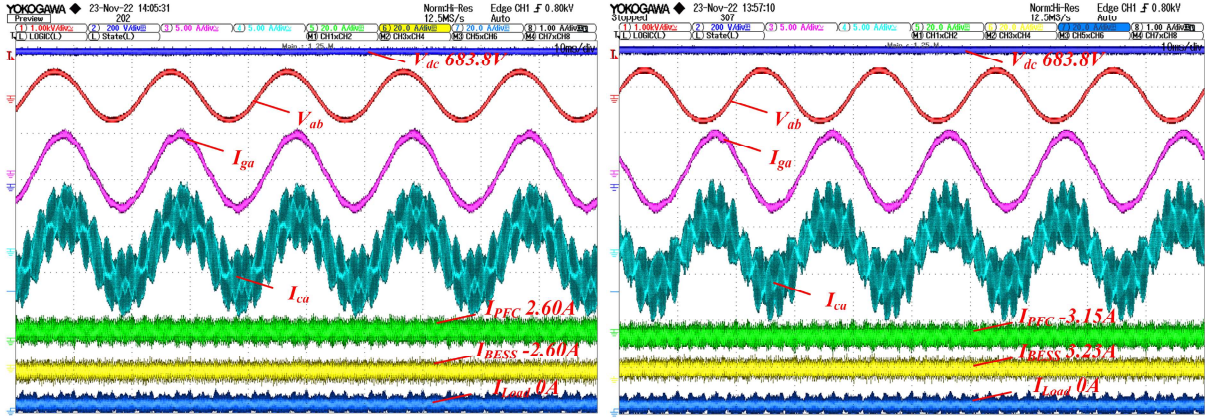
(a) Experiment results of Steady State 1 when the SOC of BESS is 20%

(b) Experiment results of Steady State 2 when the SOC of BESS is 20%
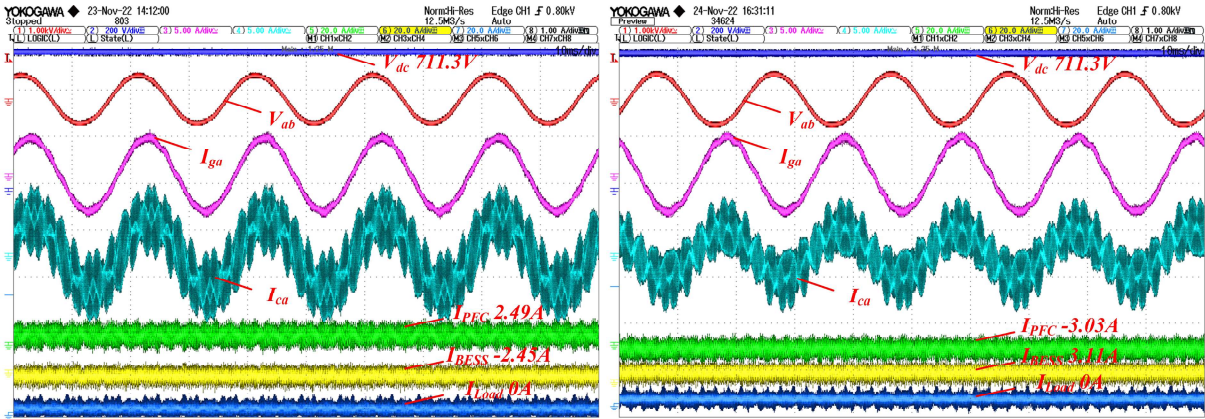
(c) Experiment results of Steady State 1 when the SOC of BESS is 50%

(d) Experiment results of Steady State 2 when the SOC of BESS is 50%
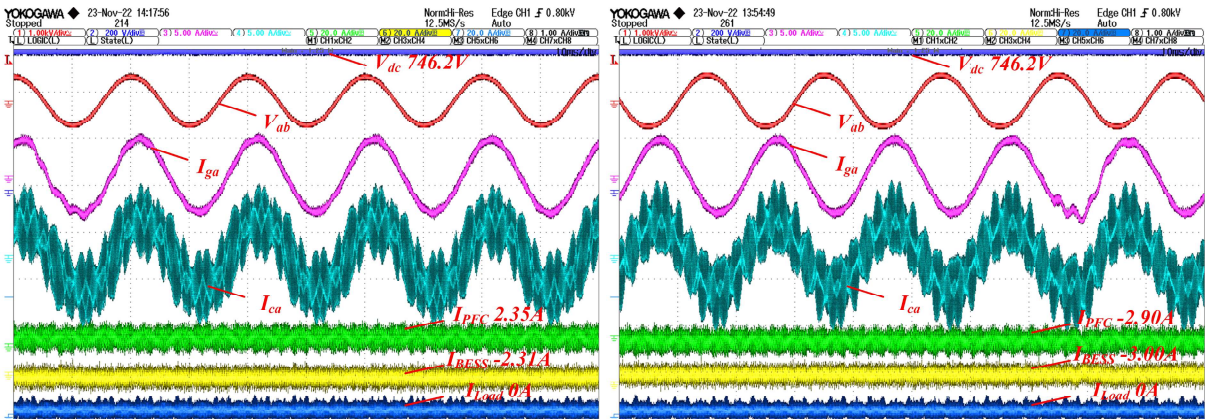
(e) Experiment results of Steady State 1 when the SOC of BESS is 80%

(f) Experiment results of Steady State 2 when the SOC of BESS is 80%

Figure 5.23: Experiment results of Steady State 1 and 2 in case of BESS under different SOC
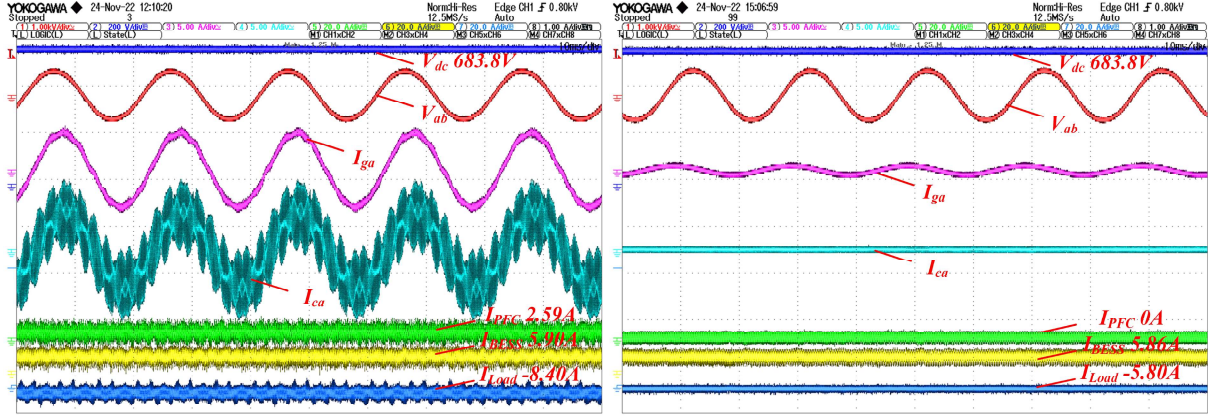
(a) Experiment results of Steady State 3 when the SOC of BESS is 20%

(b) Experiment results of Steady State 4 when the SOC of BESS is 20%
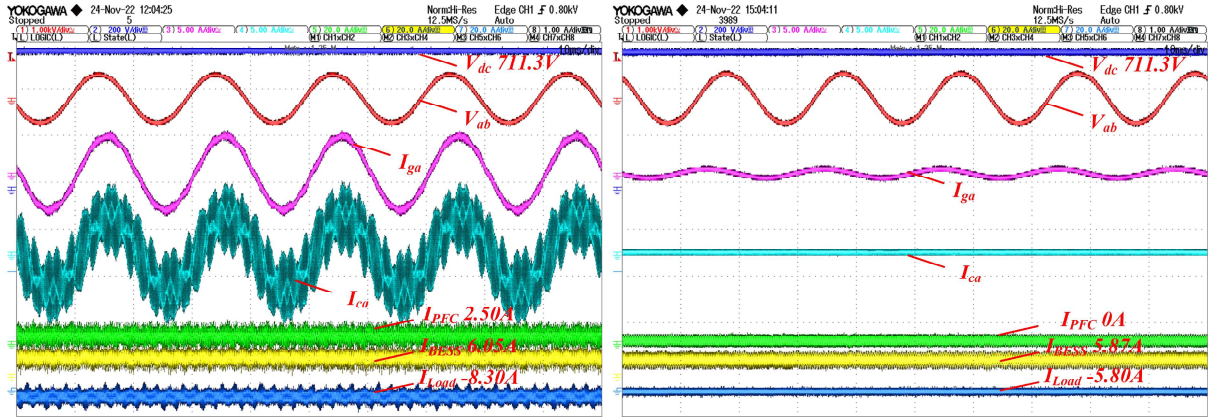
(c) Experiment results of Steady State 3 when the SOC of BESS is 50%

(d) Experiment results of Steady State 4 when the SOC of BESS is 50%

(e) Experiment results of Steady State 3 when the SOC of BESS is 80%

(f) Experiment results of Steady State 4 when the SOC of BESS is 80%

Figure 5.24: Experiment results of steady state 3 and 4 in case of BESS under different SOC
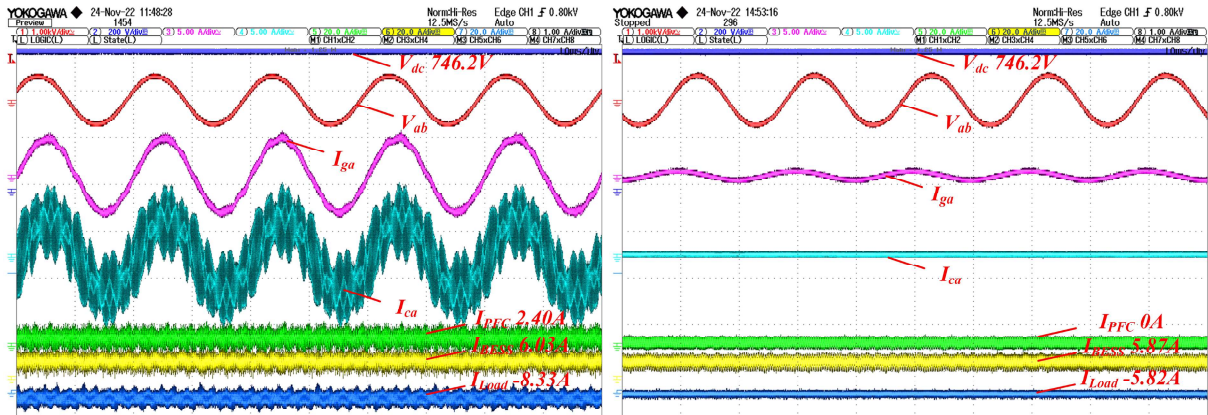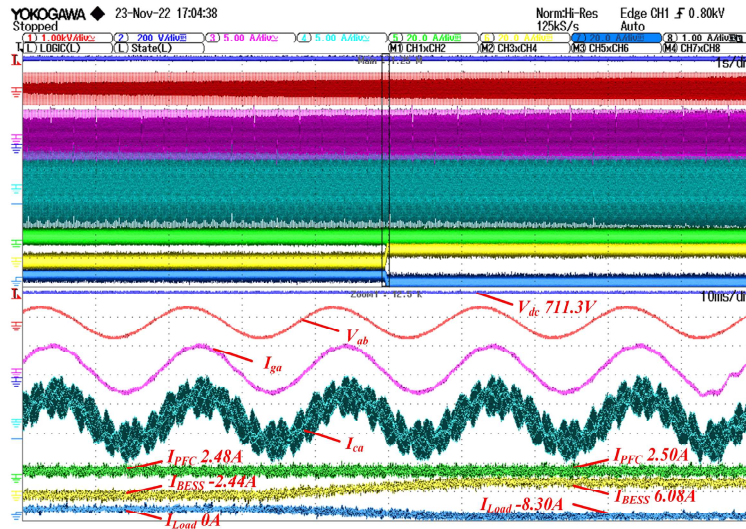
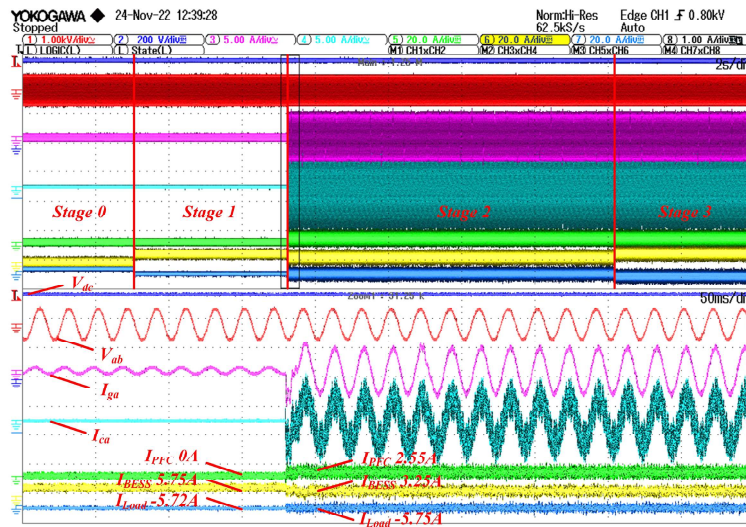**Figure 5.25:** Experiment results of transition 1

Figure 5.26: Experiment results of the first step of transition 2
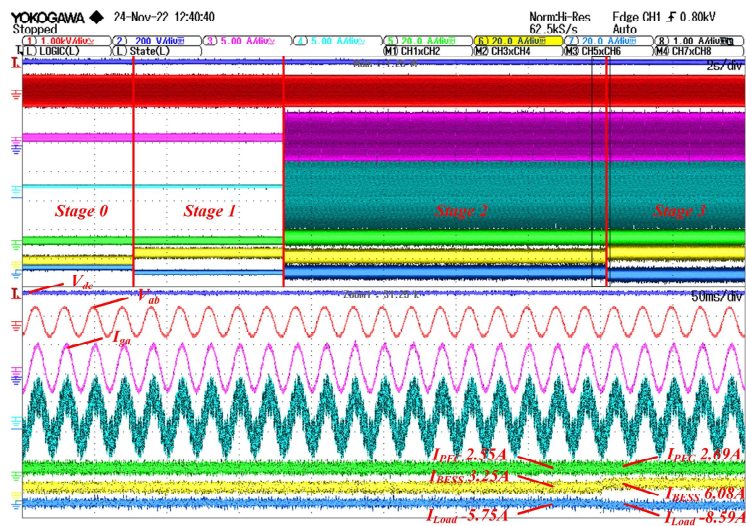

Figure 5.27: Experiment results of the second step of transition 2

The experiment results of Steady State 3 and 4 are shown in Fig 5.24. In Steady States 3 and 4, the constant current mode of the DELTA power supply will serve as a particular load. In accordance with the simulation section, the output power of the standard charging power mode and lower charging power mode in the experiment are set at 6kW and 4kW, respectively. In Steady State 3, at three different operating points, the power delivered to the load branch is calculated to be 5743.92W, 5903.79W, and 6215.85W, respectively. Likewise, in Steady State 4, the load branch absorbs 3966.04W, 4125.54W, and 4322.88W accordingly. Since the DELTA power supply is operated in constant current mode, the difference of power received by the load end at different operating points is mainly owing to the change in DC bus voltage.

The experiment results of Transition 1, the first step of Transition 2 and the second step of Transition 2 are shown in Fig 5.25, Fig 5.26 and Fig 5.27, respectively. As shown in Fig 5.25, when the SOC of BESS reaches 50%, Transition 1 is activated, and the current on each branch adjusts correspondingly. Since, in the experiment, the charging power of the grid to the BESS in Steady State 1 and the charging power of the grid to the load in Steady State 3 are both set to the same value, the current in the PFC branch does not change considerably between before and after Transition 1. And due to the abrupt shift in the DELTA power supply current on the load side (configured from 0 to -8.3A), the BESS needs to switch from the charging mode to the discharging mode to meet the power demand on the load side. Furthermore, based on the observation of I_{ga} and I_{ca}, it can be concluded that the control effect of the T-type converter during this transition is not significantly altered compared to steady states. For Transition 2, the whole process is depicted in Fig 5.26 and Fig 5.27. As stated in the simulation section, Transition 2 is mainly divided into three stages. For better distinction, they are marked as Stage 1, Stage 2, and Stage 3 in the figure. In Stage 1, the entire system is in a lower charging power mode and the BESS alone supplies the load with around 4kW of power. In Stage 2, the system is still in lower charging power mode, but at this time the total power is jointly provided by the grid and BESS. Finally, in Stage 3, the system switches to standard charging power mode. The total output power is around 6kW, and the excess power supply compared to the lower charging power mode is supplemented by BESS. By observation, the current distribution on the three branches shifted as expected. It is worth noting that, in Stage 2, the current on the BESS branch is slightly higher than the current on the PFC branch, which is still owing to the loss of the damping resistor on the PFC branch. While the load-side demand is being determined, the extra power demand will ultimately be shifted to the BESS branch.

In conclusion, based on the simulation of the whole system and experiments on the 6 kW rated lab-scaled hardware test bench, the integration concept of a BESS in an EV fast charger is validated. In this process, various directions of power flow according to the practical scenarios and the potential transitions are considered. Although the DC bus voltage will fluctuate due to the SOC of BESS and the dynamic response of the BESS during the transitions, the normal operation of the front-end 3-phase 3-level T-type converter can be guaranteed based on the current design.

6

Conclusion and Future Work

6.1. Conclusion

In this dissertation, in order to prevent overloading the grid during charging, integration of the BESS in a 450 kW EV charger is designed and validated both through simulations and a lab-scaled test-bench is verified in experiment. The 3-phase 3-level T-type converter is selected as the grid-connected PFC converter for the front end of the DC fast charger because of its superior performance, particularly for situations with low voltage and medium switching frequency. An appropriate modulation method based on the SVPWM is discussed and implemented considering the minimum switching principle and neutral voltage imbalance issue. Furthermore, effective control strategies including current loop control, voltage loop control, active damping by capacitor current feedback, and neutral point balance control are discussed and implemented.

For the design of BESS, there are two kinds of models utilized to analyze the feasible design. On the one hand, the three RC-link models is selected as an equivalent circuit model to analyze the interactions between the front-end AC/DC PFC converter and BESS during various working conditions. The proposed structure of the system integration of the DC fast charger is validated through the simulations via PLECS. On the other hand, a lumped model for Li-ion batteries combined with a sub-model strategy is conducted to preliminarily figure out a feasible solution considering the possible layouts and cooling methods, which is also verified through modeling and simulations via COMSOL.

At last, in order to confirm the feasibility of the proposed structure of the EV charger integrated with the BESS, the 6 kW rated lab-scaled hardware test bench is built in the lab. Taking consideration of the potential existing scenarios, various anticipated steady states and transitions are designed and conducted to test and verify the impact between the front-end AC/DC PFC converter and BESS comprehensively during not only steady states but also predictable transitions. Finally, it is concluded that based on the modulation and control strategy for the front-end AC/DC converter and the design scheme for the BESS, the normal operation of the system integration can be guaranteed.

6.2. Future Work

Combined with the current conclusion, potential future directions for research are listed as follows.

1. In this dissertation, the design of BESS integration mainly focuses on the interactions between the front-end AC/DC PFC converter and BESS, but the back-end part is only simplified as a current source both in the simulation and experiment platform. In the future, an isolated DC/DC converter, such as the full-bridge phase-shifted

(FBPS) converter or the dual active bridge (DAB) converter, should be included.

2. For the thermal modeling and simulation, more potential cooling methods are still needed to be explored and implemented to optimize the effect of heat dissipation. Meanwhile, an improved modeling method especially for the large-scale battery storage system is still worthy of further investigation considering its accuracy and available computing resource.

3. Although the concept of integration of a BESS to EV fast charger is experimentally validated by using a substitute of battery packs, which is the battery emulator, it would provide us further insight into the dynamic response if a real designed battery pack is used.

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