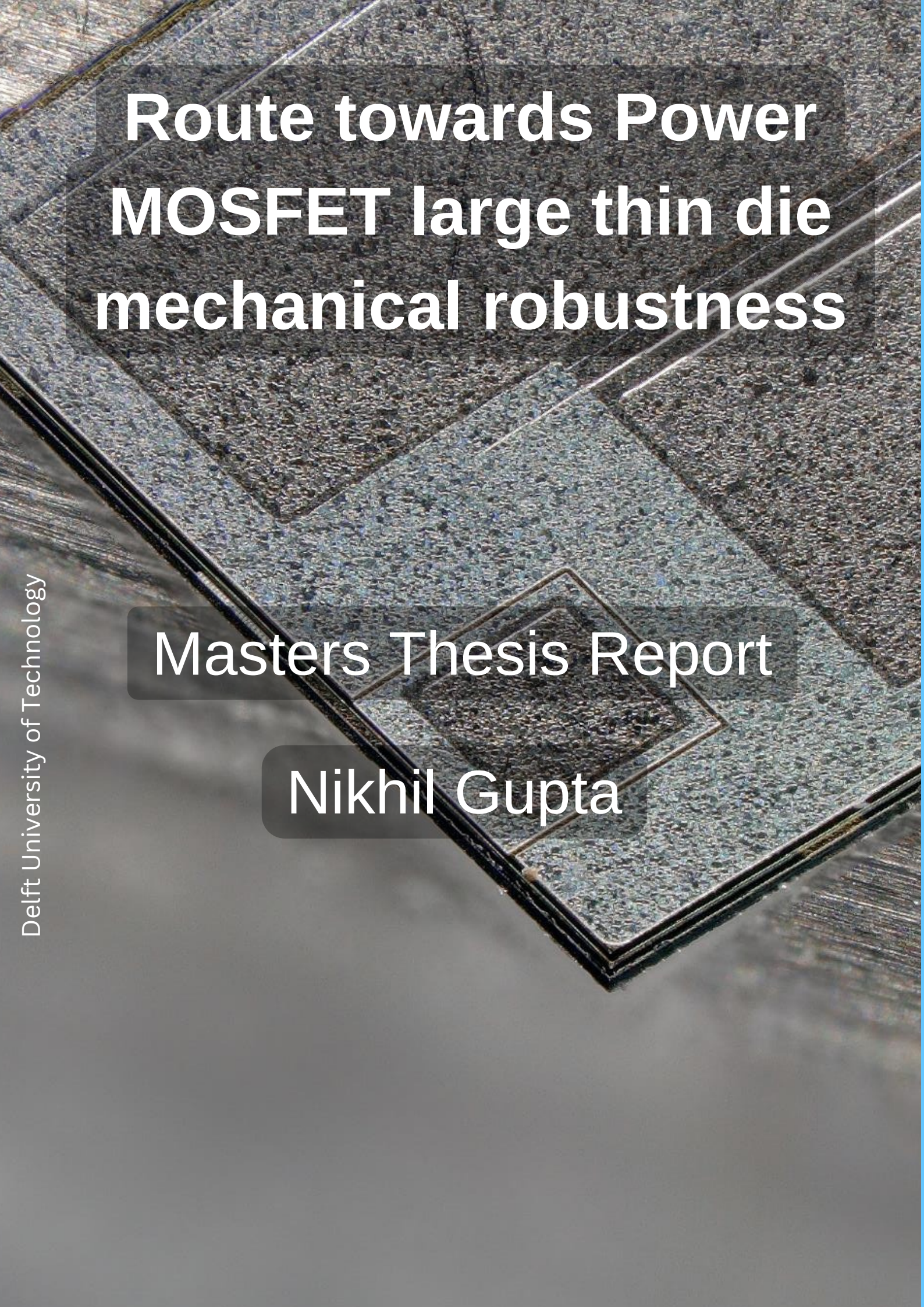

Route towards Power MOSFET large thin die mechanical robustness

Masters Thesis Report

Nikhil Gupta

Delft University of Technology

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by

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ABSTRACT

Today's cars are undergoing the greatest transformation the industry has seen. Power MOSFETs play a crucial role in making electronics more energy efficient by driving down switching losses and Rdson using a combination of next-generation trench technology and ultra-thin dies. Power MOSFET dies are becoming larger (> 5 X 5 mm) and thinner (< 50 μm) to meet the high performance lifetime requirements of the automotive industry. The high aspect ratio and the new chip designs with trench technology offer challenges for assembly, packaging and testing.

The majority of the research performed in the past, aimed to reduce the risk of die crack by improving equipment and process strategies in back-end semiconductor processing. This thesis study aims at improving die strength from a front-end approach (device fabrication process) by making dies stronger to stress from die frontside. New chip designs are presented with new metal layer layouts for improved stress distribution. Materials like polyimide are investigated as new die top material for mechanical strengthening of die frontside. Key factors which influence die strength like trench-metal interaction, wafer stress and warpage are also analyzed in this thesis report.

In this study, ultra-thin power MOSFET dies are realised on 100 mm diameter silicon wafers with dimensions of 6 X 3 X 0.050 mm. These dies are mechanical equivalent in design, robustness to commercial trench power MOSFETs. The processed wafers are grinded from the backside to realise 50 μm thin wafers which are then sawned to obtain singulated dies. The strength of the dies are characterized by three-point bending tests and analyzed using probability plots for weibull distribution.

Different chip designs are compared with each other and robust designs are presented as recommendations for fabricating stronger thin power MOSFET dies to provide high performance and throughput in assembly and packaging processes.

Keywords: Power MOSFET, ultra-thin dies, back-end, front-end, trench, polyimide, three-point bending, weibull distribution.

ACKNOWLEDGEMENTS

I would like to sincerely thank and appreciate the following people for their contribution in making this project possible. Dr. René Poelma for providing me the opportunity to work on this project in collaboration with Nexperia. I am grateful for your guidance, weekly discussions and sharp feedback which immensely helped me to shape this project in the right direction. Dr. Henk van Zeijl for his guidance through the fabrication part of this project and also for the great suggestions and discussions. I want to express my sincere thanks to Prof. Guoqi Zhang for giving me the chance to conduct my thesis research with Electronics Components Technology and Materials (ECTM) research group as well as for his excellent suggestions for improvement, constant encouragement, and pushing me to try new things.

Else Kooi Laboratory (EKL) played a big role in my project where I was allowed to use Class 100 clearnroom facilties for my sample's fabrication. I would like to thank the entire EKL team for their support. I am very grateful to Xinrui Ji for her support during my experimental phase. Her constant support and guidance allowed a smoother fabrication experience in EKL clearnroom. This project could not have been completed without support of Bob Knoppers from 'NXP Sample service center' where my wafer thinning and dicing process took place and also Patrick van Holst from department of Precision and Microsystems Engineering (PME) for giving me access to DMA tool for performing my stress measurements. My colleague Rami Younis from Nexperia constantly supported my project and helped me in learning tools required for my project.

At the end, I would like to thank my family and friends for being a constant pillar of support and motivation throughout my journey. I am thankful to my parents for providing me the opportunity to study in TU Delft for my master of science studies in microelectronics.

Nikhil Gupta
Delft, October 2022

Contents

List of Figures

List of Tables

List of Symbols & Acronyms

Symbols

CMP Chemical Vapor Polishing
DMA Dynamic Mechanical Analyzer
DOE Design Of Experiment
EKL Else Kooi Laboratory
HAR High Aspect Ratio
HF Hydrofluoric acid
HMDS Hexamethyldisilazane
HT Horizontal Trenches
ICP Inductively Coupled Plasma
LPCVD Low Pressure Chemical Vapor Deposition
MOSFET Metal Oxide Semiconductor Field Effect Transistor
MT Mixed Trenches
PAI Polyamide-imide
PECVD Plasma Enhanced Chemical Vapor Deposition
PI Polyimide
RDSON Drain-Source On Resistance
RIE Reactive Ion Etching
TEOS Tetra Ethyl Ortho Silicate
UV Ultraviolet light
VT Vertical Trenches

1 PROJECT INTRODUCTION

Automotives are experiencing the most radical transition the industry has ever witnessed. Continued electrification is causing considerable modifications from the engine to the cloud. Innovative technologies and systems for the powertrain, chassis, safety, lighting, and body electronics contribute to the enhancement of overall vehicle efficiency and the reduction of fuel consumption, CO_2 emissions, and costs. Power MOSFETs play a significant role in enhancing the energy efficiency of electronic devices by reducing switching losses and Drain-Source on resistance ($R_{DS(on)}$) through the use of cutting-edge trench technology and ultra-thin dies.

Power MOSFET devices can have two topographies, Trench MOSFET or Planar MOSFET. Trench MOSFET are used for low voltage application (< 200 V) as they offer higher channel density and lower on resistance ($R_{DS(on)}$) [2, 30]. Planar MOSFET are used for high voltage applications where on resistance is dominated by epi-layer resistance and thus high channel density from trenches is not required [2]. The figure 1.1 below shows the wide range of applications where power MOSFET are used in automotives.

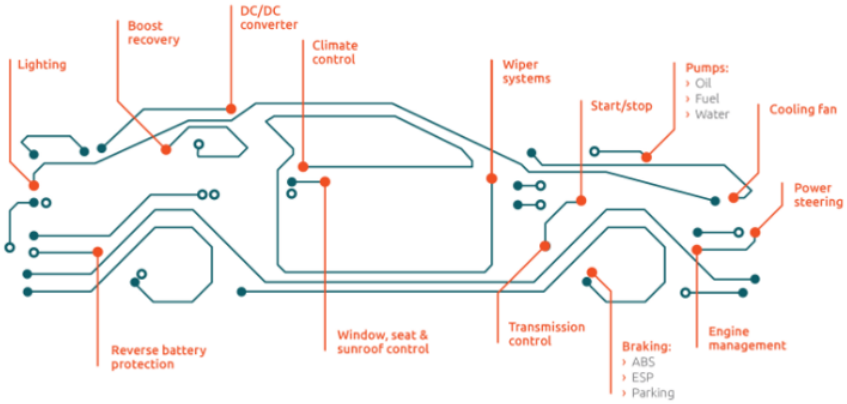


Figure 1.1: *Power MOSFET are one of the key devices for power switching and other wide range of applications in modern electric vehicles [24]*

In this project, focus is shifted to Si-based trench power MOSFETs where current is driven vertically from one surface to the other surface to achieve high driving capabilities. It is realised by packing millions of trenches on the die where each trench controls the current conduction around it with a combination of gate dielectric and gate electrodes [30].

1.1. Problem description

Power MOSFET dies are becoming larger (> 5 x 5 mm) and thinner (< 50 μm) to meet the high performance and lifetime requirements of the automotive industry. The high aspect ratio and the new chip designs (unique trench technology) offer new challenges for assembly and packaging. This is because thin substrates and large area devices make dies susceptible to fracture from small cracks induced during dicing, thinning and other handling processes. In figure 1.2, one such instance of die cracking is shown during die pick-up process where the thin die is unable to handle needle and collet force applied by the pick-up tool and results in crack. This thesis presents an experimental study on how to increase mechanical robustness and reliability of large thin power MOSFET dies to reduce the risk of die crack for next generation packaging and assembly processes.

Power MOSFET device fabrication introduces structural stress from the different depositions, etching and other processes. This can result in wafer warpage due to the tensile or compressive stresses after fabrication.

Wafer thinning and sawing processes induce additional defects and stresses in these wafers. Post grinding and sawing, the ultrathin dies are picked up from the carrier. To meet the throughput requirement of the industry, an ultra fast pick up and place process is essential. The automation tools used for this segregation induce new forces and stress on the individual dies and hence increase the risk of crack initiation and device failure. The die after pick-up is attached to a lead frame and encapsulated. This packaging process establishes electrical connections and connects the die to the outside world. During the packaging phase, the die further undergoes various additional thermal and mechanical steps which exert stress on the silicon.

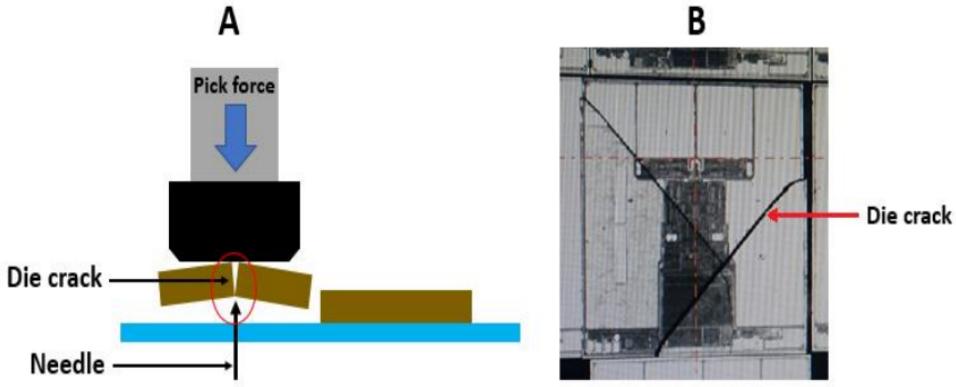
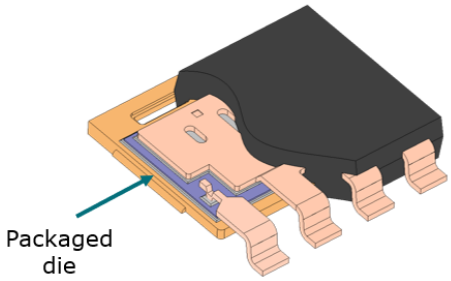


Figure 1.2: *A) Thin die cracking during die pick-up process; B) Die crack as seen in silicon die [28].*

It is imperative to ensure that the finished product is highly reliable during its lifetime. It is therefore important to prevent any factors which can potentially cause functionality failure of the installed power MOSFET device caused by die crack or other failures. For a continuous upscale in performance and efficiency of large-thin dies to drive next generation electric vehicles, wafer thinning is one of the key and most challenging strategy which demands for thin dies to be made more robust.

Why make dies thinner?

- Large thin dies offer higher efficiency, longer lifetime and sustainability as they provide lower $R_{DS(on)}$, reduced switching losses and increased current driving capability [16, 31, 29].
- Thin silicon wafers (50 μm) improve heat dissipation of dies with high power densities [29].
- Thinner dies reduce die attach solder fatigue.
- Wafer thinning increases the mechanical stability of wafers, thus enabling bendable and flexible next generation devices [31].



Parameter	< 50 um thick die	> 70um thick die	Remarks
Performance	↑	↓	On resistance
Reliability	↑	↓	Solder fatigue
Manufacturing	↓	↑	In assembly
Robustness	↓	↑	Die strength

Figure 1.3: *Thin dies packaged inside a copper-clip package for high performance and efficiency applications; Table comparing different parameters between thin and thick power MOSFET dies*

To summarize, large-thin power MOSFET devices drive the rapid electrification of automotive industry by

delivering higher performance and efficiency compared to thicker MOSFET devices.

1.2. Research Objectives

The project aims to find new insights and build new understanding in trench power MOSFET device fabrication that influence thin die fracture strength. Research topics are discussed below:

- Investigate the effects of different stress buffer techniques to minimize pre-stress in dies front side (e.g. nitride and polyimide).
- Influence of the die-top metal-system layout.
- Influence of trench layout and orientation respective to die bending stress.
- Interaction between trenches and metal die top system.

The second objective is to develop a test chip to evaluate new designs and materials to speed up the research and development in semiconductor manufacturing.

1.3. Approach

Most of the current die strengthening strategies in the industry optimize or improve back-end processing of thin chips to ensure robust yield from wafer thinning and sawing to assembly and packaging. This project focuses on improving die strength from a front-end approach (device fabrication process) by making dies stronger to stress handling from die frontside.

- The first approach is to realize different test chip designs and platform to evaluate die strength.
- Investigate with new materials such as polyimide as die top materials for their potential application as stress buffer.
- Fabricate test power MOSFETs with high sensitivity. These devices will be close mechanical copy of actual trench MOSFETs.
- Wafer thinning and sawing of processed wafers to obtain ultrathin dies (<50 μ) to induce high sensitivity for strength tests. At present, commercially available device thickness is > 75 μ.
- Measurement of ultra-thin die strength is realized using three-point bending strategy. Obtained test data analyzed using Weibull and 5-sigma limit analysis for characterizing bending strength of different die designs.

The mask design was made using L-edit software by Tanner tools. The dummy power MOSFETs are fabricated using CMOS fabrication facility in class 100 cleanroom of EKL at TU Delft . Wafer thinning and dicing was supported by NXP sample service center. Three-point bending for die strength characterization is done in faculty of PME, TU Delft using DMA tool. In some instances, the project required new process technologies and recipes to be developed to deliver comparable samples which are close to industry manufactured power MOSFET.

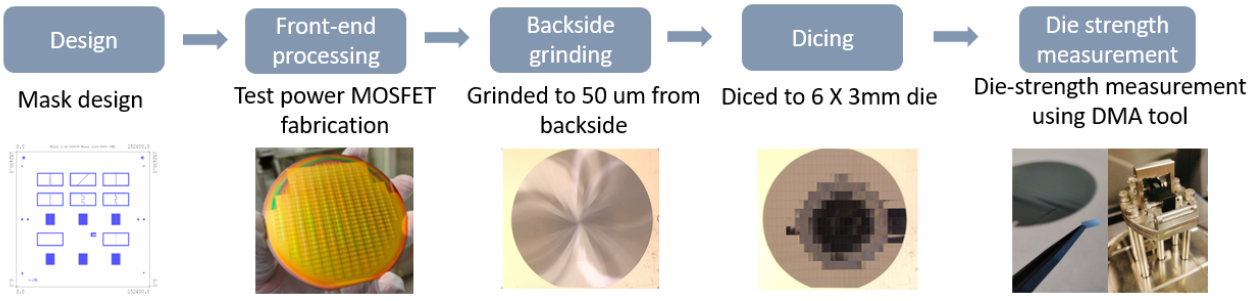


Figure 1.4: *Different stages in thin die robustness investigation*

We omit complexity such as the device electrical functionality, different trench profiles and aspect ratios for

gate and source areas. This was replaced by one common trench profile and aspect ratio for both regions. Silicon doping is also removed from the process and investigation is purely focused on the geometrical aspects of trench layout and die top system. The experimental results will then be used to propose design improvements for potential implementation in new chip designs and front-end manufacturing.

1.4. Outline

The outline of this thesis is as follows: In chapter 2, a bird's eye view of existing semiconductor process strategies, materials to strengthen thin dies are discussed. Chapter 3 highlights different design of mask layers used for lithography in fabrication process of power MOSFETs. A design of experiment is also formulated to support different designs for same process layers. In chapter 4, various fabrication processes undertaken for making test power MOSFETs using the EKL cleanroom facilities are discussed. The chapter briefly explains each of the process step and their challenges.

Following this, chapter 5 contains the back-end processing of the processed silicon test power MOSFETs. Strategies and challenges involved in wafer thinning and singulation are discussed. In chapter 6 the singulated dies are measured for their fracture strength using three-point bend test and data is analyzed using weibull analysis. Chapter 7 consists of project summary along with conclusions and recommendations.

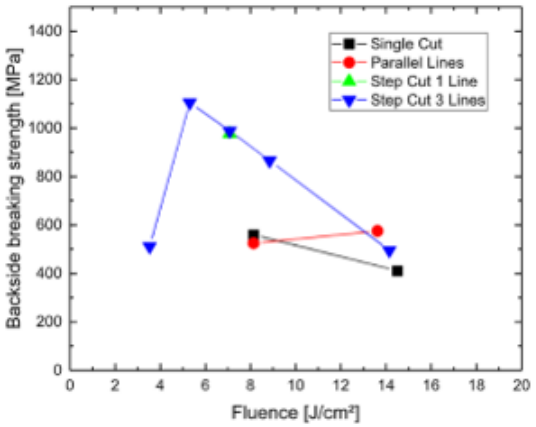
2 LITERATURE OVERVIEW

2.1. Chapter introduction

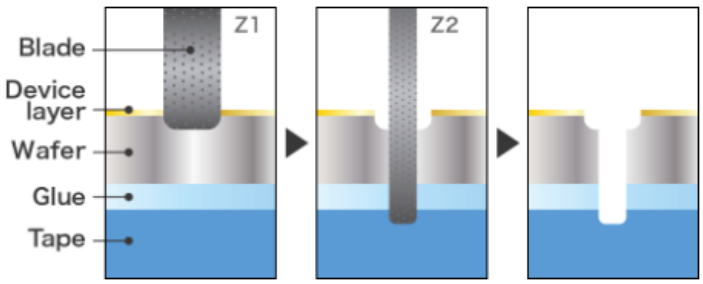
This chapter highlights different strategies used in semiconductor industry today to improve mechanical robustness of thin dies. The majority of die-strengthening techniques are implemented in the semiconductor chip's back-end process stage. This includes strategies in grinding, dicing, die pick-up and place where traditional methods were found to inflict more damage to dies on top of their existing stress from front-end device fabrication. Novel materials for die top strengthening and an outlook on a new die strength measurement technique for ultra thin dies ($< 50\ \mu$m) are also discussed later in the chapter)

2.2. Die strengthening dicing techniques

Dicing of thin silicon dies with traditional dicing technique like mechanical dicing results in increased chipping at the die edges which negatively influences the die mechanical stability. Dicing via ultrafast laser with ultra short pulses is found to enhance die strength under specific operating conditions like lowering pulse energy, scan speed and number of accumulated fluences (stream of particles) per scan in the process [9]. Also the backside breaking strength of dies are found higher using step cut dicing method as compared to parallel line cut and single line cut as seen in figure 2.1a.



(a) *Figure shows mean backside breaking strength using different sawing techniques. Dies diced with step-cut are mechanically stronger dies compared to parallel and single cut dies [9]*



(b) *The above figure explains step cutting strategy which is a dual dicing process wherein first a half cut is performed, followed by a full cut. This is done to efficiently cut the wiring layer formed during the semiconductor fabrication process [7].*

Dicing before thinning technique is another commonly used technique which promotes greater robustness than traditional dicing after grinding process [4, 22]. This technique minimizes edge crack and dicing marks which influence die strength substantially [15, 27, 22].

2.3. Post grinding wafer stress relief techniques:

Wafer thinning process is commonly used to reduce the total wafer thickness by removing silicon from backside using grinding technique [18]. Grinding the wafers have found to induce a lot of stress and warpage to thin silicon wafers. A stress relief technique used to remove this damage layer is backside wet chemical etching or Chemical Mechanical Polishing (CMP) [23].
As the strength of the singluated dies is also found correlated to its backside roughness. Using a finer grain size grinding wheel for backside grinding can help minimize this backside roughness and reduce the risk of failure caused by it. Figure below shows the influence of grinding wheel type on the backside roughness

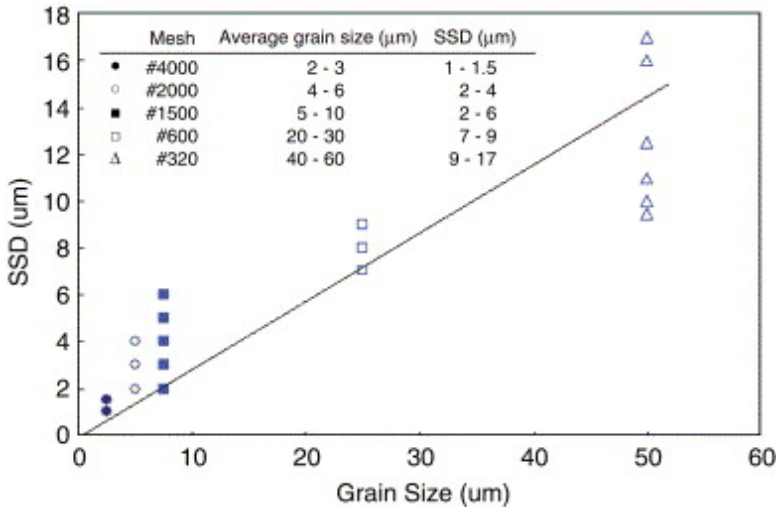


Figure 2.2: *The above graph shows the correlation between the grain size of the grinding wheel to the wafer backside roughness [20, 21]*

2.4. Die pick-up and place optimization

Dies need to be singulated for packaging, post grinding and dicing process. It requires die to be successfully picked up, without any damage from the carrier foil where the diced dies are attached. Die-cracks during pick-up of ultra-thin, high aspect ratio dies is one of the major challenges to robust yield in assembly process. In industry this process is facilitated using automated die pick-up and place tool. An unoptimized process can lead to increased risk of die breakage or pick-up failure, leading to unusable damaged dies. Some of the steps undertaken to optimize this process are discussed below

- Optimize collet (where the die sticks after de-attaching from wafer) shape and push-down force applied on the die during the pick up.
- Ejection needles can result in localised damage on die. Needle positions and size used for pushing the die from below the foil are optimized to minimize their negative impact on thin die pick-up
- Thin dies are found to have an increased adhesion with dicing foil which leads to an increased pull-force [5]. Very low adhesive UV foils are thus required for die pick-up process.

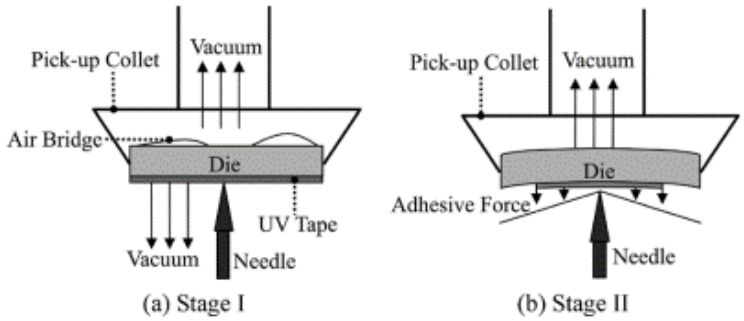


Figure 2.3: *The above figure shows two stages in the die picking process, Stage 1 where collet pushes down to contact the die and applies vacuum; Stage 2 where the needle raises up to push the die and tape beneath move upwards and peels the tape from die. This is followed by collet pulling the die up under vacuum pressure [19]*

Ejectorless die pick-up process eliminates the use of ejector pins to achieve robust pick-up of high aspect ratio thin die at the cost of reduced throughput [29]

2.5. Novel material for die top strengthening

Polymers were investigated to support the die top as buffer layer for mechanical robustness. Polymers like polyimide have unique properties suitable for this strengthening like

- High tensile strength over wide temperature range (-270 °C to 300°C)
- Excellent resistance to stress cracking
- High glass transition temperature up to 400°C
- Minimal thermal expansion
- Good processability compatible with current silicon based semiconductor fabrication.

Polyamide-imide (PAI) is a polymer which shows properties of both polyimide and polyamide as well. Torlon, a PAI from manufacturer Solvay promises to exhibit metal like performance at elevated temperatures as it can retain its toughness to resist cracking at higher temperatures. As per manufacturer, Torlon has the highest strength and stiffness than any commercial thermoplastic. This property of PAI polymer makes it an ideal candidate for its application as stress buffer layer for die top strengthening. In the figure 2.4, key properties like coefficient of thermal expansion (CTE) and material toughness is compared between Torlon (PAI) and other materials.

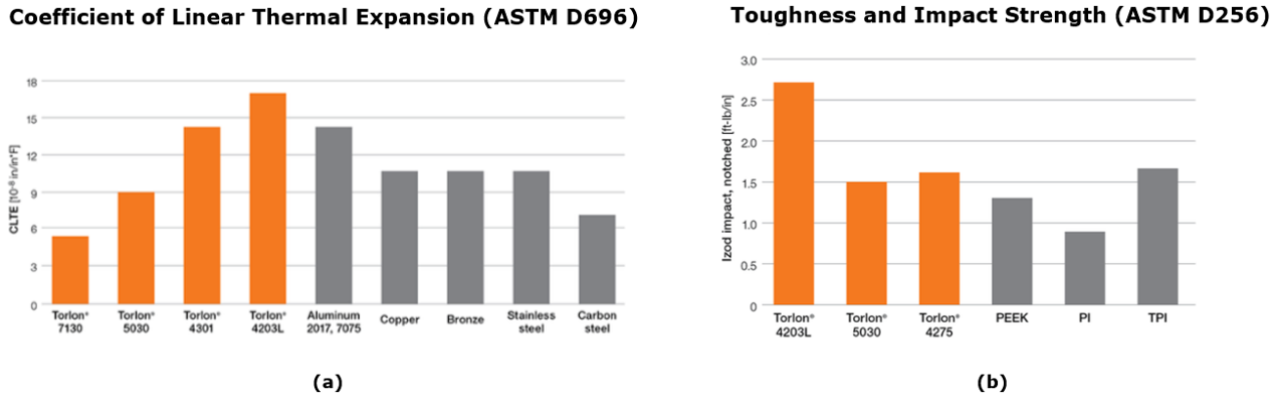


Figure 2.4: *Figure (a) shows histogram comparison between Torlon and metals where Torlon 7130 shows minimal thermal expansion; (b) shows histogram comparison between polymers for their toughness and Impact strength where Torlon is more than two times stronger than other polymers [34]*

2.6. Cantilever bending test for ultra-thin die strength measurement

The traditional method for quantifying the strength of a silicon die is known as three point bending test. Detailed explanation of this testing strategy will follow in the testing chapter 6. In all the present literature, the three point bending test has been found the dominant testing method even for thin silicon dies (> 50 μm). Silicon dies on thinning down to even lower thickness offer new challenges to three point test strategy and affect the data's credibility. This phenomena is owning to increased flexibility found in silicon wafers on becoming ultra thin. The major issues in three point bend test are discussed below:

- High data variations for low thickness silicon dies due to increased silicon flexibility.
- Non-linear force-displacement curve which are not supported by the mathematical stress calculation equations (figure 2.5)
- Silicon young's modulus reduces with 50 μm die thickness and below
- Increased silicon flexibility requires the supports in three point bend testing to be closer together, causing practical challenges in test setup. [25]

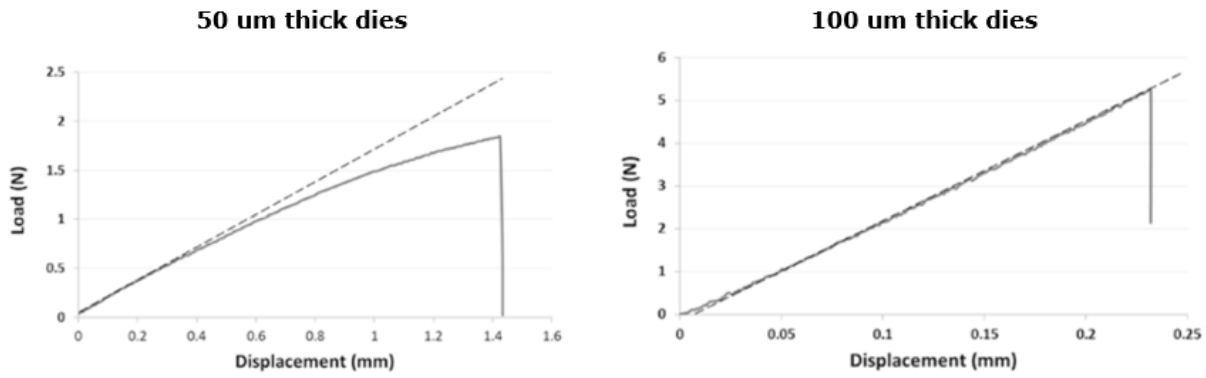


Figure 2.5: *Load tip force vs displacement curve for Si at 50 µm um and 100 µm thickness respectively as measured in three point bend test. The slope of the curve (stiffness) for 50 µm is seen to follow non-linear path compared to 100 µm thick silicon die [33]*

A novel bend test method known as Cantilever bending test offers solution to above challenges for measuring the strength of ultra-thin dies. The principle test setup is shown below in figure 2.6.

The die sample is clamped into one support and the top side is pushed to bend the die (shear stress). A portion of the die hangs at top and the hanging height of die and the force required to break the die is measured. This test strategy allows very short bending span, eliminating need to go for large deflections (a disadvantage in three point bending for ultra-thin die).

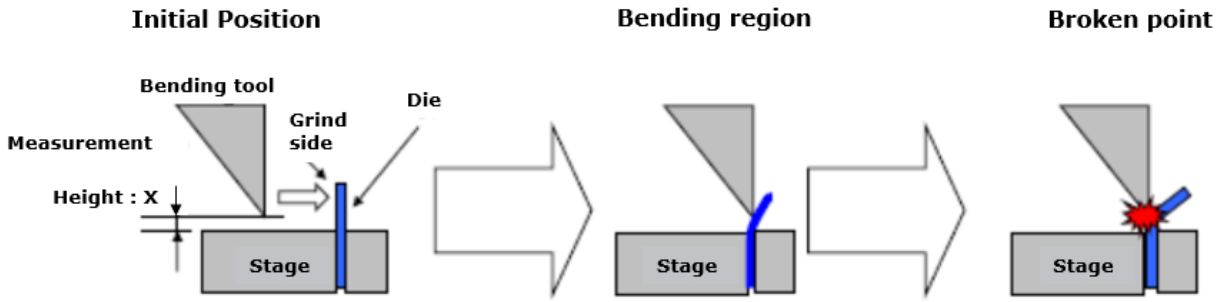


Figure 2.6: *The above figure shows different stages in the cantilever die bending test. Stage 1) die is clamped in one support with grinded side exposed to bending tool; Stage 2) bending tool applies shear stress to bend the die topside; Stage 3) die breaks around contact point [26].*

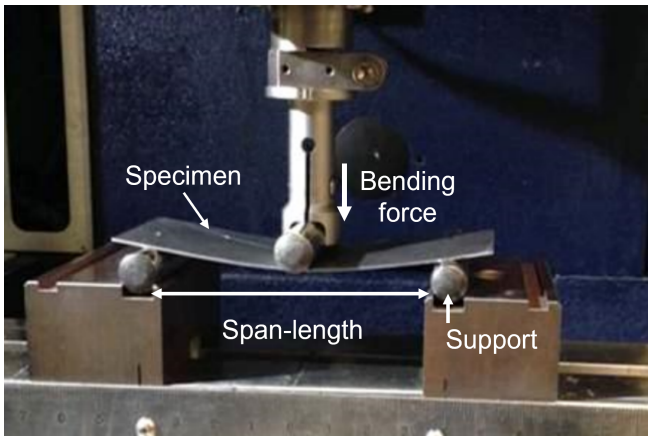


Figure 2.7: *Traditional 3-point bend test setup by bruker where load-displacement control modes are used for die strength measurement [3].*

Hsin-Chih Shih (2019) in his study [33], performed a comparative study between three point bending and cantilever bending test for die strength measurements of silicon dies with different thickness. The test results showed die strength data measured with cantilever bending significantly improved the problem of data variations (standard deviation) previously seen in three point bending test.

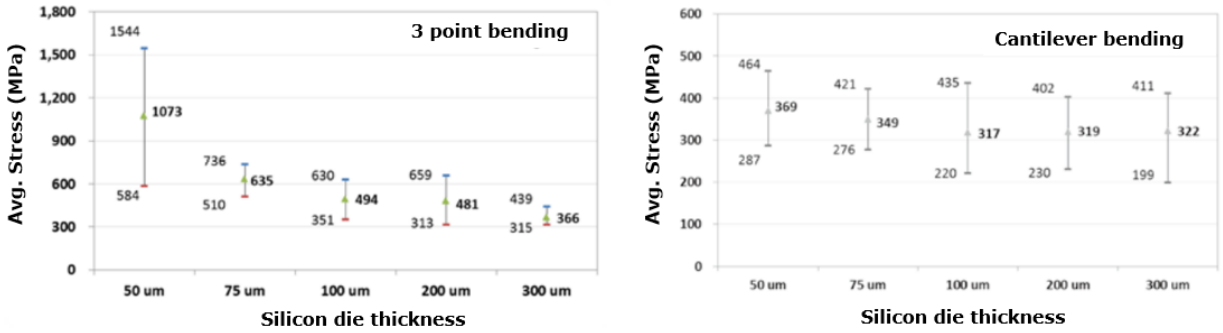


Figure 2.8: *Figure shows relation between average die stress vs silicon die thickness for two strength measurement techniques, 3-point bending (on left) and cantilever bending (on right). 50 µm dies in 3-point bending test show high data variation which is reduced by cantilever bending test as it can support very short span length required for ultra thin dies [33]*

2.7. Chapter Summary

In this chapter, different strategies for making thin dies mechanically robust are discussed. Most strategies aim to improve die strength from improving equipment and process strategies in back-end semiconductor processing. New novel materials like Polyamide-imide also show promise for semiconductor processing as potential die top passivation layer. New die strength measuring strategy are also discussed which offer solution to challenges in strength measurement for ultra-thin dies. Based on the literature, it is implied that no major research is being undertaken to make ultra-thin dies stronger at fabrication level and more emphasis is done in developing techniques for smooth processing of fabricated dies in back-end process. In this project, we attempt to make dies more robust at front-end level by using new design and approaches which can be realised using existing semiconductor infrastructure.

3 CHIP DESIGN AND DOE

3.1. Chapter introduction

The project aims to make large thin Power MOSFET dies more mechanically robust. In this chapter, the design parameters and considerations for fabricating the test chip are defined. These test chips are a close mechanical copy of commercially available power MOSFET chips. The design is simplified which allows for better reproducibility and analysis for increased stress and failure in dies. We define different investigation routes later in the chapter under design of experiments section.

3.2. Power MOSFET chip design

The goal is to design a test chip which replicates the design and sensitivity of commercially available power MOSFET chip. After that, new layer stacks and designs are added to create various design routes for investigation. Each design route is proposed to either improve fracture strength of test chip or give new insights and understanding to factors which increase the risk of die crack.

1. **Commercial Power MOSFET vs Dummy Power MOSFET chip cross section**
    - Similar layer stack with relevant process layers like trenches, oxide, metal and nitride.
    - Test design simplified for one thicker metal layer rather than two different metal layers for simplicity. Total metal thickness is same.
    - To investigate impact of gap between gate and source metal layers, dummy chip is designed with identical 50 μm gap to introduce similar sensitivity.

(a) *Commercial Power MOSFET chip cross-section*

(b) *Test chip cross-section*

Figure 3.1: *Die cross-section comparison between commercial and dummy power MOSFET chip.*

2. **Die outline**
    - Similar dimension kept for dummy chip (6 X 3 mm) as compared with a large MOSFET chip.
    - Design simplified (in figure 3.2) to focus on the gate area.
    - Similar thickness of the test chip for testing.

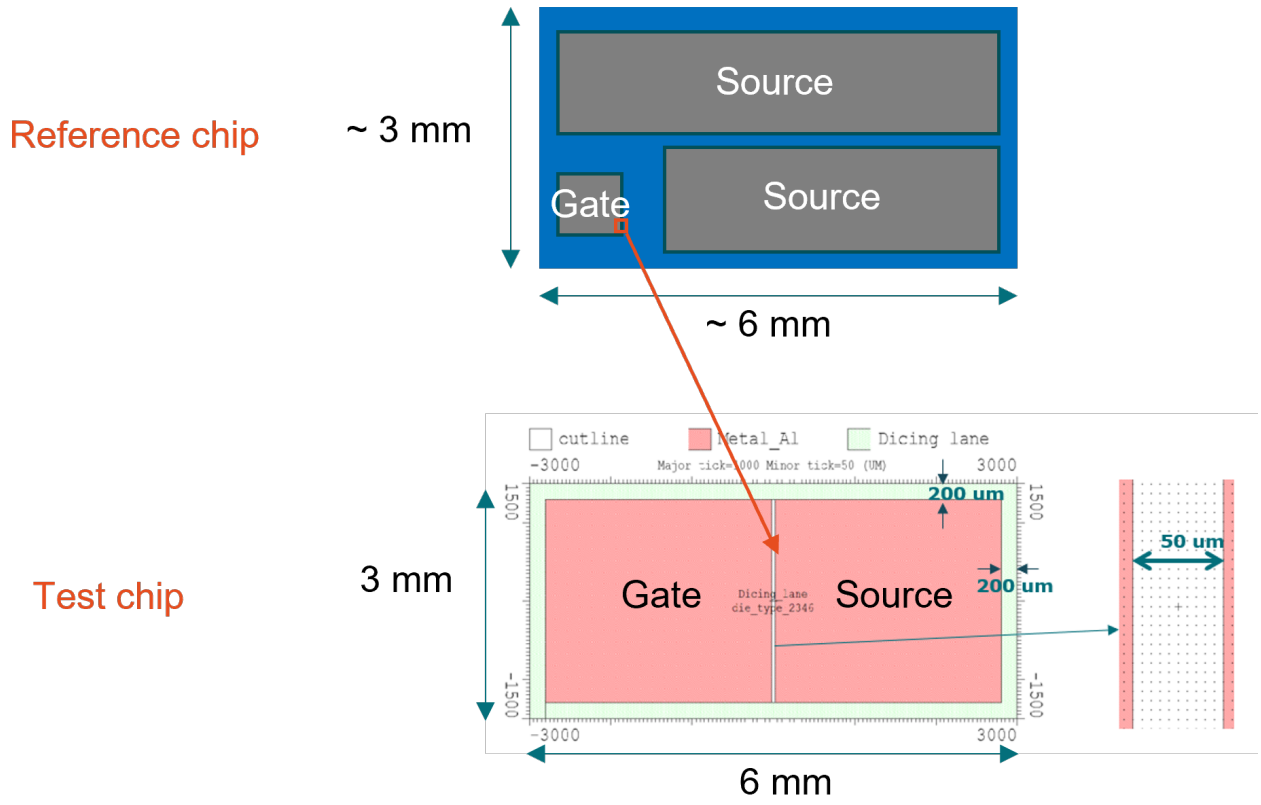


Figure 3.2: *Outline of commercial large MOSFET die as compared to test chip die. Gate-Source gap is same for both outlines.*

3. **Trenches in chip design**

- Two different direction of trenches are observed in reference MOSFET which is arrangement either parallel (Gate) or perpendicular (Source) to long axis of die. Test chip is also designed to have this mixed trench design.
- Trenches in gate and source area for test chip are designed for same aspect ratio (depth : 5 μm ; width : 2 μm ; Aspect Ratio : 2.5) and pitch of 5 μm with respect to reference MOSFET where trench aspect ratio and pitch varies for gate and source area.
- The profile and aspect ratio of trenches is also fabricated to make close resemblance to reference MOSFET.

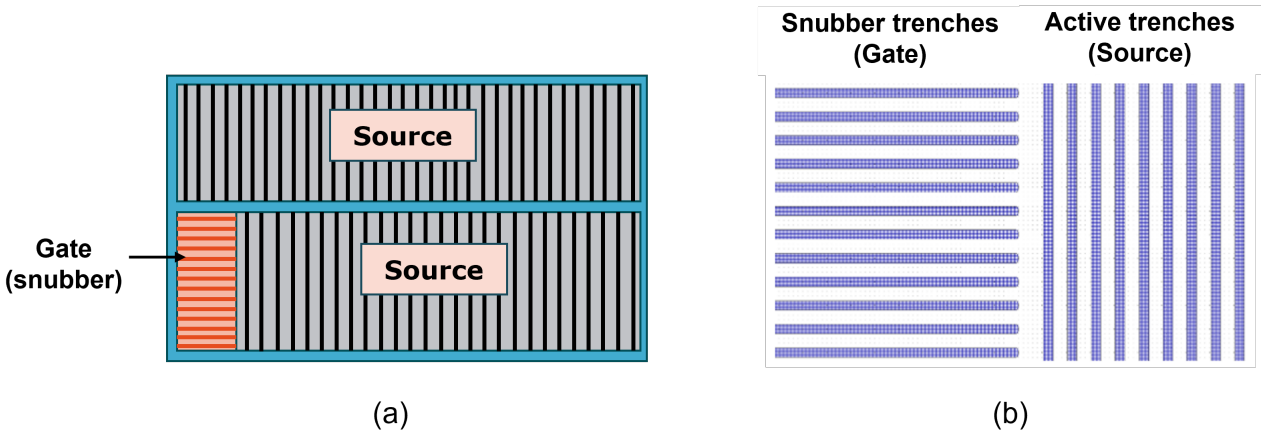


Figure 3.3: *a) Trench layout and orientation in commercial power MOSFET; b) Trenches in dummy test chip*

3.3. Test chip design

In this section, different designs used for patterning key process layers in the test Power MOSFET like the trenches in silicon and thick die top metallization layer. These designs are further divided into two types as discussed below

- **Standard chip design:** This design is used to prepare standard test chip which is a close mechanical copy of commercial trench power MOSFET chip.
- **New designs for strength improvement investigation:** These designs explore new layouts for metal and trench layers for investigation. Each new proposed design is proposed to influence the die strength during the three point bend test.

Figure 3.4 below shows the schematic for the loading and bending condition of the die for three point bend test. This bending test provides experimental data to characterize fracture strength for die samples. The project aims to design and fabricate different chip designs to compare in order to find ideal design for ultrathin dies.

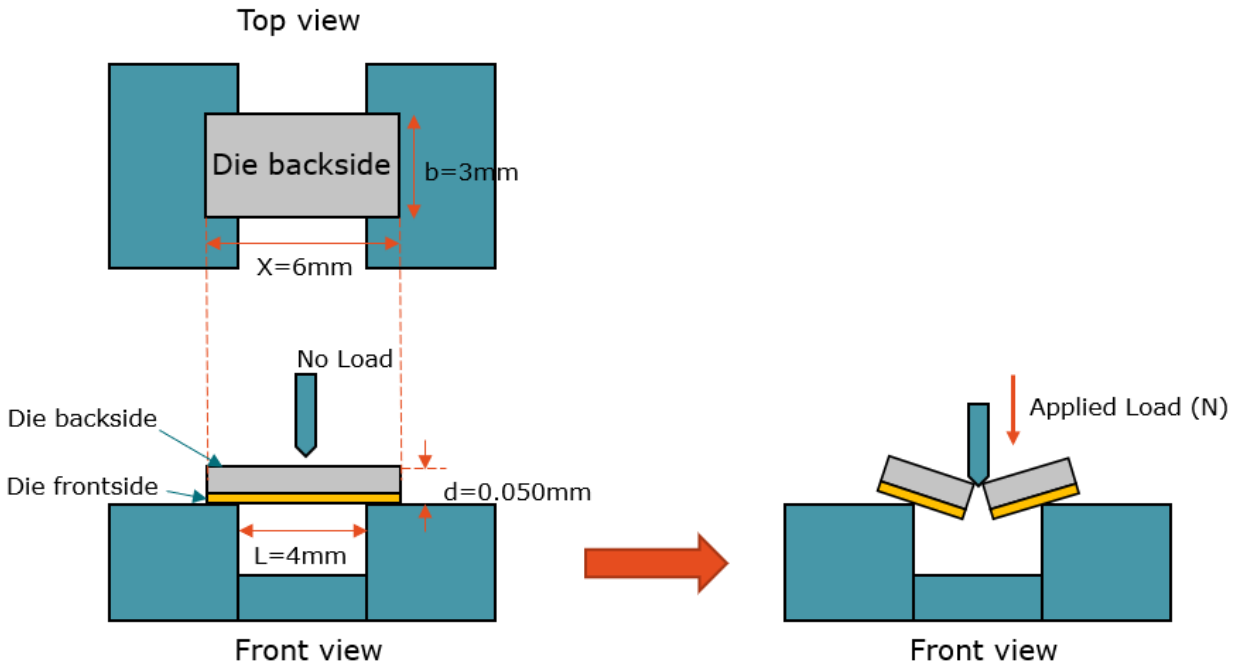


Figure 3.4: *The above schematic shows die specimen loading setup. Die is flipped exposing silicon backside to applied force and die cracks from frontside first under tensile stress*

3.3.1. Different top metal design for test chip

- **Standard Test chip: Gate-Source with 50 μm gap**

  This chip design is used to replicate commercial power MOSFET design in a simplified form to better investigate factors affecting die strength near gate area. In this chip design, gate and source metal areas are separated by a vertical line gap. This gap is 50 μm wide. The green coloured border as seen in figure 3.5 corresponds to dicing lane where metal is absent and provides a path for the dicing blade to cut through the wafer for die singulation as discussed in chapter 5. The dicing lane is 200 μm wide.

  High fracture toughness is one of the key material properties of metals like aluminium which prevents crack propagation through the die after its origination under stress [38, 13]. In the absence of metal, the crack is found to propagate in vertical line gap as materials within the path have low fracture toughness compared to aluminium metal.

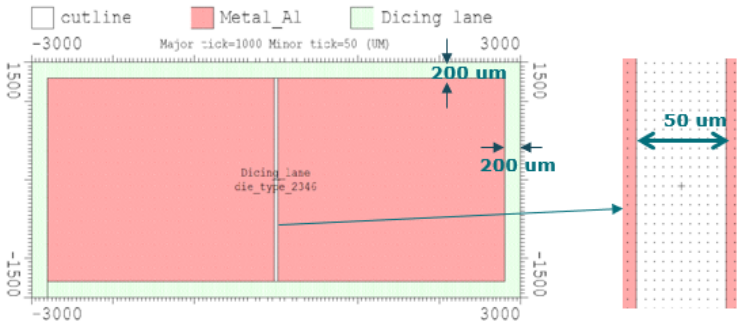


Figure 3.5: *Standard test chip where gate and source metal area are separated by a 50µm vertical line gap*

- **Improvement Design 1: Reducing Gate-Source gap to 20 μm**

  In this design, gate source metal gap is reduced from previous 50 μm to 20 μm gap. This mask design was used for investigating the effect of gap between gate-source metal on die strength in mechanical testing. Dicing lane is also present in the design. The decreased width of metal gap (50 to 20 μm) also creates increased total metal density in the silicon die. The increased metal density can also potentially improve the current spreading and density.

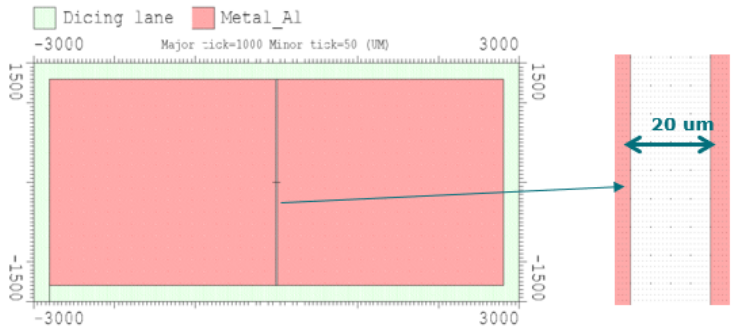


Figure 3.6: *Chip design with reduced gate and source metal area separation (20µm)*

- **Improvement Design 2: 45° angle for Gate-Source gap**

  The Power MOSFET have trenches at the front side. Trenches are nothing but deep openings in silicon which are filled with suitable materials. These trenches go in two different orientations, horizontally in the gate area and vertically along the source area. In crystalline silicon < 1 0 0 > , a small crack can completely propagate in the entire crystal plane. In thin dies, trenches are very vulnerable hot-spots for crack origination and under small stress, this crack can propagate along the trench in the silicon plane especially in the metal absent gap area.

  To counter for crack propagation in metal gap, the gap line is designed to form an angle of 45 ° to the metal layer instead of straight path. The gap between the two metal blocks is kept same as 50 μm. With this design, in the event of crack origination in trench, the angled pattern is expected to prevent crack propagation in vertical path because gap area is shifted by 45 ° to both trench directional axis

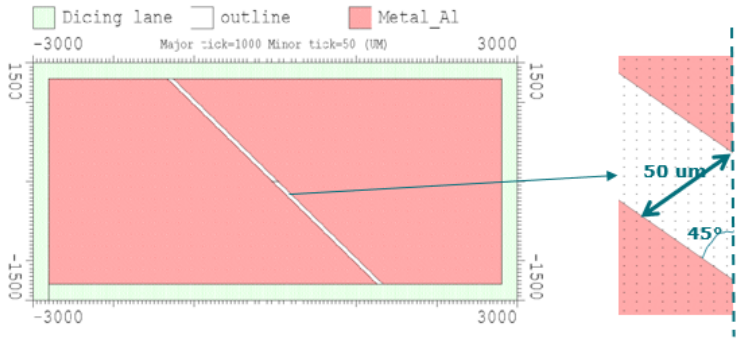


Figure 3.7: *Chip design where gate-source vertical separation is replaced with a 45° angled metal layer*

- **Improvement Design 3: Meander for Gate-Source gap**

  This improvement design aims to improve strength of chip near vertical metal absent area by introducing a meander design to replace vertical line gap. The idea behind the design is to introduce metal coverage in the most likely crack propagation area. As mentioned previously, metals like aluminium have high fracture toughness [38, 13] which prevents crack propagation through it. The gap between the two Gate-Source metal areas remains 50 μm throughout the meander in view of chip design requirements.

  Four different meander shapes were designed namely 1) Meander with thick fingers; 2) Meander with thin fingers; 3) Meander with thick fingers and reduced horizontal width; 4) Meander with thick fingers and enhanced horizontal width. Out of 4 designs, 2 designs were selected i.e. 1 and 2 (refer figure 3.8) for fabrication and three point bending test to study their effect on die fracture strength. As die crack are generally observed in the direction perpendicular to die axis between gate and source gap, these two designs investigate the influence of metal width, where the former has thicker metal and the latter has narrow metal width in the direction of crack.

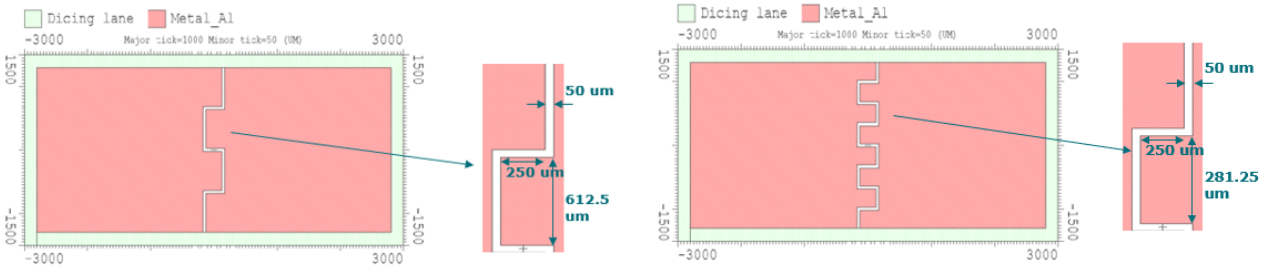


Figure 3.8: *Chip design with different meander layouts for die metallization. The key difference between the two designs is that former has thicker metal between meander fingers compared to the latter.*

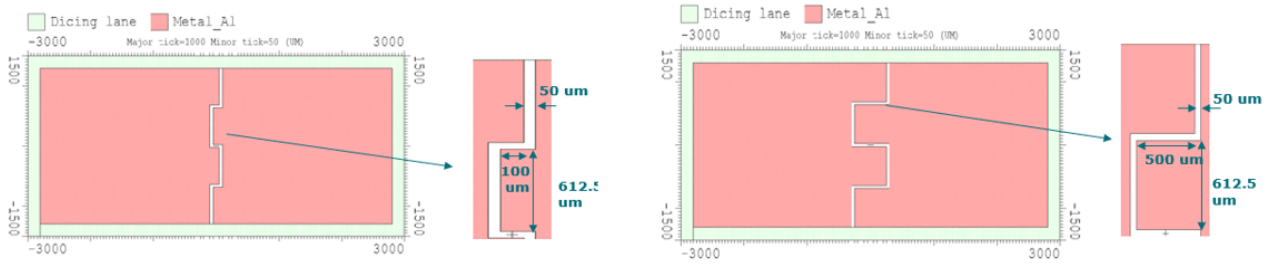


Figure 3.9: *Chip design with additional meander layouts for die metallization. This layout provides better insights for meander design optimization.*

3.3.2. Silicon trench designs

These mask designs are made to pattern the silicon substrate of the wafer. Trenches are deep openings which are filled with suitable material and can stretch over over the entire die. Trenches found in commercial power MOSFET devices were used as reference for designing these trenches. The trenches in the dummy test power MOSFET dies were designed to be 2 μm wide with 5 μm pitch. This allows for enough spacing between the trenches for good resolution in patterning via lithography and etching.

Design modifications

- ◇ The trenches edges were curved using fillet command in L-edit software to avoid any sharp corner in the design (potential crack hot-spots) and also to optimize them for better stress distribution.
- ◇ The total area with trenches cover horizontally, a width of 2 mm out of total 6 mm dies length. The testing area will be central axis of the die and 2 mm is enough to create required sensitivity in die for testing.
- ◇ Trenches do not extend vertically till the dicing lanes. 10 μm space is left unpatterned between the dicing lane and trench. This is to prevent etching or removal of trenches close to dicing lane in the event of material removal from the dicing lane.

- **Mixed Trenches no gap:**

  These mask design is named as Mixed trenches as it contain two different orientation of trenches. Trenches in gate area span in horizontal direction (parallel to die axis) where as trenches in source area span in vertical direction (perpendicular to die axis). The width and pitch of the two design is kept the same that is 2 μm and 5 μm respectively.

  The trenches patterned with this mask design are used as reference trench design to compare with other trench design present in the mask. This trench design is closest to commercial available power MOSFET trench design. In this pattern, the two trench orientation are placed next to each other with a separation gap of < 5 μm between them.

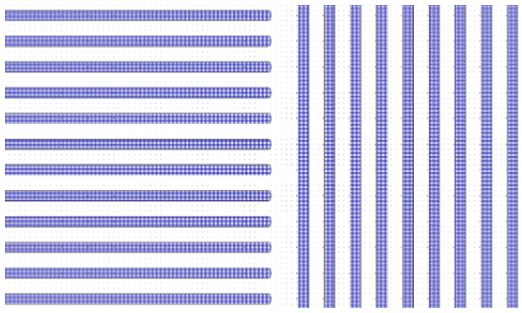


Figure 3.10: *Figure shows trenches with two different orientations inside the chip. This dual trench orientation pattern is also seen in commercial power MOSFET devices.*

- **Mixed Trenches with gap:**

  The trenches in this design are similar to trench design discussed above as it also have trenches in two different orientation. The key difference in this design is the gap between the two different orientation near the middle of die, which is increased to 50 μm (figure3.11). The idea behind the design is to remove the trenches in the area where in metallization step, the metal is absent (no metal gap). This design potentially reduces the sensitivity of die in non-metal area and hence makes the die more robust.

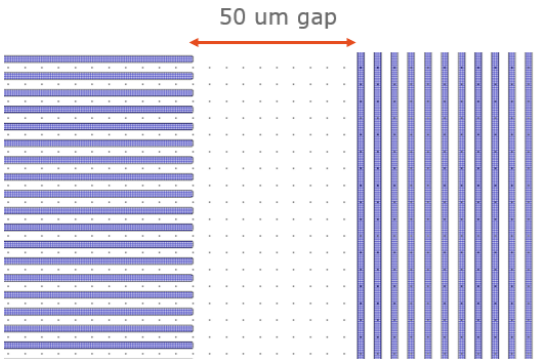


Figure 3.11: *Chip with mixed trench orientation but separated by a 50 μm gap*

- **Vertical Trenches with no gap:**

  In this mask design, we have only unidirectional trenches with vertical spread (perpendicular to the die axis). The same trench layout span across the entire 2 mm middle zone of die, designated for trenches the the mask design. No specific gap is present between the vertical trenches in the gate and source area of the die (figure 3.12). This mask design is used to investigate the die strength of 50 μm thick die with only vertical direction trenches

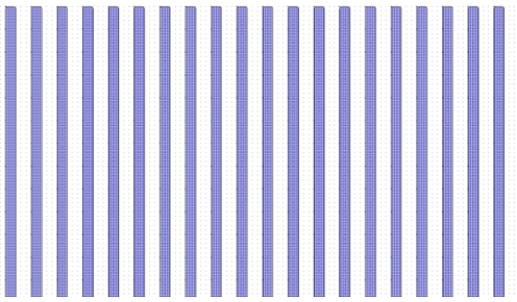


Figure 3.12: *Chip design with only vertically oriented trenches*

- **Horizontal Trenches with no gap:**

  In this mask design, we have only unidirectional trenches with vertical spread (perpendicular to the die axis). The same trench layout span across the entire 2 mm middle zone of die, designated for trenches the the mask design. No specific gap is present between the vertical trenches in the gate and source area of the die (figure 3.20). This mask design is used to investigate the die strength of 50 μm thick die with only vertical direction trenches

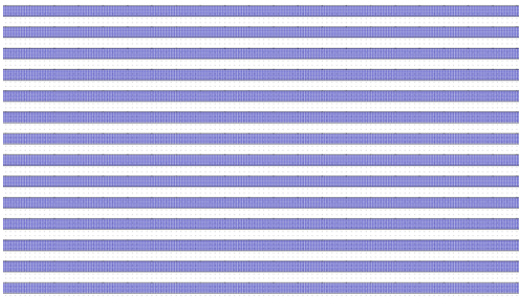


Figure 3.13: *Chip design with only horizontally oriented trenches*

3.3.3. Mask design

All the different mask designs required for patterning the layers for the test chip and other improvement designs are placed in a single mask cell. This mask cell is used for converting the cell into actual mask for lithography. The image seen in 3.14 is mirror image of actual mask layouts (chromium side up versus chromium side down) which was mirrored by mask fabrication software. During mask fabrication the

chromium side of the mask is facing up while at exposure the mask is used with the chromium side down.

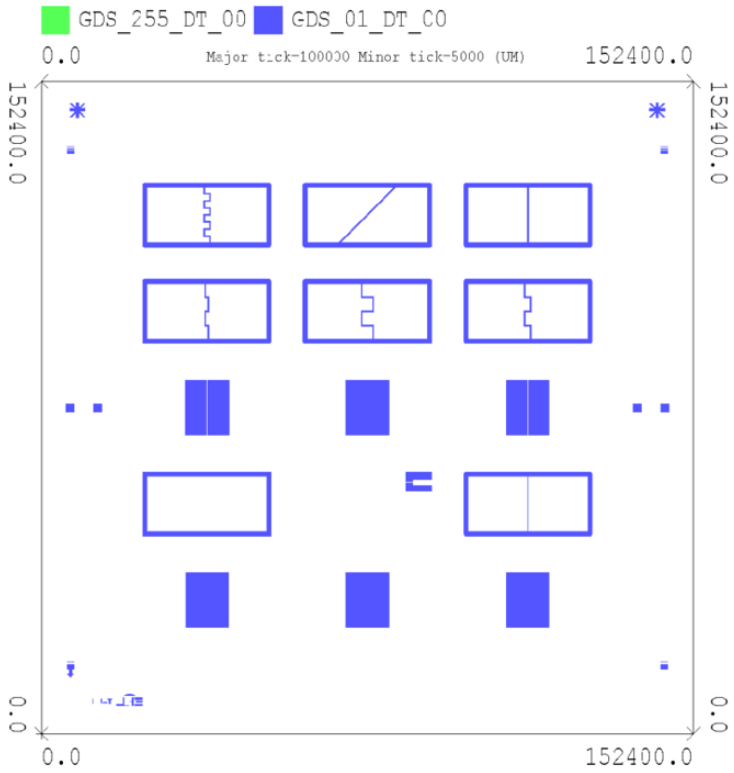


Figure 3.14: *The top cell which consists of all the various mask designs in single mask cell. The first two rows represents different pattern for metal layer. Third and fifth row show masks with different trench orientations.*

Multi image mask exposure job

The ASML wafer-stepper PAS5500 in EKL cleanroom is equipped with a variable rectangular aperture just above the mask (see figure 3.15). The purpose of this aperture is to minimise the illuminated area on the mask to match the image area. The mask blanking system consists of 4 independent programmable blades. The blade positions can be controlled by the exposure job. For the die dimension of 6 X 3 mm, the exposure job allows for 15 different mask designs in one single mask top cell. Each of the design has an image or reticle ID assigned to it which can be called in the exposure job to illuminate the required mask design for exposure on the entire wafer.

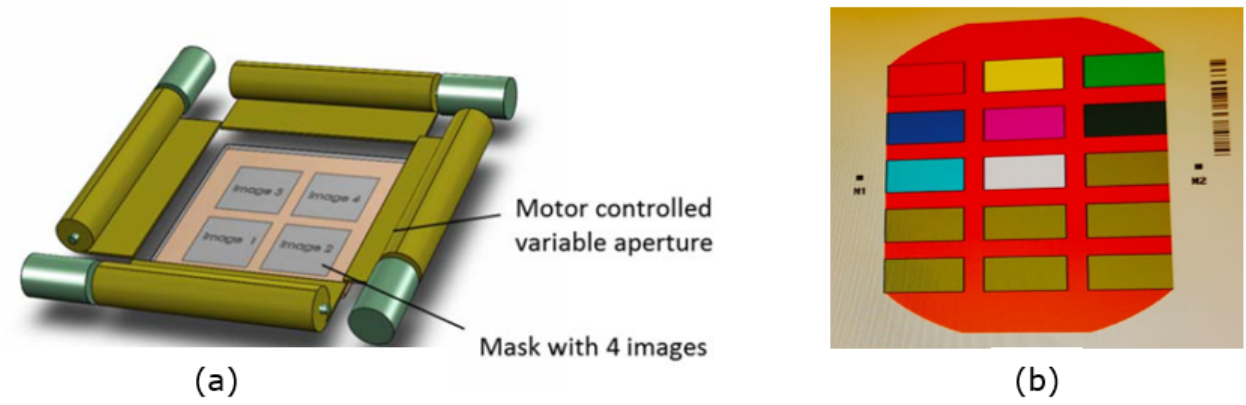


Figure 3.15: *(a) The mask blanking system of the PAS5500/80 waferstepper with 4 images; (b) job for mask blanking system with 15 images.*

3.4. Design of experiments (DOE)

There are numerous chip design possibilities with available metal and trench design on the manufactured mask. A design of experiment (DOE) was formulated to narrow down the design combinations for fabrication process. The DOE is divided into 4 different studies, each study focuses on one design aspect and investigates their influence on ultrathin die robustness. The different studies are listed below:

- Study 1: Investigating effect of layer addition on silicon top
- Study 2: Metal pattern investigation for robust gate
- Study 3: Polyimide for die-top strengthening
- Study 4: Impact of Trench Orientation on die strength improve die strength compared to baseline silicon die.

3.4.1. Study 1: Investigating effect of different material addition on silicon top

- **Bare silicon die - Baseline:** The bare silicon die without any lithography and other subsequent process layers like metal and nitride, serves as baseline chip for comparison with other design specimens. The biggest advantage of this chip is that it provides with valuable insights in how much a die's fracture strength is influenced by new process additions like trenches, metallization, passivation layers, polyimide etc.

Figure 3.16: *The figure shows different die cross-sections with various semiconductor process layers. Die cross-section are namely (a) Si + 4 µm Al die; (b) Si + 6 µm Al die; (c) Si + 4 µm Al + passivation layers; (d) Si + 5 µm PI*

- **Effect of metallization:** This design aims to study the influence of addition of aluminium metal on silicon die top (refer figure a). Aluminium is a commonly used metal for trench power MOSFETs. The metal thickness used for this chip design investigation is 4 μm. It is expected for aluminium metal to improve die strength compared to baseline silicon die.
- **Effect of thicker metallization:** A thicker metal layer is used for this chip design (refer figure b) as compared to design a to study the effect of increase in metal thickness to die strength. The metal thickness used for this chip design investigation is 6 μm
- **Process layers as seen in MOSFET design:** This chip design aims to include all the relevant process layers in standard power MOSFET without any patterns (absence of trenches and metal gap). In figure 3.16 c, different layers included in this chip design are shown
- **Effect of Polyimide:** Polyimide is one of key process layers under investigation on its potentially positive response to overall die strength (increased strength). A thick layer of 5 μm polyimide (Durimide 7520) is deposited on bare silicon die to study its influence on die strength. It is expected for polyimide to improve die strength compared to baseline silicon die.

3.4.2. Study 2: Metal pattern investigation for robust gate

This study aims to investigate different patterns in the metal layer stack (refer figure 3.17). Five different chip designs are selected from the available reticle layouts. One of the layout is use to fabricate the standard test chip (50 μm gap between Gate-Source) which is used as baseline for die strength comparison with other layouts in this study. The trenches used in this design will also be the standard mixed orientation trenches which is horizontally aligned trenches in gate area and vertically aligned trenches in source area as seen in trench MOSFET devices.

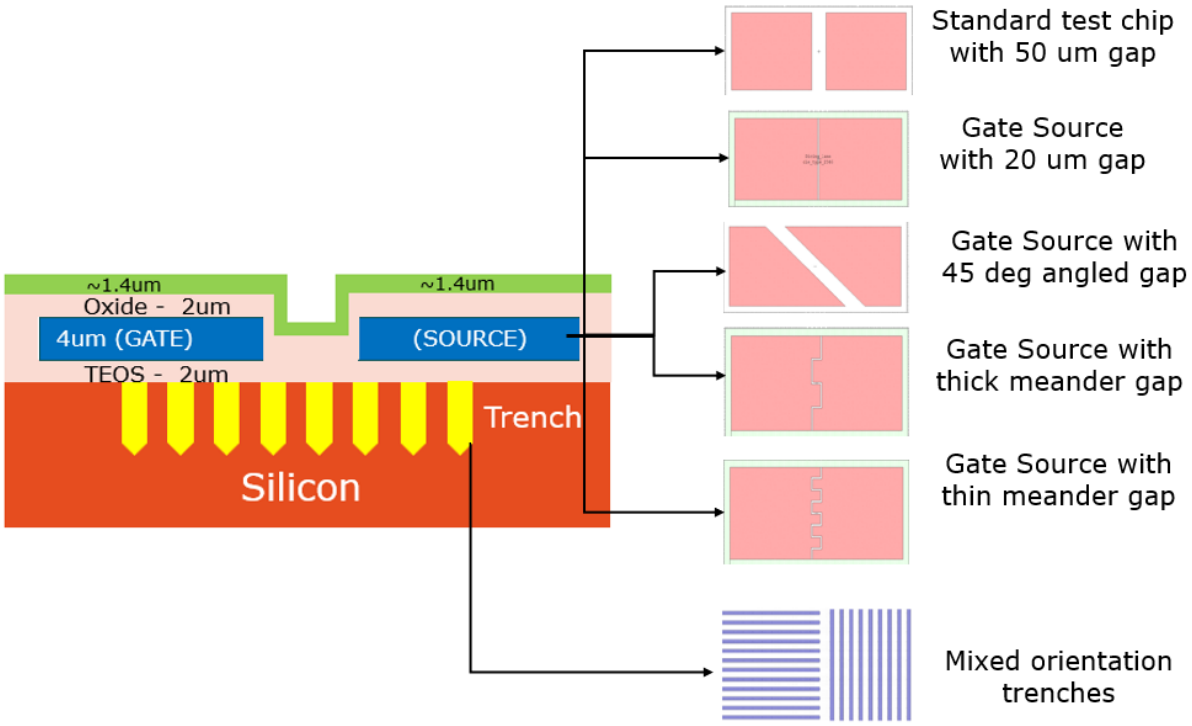


Figure 3.17: *Test chip of 3 x 6 mm, 50 µm thick with different top metal mask designs*

3.4.3. Study 3: Polyimide for die-top strengthening

This study aims to investigate the influence on die robustness by addition of thick polyimide (PI) films on die top (refer to figure3.18). Standard chip design is used as substrate for this addition which has silicon nitride as its topmost layer. Investigation is done for two different PI thickness i.e. 5 μm and 10 μm to also get insights on PI thickness on die strength. PI is relatively lower stiffness material as compared to other underlying layers in the die. For trenches in silicon, two different trench styles are included , (1) with standard mixed orientation trenches where the two trench arrangements are continuous and (2) where trench arrangements have 50 μm gap.

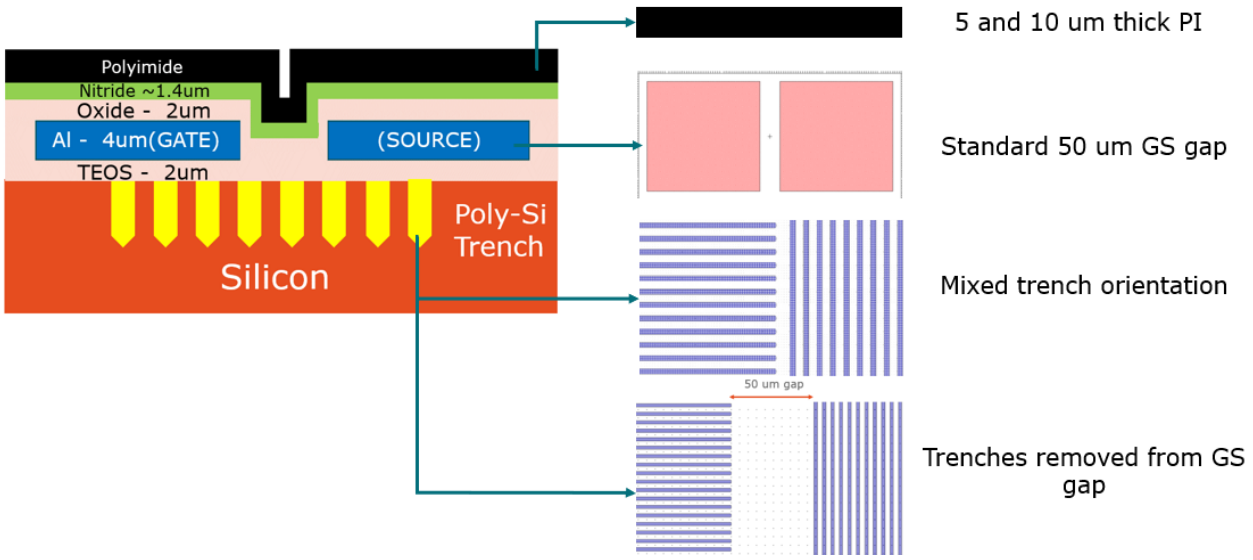


Figure 3.18: *Die cross-section highlighting different trenches and polyimide thickness for investigation*

3.4.4. Study 4: Impact of Trenches and their orientation on die strength

In general, trench MOSFETs have mixed trench orientations which are horizontally and vertically aligned in gate and source area respectively. Trenches bring sensitivity in the chip design because of deep etching of crystalline silicon and its filling. Presence of void in filling may add additional stress and sensitivity in the chip design. It is important to understand the contribution of trenches in the overall stress of the chip and factors leading to its failure during packaging and assembly processes. Two different designs are realised to study and compare their influence on chip design.

- **Vertical trenches:** The source region in trench MOSFETs is the region which hosts vertical trenches. In this study, a chip is designed purely with vertical trenches. Trenches are filled with poly-silicon and covered with aluminium metal for polished surface.

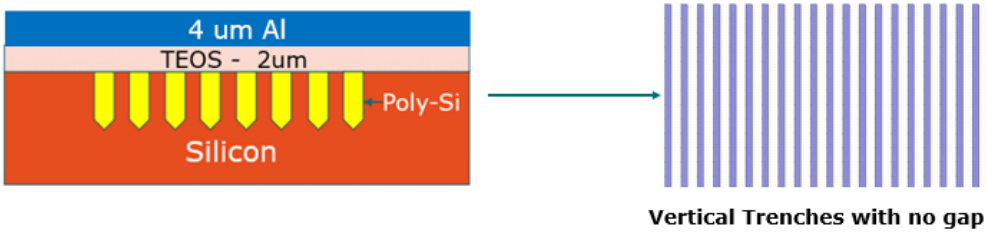


Figure 3.19: *Die cross-section for investigating die strength with only vertical trenches*

- **Horizontal Trenches:** The gate region in trench MOSFETs is the region which hosts horizontally aligned trenches. In this study, a chip is designed purely with horizontal trenches. Trenches are filled with poly-silicon and covered with aluminium metal for polished surface.

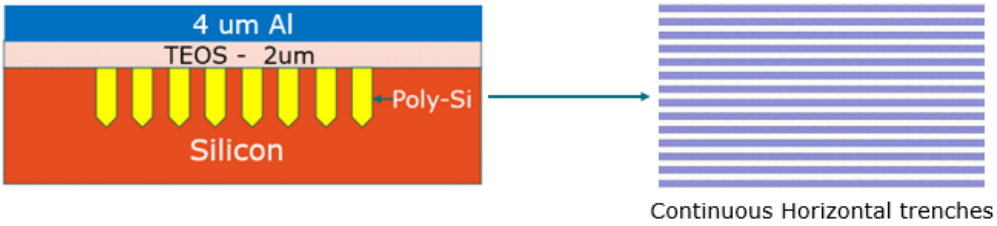


Figure 3.20: *Die cross-section for investigating die strength with only horizontal trenches*

3.5. Chapter summary

In this chapter, different design parameters and considerations for test chip designs are defined. The aim is to improve ultrathin die robustness, for which we introduce a standard test chip which is a close mechanical copy of commercial trench power MOSFET along with many improvement designs (refer to the DOE) to potentially improve die robustness. Four different studies are defined to investigate the effect of different aspects of chip design on die strength namely 1) addition of new layers on silicon; 2) Polyimide for die top; 3) trenches in silicon; 4) die-top metal layer pattern.

4 CLEANROOM FABRICATION OF POWER MOSFETS

4.1. Chapter Introduction

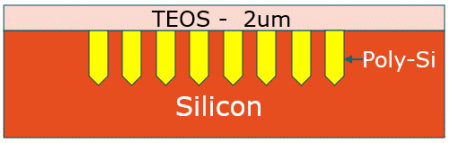
This chapter highlights the key fabrication steps for fabricating dummy power MOSFET design on 100 mm silicon wafers. The fabricated power MOSFET designs are similar to commercially available trench power MOSFETs. Major power MOSFET fabrication challenges like trench layout, profile, wafer warpage are also discussed later in the chapter to highlight key challenges and their plausible solutions in semiconductor manufacturing.

4.2. Fabrication stages

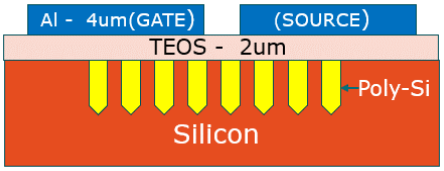
Every fabrication process starts with bare silicon wafers. Single side polished 100 mm diameter n-type silicon wafers with < 1 0 0 > orientation were used for the device fabrication. A process flow highlighting the different fabrication stages for fabricating dummy power MOSFET devices are shown below:

1. Trench formation (ICP-RIE etching with oxide mask)

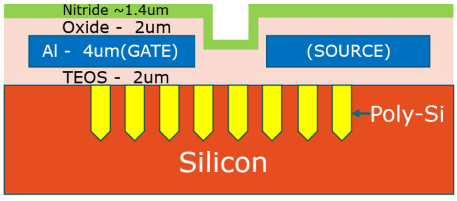
2. Trench poly-silicon filling



3. Die top metallization (Aluminium @350°C)



4. Passivation layers (PECVD Ox + Nitride)



Trenches in Silicon

Trenches are important design parameter of power MOSFET devices as they enable vertical current conductivity from one surface to other surface which allows high current driving capabilities and also help achieve very low drain-source resistance ($R_{DS(on)}$). There can be millions of these trenches in one chip increasing cell packing density [32]. Fabricating these high aspect ratio trenches with desired depth and profile is one of the most challenging and important process steps in achieving high performance trench MOSFETs.

Trenches critically affect not only the performance of a die but also its mechanical robustness. They are essentially grooves etched in silicon substrate and are key hot-spots for crack origination and propagation for thin power MOSFET dies (< 50 μm). In semiconductor process, the fabricated wafers undergo various stages of back-end processing like wafer thinning, dicing, assembly, packaging and at the end operation in

real world scenario. In our processed wafers, trenches play a key role in increasing our dies sensitivity to stress both at the gate and source area. This ensures that the die stress environment is similar to real world stress conditions.

In commercial trench power MOSFETs trenches are arranged in two different orientations. Deep Trenches (snubber trenches) under gate area and shallow trenches (active trenches) across the source area. The arrangement of trenches also depend upon their application area. Gate trenches are aligned parallel to long axis of die (horizontal trenches) in contrast to perpendicular alignment to long axis of die for latter of source trenches (vertical trenches). Based on the DOE as discussed in Chapter 3 , wafers will be fabricated with different trench orientations and layouts to investigate their impact on large thin die mechanical robustness.

4.2.1. Deep silicon trench fabrication

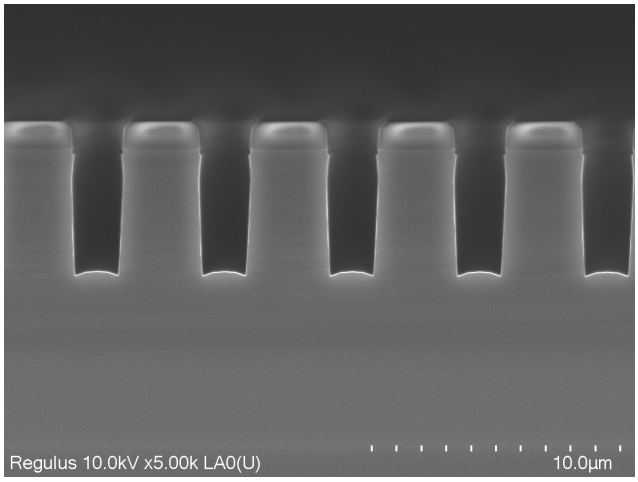
Inductively Coupled Plasma - Reactive Ion Etching etching (ICP-RIE) technique was used to etch trenches in silicon substrate. PECVD Oxide is used as the masking material for trench formation. Trikon Omega 201 tool is used for this etching application where plasma particles are used to etch the silicon in the exposed mask area..

The trenches found in commercial trench power MOSFET are used as reference to create similar trenches in test devices. The trench parameters seen in dummy power MOSFET devices are mentioned in table 4.1. The key design aspects for the trench are the trench width, depth, pitch, profile and material for trench filling. Trench parameters not only affect the electrical performance and efficiency of power MOSFET devices but also their mechanical robustness.

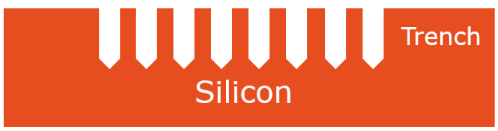
Trench parameter	Comment
Width (w)	2 μm
Height (d)	5 μm
Aspect ratio (d/w)	2.5
Pitch	5
Desired profile	U-shaped
Trench fill	Poly-silicon

Table 4.1: *Trench parameters as seen in dummy power MOSFET devices.*

Figure 4.1 shows SEM image of a wafer cross-section with only trenches. These trenches are ~5 μm deep with aspect ratio 2.5 and are made using Plasma Enhanced Chemical Vapor Deposition (PECVD) oxide hard mask. They have an anisotropically etched profile with slightly tapered walls which supports conformal filling in them.



(a)



(b)

Figure 4.1: *(a) SEM image showing trenches in silicon with leftover oxide mask; (b) Die cross-section with trenches in silicon in the middle region of wafer.*

Fabrication Tip: Use PECVD oxide mask for deep silicon trenches and photoresist mask for shallow trenches (aspect ratio : 1).

4.2.2. Trench filling with poly-silicon

The open trenches are filled inside in order to close them from top. The choice of filling material, trench profile and the deposition technique determines the filling capability of trenches. Trenches found in commercial devices are filled with poly-silicon which is also the choice of filling material for our trenches. The trench filling consists of many process stages as enumerated below

1. The residual oxide mask in the etched trenches are removed by wet chemical etching process. A solution of BHF (7:1) etches away residual silicon oxide selectively without etching the underlying silicon substrate.
2. The outline of trenches are covered with a thin 150 nm PECVD TEOS (gives a navy blue colored layer).
3. Poly-silicon material is filled inside trenches using low pressure chemical vapor deposition (LPCVD) in the furnaces. The 2 μm wide openings are closed from top.

Poly-Silicon is a commonly used as trench MOSFET filling material. LPCVD deposition allows highly conformal layer deposition and minimize void sizes as compared to plasma enhanced depositions (PECVD).

(a) **(b)**

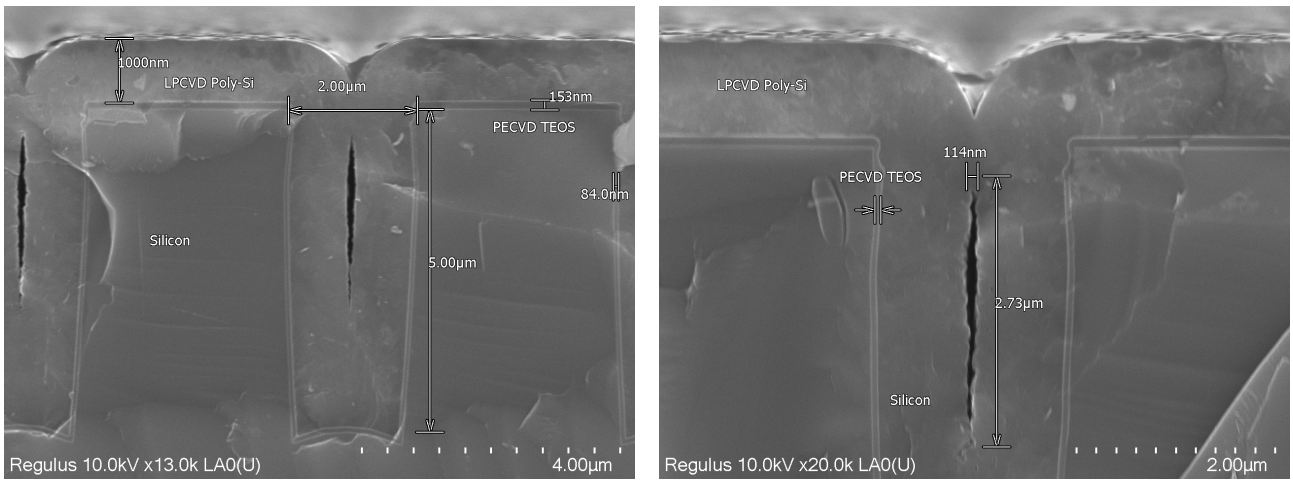
Figure 4.2: *(a) SEM image showing trenches filled with poly-silicon in low pressure deposition; (b) Die cross section showing poly-silicon trench filling.*

In figure 4.3 small voids are observed in SEM observation of wafer cross-section. Even with optimized trench profile and low pressure filling, voids are not completely removed. The void is created because of slight curvature in the upper walls of trench which closes the trench mouth first before it is completely filled with poly-silicon.

Residual Poly-Si removed and oxide cover added

The additional poly-silicon left over in between the trenches over the silicon needs to be etched out. The thin PECVD TEOS layer deposited previously before poly-si filling supports this etch-back process by acting as a stopping layer. The plasma particles have high etch selectivity to poly-silicon as compared to silicon oxide (TEOS) and thus using ICP-RIE etching in Trikon Omega 201, poly-silicon is etched out leaving behind shiny blue coloured TEOS layer underneath. The key applications of thin TEOS layer are enumerated below:

1. TEOS film acts as stopping layer as it prevents the plasma etching of underlying primary silicon substrate. This process is referred as etch back process and is used in all process wafers to remove excessive poly-Si on wafer top.

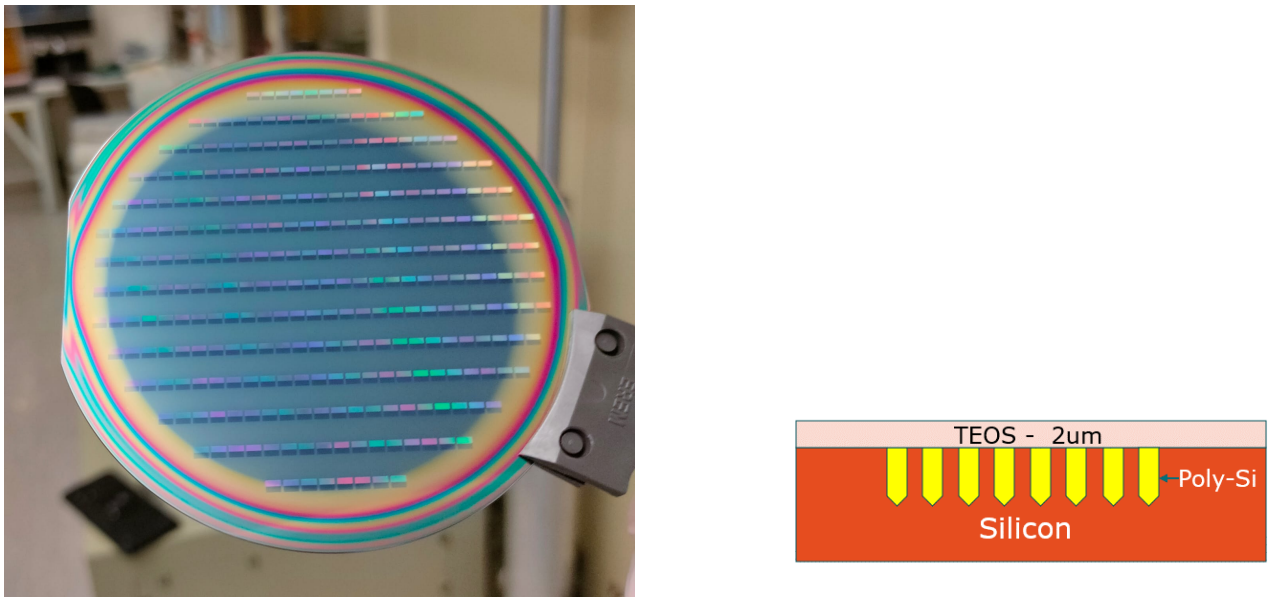


(a) **(b)**

Figure 4.3: *SEM image showing voids inside poly-silicon filled trenches. Residual poly-silicon is also observed on top of silicon substrate in between the trenches.*

2. This thin film also mimics the gate oxide (dielectric) as found in trench gate power MOSFETs.
3. TEOS film makes it easier to distinguish between silicon and poly-si structures in SEM trench observations.

The wafers are then covered with a 2 μm thick layer of TEOS using PECVD method. This deposition covers the trench tops and insulates the trenches from metal layer deposition in subsequent process step (Refer figure 4.4b)



(a) **(b)**

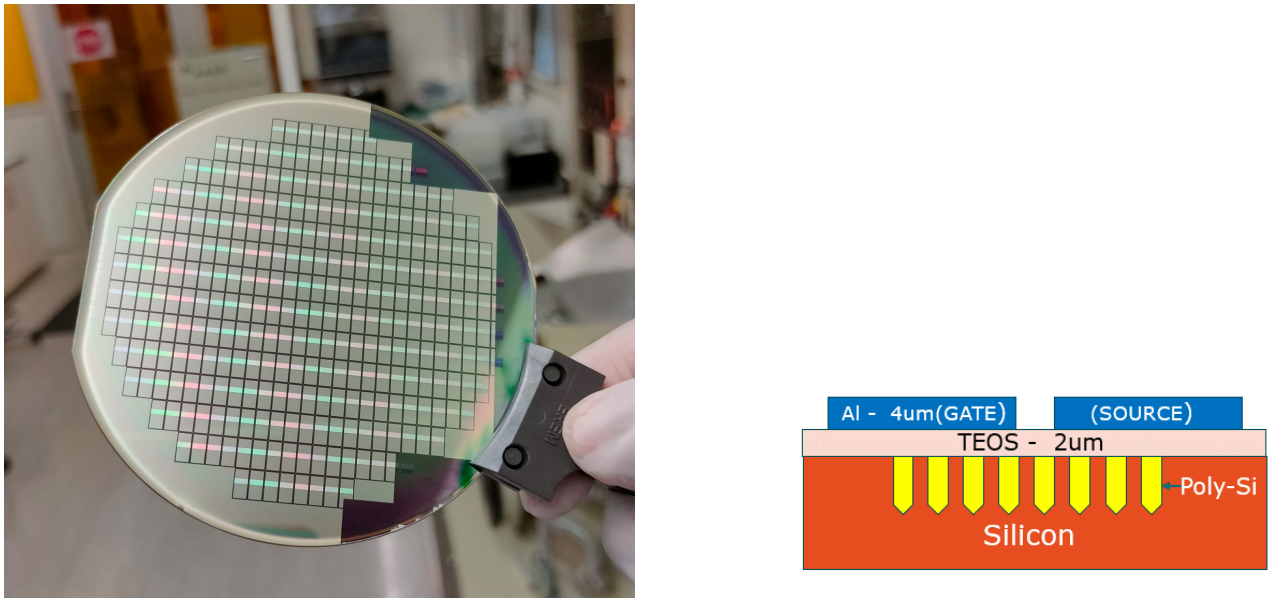
Figure 4.4: *(a) LPCVD Poly-Si etched back using ICP-RIE etcher using 150 nm TEOS as stopping layer; (b) Die cross-section after the process step.*

Fabrication Tip: In poly-si back-etch process, etch the poly-si until shiny blue color is observed on wafer top. In figure 4.4a, wafer middle section can be seen displaying the navy blue color from TEOS indicating the successful poly-silicon etch back process. It is to be noted that plasma etching action of Trikon Omega 201 tool was found to be more uniform in the middle section of wafer, compared to the wafer edges. 4.4a.

4.2.3. Die top metallization with aluminium

The next stage in the process is deposition and patterning of metal layer. Pure aluminium layer is used for the deposition. AlSi is another material that can also be used for this process. A 4 μm thick pure aluminium was deposited using Trikon Sigma 204 tool at a temperature of 350°C. The aluminium sputtered at higher temperature (350°C) offers better stress handling capability as compared to lower temperature sputtering recipes (50°C). The best way to distinguish between the high and low temperature aluminium depositions is by their grain size where the former has bigger grains than the latter.

After a layer of pure aluminium is deposited, the wafers are subjected to the process of lithography to obtain the desired gate - source metal pattern from the available 8 patterns as discussed previously in the DOE in chapter 3. The process steps involved in the patterning process includes wafer photoresist coating, UV light exposure to develop the photoresist mask in desired pattern using ASML wafer-stepper, developing the exposed wafer, etching the pattern using plasma etcher (Trikon Omega 201) and lastly stripping the residual photoresist to obtain patterned metal layer. The completed wafer from this process stage can be seen in figure 4.5a



(a) **(b)**

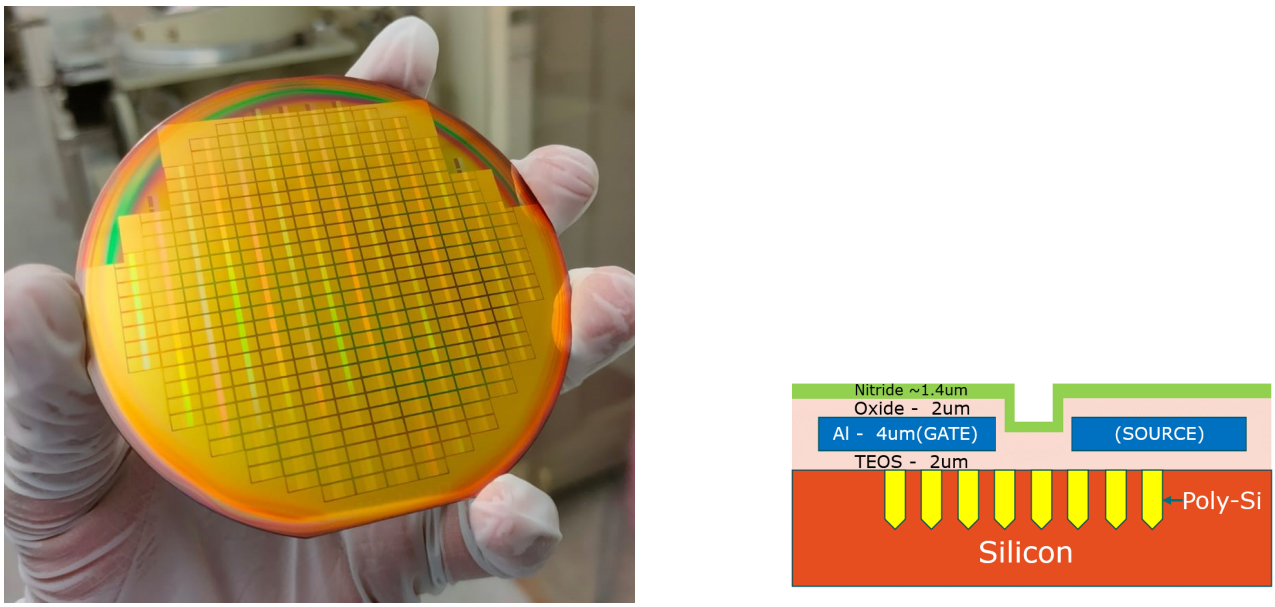
Figure 4.5: *(a) Pure aluminium deposited and patterned in desired gate-source layout; (b) Die cross-section post die-top metallization step.*

Fabrication Tip: The small feature size of metal patterns on wafer create end-point detection error during metal pattern etching in Trikon Omega 201. Expose an additional half ring structure during he lithography step. This increases the total wafer etching area and thus supporting end-point detection.

4.2.4. Passivation layers

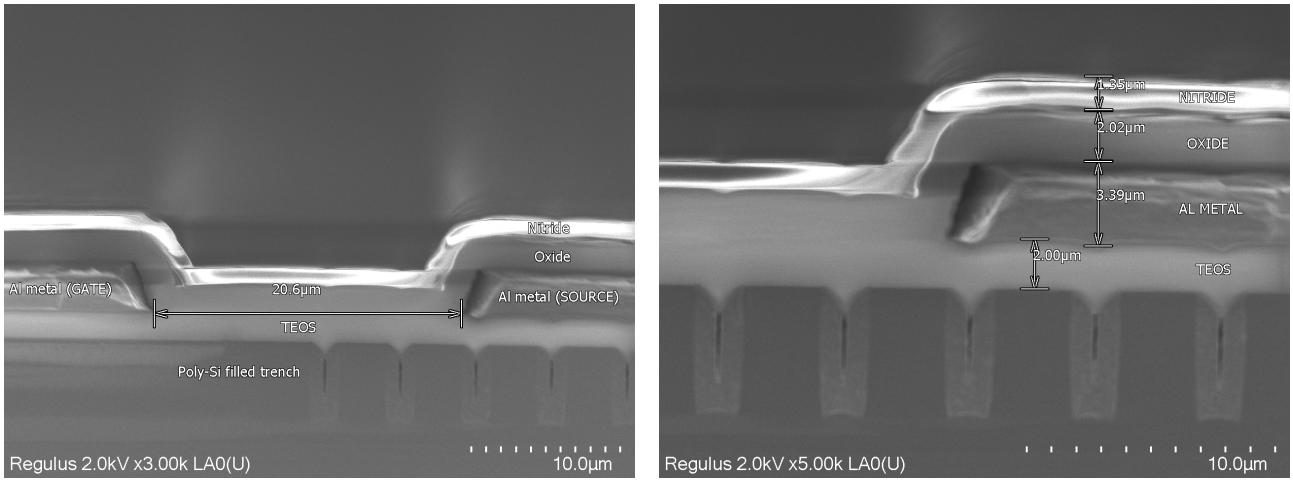
The next process step in power MOSFET device fabrication was deposition of passivation layers like silicon oxide and silicon nitride on the top of patterned metal layer. A 2 μm silicon oxide layer is followed by 1.4 μm nitride layer are deposited using PECVD deposition technique and was performed using the Novellus concept 1 tool. The PECVD allows deposition of films like silicon oxide and nitride at lower temperatures (~ 400°C) to prevent the melting of aluminium layer beneath as compared to other methods like LPCVD which uses higher temperature for film deposition.

The wafer where the aluminium layer pattern is that of standard 50 μm gap between the Gate-Source metal is referred as our reference dummy power MOSFET. The silicon nitride layer on die top is used commonly in semiconductor devices as a scratch protection film and also to enhance device mechanical robustness. The wafer and its cross-section can be seen in the figures 4.6a, 4.7a.



(a) **(b)**

Figure 4.6: *(a) Processed wafer with dummy Power MOSFET dies similar to commercial trench power MOSFET dies; (b) Die cross-section post passivation layer deposition. This cross-section i*



(a) **(b)**

Figure 4.7: *(a) SEM image showing dummy Power MOSFET cross-section which is similar to commercial trench power MOSFET device cross-section; (b) A close-up SEM image showing different process layers and their thicknesses in test wafers.*

4.2.5. Polyimide processing

Polyimide film (PI) is processed on top of nitride film. The idea is to use thick polyimide film as mechanical buffer to improve die frontside strength. Durimide 7520 PI by Fujifilm is an ideal candidate for this application as it offers good properties and processibility. Key properties of Durimide 7520 are listed in table below:

Properties	Value	Unit
Tensile strength	215	MPa
Young's modulus	2.5	GPa
Glass transition Temperature	285	°C
Film thickness	3-40	μm
Coefficient of thermal expansion	55	ppm/°C
Developer	HTRD2/RER600	

Table 4.2: *Cured Film Properties of Durimide 7520*

The polyimide was deposited using spin-coating technique. The final thickness of polyimide is determined by the spin speed of the coating stage. The spin speeds were adjusted to obtain the desired thickness of 5 μm and 10 μm to that of 3600 RPM and 2000 RPM respectively. The Durimide 7520 deposition process is as follows

1. **Spin coating:** The wafer is loaded on spinning plate. Durimide 7520 is poured on top of wafer to make a circular coin shape. The wafer is spin at 3600 RPM to spread the polymer and achieve the desired thickness of 5.
2. **Soft baking:** The wafer is loaded on hot plate at 100 °C and baked for 3 minutes.
3. **Wafer Curing:** Post baking, wafer is loaded in Koyo curing oven where the wafer is cured at 350° C for 1 hour duration.
4. **Annealing:** The cured wafer is annealed in oven at 150 °C for 3 hour duration. This step allows to relive stress in PI layer introduced from its shrinkage during rapid curing process.

The film thickness of cured PI film is determined using Dektak profilometer. The thickness of PI film post spinning and baking is higher than cured PI thickness. The film shrinks to upto 45 % during the curing process to allow cross-linking of polymer bonds to achieve PI hardening [12].

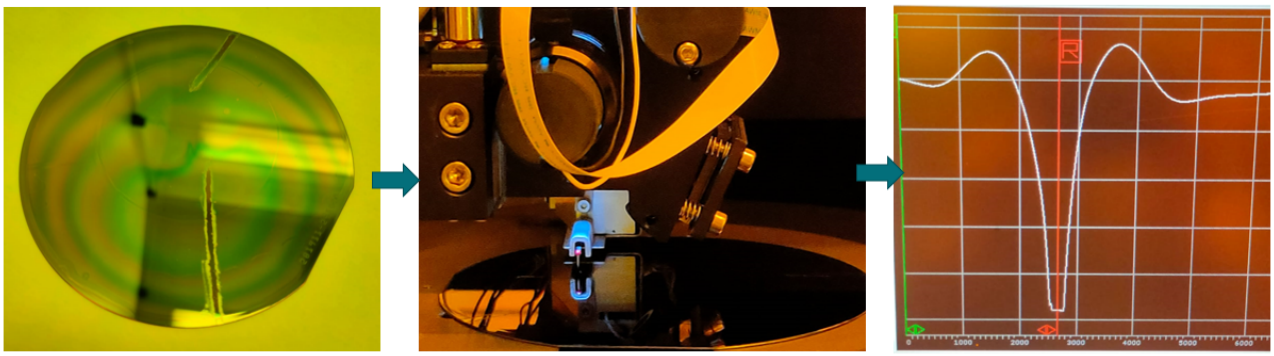


Figure 4.8: *Figure (a) PI is removed in a vertical line using acetone; (b) PI thickness measured using Dektak profilometer; (c) Graph showing difference between PI covered and uncovered region;*

Fabrication Tip: Use low spinning duration for the coating step. Higher spinning duration results in fast cooling of polyimide layer and leaving a circular ring print on the wafer top.

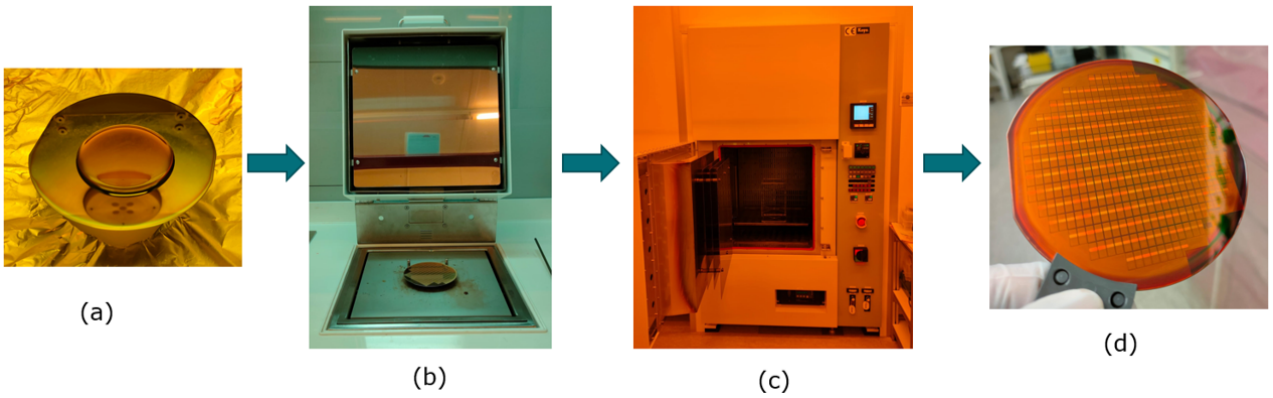


Figure 4.9: *Figure (a) shows polyimide on top of wafer for spin coating; (b) shows soft baking of polyimide on hot-plate; (c) Curing of wafer with polyimide post baking; (d) wafer with polyimide on top*

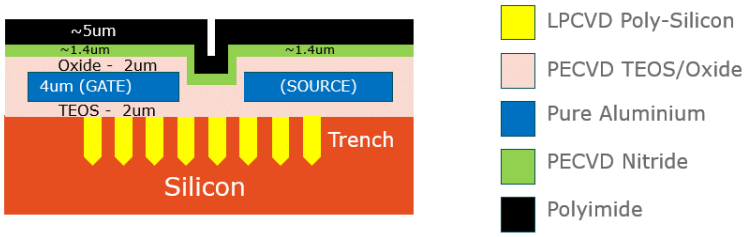
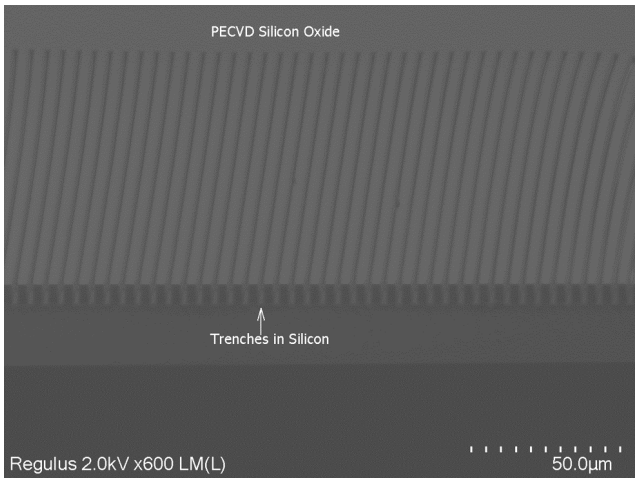


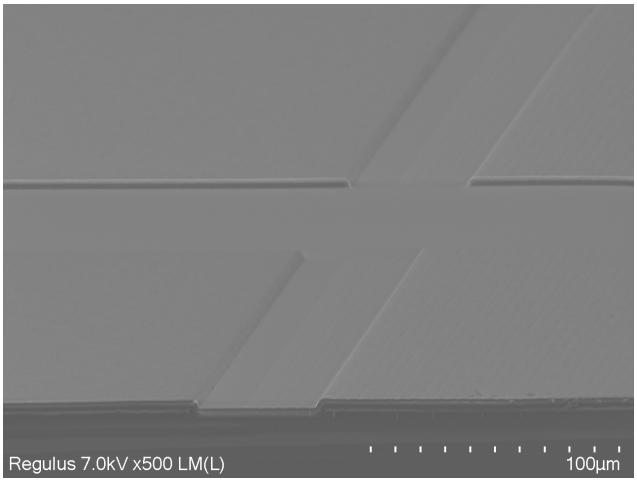
Figure 4.10: *Die cross-section with different process layers*

4.3. Silicon trench fabrication analysis: Challenges and Solutions

Trenches are patterned into silicon substrate using lithography. The ASML wafer-stepper was used for patterning the silicon. The wafer goes through steps of positive photoresist coating, exposure with desired trench design in reticle followed by developing process. The developed wafer is then plasma etched where the plasma radicals etch through exposed silicon material. This step is followed by plasma stripping to remove left over photoresist to obtain the trench in Silicon. The equipment used for the etching process is Trikon Omega 201 ICP-RIE (Inductively Coupled Plasma - Reactive Ion Etching) etcher. The etching selectivity of plasma radicals for SPR photoresist to silicon was determined in a separate test run to prevent over etching and damage to the silicon substrate underneath.



(a) *Trenches seen in wafer cross-section loaded in SEM. Trenches are filled with Poly-Si and covered with oxide.*



(b) *Step height seen in middle of die cross-section due to absence of metal layer between gate and source regions*

Figure 4.11: *SEM images of wafer cross-section with trenches*

4.3.1. New process recipes for silicon trench etching

The most challenging part of power MOSFET device fabrication is trench etching. In the absence of trench etch recipe, new recipe was formulated where key process parameters like pressure, gas flows, masks were investigated. The final goal was to obtain trenches similar to trenches found in commercial trench MOSFET devices i.e. high aspect ratio (> 2.5), straight walls, rounded bottom, high etch selectivity.

In this subsection, various trench etching test runs and key observations from the tests are discussed. For process simplification the plasma etch power and pressure were not changed. The etching recipes with very low process pressure were selected for reference as low pressure rates are suitable for anisotropic etching. High selectivity with masking layer allows for deeper trenches with thin masks which provides better lithography resolution and also support semiconductor applications where deeper trenches are required. Slightly tapered anisotropic trench profile allows for more conformal filling of trenches to prevent formation of voids. Two different masking materials are tested i.e. photoresist mask (soft mask) and PECVD oxide mask (hard mask).

The finished process wafer is observed under SEM to observe th effect of change in process parameters on trench profile, aspect ratio, etch selectivity. The SEM used for the observations is Hitachi Regulus 8230 Scanning Electron Microscope (SEM). The wafer is cleaved using a diamond tip tool to cleave the <100> silicon orientation orthogonally to trench layout as shown in figure 4.12 . The obtained cleave in attached to support clamp and observed under SEM.

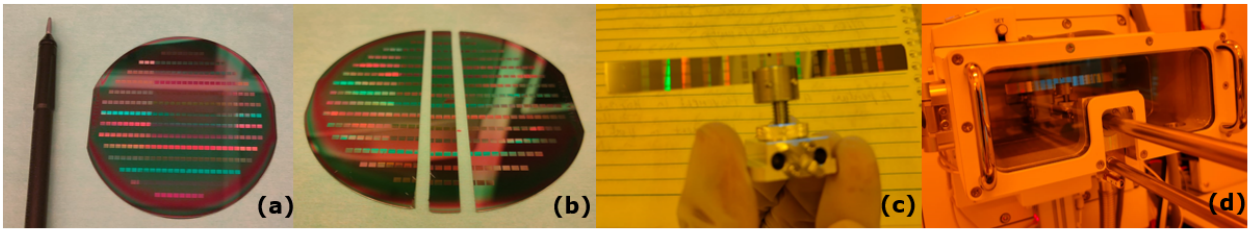


Figure 4.12: *(a) shows <100> wafer with diamond tip tool for cleaving, (b) cleaved wafer with a thin wafer strip, (c) shows thin wafer strip attached to the clamp, (d) shows loading of clamped wafer strip in SEM tool*

4.3.2. Trenches with photoresist mask

Photoresist mask is a standard masking material for patterning process layers in semiconductor manufacturing. The performance of this masking material was tested to create high aspect ration trenches. In the first test run, a 3 μm thick photoresist mask was used in combination with fluorine plasma radicals to etch into silicon to create trenches in silicon. Table 4.3 shows different process parameters and observed results from the etching recipe.

Process Parameters	
ICP-RIE etch recipe	Deep_Si @20
Mask material	3.1 μm Photoresist
Etch time (mm:ss)	1:40
Temperature (C)	20 ± 3
Pressure (mT)	10 ± 10 %
RF Power (Watts)	15 ± 10 %
ICP-RIE Power (Watts)	500 ± 25 %
Gases (Fluorine Chemistry)	
HBr sccm	40 ± 10 %
Oxygen sccm	20 ± 10 %
SF6 sccm	20 ± 10 %

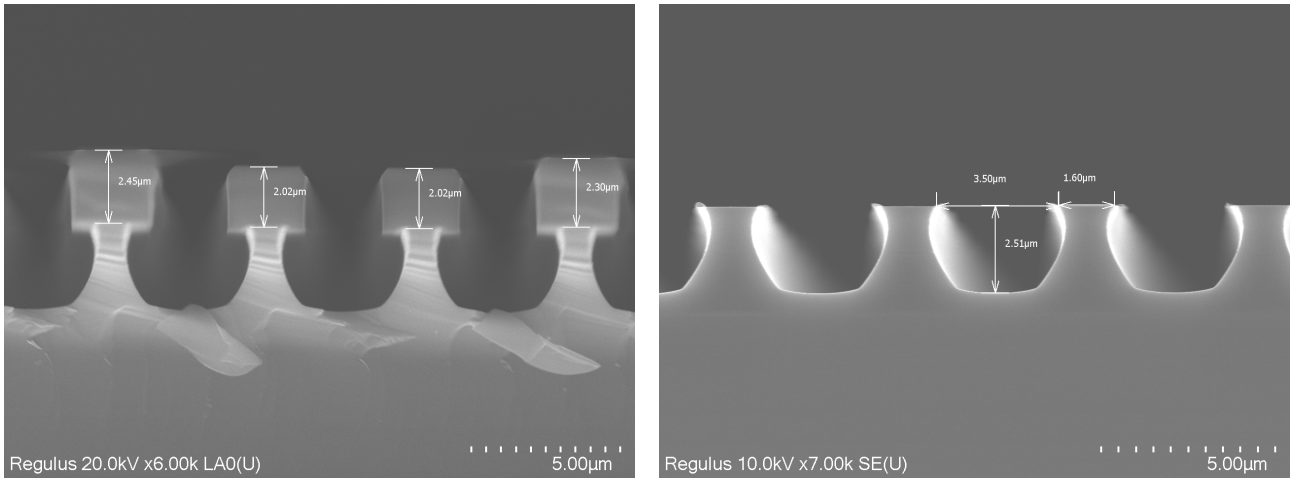
(a) *Different parameters used for processing test run 1*

Results	
Selectivity (Si to P.R.)	2.57
Depth (d)	2.5 μm
Width (w)	3.5 μm
Aspect Ratio (d/w)	0.73
Etch rate	1.79 μm/min
Profile	Rejected (isotropic)

(b) *Observed results for test run 1*

Table 4.3: *Test run 1 for trench etch recipe development*

In the SEM analysis for trench profile (refer figure 4.13), trenches were found to be isotropically isotropically etched with half of the desired depth (2.5 μm). This was due to isotropic etching action by fluorine radicals [6]. The advantage of this method is that it has a fast silicon etch rate at the cost of trench profile and poor photoresist selectivity and thus trench test 1 process parameters were rejected.

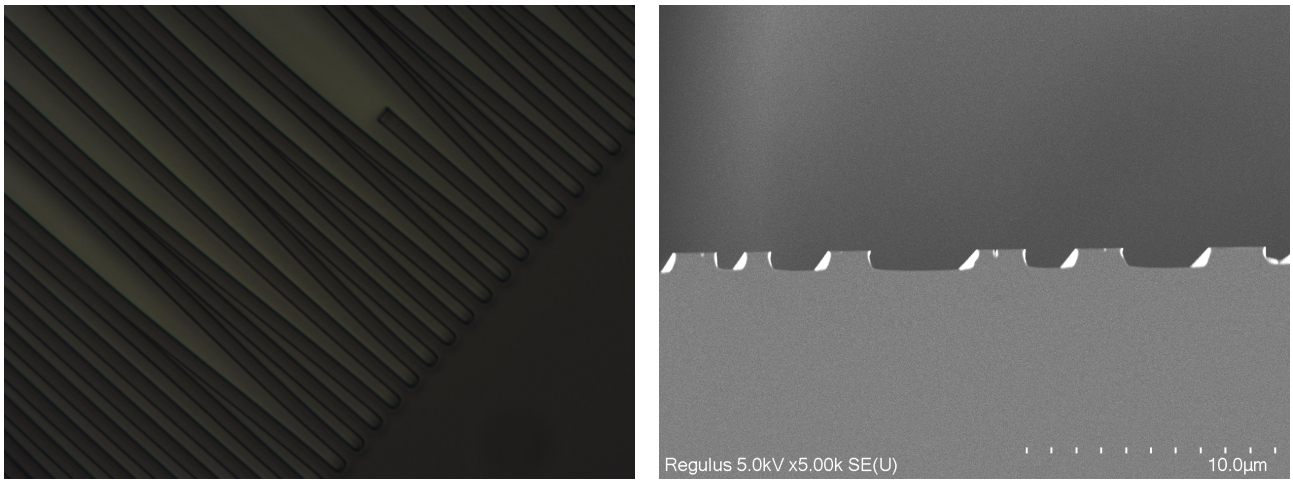


(a) *The SEM image of trenches obtained using Deep Si etch recipe. The square blocks are the leftover photoresist mask*

(b) *Magnified SEM image of trench obtained using Deep Si etch recipe with photoresist stripped.*

Figure 4.13: *SEM observations for trenches obtained with test run 1*

It was also observed that adhesion between the photoresist and silicon plays an important role for patterning high resolution trench patterns in lithography process. Hexamethyldisilazane (HMDS) coating is used to facilitate good adhesion to realise high resolution patterns. Inconsistent HMDS application was found to have drastic effect on trench resolution as shown in figure 4.14a, 4.14b.



(a) *Bad trench resolution due to bad HMDS adhesion*

(b) *Irregular trench shapes due to bad HMDS adhesion*

Figure 4.14: *HMDS adhesion issue with wafer development leading to bad trench resolution*

Trench test 2

In the second test run, fluorine gas was replaced by chlorine gas for the etching process. Etching action of chlorine radicals is relatively more anisotropic than fluorine radicals in silicon etching but at the cost of a slower etch process. The test was conducted using the process parameters as mentioned in the table 4.4a and etched results are listed in table 4.4b.

The wafer fabricated with above etch parameters was cleaved for SEM analysis. The trenches in the wafer were found to have a tapered profile with poor aspect ratio and selectivity (refer figures 4.15. The biggest disadvantage of this etch recipe is its slow silicon etch rate. The etch time required for achieving a 5 μm

Process Parameters	
ICP-RIE etch recipe	Si_Bulk
Mask material	3.1 μm photoresist
Etch time (mm:ss)	15 min
Temperature (C)	20 ± 4
Pressure (mT)	60 ± 10 %
RF Power (Watts)	20 ± 10 %
ICP-RIE Power (Watts)	500 ± 25 %
Gases (Chlorine Chemistry)	
HBr sccm	40 ± 10 %
Chlorine sccm	80 ± 10 %

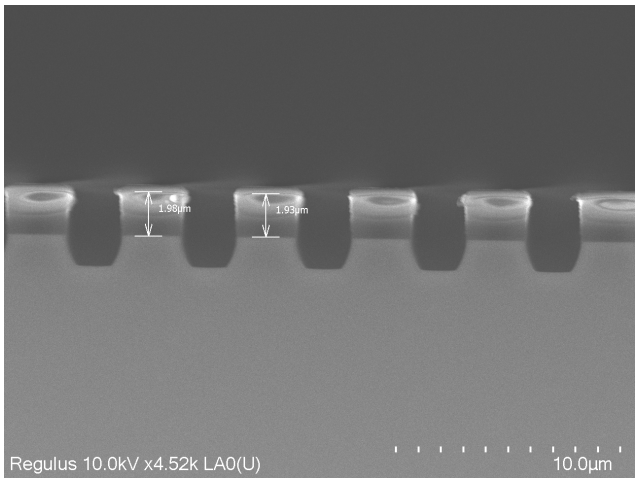
(a) *Different parameters used for Test run 2*

Results	
Selectivity (Si to P.R.)	1.22
Depth (d)	1.35 μm
Width (w)	2.45 μm
Aspect Ratio (d/w)	0.55
Etch rate	0.09 μm/min
Profile	Rejected (slow process)

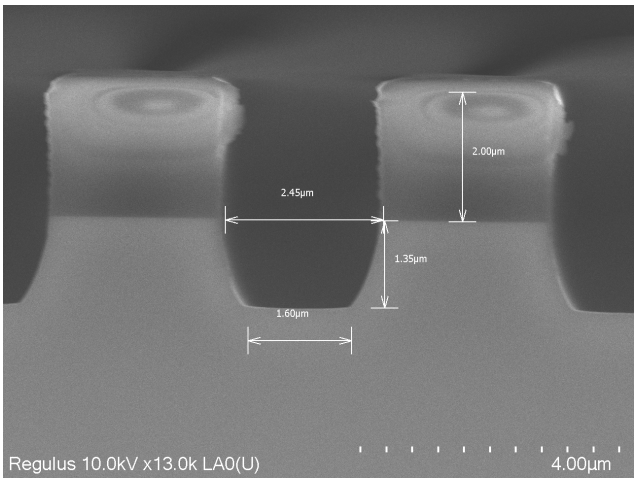
(b) *Observed results for test run 2*

Table 4.4: *Test run 2 for trench etch recipe development.*

trench depth is greater than 1 hour per wafer which is not desired in a high throughput semiconductor manufacturing. Thus trench test 2 process parameters were rejected.



(a) *SEM image of trenches obtained using Si Bulk etch recipe. The square blocks are the leftover photoresist mask.*



(b) *Magnified SEM image of shallow trench obtained using Si Bulk etch recipe*

Figure 4.15: *SEM observations for trenches obtained with test run 2*

Trench test 3

In the third silicon etch test, new process parameters are applied as mentioned in the table 4.5a where process temperature and RF power is increased and process pressure is decreased. The recipe is derived from an existing recipe to pattern different silicon waveguides. The result were anisotropically etched shallow trenches with tapered profile with an aspect ratio close to 1 (refer table 4.5b). This recipe was also found to etch photoresist considerably not just in vertical direction but also in the lateral direction (see figure 4.16). The amount of photoresist mask thickness thus required to obtain a depth of 5 μm is quite high (> 6 μm resist) which can affect the lithography resolution for small feature designs and thus test run 3 result was rejected for deep trench etching but was found ideal for shallow trench fabrication because of tapered anisotropic profile which is ideal to fill void free trenches.

Process Parameters	
ICP-RIE etch recipe	SI_WG
Mask material	3.1 μm Photoresist
Etch time (mm:ss)	5 min
Temperature (C)	25 ± 5
Pressure (mT)	5 ± 10 %
RF Power (Watts)	40 ± 10 %
ICP-RIE Power (Watts)	500 ± 25 %
Gases (Chlorine Chemistry)	
HBr sccm	40 ± 10 %
Chlorine sccm	30 ± 10 %

(a) *Different parameters used for test 3*

Results	
Selectivity (Si to P.R.)	Bad (lateral P.R. etch)
Depth (d)	2.30 μm
Width (w)	2.53 μm
Aspect Ratio (d/w)	~0.9
Etch rate	0.46 μm/min
Profile	Ideal for shallow trenches

(b) *Observed results after processing*

Table 4.5: *Test run 3 for trench etch recipe development.*

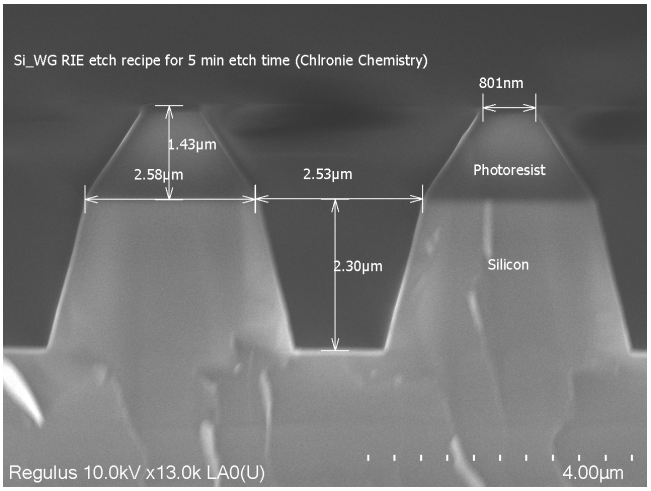


Figure 4.16: *The SEM image of tapered shallow trenches as obtained from recipe Si_WG (test run 3). The pyramid blocks are leftover photoresist post etching*

4.3.3. Trenches with PECVD oxide mask

Silicon etch recipes with photoresist mask were found ideal for shallow trenches but not for deeper trenches (> 5 μm depth). The key drawbacks observed from using photoresist mask were poor etching selectivity to silicon, etch profile etc. In this section, challenges and solutions for obtaining high aspect ratio deep trenches using silicon oxide mask are discussed.

The silicon oxide mask also referred as hard mask is a patterned oxide layer which can be used as a mask to transfer pattern in other process layers. The oxide mask is created by a series of process steps as listed below:

1. Plasma enhanced chemical vapor deposition (PECVD) deposition of 2 μm silicon oxide using Novellus concept tool on silicon wafers.
2. This is followed by a 1.4 μm positive photoresist coating. The wafer then goes through stages of lithography to pattern the photoresist layer.
3. The exposed oxide areas on the wafer are etched out using Drytek Triode 384T tool.
4. The residual photoresist mask is stripped away using plasma in Tepla tool.
5. The patterned oxide acts as thew new mask for etching pattern in silicon like trenches

Figure 4.17 shows different stages in making PECVD oxide mask using die-cross-sections.

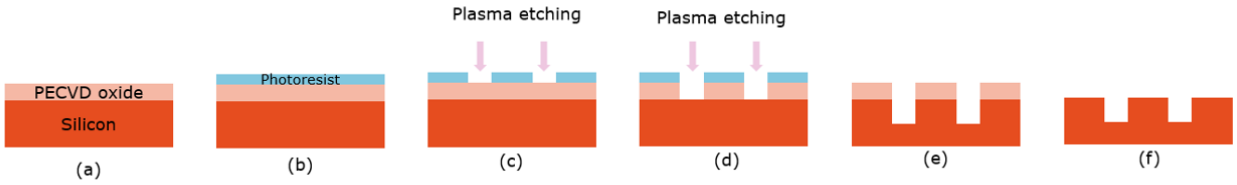


Figure 4.17: *The above figure shows different stages for making trenches using oxide based mask.(a) Silane based oxide deposited using PECVD. (b) Photoresist coated on top of oxide. (c) Photoresist layer patterned using lithography and then exposed oxide area etched using plasma etching. (d) Silicon etched using patterned oxide mask. (e) Residual oxide mask to be remove using BHF chemical solution (f) Final patterned silicon die*

Trench test 4

Based on results from etching with photoresist mask, the same etch recipe namely SI_WG was for etching with PECVD oxide mask. The etching was performed for two different etch times of 5 min (1) and 8 min (2) to analyze the influence of time on silicon etch results. The process parameters and obtained etch results are listed in table 4.6 below.

Process Parameters	
ICP-RIE etch recipe	SI_WG
Mask material	2 μm PECVD Oxide
Etch time (mm:ss)	5 / 8 min
Temperature (C)	25 ± 5
Pressure (mT)	5 ± 10 %
RF Power (Watts)	40 ± 10 %
ICP-RIE Power (Watts)	500 ± 25 %
Gases (Chlorine Chemistry)	
HBr sccm	40 ± 10 %
Chlorine sccm	30 ± 10 %

(a) *Different parameters used for processing*

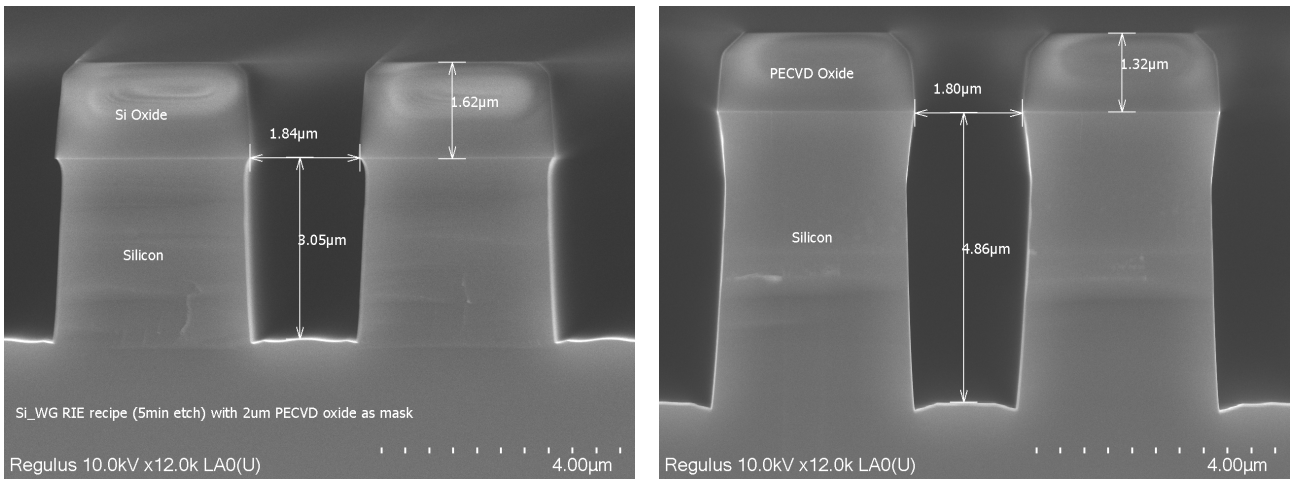
Results	
Selectivity (Si to Oxide)	~8
Depth (d)	3 / 4.86 μm
Width (w)	1.84 / 1.8 μm
Aspect Ratio (d/w)	1.65 /2.7
Etch rate	0.6 μm/min
Profile	Anisotropic (Straight)

(b) *Observed results after processing*

Table 4.6: *Test run 4 for trench etch recipe development.*

Trench profiles observed in SEM for process parameters discussed above are shown in figures 4.18a and 4.18b. The results indicate a clear influence of plasma etch time on trench profile especially at the trench bottom. A flatter trench bottoms was obtained with a shorter etch time of 5 min as compared to 8 min etch time where small microtrenches were observed at trench bottom. The trench profile have desired traits like slightly sloped sidewalls which supports void-free trench filling and high silicon to oxide etch selectivity which allows for even deeper trenches in silicon to obtain high aspect ratio trench designs.

The major drawback observed from this etch process was hanging silicon grooves near the trench top. In both the trench profiles, the width of etched trench were found lower than the 2 μm width designed in the mask reticle. This hanging groove can potentially prevent conformal filling of trenches and leave big voids in middle. It was required to remove the protruding silicon sidewalls for better trench filling as discussed in the next process test.



(a) *The SEM image of trenches with a 5 min ICP-RIE etch time. The profile has flat bottom and straight side-walls*

(b) *The SEM image of trenches with a 5 min ICP-RIE etch time. Sidewall hanging is observed on trench top.*

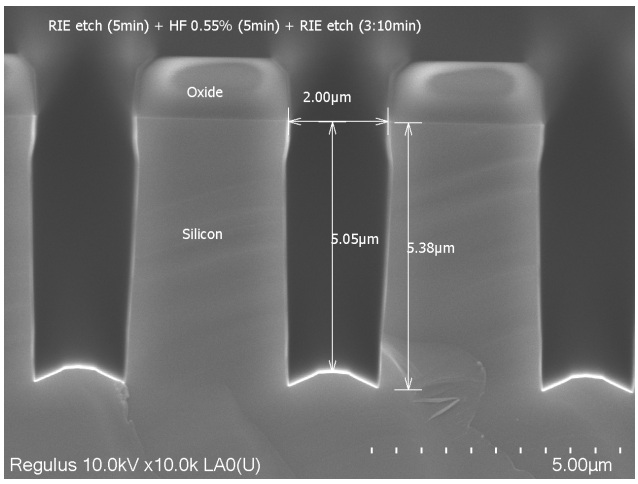
Figure 4.18: *The SEM image for trenches obtained by using Si_WG recipe with PECVD oxide mask for two different etch times (a) 5 min etch; (b) 8 min etch*

Trench test 5

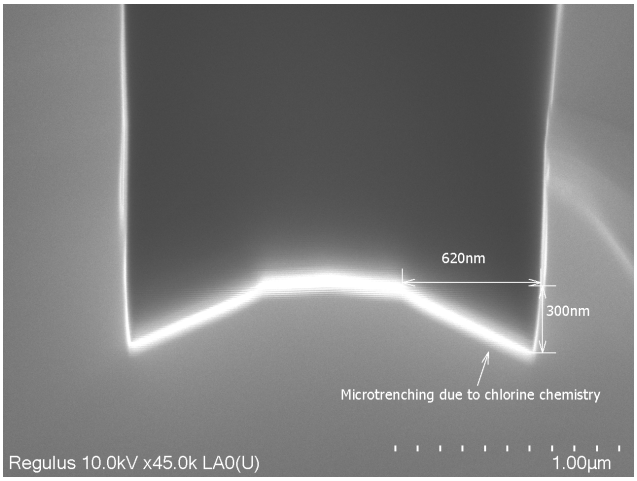
A 8 min etch time has been found ideal for obtaining desired trench depth of 5 μm. In order to obtain the desired trench width of 2 um, it was required to remove the hanging silicon sidewalls near trench top. The etching process was split in three stages to remove or reduce the effect of silicon sidewall on trench width as mentioned below:

1. 5 min ICP-RIE etch time which is two-third of the total etch time (8min 10 sec) was performed in first stage.
2. 5 min wet etch of samples using Hydrofluoric (HF) solution of 0.55 % to isotropically etch silicon oxide. This step removes ~ 100 - 200 nm of silicon oxide mask near trench groove from each side.
3. Remaining one-third of ICP-RIE etch time (3 min : 10 sec) was performed in last stage. The now exposed silicon groove is etched using plasma radicals as in the absence of protective silicon oxide mask (etched in step 2), the underlying silicon can be etched using plasma etching .

the trench etch results are analyzed using SEM images as shown in figure 4.19a, we observe that the desired trench width of 2 um is successfully obtained using the above mentioned etch process but the small microtrenches from earlier test have become substantially bigger as shown in figure 4.19b. The increase in micro-trench size can be explained because of an increased frequency of ion deflections from sloped sidewalls, which deflect the incoming plasma ion direction. This increases the ion flux quantity at the trench corners and thus increasing the etch rate at corner locations resulting in microtrenching. The hanging groove at the trench top sidewall also promotes larger incoming ion deflection [1].



(a) *The SEM image of trench obtained after three step etch process: 5 min ICP-RIE etch + 5 min HF 0.55 + 3 min 10 sec ICP-RIE etch*



(b) *Microtrenches seen at trench bottom from three step etch process.*

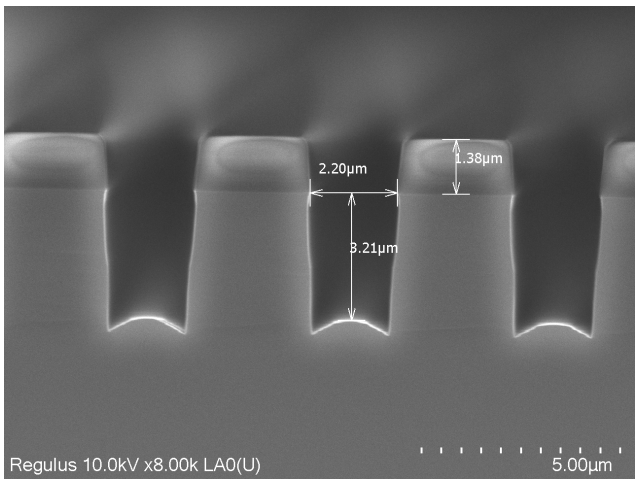
Figure 4.19: *The SEM image for trenches obtained by test run 5.*

Trench test 6

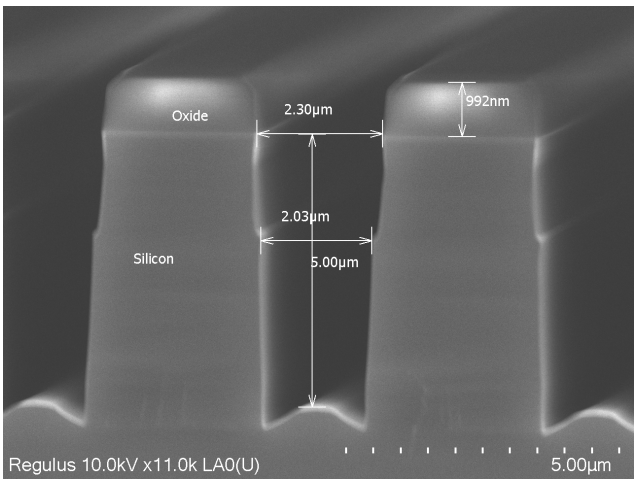
This test run aimed at reducing or eliminating the microtrenches at trench bottom as observed in previous etch recipes. In the following test it was observed that both oxide mask etching time in HF 0.55% solution and final etch stage ICP-RIE etching time have major influence in the size of microtrenches as compared to first ICP-RIE etch time.

Longer the etch time in both HF 0.55% solution and second ICP-RIE etch, bigger are the microtrenches. The possible reasoning is that post oxide mask wet etching in the HF solution, the incoming chlorine radicals (ions) hit trench sidewalls at higher grazing angles ($> 80°C$) than first ICP-RIE etch step, this results in increased silicon etching at corners compared to middle bottom of trench resulting in deeper microtrenches. The experimental analysis is discussed below based SEM image observations (see figure 4.20a) and literature.

1. **2nd ICP-RIE etch time** The first etch time in ICP-RIE chamber was halved from 5 min to 2 min : 30 sec while keeping the HF etch time and 2nd ICP-RIE time same as used in trench test 5. SEM figure 4.20a shows large microtrenches even with reduced 1st ICP-RIE etch time indicating the influence of 2nd ICP-RIE etch time on size of microtrenches.
2. **HF etch time:** The HF solution etch time is increased from 5 min to 13 min : 15 sec while keeping both the ICP-RIE etch times same that is (5 min in 1st ICP-RIE and 3 min : 10 sec in 2nd ICP-RIE). The SEM figure 4.20b shows largest observed microtrenches in the test which highlights the influence of oxide mask coverage on trench sidewalls and trench bottom.



(a) *The above SEM image shows the influence of high etch time in 2nd ICP-RIE etch stage on trench bottom.*



(b) *The SEM image shows influence of increasing HF etch time on trench sidewall and bottom profile*

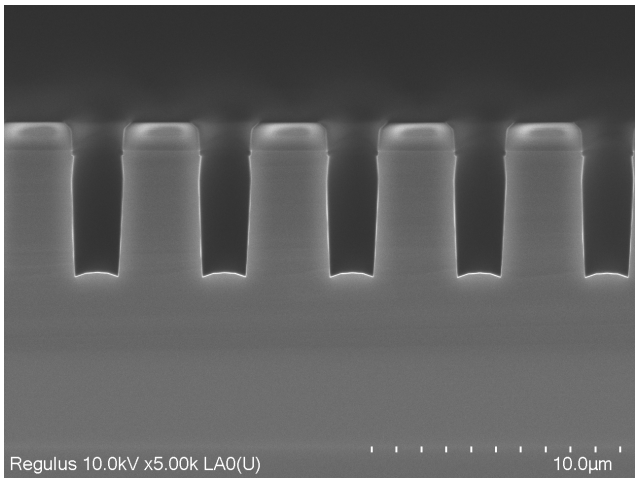
Figure 4.20: *The SEM images show key process parameters influencing trench bottom (a) and trench sidewall profile (b).*

Trench test 7 (Optimized trenches)

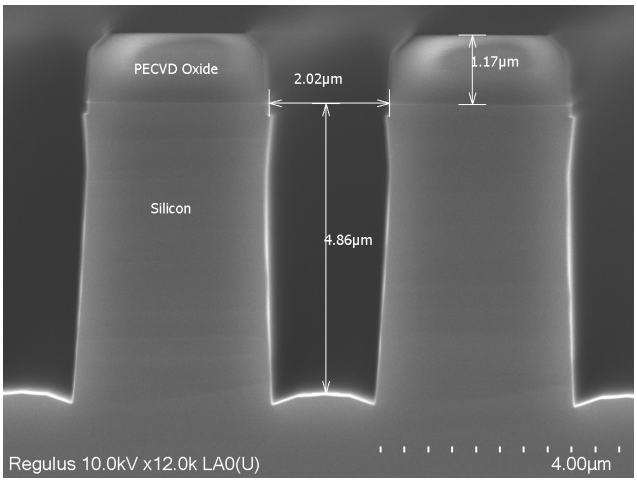
Microtrenches were required to be eliminated or reduced without using complex processing techniques. Based on the results obtained in previous trench etch test runs, a etch process recipe was formulated to obtain optimized trench design which fulfills most of our desired trench design criteria like trench pitch, aspect ratio and profile (refer figure 4.21 below). The HF solution etch time was optimized to remove very controlled amount of silicon oxide mask, required to expose hanging sidewall to get 2μm width. The majority of the ICP-RIE etch is done in first stage and the 2nd plasma etch step helps remove the hanging sidewall to open up the trench top. The optimized etch recipe is as follows

5 min ICP-RIE etch + 6 min 30 sec HF 0.55 % + 15 sec ICP-RIE etch

The process parameters used for ICP-RIE etch are same as discussed in Trench test 4 and only etch time is changed.



(a) *SEM image showing overview of the trenches in silicon.*



(b) *Magnified SEM image of trench with optimized etch recipe.*

Figure 4.21: *The SEM images showing trenches obtained by optimizing trench etch parameters to obtain desired trench aspect ratio and profile.*

4.4. Wafer stress and warpage analysis

A processed wafer internal stress and warpage are important factors which influence the subsequent stages in thin semiconductor chip manufacturing like grinding and dicing. It is thus important to understand the nature of the stresses and bow introduced by various process layers used for fabricating power MOSFET devices. The amount of stress and bow induced by different process materials depend upon their process parameters and film thickness. Flexus-2320-S tool was used for measurement of stress in wafers by deposition of thin films (see figure 4.22b). It computes film stress by measuring the change in substrate radius of curvature generated by the deposition of a thin film on the silicon substrate. It used two different wavelengths of light (670nm and 780nm) with 50 scan points for the measurement. The study for wafer warpage and stress is divided into four tests which are discussed below:

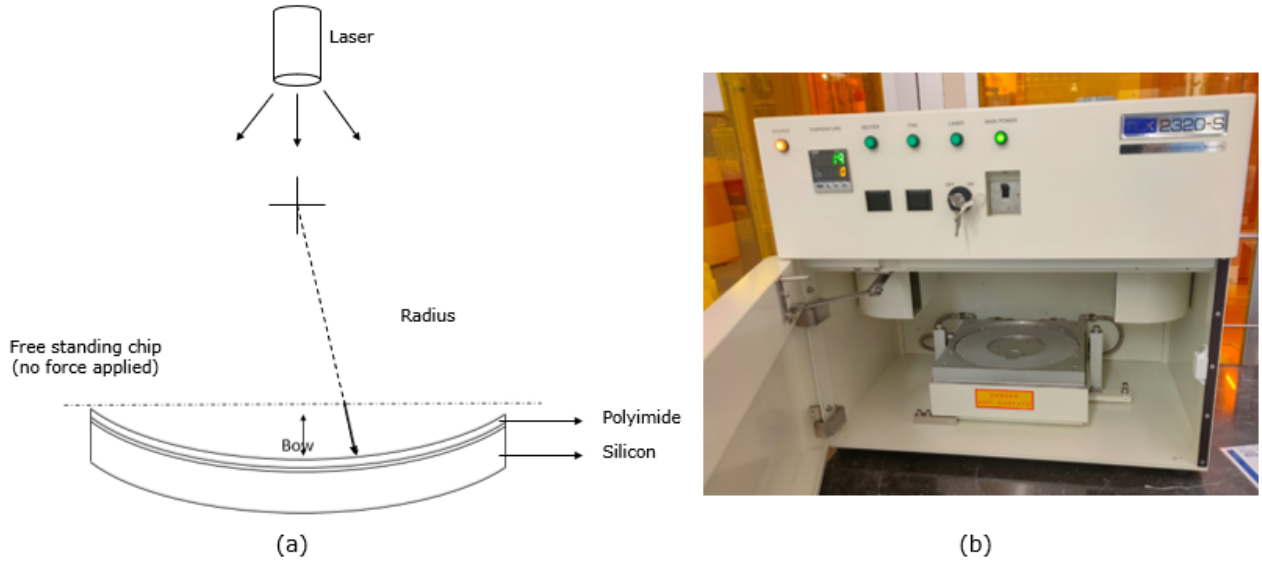


Figure 4.22: *(a) figure representing bow and radius of a warped silicon die with PI film; (b) Flexus tool used for thin film stress measurements in 100 mm wafers*

Process layer	Bow (um)	Stress (MPa)	Radius (m)	Film thickness (nm)
Warpage Test 1				
Bare Si wafer	0.61	N/A	- 2E+06	N/A
Si + PI top	- 14	+ 30	56.5	5000
Warpage Test 2				
Bare Si wafer	1.59	N/A	- 621.4	N/A
Si + TEOS	18.87	- 90	- 42.8	2000
Si+ TEOS + PI	2.25	- 14	- 408.5	5000
Warpage Test 3				
Bare Si wafer	0.92	N/A		N/A
Si + TEOS	17.72	- 91.5	- 45.1	2000
Si + TEOS + Al	8.03	-13.4	- 97.834	4000
Si + TEOS + Al + Passivation layer (Ox + Si_3N_4)	25.1	-27	- 31	2000 + 1400
Warpage test 4				
Si + TEOS	17.73	- 89.9	- 44.9	2000
Si + TEOS + Aluminium1	8.03	-13.4	- 97.834	4000
Si + TEOS + Aluminium2	- 1.55	+ 19.5	777	6000

Table 4.7: *Table shows effect of different materials and their thickness on wafer warpage. In stress measurements, negative sign (-) refers to compressive stress and positive sign (+) indicates tensile stress in film.*

1. **Warpage test 1 - Pre-stress in PI:**

   A 5 μm thick PI film was investigated for amount of stress and warpage induced by PI in silicon wafers. Pi film was found to be induce tensile stress in silicon wafer with an increased negative bow as seen in figure 4.23(frowny face). This stress come from the PI curing process where the polymer shrinks to allow the cross-linking of bonds for material hardening.

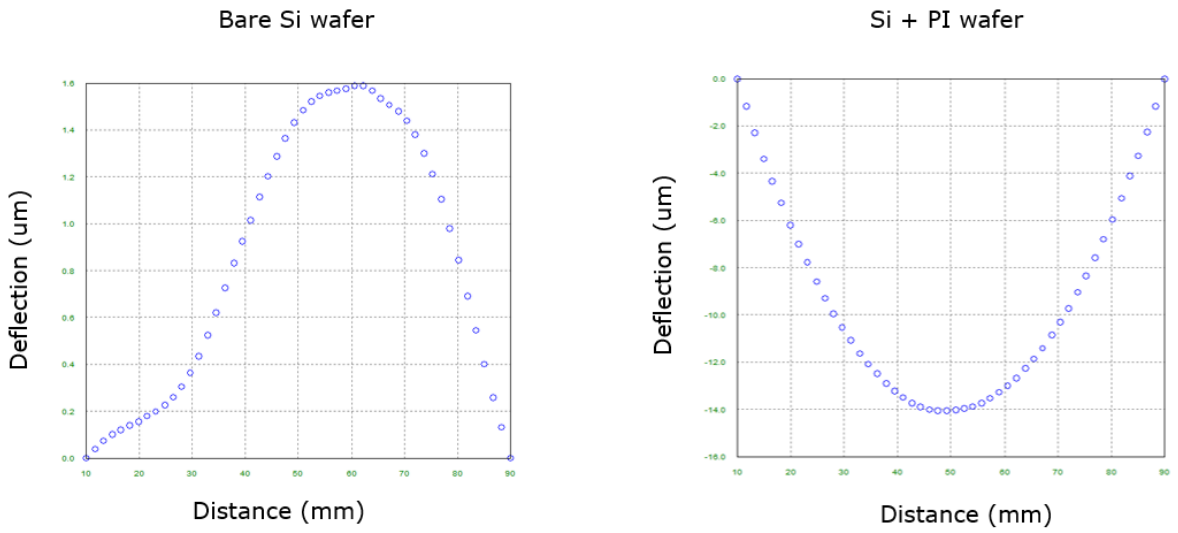


Figure 4.23: *Wafer bow measurements for bare silicon wafer (on left) as compared to wafer bow with addition of PI film on top. Cured PI film exhibits tensile stress.*

2. **Warpage test 2 - Effect of TEOS film in wafer warpage:**
   TEOS film is highly compressive. An addition of 2 μm thick film has induced 90 MPa compressive stress on the wafer (refer table 4.7). In the same test, an additional film of PI was added on top of TEOS which has previously shown tensile nature. The PI film was found to compensate slightly for the negative TEOS film stress. This is implied from the test that a right ratio of TEOS + PI is required to create a ideal flat wafer.

3. **Warpage test 3 - Warpage induced by power MOSFET device layers:**
   In this test, wafer warpage was tested for key process layers stack as seen in power MOSFET devices. A 4μm pure aluminium film was added on top of TEOS to study the effect of the two materials together on wafer warpage and stress. Tensile nature of pure aluminium film was found to compensate for the high compressive nature of TEOS film by slightly reducing the wafer bow and stress. A further addition of MOSFET passivation layers which is a combination of 2μm silicon oxide and 1.4μm silicon nitride led to an increased in wafer warpage because of the compressive nature of the passivation films.

4. **Warpage test 4 - Effect on warpage by increased metal thickness:**
   In the previous test, tensile stress in pure aluminium film was found to compensate slightly for high compressive stress in TEOS film. In this test, a thicker aluminium film of 6μm was investigated as compared to previous 4μm film. A thicker pure aluminium film was found to significantly reduce the wafer warpage and create a near flat wafer with tensile stress.

4.5. Chapter Summary

This chapter highlights various process stages used in fabrication of a dummy power MOSFET device. This dummy power MOSFET has all the relevant process layers like deep silicon trenches, patterned metal layer, passivation layers. A layer of thick polyimide film is added on top of nitride layer to investigate its potential impact on die strengthening. A new process recipe was discussed to fabricate deep anisotropically etched silicon trenches. It is followed by a study to investigate effect of different materials and their thickness on wafer warpage and stress where the polyimide film post-curing showed high tensile stress in the film.

5 WAFER THINNING AND DICING

5.1. Chapter introduction

The process wafers after fabrication have an average thickness of 535 μm. The desired thickness for the test Power MOSFET dies is 50 μm and an individual die size of 6 X 3 mm. The desired thickness of 50 μm is achieved by removing the silicon from wafer backside using grinding process. After grinding, to obtain individual Power MOSFET dies from the wafer, dicing process is used to dice across the wafer. The wafer is loaded on top of UV foil to facilitate the transfer of wafer in between the equipments and post grinding and dicing, the foil is released using UV light exposure to remove to separate the dies from wafer carrier.

5.2. Grinding

As mentioned earlier grinding process is used to reduce the wafer thickness by removing silicon from backside. DAG810 automatic surface grinder was used for the grinding process. Different types of grinding wheels can be used with DAG810 depending on the backside roughness requirement. Standard grinding wheel SD1400 was used for grinding of project test wafer where SD refers to grit type and 1400 refers to grit size [8]. Higher the grit size, better is the backside smoothness (lower roughness). The grinding tool uses two probe system to constantly monitor the wafer thickness during the process for 8 inch wafer where one probe is at the middle of chuck, the other probe is at the edge of chuck. In 4 inch wafers only 1 probe is required (middle probe) due to its smaller size.The process also used a lot of demi-water during grinding to aid the process. The grinding process for 4 inch test wafers goes as follows:

1. Wafer is loaded with backside top on UV foil attached to a FCC carrier.
2. Wafer is grinded from backside for 996 sec to achieve 50 μm thickness.
3. The wafer is cleaned in cleaner DCS1440 by fast spinning and constant air blow.

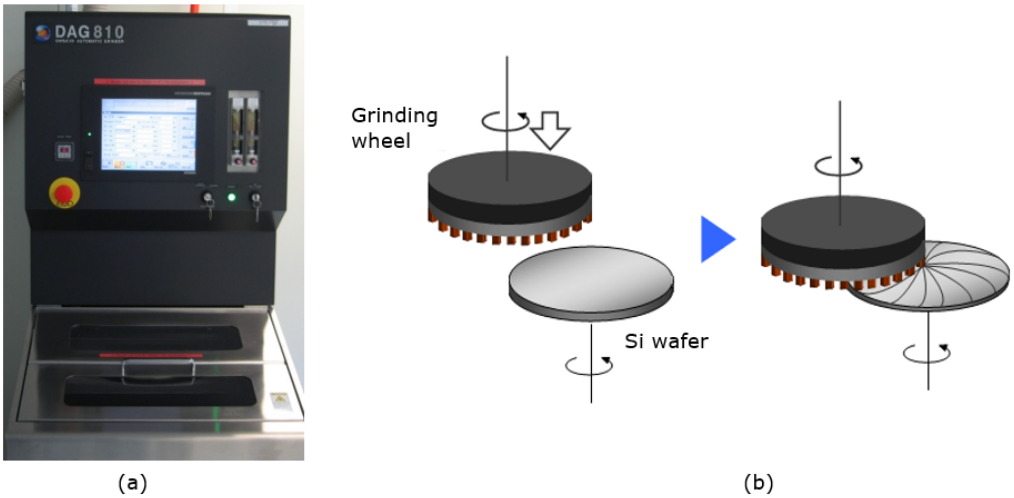
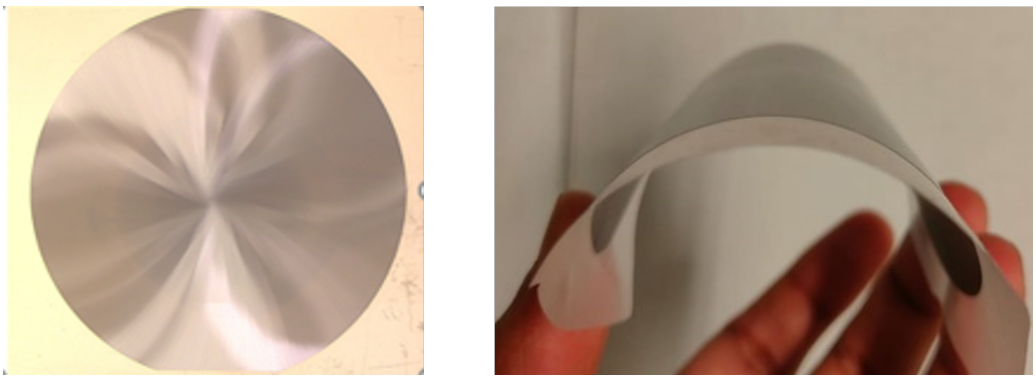


Figure 5.1: *Figure (a) shows the DAG810 automatic Surface grinder tool and figure (b) shows the Grinding mechanism [8]*

The grooves seen in the wafer post grinding (figure5.2) are from grinding wheel and its size is dependent on its grit size.

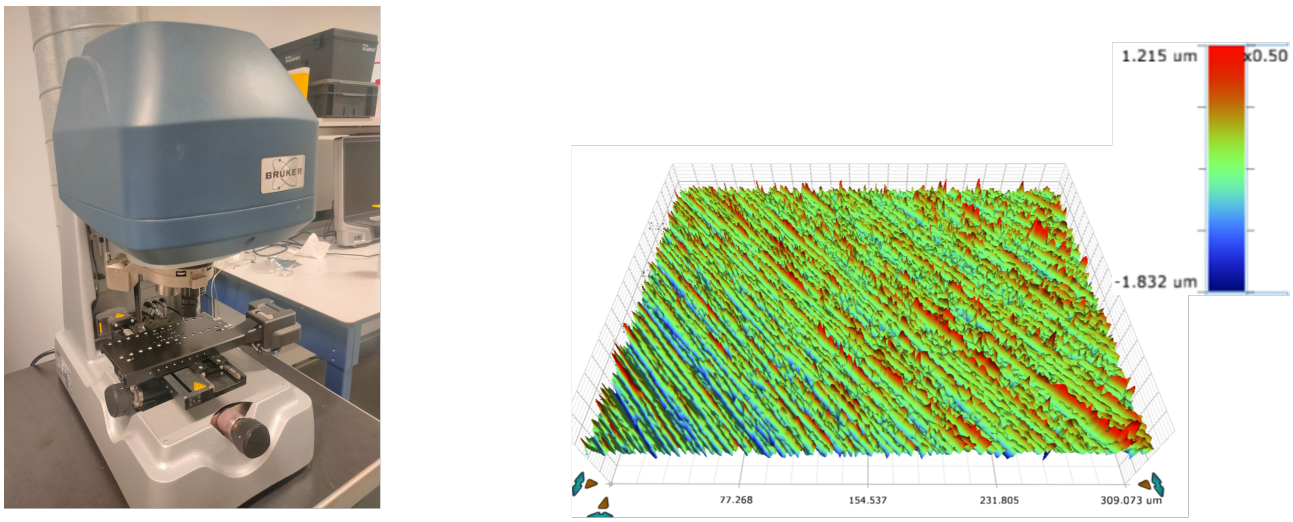


(a) (b)

Figure 5.2: *a) Backside grinded silicon wafer; (b) Extreme flexibility shown by 50µm thin silicon wafer*

5.3. Backside roughness post grinding

The backside roughness is determined by the grit size of the grinding wheel. High backside roughness can adversely affect the silicon die strength. White light interferometer by bruker was used to measure the backside roughness of silicon die samples which have been grinded to 50 μm thickness. The figure 5.3 below shows the measured rectangular plane (300 X 232 μm) and the 3D plot for the plane. The red and blue color in the plot legend signifies the peaks and depths respectively. Greater the difference between the longest peak and depth, greater is the chance for fracture or crack origination in that area.



(a) (b)

Figure 5.3: *(a) White light interferometer used for thin die backside roughness measurements; (b) 3-D plot for grinded silicon backside*

Parameter	Value (um)
Rz	2.574
Rpm	1.146
Rvm	-1.428
Sa	0.148
Sq	0.196

Table 5.1: *Roughness parameters for grinded die backside*

where,

Rz : Average maximum height of the profile
Rpm : Average distance between the highest profile points and the mean data plane.
Rvm : Average distance between the lowest profile points and the mean data plane
Sa : Mean roughness over the 3D surface
Sq : Root Mean Square Roughness evaluated over 3D surface

5.4. Dicing

As mentioned in above section, the wafer is mounted on top of a new UV foil. This time the wafer is placed with frontside top and loaded in the dicing equipment. DAD3350 automatic dicing saw from Disco was used for dicing of test Power MOSFET wafers. SD4000 dicing blade used was used for the process where SD refers to the grit type and 4000 refers to grit size of the blade. From the batch of 16 wafers, half the wafers had cross marker and half wafer did not have any marker. The marker helps in accurate and precise dicing of wafers into dies by allowing the operator to set correct sawing lanes in middle of marker. The sawing length in dies post dicing is ~50 μm. The dicing process is as follows:

- Wafer mounted on low adhesive UV foil with frontside top.
- Wafer diced into individual dies using dicing marker if available.
- Wafer is cleaned in cleaner DCS1440 by fast spinning and constant air blow.
- UV foil is released by extended UV light exposure (7 min) in Dinies UV-chamber M3 tool.

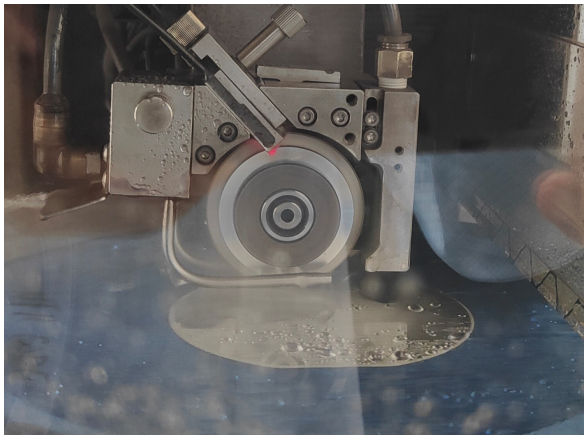


Figure 5.4: *Dicing blade dicing through silicon wafer to make 6X3 mm dies*

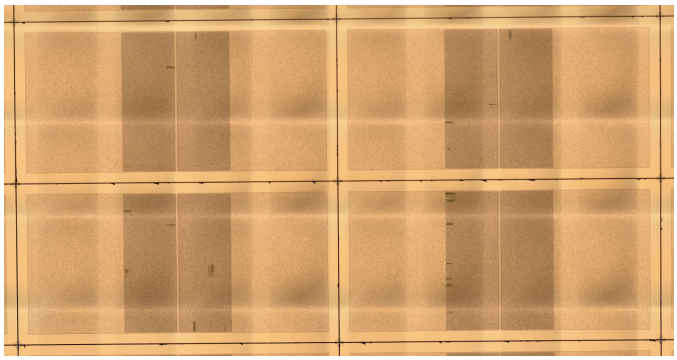


Figure 5.5: *Individual dies seen post dicing process*

Dicing wafer with markers

Dicing markers are created in wafer to support the dicing process. These markers are designed to shape like a cross mark or a plus mark which can be visualized in the equipment screen to mark the path for dicing

blades. The marker is formed by patterning the aluminium metal layer during the fabrication process. The markers are located at the corners of the each die. Diced die dimensions are accurate and precise as seen in figure 5.6.

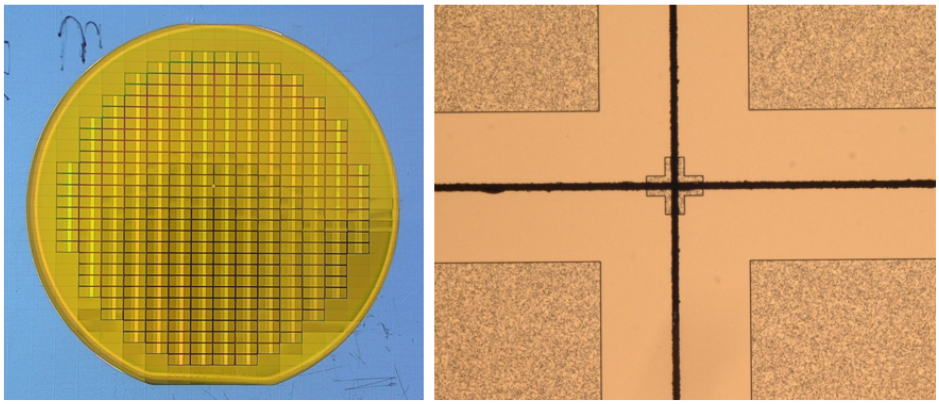


Figure 5.6: *Wafer diced into individual dies using cross marker*

Dicing wafer without markers

Wafers where the aluminium metal layer is not patterned during the fabrication process, do not have dicing markers present in them. The layer is not patterned owing to the design requirement of the particular wafer. These wafers are diced without the support of dicing markers. The wafers are diced by manually setting the sawing lane path of the dicing wheel in between the dies. Diced dies are less accurate and precise in dimensions as compared to diced dies with markers.

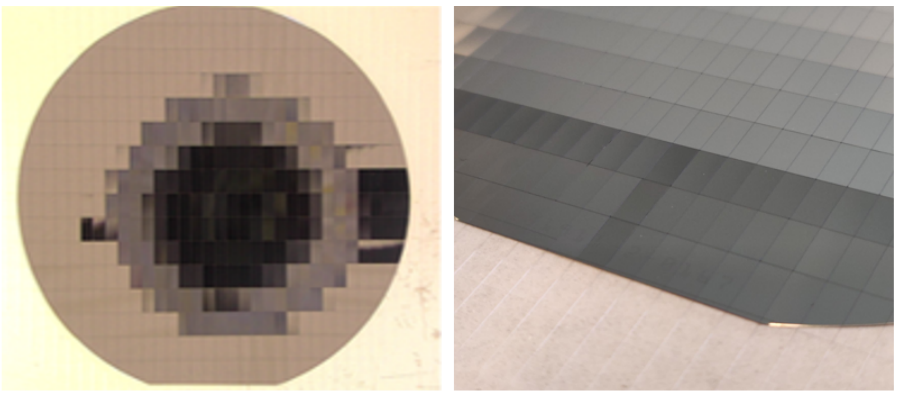


Figure 5.7: *Wafer diced into individual dies without cross marker*

The dies obtained from mechanical dicing process show small chipping damage at the edges when observed under high magnification of microscope. To reduce the impact of sawing imperfections, same process parameters and dicing tools were used for dicing of all process wafers.

5.5. Low adhesive UV foil

Post grinding process, the foil covering thinned wafer frontside is removed and replaced with a low adhesive UV foil on wafer backside to prepare the wafer sample for dicing process. Post wafer dicing, dies need to be picked up from the foil without damaging or stressing the die samples. Any damage inflicted in the die during the pickup process can negatively influence the die strength measurement results in three point bending test.

The very low adhesive foil is critical to die singulation process from wafer as it allows manual die pick up from foil with the help of tweezers with minimum or negligible stress induced in dies. The low adhesion between the sawned dies and foil is attained by over exposing the foil to UV light for extended time. All the

test wafers in this project are exposed to total 7 minutes UV light in contrast to standard 4 minutes of UV exposure. **365 nm wavelength UV light** is used in combination with **5.5 mW/sq-cm exposure power** in the tool Dinies UV-chamber M3. Higher the exposure energy, lower is the required peel force for die removal from foil.

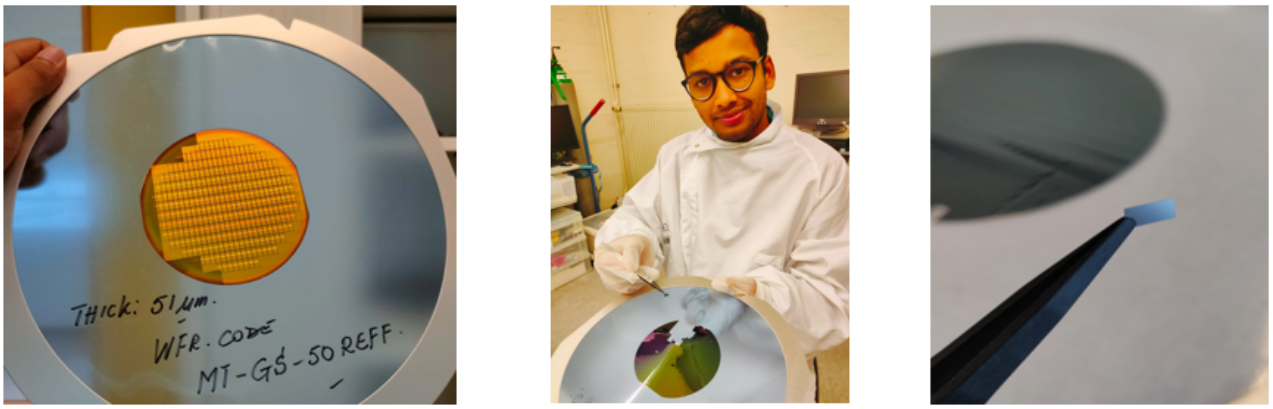


Figure 5.8: *Wafer mounted on top of low adhesive UV foil were singulated manually using tweezers.*

5.6. Chapter summary

In this chapter, grinding and dicing processes for obtaining ultra thin 50 μm dies were discussed. Low adhesive UV-foil with overexposure ensures release of dies from dicing foil with minimum induced stress from manual tweezers. Chipping was observed in diced dies which can make dies more sensitive to failure. Low backside roughness (post grinding process) was observed using a white light interferometer test. The influence of grinding and dicing roughness on die strength characterization is reduced by using similar process parameters for all the wafer samples.

6 DIE STRENGTH CHARACTERIZATION

6.1. Chapter introduction

The singulated die are ready for strength characterization. The flexural strength of thin dies is determined by three-point bend (TPB) test strategy. It is a popular measurement technique where a die is bent under an applied load. The die breakage force and the absolute deflection of die can be measured for strength calculations. Different die designs will be tested separately and then compared with each other using weibull analysis.

6.2. Die strength measurement setup

Dynamic Mechanical Analyzer (DMA) tool is a versatile tool which allows various stress tests (tensile, cantilever test etc) along with three point bending for diverse specimen lengths. The main advantage of three-point bend test is its ease of specimen preparation and testing. For this test, DMA Q800-2320 tool was used, wherein the test chip is loaded on two supporting pins separated by a fixed distance apart (span length) and a force indenter applies load from top on die backside until it fractures.

- **Tool used :** DMA Q800-2320 (Dynamic Mechanical Analyzer)
- **Experiment :** 3-point bend test
- **Parameters measured :** Static force, Displacement
- **Sample size :** 40 samples of Silicon based dies (Dimension : 6 X 3 X 0.050 mm)
- **Die designs tested :** 18 designs (> 130 hours of testing)

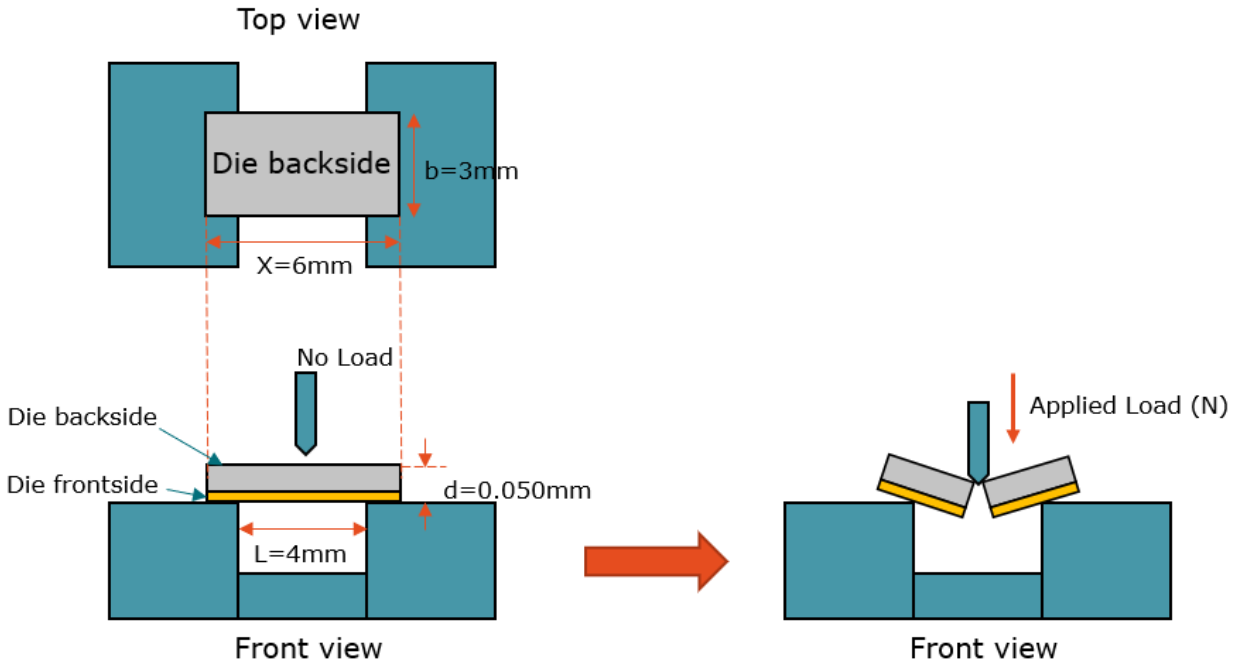


Figure 6.1: *The above schematic shows die specimen loading setup. Die is flipped exposing silicon backside to applied force and die cracks from frontside first under tensile stress*

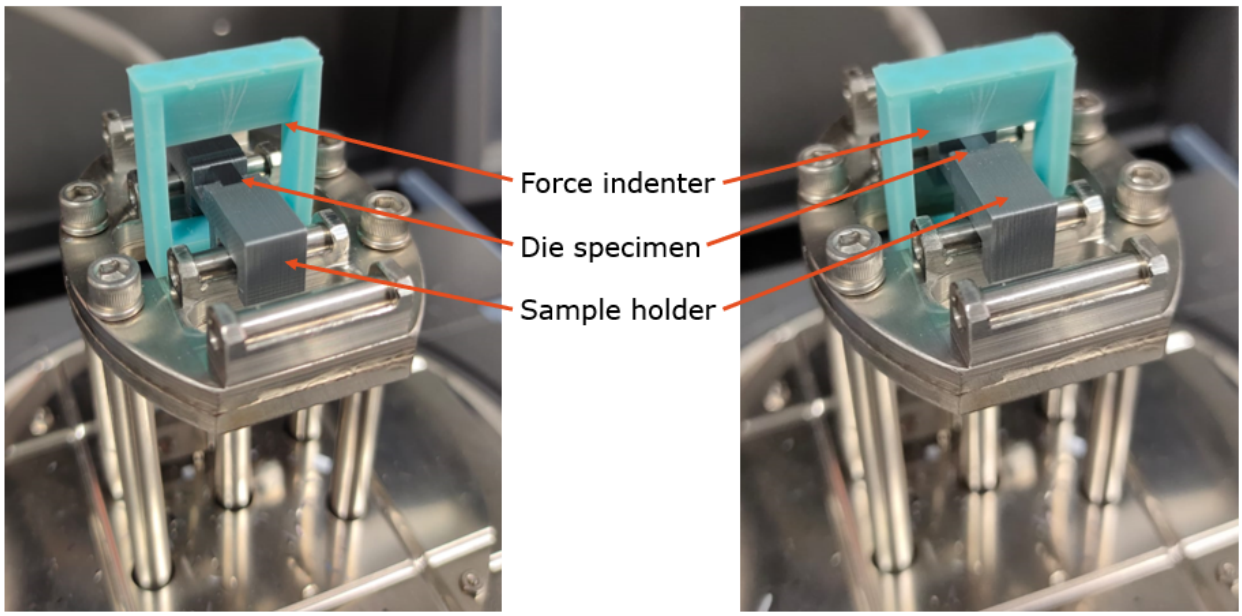


Figure 6.2: *The DMA test setup for three-point bend test for die strength characterization. The die rests on top of sample holder and a indenter (in green) applies load on the die.*

It is important to perform indenter's mass calibration before starting the test [35]. This helps adjust bending force of the tool for the mass and material of the wedge.

DMA tool customization

- **Force indenter:** The large radius of loading wedge influences the accuracy of calculated mechanical stress [11]. An indenter made with resin printer with a sharp wedge was printed to remove the influence of loading wedge. The compliance for the new wedge was ≈2.5 μm/N.
- **Die sample holder:** The DMA tool was designed for sample holder > 20 mm. A sample holder was printed using resin printer to support the test chip of dimension (6 X 3 X 0.050 mm). The span length between the two support ends is 4 mm.
- **Waffle pack:** The dies are released from the low adhesive foil post dicing using tweezers. These dies need to be transported between the pickup environment and testing environment, waffle pack was printed to support the transport of singulated chips.

6.3. Testing methodology

- The thin dies are picked up using fine tip tweezers (non-metal) from waffle pack and visually inspected for any physical damage like cracks and breakage.
- Good dies are gently placed in the custom made sample holder. The die is placed such that approximately 1mm of die edge is resting on top of the holder supports on both sides, which leaves 4 mm of die length also known as span length hanging.
- The die strength tests are done to measure the front side strength of the dies. In 3-point bend test strategy, the die is flipped. This exposes the grinded back-side of die to the sharp wedge of the DMA tool from where the force is applied o the die. This is because silicon which is brittle in nature handles compressive strength better than tensile strength, so we observe the frontside of die cracking first under tensile stress applied by the load from the DMA sharp wedge.

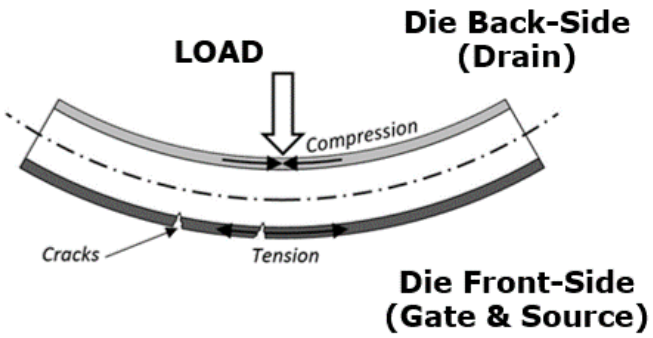


Figure 6.3: *The figure shows the nature of stresses seen on the die under applied load. The silicon backside experiences compressive stress and die frontside undergoes tensile stress which results in crack formation.*

- The load on the die is applied using two ramp force functions. The first ramp force function 0.010 N/min to 0.010 N/min.
    1. Allows proper line contact between the sharp wedge and die sample.
    2. Die doesn't move during beginning of measurement.
- The next function is ramp force where the force applied on die sample gradually increases 0.2 N/min to 1 N/min. The values of the force function are variable and can be changed depending on nature of sample. The die crack is observed during this step and the measurements are stopped for analysis of the acquired data.
- The die breakage force and die displacement is measured using Force versus displacement graph where the slope corresponds to sample stiffness. The difference is taken between the values from point B to point A which gives absolute deflection and load undergone by die before breakage. Figure 6.5 shows the Force-Displacement graph generated by the DMA tool for data acquisition.

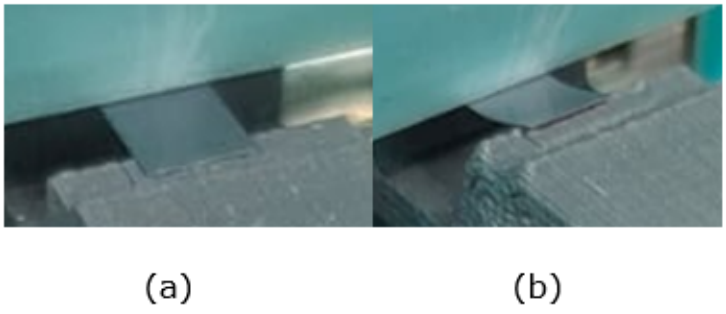


Figure 6.4: *(a) shows a custom made force indenter making contact with the backside of die (silicon) (b) thin die bending under applied load. ultra-thin silicon dies shows extraordinary flexibility*

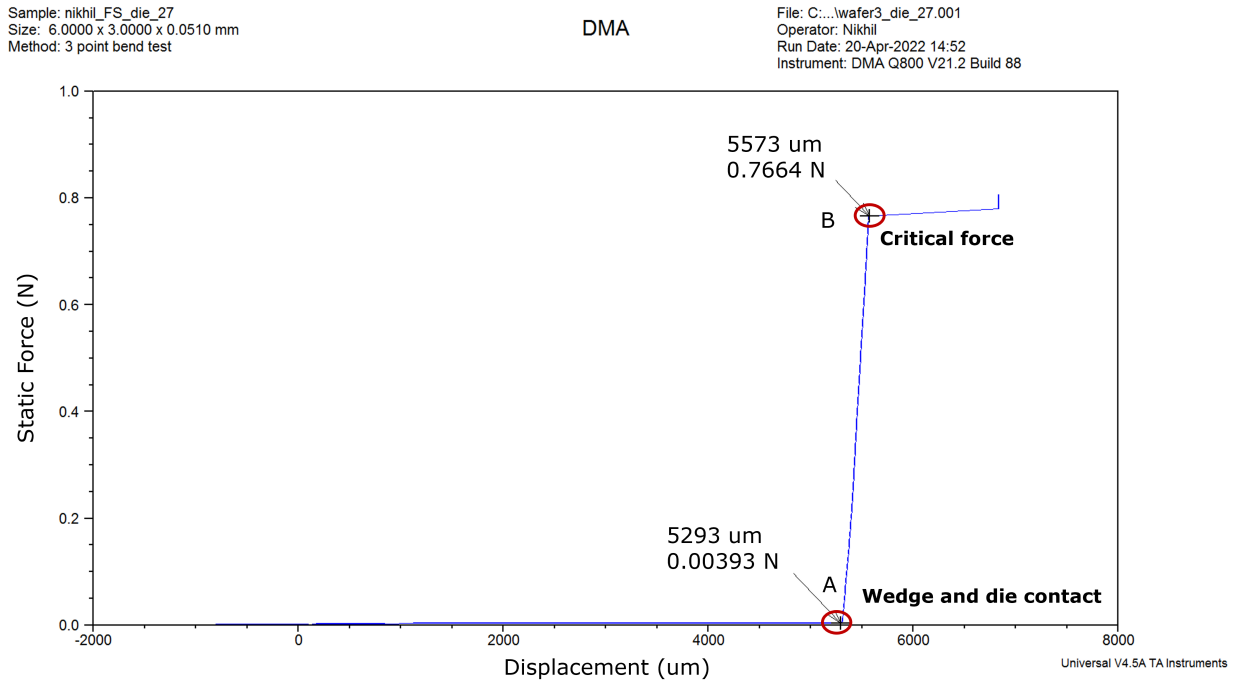


Figure 6.5: *Force- Displacement graph for a bare silicon die without any process layers. Point A marks the contact between the wedge and die where point B refers to the force and displacement where the die cracks.*

- The process is repeated for 35-40 samples, in order to generate Weibull probability plots for failure analysis. A good sample size allows for better curve fitting along with scatter plots for comparison between different specimens. The process is time consuming and thus 40 samples were selected to generate reasonable data plots for assessment.
- The experiment generated Force - Displacement graphs are linear in nature. The standard flexural stress equations [37] is used to characterize strength for thin dies which goes as follows

$$\sigma_f = \frac{3FL}{2bd^2} \tag{6.1}$$

where
σ_f = Stress in outer fibers at Midpoint (MPa)
F = Breaking load (N)
L = Support span length (mm)
b = Width of die (mm)
d = Thickness of die (mm)

Here, some parameters are fixed and depend on die geometry such as L = 4 mm, b = 3 mm, d = ~ 50 μms . The exact thickness of die specimens is a known parameter, with variations of 1-5 μms between chip designs. Breaking load (N) is measured from three-point bending test.

6.4. Analytical equation for stress calculation

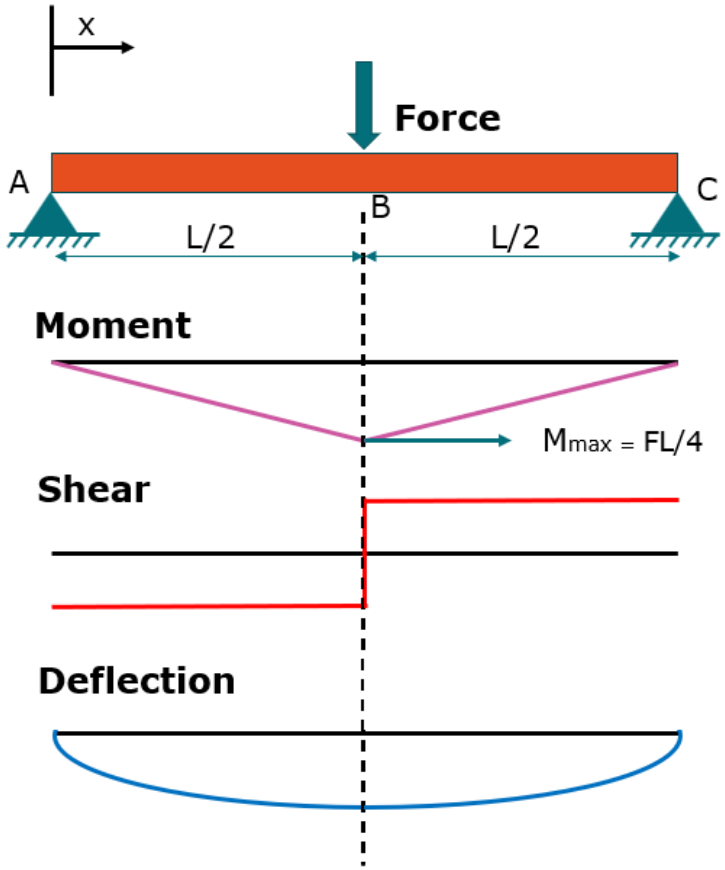


Figure 6.6: *Figure shows a schematic of a reactangular beam under three point bend test (top) and plots of bending moment (M), shear (Q) and bending deflection (D). Schematic is a production provided by [39]. Maximum bending moment M is observed at centre of the beam.*

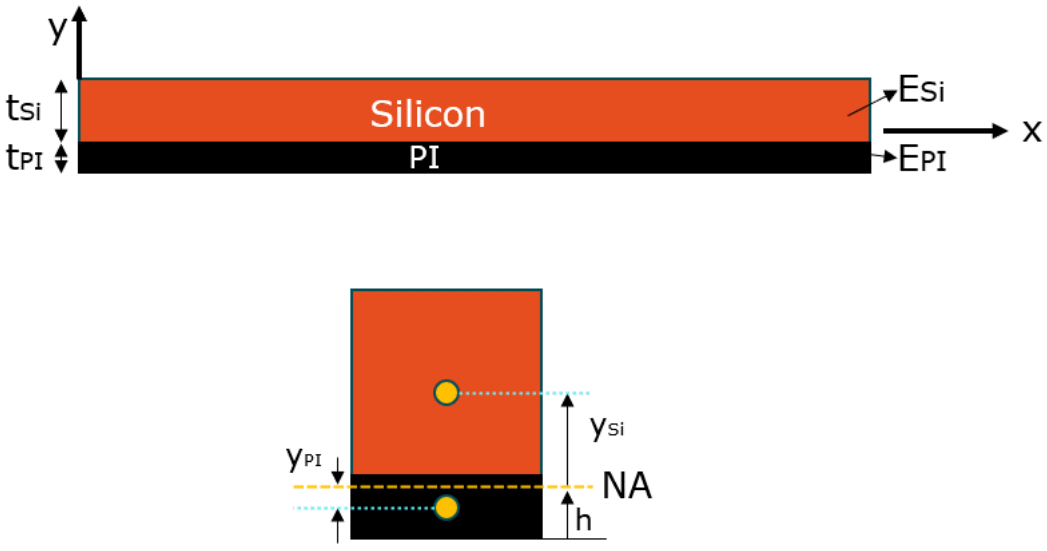


Figure 6.7: *Schematic of a composite beam of two materials with different young's modulus.*

In non-composite beams, the stress at the neutral axis (NA) of the beam is zero and the axis lies generally in the exact middle of the beam. In composite beams, this neutral axis is not in the middle as the relative stiffness and thickness of each of the material section affect the neutral axis positioning in the beam. For

dies with nitride top, the young's modulus of different layers is comparable and can be treated as a single non-composite beam. For dies with thick PI top, the equation 6.1 cannot be used for stress measurements and the equation needs to be modified to account for a bi-layer system. During three-point bending test, the tensile stress in PI film under applied load is quite less as compared to stress in underneath layers. This is because PI is a soft material with a very low young's modulus (E_{PI}: 2.5 GPa) [12] as compared to materials like silicon (E_{Si} ~ 170 GPa) [17] or other materials found in die cross-section. Thus, a new analytical equation is derived for calculating fracture stress in a bi-layer system of silicon and polyimide materials. The equation is derived from the work done in [10].

The bending stress in a composite beam can be determined at any interior location by applying the moment equilibrium equation. We know that addition of the moments acting on the beam leads to,

$$\sum M_z = 0$$

$$= \int (\sigma_s y)\, dA + M$$

$$= M + \int_{A_1} \sigma_{Si}\, y dA + \int_{A_2} \sigma_{PI}\, y dA$$

Making use of bending stress (σ) and radius of curvature (ρ) relationship, ($\sigma = -\frac{Ey}{\rho}$) gives:

$$M = \frac{E_{Si}}{\rho} \int_{A_1} y^2\, dA + \frac{E_{PI}}{\rho} \int_{A_2} y^2\, dA$$

$$M = \frac{E_{Si}}{\rho} I_{Si} + \frac{E_{PI}}{\rho} I_{PI}$$

Rearrangement of above equation gives

$$\rho = \frac{(E_{Si} I_{Si} + E_{PI} I_{PI})}{M}$$

Revisiting relationship between bending stress and beam curvature of each material section provides:

$$\sigma_{Si} = -E_{Si} \frac{y_{Si}}{\rho} \; and \; \sigma_{PI} = -E_{PI} \frac{y_{PI}}{\rho}$$

$$\sigma_{Si} = \frac{M y_{Si} E_{Si}}{(E_{Si} I_{Si} + E_{PI} I_{PI})} \tag{6.2}$$

$$\sigma_{PI} = \frac{M y_{PI} E_{PI}}{(E_{Si} I_{Si} + E_{PI} I_{PI})} \tag{6.3}$$

Here, M is the maximum bending moment found at middle of the bending beam where the beam fractures under applied force F (Refer figure 6.6) and y_{PI} and y_{Si} are distances from neutral axis (NA) to the centroid of PI film and silicon substrate respectively. The symmetry of the beam is used to calculate the bending moment at beam middle where the beam moment at the center can be modeled for half beam with span length L/2 and fracture force F/2. The relationship between bending moment (M) and fracture force (F) can be given by

$$M = \frac{FL}{4} \tag{6.4}$$

where L is total span length of the beam under bending test. The new neutral axis (n) for each material section can be given using below equations:

$$n_{Si} = \frac{(t_{Si}^2 E_{Si} + 2 t_{PI} E_{PI} t_{Si} + t_{PI}^2 E_{PI})}{2(t_{Si} E_{Si} + t_{PI} E_{PI})} \tag{6.5}$$

$$n_{PI} = t_{Si} + t_{PI} - n_{Si} \tag{6.6}$$

Here t_{Si} and t_{PI} denote the thickness of silicon and PI film. From the above equations, the distance from neutral axis to the centroid of the material area can be calculated.

$$y_{Si} = t_{Si} - n_{Si} \quad and \quad y_{PI} = n_{PI} \tag{6.7}$$

Moment of inertia (I) for the two material sections can be calculated using equations below:

$$I_{Si} = \frac{b t_{Si}^3}{12} + b t_{Si} (n_{Si} - \frac{t_{Si}}{2})^2 \tag{6.8}$$

$$I_{PI} = \frac{b t_{PI}^3}{12} + b t_{PI} (n_{PI} - \frac{t_{PI}}{2})^2 \tag{6.9}$$

6.5. Die fracture strength analysis using Weibull distribution

Weibull distribution is used to evaluate and compare the fracture strength of different chip designs. A sample size of 40 dies is tested for each design to generate sufficient dataset for weibull distribution. The markers in the plot represent the fracture stress for each individual die sample in weibull distribution plots.

6.5.1. Setting up a reference die

The bending stress (fracture stress) data obtained using three point bending experiment and stress equations need to be analyzed for comparing die strength between different chip designs and approaches. Weibull probability distribution plots are used as means for comparing and analyzing die strength of these chips. The aim was to first fabricate a reference chip which mimics the mechanical robustness of the frontside of a commercially available trench power MOSFET chip (reference chip) and then add new top metal designs, thick films and new trench layouts to analyze the response of new design approaches to die mechanical robustness.

The reference chip is referred as Standard test chip in the project and this contains Gate-Source metal regions separated by a 50 μm line gap with mixed oriented trenches i.e. vertically aligned trenches under the source area and horizontally aligned trenches underneath the metal gate area in the silicon substrate. The patterned metal layer is covered with passivation materials like oxide and nitride as also seen in commercial power MOSFET chip.
In the figure 6.8, probability plot for weibull distribution can be seen for comparing the frontside fracture strength of commercial trench MOSFET chip and the standard test chip. The table 6.1 highlights key remarks between the two dies. It is observed that the strength as well as the distribution of the two chips is almost identical where the average frontside strength of a commercially available trench power MOSFET chip for a dimension of (~6 X ~3 X 52 mm) was found as **318 MPa** and the average strength of EKL cleanroom fabricated chip (6 X 3 X 0.051 mm) was found as **339 MPa**. It is important to note that the standard deviation in data was also found identical (51) and the effect of different die thickness was removed by the stress equation 6.1 used for fracture strength calculation.

Chip design	Dimension (mm)	Average die strength (MPa)	Standard deviation	die thickness (um)	Sample size
Commercial chip	5.5 X 2.8 X 0.052	318	50	52	30
Standard test chip	6 X 3 X 0.051	339	51	51	40

Table 6.1: *Data comparison for frontside strength between commercial and standard test chip*

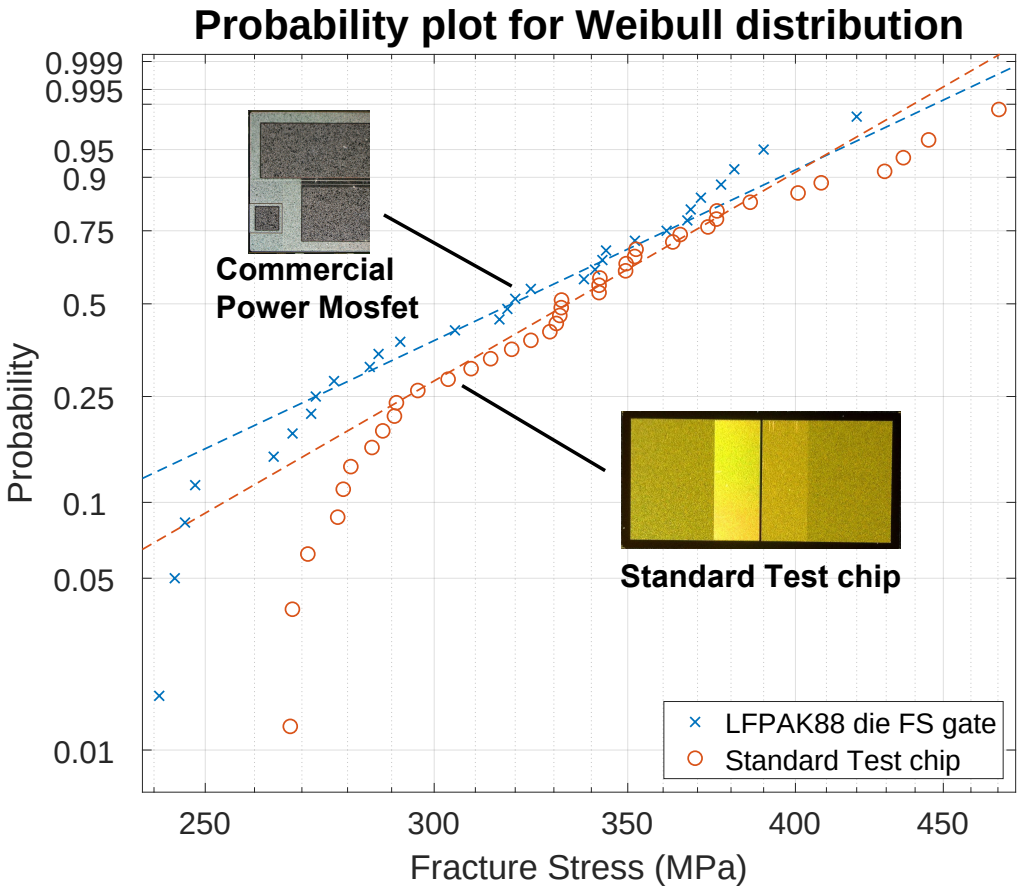


Figure 6.8: *Weibull distribution for fracture stress comparison of two chips namely commercial trench power MOSFET chip and standard test chip*

It can be implied from the above discussion that the standard test chip is a good mechanical reference to commercial power MOSFET chip and is ideal for comparative study to investigate the response of new top metal designs and films for their positive or negative impact on die robustness.

6.5.2. Die designs with negative response to die strength

In the investigation to find new die designs which can positively influence die strength, some designs did not perform as expected previously and a decrease in average die strength was seen in some of the design approaches. All the chips have same dimension, trench layouts and identical die thickness as well (6 X 3 X 0.051 mm). Same loading conditions and ramp force function was used for applying load on die backside for three point bending test. Standard test chip was used as baseline for the analysis.

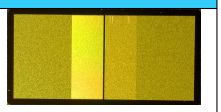
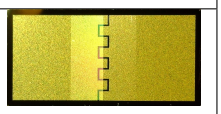
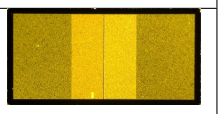
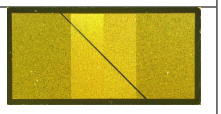
Chip design	Average die strength (MPa)	Standard deviation	die thickness (um)	Die top view
Standard test chip	339	51	51	
Die with Thin meander	283	40	52	
Die with reduced G-S gap	307	35	51	
Die with angled G-S gap	261	39	51	

Table 6.2: *Data comparison between standard test chip and designs which reduced die frontside strength.*

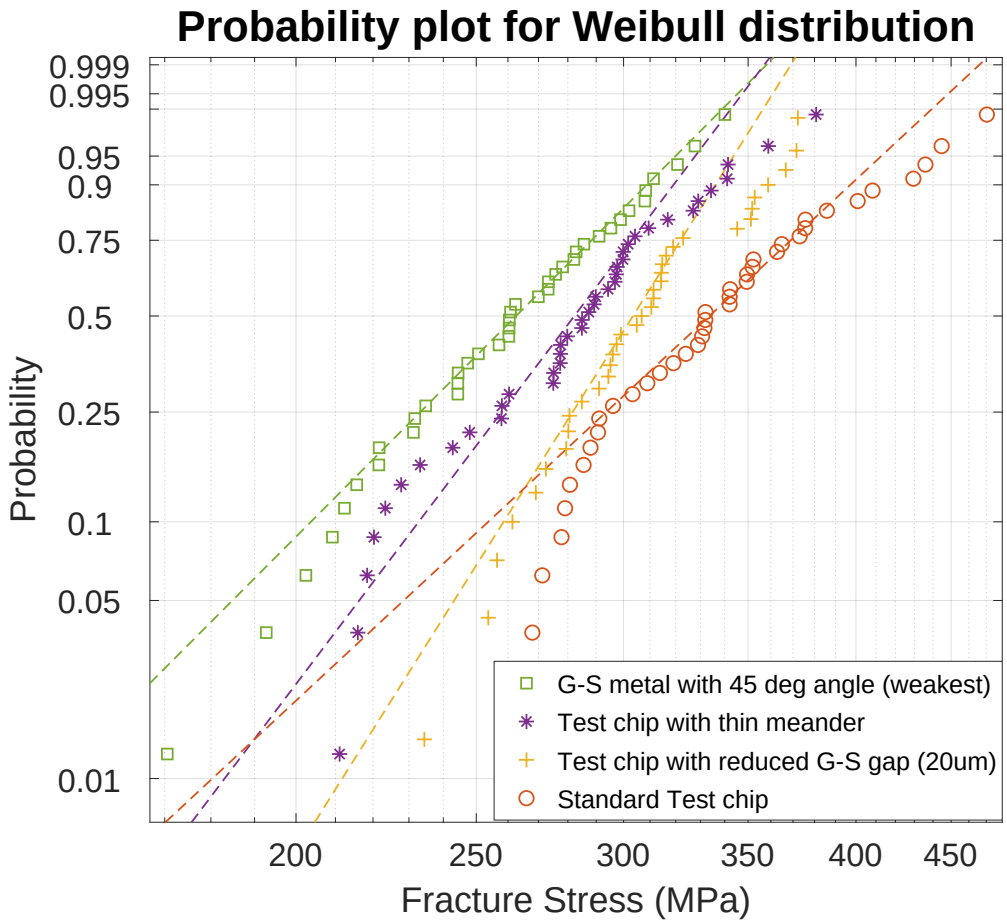
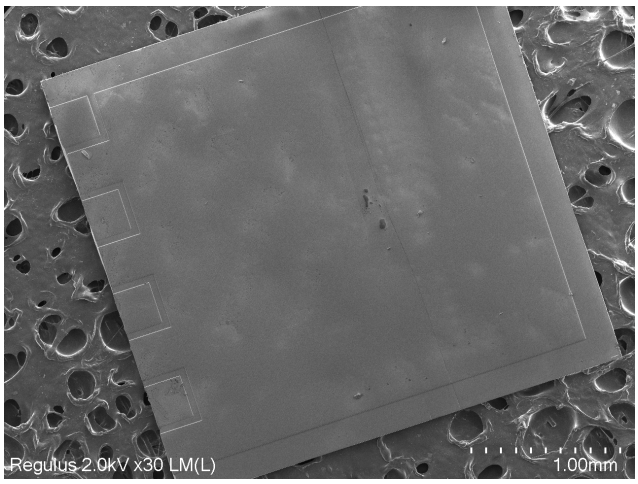


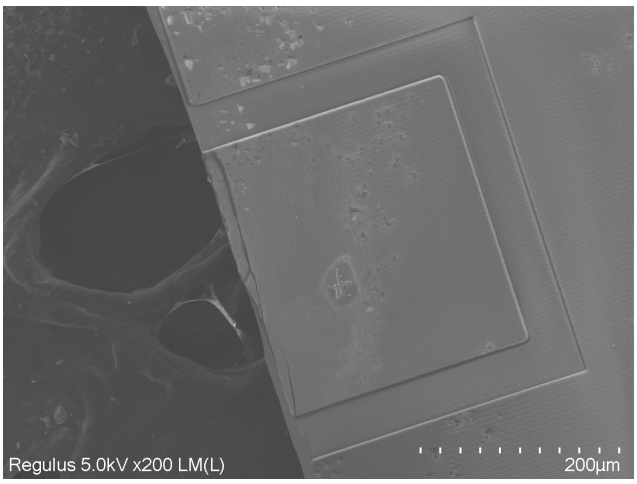
Figure 6.9: *Weibull probability plot for die designs which decreased frontside die strength as compared to standard test chip. Dies with angled G-S separation showed lowest fracture strength.*

Table 6.2 and weibull plots in figure 6.9 indicate the behaviour of these die designs. The key highlights are discussed briefly and listed below

- **Die with thin meander:** represents the die where gate-source separating vertical line gap is replaced with a meander. The average die strength was found to decrease from **339 MPa** to **283 MPa** when compared to standard test chip. The bending tests were followed by SEM inspection to locate vulnerable areas to die crack initiations shown in figure 6.10.



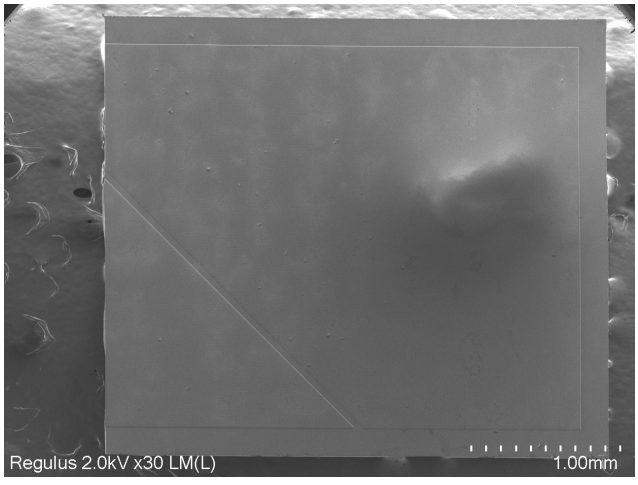
(a) *Majority of the die cracks are seen in meander along the path formed by metal absent areas*



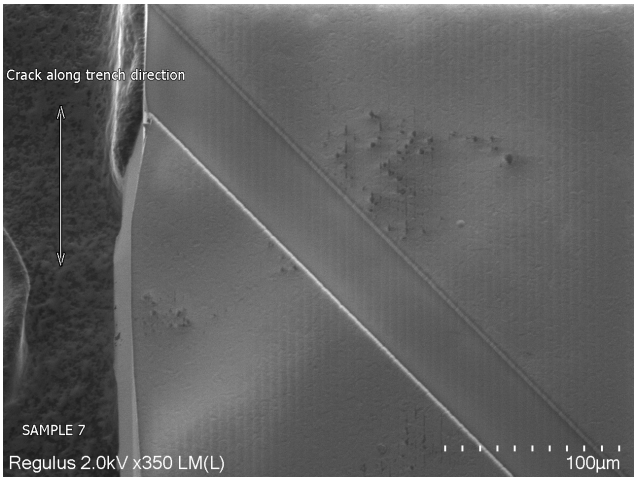
(b) *Higher magnification inspection shows die crack location along vertical trenches*

Figure 6.10: *SEM analysis for die crack for thin meander chip design.*

- **Die with reduced Gate-Source gap :** In the standard test chip, the gate-source metal sections are separated by a gap of 50μm. In this design, investigation is done where this gap is further reduced to 20μm. The die strength exhibited by this design is higher as compared to other poorly performing designs (**307 MPa**) but still less as compared to standard test chip (**339 MPa**). A plausible explanation is still required explaining this behaviour.
- **Die with angled Gate-Source gap :** In this die design, the gate-source vertical line separation was replaced with an angled line separation (45 °). The die failure in this sample space was found to be random but in the die middle region where the gate-source separation is seen. In majority of dies, the crack was found to initiate in the region where trenches are aligned in the direction of crack propagation which is along vertical trenches (as shown in figure 6.11a and 6.11b) and in other instances, die cracks were also seen to initiate perpendicular to trench orientation. This die design performed the weakest in die strength as compared to other chip designs. The angled die design show fracture strength of **261 MPa** in contrast to **339 MPa** of the standard test chip.



(a) *Majority of the die cracks are seen in the region with angled gate-source separation*



(b) *On higher magnification inspection, die cracks are seen propagating along vertical trenches*

Figure 6.11: *SEM analysis for die crack for angled gate-source separated chip design*

6.5.3. Die designs with positive response to die strength

Here, the die designs which showed positive response to die robustness in comparison with standard test chip are discussed. Two designs are identified, die with thick meander and die where trenches are strictly underneath metal layer. Thick meander refers to meander design with wider metal width in direction of

crack propagation. Please note, thick meander design is different from previously discussed thin meander design where the metal width was much lower in the die crack direction. The thick meander die was obtained with a thickness of 57μm from a grinding miscalculation. The effect of this increased die thickness on die strength is eliminated using the stress equation 6.1

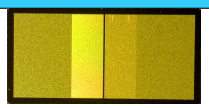
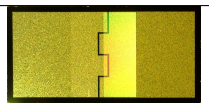
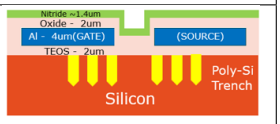
Chip design	Average die strength (MPa)	Standard deviation	die thickness (um)	Die layout
Standard test chip	339	51	51	
Die with Thick meander	350	39	57	
Die with trenches only under metal	364	37	52	

Table 6.3: *Data comparison between standard test chip and designs which improved die frontside strength.*

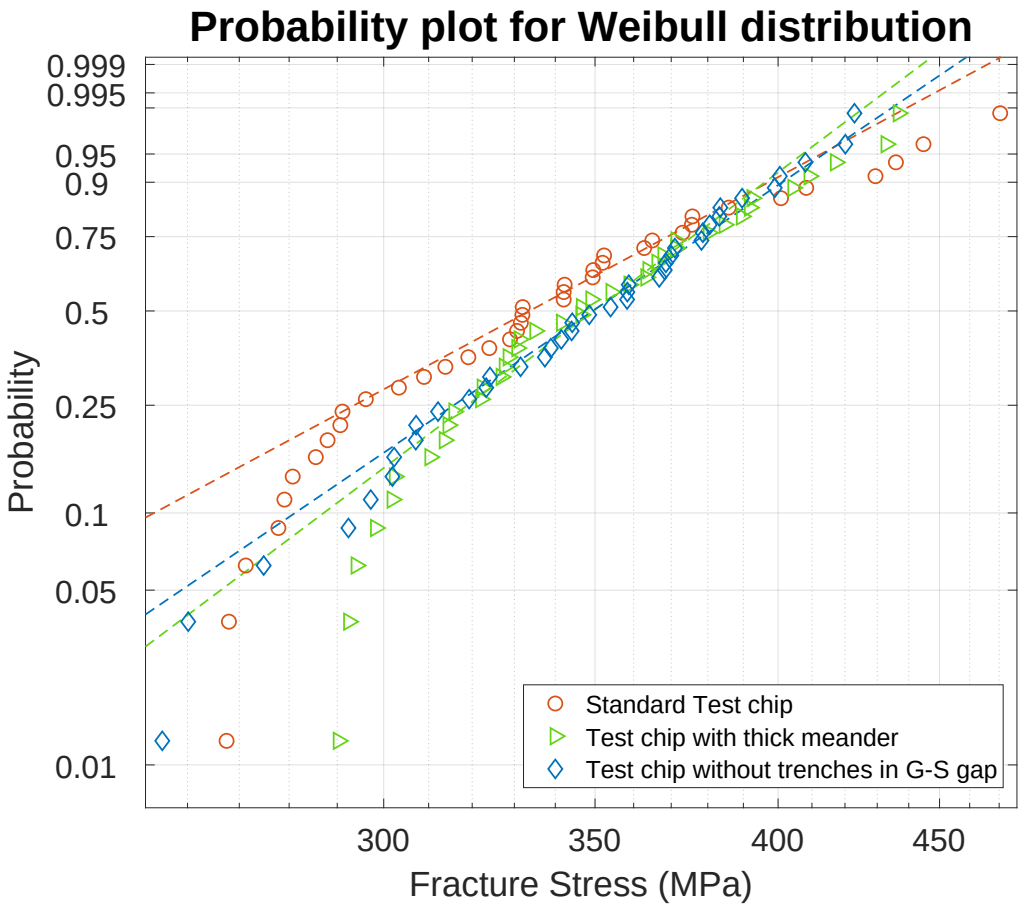


Figure 6.12: *Weibull probability plot showing die designs which increased die strength as compared to standard test chip. Die design with thick meander and design where trenches are covered with metal layer above show higher die fracture strength*

Table 6.3 and weibull plots in figure 6.12 indicate the behaviour of these die designs. The key observations are discussed below:

1. **Die with thick meander:**
   - Thick meander design improved fracture strength of standard test chips from **339 to 350 MPa**. Standard deviation in the dataset also improved with thick meander chip design (Refer table 6.3 and figure 6.12. In the two designs, trench layouts and layer stacks are exactly same and purely the effect of metal pattern influences the die fracture strength during three point bending test.
   - Wider metal in this meander design is the key to improving die strength with this metal design layout. The die strength can be further increased by optimizing the meander design to facilitate wider metal area in direction of crack propagation.
   - In SEM observations for die failure analysis, two crack initiation locations were identified for thick meander chip design.

   Location 1: Metal absent gap between Gate-Source area along the vertical trenches.

   Location 2: Crack in the vertical trenches under the metal area away from the meander pattern.

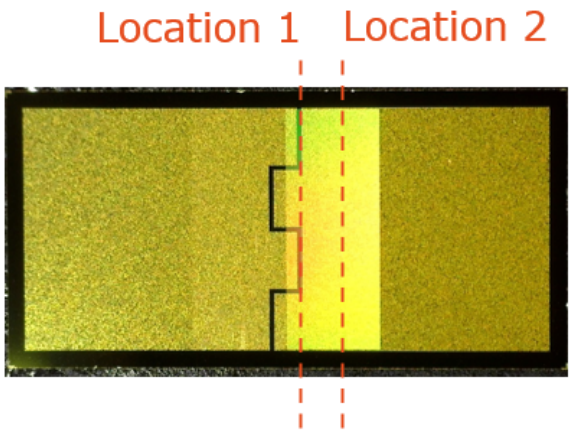


Figure 6.13: *Die crack seen observed at the meander path in metal absent region (left), closer inspection reveals crack initiation along vertical trenches (right)*

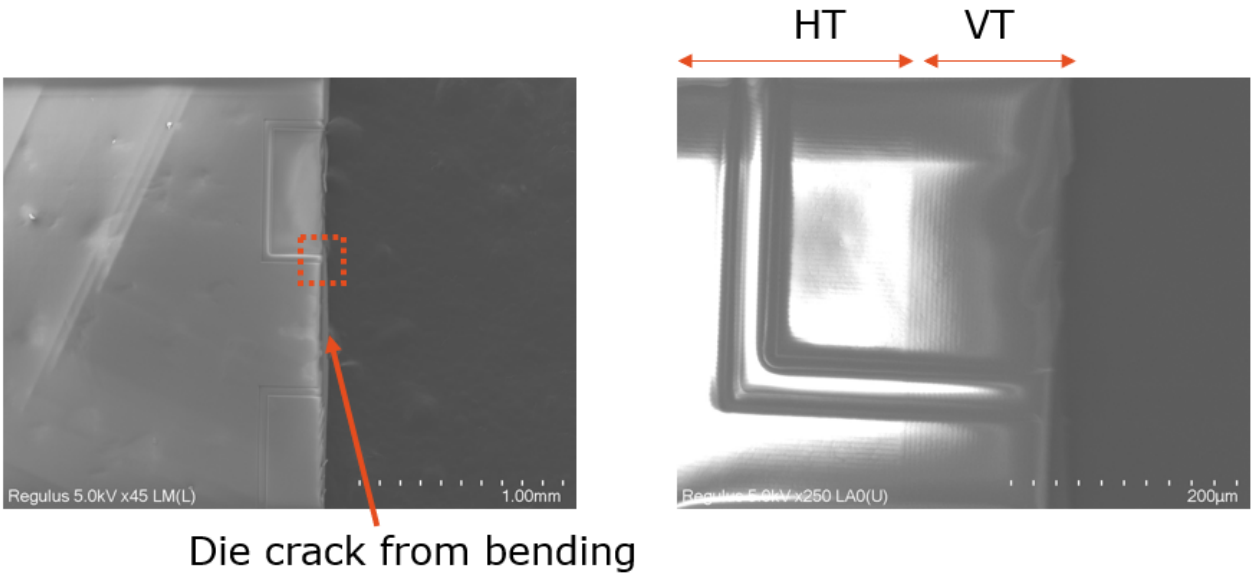


Figure 6.14: *The SEM image of die crack seen at the meander path in metal absent die region (left), closer inspection reveals crack initiation along vertical trenches (right)*

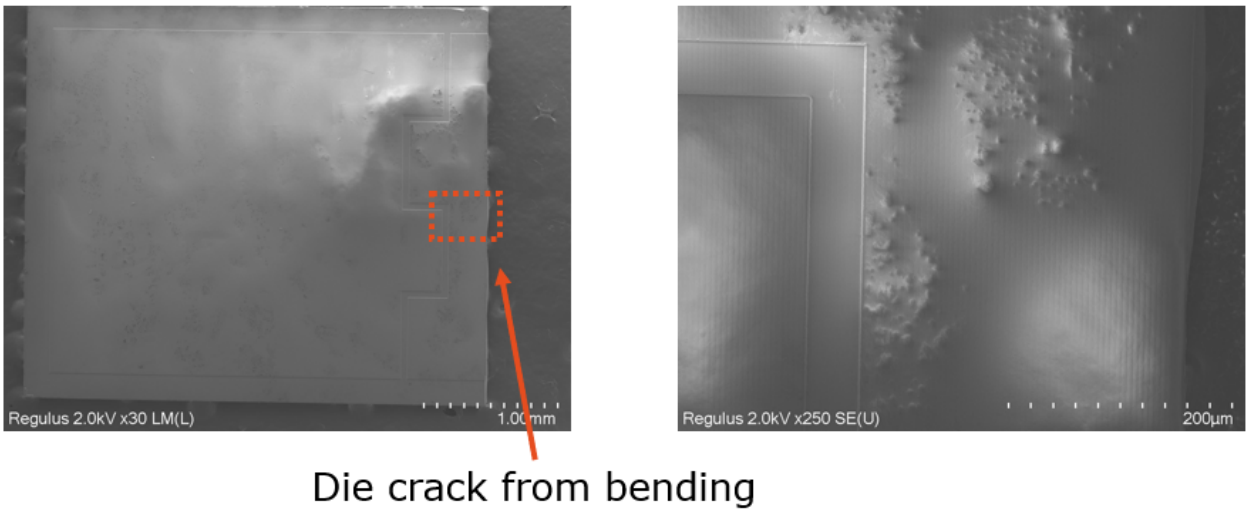
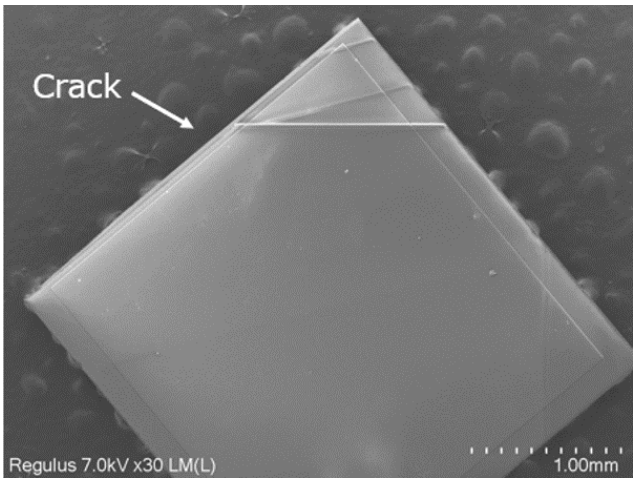
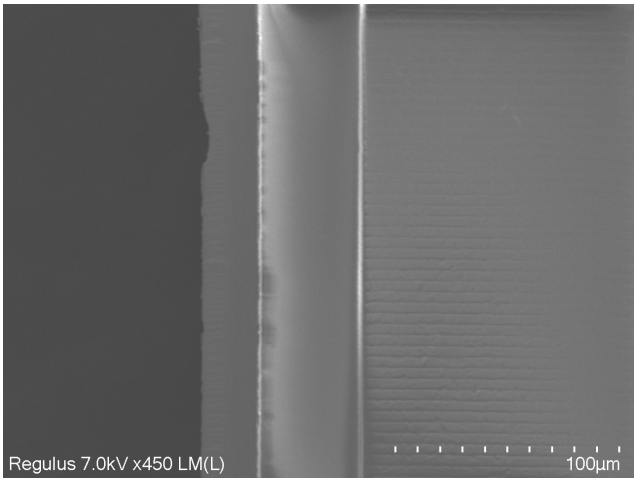


Figure 6.15: *The SEM shows die crack seen in thick meander die at location 2 (left) and closer inspection reveals crack initiation along vertical trenches under the metal (right).*

2. **Die with trenches only under metal:**
    - In this design, trenches are removed from under the gate-source separation gap where metal layer is not present. Trench layout is strictly kept under metal covered layer.
    - Die design with trenches strictly under metal layer show increase in die strength from **339 MPa to 364 MPa**.
    - Metal are high fracture toughness materials [13] and they prevent crack initiation and its propagation across it.
    - Die failure analysis is performed using SEM to observe crack initiation locations. Trenches are critical hot-spots for die crack initiation. Die areas with trenches not covered with metal top show high risk of die crack. In the figure 6.16a and 6.16b, die cracks are found to initiate in region where vertical trenches under metal in contrast to standard test chip where the dies are seen to crack in trenches under metal absent die middle location.
    - Trenches are thus observed to be critical hot-spots for die crack initiation. Die areas with trenches not covered with metal show high risk of die crack.



(a) *The SEM image shows die crack in location away from metal absent gate-source gap and in the trench covered source metal area.*



(b) *Higher magnification SEM image shows die cracks in metal covered vertical trenches in source region of die. Crack propagates in the same direction as direction of trenches.*

Figure 6.16: *SEM analysis for die crack for thick meander chip design.*

6.5.4. Polyimide analysis as new die top material

Polyimide (PI) is investigated as potential new die top material to act as mechanical buffer to relieve die stress. PI film for two different thicknesses (5 μm and 10 μm) were added on top of standard test chip for this chip design and then data is compared with our standard test chip without any PI. Warpage was observed in the dies with thick PI film because of high amount of shrinkage in PI layer during the curing process. This warpage was reduced using the annealing process to relieve the stress in PI layer.

The Fracture strength data of standard test chip with PI is also compared with bare silicon dies (no trenches and pattern) silicon and metal are also plotted in the Weibull plots for a better comparison. The study is divided into experimental analysis of effect of thick PI film on 1) die strength and 2) die bending deflection.

Effect of PI film on die frontside strength

To measure the die strength for dies with PI top, the new analytical equation derived earlier for calculating individual stresses in dies with films of varying young's modulus is used (refer 6.2. PI is a soft high compliance material so the maximum bending stresses (tensile stress) are seen in silicon layer underneath instead of PI, So we calculate for maximum bending stress for Silicon substrate thickness. This reasoning is later validated using finite element analysis as discussed later in this chapter.

Chip design	Average die strength (MPa)	Standard deviation	die thickness (um)	Sample size
Standard test chip	339	51	51	40
Bare Si die	790	108	51	40
Bare Si + metal die	920	87	51	40
Standard test chip + 5 um PI	760	101	46	40
Standard test chip + 10 um PI	801	104	52	40

Table 6.4: *Data comparison between standard test chip and dies with Polyimide and bare dies without trenches*

The key observations from the table 6.4 and probability plot for weibull distribution in figure 6.17 are discussed below:

- Dies with **5 μm PI film** PI top show significant improvement in their fracture strength from **(339 MPa)** to **(760 MPa)** as compared to standard test chip with nitride top.
- The increase in fracture strength with PI film can be explained as PI prevents crack from initiating. Die crack is found to initiate at sharp corners, trenches and with addition of PI on die top, it is harder for crack to initiate and propagate. The polyimide also offers good fracture toughness and tensile strength [12, 13, 14].
- Some increase in die strength can be attributed to pre-stress (tensile) in PI film because during the three point bending test, the applied load first needs to overcome the pre-stress before silicon underneath is stressed. Thus dies with PI film break at higher load force.
- **10 μm thick PI film** did not increase the die strength as substantially as compared to 5μm PI film. Note that increasing the PI thickness to 10 μm also means decreasing the amount of the silicon substrate to ensure a total 50 μm die thickness. This leads to increase in die warpage because of high tensile stress in PI film.

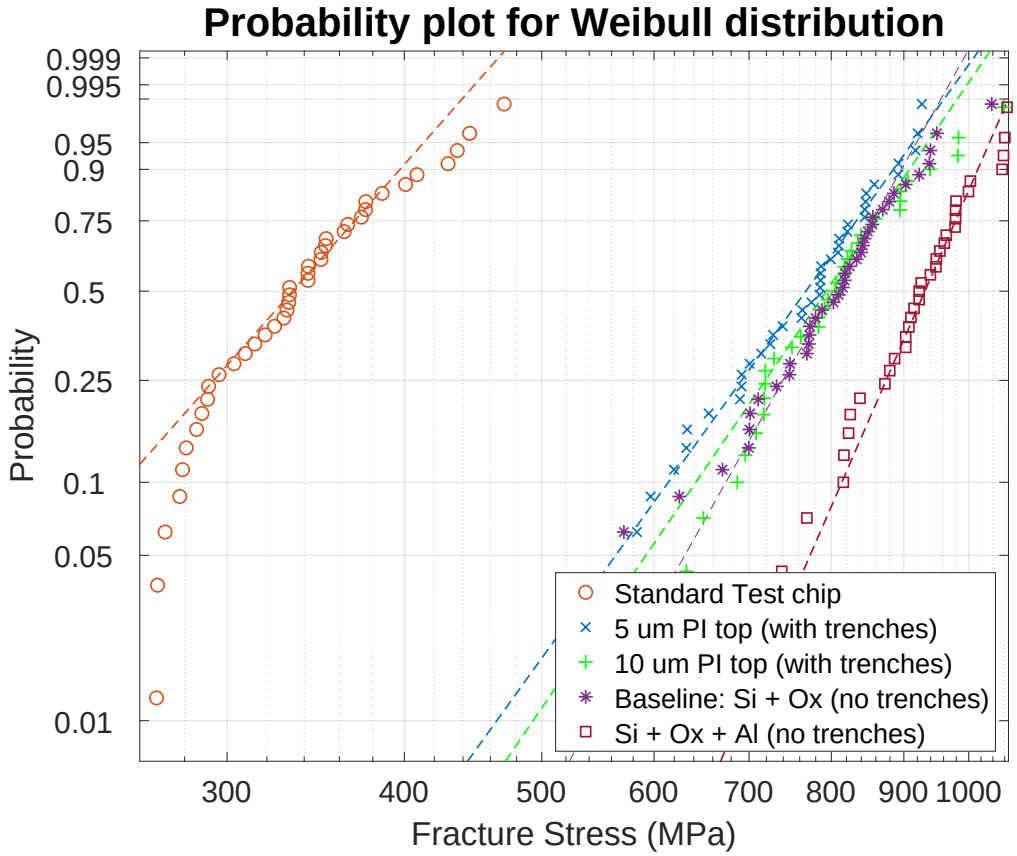


Figure 6.17: *Weibull probability plot implying effect of PI addition on die strength compared to die without PI*

- 5 μm PI film makes die with trenches and patterned metal layer as strong as bare silicon die without trenches and patterns for the same die thickness (refer to data in table 6.4).
- The influence of metal deposition on top of bare silicon die can be clearly seen in the weibull plot. The fracture strength of die increases from **790** MPa to **920 MPa** with deposition of 4 μm Aluminium on die top. Please note that both bare dies in comparison have similar thickness.
- The experimentally tested chips were deposited with PI film over the entire chip layout. Power MOSFET devices have openings on die frontside for attachment with copper clip package. A chip design is thus proposed with 5 μm PI film for commercial power MOSFET chips with maximized PI coverage area.

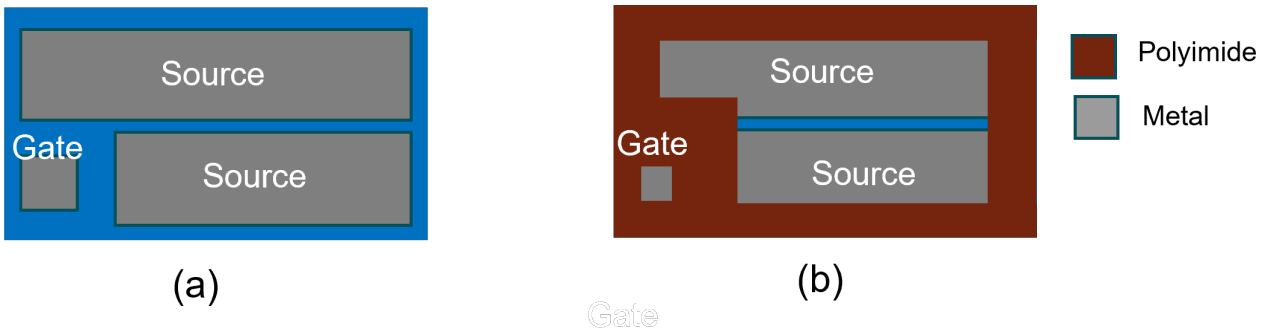


Figure 6.18: *(a) Standard commercial power MOSFET chip; (b) Proposed chip design with 5 µm PI film on front-side.*

Effect of PI on die bending deflection

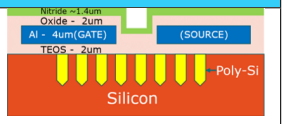
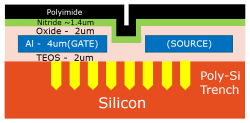
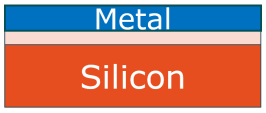
Chip design	Average Displacement (um)	Std. deviation	Die thickness (um)	Die cross-section
Standard test chip	207	51	51	
Standard test chip + 5 um PI	319	39	46	
Bare Si die	570	108	51	
Bare Si + 4 um Al die	757.5	87	51	

Table 6.5: *Data comparison between standard test chip and other die designs for maximum die bending deflection under applied fracture force.*

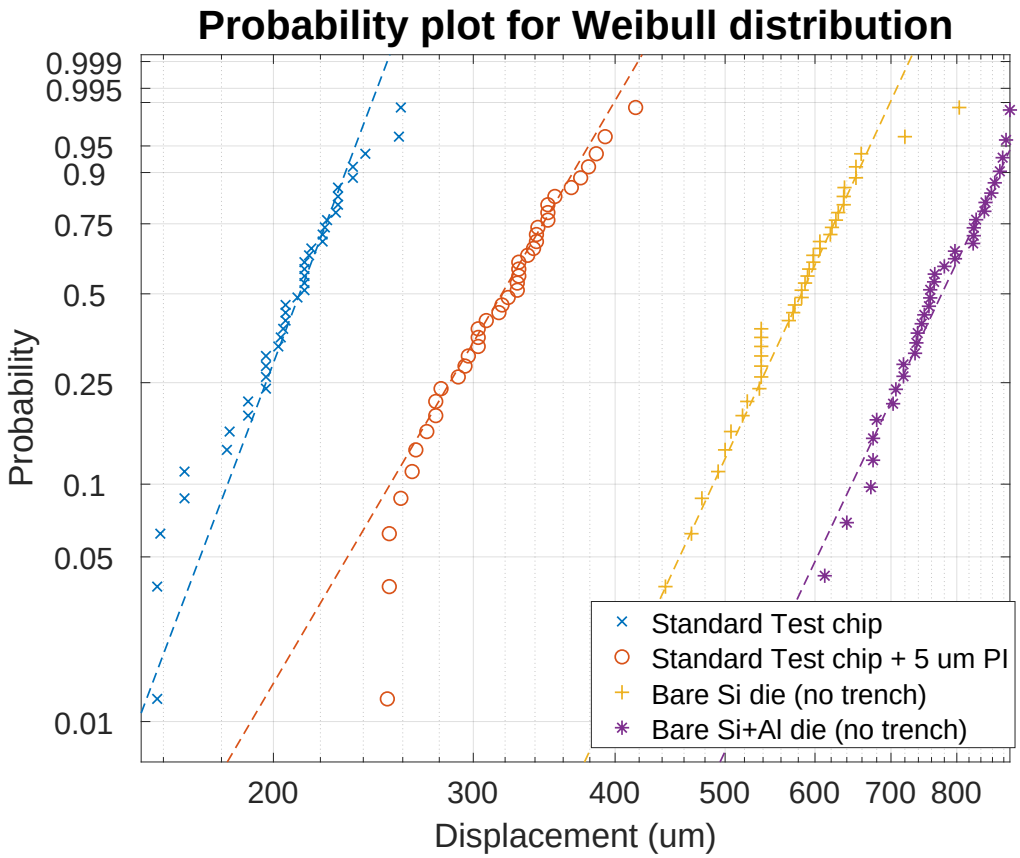


Figure 6.19: *Weibull probability plot showing effect of addition of PI film on bending displacement of thin die compared to dies without PI*

The key observations from the table 6.5 and weibull probability plot (see below figure 6.19) are discussed below:

- The bending displacement increases on addition of PI film on standard test chip from **207 μm** to **319 μm**. This can be explained as PI film is a very low stiffness material with low young's modulus as compared to brittle materials like silicon.
- The increase in bending deflection can also be explained as generally load vs displacement plot for die strength measurements are linear plots. Greater the load required to fracture the die, higher is the bending deflection. Dies with PI show higher frontside strength and thus a higher displacement is justified. .
- Bare dies like that of silicon and silicon with metal top show higher displacement due to higher fracture strength of these dies in the absence of trenches and metal patterns.

6.5.5. Metal layout and trench orientation interaction

In this study, the impact of trenches and their orientation on die strength is discussed. Two die designs with two different trench orientations (Horizontal and vertical) are compared. These trench designs are covered with a continuous layer of aluminium metal on top. In order to understand the amount of sensitivity induced by trenches in silicon, the designs are compared to Bare silicon dies with metal top. These bare dies have no trenches or pattern.

Chip design (6 X 3 X 0.051 mm)	Average die strength (MPa)	Standard deviation	die thickness (um)
Standard test chip	339	51	51
Vertical trenches + metal dies	395	47	53
Horizontal trenches + metal dies	400	51	51
Bare Si + metal die	920	87	51

Table 6.6: *Data comparison between dies with different trench orientation and die without trenches*

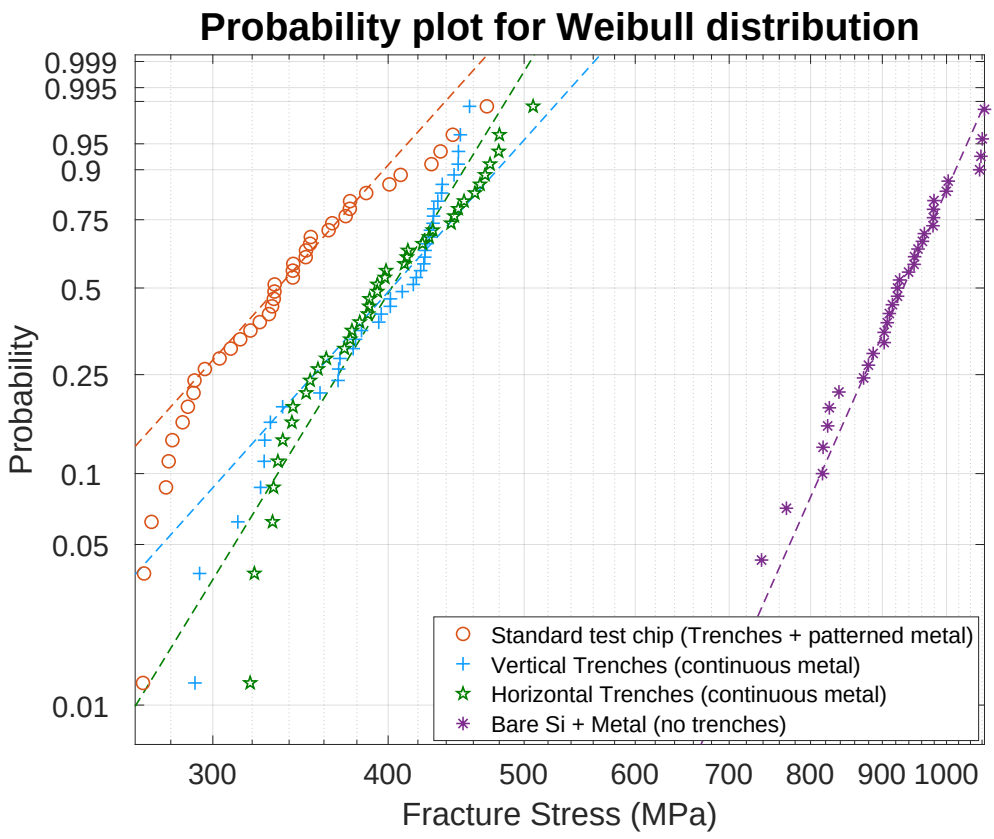


Figure 6.20: *Weibull probability plot for comparison of dies with and without trenches and continuous metal layer*

The key observations from the table and probability plot for weibull distribution are discussed below:

- Trenches play the biggest role in reducing die robustness. The fracture strength of bare dies without silicon trenches and metal top takes a nosedive from **920 MPa** to **400 MPa**.
- Horizontal trenches show higher resistance to die cracking compared to vertical trenches as vertical trenches are present in the direction of die bending axis.
- The effect of trench orientation in die strength is reduced by an addition of a continuous metal layer on top of trenches. In the absence of this metal layer, trench orientation will show higher sensitivity to die bending axis.

6.6. Result validation using Finite Element

Finite element analysis was performed using Comsol tool to observe the distribution and type of stress inside the chip under an applied load. A test chip is modeled with dimension 6 X 3 X 0.046 mm with layer stack of bulk Si substrate and 5 μm Polyimide on die top (Si + PI). The beam model used for the finite element analysis is discussed below:

- **Geometry:** The die is modeled in 2 dimensional plane as a rectangular block with two different material sections. Bulk of the beam is silicon substrate (41μm) with a thick film of polyimide top (5μm). Using design symmetry, the beam can be modeled to represent only half span length of die.
- **Materials:** The young's modulus and poisson ratio for PI is adjusted using the specifications provided by PI manufacturer [12]. Single-crystal, isotropic silicon with standard parameters is used to model bulk silicon substrate in die.
- **Solid Mechanics:** Prescribed Displacement function is used to specify the boundary conditions for the beam model. The boundary where the load is applied is fixed to prevent beam displacement in x axis and only vertical displacement (y-axis) is allowed as also seen in three point bending test. Another boundary condition is used to fixate the end of beam, here the beam movement is restricted in y axis and only displacement in x-axis is allowed which is brought by die slipping from the support beams during bending.
  Point Load is added in the silicon side of beam which is modeled to mimic load applied on silicon die backside during three-point bending test. Load applied here is similar to fracture load calculated in experimental three-point bending measurements.
- **Study:** Stationary study is used simulate the beam model and analyze the stress distribution. It is a time independent study.

From previous discussions it is known that during three-point bending test, the die first yields at frontside under tensile stress and in the figure obtained from the finite model shows 6.21 that maximum tensile stress is observed in silicon-PI interface. In trench MOSFET devices, poly-silicon filled trenches are present in this layer. Trenches are relatively vulnerable to stress compared to other process layers and is one of key reasons why die cracks are found to originate from trenches in MOSFET devices. Polymers like polyimide are relatively softer materials with high compliance and low young's modulus and hence the bulk of stress is seen in high stiffness materials like silicon in the thin die.

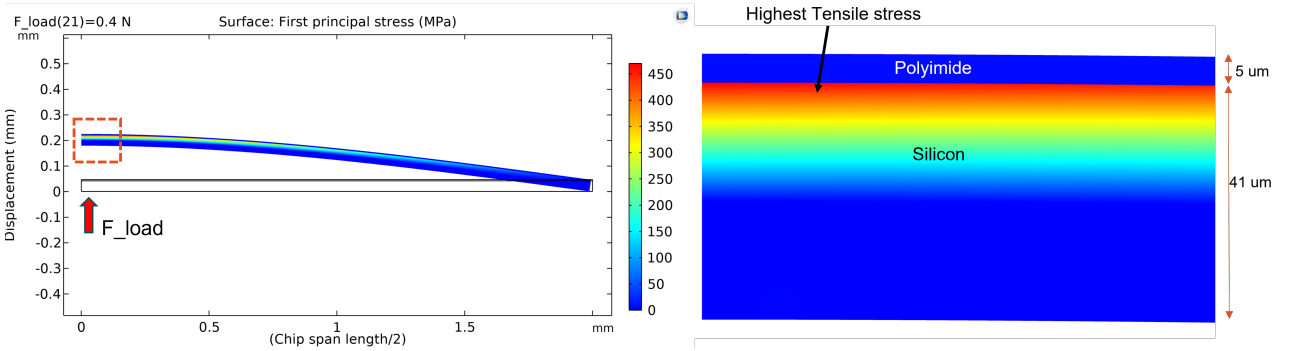


Figure 6.21: *FEA for tensile stress in thin silicon die with polyimide top. Maximum tensile stress (in red) is observed at silicon substrate. Soft materials like PI experience lower tensile stress (in shades of blue) because of their low stiffness.*

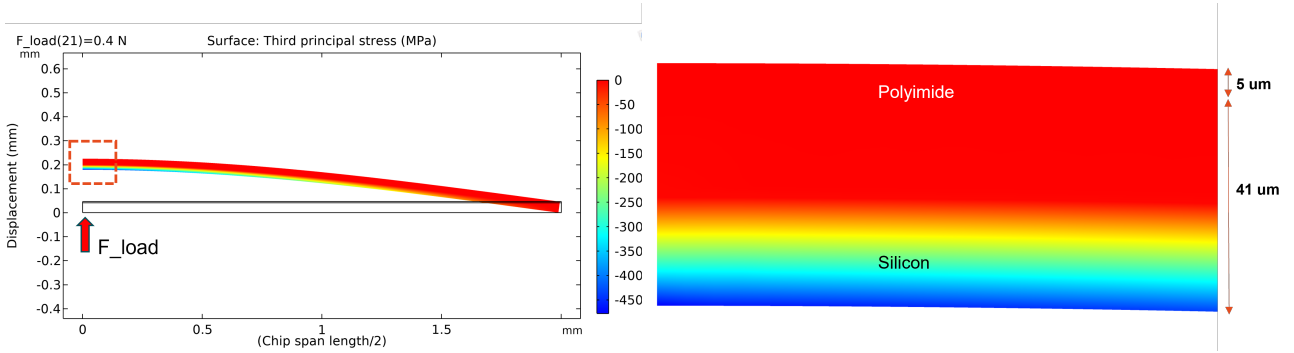


Figure 6.22: *FEA for compressive stress in thin silicon die with polyimide top. Maximum compressive stress (in red) is observed at silicon top where load is applied. Negligible compressive stress is observed in PI film*

6.6.1. New stress equation validation using Finite element analysis

For dies with PI top, new stress equation were derived (refer below and equation derivation can be found in 6.2 and 6.3). In composite beams with thin silicon and thick polymer top, standard flexural stress equation cannot be used as neutral axis and moment of Inertia are affected by the large difference in two materials young's modulus. Finite Element Analysis (FEA) is used to validate these analytical equation using a simple beam model with silicon and PI top. A point load of 0.4 N is applied in the middle of the silicon backside of the die to middle to mimic the three point bending test.

$$\sigma_{Si} = \frac{M y_{Si} E_{Si}}{(E_{Si} I_{Si} + E_{PI} I_{PI})}$$

$$\sigma_{PI} = \frac{M y_{PI} E_{PI}}{(E_{Si} I_{Si} + E_{PI} I_{PI})}$$

in the figure 6.23 for a Stress-Displacement plot, we observe that the scatter plots which represent the data from analytical equations as calculated separately for Silicon and PI material section satisfy both the curves representing Silicon and PI finite element analysis Stress-Displacement plots which validates the use of new stress calculations for dies with PI top.

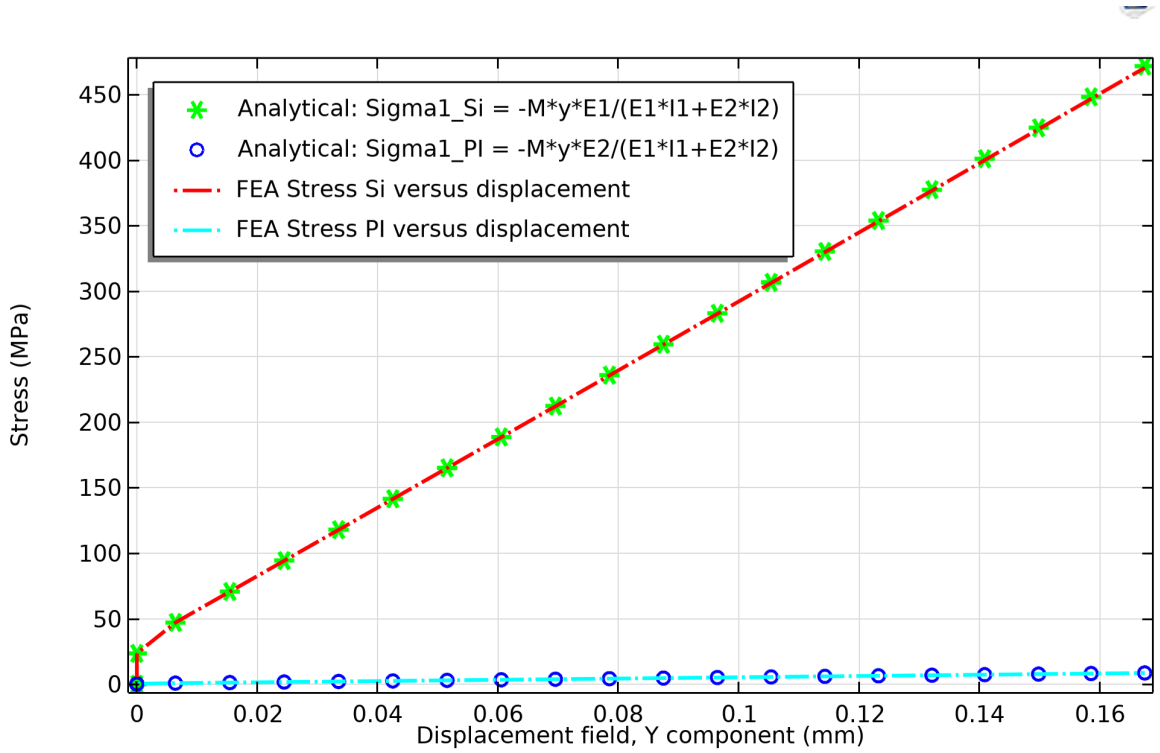


Figure 6.23: *Figure shows stress-displacement plot where stress in silicon and PI film calculated via new analytical equation satisfies the stress measured by the finite element model.*

6.6.2. Polyimide pre-stress analysis

In the three point bending tests for dies with PI top, large warpage was observed in thin dies where the PI top layer was found to be under tensile stress due to the large shrinkage in PI during curing process. Finite element analysis is used to simulate and compare different dies with or without pre-stressed PI top and also to understand the effect of silicon thickness on the chip stress levels

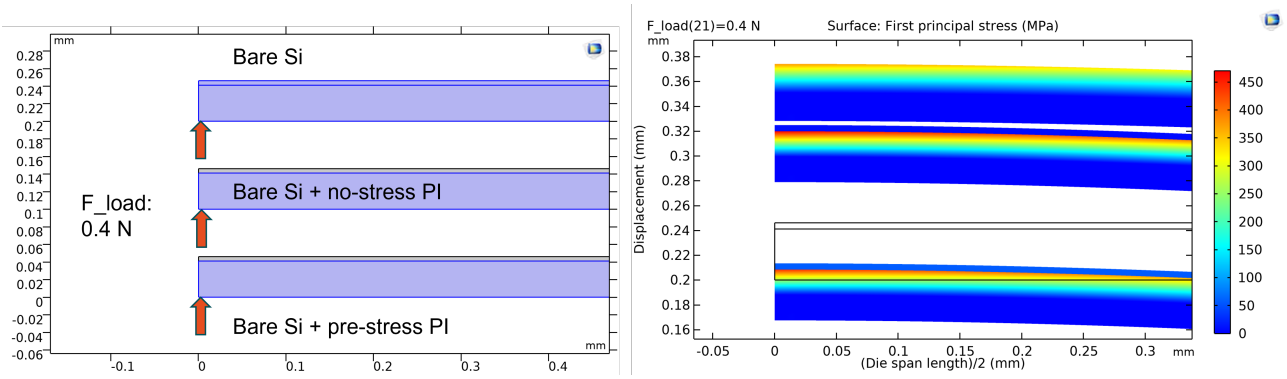


Figure 6.24: *Three different beams are modeled to analyze the effect of silicon thickness and PI film pres-stress on die stress measurements.*

1. **Bare Si:** In this model, highest stress was seen in the bare silicon die without PI. It is important to note that total silicon thickness is highest in this model (46μm). Higher the stress in silicon, lower is load required from the force indenter to make the die yield/fracture. This die shows lowest fracture strength.

2. **Bare Si + PI top (no stress):** In this die model with PI top with no initial stress in layer, lower stress was seen as compared to bare silicon die without PI. The total thickness of silicon in die is also reduced to 41μm and has a 5μm PI top. For a displacement of 120 μm, a difference of 100 MPa can be seen in the plot between the two models with or without PI (see figure 6.25)

3. **Bare Si + PI top (pre-stressed):** In practice, dies with PI top showed warpage because of pre-stress in PI from curing process. To investigate the effect of pre-stress on die strength, a practical finite model of die with PI top is used. Here the PI is pre-stressed (tensile) with a 50 MPa tensile stress which in practice comes from the material shrinkage during the curing process. In the fabrication process, annealing was used to minimize this pre-stress. The total die thickness is same as seen other PI top die (41 μm Si + 5 μm PI). In the stress-displacement plot (shown in figure 6.25), lowest stress was seen in the curve where PI was pre-stressed (tensile) which implies more load needs to be applied as the die bending first needs to overcome the PI pre-stress and die warpage before silicon layer underneath is stressed. So a greater load (F) is required before the die with pre-stressed PI film yields as compared to yielding force in other die models.

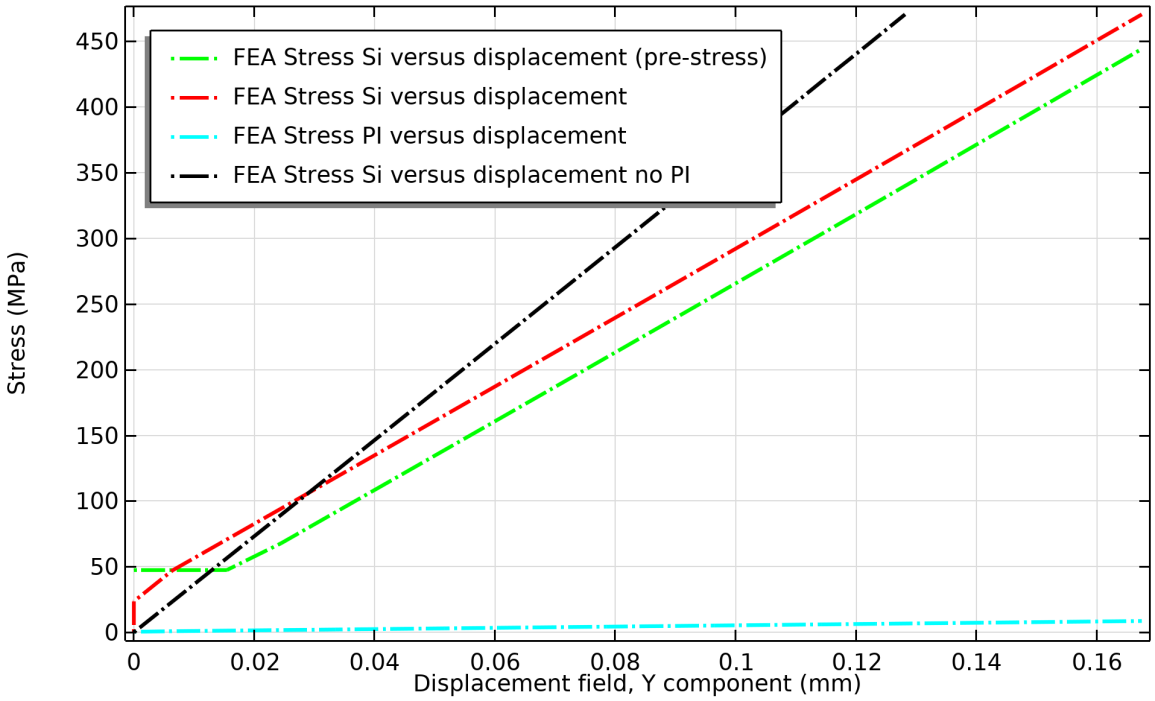


Figure 6.25: *Finite element*

6.7. 6-sigma methodology for robust assembly yield

In semiconductor manufacturing, 6-sigma methodology is used to monitor yield of semiconductor device manufacturing especially in fabrication and assembly process. In assembly, in order to achieve < 1 ppm die loss (99.999943 % success rate) for a robust high yield assembly process with high aspect ratio dies (6 X 3 X 0.050 mm), a 5-sigma limit is applied to get a robust semiconductor device yield to maintain a high throughput (refer figure 6.26). To achieve an even higher 6-sigma process yield, dies need to made more stronger because an additional sigma band means lesser forces and stresses can be applied on dies by the pushing needles or pick-up collet in the assembly process, making it more challenging to effectively pick-up and the place ultra-thin dies from the dicing foil.

In order to have a 5-sigma robust yield for high fracture risk devices, the pick-up and place tool need to operate at 5-sigma limit stress limits to avoid cracks or other failures during the process. This methodology also helps in performing root cause analysis and setting up desired performance standards for semiconductor devices during the process. As power MOSFET devices are becoming larger and thinner, they offer new challenges in maintaining a robust high yield assembly process. The 5-sigma limit value is becoming smaller and smaller making it difficult for the semiconductor manufacturing tools to sustain a high throughput as found in thicker devices (> 70 μm). It is therefore required to make ultra-thin dies stronger to achieve 5 or 6-sigma process yield.

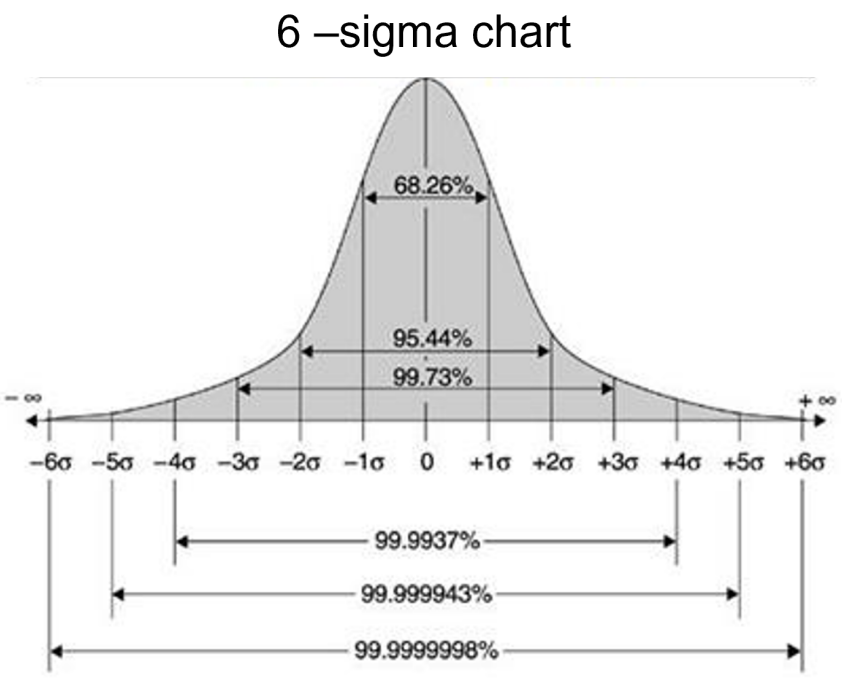
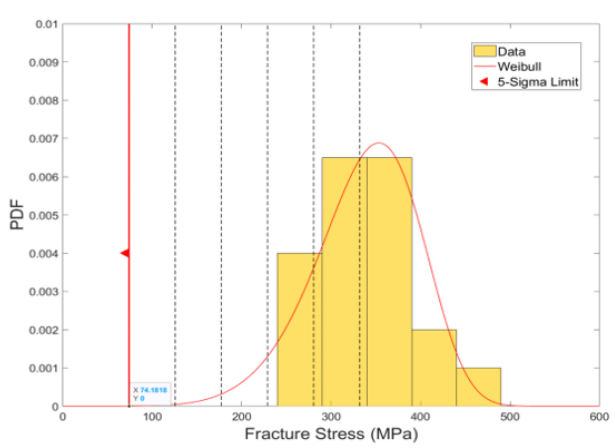


Figure 6.26: *6-sigma chart for monitoring yield in assembly process [36].*

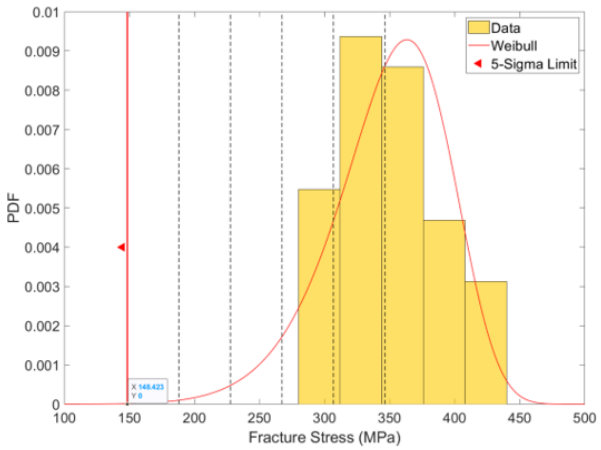
In this section, standard test chip (M1) and chip with thick meander design (M2) are compared to find chip design more robust to assembly process between the two. Table 6.7 shows the data for the two different chip designs.

Die design	5-sigma limit	Std. deviation	Sample size	Median fracture stress
Standard test chip (M1)	74 MPa	51	40	337 MPa
Thick meander chip (M2)	148 MPa	39	40	346.5 MPa

Table 6.7: *5-sigma limit value comparison between standard test chip (M1) and chip with thick meander (M2)*



(a) *Data distribution for standard test chip. This design shows a 5-sigma yield of 74 MPa.*



(b) *Data distribution for Thick meander chip. This design shows a 5-sigma yield of 148 MPa.*

Figure 6.27: *Data distribution for the front-side die strength of standard test chip (M1) and thick meander chip (M2). 5-sigma value for robust high yield assembly process can be obtained from this distribution.*

The performance of thick meander chip (M2) is found better than standard test chip (M1) where the 5-

sigma limit value increases from 74 MPa to 148 MPa which is a 100 % increase in die robustness in assembly process.

6.8. Chapter Summary

Die strength characterization realized for different test chip designs using three point bending test. A new analytical equation was derived for stress calculations in composite beams and were validated using finite element analysis. The obtained data is analyzed using probability plots for weibull distribution. Die design with thick meander metal layer pattern, design where trenches are strictly kept only under metal area and dies with PI top are found to show positive improvement in die robustness at frontside. A finite element analysis was done to understand the influence of pre-stress in PI film on strength measurements. Use of 6-sigma methodology is discussed at the end to compare assembly yields between chip designs.

7 SUMMARY AND CONCLUSIONS

7.1. Project Summary

In order to meet the continuously increasing demands for high performance and efficiency to drive the electrification of automotives, power MOSFET dies are becoming larger (> 5 X 5 mm) and thinner (< 50 μm). This high aspect ratio die design along with presence of advanced trench technologies in the dies, increases the risk of die failure during the subsequent semiconductor processes like assembly, packaging and testing. The project aimed to take on this challenge and use novel materials and designs to make next generation power MOSFET dies more mechanically robust and to find a way to use a test chip to speed up the semiconductor manufacturing process.

Factors like interaction of trenches with metal and their orientation was investigated to find more insights into die crack behavior under stress. In the experimental study, chips with different metal patterns, trench orientations and die top materials were investigated to experimentally validate the effect of new design and approaches on thin die robustness. The process steps involved in the study are briefly discussed below.

1. **Die design:** The process flow starts with die design. In chapter 3, various metal layer and trench pattern designs along with a design of experiment (DOE) is discussed. The DOE highlights different combination of mask patterns and layers for die design for fabrication.
2. **Sample fabrication:** The die designs discussed in DOE are fabricated on 100 mm n-doped silicon wafers (refer chapter 4). In total wafers with 20 designs were fabricated to study and find new design approaches to improve frontside die robustness. An in-depth analysis for obtaining high aspect ratio trenches were also presented in chapter 4.

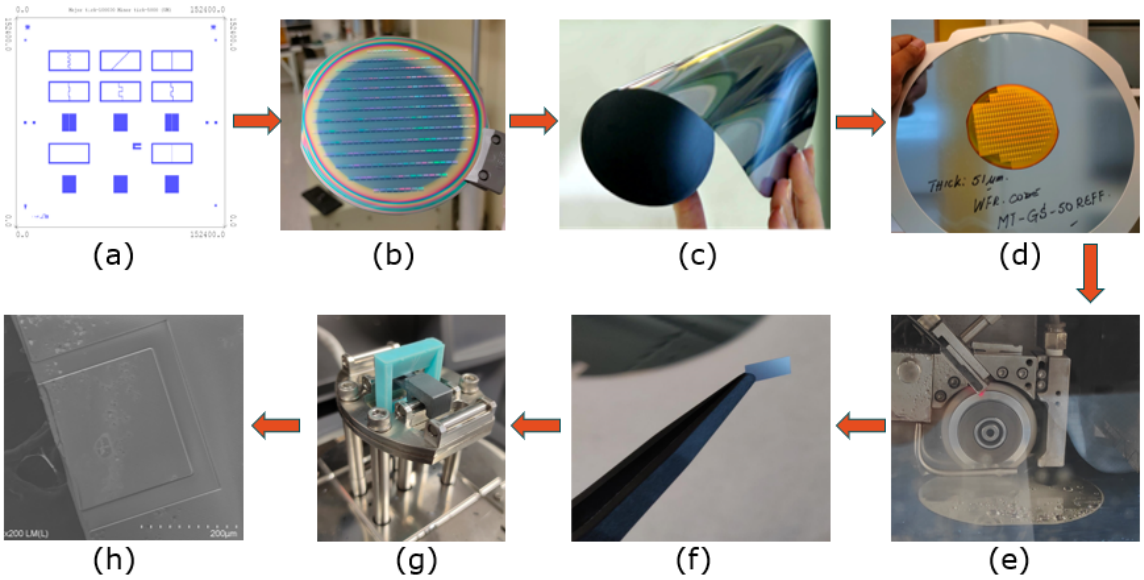


Figure 7.1: *Figure shows the flow for the various process steps in the project. (a) Mask cell for different metal and trench designs,(b) die fabrication on 100 mm silicon wafers, (c) Wafer thinning from backside t0 50 µm. (d) Low adhesive UV foil for mounting thin wafer, (e) wafer dicing for die singulation, (f) Die pick up with tweezers, (g) Die bending test for strength characterization, (h) Die failure analysis in SEM*

3. **Wafer backside thinning:** Processed wafers are grinded from backside to obtain 50 μm ultra thin silicon wafers (refer 5). It was ensured that backside roughness across all wafers is minimum and

constant to mitigate its effect on die strength measurements later. High flexibility and warpage was observed in thin silicon wafers.

4. **Wafer dicing for die singulation:** Grinded wafers were mounted on low adhesive UV foil and diced using sawing blade to obtain chips of dimension 6 x 3 X 0.050 mm (refer 5). Some chipping damage was observed on die edges but using same process parameters for dicing each wafer minimized effect of dicing on die strength measurements.
5. **Thin die pick up:** The low adhesive UV foil allows thin die pick up from foil without damaging the die. The foil is overexposed in UV light for 7 min as compared to standard 4 min which reduces the peel force for die pickup. Dies are pushed from backside manually and picked with tweezers.
6. **Die strength measurements:** Three point bending test are used for measuring frontside fracture strength of our sample dies. Die breaking load (F) and displacement (D) are measured from the test and used to calculate fracture strength of die samples for different designs. A sample size of 40 dies is tested for each die design and in total over 1000 dies are tested for strength characterization in this project. The datasets are analyzed for different designs using probability plots for weibull distribution See chapter 6.
7. **Die failure analysis:** The fractured dies are observed under SEM for failure analysis. Finite element analysis is done to explain behaviour of materials like PI. The observations from SEM analysis, in combination with finite element and weibull plots are used for reaching conclusions and deepening our understanding on thin die robustness.

In chapter 6, the results from the three-point bend test were shown in form of probability plots for weibull distribution and data distribution plots for 5-sigma limit of various chip designs.

In order to compare die strength between various chip designs in DOE, a reference chip was fabricated namely standard test chip (see figure 7.2). This chip is fabricated to mimic mechanical robustness of commercial trench power MOSFET and in three-point bending experiment, the die strength and data distribution agrees well with the commercial power MOSFET thus validating the standard test chip as an ideal reference for the comparative study with other chip designs.

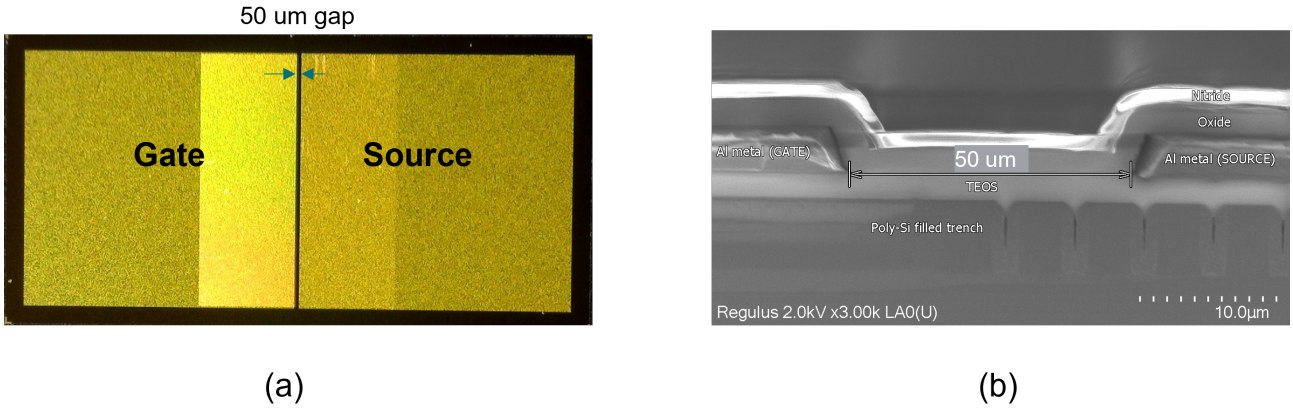


Figure 7.2: *(a) Standard test chip outline; (b) Chip cross-section.*

Different chip designs were fabricated, tested and compared to standard test chip for evaluating their positive or negative response to die strength. Some of the designs did not perform as expected and resulted in decrease in die strength. However some new dies designs are found to improve frontside strength of thin dies. A bar graph chart showing front-side strength for different chip designs is shown below in figure 7.3. The chip designs cover different design aspects such as 1) effect of new metal layouts; 2) effect of materials such as polyimide as stress buffer; 3) metal-trench interaction.

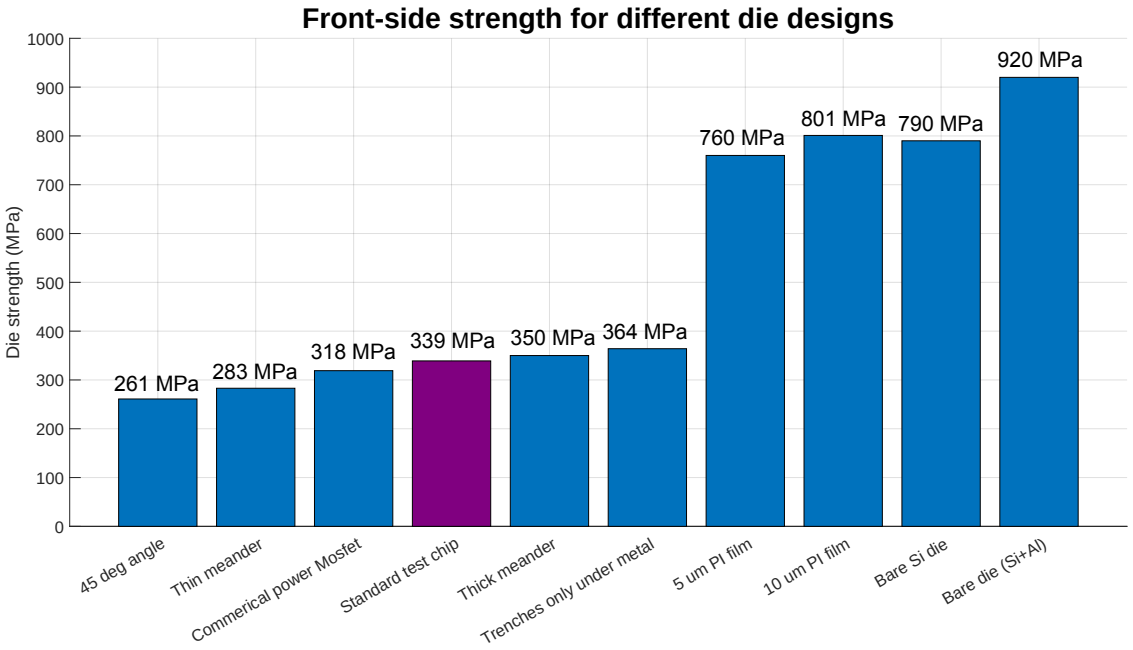


Figure 7.3: *Bar chart showing front-side die strength of different die designs*

7.2. Conclusions and Recommendations

- Die strength of standard test chip is found to improve significantly from 339 MPa to 760 MPa with addition of 5 μm PI film (see figure 6.17) . We therefore conclude and recommend a 5 μm thick PI as new die top film on top of nitride layer in power MOSFET devices to reduce the risk of die crack. The film can be patterned to cover vulnerable areas to improve die robustness in assembly, packaging and testing. The PI will also act as stress buffer to relieve die stress between the nitride and hardened epoxy moulding compound (EMC) in the package. Die cracks generally initiate around the sharp corners or trenches and the soft PI film addition is found effective to prevent this crack initiation and propagation.
- A 10 μm PI film did not show a significant die strength increase as compared to 5 μm PI film (see figure 6.17). Hence, we suggest that 10 μm PI film should not be used because they are also not cost effective and they bring new processing challenges.
- In this study, PI film was deposited to cover the entire test chip to investigate its effect as stress buffer on the entire chip layout (gate-source). In practice, PI cannot be use to cover the entire chip. We therefore recommend to maximize polyimide coverage area over the power MOSFET chip, which is limited not only to edges but the maximum area of the chip while leaving essential space for clip attachment to get maximum benefit of strengthening effect of polyimide (see proposed chip schematic in figure 6.18). PI film also has potential application in GaN based power MOSFET devices to reduce nitride passivation crack challenge in dies.
- Thicker meander design is found to increase die fracture stress from 339 MPa to 350 MPa (refer figure 6.12). It is thus concluded and recommended to replace the traditional gap between gate-source metal area with a thicker meander gap only if electrical performance is not affected.
- Experimental results show that trenches are hot-spots for die crack initiation. Die areas with trenches that are not covered with metal, show higher risk of crack (see figure 6.12). A design rule is therefore recommended to keep trench layouts always under metal layer as covering the trenches with metal reduce the risk of crack in ultra-thin dies.
- In the SEM observations for die crack analysis, die crack was found along vertical trenches in the majority die samples (see figure 6.15 and 6.14). Thus, we conclude that alignment of die bending axis and trench orientation are critical. A continuous metal layer, covering the trenches is found to

reduce the effect of different trench orientations (refer figure 6.20) and is therefore recommended as a solution to reduce the effect of trench orientations on die frontside strength.

- The study also highlights the influence of wafer/die bow and warpage on die strength (refer figure 6.25). A follow up study is required to investigate and correlate effect of different metal designs, materials such as polyimide, trenches on wafer/die warpage.
- PECVD silicon oxide mask is recommended for fabricating high-aspect ratio trenches (refer figure 4.21b) as compared to photoresist mask.
- A new study is proposed to investigate novel materials such as Polyamide-imide (PAI) as die top stress buffer. It is an ideal candidate for die top as it is semiconductor manufacturing compatible and offers very high fracture toughness [13] and glass transition temperature as compared to regular polyimides.

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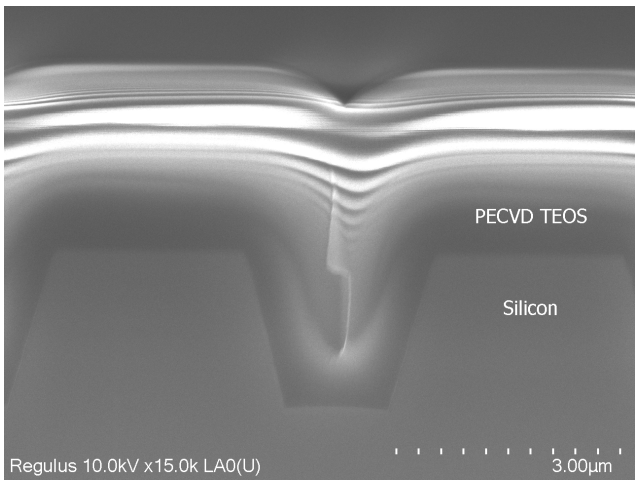
A Appendix A

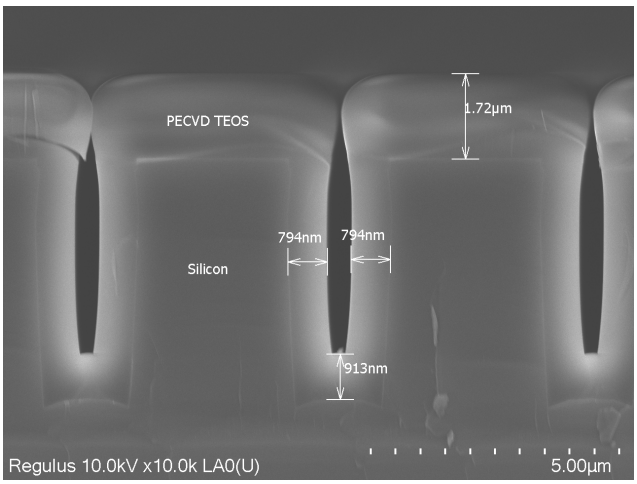
A.1. Trench filling with PECVD TEOS

Trenches obtained with polyimide and PECVD oxide mask were filled with PECVD TEOS. In case of shallow trenches, void-free filled trenches are obtained because of tapered trench sidewalls. In deeper trenches, the curved sidewall leads to trench filling with big voids in middle.

In our test design, deeper trenches are fabricated to replicate sensitivity of commercial trench power MOSFET. In order to reduce void size LPCVD (low pressure deposition) was used in place of PECVD deposition method as it provides more conformal trench filling. Thus, reducing the size of trench-voids which is desired.



(a) *SEM image showing PECVD TEOS filled shallow trench. No voids seen in trench filling.*



(b) *SEM image showing PECVD TEOS filled deep trench. Big voids are seen in trench filling.*

A.2. Effect of wedge radius on die strength measurements

The standard force indenter with DMA tool for three point bend test is a clamp with high radius steel cylinder (radius = 1.75 mm) with low compliance (< 0.6 um/N). The data from initial sample testing showed high data variations which corresponds to high standard deviation in the measured data. An experimental test was conducted to study the influence of wedge radius on die strength results. To compare, a custom made resin indenter was printed with a sharp wedge (radius = 0.25mm) which shows higher compliance (2.4 um/N) to compare the datasets obtained from two different radii wedges i.e. higher radius and sharp clamp. The higher compliance of the clamp does not affect the measured breaking force for bending strength measurements, this was also confirmed with the tool manufacturers. The test was conduced on silicon dies (Dimension: 6 X 3 X 0.051 mm) with process layers of silicon oxide and aluminium metal on top. The test results are shown below in table A.1 where we compares the average die strength and standard deviation for a sample of 30 dies with both radius wedges. M1 refers to test strategy with high radius wedge whereas M2 refers to test strategy with sharp wedge. The figure A.2 shows the probability plot for weibull distribution for the two wedges.

Parameters	High radius wedge (M1)	Sharp wedge (M2)
Average die strength	1208 MPa	919 MPa
Standard deviation	215 MPa	87 MPa

Table A.1: *Sample of 30 dies with thickness of 51 µm were tested and compared for two different radius wedges to study their influence on die strength. Sharp radius wedge (M2) is found to perform better than high radius wedge (M1).*

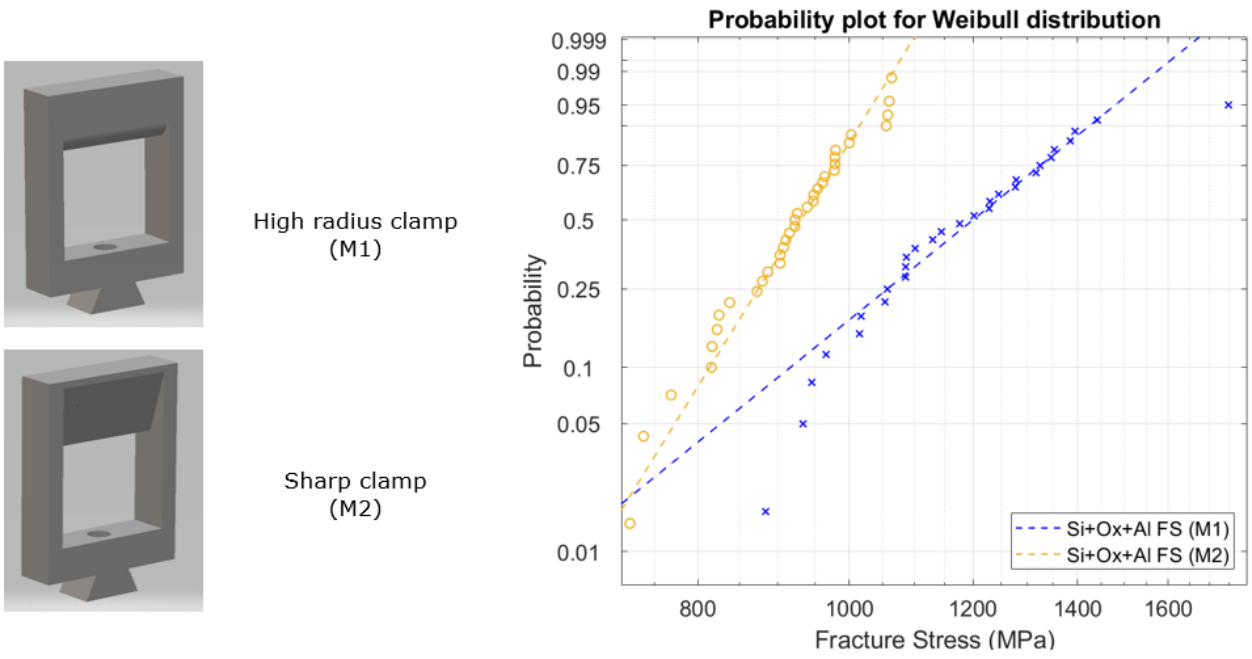


Figure A.2

Observations

- Standard deviation in the measured data reduced drastically from 215 MPa to 87 MPa by using sharper clamp. The probability plot for M2 had higher slope than M1
- Lower standard deviations reduce data variations between the sample size
- The average die strength is reduced from 1208 MPa to 919 MPa. The new data is found to be in good agreement with bare 50 μm thick silicon die strength as seen in literature [15].

Reasoning

- The boundary conditions of high radius clamp affect the load application and data measurement.
- Large area contact clamp are not supported by stress equations.