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ZVT Interleaved High Step-Up Converter For Renewable Energy Systems

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***Abstract*—In this paper, a novel interleaved high step-up (HSU) converter is presented. The proposed converter features a large voltage gain and common input-output grounding. In this interleaved HSU converter, by using only one zero voltage transition (ZVT) auxiliary circuit with one auxiliary switch and low number of elements, soft switching (SS) performance for all the semiconductors over a wide range of load variations is achieved. This leads to advantages of high efficiency and low complexity, expense, and size. The characteristics of the proposed converter are compared to similar state of the art converters, and to confirm its effectiveness, the simulation results of the proposed converter are presented.**

Keywords— High step-up (HSU) converter, interleaved converter, renewable energy (RE), soft switching (SS), zero voltage transition (ZVT)

I. Introduction

High step-up (HSU) converters are among the necessary components of many renewable energy (RE)-based industries [1]. In such applications, since the output voltage of the RE sources is usually low, HSU converters are demanded in the role of high gain interface circuits to deliver power to the grid or other loads [1]-[11]. Another important application of HSU converters is in the pulse generators (PGs) used in electroporation [12]. In electroporation, cell membranes of dangerous microorganisms are attacked by a sequence of high voltage pulses. In these PGs, a low input voltage is increased to a proper high output voltage by a HSU converter. Afterwards, a high voltage switch is used to generate high voltage pulses.

If an application does not demand electrical isolation, it is preferred to use non-isolated converters because they are usually more compact and affordable in comparison to the isolated topologies [1]. In many non-isolated HSU converters, to reduce the input current ripple and the semiconductors current stress, and improve the heat sharing, an interleaved structure is used [3]-[11].

In interleaved HSU converters, similar to other DC-DC converters, the switching frequency should be tuned to be high enough to decrease their volume and enhance their transient response. However, to suppress the problems associated with high switching frequency such as increased switching losses and EMI, different soft switching (SS) techniques are presented in literature for interleaved HSU converters [3]-[11]. SS techniques can be categorized to passive [2]-[4], and active SS methods [5]-[11]. Interleaved HSU converters which employ active SS techniques, can use simple and typical PWM control methods. The most used active SS techniques in HSU converters are active clamp [5]-[8], and zero voltage transition (ZVT) methods [9]-[11]. In the interleaved HSU converters which use active clamp circuits, the main switches turn on at zero voltage switching (ZVS) condition. This eliminates the switching and capacitive turn on losses. However, they employ one set of active clamp circuits with an auxiliary switch for each interleaved phase which adds to the converter cost, size, and complexity. Also, in these converters, SS performance is lost at light loads [5]-[8]. In contrast, in the ZVT interleaved HSU converters introduced in [9]-[11], full SS performance is achieved over a wide range of load variations. The converter introduced in [9], requires two auxiliary circuits with two additional switches and series diode with main switches which increases the conduction loss. The ZVT interleaved HSU converter of [10] needs one auxiliary circuit per phase while it does not operate at full SS condition. Using too many elements especially extra active switches, in addition to significantly increasing the cost of the system, creates a lot of complexity. The ZVT interleaved HSU converter presented in [11], uses only one auxiliary circuit with low number of elements for two phases but it suffers from lack of common input-output grounding.

This manuscript introduces a novel ZVT interleaved HSU converter for RE applications. In the proposed converter, ZVS condition at turn on and turn off transitions for the main switches, zero current switching (ZCS) condition at the turn off instant for all the diodes, and ZCS performance for the auxiliary switch are achieved over a wide range of load variations. This SS performance relieves the switching losses and the diodes reverse recovery problem and enhances the

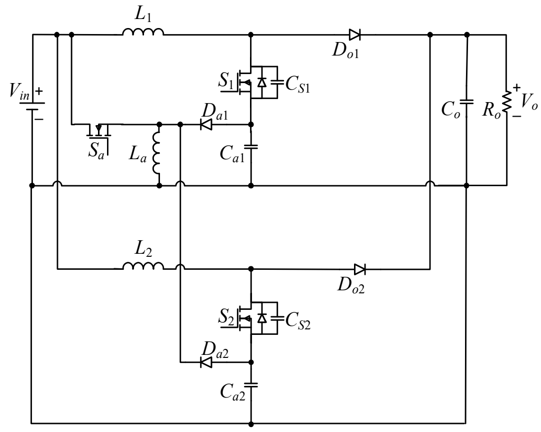

Fig. 1. Proposed ZVT interleaved HSU converter.

converter efficiency. The ZVT cell utilizes only one switch and a low number of passive components. In the proposed converter, in contrast to many of its counterparts [9]-[11], the ZVT cell in addition to providing SS performance, helps to increase the voltage gain. The proposed HSU converter uses series capacitors to increase the voltage gain. Due to using interleaved structure, the semiconductors current stress and the input current ripple are low which extends the RE system life span. The proposed converter also benefits common input-output grounding feature.

II. Proposed Converter and Operational Principles

A. Proposed Interleaved ZVT HSU Converter

The introduced interleaved ZVT HSU converter is presented in Fig. 1. In this converter, S_1 and S_2 denote the main switches; D_{o1} and D_{o2} represent the main diodes, and R_o and C_o are the output load and capacitor, respectively. The ZVT cell consists of the auxiliary switch S_a, the auxiliary diodes D_{a1} and D_{a2}, the small auxiliary inductor L_a, and the switches snubber capacitors C_{S1} and C_{S2}. The auxiliary inductor L_a has three key functions: its current helps to completely discharge the snubber capacitors and provide ZVS turn on condition for the main switches; it helps to establish ampere-second balance of C_{a1} and C_{a2}; and it is the turn on snubber for the auxiliary switch. The energy stored in the capacitors C_{a1} and C_{a2} which are located in series with the main switches, help to increase the converter voltage gain.

B. Operational Principles

The proposed converter is analyzed at the steady state. S_1 and S_2 operate with the same duty cycles but 180º phase difference between their gate signals. Because of its symmetrical structure, L_1=L_2=L, C_{a1}=C_{a2}=C_a, C_{S1}=C_{S2}=C_S, and the semiconductor elements of the two phases are similar. Besides, it is assumed that L_1 and L_2 values are high enough so that their currents are continuous and constant. Based on these assumptions, there exist twelve operational modes in each switching period (T_{sw}), but considering the equality of two interleaved phases, only half a switching period, which consists of six modes is reviewed here. Figs. 2 and 3 respectively represent the key waveforms and the modes equivalent circuits.

Before t_0, S_a and S_1 are ON, and all the other semiconductor elements are OFF. L_a is getting charged by V_{in}

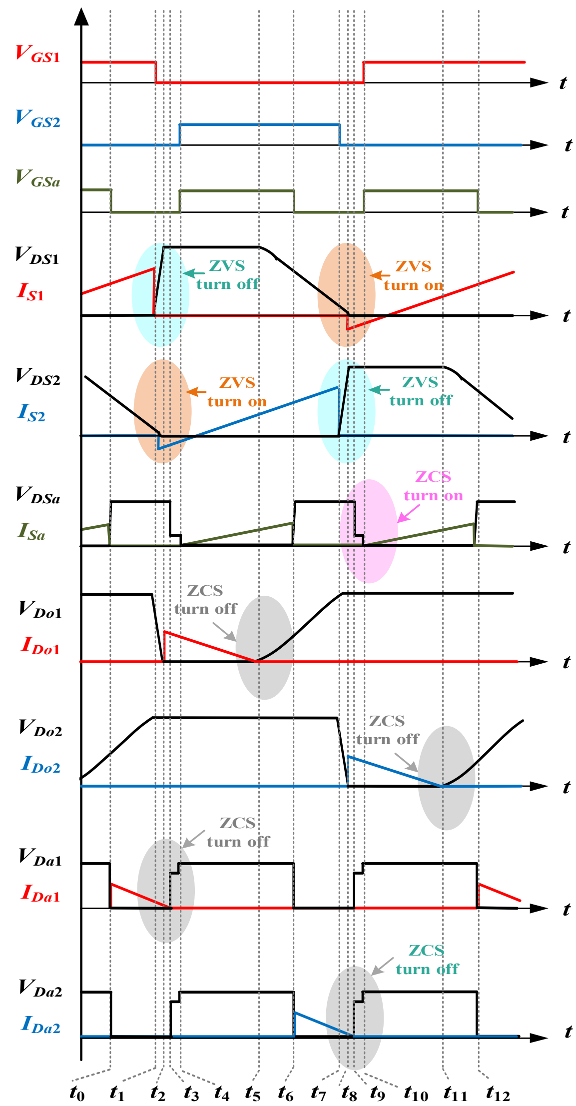

Fig. 2. Key waveforms.

as well as the energy stored in C_{a2} and C_{S2}. C_{a1} is being charged by I_{L1}. At the output, C_o is supplying R_o.

Mode 1 [t_0~t_1] (Fig. 3(*a*)): At t_0, the auxiliary switch turns off and the auxiliary diode D_{a1} becomes ON, and due to the V_{Ca1} negative polarity, I_{La} starts decreasing according to (1). C_{S2} continues to be discharged. At t_1, the gate signal of S_1 is removed and due to its snubber capacitor C_{S1}, this switch turns off at ZVS. For this mode, the following equations can be written:

$$I_{L_a} = -\frac{V_{C_{a1}}}{L_a}(t - t_0) + I_{L_a}(t_0) \quad (1)$$

$$V_{L_1} = V_{in} + V_{C_{a1}}. \quad (2)$$

Mode 2 [t_1~t_2] (Fig. 3(*b*)): At the beginning of this mode, S_1 turns off and consequently, C_{S1} starts being charged by I_{L1} linearly according to (3) and thus, S_1 achieves ZVS at turn off. During this mode, C_{S2} is discharged completely and hence, S_2 antiparallel diode turns on. I_{La} continues reducing with the

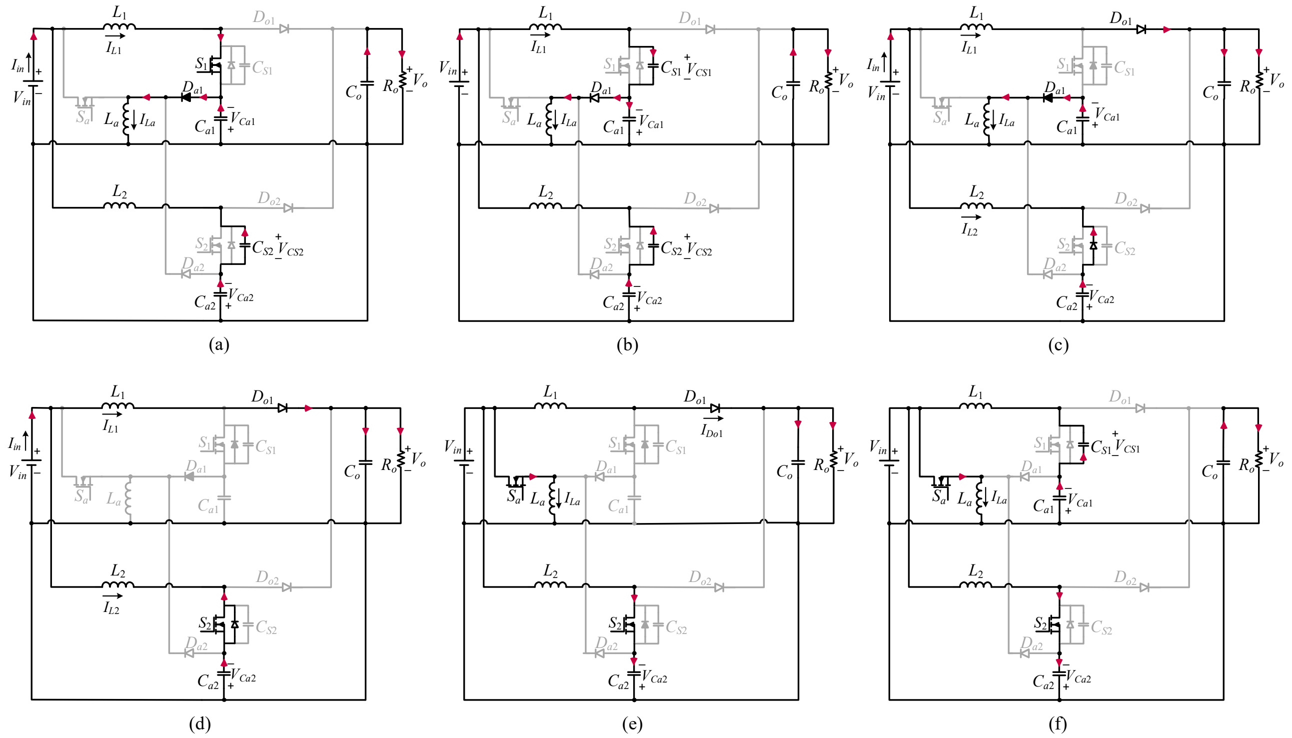

Fig. 3. Modes equivalent circuits. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

same slope as written in (1). At t_2, V_{CS1} increases to V_o+V_{Ca1}, and hence, D_{o1} turns on.

$$V_{C_{S1}} = \frac{I_{L_1}}{C_S}(t - t_1). \tag{3}$$

Mode 3 [t_2~t_3] (Fig. 3(*c*)): At t_2, D_{o1} turns on and begins to conduct I_{L1} to the load. During this mode, since S_2 antiparallel diode is on, S_2 gate signal is applied and it turns on at ZVS. In this interval, I_{La} keeps decreasing until it reaches zero and thus, D_{a1} turns off at ZCS at the end of this mode. For this mode, the below equation is valid:

$$V_{L_1} = V_{in} - V_o \tag{4}$$

Mode 4 [t_3~t_4] (Fig. 3(*d*)): At t_3, D_{a1} turns off. L_1 energy is being transferred to the load through D_{o1} and L_2 is being charged by V_{in}+V_{Ca2}. At t_4, S_a gate signal is applied.

Mode 5 [t_4~t_5] (Fig. 3(*e*)): At the start of this interval, S_a turns on at ZCS due to presence of L_a. I_{La} starts increasing linearly according to (5). According to (6), by increasing I_{La}, I_{Do1} decreases conversely until it becomes zero at t_5 and thus, D_{o1} turns off at ZCS.

$$I_{L_a} = \frac{V_{in}}{L_a}(t - t_4) \tag{5}$$

$$I_{D_{o1}} = I_{in} - I_{L_2} - I_{L_a}. \tag{6}$$

Mode 6 [t_4~t_5] (Fig. 3(*f*)): At the beginning of this mode, D_{o1} turns off. I_{La} continues increasing with the previous slope as indicated in (5), and it discharges C_{S1}. At t_6, S_a turns off again and the next half a switching cycle starts.

TABLE I
THE CONVERTER SPECIFICATIONS USED IN THE SIMULATIONS

Parameter	Symbol	Specification
Input voltage	V_{in}	48 V
Output voltage	V_o	400 V
Nominal output power	$P_{o(\text{nom})}$	400 W
Output capacitor	C_o	47 µF
Boost inductors	L_1, L_2	120 μH
Auxiliary inductor	L_a	10 µH
Series capacitors	C_{a1}, C_{a2}	6.8 µF
Snubber capacitors	C_{S1}, C_{S2}	3.9 nF

III. MATHEMATICAL ANALYSIS

A. Voltage Gain

By applying the volt-second balance to the inductor L_a during one switching cycle and omitting the short transition of mode 4, the voltage across the series capacitors is obtained as:

$$V_{C_{a1}} = V_{C_{a2}} = V_{C_a} = V_{in}\left(\frac{D'}{1 - D'}\right) \tag{7}$$

where D' is the auxiliary switch duty cycle.

If the volt-second balance is applied to L_1 and V_{Ca} is substituted from (7), the converter voltage gain is obtained as below:

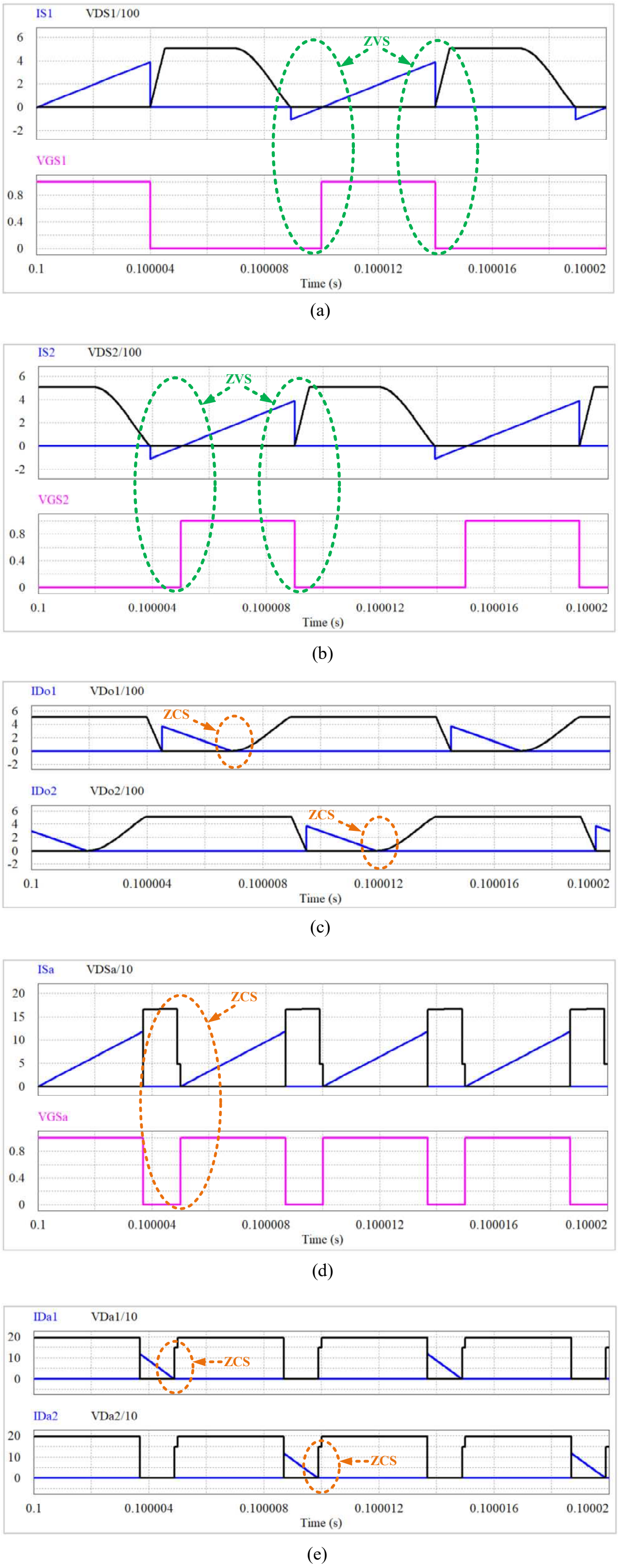

Fig. 4. Simulation current and voltage waveforms at full load.

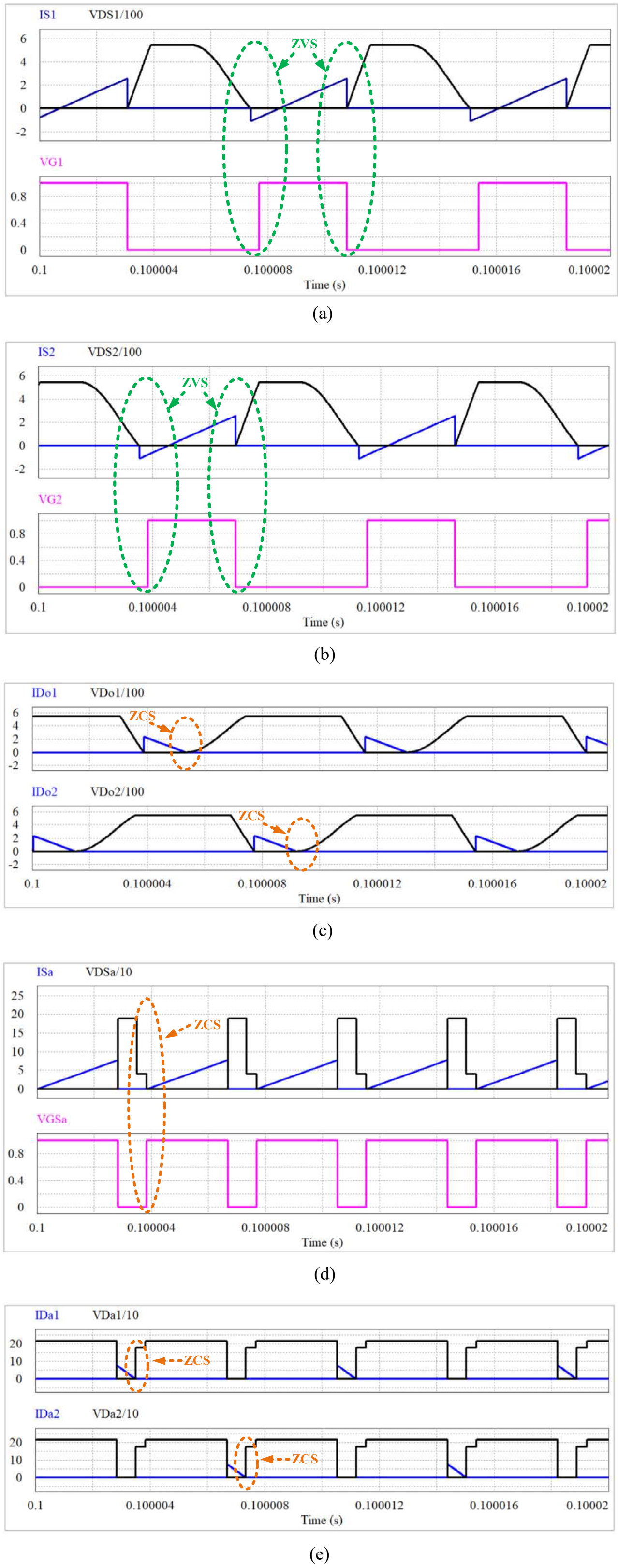

Fig. 5. Simulation current and voltage waveforms at light load.

$$M = \frac{V_o}{V_{in}} = \frac{1 + \sqrt{1 + \left[2\left(\frac{D}{1-D'}\right)^2 \frac{R_o}{L f_{sw}}\right]}}{2} \tag{8}$$

where D and f_{sw} are the main switches duty cycle and switching frequency, respectively. As (8) shows, in the proposed converter, in addition to D, there is another degree of freedom, i.e. D' for adjusting its high voltage gain.

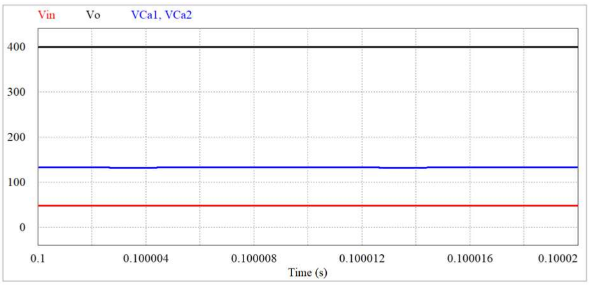

Fig. 6. Simulation voltage waveforms of V_{in}, V_o, V_{Ca1}, and V_{Ca2} at full load.

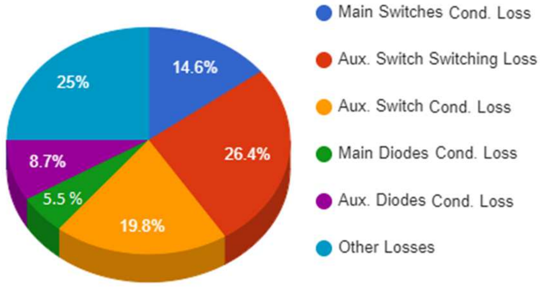

Fig. 7. Theoretical loss analysis of the proposed ZVT interleaved HSU converter.

TABLE II
CONVERTER PERFORMANCE COMPARISON

Feature		[7]	[8]	[11]	proposed converter
Number of elements	switches	4	4	3	3
	diodes	7	4	6	4
	magnetic cores	6	3	2	3
	windings	6	6	6	3
	capacitors	9	6	6	5
SS of main switches	turn-on	ZVS	ZVS	ZVS	ZVS
	turn-off	ZVS	HS*	ZVS	ZVS
Voltage gain (CCM)		$\frac{3}{D'+D}+\frac{2}{D'}$	$\frac{2+2nM}{1-D}$	$\frac{2(n+2)}{1-D}$	$\frac{1+\sqrt{1+\left[2\left(\frac{D}{1-D'}\right)^2\frac{R_o}{Lf_{sw}}\right]}}{2}$
Main switches voltage stress		$\frac{1}{4}V_o$	$\frac{1}{2+2nM}V_o$	$\frac{1}{2(n+2)}V_o$	$\left(1+\frac{D'}{M(1-D')}\right)V_o$
Main diodes voltage stress		$\frac{1}{4}V_o$	$\frac{4n}{2+2nM}V_o$	$\frac{n+1}{n+2}V_o$	$\left(1+\frac{D'}{M(1-D')}\right)V_o$
Common input-output grounding		No	No	No	Yes

*HS: hard switching

B. *Voltage Stress of the Semiconductors*

By applying KVL to the loop consisting of D_{o1}, V_{Ca1}, and C_o in Fig. 3(*c*), as well as the loop including C_{a2}, S_2, and C_o in Fig. 3(*d*), the voltage stresses of the main switches and diodes are obtained as:

$$V_{S_{1,2(max)}} = V_{D_{o1,2(max)}} = \left(1+\frac{D'}{M(1-D')}\right)V_o. \tag{9}$$

By writing KVL in the loop of V_{in}, S_a, and C_{a1} in Fig. 3(*a*), and the loop constituting S_a, V_{in}, and C_{a2} in Fig. 3(*e*), the auxiliary switch and diodes voltage stresses are calculated as:

$$V_{S_{a(max)}} = V_{D_{a1,2(max)}} = \left[1+\left(\frac{D'}{1-D'}\right)\right]\left(\frac{V_o}{M}\right). \tag{10}$$

IV. SIMULATION RESULTS

In order to confirm the theoretical analysis, and investigate the performance and usefulness of the proposed HSU converter, it is simulated by using PSIM software. The converter is designed to convert V_{in}=48 V to V_o=400 V at the nominal power of $P_{o(\text{nom})}$=400 W. The values of the converter elements which are used in the simulations are presented in Table I.

Fig. 4 shows the simulated waveforms of the converter switches and diodes at full load. As Figs. 4(*a*) and (*b*) clearly confirm, the main switches S_1 and S_2 achieves ZVS performance at both turn on and turn off transitions. According to these figures, V_{CS1} and V_{CS2} start increasing almost linearly when the related switches gate signals are removed which validates equation (3). These figures also show that as stated in the operation analysis, before applying the switches gate signals, V_{CS1} and V_{CS2} decrease to zero and thus, the main switches achieve ZVS at turn on transition. Figs. 4(*c*)-(*e*) confirm that the auxiliary switch as well as the main and auxiliary diodes operate at ZCS condition. The current waveforms in these figures fully confirm the equations of (5) and (6) as well as the explanations written in modes 3 and 5 of the theoretical analysis section. Due to this SS performance, the converter switching and reverse recovery losses are decreased, and its efficiency increases considerably. In Fig. 5, the waveforms of semiconductor elements at about

30 % of the nominal load are shown which confirms that the proposed HSU converter is capable of operating at SS performance at a wide range of load variations. Also, as this figure shows, by decreasing the load, the switching frequency is increased to tune the voltage gain which was previously predicted by (8). As observed from Figs. 4 and 5, the voltage stresses across the semiconductors are almost equal to their theoretical values obtained by (9) and (10).

Fig. 6 exhibits the simulated waveforms of V_{in}, V_o, and the series capacitors voltages V_{Ca1} and V_{Ca2}. As can be seen, the proposed HSU converter features a high voltage gain and the voltage across two series capacitors in each phase are constant and identical. The value of the voltage gain and the series capacitors voltages which are presented in this figure are in close agreement with (7) and (8). This validates the high precision of the converter mathematical analysis. Fig. 7 illustrates the theoretical loss analysis of the proposed ZVT interleaved HSU converter at full load. For calculating the losses, based on the semiconductors ratings defined by (9) and (10), TK20A60W, IRF200B211, and MUR460, are considered as the main switches, auxiliary switch, and all the diodes, respectively, and their characteristics are extracted from their datasheet. Due to the SS operation, the switching and capacitive turn-on losses of the main switches are almost zero. The losses associated with cores, windings, and gate drivers are included in the section of other losses in Fig. 7. For the proposed converter, the full load efficiency is obtained as 96.2%.

V. Performance Comparison

A comparison between the proposed converter and the most recent and prevailing SS interleaved HSU converters is shown in Table II. As this comparison confirms, the proposed converter uses the least number of elements while features high voltage gain and full SS performance. Besides, in contrast to the converters introduced in [7], [8], and [11], the proposed converter features common input-output grounding.

VI. Conclusion

This paper proposes a novel ZVT interleaved HSU converter. In this converter, high voltage gain and SS performance for all the semiconductor elements are achieved by using low elements count. The mathematical analysis of the converter is presented. The comparison between the proposed converter and most recent counterparts are presented to show the features of the proposed converter in terms of high voltage gain, low component count, and full SS performance. The simulation results of the proposed converter confirm SS performance of all the semiconductors over a wide range of load changes.

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