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A 9.1 mW Inductive Displacement-to-Digital Converter with 1.85 nm Resolution

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Abstract

A displacement-to-digital converter (DDC) based on inductive (eddy-current) sensor is presented. The sensor is embedded in a self-oscillating front-end, whose 145MHz output is then digitized by a ratiometric ΔΣ ADC. Over a 10μm range, the DDC achieves 1.85nm resolution (1.02 pH), in a 2kHz bandwidth. It draws 9.1mW from a 1.8V supply making it the most energy-efficient ECS interface ever reported.

Keywords: eddy-current, inductance, displacement, sensor, precision, chopping, delta, sigma, ADC, oscillator.

Introduction

Nanometer displacement sensors are a critical part of high-tech equipment, e.g. wafer scanners. Capacitive and eddy-current sensors (ECS) are attractive due to their compactness. ECSs have the added advantage of their robustness to environment (e.g. humidity) and contactless operation. ECS performance can be improved by locating them close to their interface circuitry [1-3]. However, the power dissipation of this circuitry must then be minimized to avoid self-heating issues, especially in vacuum environments [4,5].

A self-oscillating front-end is an efficient manner of driving the coils of an ECS [1-3]. Its displacement-dependent output signals can then be ratiometrically digitized by a continuous-time (CT) ΔΣ ADC [6]. The ADC must be able to cope with a wide range of excitation frequency f_{exc} because sampling frequency F_s is derived from f_{exc} ($F_s = f_{exc}/2^N$). But f_{exc} depends on the inductance of the sensor which is not well defined. Furthermore due to small standoff (X_{so}), such coils have a low Q, and so the ADC must be robust to jitter in f_{exc}.

Architecture and Implementation

A simplified block diagram of a DDC is shown in Fig. 1. Off-chip sensor (L_{sen}) and reference (L_{ref}) coils form part of an LC oscillator. The amplitude of oscillator outputs V_{sen} and V_{ref} is proportional to L_{sen} and L_{ref} respectively. In [1,2], the amplitudes of V_{sen} and V_{ref} are first demodulated and then digitized by an external ADC. Their ratio is a measure of displacement which, advantageously, is insensitive to the drift and noise of the excitation oscillator [2,3]. In this work, all these functions (demodulation, digitization and ratiometric readout) are achieved by an on-chip ratiometric ΔΣ ADC.

Fig. 2(a) shows the self-oscillating front-end which generates f_{exc} using L_{sen}, L_{ref} and an 8pF on-chip capacitor. As shown in Fig. 2(c-d), V_{sen} and V_{ref} are first converted into currents via capacitors C_{in} = 0.5 pF and C_{ref} =500 fF. These are then down-converted by a passive mixer and used as the input and reference of the charge balancing ADC. To relax the ADC's dynamic range, sensor's offset ($\propto X_{so}$) is compensated by the current I_{soc} ($\propto V_{ref}$). The maximum displacement (X_{max}) is defined by the ratio $\beta = C_{ref}/C_{in} = X_{max}/X_{so}$) [1]. A high-speed comparator generates the mixer clock f_{mix} (= f_{exc}) and a synchronous sampling clock F_s (= $f_{mix}/2^N$).

The 1st OTA G_{m1} is the most critical block, since it must provide a low input impedance at 145 MHz to assist capacitors for voltage-to-current conversion. The OTA consists of a gain-boosted telescopic amplifier, with >90dB DC gain and > 1GHz unity-gain frequency, which employs 2-stage Miller-compensated gain-boosting amplifiers (Fig. 2(b)). Both amplifiers are chopped, at F_s to reduce their offset and 1/f noise [7]. As shown in Fig. 2(d), the inputs of the 1st integrator are rectified sinusoids, whose limited slew-rate mitigates the effect of clock jitter in f_{mix}. The gain of the 1st integrator of the $\Delta\sum$ ADC (Fig. 3) can be expressed as $\omega_{u1} = (4.C_{in}.f_{exc})/C_1$. Thus setting $F_s = f_{exc}/2^N$ ensures that the modulator's noise-shaping tracks f_{exc} over a wide range.

Measurement Results

The prototype ECS interface occupies 0.264 mm2 in a 0.18μm CMOS process and is characterized by a PCB-based ECS (Fig. 4). L_{ref} is positioned 55 μm from a Copper target, using stainless steel spacers. The target on the sensor side is moved at 1 μm step , around X_{so} = 55 μm, using a linear precision stage. The effective inductance of coils is ≈ 75 nH, which includes 20 nH parasitic inductance (L_{par} in Fig. 2(a)) due to coil-to-chip trace.

Fig. 5 shows the measured transfer characteristics of the interface around X_{so} = 55 μm, at different oscillator bias currents ($I_{ss,osc}$) and F_s. The interface's ratiometric property in suppressing $I_{ss,osc}$ and the wide F_s operation of CTΔΣADC can be noticed. The small offset between various curves is attributed to the initial target alignment mismatch (≤ 1 μm) between different experiments.

Fig. 6 depicts the output spectrum the DDC output. The interface achieves a peak SNR of 76.4 dB (ENOB = 12.4 bits). This evaluates to a displacement resolution of 1.85 nm, in 10 μm range. The oscillator amplitude noise ($i_{n,osc}$) is not completely suppressed by ratiometric measurement due to the finite input impedance of ADC and clock comparator. Fig. 7 shows the output spectrum of the interface at various $I_{ss,osc}$ and F_s. The dominant $i_{n,osc}$ and its reduction at higher $I_{ss,osc}$ can be noticed. The ADC's noise-shaping is preserved up to F_s = 9 MHz and only starts to deviate around Fs = 18 MHz.

Fig. 8 summarizes the performance and compares this interface against state-of-the-art. This interface achieves 1.85 nm displacement resolution in a 2 kHz bandwidth, after consuming only 9.1 mW power. This corresponds to an inductance resolution of 1.02 pH. Moreover, more resolution can be achieved by reducing L_{par}, whose presence desensitizes the ECS. With L_{par} = 0, the estimated resolution is about 1 nm (=$\beta * X_{so}/2^{ENOB}$). The proposed DDC integrates all important ECS functionalities on-chip, and reduces the required chip area and power consumption by more than half when compared to [1,2]. It is also able to operate over a wide range of excitation frequency f_{exc}, allowing it to be flexibly used with different ECS coil designs.

References

[1] V. Chaturvedi, *et al*., *ISSCC*, Feb 2017 (to appear).
[2] M. R. Nabavi, *et al., JSSC,* vol. 48, no. 11, Nov., 2013.
[3] A. Fekri, et al., ESSCIRC, Sept, 2014.
[4] Baumer IPRM, available: www.baumer.com
[5] M. Oberle, et al., *JSSC*, vol. 37, pp. 916–925, Jul 2002.
[6] M. Pertijs, et al., JSSC, vol. 40, no. 12, Dec 2005
[7] S. Billa, et al., ISSCC, Feb 2016.

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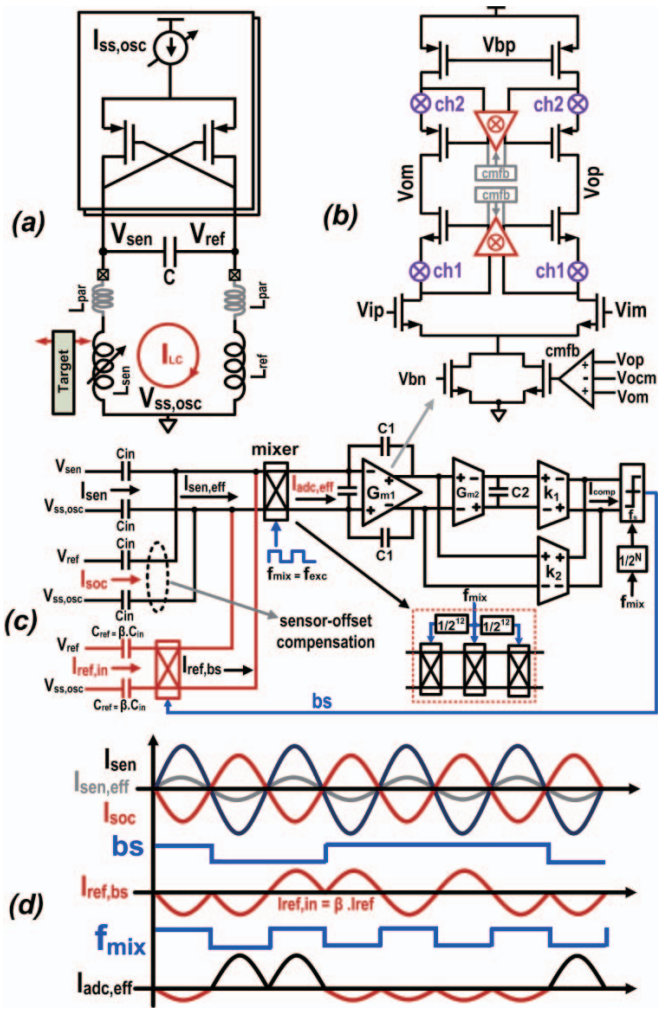

Fig. 2 Architecture and working principle of the DDC interface.

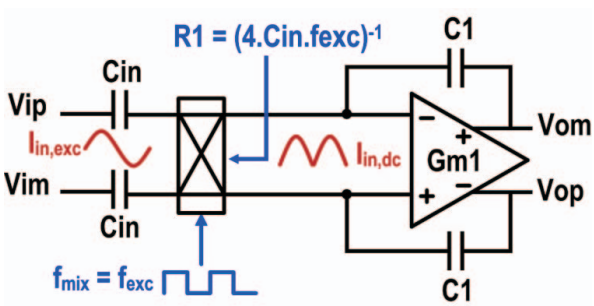

Fig. 3 First integrator of the ∆∑ ADC tracks excitation frequency.

	This work	[1]	[2]	[3]	[4]	[5]
Stand-off Distance	**55 µm**	105 µm	3 mm	3 mm	1 mm	3 mm
Power consumption excluding ADC (mW)	**9.1#**	19.8	18	18#	750	7.3
Sensor Excitation Frequency (Hz)	**145M**	126M	20M	15M	-	312.5k
Displacement resolution (nm) (Inductance resolution (pH))	**1.85 (1.02)**	0.6 (0.58)	65 (1.5)	135 (3.8)	60 (-)	2930(-)
Bandwidth (Hz)	**2k**	2k	1k	1k	500	10k
Resolution (bit)	**12.4 (ENOB)***	14.1 (ENOB)*	15.5 (ENOB)	15	-	10
Technology	**0.18 µm CMOS**	0.18 µm CMOS	0.35 µm BICMOS	0.35 µm BICMOS	-	0.6 µm CMOS

ADC and ratiometric readout integrated in the interface
* Calculated in useful displacement range

Fig. 8 Performance Summary and Comparison table.

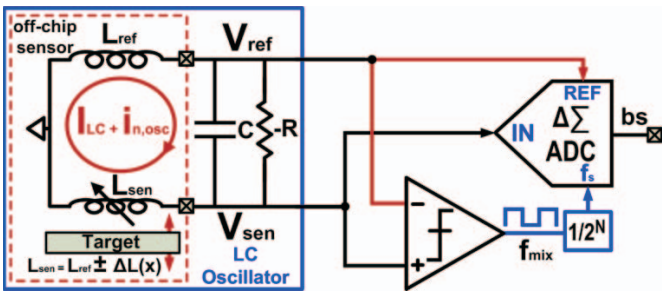

Fig. 1 Displacement-to-Digital converter with ratiometric output.

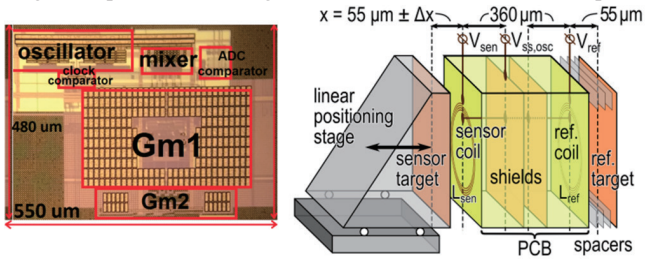

Fig. 4 Chip microphotograph and PCB based eddy-current sensor.

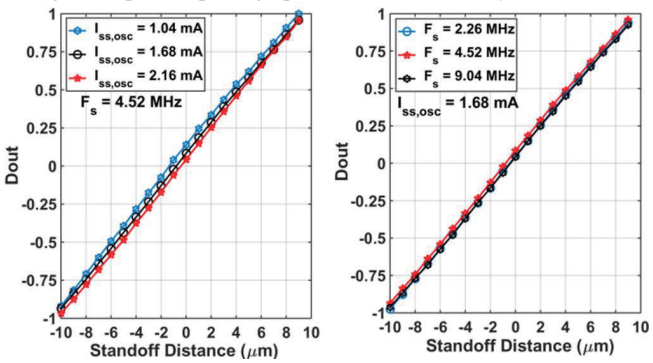

Fig. 5 Transfer characteristics of the interface, around X_{so} = 55 um.

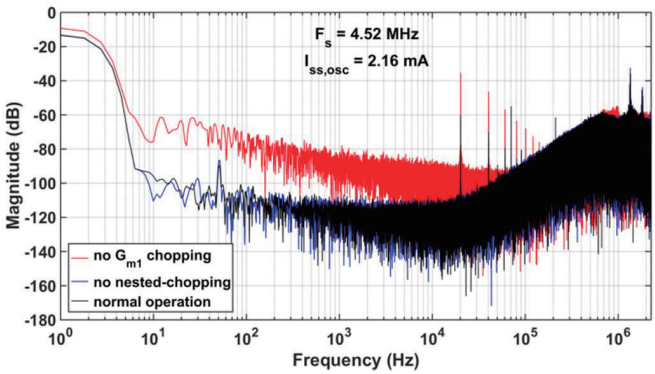

Fig. 6 Output spectrum of the DDC interface.

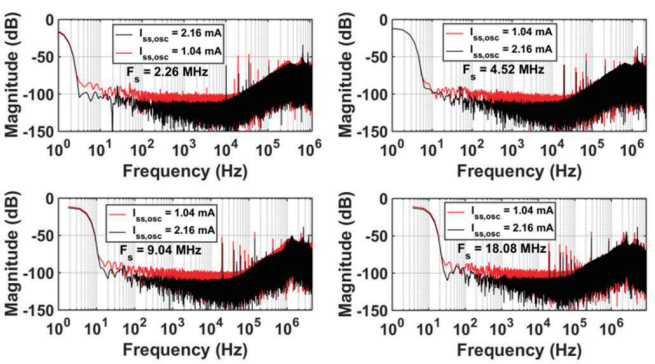

Fig. 7 Output spectrum at different sampling frequencies showing the dominant oscillator amplitude noise.

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