High-Precision Fabrication of Single-Crystal Silicon Nanopores with Extremely Small Feature Sizes

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DOI
10.4233/uuid:9077903c-8212-4c19-8b21-97c1669e8dad

Publication date
2025

Document Version
Final published version

Citation (APA)
Hong, H. (in press). *High-Precision Fabrication of Single-Crystal Silicon Nanopores with Extremely Small Feature Sizes.* [Dissertation (TU Delft), Delft University of Technology].
https://doi.org/10.4233/uuid:9077903c-8212-4c19-8b21-97c1669e8dad

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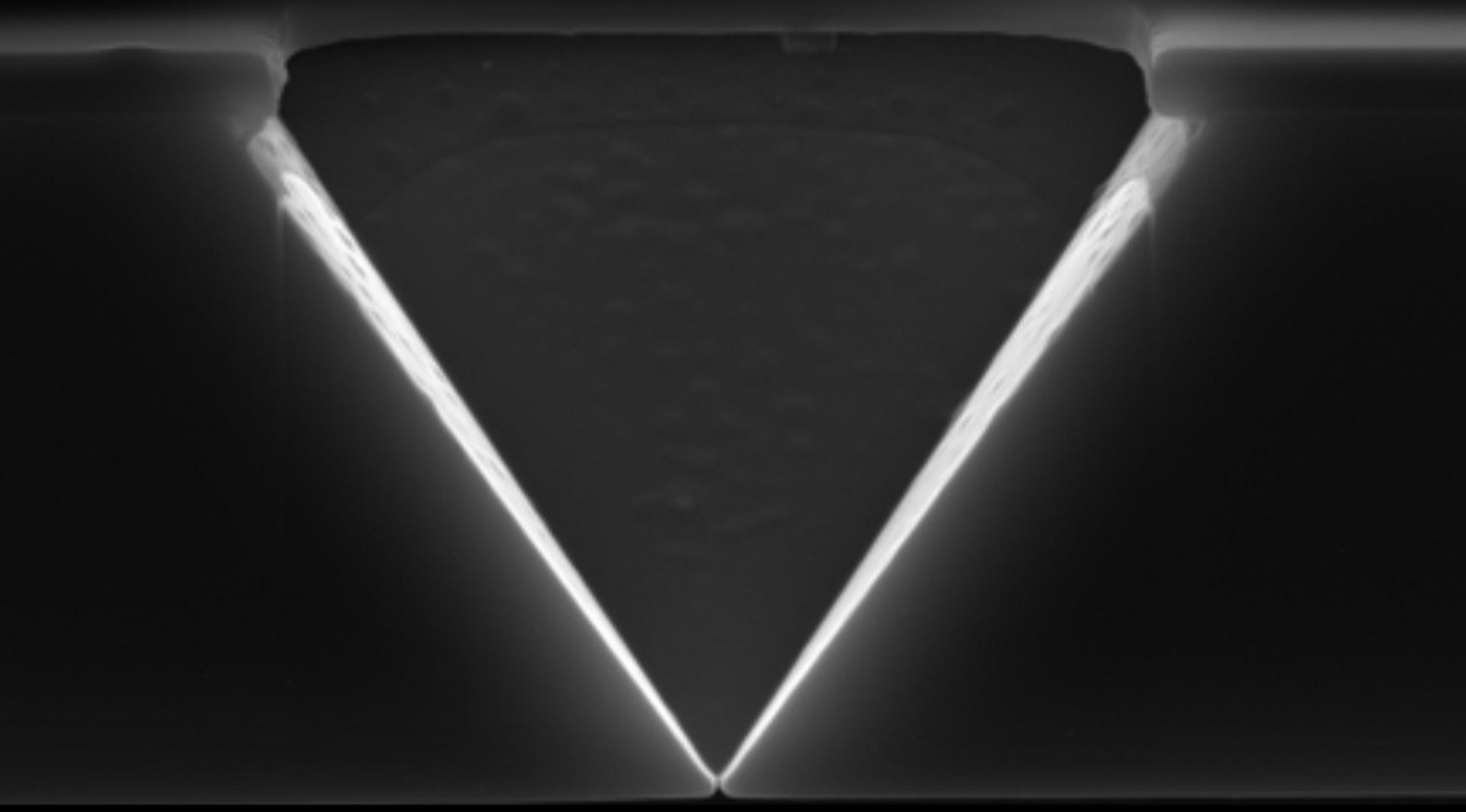

High-Precision Fabrication of Single-Crystal Silicon Nanopores with Extremely Small Feature Sizes

Dissertation

For the purpose of obtaining the degree of doctor at Delft University of Technology
by the authority of the Rector Magnificus prof.dr.ir. T.H.J.J. van der Hagen
chair of the Borad for Doctorates
to be defended publicly on
Friday 6 June 2025 at 15:00 o'clock

by

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Keywords: Silicon nanopore, TSWE, Etch-stop, Ionic current, Heavy doping, Electrochemical passivation

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Printed by: Gildeprint
Front & Back: Cover artwork by Hao Hong

To all those who have helped me.
Hao Hong

CONTENTS

SUMMARY

Silicon nanopores have emerged as the cornerstone of ionic and nanofluidic channels, enabling diverse applications such as biosensing, DNA-based information storage, and nanopore batteries. Their mechanical robustness, surface functionalization versatility, and seamless integration with nanofluidic devices make them highly adaptable to advanced technologies. The three-step wet etching (TSWE) method has shown great promise in fabricating silicon nanopores. However, precise control of silicon etching and achieving reliable etch-stop remain significant challenges. This thesis investigates the controllable fabrication of single-crystal solid-state silicon nanopores with extremely small dimensions using the TSWE method. Novel methodologies are introduced to address these challenges, exploring their applications in nano-mask lithography, biosensing, and ionic field-effect transistors (FETs). By analyzing nanopore formation principle at the atomic scale, the study establishes a quantitative relationship between nanopore size and the related ionic current, enabling the fabrication of nanoslits as small as 3 nm. The research integrates heavy boron doping and electrochemical passivation to regulate etching rates and achieve precise etch-stop, significantly enhancing fabrication controllability and scalability, with potential for large-scale production. The fabricated nanopores were further utilized in ionic FETs, demonstrating three-dimensional gating to modulate surface charge density. This enabled transitions between ohmic and diode-like regimes and enhanced ionic current rectification, as validated by COMSOL simulations. Additionally, the nanopores were successfully applied in biosensing, achieving high-sensitivity detection of biomolecular translocation events. Nano-mask lithography was also demonstrated, utilizing the nanopores as hard masks for focused ion beam (FIB) lithography to achieve precise and reproducible pattern transfer. These findings underscore the potential of single-crystal silicon nanopores for advanced applications in nanofabrication, biosensing, and ionic circuit development. This work establishes a foundation for future exploration in ion transport, nanofluidics, and scalable device manufacturing.

SAMENVATTING

Silicium nanoporiën hebben zich ontwikkeld tot de hoeksteen van ionische en nanofluïdische kanalen, waardoor diverse toepassingen mogelijk zijn, zoals biosensing, op DNA gebaseerde informatieopslag en nanopore batterijen. Hun mechanische robuustheid, veelzijdigheid in oppervlaktefunctionalisatie en naadloze integratie met nanofluïdische apparaten maken ze zeer geschikt voor geavanceerde technologieën. De driestaps nat etsen (TSWE) methode is veelbelovend gebleken voor het maken van silicium nanoporiën. Echter, nauwkeurige controle van het etsen van silicium en het bereiken van betrouwbare etch-stop blijven belangrijke uitdagingen. Dit proefschrift onderzoekt de controleerbare fabricage van enkel-kristallijne vaste silicium nanoporiën met extreem kleine afmetingen met behulp van de TSWE methode. Nieuwe methodologieën worden geïntroduceerd om deze uitdagingen aan te pakken, waarbij hun toepassingen in nano-masker lithografie, biosensing en ionische field-effect transistors (FET's) worden onderzocht. Door het principe van de vorming van nanoporiën op atomaire schaal te analyseren, legt het onderzoek een kwantitatief verband tussen de grootte van nanoporiën en de bijbehorende ionenstroom, waardoor de fabricage van nanoslits zo klein als 3 nm mogelijk wordt. Het onderzoek integreert zware boordoping en elektrochemische passivering om etssnelheden te reguleren en een precieze ets-stop te bereiken, waardoor de beheersbaarheid en schaalbaarheid van de fabricage aanzienlijk worden verbeterd, met mogelijkheden voor productie op grote schaal. De gefabriceerde nanoporiën werden verder gebruikt in ionische FET's, waarbij driedimensionale gating werd gedemonstreerd om de oppervlakteladingsdichtheid te moduleren. Dit maakte overgangen mogelijk tussen ohmse en diode-achtige regimes en verbeterde ionische stroomgelijkrichting, zoals gevalideerd door COMSOL-simulaties. Daarnaast werden de nanoporiën met succes toegepast in biosensing, waarbij met hoge gevoeligheid biomoleculaire translocatiegebeurtenissen werden gedetecteerd. Nano-masker lithografie werd ook gedemonstreerd, waarbij de nanoporiën werden gebruikt als harde maskers voor gefocusseerde ionenbundel (FIB) lithografie om nauwkeurige en reproduceerbare patroonoverdracht te bereiken. Deze bevindingen onderstrepen het potentieel van silicium nanoporiën met één kristal voor geavanceerde toepassingen in nanofabricage, biosensing en de ontwikkeling van ionische circuits. Dit werk legt de basis voor toekomstig onderzoek naar ionentransport, nanofluïdica en schaalbare productie van apparaten.

1

Introduction

1.1. BACKGROUND

1

Nanopores are nanochannels embedded in biological membranes and structures, or through-holes in specific solid materials such as silicon and silicon nitride. The concept of nanopores was first proposed in 1989, with the initial report of a biological nanopore used for nucleic acid sensing announced in 1996 [1]. This approach, which employs nanopores as platforms for biological molecular detection, has garnered significant attention from researchers worldwide [2-4].

As one of the most fundamental applications of nanopores, biomolecule detection like DNA sequencing offers advantages such as amplification-free processing, no labeling requirements, ultra-long read lengths, and low cost, making it one of the most promising methods for single-point biomolecular detection [5]. Figure 1.1 shows an illustration of nanopore-based biomolecular detection using the ionic current trace method. Nano-sized openings in membranes separate two chambers containing an electrolyte solution, commonly referred to as the cis and trans sides. One of the chambers includes biomolecules to be detected. When an electric field is applied across the membrane via a pair of nonpolarizable electrodes (Ag/AgCl electrodes) placed on each side, the nanopore serves as the sole channel for mobile ions and biomolecules to traverse from one chamber to the other. Before the analyte enters the nanopore, a steady ionic current, known as the open-pore current, is recorded through the nanopore. The translocation of biomolecules through the nanopore is detected as a transient change in conductivity, resulting from the partial blockage of the nanopore by the analyte. Biomolecule detection using nanopores can be achieved via optical or electrical detection, with the latter being more convenient as it does not require expensive optical instrumentation. Electrical detection methods including the ionic current trace can be further categorized based on the detection principle: current blocking, tunneling current, and capacitance change [6]. Among these, the current blocking method stands out as the simplest and most cost-effective strategy for sequencing. This method leverages the principle that biomolecules, being charged, are driven through the nanopore under an external bias voltage, causing a detectable blockage in the ionic current. The blocking current and dwell time induced by biomolecules serve as key metrics for molecular identification. Importantly, even slight differences in the shape, size, and charge of biomolecules can cause significant variations in the blocking current and dwell time, thereby enabling efficient and precise biomolecule detection [7-9].

Biological nanopores demonstrate excellent compatibility with biomolecules, making them ideal for DNA detection applications. However, due to their mechanical robustness, ability to functionalize surfaces with organic or inorganic treatments, and seamless integration with nanofluidic devices [10], solid-state nanopores have emerged as pivotal tools for biosensing. These tools have been widely applied in the detection of biomolecules, proteins, and DNA [11–13]. Traditional detection mechanisms often rely on electrokinetic forces to drive molecule translocation through the nanopore, producing a blockade current. Despite their utility, these methods frequently suffer from

low temporal resolution and inconsistent blockade signals. One critical challenge in advancing nanopore sensing lies in slowing the translocation speed and improving the signal-to-noise ratio. Various strategies have been developed to address these limitations, including the use of protein motors [14], ionic liquids [15], and sequential DNA unzipping techniques [16]. Additionally, purely electrical molecule sensing enhanced by opto-electrical approaches has become a powerful complement to traditional detection methods [17].

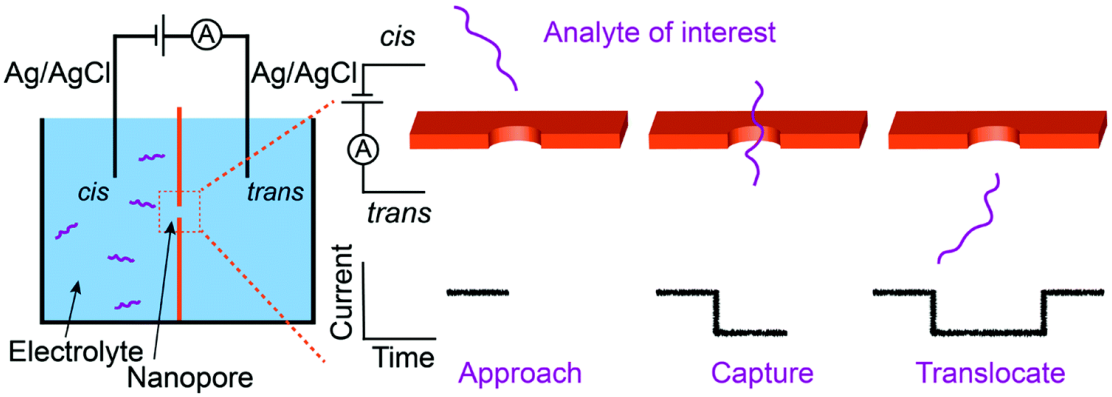

Figure 1.1 Illustration of nanopore-based biomolecule detection using ionic current trace method

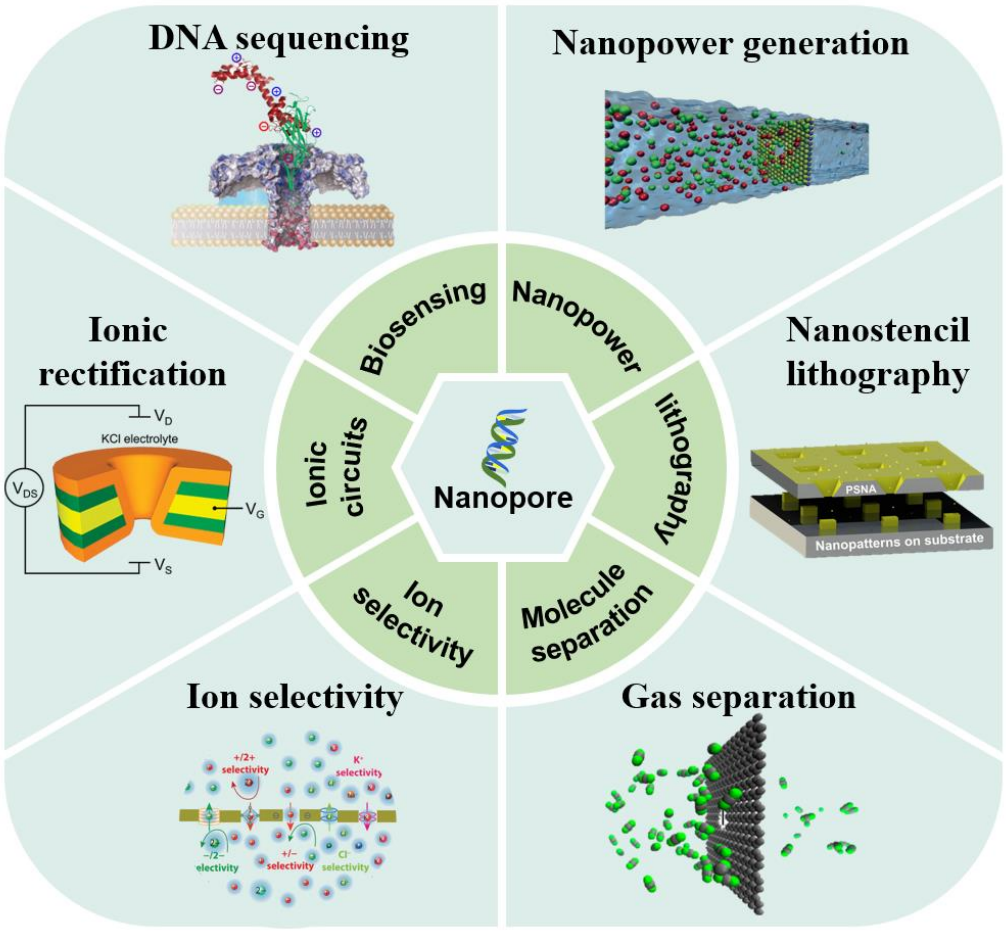

Figure 1.2 Various applications of solid-state nanopores

1

Beyond molecular detection, solid-state nanopores have demonstrated versatility in diverse applications, as shown in Fig. 1.2, including DNA-based information storage [18], nanopore batteries [19], nanopower generators [20,21], ionic rectification [22,23], and nanostencil lithography [24]. Despite their versatility, different applications often demand specific materials, fabrication methods, and analytical techniques. Following the discovery of two-dimensional materials, the range of materials used for solid-state nanopores has expanded beyond traditional choices such as silicon [25,26], oxides [27,28], and nitrides [29–31], to include like graphene [32,33], MoS_2 [34,35], and carbon nanotubes [36,37]. Consequently, several fabrication methods tailored to specific materials have been proposed to advance the performance and applicability of solid-state nanopores.

1.2. FABRICATION METHOD OF SOLID-STATE NANOPORE

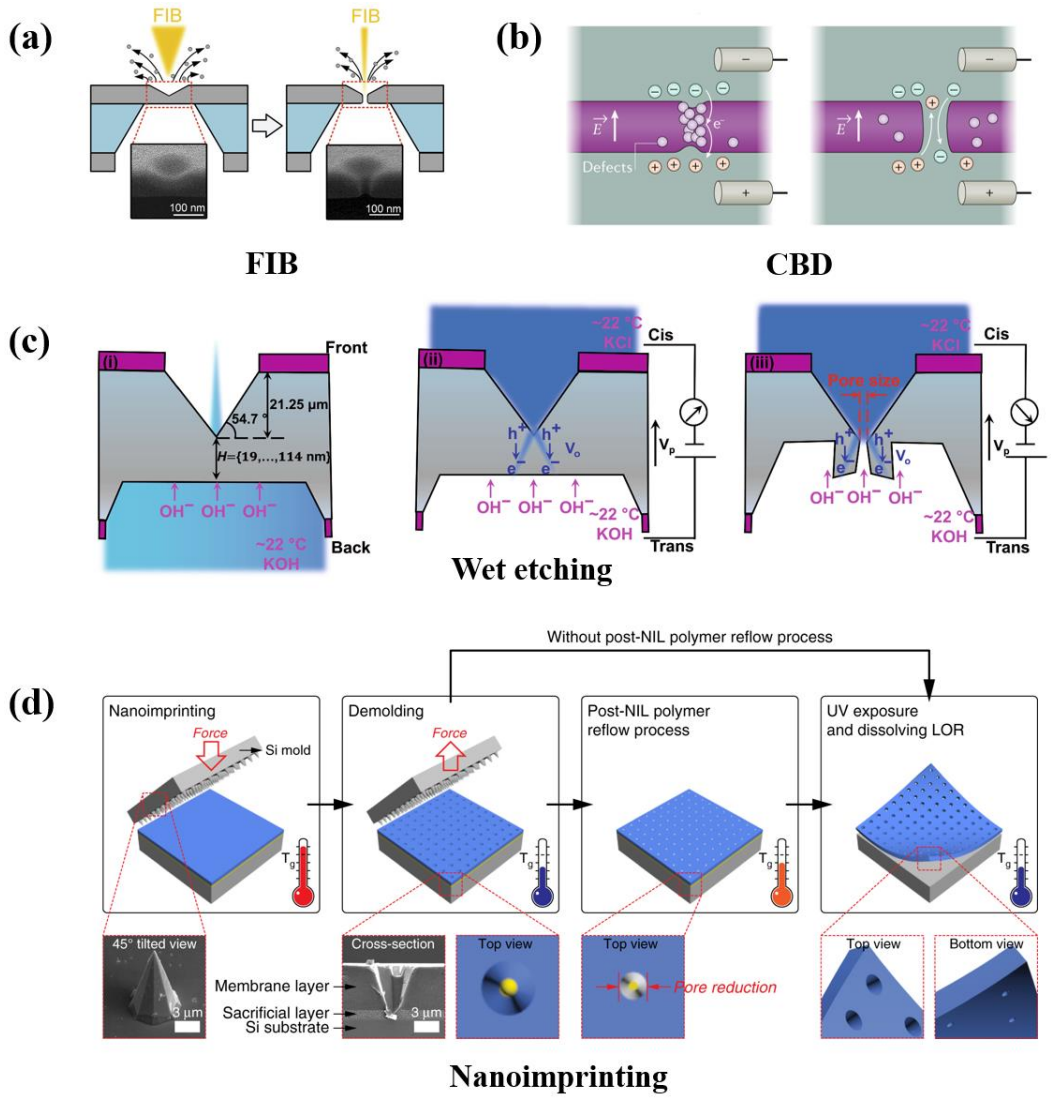

Figure 1.3 Different fabrication methods of solid-state nanopores. a) focused ion beam b) controlled dielectric breakdown c) wet etching d) nanoimprinting

Different fabrication methods have been proposed for various substrate materials, tailored to their unique properties and requirements. In addition to variations in materials, the structures of nanopores fabricated by different methods also vary significantly. Currently, the predominant fabrication techniques include focused ion beam/transmission electron microscope (TEM), controlled dielectric breakdown (CBD), nanoimprinting, and wet etching with different feedback controls. These methods enable the precise fabrication of nanopores with distinct geometries, sizes, and properties, catering to a wide range of applications. The corresponding fabrication illustrations are shown in Fig. 1.3. Furthermore, Table 1 provides a detailed comparison of the reported solid-state nanopore fabrication methods, highlighting their advantages, limitations, and suitability for specific applications. This comparison serves as a guide for selecting appropriate fabrication techniques based on experimental requirements and target nanopore characteristics.

1.2.1. FIB/TEM

Using focused ion beam (FIB) or transmission electron microscopy (TEM) to directly drill nanopores in suspended films is currently the most commonly employed method for fabricating single solid-state nanopores. Nanopores based on different materials, such as silicon nitride, MoS_2, and graphene, have been successfully fabricated using these techniques [38–43].

In 2001, Li et al. utilized an Ar+ beam from a high-energy ion gun to fabricate the first solid-state nanopore on a silicon nitride film. The fabrication process involved the following steps: first, the bulk silicon was etched from the backside to expose the thin film, suspending the film in a specific area. Then, FIB was employed to directly drill the nanopore. This method has since enabled researchers to fabricate nanopores of various sizes in thin films of different materials [44 – 47]. Gierak et al. improved the Ga+ direct-writing system of FIB and successfully fabricated a nanopore with a 2.5 nm diameter on a 20 nm thick SiC film [48]. However, due to the large FIB beam spot, most nanopores fabricated using FIB by other teams are larger than 10 nm in diameter. In 2016, helium ion microscopy (HIM) emerged as a nanopore fabrication technology. Its smaller beam spot and more precise sample scanning capabilities enabled the effective fabrication of sub-10 nm nanopores. This advancement marked a significant improvement in the resolution and scalability of nanopore fabrication using ion beams. Compared with FIB, TEM offers a smaller beam spot and higher resolution, allowing for simultaneous drilling and imaging during the fabrication process. This feature enables visual control of nanopore preparation in real time. Using the TEM method, Michiel et al. demonstrated precise control over the shape of small nanopores (~5 nm diameter) in 20 nm Si_3N_4 membranes by employing TEM at varying resolutions [49]. Kim et al. developed and optimized a procedure for the rapid fabrication of single nanopores and nanopore arrays in thin Si4N3 membranes using TEM. This TEM-based

procedure achieved highly tunable and reproducible nanopores ranging from 2 to 20 nm in diameter [50].

1

Although FIB and TEM enable fast and controllable fabrication of nanopores with extremely small sizes, these methods still face limitations. These challenges include manual alignment, low throughput, the need for highly trained operators, and reliance on expensive equipment. As a result, these drawbacks present significant barriers to the cost-effective and large-scale fabrication of nanopores, which are critical for expanding their practical applications.

1.2.2. CDB

Controlled dielectric breakdown is an in situ nanopore fabrication method that uses only a voltage-current reading apparatus, which opens up the possibility of fabricating nanopores integrated with complex, potentially nonplanar, geometries [51–54]. The mechanism of this method is that, under the action of the breakdown voltage, the defects or holes in the dielectric film are continuously generated and accumulated over time until a path is formed in the membrane. Thus, the fabrication of nanopores is completed. In 2014, Kwok et al. introduced a fast and straightforward approach for fabricating single nanopores as small as 2 nm in diameter with sub-nm precision, directly in solution, by controlling dielectric breakdown at the nanoscale. Despite its potential, CBD presents several challenges in the fabrication of solid-state nanopores. One significant issue is the formation of multiple nanopores [55,56]. This problem becomes particularly pronounced when fabricating large-sized nanopores because the membrane is exposed to high electric fields for prolonged periods during the pore expansion phase, increasing the likelihood of additional breakdown events. However, it was recently shown that increasing the conductivity of the solution during the pore expansion phase decreased the probability of forming multiple pores. This is because nanopore expansion is driven by electrochemical reactions arising from significant ionic current flow through the pore. As such, increasing the conductivity of the solution allows higher current at lower potentials, thus enabling nanopore expansion with a decreased risk of new breakdown events occurring. This adjustment not only improves the reliability of the process but also enhances the scalability of CBD for practical applications.

Another challenge associated with CBD is the random positioning of fabricated nanopores. To address this issue, researchers have proposed several methods for achieving controllable nanopore fabrication. For example, localized laser irradiation and heating of specific regions of the dielectric film can concentrate defects and holes in the irradiated areas, ensuring that nanopores predominantly form in the targeted locations [57]. This method enhances spatial control and reduces fabrication variability, making it suitable for applications requiring precise pore positioning. Additionally, Wang et al. utilized silicon oxide films with pyramid structures to achieve self-aligned nanopore fabrication. The self-enhanced electric field at the vertex of the pyramidal membrane, combined with the optimized thickness distribution resulting from the thermal oxidation process (where the vertex region is the thinnest), ensures that

nanopores preferentially form at these vertices, thereby mitigating the issue of random positioning.

1.2.3. WET ETCHING WITH DIFFERENT FEEDBACK CONTROL

In 2013, the research group led by Zewen Liu at Tsinghua University pioneered the development of a three-step anisotropic wet etching method for the fabrication and study of single-crystal silicon solid-state nanopores. By analyzing the formation principles of nanopores from atomic-layer and macroscopic perspectives, and leveraging the characteristics of anisotropic wet etching, the group successfully established a systematic approach for the controllable fabrication of sub-10 nm nanopores. This was achieved by integrating techniques such as the color-feedback method, ionic current-monitored method, dielectric breakdown method, and electrochemical passivation method with the TSWE process.

Their outstanding work also included the first report of the world's smallest feature size (3 nm) nanoslits, marking a significant milestone in nanopore/slit fabrication. Furthermore, the group explored various applications of the fabricated nanopores and nanoslits, including biosensing, ionic rectification, and nano-mask lithography, demonstrating the versatility and potential of these structures. The research achievements of this group have significantly advanced the field of silicon nanopores, providing foundational knowledge and practical methodologies that have greatly contributed to their controllable fabrication and application.

The fabrication method based on anisotropic chemical wet etching is considered one of the most promising techniques for silicon nanopore fabrication due to its compatibility with semiconductor processes and MEMS technologies, enabling cost-effective production. Additionally, the inherent semiconductor properties of silicon facilitate straightforward surface modifications and the integration of gates, allowing for the physical and electrical characteristics of nanopores to be tailored for a wide range of applications [58,59].

However, over-etching remains a significant challenge for the controllability of the wet etching method. The primary causes of over-etching are the inability to detect the pore-opening event in real-time and the failure to achieve a rapid etch-stop after the formation of nanopores with the desired size. To address these issues, significant efforts have been devoted to monitoring pore-opening events and mitigating over-etching. Park et al. introduced a current-monitored method that accurately measures the current across silicon chips to detect pore-opening events [60]. Furthermore, Hong et al. established a quantitative relationship between the ionic current and nanopore size, enabling the prediction of nanopore dimensions during the etching process [61]. Deng and Chen et al. developed a color-feedback mechanism where the etchant changes color to indicate pore-opening events and a diffusion model was proposed to analyze the influence of this feedback mechanism on nanopore size [62,63]. Additionally, some researchers have implemented rapid etch-stop methods, such as introducing a stopping medium to halt the etching reaction after the pore-opening event [64]. Yang et al.

designed a spectral detection system to precisely measure the remaining silicon thickness and combined this with photoinhibition-assisted KOH etching to reduce the etching rate, achieving controllable fabrication of silicon nanopores [65]. These strategies have significantly improved the ability to monitor and control the etching process, providing insights into overcoming the challenges associated with over-etching.

Despite these advances, accessible methods that are fully compatible with semiconductor fabrication processes for precisely controlling the silicon etching process remain lacking. The ultimate goal of eliminating the over-etching effect and achieving fully controllable fabrication of silicon nanopores has yet to be realized.

1.2.4. NANOIMPRINTING

Unlike the previously described methods, the materials of the fabricated nanopores are primarily inorganic materials such as silicon. Compared to silicon and glass-based inorganic materials, polymers have low material costs, a wide range of physiochemical properties, surface-modification protocols. Nanochannel/nanoslit structures in a polymer substrate have mainly been fabricated by nanoimprinting mostly because the long channel/slit structures do not require high aspect-ratio molding. In contrast, the fabrication of perforated nanopores in a polymer substrate requires extremely high aspect-ratio molding because the thickness of the polymer substrate (or membrane) cannot be reduced by the same ratio as the reduction in the pore size to maintain the mechanical strength of the polymer substrate (or membrane). To date, sub-10 nm pores in polymer substrates have only been demonstrated via ion track-etching techniques [66]. A polymer film is irradiated by single energetic heavy ions, followed by chemical etching of the resulting latent tracks. Using ion track-etched nanopores, the ion transport behaviors across nanopore membranes have intensively been studied by the Siwy group for potential applications in nanofluidic electronics, biosensing, separation and single-molecular manipulations [67-69]. The track-etching method in combination with a masking technique enabled the production of a single nanopore in polymers. However, it is difficult to position the nanopore at an exact location of a substrate in a deterministic manner, which is important for scaling up the fabrication of nanopore devices and integrating the nanopore device with additional device components such as nanoelectrodes or electronics. In conclusion, nanoimprinting is one of the most promising approaches to fabricate nano-devices based on polymer-based nanopore in a high-throughput way. Its scalability and compatibility with polymer substrates make it particularly suitable for the mass production of nanopore-based systems.

From the summary and analysis of solid-state nanopore fabrication methods, it is evident that the reported techniques face challenges involving trade-offs between fabrication efficiency, cost, scalability, and the achievable minimum nanopore diameter. Focused ion beam and transmission electron microscopy drilling methods can efficiently fabricate sub-10 nm nanopores in thin films. However, the low throughput and reliance on expensive equipment make these methods unsuitable for large-scale

fabrication. Similarly, the controlled dielectric breakdown method enables the cost-effective and straightforward production of individual nanopores as small as 1 nm. Despite its simplicity, this method is limited by issues such as the formation of multiple nanopores, particularly during the fabrication of larger pores. Furthermore, while polymer nanopores fabricated via nanoimprinting offer potential advantages in terms of material properties and low-cost scalability, their integration into current electronic devices remains limited due to the predominant use of inorganic materials, such as silicon, in large-scale integrated circuits.

In contrast, the wet etching method with feedback control provides a cost-effective and scalable solution for the fabrication of silicon nanopores, owing to its compatibility with semiconductor technologies and MEMS processes. Additionally, the size and material properties of silicon nanopores can be modified through various deposition techniques, such as atomic layer deposition (ALD), significantly enhancing their versatility. The semiconducting nature of silicon further enables the regulation of electrical characteristics by incorporating gates, making silicon nanopores highly adaptable to diverse applications.

Table 1.1 Comparison of the reported solid-state nanopore fabrication methods

Method	**Material**	**Feature size**	**Shape**	**Scale**	**Controllability**	**Cost**
FIB、TEM	Si、Si_3N_4、Graphene	1.3 nm	Cylinder	Individual	Good	High
CBD	Si_3N_4、SiO_2、H_fO	1~3 nm	Cylinder	Individual	Bad	Low
Ion track etching	Polyimide polyester	51 nm	Cylinder	Array	Middle	Middle
Nanoimprint	AlO、polymer	10 nm	Cylinder	Individual or array	Good	High
Metal assisted chemical etching	Si	50 nm	Pyramid	Array	Bad	Middle
Anisotropic wet etching	Si	0.98 nm	Pyramid	Individual or array	Good	Low

However, the wet etching method faces a critical limitation in its lack of precise controllability, presenting significant challenges in fabricating silicon nanopores with

extremely small diameters. Smaller nanopores are essential for the detection of small molecules, as they substantially improve the signal-to-noise ratio. To enable reproducible large-scale fabrication of silicon nanopores, addressing the controllability issue in the wet etching process is imperative. Solving this challenge will pave the way for the widespread adoption of silicon nanopores in advanced sensing and nanofluidic applications.

1.3. ADVANTAGES OF SINGLE-CRYSTAL SILICON NANOPORE

Addressing the significant challenges associated with single-crystal silicon nanopore fabrication, this thesis proposes a controllable fabrication method for silicon nanopores using anisotropic wet etching. Compared with other nanopore materials, silicon nanopores offer several distinct advantages in terms of fabrication method, structure, and material properties.

Fabrication Method

The fabrication method introduced in this thesis is based primarily on anisotropic wet etching using KOH aqueous solutions, and the proposed etch-stop approach is based on the properties of the semiconductor nature of silicon. As a result, this fabrication process is inherently compatible with semiconductor manufacturing and MEMS technologies, enabling large-scale and cost-effective fabrication of silicon nanopores.

Nanopore Structure

The well-established anisotropic wet etching process allows the development of silicon nanopores with a pyramid structure, where the minimum effective size at the tip of the pyramid can approach the scale of a single silicon atom. This demonstrates the potential of this method for fabricating nanopores with extremely small sizes. Additionally, the asymmetric geometry of the pyramid structure induces an asymmetric surface charge distribution, resulting in ionic rectification. Nanopores with inherent rectification properties hold significant promise as candidates for ionic field-effect transistors and have enormous potential for applications in energy conversion, biosensing, and ionic circuits. These unique structural features also offer opportunities for advanced nanofluidic systems, where controlled ion transport is critical.

Silicon Material

Silicon, as a fundamental material in integrated circuits, provides essential support for the entire information industry. It exhibits excellent thermodynamic and chemical stability and is fully compatible with semiconductor processes. Following the fabrication process, the surface of the silicon nanopore can be further modified using various deposition techniques to tailor its structure, size, and surface properties. Moreover, due to silicon's semiconductor nature, its electrical properties can be modulated through doping or other modifications. The involvement of gate structures enables further regulation of silicon's electrical characteristics, making it adaptable to

different fabrication processes and applications. This adaptability positions silicon nanopores as versatile platforms for integration into next-generation sensing, computational, and energy conversion technologies.

1.4. THESIS STRUCTURE

This thesis focuses on fabricating single-crystal solid-state nanopores using a three-step wet etching method. The research encompasses the analysis of the formation principles of silicon nanopores, the factors influencing the fabrication process, and the realization of extremely small nanopores using a highly sensitive ionic current-monitored method. The potential applications based on silicon nanopores including nano-mask lithography and biosensing were verified. Furthermore, the controllable fabrication of nanopores through a wet etching process is achieved by incorporating an electrochemical passivation etch-stop strategy. Finally, an ionic FET based on the fabricated silicon nanopore is developed, and its electrical properties are systematically investigated. The structure of this thesis is organized as follows:

Chapter 1 introduces the research background, providing an overview of the current state of solid-state nanopore fabrication methods. The chapter highlights the advantages of single-crystal silicon nanopores over other types of nanopores and establishes the significance of this study.

Chapter 2 explores the formation principles of single-crystal silicon nanopores fabricated by anisotropic wet etching from the atomic and macroscopic perspectives. The chapter also investigates key factors influencing the etching process and then proposes the advanced TSWE method based on anisotropic wet etching for fabricating nanopores/slits, offering a comprehensive understanding of the fabrication process.

Chapter 3 reports a highly sensitive ionic current-monitored method to realize the fabrication of single-crystal silicon nanopores/nanoslits with extremely small sizes. Quantitative analysis of nanopore size and corresponding ionic current provides a theoretical basis for controllable fabrication. By combining slow (111) crystal plane etching and a fast-stop system with the TSWE method, extremely small nanopores and nanoslits are successfully obtained. Finally, the nano-mask lithography based on the obtained nanopore is verified.

Chapter 4 presents an etch-stop strategy based on heavy boron doping and electrochemical passivation to develop the precise control of silicon etching and further realize the etch-stop of silicon during the etching process. Based on the proposed slow etching and etch-stop approach, the controllable fabrication of single-crystal silicon nanopores by the TSWE method was achieved.

Chapter 5 reports an ionic field-effect transistor based on the fabricated single-crystal silicon nanopore. The electrical characteristics of the ionic FETs were studied, and the potential application of biosensing was confirmed.

Chapter 6 summarizes the achievements of this thesis, and a brief outlook for future research is also given.

REFERENCE

[1] Kasianowicz JJ, Brandin E, Branton D, et al. Characterization of individual polynucleotide molecules using a membrane channel. Proceedings of the National Academy of Sciences of the United States of America. 1996, 93(24), 13770-13773.
[2] Feng Y, Zhang Y, Ying C, et al. Nanopore-based Fourth-generation DNA Sequencing Technology. Genomics, Proteomics & Bioinformatics. 2015, 13(3), 4-16.
[3] Venkatesan BM, Bashir R. Nanopore sensors for nucleic acid analysis. Nature Nanotechnology. 2011, 6(10), 615-624.
[4] Miles BN, Ivanov AP, Wilson KA, et al. Single molecule sensing with solid-state nanopores: novel materials, methods, and applications. Chemical Society Reviews. 2012, 42(1), 15-28.
[5] Dekker C. Solid-state nanopores. Nature Nanotechnology. 2007, 2, 209.
[6] Deng T, Li M, Wang Y, et al. Development of solid-state nanopore fabrication technologies. Science Bulletin. 2015, 60(3), 304-319.
[7] Storm AJ, Chen JH, Zandbergen HW, et al. Translocation of double-strand DNA through a silicon oxide nanopore. Physical Review E. 2005, 71(5), 10.
[8] Larkin J, Henley R, Bell DC, et al. Slow DNA transport through nanopores in hafnium oxide membranes. Acs Nano. 2013, 7(11), 10121-10128.
[9] Fologea D, Gershow M, Ledden B, et al. Detecting Single Stranded DNA with a Solid State Nanopore. Nano Letters. 2005, 5(10), 1905.
[10] Wanunu, M.; Meller, A. Chemically, Modified Solid-State Nanopores. Nano Lett. 2007, 7 (6), 1580-1585.
[11] Yusko EC, et al. Real-time shape approximation and fingerprinting of single proteins using a nanopore. Nat. Nanotechnol. 2017, 12, 360-367.
[12] Chuah K, et al. Nanopore blockade sensors for ultrasensitive detection of proteins in complex biological samples. Nat. Commun. 2019, 10, 2109.
[13] Xing Y, Dorey A, Jayasinghe L, Howorka S. Highly shape-and size-tunable membrane nanopores made with DNA. Nat. Nanotechnol. 2022, 17, 708-713.

[14] Brinkerhoff, H., Kang, A. S., Liu, J., Aksimentiev, A. & Dekker, C. Multiple rereads of single proteins at single–amino acid resolution using nanopores. Science 374, 1509-1513 (2021).
[15] Feng, J. Liu, K. Bulushev, R. D. Khlybov, S.; Dumcenco, D.; Kis, A. Radenovic, A. Identification of Single Nucleotides in MoS2 Nanopores. Nat. Nanotechnol. 2015, 10, 1070-1076.
[16] Yamazaki, H.; Hu, R.; Zhao, Q.; Wanunu, M. Photothermally Assisted Thinning of Silicon Nitride Membranes for Ultrathin Asymmetric Nanopores. ACS Nano 2018, 12, 12472-12481.
[17] Wang, R.; Gilboa, T.; Song, J.; Huttner, D.; Grinstaff, M. W.; Meller, A. Single-Molecule Discrimination of Labeled DNAs and Polypeptides Using Photoluminescent-Free TiO2 Nanopores. ACS Nano 2018, 12 (11), 11648-11656.
[18] Kaikai C, Jinbo Z, Ulrich F. Keyser, Nanopore-Based DNA Hard Drives for Rewritable and Secure Data Storage. Nano Lett. 2020, 20, 3754.
[19] Liu, C., Gillette, E., Chen, X. et al. An all-in-one nanopore battery array. Nature Nanotech 9, 1031-1039 (2014).
[20] J. D. Feng, M. Graf, K. Liu, D. Ovchinnikov, D. Dumceno, M. Heiranian, V. Nandigana, N. R. Aluru, A. Kis, A. Radenovic. Single-layer MoS2 nanopores as nanopower generators. Nature 536, 197-200 (2016).
[21] Makusu Tsutsui, Wei-Lun Hsu, Denis Garoli, Iat Wai Leong, Kazumichi Yokota, Hirofumi Daiguji, and Tomoji Kawai. ACS Nano 2024 18 (23), 15046-15054
[22] Siwy. Z, Ion-Current Rectification in Nanopores and Nanotubes with Broken Symmetry. Adv. Funct. Mater. 2006, 16, 735.
[23] H. Hong, X. Lei, J. Wei, Y. Zhang, Y. Zhang, J. Sun, G. Zhang, P. M. Sarro, Z. Liu, Rectification in Ionic Field Effect Transistors Based on Single-crystal Silicon Nanopore. Adv. Electron. Mater. 2024, 10, 2300782.
[24] T. Deng, Y. F. Wang, Q. Chen, H. J. Chen, Z. W. Liu. Massive fabrication of silicon nanopore arrays with tunable shapes. Applied Surface science 390, 681-688, (2016).
[25] Chen Q, Liu Z. Fabrication and Applications of Solid-State Nanopores. Sensors. 2019, 19(8), 1886.
[26] S. S. Zeng, C. Y. Wen, P. Solomon, S. L. Zhang, Z. Zhang. Rectification of protein translocation in truncated pyramidal nanopores. Nat. Nanotechnol, 2019, 14, 1056-1062.
[27] Chang, H.; Kosari, F.; G., A.; Alam, M. A.; Vasmatzis, G.; Bashir, R, DNA-Mediated Fluctuations in Ionic Current through Silicon Oxide Nanopore Channels Nano Lett. 2004, 4, 1551-1556.
[28] Wang, Yifan. Chen, Qi. Liu, Zewen, Self-Aligned Nanopore Formed on a SiO2 Pyramidal Membrane by a Multipulse Dielectric Breakdown Method. Journal of Physical Chemistry C, 2018, 122, 11516-11523.
[29] Waugh, M., Briggs, K., Gunn, D. et al. Solid-state nanopore fabrication by automated controlled breakdown. Nat. Protoc 15, 122-143 (2020).

[30] Lei. X, Zhang. J, Hong. H, Wei. J, Liu. Z, Jiang. L, Controllable Fabrication and Rectification of Bipolar Nanofluid Diodes in Funnel-Shaped Si3N4 Nanopores, all. 2023, 19, 2303370.
[31] E. Cao, D. Cain, S. Silva, Z. S. Siwy, Ion Concentration Polarization Tunes Interpore Interactions and Transport Properties of Nanopore Arrays. Adv. Funct. Mater. 2024, 34, 2312646.
[32] Su, S., Zhang, Y., Peng, S. et al. Multifunctional graphene heterogeneous nanochannel with voltage-tunable ion selectivity. Nat Commun 13, 4894 (2022).
[33] Wang J.; Cheng C.; Zheng X.; Idrobo J. C.; Lu A.-Y.; Park J.-H.; Shin B. G.; Jung S. J.; Zhang T.; Wang H.; et al. Cascaded Compression of Size Distribution of Nanopores in Monolayer Graphene. Nature 2023, 623 (7989), 956-963.
[34] Heekyeong Park, Seungho Baek, Anamika Sen, Bongjin Jung, Junoh Shim, Yun Chang Park, Luke P. Lee, Young Jun Kim, and Sunkook Kim, Ultrasensitive and Selective Field-Effect Transistor-Based Biosensor Created by Rings of MoS2 Nanopores, ACS Nano 2022 16 (2), 1826-1835.
[35] Wang, F., Zhao, C., Zhao, P. et al. MoS2 nanopore identifies single amino acids with sub-1 Dalton resolution. Nat Commun 14, 2895 (2023).
[36] Ramya H. Tunuguntla et al. Enhanced water permeability and tunable ion selectivity in sub-nanometer carbon nanotube porins. Science, 357, 792-796 (2017).
[37] Peng W, Yan S, Zhou K, Wu HC, Liu L, Zhao Y. High-resolution discrimination of homologous and isomeric proteinogenic amino acids in nanopore sensors with ultrashort single-walled carbon nanotubes. Nat Commun. 2023 May 9;14(1):2662.
[38] Kim MJ, Mcnally B, Murata K, et al. Characteristics of solid-state nanometer pores fabricated using a transmission electron microscope. Nanotechnology. 2007, 18(20), 7554-7560.
[39] Lin Y, Ying YL, Shi X, et al. Direct sensing of cancer biomarkers in clinical samples with a designed nanopore. Chemical Communications. 2017, 53(84), 11564.
[40] Krapf D, Wu MY, Smeets RM, et al. Fabrication and characterization of nanopore-based electrodes with radii down to 2 nm. Nano Letters. 2006, 6(1), 105-109.
[41] Lo CJ, Aref T, Bezryadin A. Fabrication of symmetric sub-5 nm nanopores using focused ion and electron beams. Nanotechnology. 2006, 17(13), 3264-3267.
[42] Wu S, Cao F, Zheng H, et al. Fabrication of faceted nanopores in magnesium. Applied Physics Letters. 2013, 103(24), 1193.
[43] Morin A, Lucot D, Ouerghi A, et al. FIB carving of nanopores into suspended graphene films. Microelectronic Engineering. 2012, 97(6), 311-316.
[44] Gierak J, Madouri A, Biance AL, et al. Sub-5nm FIB direct patterning of nanodevices. Microelectronic Engineering. 2007, 84(5), 779-783.
[45] Patterson N, Adams DP, Hodges VC, et al. Controlled fabrication of nanopores using a direct focused ion beam approach with back face particle detection. Nanotechnology. 2008, 19(23), 235304.

[46] Marshall MM, Yang J, Hall AR. Direct and Transmission Milling of Suspended Silicon Nitride Membranes with a Focused Helium Ion Beam. Scanning. 2012, 34(2), 101-106.
[47] Hemamouche A, Morin A, Bourhis E, et al. FIB patterning of dielectric, metallized and graphene membranes: A comparative study. Microelectronic Engineering. 2014, 121(6), 87-91.
[48] Gierak J, Mailly D, Hawkes P, et al. Exploration of the ultimate patterning potential achievable with high resolution focused ion beams. Applied Physics A. 2008, 1089(1), 187-194.
[49] Michiel van den Hout et al, Controlling nanopore size, shape and stability. Nanotechnology. 2010, 21, 115304.
[50] Kim, M, Wanunu, M., Bell, D. and Meller, A, Rapid Fabrication of Uniformly Sized Nanopores and Nanopore Arrays for Parallel DNA Analysis. Adv. Mater, 2006, 18, 3149-3153.
[51] Y Kwok, H. Briggs, K. Tabard-Cossa, V. Nanopore Fabrication by Controlled Dielectric Breakdown, PLoS ONE 9, e92880 (2014).
[52] Arcadia, C. E., Reyes, C. C, Rosenstein, J. K. In situ nanopore fabrication and single-molecule sensing with microscale liquid contacts. ACS Nano 11, 4907-4915 (2017).
[53] Zhang. Y, Miyahara. Y, Derriche. N, Yang. W, Yazda. K, Capaldi. X, Liu. Z, Grutter. P, Reisner. W. Nanopore formation via tip-controlled local breakdown using an atomic force microscope. Small Methods 3, 1900147 (2019).
[54] Waugh, M., Briggs, K., Gunn, D. et al. Solid-state nanopore fabrication by automated controlled breakdown. Nat. Protoc 15, 122-143 (2020).
[55] Wang, Y., Ying, C., Zhou, W. Vreede. L., Liu, Z., Tian, J. Fabrication of multiple nanopores in a SiNx membrane via controlled breakdown. Sci Rep 8, 1234 (2018).
[56] Cuifeng Ying, Jared Houghtaling, Olivia M. Eggenberger, Anirvan Guha, Peter Nirmalraj, Saurabh Awasthi, Jianguo Tian, Michael Mayer. Formation of Single Nanopores with Diameters of 20–50 nm in Silicon Nitride Membranes Using Laser-Assisted Controlled Breakdown. ACS Nano 12, 11458-11470 (2018).
[57] Yamazaki H, Hu R, Zhao Q, et al. Photothermally Assisted Thinning of Silicon Nitride Membranes for Ultrathin Asymmetric Nanopores. Acs Nano. 2018, 12(12), 12472-12481.
[58] Ye Ai, Jing Liu, Bingkai Zhang, Shizhi Qian, Ionic current rectification in a conical nanofluidic field effect transistor, Sensors and Actuators B: Chemical, Volume 157, Issue 2, 2011, Pages 742-751.
[59] Nguyen Van Toan et al, Ion transport by gating voltage to nanopores produced via metal-assisted chemical etching method, Nanotechnology, 2018, 29, 195301.
[60] Park SR, Peng H, Ling XS. Fabrication of nanopores in silicon chips using feedback chemical etching. Small. 2007, 3(1), 116-119.

[61] Hong, H., Wei, J., Lei, X. et al. Study on the controllability of the fabrication of single-crystal silicon nanopores/nanoslits with a fast-stop ionic current-monitored TSWE method. Microsyst Nanoeng, 2023, 9, 63.
[62] Deng, Tao et al, Controllable Fabrication of Pyramidal Silicon Nanopore Arrays and Nanoslits for Nanostencil Lithography, Journal of Physical Chemistry C, 2014, 118, 18110-18115.
[63] Qi Chen, Yifan Wang, Tao Deng, Zewen Liu, Fabrication of nanopores and nanoslits with feature sizes down to 5 nm by wet etching method, Nanotechnology. 2018, 29, 085301.
[64] Siwy, Z., Dobrev, D., Neumann, R, Preparation of synthetic nanopores with transport properties analogous to biological channels, Appl Phys A. 2003, 76, 781.
[65] Yang, J., Pan, T., Xie, Z, In-tube micro-pyramidal silicon nanopore for inertial-kinetic sensing of single molecules, Nat Commun. 2024, 15, 5132.
[66] Siwy, Z. S. and Howorka, S. Engineered voltage-responsive nanopores. Chem. Soc. Rev. 2010, 39, 1115-1132.
[67] Mara, A., Siwy, Z., Trautmann, C., Wan, J. & Kamme, F. An asymmetric polymer nanopore for single molecule detection. Nano Lett. 4, 497-501, (2004).
[68] Heins, E. A., Siwy, Z. S., Baker, L. A. & Martin, C. R. Detecting single porphyrin molecules in a conically shaped synthetic nanopore. Nano Lett. 5, 1824-1829, (2005).
[69] Vlassiouk, I. & Siwy, Z. S. Nanofluidic diode. Nano Lett. 7, 552-556, (2007).

2

ANALYSIS OF THE FORMATION PRINCIPLE OF SILICON NANOPORES BASED ON ANISOTROPIC WET ETCHING

2.1. INTRODUCTION

The formation principles of nanopores provide critical theoretical guidance for predicting the morphology and size of fabricated nanopores, as well as for achieving controllable and reproducible fabrication of extremely small nanopores. This chapter focuses on the anisotropic etching of single-crystal silicon using potassium hydroxide (KOH) solution, a widely adopted method in microscale and nanoscale silicon manufacturing.

The chapter begins by exploring the formation principle and dimensional variation models of single-crystal silicon nanopores fabricated by anisotropic wet etching from an atomic-scale and macroscopic perspectives. Then the mechanism and characteristics of anisotropic silicon etching was discussed. Additionally, factors affecting the silicon etching process and nanopore quality are systematically discussed. Finally, leveraging the characteristics of anisotropic etching, a TSWE fabrication method is established, enabling the low-cost, large-scale fabrication of single-crystal silicon nanopores.

2.2. FORMATION PRINCIPLE OF SILICON NANOPORES

The anisotropic etching-based model for the formation of pyramidal silicon nanopores was first proposed by our group in 2013. To further elucidate the formation process of nanopores and optimize the control over their size and morphology, we analyze the underlying principles of anisotropic wet etching for the fabrication of conical silicon nanopores from atomic-layer and macroscopic perspectives.

To clarify the theoretical minimum value of the nanopore feature size obtained by wet etching, we performed an analysis on the single-crystal silicon atomic layers. According to the anisotropic etching characteristics of silicon, after the first step of wet etching, an inverted pyramid structure composed of four (111) planes is formed and intersects a silicon atom on a (100) plane. To simplify the analysis, we assume that the silicon atoms are etched layer by layer along the (100) direction during the third step. Under this assumption, we constructed a schematic diagram of the arrangement of silicon atoms, as shown in Fig. 2.1, in which each silicon atom is connected by chemical bonds with two silicon atoms in each of the two adjacent layers. The silicon atoms of the same color are arranged on the same (100) plane, and the silicon atoms on the black dotted line are located on the same (111) plane. As shown in Fig. 2.1, the two black dotted lines intersect at silicon atom A0 on the 1st layer. During the third step of the etching, the silicon atoms are etched layer by layer along the direction of the arrow. When the silicon atom A0 of the 1st layer is etched away, the A1 and A2 atoms are exposed and remain because these two atoms are connected by chemical bonds with the silicon atoms A3 and A4 of the 3rd layer. At this time, it can be considered that the nanopore is formed, and the nanopore obtained currently is within its theoretical minimum size, which is the distance between two adjacent silicon atoms on the (110) plane, as $\sqrt{2}a/2$

($\boldsymbol{a}$ is the lattice constant of silicon, 0.54 nm). Therefore, the theoretical minimum feature size of the nanopores obtained by wet etching is 0.38 nm.

Next, we summarize the variation in nanopore sizes as the etching process progresses. Due to over-etching, the silicon atomic layer continues to be etched to form larger nanopores. It can be concluded that when silicon atoms on the $\boldsymbol{n}$th layer are etched away, the feature size of the nanopore is $\frac{\sqrt{2}a}{2} \cdot \left[\frac{n}{2}\right]$. Therefore, since the nanopores are just formed and then continue to increase in size, their feature sizes should be 0.38, 0.76, 1.14 nm and so on. These results reveal the potential of the proposed TSWE method for fabricating nanopores/nanoslits with extremely small feature sizes.

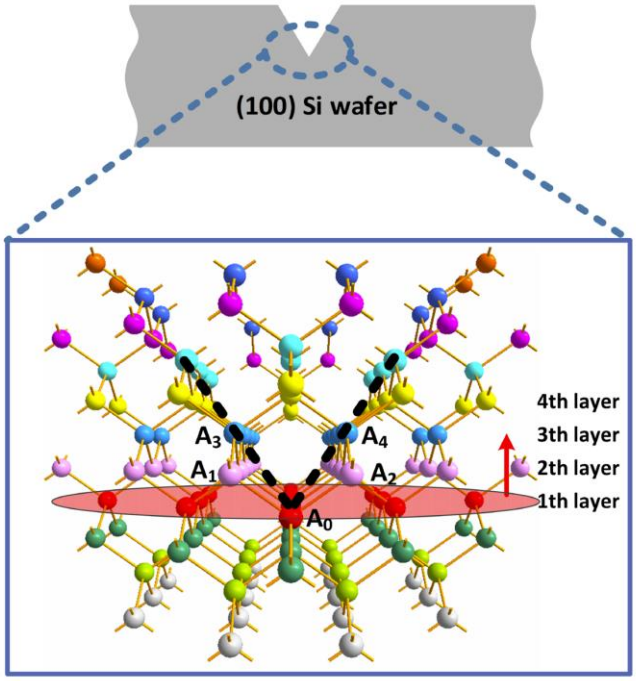

Figure 2.1 Schematic diagram of the arrangement of silicon atoms and the etching front progression during etching.

By analyzing the formation mechanism of nanopores from an atomic scale perspective, we have identified the theoretical minimum size of nanopores and their variation patterns. However, since the control of the wet etching process is typically conducted on a macroscopic scale, achieving atomic-level precision in etching outcomes is challenging. Therefore, it is also necessary to analyze the formation of nanopores from a macroscopic perspective.

Figure 2.2 illustrates the model for nanopore fabrication by anisotropic wet etching. Based on the fabrication process described earlier, square-shaped windows with dimensions W_1 and W_2 were first created on the front and back sides of the silicon wafer, respectively. Subsequently, the silicon wafer underwent a three-step wet etching process using a KOH aqueous solution.

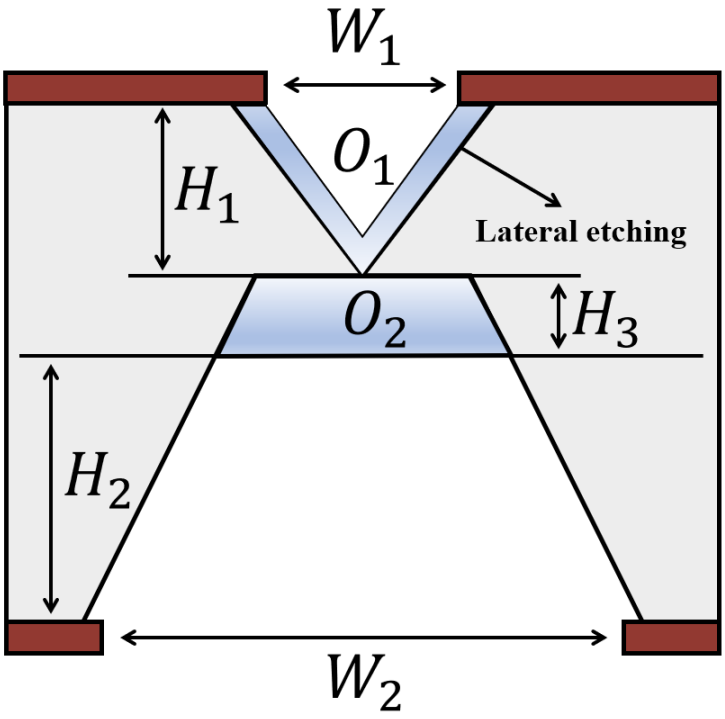

Figure 2.2 Model for silicon nanopore fabrication by anisotropic wet etching.

In the first step, anisotropic wet etching was performed on the front side of the silicon wafer, forming an inverted pyramid structure with an apex angle of 54.74°. If the lateral etching effect of silicon is neglected, the four (111) crystal planes intersect at point O_1. To more accurately explain the nanopore formation mechanism, we consider the intersection point O_2 of the four (111) crystal planes after accounting for lateral etching. This intersection point O_2 represents the apex of the final inverted pyramid structure, with the corresponding etching depth on the front side denoted as H_1, as described by eq 2.1.

$$\boldsymbol{H_1 = \left(V_{1_{(100)}} + \frac{V_{1_{(111)}}}{cos54.74^\circ}\right) \times t_1} \tag{2.1}$$

Here, $v_{1_{(100)}}$ and $v_{1_{(111)}}$ represents the etching rate of (100) and (111) silicon crystal plane, respectively. And t_1 means the etching time.

In the second step, the anisotropic wet etching is employed to form an etching cavity on the backside of the wafer, reducing the thickness of the silicon substrate. The depth of the corresponding etching cavity is denoted as H_2. It is evident that the etching depth in this step must be carefully controlled to satisfy the condition $H_1+H_2<H$, where H represents the thickness of the silicon wafer.

$$\boldsymbol{H_2 = \left(V_{2_{(100)}} + \frac{V_{2_{(111)}}}{cos54.74^\circ}\right) \times t_2} \tag{2.2}$$

Similarly, $v_{2_{(100)}}$ and $v_{2_{(111)}}$ represents the etching rate of (100) and (111) silicon crystal plane during the second wet etching step, respectively. And t_2 means the etching time.

In the third step, the remaining silicon film with thickness of H_3 is gradually etched until the apex of the inverted pyramid is reached, at which point the nanopore is considered to be fully formed. Assuming the etching rates of the silicon (100) and (111) crystal planes during the third step are $v_{3_{(100)}}$ and $v_{3_{(111)}}$, respectively, the time required for the nanopore to form, starting from the beginning of the third etching step, is denoted as t_3.

$$t_3 = (H - H_1 - H_2) / \left(V_{3_{(100)}} + \frac{V_{3_{(111)}}}{cos 54.74^\circ} \right) \tag{2.3}$$

Based on the above analysis, if other errors, such as the thickness variation of the silicon wafer, are neglected and the etching rates in all three etching steps are constant, the time required for nanopore formation can be calculated. Furthermore, the variation in nanopore sizes can also be analyzed in greater detail.

After establishing a model for nanopore formation by anisotropic wet etching, we can analyze and summarize the size and dimensional variation of nanopores during the etching process based on this model. Assuming that the etching stops precisely at the moment when the silicon atoms at the apex of the inverted pyramid are fully etched, the nanopore is considered to be formed. At this point, the theoretically smallest nanopore size is achieved.

If the feature size of the nanopore at the moment of its formation is defined as D_0, then as etching continues, the relationship between the feature size D of the nanopore and the over-etching time t can be expressed by the following equation:

$$D = 2V_{ae} \times t \times tan 57.74^\circ + D_0 \tag{2.4}$$

Here, V_{ae} represents the average etching rate of the (100) silicon crystal plane. By combining atomic-scale and macroscopic perspectives to analyze the formation mechanism of nanopores, we derived a quantitative relationship between nanopore size and over-etching time. This finding demonstrates that the feature size of nanopores can be precisely tuned by controlling the over-etching duration. Furthermore, by adjusting the shape of the wet etching windows on the front side, it becomes possible to fabricate nanopores and nanoslits with controllable aspect ratios.

Figure 2.3 illustrates the square and rectangular etching windows, along with electron microscope (SEM) images of the resulting nanopores and nanoslits. For square etching windows, where the length and width are equal, the anisotropic nature of the etching process causes the four (111) crystal planes to converge at a single point on the (100) crystal plane. Consequently, after the apex of the inverted pyramid is etched through, the resulting nanopore retains a square morphology.

In contrast, for rectangular etching windows, where the length and width are unequal, the four (111) crystal planes converge along a line on the (100) crystal plane rather than at a single point. Theoretically, the length of this line corresponds to the difference between the length and width of the etching window. As a result, after the apex of the inverted pyramid is etched through, a nanoslit with a defined initial length is formed. The aspect ratio of this nanoslit can be further adjusted by modifying the dimensions of the etching window, allowing for precise control over its geometry.

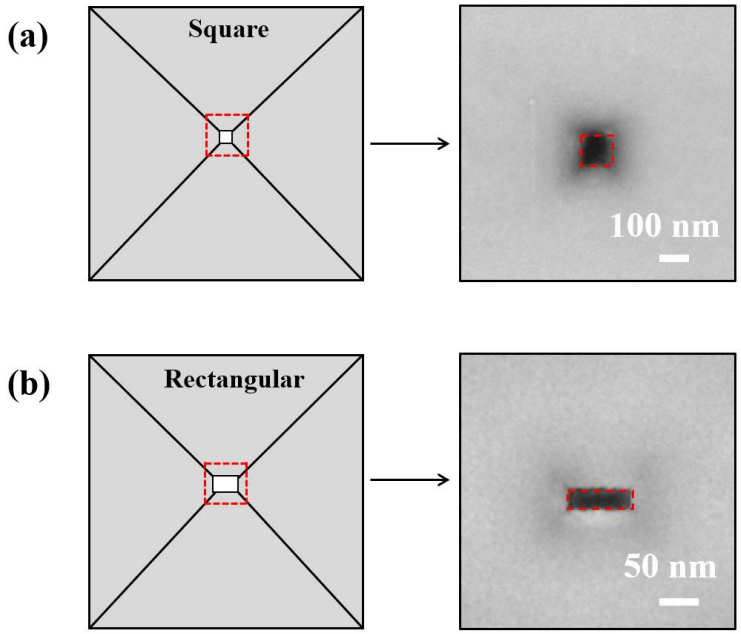

Figure 2.3 a) Square and b) rectangular etching window and corresponding SEM image of nanopore and nanoslit.

2.3. ANISOTROPIC WET ETCHING OF SINGLE-CRYSTAL SILICON

2.3.1. STRUCTURE OF SINGLE-CRYSTAL SILICON

Silicon is arguably the most well-studied material to date. It is abundantly available, ranking as the second most abundant element in the Earth's crust after oxygen. As a result, silicon is considered an inexhaustible resource. Single-crystal silicon exhibits exceptional electronic properties, which form the foundation of modern microelectronics technology and integrated circuits.

The crystal structure of single-crystal silicon is illustrated in Fig. 2.4. Single-crystal silicon adopts a face-centered cubic (FCC) lattice structure, with its smallest unit composed of a tetrahedron formed by five silicon atoms [1]. The entire silicon crystal is constructed through the periodic and orderly repetition of these unit cells in three-

dimensional space. Additionally, the arrangement of atoms varies across different crystallographic planes within the silicon crystal.

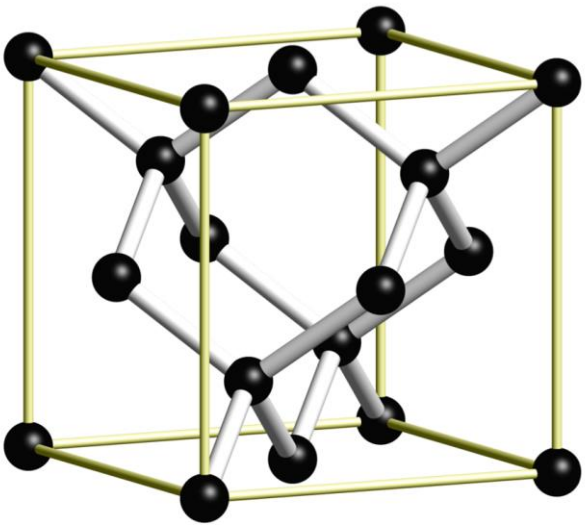

Figure 2.4 Crystal unit cell silicon

2.3.2. PRINCIPLE OF ANISOTROPIC ETCHING OF SILICON

In single-crystal silicon, three commonly observed crystallographic planes are the (110), (111), and (100) planes, as illustrated in Fig. 2.5. The atomic density varies significantly among these planes, leading to distinct structural and chemical properties. The (110) plane has the lowest atomic density; on this plane, each silicon atom forms one covalent bond with a sub-surface atom and two covalent bonds with surface atoms. The (111) plane exhibits the highest atomic density, with each silicon atom forming three covalent bonds with sub-surface atoms. The (100) plane has an intermediate atomic density, where each silicon atom forms two covalent bonds with sub-surface atoms.

This microscopic anisotropy, stemming from the varying atomic arrangements and orientations across different crystallographic planes, manifests as macroscopic differences in the etching rates of these planes during wet etching. This phenomenon, known as anisotropic etching, is critical for the precision fabrication of silicon microstructures and nanopores. It highlights the dependence of etching processes on crystallographic orientation, offering an approach for the design and control of silicon-based nanostructures.

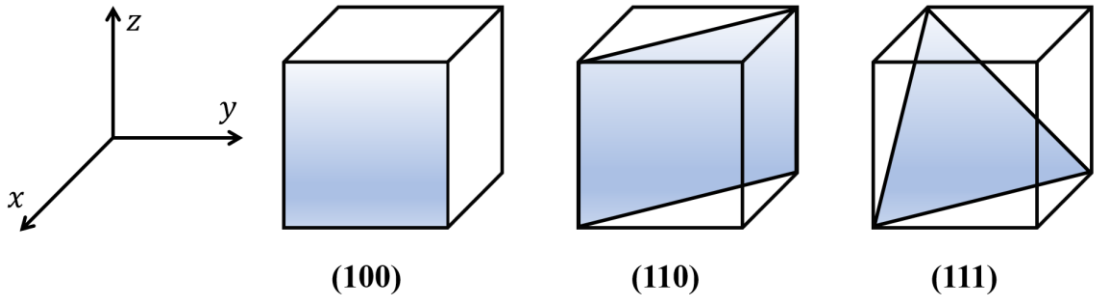

Figure 2.5 Schematic diagram of three typical crystal planes of silicon

Anisotropic etching of silicon refers to the variation in etching rates across different crystallographic planes of silicon. This principle enables the fabrication of a wide range of microstructures on silicon substrates. All anisotropic etchants are aqueous alkaline solutions, with the primary component being either organic or inorganic. The first organic etchant system, proposed in 1962, consisted of hydrazine (N_2H_4) and water, with pyrocatechol ($C_6H_4(OH)_2$) as an additive [2]. However, studies demonstrated that pyrocatechol is not an essential component and can be omitted [3]. Later experiments introduced iso-2-propyl alcohol as a third component, which acted as a moderator. Subsequently, hydrazine was replaced by ethylenediamine ($NH_2(CH_2)_2NH_2$) (EPW), a more stable and less toxic alternative.

Purely inorganic aqueous solutions, such as potassium hydroxide and sodium hydroxide (NaOH), have long been recognized for their ability to etch silicon anisotropically. Improved etching behavior was observed with the addition of isopropyl alcohol to these solutions [4]. Similarly, other alkaline hydroxides, such as lithium hydroxide (LiOH) and cesium hydroxide (CsOH), exhibit comparable etching characteristics [5]. Aqueous solutions of ammonium hydroxide (NH_4OH) have also been reported to enable anisotropic etching [6]. Furthermore, ammonium hydroxide solutions with hydrogen peroxide (H_2O_2) are widely used for cleaning silicon wafers [7]. More complex derivatives of ammonium hydroxide, such as quaternary ammonium hydroxides—including tetramethyl ammonium hydroxide ($N(CH_3)_4OH$) and choline ($(CH_3)_3N(CH_2CH_2OH)\ OH$)—can also serve as effective anisotropic etchants [8]. In this thesis, we focus on anisotropic etching based on the KOH aqueous solution.

KOH wet etching is an anisotropic etching technique commonly used in the fabrication of silicon microstructures and microelectromechanical systems (MEMS). The chemical reaction governing the etching process in alkaline solution is investigated by many researchers and several models have been proposed [9-15]. Among the different models, Gosalvez et al. model is more appropriate to explain the etching mechanism in alkaline solution [15]. The chemical reaction governing the etching of silicon in KOH can be generally summarized as:

$$\boldsymbol{Si + 2OH^- + 2H_2O = Si(OH)_4^{2-} + H_2 \uparrow} \quad (2.5)$$

In this reaction, hydroxide ions (OH^-) react with silicon, producing soluble silicate ions $(Si(OH)_4^{2-})$ and releasing hydrogen gas (H_2). The most critical factor affecting

this reaction is the OH^- concentration, which directly determines the kinetic rate of this etching reaction, i.e. the higher the concentration of reactants, the faster the rate, which will be analyzed more fully subsequently. It is worth mentioning that KOH etching is usually improved by the addition of isopropyl alcohol (IPA). Although the incorporation of IPA in silicon etching is not part of the research conducted in this thesis, the effects of IPA that have been reported on silicon etching are summarized below [16].

Surface Moderation: IPA acts as a moderator, reducing the etching rate of silicon and helping to achieve smoother surfaces. By moderating the interaction between hydroxide ions and silicon, IPA minimizes surface roughness and enhances the uniformity of the etched features.

Control of Anisotropy: The addition of IPA enhances the anisotropy of the etching process by differentially influencing the etching rates of various crystallographic planes. This improves the precision in fabricating microstructures on silicon substrates.

Reduced Bubble Formation: IPA helps reduce bubble formation on the silicon surface during etching. Bubbles can impede the etchant's access to the silicon surface and lead to irregularities; IPA mitigates this issue by improving the wettability of the silicon surface.

Surface Energy Adjustment: IPA alters the surface energy at the silicon-liquid interface, contributing to a more controlled and predictable etching process.

2.3.3. FACTORS AFFECT THE SILICON ETCHING

To enhance the controllability of the silicon etching process and facilitate the precise fabrication of nanopores, it is crucial to regulate the etching rate. This section summarizes key factors influencing the silicon etching rate, including crystal plane orientation, etching temperature, etchant concentration, doping concentration, and external electrochemical potential. Through an exploration of these factors, a comprehensive understanding of how KOH-based anisotropic etching can be optimized for fabricating nanopores with desired geometrical characteristics. These factors are briefly outlined below.

Firstly, the effect of temperature on the silicon etching rate for the (100) crystal plane was studied. Figure 2.6 presents the Arrhenius plot of the silicon etching rate at various temperatures. The graph clearly demonstrates that the etching rate of silicon increases with rising temperature. This behavior can be explained by the Arrhenius equation, which describes the temperature dependence of reaction rates:

$$\boldsymbol{R = A e^{-E_a/kT}} \tag{2.6}$$

Here R represents the etching rate, A is the pre-exponential factor, E_a is the activation energy, k is the Boltzmann constant (1.38×10^{-23} J/K), and T is the absolute temperature in Kelvin. The term kT corresponds to the average thermal energy of a single particle. As the temperature increases, the exponential term becomes larger, resulting in a higher etching rate. And the same conclusion has been conducted by other researchers [17].

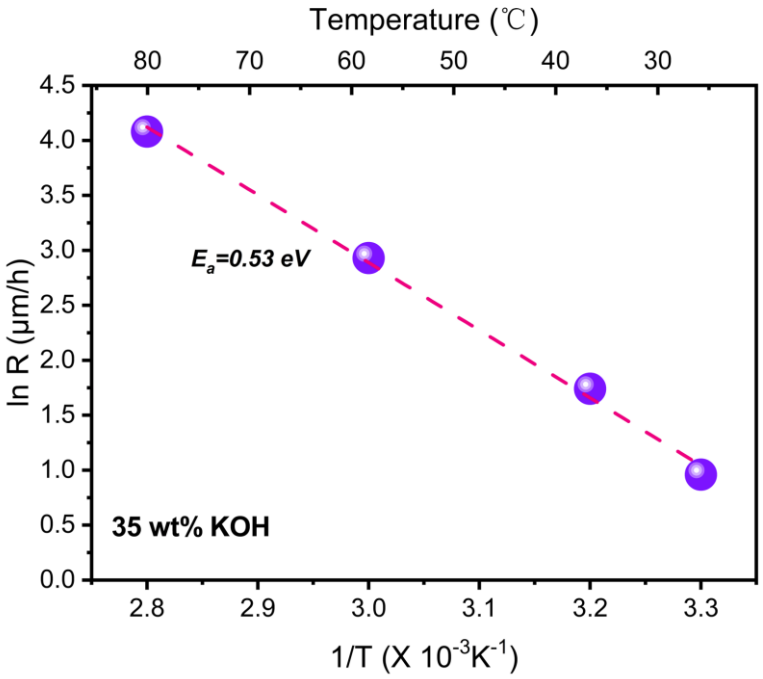

Figure 2.6 Arrhenius diagram of silicon etching rate for (100) crystal plane in a 35 wt% KOH solution.

In addition to temperature, the concentration of the KOH solution is another crucial factor influencing the silicon etching rate. Here summarizes the effects of KOH concentration on the silicon etching rate, as illustrated in Fig 2.7.

At **low concentrations (<20%)**, the etching reaction is primarily limited by the reaction kinetics of OH^- ions. As the concentration increases, the OH^- ion concentration rises, leading to a significant enhancement in the reaction rate. Additionally, the physical properties of low-concentration solutions, such as lower viscosity and higher diffusion coefficients, facilitate the removal of reaction byproducts, further promoting the etching process.

At **medium concentration range (20%-30%)**, the etching rate reaches its peak. On the one hand, the OH^- ion concentration is sufficient to saturate the reaction kinetics. On the other hand, the viscosity of the KOH solution at this concentration remains moderate, allowing reaction byproducts presented in eq 2.1 to diffuse away from the etching interface without hindering further reactions. Moreover, the solution at this concentration can form a relatively stable boundary layer on the silicon surface, reducing localized uneven etching.

At **high concentrations (>30%)**, further increases in KOH concentration result in a significant rise in solution viscosity. This leads to slower diffusion of OH^- ions, making the etching rate diffusion-limited. Additionally, the removal of reaction byproducts becomes more difficult, as they tend to accumulate on the silicon surface, forming physical barriers that hinder the etching process. Furthermore, high-concentration KOH solutions may form a passivation layer on the silicon surface, inhibiting further etching. This passivation layer is likely caused by the deposition of reaction byproducts from the solution. Finally, excessive OH^- concentrations may trigger secondary reactions, leading to nonlinear changes in the etching rate.

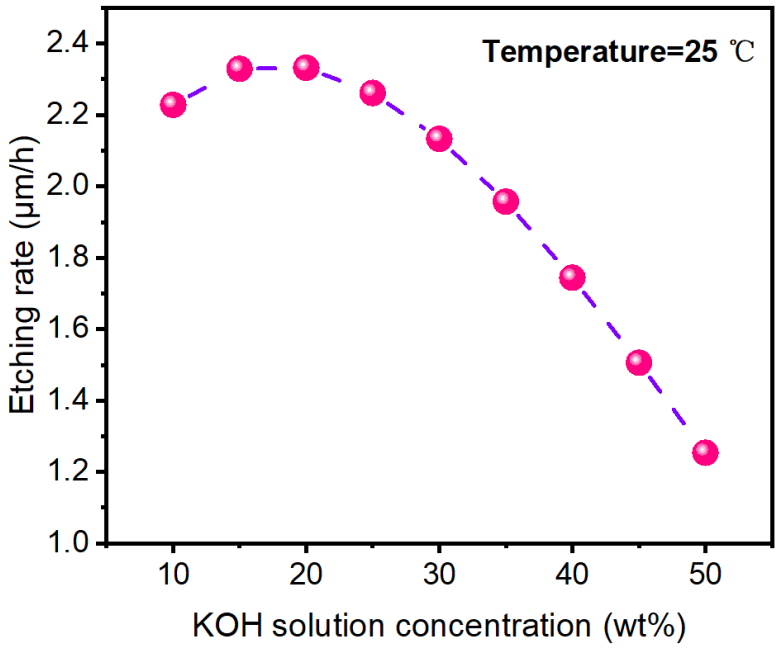

Figure 2.7 Effect of KOH solution concentration on silicon etching rate for (100) crystal plane.

It has been well-documented in the literature that the concentration of KOH solution significantly influences the surface roughness of silicon after etching. Under specific conditions, particularly at a KOH concentration of approximately 30 wt%, the surface roughness of silicon reaches its minimum [18,19]. During the fabrication of silicon nanopores by KOH-based wet etching, excessive surface roughness induced by etching can pose considerable challenges to the uniformity of silicon nanopore arrays. Furthermore, the limited precision of photolithography, including mask errors, may also result in poor uniformity within the nanopore arrays. These issues, however, can be mitigated by employing higher-precision photolithography and nanoimprint techniques [20]. Since this thesis primarily focuses on the fabrication of individual nanopores with extremely small dimensions, such etching-induced non-uniformity is negligible within the small etching area. Consequently, the impact on the fabrication of individual, extremely small-sized nanopores is minimal, and the influence of surface roughness on nanopore fabrication will not be further investigated in this section.

Figure 2.8 presents the lateral under etch rates as a function of orientation when using a 50% KOH solution at a temperature of 78℃ of <100> silicon wafer. It is evident from the figure that the etching rate of the (100) crystal plane is significantly higher than that of the (111) crystal plane. This difference is generally attributed to variations in the density of dangling bonds on these crystal planes. For instance, the dangling bond density of the (100) crystal plane is twice that of the (111) crystal plane, which partially explains why the etching rate of the (100) crystal plane is higher. However, experimental results indicate that the etching rate of the (100) crystal plane is approximately 100 times greater than that of the (111) crystal plane, with this ratio being influenced by temperature. This observation suggests that dangling bond density alone cannot fully account for the observed differences in etching rates among crystal planes. To address this limitation, the electrochemical model proposes that the etching rate variations are influenced not only by the density of dangling bonds but also by differences in the back-bond structures on the silicon surface [21].

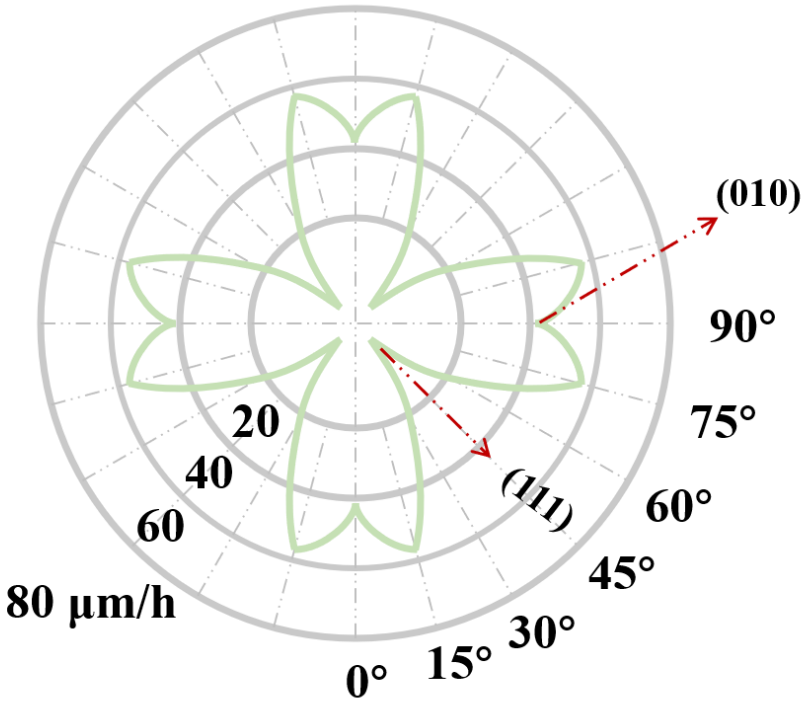

Figure 2.8 Lateral under etch rates as a function of orientation when using a 50% KOH solution at a temperature of 78℃ of <100> silicon wafer.

For the effect of crystal plane orientation on silicon etching. The number of dangling bonds on the silicon surface is closely related to its crystallographic orientation. The (111) crystal plane has the fewest dangling bonds, with each surface silicon atom possessing only one dangling bond. In contrast, the (100) crystal plane exhibits the highest number of dangling bonds, with each surface silicon atom having two dangling bonds. For the etching of the (100) crystal plane, each silicon atom with two dangling bonds can react with two OH^- and transfer two electrons to the conduction band, as

illustrated in Fig. 2.9a. Subsequently, the two Si-Si back bonds in $Si(OH)_2$ are broken, resulting in the formation of a positively charged silicon hydroxide complex, as shown in Fig. 2.9b. For the (111) crystal plane, the initial reaction involves each surface silicon atom binding with only one OH^-, as depicted in Fig. 2.9c. The subsequent step requires breaking three back bonds of the surface silicon atom, transferring three electrons to the conduction band, and binding with three OH^-, as illustrated in Fig. 2.9d. Once $Si(OH)_4$ is formed, the reaction proceeds similarly to that of the (100) crystal plane. However, due to the presence of three back bonds in the silicon atoms of the (111) crystal plane, the electron energy levels associated with these bonds are lower. As a result, the reaction depicted in Fig. 2.9d proceeds significantly more slowly than the reaction shown in Fig. 2.9b. Consequently, the etching rate of the (111) crystal plane is substantially lower than that of the (100) crystal plane. In addition, for the (110) crystal plane, although each surface silicon atom has only one dangling bond, its back-bond structure is more complex. One of the back bonds is connected to an internal atom, similar to the back-bond structure of the (111) crystal plane, while the other two are bonded to adjacent surface atoms, resembling the back-bond structure of the (100) crystal plane. This configuration gives the (110) crystal plane a back-bond structure that combines characteristics of both the (100) and (111) crystal planes. As a result, the etching rate of the (110) crystal plane typically lies between those of the (100) and (111) crystal planes, reflecting the intermediate nature of its back-bond structure.

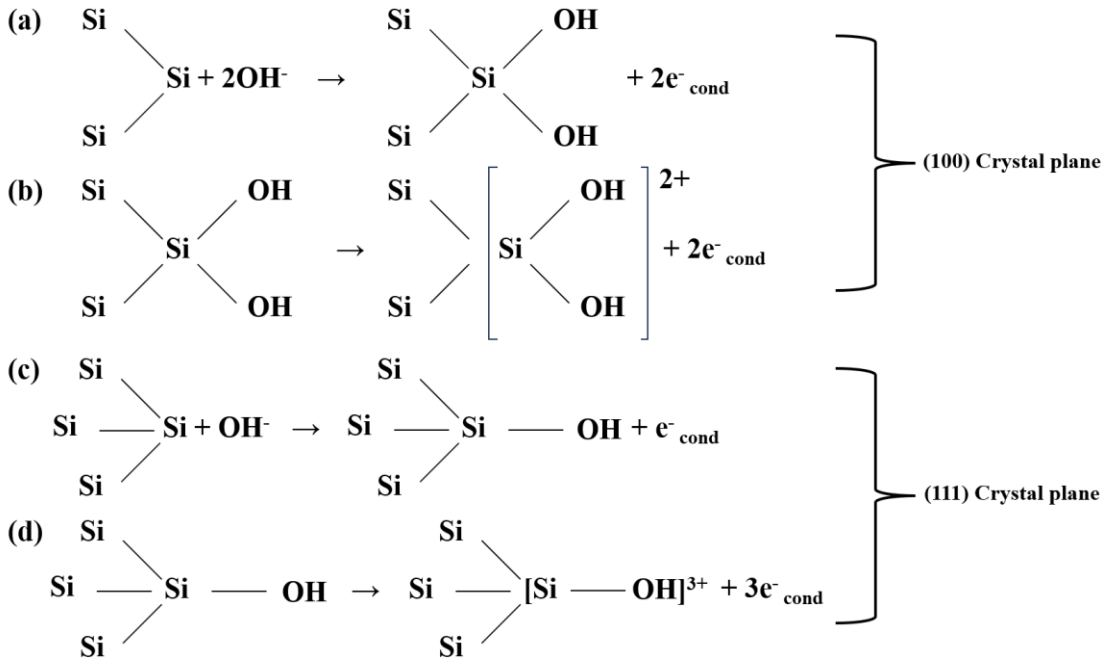

Figure 2.9 Illustration of mechanism of (100) and (111) crystal plane etching reaction.

For the effect of doping concentration on silicon etching, our primary research focus is on boron-doped P-type silicon. According to the study by Seidel et al, the etching rate

R remains approximately constant when the boron doping concentration N_B is less than $2\times10^{19}\,cm^{-3}$ [21]. However, when the boron concentration exceeds this value, the etching rate becomes inversely proportional to the fourth power of the boron concentration. First, we explain the effect of heavy doping on etching rate using the space charge layer (SCL) model.

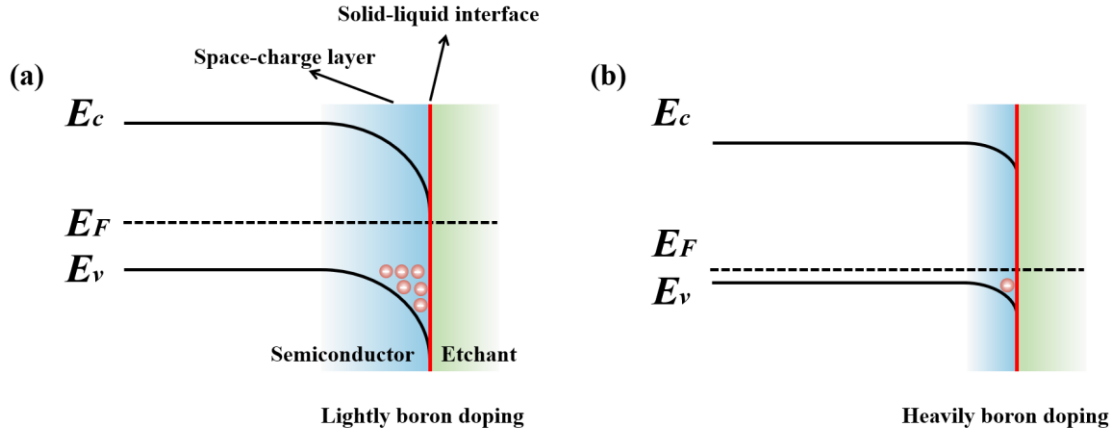

Figure 2.10 Band diagram of heavily/lightly doped P-type silicon and the interface with the etchant.

To more clearly elucidate the influence of doping concentration on the silicon etching rate through the space charge layer model, we first describe the silicon etching process using an electrochemical model.

$$\boldsymbol{Si + 4OH^- \rightarrow Si(OH)_4 + 4e_c} \quad (2.7)$$

$$\boldsymbol{4H_2O + 4e_c \rightarrow 4OH^- + 2H_2\uparrow} \quad (2.8)$$

The above reaction shows that the electron required for the second step of the reduction reaction is generated during the oxidation reaction. Figure 2.10 exhibits band diagram of heavily/lightly doped P-type silicon and the interface with the etchant. From the figure it can be observed that the Fermi level drops into the valence band due to the heavy boron-doped, inducing a sharp shrinkage of the space charge layer. The change in the width of the space charge layer induced by the doping concentration can be quantitatively described by the formula ($\boldsymbol{W = \sqrt{2\varepsilon\varepsilon_0 V_B/eN_D}}$) when a semiconductor comes into contact with a liquid interface, where W and N_D represent width of the surface charge layer and the doping concentration, respectively. As a result, heavy doping leads to an equivalent narrowing of the potential well given by the downward bending of the energy bands on the silicon surface. As a result, electrons, generated from an oxidation reaction, injected into the conduction band cannot be confined and easily tunnel through the SCL into the deeper regions of the silicon. The high hole concentration in the heavy boron-doped silicon promotes electron-hole recombination, thereby depleting the electrons available for subsequent reduction reactions and further impeding the silicon etching reaction.

Alternatively, the phenomenon can also be explained by a strain model. The strain model posits that a natural oxide layer, or pre-passivation layer, with a thickness of a few angstroms, inherently exists on the surface of silicon. In a diluted KOH solution, this oxide layer, composed of a few atomic layers of SiO_x ($1 \leq x \leq 2$), forms on the silicon surface. Compared to the etching of silicon, the etching rate of SiO_2 is significantly slower. For low doping concentrations, the etching process proceeds normally because the growth rate of SiO_x is much smaller than its etching rate. However, at higher doping concentrations, significant strain (stress) is introduced into the silicon lattice due to boron doping, which results in defects within the single-crystal silicon. These defects accelerate the growth rate of SiO_x, causing it to outpace its etching rate. Consequently, the silicon etching rate slows significantly and may eventually stop. This phenomenon indicates that stress plays a crucial role in the etching process and is strongly influenced by the doping concentration. Notably, substantial stress is only generated when the doping concentration exceeds a critical threshold, referred to as the threshold doping concentration. Beyond this threshold, the induced stress is proportional to the boron doping concentration, further intensifying the effects of the strain model on the etching behavior. [22].

In addition to qualitatively analyzing the effect of doping concentration on the silicon etching rate through the space charge layer model and the strain model, we will conduct a quantitative analysis to establish a theoretical relationship between doping concentration and etching rate. Based on this observation, the relationship between the etching rate R and the boron concentration N_B can be divided into two distinct regions. Firstly, a constant etching rate region, where R_i remains nearly constant for $N_B < 2\times10^{19}\,cm^{-3}$. Secondly, a rapid decline region, where etching decreases sharply as N_B increases beyond the threshold concentration N_0. We define the threshold doping concentration as the dividing point between these two regions. Below this threshold, the etching rate remains stable, while above it, the etching rate experiences a rapid decline due to the inverse fourth-power dependency on doping concentration. This behavior can be quantitatively described by the following equation:

$$\boldsymbol{R = R_i} \qquad \boldsymbol{N_B \ll N_0} \tag{2.9}$$

$$\boldsymbol{R \approx 1/N_B^4} \qquad \boldsymbol{N_B \gg N_0} \tag{2.10}$$

Without considering the mechanism involved, the above mentioned boundary conditions can be satisfied by the following equation:

$$\boldsymbol{R = \frac{R_i}{[1+(N_B/N_0)^a]^{4/a}}} \tag{2.11}$$

The parameter a is a real number that can take any positive value greater than zero, it determines the smoothness of the transition region around N_0. Inspection of Equation

2.11, indicates that the overall temperature behavior of the etch rate R is a superposition of the temperature dependence of R_i and of the critical boron concentration N_0 which both obey an Arrhenius law (equation 2.6) with different activation energies E_1 and E_2. According to the Arrhenius equation:

$$\boldsymbol{R_i(T) = R_0 e^{-E_1/KT}} \tag{2.12}$$

$$\boldsymbol{N_0(T) = N_0' e^{-E_2/KT}} \tag{2.13}$$

By substituting the above two equations into equation 2.11, we obtain:

$$\boldsymbol{R(T) = \frac{R_0 e^{-E_1/KT}}{\left[1+\left(N_B/N_0' e^{-E_2/KT}\right)^a\right]^{4/a}}} \tag{2.14}$$

When $N_B \gg N_0$, the equation 2.14 can be further simplified.

$$\boldsymbol{R(T) = \frac{R_0 N_0'^4}{N_B^4} e^{-(E_1+E_2)/KT}} \tag{2.15}$$

From this equation it becomes apparent, that for high boron concentrations ($N_B \gg N_0$), the activation energy of the etch rate should increase by four times the activation energy of the critical boron concentration. In subsequent experiments, the experimental results will be utilized to verify the aforementioned conclusion regarding the impact of boron doping on the silicon etching rate. Specifically, the relationship between the boron doping concentration and the etching rate will be systematically investigated across both the constant etching rate region and the rapid decline region. This validation will not only confirm the threshold doping concentration as the critical point but also provide quantitative evidence to support the inverse fourth-power dependency of the etching rate on boron concentration beyond the threshold. These findings will further elucidate the role of doping concentration in anisotropic etching processes and offer a theoretical basis for optimizing fabrication techniques.

Now the effect of external electrochemical potentials on silicon etching will be discussed. Electrochemical potential-based silicon etching retains the characteristics of anisotropic wet etching while introducing precise control over the etching rate. This control is achieved by adjusting the potential of the silicon relative to the etching solution to induce passivation. This approach is widely applied in the preparation of silicon films and is notable for its reduced dependence on doping concentration, making it particularly valuable in sensor fabrication. A three-electrode system is commonly employed to elucidate the mechanism of electrochemical etching. In this system, the working electrode (WE) is connected to the silicon wafer, where the primary etching reaction occurs. The counter electrode (CE), typically platinum, is immersed in the etching solution and serves as the current-supplying electrode. The reference electrode (RE), often a saturated calomel electrode (SCE), provides a stable and known potential

reference. The RE is connected to the reaction system via a salt bridge and does not conduct current under normal operation. In this etching system, a bias potential is applied between the working electrode and the counter electrode, creating a circuit for current flow. The reference electrode ensures the precise measurement and control of the potential applied to the working electrode. Figure 2.11 illustrates a typical current-voltage (I-V) curve observed during electrochemical silicon etching. Key characteristics of the I-V curve are as follows:

Open-Circuit Potential (Vocp): The potential at which the net current is zero, representing the equilibrium potential of the system.

Passivation Potential (Vpp): The potential at which the current reaches its maximum. This point signifies the onset of passivation as a silicon oxide layer begins to form.

Flade Potential (Vfp): The potential at which the current decreases rapidly and stabilizes at a lower value due to forming a stable passivation layer.

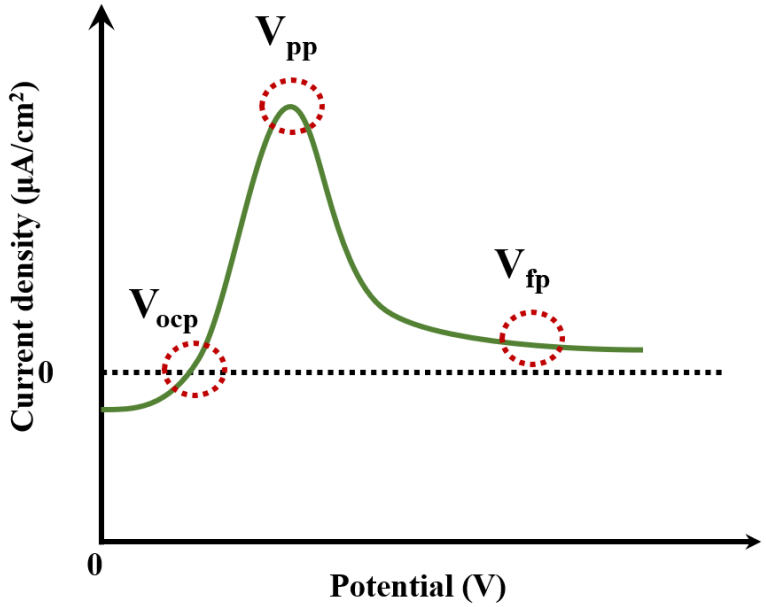

Figure 2.11 I-V characteristics curve of electrochemical etching.

As the potential is adjusted across these regions, distinct etching mechanisms are observed. In the following, we will explore the silicon etching mechanisms corresponding to different potential ranges, providing insights into the behavior of silicon under electrochemical etching conditions.

Silicon can undergo anisotropic etching in KOH, with the (100) crystal plane exhibiting the highest etch rate compared to other crystallographic planes. The etching mechanism is strongly influenced by the molecular interactions in the solution, and H_2O plays a pivotal role in facilitating the etching process for most anisotropic etchants.

The proposed mechanism begins with a water molecule attacking and breaking a Si-Si bond, leading to the formation of surface species such as Si-H and Si-OH groups. These intermediate species undergo further reactions with water and hydroxide ions (OH^-),

resulting in the formation of a doubly ionized silicate species, $Si(OH)_2(O^-)_2$. This silicate species is then dissolved into the solution, completing the etching process.
The overall net reaction for the etching of silicon in KOH can be expressed as:

$$\boldsymbol{Si + 2H_2O + 2OH^- \rightarrow 2H_2 \uparrow + Si(OH)_2(O^-)_2} \quad (2.16)$$

Below, the mechanism of etching under different characteristic potentials will be explained with the aid of band diagrams.

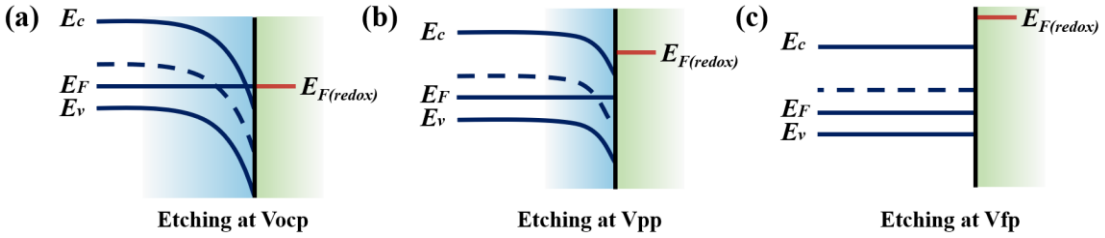

Figure 2.12 Simplified energy band diagram of p-type Si for a) open circuit potential b) passivation potential c) flade potential.

At the open-circuit potential (OCP), the Fermi level of silicon (E_F) aligns with the redox potential of the solution (E_{Fredox}), ensuring equilibrium at the silicon-electrolyte interface [23]. This equilibrium condition is illustrated in the simplified band diagram shown in Fig. 12a. A positive band bending occurs for both n-type and p-type silicon, induced by the initial injection of electrons from the solution into the silicon surface. These electrons subsequently participate in the formation of the doubly ionized silicate, which is removed into the solution as part of the etching process.
Although the chemical etching reaction remains identical for both p-type and n-type silicon, the extent of band bending differs due to their distinct electrical properties. From the known values of the OCP and flat-band potential (Vfp), it can be concluded that p-type silicon exhibits greater band bending compared to n-type silicon under identical conditions. This difference arises from the relative positions of the Fermi level within the silicon band structure, influencing the distribution of charge carriers at the surface and, consequently, the etching dynamics.
If the potential of the Si working electrode is improve by the applied potential, hole concentration at the Si surface will significantly increase, resulting in promoting the surface to a higher oxidation state [24]:

$$\boldsymbol{Si + 2h^+ \rightarrow Si^{+2}} \quad (2.17)$$

At these potentials water molecules will be electrolyzed and the OH- groups are attracted towards the silicon surface where they hydrolyze the surface Si atom:

$$\boldsymbol{Si^{+2} + 2OH^- \rightarrow Si(OH)_2} \quad (2.18)$$

As the applied potential increases, hydroxide ions (OH^-) accumulate at the silicon surface, inhibiting the attack of water molecules on the silicon substrate. This leads to the formation of a low-density oxide layer at the silicon-water interface, which acts as an additional barrier to water molecule penetration. Consequently, the etching rate decreases with further increases in the applied potential, while the rate of oxide growth accelerates. Eventually, the process transitions entirely from etching to oxide growth, with the silicon surface being passivated by a silicon dioxide (SiO_2) layer. The formation of SiO_2 is accompanied by the liberation of hydrogen gas (H_2), as described in the reaction:

$$\boldsymbol{Si(OH)_2 \rightarrow SiO_2 + H_2 \uparrow} \tag{2.19}$$

The external potential at which the silicon surface becomes passivated is referred to as the passivation potential. At this potential, the holes required for surface passivation are either generated within the space charge region of the silicon or transported to the Si/KOH interface from the electrolyte solution. This passivation process leads to the formation of a stable oxide layer, effectively halting further etching. A simplified band diagram illustrating this condition is presented in Fig. 12b. The reaction described in Equation 2.19 is intrinsically linked to the potential of the silicon. At lower potentials, where the current is small, the growth rate of the oxide layer is relatively slow, and the oxide layer formed is porous. This porous structure provides minimal protection, allowing silicon to be easily etched. As the potential (and corresponding current) increases, the growth rate of the oxide layer also accelerates, leading to a denser and more protective oxide layer. When the potential (current) becomes sufficiently large and reaches the passivation potential (Vpp), the silicon surface is entirely covered with a compact and stable oxide layer, effectively halting further etching.

At very high potentials, specifically at the Flade potential (Vfp), the growth rate of the oxide layer surpasses its dissolution rate, leading to the development of a thick and stable oxide layer on the silicon surface. This oxide layer acts as a robust mask, isolating the silicon from the etching solution. As a result, the reaction between the silicon surface and the etchant. At this stage, the silicon band gap is no longer bent, as depicted in Fig. 12c, reflecting the absence of significant charge carrier exchange at the interface. Consequently, the etching process effectively halts, and the silicon surface remains passivated under the protective oxide layer.

Electrochemical etching based on a three-electrode system allows precise control of the silicon etching process by regulating the growth of the passivation layer (oxide layer) through the application of external potential. This enables the regulation of etching dynamics with high precision, making it an effective approach for silicon processing. In addition to potential regulation, the efficiency and characteristics of electrochemical etching are influenced by several factors, similar to other chemical etching techniques:

Silicon Crystal Orientation: The anisotropic nature of silicon etching results in different etch rates for various crystal planes. For instance, the (100) crystal plane typically exhibits a higher etching rate compared to the (111) plane due to differences in atomic density and dangling bond configurations.

Doping Concentration: The concentration and type of dopants significantly impact the etching behavior. Higher doping concentrations, particularly with boron, can reduce etch rates by enhancing passivation through increased stress and oxide growth.

Etching Temperature: Temperature influences the reaction kinetics and diffusion rates in the etching solution, directly affecting the etching rate and surface quality of the silicon.

Light Exposure: Light exposure can generate electron-hole pairs in the silicon, which may alter the local electrochemical conditions and impact the etching dynamics, especially for photo-assisted etching processes.

Etching Solution Ratio: The concentration of the etching solution components, such as KOH and water, determines the aggressiveness of the etchant and the resulting etching characteristics, including rate, surface roughness, and passivation layer formation.

By understanding and optimizing these parameters, electrochemical etching can be tailored to achieve precise and uniform silicon structures for various applications in microelectronics and MEMS technologies.

2.4. FABRICATION OF SILICON NANOPORES BASED ON ANISOTROPIC WET ETCHING

Building on the principles of anisotropic wet etching and the underlying formation mechanism of nanopores, we propose a three-step wet etching method for the fabrication of single-crystal silicon nanopores and nanoslits. A thorough understanding of these process flows can help identify critical process parameters and evaluate their effects on the morphology and dimensions of the nanopores. Figure 2.13 exhibits the schematic illustration of the main fabrication process flows based on anisotropic wet etching. A 4-inch silicon-on-insulator (SOI) wafer was employed as the initial substrate. This wafer consisted of a 5.0±0.5 μm thick undoped silicon (100) device layer, which was separated from the 300±10 μm thick undoped bulk silicon (100) substrate by a 1000±50 nm buried oxide layer (SiO_2, referred to as the “BOX” layer). The SOI structure provided a high-quality silicon device layer and a well-defined BOX layer, essential for precise control over etching processes. The detailed fabrication steps of the proposed TSWE method are illustrated in Fig. 2.13.

In the first step of the process, 100 nm of silicon dioxide (SiO_2) and 200 nm of silicon nitride (Si_3N_4) were deposited on both sides of the cleaned SOI wafer. The SiO_2 layer

was grown by thermal oxidation, while the Si_3N_4 layer was deposited using low-pressure chemical vapor deposition (LPCVD). These layers served distinct purposes: the SiO_2 acted as a stress buffer to mitigate mechanical strain during processing, while the Si_3N_4 functioned as a robust mask layer for subsequent etching. Then patterns were transferred to both sides of the wafer using double-sided photolithography to achieve precise alignment of etching windows. Inductively coupled plasma (ICP) etching was then utilized to partially remove the $Si3N_4$ and SiO_2 layers, thereby exposing defined etching windows on both the front and back surfaces of the wafer for further etching. The TSWE process was subsequently implemented.

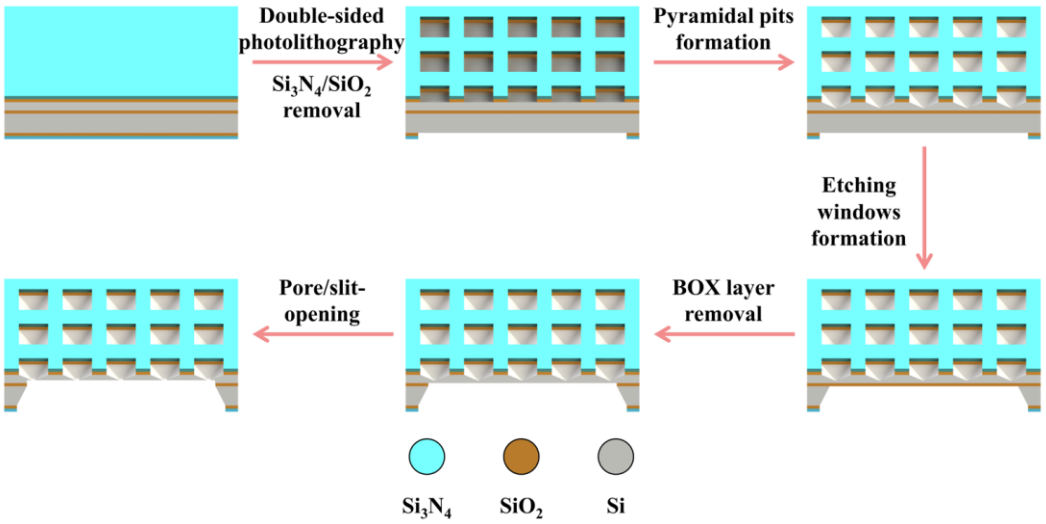

Figure 2.13 Schematic illustration of the main fabrication process flows based on anisotropic wet etching.

The first etching step was performed on the front side of the wafer in a 33% wt KOH solution at 80°C. This step resulted in the formation of pyramid-shaped pits, a characteristic feature due to the anisotropic nature of KOH etching. In the second step, the same etching process was applied to the back side of the wafer to create back etching windows, the etching will stop at the BOX layer due to the extremely low etching rate of SiO_2. It is important to note that the two aforementioned wet etching steps were carried out using a custom-designed etching setup, as shown in Fig. 2.14a. This setup, constructed from Teflon material, was specifically designed to enable single-sided etching of 4-inch silicon wafers while effectively preventing contamination. Subsequently, the BOX layer was removed using buffered hydrofluoric acid, exposing the silicon device layer for further processing. Finally, to achieve precise control over the nanopore fabrication process and to produce nanopores with distinct sizes, the 4-inch SOI silicon wafer was diced into multiple 9×9 mm^2 small chips. And the third wet etching step was carried out on these smaller pieces. This wet etching process began from the exposed windows on the backside of the chip, where the (100) crystal planes were etched upwards in an anisotropic manner. The etching progressed until the apex of the inverted pyramid structure, pre-formed on the front side, was fully etched through,

leading to the successful formation of nanopores. Similarly, the third wet etching step was also conducted using the Teflon-based etching apparatus designed for small chips, as illustrated in Fig. 2.14b.

This carefully controlled wet etching process enabled the precise fabrication of silicon nanopores with well-defined geometries and minimized damage to surrounding structures. The use of a high-quality SOI wafer, combined with advanced photolithographic alignment and etching techniques, ensured the repeatability and accuracy of the proposed method.

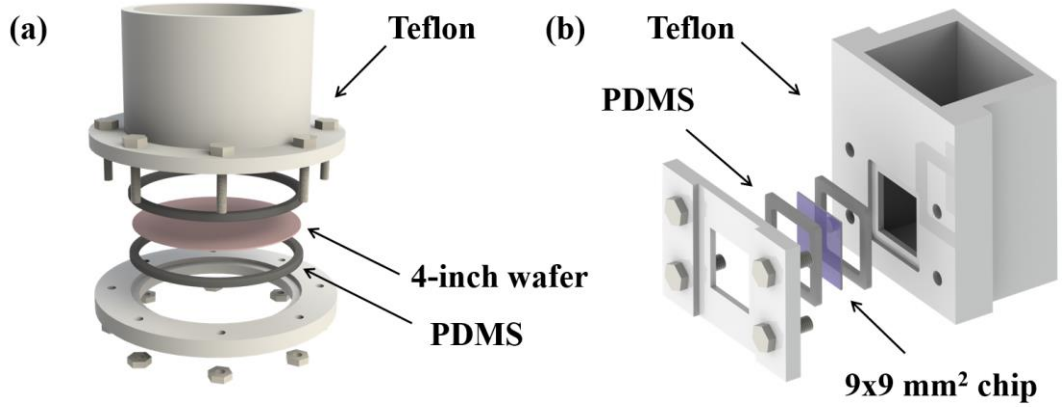

Figure 2.14 Schematic illustration of the homemade etching apparatus for a) 4-inch wafer and b) 9x9 cm^2 chip.

2.5. CHAPTER SUMMARY

In this chapter, we delve into the principles of anisotropic wet etching, with a particular emphasis on the methods and formation principles underpinning nanopore fabrication using this technique. We begin by summarizing nanopore fabrication models and dimensional variation models from both atomic-scale and macroscopic perspectives. These comprehensive analyses provide a robust theoretical framework for understanding nanopore formation mechanisms and serve as the foundation for achieving precise and controllable silicon nanopore fabrication through wet etching.

Subsequently, we systematically analyze key factors influencing the fabrication process, including temperature, etchant concentration, crystal orientation, doping concentration, and external electrochemical potentials. Each factor is explored in detail to elucidate its impact on the etching dynamics and nanopore quality.

Finally, leveraging insights from various anisotropic etching processes, we have developed an advanced TSWE method tailored for the preparation of silicon nanopores. This innovative approach facilitates not only the efficient fabrication of silicon nanopores but also establishes a reliable framework for controlling critical fabrication parameters, enabling the production of accurate and reproducible nanopore structures.

REFERENCE

[1] Jieyi Y. Jian G, Fanghong X, Xiuhong Y, Hongtao Y, Xinglong D, Hao H, Ang D, Xie Q, Guozhong C. Formation mechanism and optical characterization of polymorphic silicon nanostructures by DC arc-discharge. RSC Adv. 2015, 5, 68714-68721.
[2] H. Seidel et al. Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I. Orientation Dependence and Behavior of Passivation Layers. J. Electrochem. Soc. 1990, 137, 3612.
[3] E. S. Ammar and T. J. Rodgers, UMOS transistors on, in IEEE Transactions on Electron Devices,1980, vol. 27, no. 5, pp. 907-914.
[4] R. M. Finne and D. L Klein. A Water-Amine-Complexing Agent System for Etching Silicon. J. Electrochem. Soc. 1967, 114, 965.
[5] C. D. Fung, P. W. Cheung and W. H. Ko, A generalized theory of an electrolyte-insulator-semiconductor field-effect transistor, in IEEE Transactions on Electron Devices, 1986, vol. 33, no. 1, pp. 8-18.
[6] Orest J. Glembocki, Robert E. Stahlbush and Micha Tomkiewicz. Bias-Dependent Etching of Silicon in Aqueous KOH. J. Electrochem. Soc. 1985, 132, 145.
[7] Grundner, M., Jacob, H. Investigations on hydrophilic and hydrophobic silicon (100) wafer surfaces by X-ray photoelectron and high-resolution electron energy loss-spectroscopy. Appl. Phys. A 39, 73-82 (1986).
[8] R. J. Hamers, R. M. Tromp, and J. E. Demuth. Surface Electronic Structure of Si (111)-(7×7) Resolved in Real Space. Phys. Rev. Lett. 1986, 56, 1972.
[9] Palik ED, Bermudez VM, Glembocki OJ. Ellipsometric study of orientation dependent etching of silicon in aqueous KOH. J Electrochem Soc, 1985, 132, 871-884.
[10] Seidel H, Csepregi L, Heuberger A, Baumgärtel H. Anisotropic etching of crystalline silicon in alkaline solutions I. Orientation dependence and behavior of passivation layers. J Electrochem Soc. 1990, 137, 3612-3626.
[11] Raley NF, Sugiyama Y, Van Duzer T. (100) Silicon etch rate dependence on boron concentration in ethylenediamine pyrocatechol water solutions. J Electrochem Soc, 1984, 131, 161-171.
[12] Elwenspoek M. On the mechanism of anisotropic etching of silicon. J Electrochem Soc, 1993, 140, 2075-2080.
[13] Allongue P, Brune H, Gerischer H. In situ STM observations of the etching of n-Si (111) in NaOH solutions. Surface Sci, 1992, 275, 414-423.
[14] Allongue P, Costa Kieling V, Gerischer H. Etching of silicon in NaOH solutions II. Electrochemical studies of n Si (111) and (100) and mechanism of the dissolution. J Electrochem Soc,1993, 140, 1018-1026.
[15] Gosalvez MA. Atomistic modeling of anisotropic etching of crystalline silicon. PhD Thesis, Dissertation 123, Dissertations of Laboratory of Physics, Helsinki University of Technology, 2003.

[16] S A Campbell, K Cooper, L Dixon, R Earwaker, S N Port and D J Schiffrin. Inhibition of pyramid formation in the etching of Si p (100) in aqueous potassium hydroxide-isopropanol. J. Micromech. Microeng.1995, 5, 209.
[17] Svetlana Tatic-Lucic, Wen-Yue Zhang, Navneet Navneet. Etch-stop characteristics of heavily B/Ge-doped silicon epilayer in KOH and TMAH. Sensors and Actuators A: Physical. 2005, 123, 640-645.
[18] Tanaka H, Yamashita S, Abe Y, Shikida M, Sato K. Fast etching of silicon with a smooth surface in high temperature ranges near the boiling point of KOH solution. Sens Actuators A. 2004, 114, 516-520.
[19] Pal, P., Swarnalatha, V., Rao, A.V.N. et al. High speed silicon wet anisotropic etching for applications in bulk micromachining: a review. Micro and Nano Syst Lett.2021, 9, 4.
[20] Qi Chen, Yifan Wang, Tao Deng and Zewen Liu. Fabrication of nanopores and nanoslits with feature sizes down to 5 nm by wet etching method. Nanotechnology, 2018, 29, 085301.
[21] H. Seidel, L. Csepregi, A. Heuberger and H. Baumgärtel. Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I . Orientation Dependence and Behavior of Passivation Layers. J. Electrochem. Soc, 1990, 137, 3612.
[22] E. D. Palik. Study of the Etch-Stop Mechanism in Silicon. J. Electrochem. Soc. 1982, 129, 2051.
[23] Orest J. Glembocki, Robert E. Stahlbush and Micha Tomkiewicz. Bias-Dependent Etching of Silicon in Aqueous KOH. J. Electrochem. Soc, 1985, 132, 145.
[24] S.K Ghandhi. VLSI Fabrication Principles, John Wiley & Sons, New York 1983, ch. 7, 401-403.

3

FABRICATION OF SILICON NANOPORE/NANOSLIT WITH EXTREMALLY SMALL FEATURE SIZE BY IONIC CURRENT-MONITORED TSWE METHOD

3.1. INTRODUCTION

The application of single-crystal silicon nanopore structures in single-molecule analytical devices represents an emerging approach to the separation and analysis of nanoparticles [1]. To improve the resolution and signal-to-noise ratio (SNR) in nanopore-based molecular detection, increasingly stringent requirements have been placed on nanopore size. Additionally, nanopores play a pivotal role in numerous physiological processes, including material transfer, energy conversion, and signal transmission. For instance, signals are transmitted from nerves to the brain through nanopores during sensory processes such as sight, smell, hearing, and touch. These processes rely on the high-speed ionic transport (~10^7 ions per second per channel) of selective nanopores, which is highly dependent on nanopores with extremely small sizes, unique structures, and charge distributions [2–6]. Silicon nanopores are among the most promising candidates for mimicking these selective nanochannels. However, over-etching caused by wet etching techniques presents significant challenges to the fabrication of extremely small single-crystal silicon nanopores using anisotropic wet etching [7].

The objective of this chapter is to develop a precise and controllable fabrication strategy for silicon nanopores by introducing an ionic current-monitored method to mitigate the effects of over-etching. This approach aims to enable real-time detection of pore-opening events during the etching process. Theoretical analysis will be conducted to establish a quantitative relationship between nanopore size and ionic current, providing a foundation for precise control of nanopore dimensions. Furthermore, the fabrication of extremely small nanopores and nanoslits will be achieved by integrating the ionic current-monitoring technique with the slow etching characteristics of the (111) crystal plane and a fast-stop etching system, ensuring minimal over-etching and enhanced fabrication accuracy.

3.2. IONIC CURRENT-MONITORED TSWE METHOD

3.2.1. MECHANISM OF IONIC CURRENT-MONITORED TSWE METHOD

The effective detection of pore-opening events has long been regarded as one of the most efficient methods to minimize over-etching. In 2014, our group proposed a TSWE method based on color feedback for the large-scale fabrication of nanopores. This approach successfully produced single nanopores with feature sizes of 30 nm and 13 nm, exhibiting square-like and strip-like morphologies (tapered at the narrow opening), respectively, as well as nanopore arrays with an average size of 60 nm [8]. However, the color feedback method relies on the presence of a reference pore structure and still presents challenges in achieving precise control over pore-opening events. In this study, we introduce a highly sensitive ionic current detection method for monitoring the ionic current across the nanopore chip during the etching process. This method enables the

timely detection of pore-opening events, effectively mitigating over-etching. Furthermore, it facilitates real-time monitoring of the ionic current corresponding to the nanopore, providing a direct basis for determining the nanopore size during the etching process. By leveraging the quantitative relationship between ionic current and nanopore size, this conclusion significantly advances the fabrication of nanopores with extremely small sizes. Ultimately, it paves the way for achieving controllable and precise fabrication of silicon nanopores, meeting the different requirements of various nanoscale applications.

The fabrication process of the TSWE method has been detailed in Chapter 2. Here, we focus specifically on the third step, which involves ionic current-based detection during the etching process. Fig 3.1 shows a schematic illustration of the highly sensitive ionic current-monitored etching. From the figure, it can be observed that KCL electrolyte solution and KOH etchant solution is added to the front and backside of the silicon chip, respectively. Two Ag/AgCl electrodes connected to a source meter are immersed in the KCL electrolyte and KOH etchant to monitor the current across the nanopore chip in real time. The KOH solution is used to etch the backside (100) crystal plane of the chip until the apex of the inverted pyramid on the front side is opened, forming the nanopore. Meanwhile, the KCl electrolyte solution on the front side acts as the conductive medium after the nanopore channel is formed, ensuring that a circuit is completed across the chip and ionic current is generated.

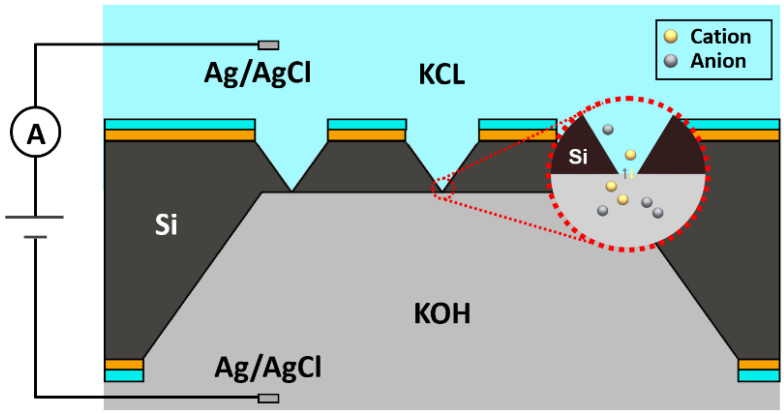

Figure 3.1 Schematic illustration of the highly sensitive ionic current-monitored etching.

The ionic current primarily originates from the potassium ions, chloride ions, and hydroxide ions in the KCL and KOH solutions. Notably, when the nanopore has not yet formed, no circuit exists, as the two solutions are separated by the silicon chip, preventing ion exchange. Theoretically, the ionic current at this stage should be zero. In practice, however, a small current can still be detected due to surface charges on the silicon, which form when it comes into contact with the electrolyte solution [9]. If the silicon membrane separating the two solutions is modeled as a resistance, its resistance decreases as the etching process progresses and the membrane becomes thinner.

Consequently, the monitored current gradually increases. Finally, at the moment the apex of the inverted pyramid is opened and the nanopore is formed, the solutions on both sides of the chip establish a conductive path, leading to a sharp increase in ionic current. This sudden jump in current, referred to as the "pore-opening point," serves as a symbol for the formation of the nanopore.

Figure 3.2 presents a typical current-time curve recorded during the pore-opening event. Prior to the pore-opening event, a gradual increase in ionic current is observed during the etching process, indicating the progressive thinning of the remained silicon membrane. Upon the occurrence of the pore-opening event, a significant and abrupt change in ionic current is recorded. The change in ionic current before and after the pore-opening event exceeds a factor of 10. This highly sensitive current response provides strong validation for the effectiveness of the ionic current-monitored method in detecting pore-opening events with high precision. It is important to note that if the etching process is not promptly terminated after the formation of the nanopore, continued etching will lead to over-etching, resulting in an increase in nanopore size. Correspondingly, the ionic current will also increase due to the enlarged nanopore size. These observations underscore the necessity of precise control over the etching process to mitigate over-etching and achieve the desired nanopore dimensions.

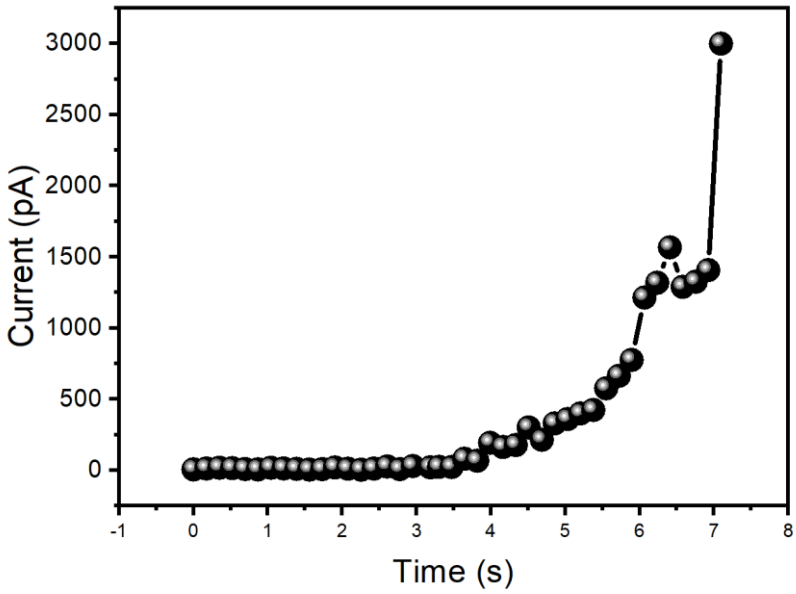

Figure 3.2 A typical current–time curve recorded during the slit-opening event.

3.2.2. IONIC CURRENT NOISE OPTIMIZATION

In the fabrication of nanopores using the ionic current-monitored TSWE method, ionic current plays a critical role in the fabrication system. Not only does the change in ionic current serve as the basis for detecting pore-opening events, but the ionic current itself is also a key indicator for determining the nanopore size after pore-opening. For nanoslits, the initial morphology typically results in a relatively large opening area at the moment of slit formation, leading to a significantly higher ionic current compared

to the pre-opening state. This phenomenon is corroborated by the slit-opening current shown in Fig. 3.2. Similarly, for nanopores with large dimension or nanopore arrays, a substantial change in ionic current is observed at the pore-opening moment.

However, for extremely small individual nanopores, the change in ionic current at the pore-opening event is less pronounced compared to the aforementioned cases. In such instances, excessive ionic current noise during the etching process can amplify or diminish the pore-opening current signal, resulting in false alarms or failure to detect the pore-opening event in a timely manner. Moreover, inaccurate ionic current measurements can adversely impact the calculation of nanopore dimensions, hindering the ability to achieve controllable fabrication of nanopores. Therefore, optimizing ionic current noise during the fabrication of extremely small nanopores is crucial. By ensuring accurate pore-opening detection and precise estimation of nanopore dimensions, the fabrication of nanopores with extremely small sizes can be effectively realized.

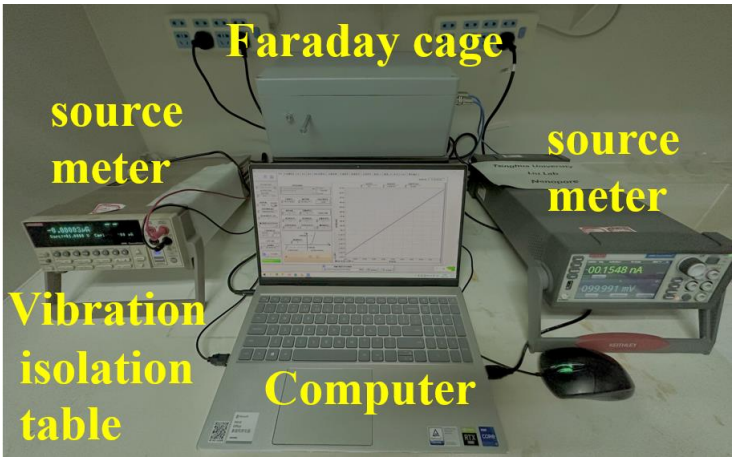

Figure 3.3 Schematic of fabrication setup of silicon nanopores based on the ionic current-monitored TSWE method

Figure 3.3 demonstrates the schematic of fabrication setup of silicon nanopores based on the ionic current-monitored TSWE method. The manufacturing system is equipped with two high-precision source meters. A Keithley 2450 (on the right) is employed to monitor the ionic current corresponding to the nanopore in real-time during the etching. This source meter provides the bias voltage while simultaneously recording the ionic current on both sides of the nanopore. It offers a maximum DC/pulse output voltage of 210 V, a DC current of 3.03 A, and a pulse current of 10.5 A, with a current measurement accuracy of up to 10 fA. The second source meter (on the left) is utilized to apply voltage in subsequent testing processes.

To optimize ionic current noise during the experiments, we categorized potential noise sources into two types: external environment noise and internal ionic current noise. External environment noise includes mechanical vibration noise and noise caused by electromagnetic waves. To minimize external noise, all experimental equipment was

placed on a vibration isolation table to reduce mechanical vibrations. Additionally, the etching fixture connected to the etching chip was fully enclosed in a metal Faraday shielding box to eliminate electromagnetic interference (EMI) from the external environment. Current noise optimization is crucial as the ionic current during testing can be as low as a few pA. To meet the requirements for a highly sensitive current monitoring and signal transmission system, a triaxial cable was used to connect the high-precision source meter to the Ag/AgCl electrodes placed in the etching or electrolyte solution. This setup not only enhances resistance to EMI but also minimizes the potential for signal radiation from the transmission lines.

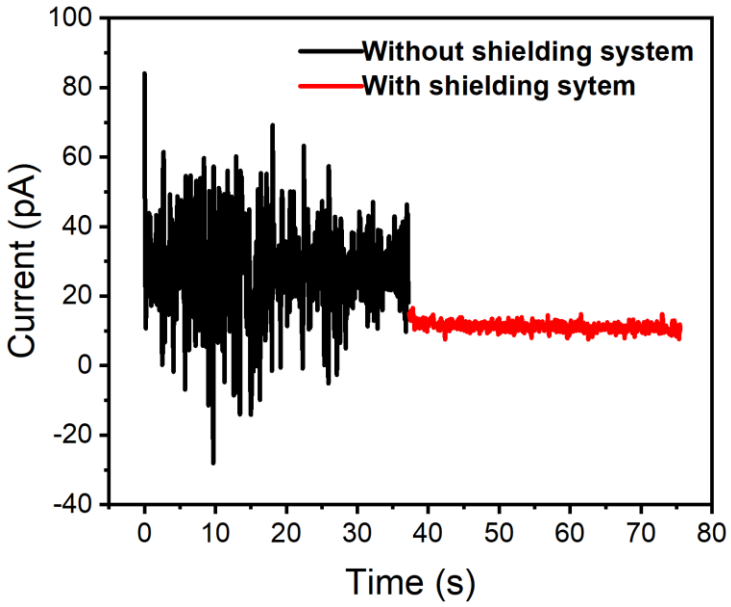

Figure 3.4 Comparison of ionic current noise before and after the shielding system

To evaluate the effectiveness of the noise-optimizing measures, we recorded the ionic current during the etching process under conditions with and without the shielding system. Figure 3.4 illustrates the comparison: the black curve represents the current signal measured without the shielding system, while the red curve represents the signal measured with the shielding system. Since nanopores had not yet formed during this phase, the ionic current was extremely small, measuring only a few pA. These small current underscores the necessity of noise optimization. As evident from the comparison, the shielding device significantly reduced the noise in the ionic current measurements, demonstrating the effectiveness of the implemented measures.

We have already optimized the external environment noise in the previous step. To further optimize and test the noise present in the ionic current during the measurement, we will use the current noise power spectral density (PSD) to characterize and analyze the source of noise in the nanopore. Figure 3.5 shows an example of the noise power spectrum of a nanopore. It can be seen that the noise of an ionic current measurement system for nanopores is mainly composed of four parts: flicker noise (1/f noise),

thermal noise, dielectric noise, and amplifier noise. Overall noise S_1 and the frequency dependences of the components of S_1 are expressed in Equation 3.1:

$$\boldsymbol{S_1 = S_{Flicker}(\propto 1/f) + S_{Thermal}(\propto 1/R_p) + S_{Dielectric}(\propto f) + S_{Amp}(\propto f^2)} \quad (3.1)$$

where $S_{Flicker}$, $S_{Thermal}$, $S_{Dielectric}$, and S_{Amp} each indicate the noise powers from each noise sources, f is the frequency, and R_p is the pore resistance. These noise sources have different effects on the overall noise characteristics of the system [10-12].

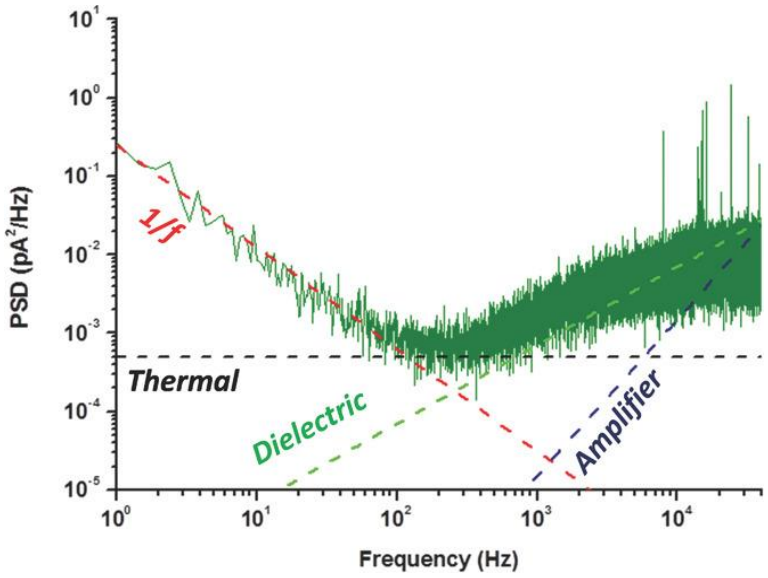

Figure 3.5 A sample noise power spectral density of a nanopore.

Flicker Noise (1/f Noise)

Flicker noise, also known as 1/f noise, originates from defects in the materials or interfaces within the measurement system. It is typically associated with charge trapping and release processes. The power spectral density of flicker noise is inversely proportional to the frequency, making it more prominent at lower frequencies. The approaches to decrease flicker noise are minimizing material defects in the electrode or electrolyte and using high-quality components with low 1/f noise characteristics. The flicker noise can be expressed by the following equation:

$$\boldsymbol{S_{Flicker} = \frac{a}{N_c f} I^2} \quad (3.2)$$

Here $S_{Flicker}$ is the flicker noise power spectrum, a is the Hooge parameter and $\boldsymbol{a = \overline{\Delta n_t^2} k_B T / N \Delta E}$. N_c, f, and I represent number of ions on nanopore cross-section, measurement frequency, and ionic current, respectively.

Thermal Noise (Johnson-Nyquist Noise)

Thermal noise arises from the random thermal motion of charge carriers (electrons or ions) in resistive elements of the system. It is white noise, with equal power across all frequencies, and is directly proportional to the resistance and temperature. The approaches to decrease thermal noise are to reduce system resistance and lower the operating temperature of the measurement setup. The thermal noise can be expressed by the following equation:

$$S_{thermal} = 4kTG_p \tag{3.3}$$

Here $S_{thermal}$ is the flicker noise power spectrum, k is the Boltzmann constant, T is the absolute temperature and G_p is the electrical conductivity.

Dielectric Noise

Dielectric noise originates from the polarization and depolarization processes in the insulating materials of the system, such as the dielectric layer in capacitors or the insulator between electrodes. It is highly dependent on the dielectric constant and the dissipation factor of the material. This type of noise is more pronounced in systems with high capacitance. The approaches to decrease dielectric noise are using low-loss, high-quality dielectric materials with low dissipation factors and minimizing parasitic capacitances in the measurement circuit.

Amplifier Noise

Amplifier noise is generated internally within the signal amplification electronics, typically arising from the input stage of the amplifier. It includes both voltage noise and current noise. The overall impact depends on the input impedance of the system and the noise characteristics of the amplifier. The approaches to decrease thermal noise are using low-noise amplifiers with minimal input noise levels and optimizing the circuit design to match the amplifier's input impedance for minimal noise contribution.

Understanding the relative contributions of these noise components is critical for further optimizing the ionic current measurement system. By addressing each source through targeted interventions, such as material improvements, circuit optimization, and environmental control, the system's overall noise level can be minimized, enabling highly precise and accurate ionic current measurements during nanopore fabrication.
During our testing, two factors significantly influenced the observed noise characteristics. First, the conductivity and ionic current were very weak before the nanopores were formed. Second, our objective was to fabricate extremely small nanopores, which inherently correspond to very low conductivity and ionic current. Consequently, as shown in eq 3.3, the contribution of thermal noise to the total noise is negligible and can be reasonably ignored in this context. Additionally, because the test frequency used in our ionic current monitoring was relatively low (<100 Hz), the noise

in the monitored ionic currents at low frequencies was predominantly flicker noise, exhibiting a characteristic 1/f behavior. This low-frequency noise in solid-state nanopores originates from the electrolyte ion trapping–detrapping process occurring on the inner surface of the nanopores [13].

Next, we employ the noise power spectral density to analyze the noise characteristics during the test process and further optimize the ionic current noise by adjusting the test parameters. First, the noise power spectral density is used to compare the external environment noise with and without the shielding system. As shown in Fig. 3.6, the noise across all frequency bands is significantly reduced when the shielding system is employed. This observation is consistent with the conclusion drawn from Fig. 3.4, confirming the effectiveness of the shielding system in reducing external noise. Moreover, the use of the shielding system notably reduces noise fluctuations, as evidenced by the smoother noise spectrum in the presence of the shielding system. This reduction in fluctuations indicates that environmental vibrations, which contribute to noise instability, are effectively mitigated by the shielding measures. These results highlight the critical role of the shielding system in enhancing the stability and accuracy of ionic current measurements.

Figure 3.7 presents the ionic current and its associated noise at different test frequencies (3 Hz, 5 Hz, 15 Hz, 30 Hz, and 60 Hz) with the shielding system. It is evident that the noise increases significantly when the frequency exceeds 15 Hz and continues to rise with increasing frequency. Figure 3.8a further illustrates the noise of the ionic current at 3 Hz, 5 Hz, and 15 Hz. While the noise increases with frequency, it remains very small (<2 pA) at 3 Hz and 5 Hz. Figure 3.8b compares the noise at these three frequencies through the power spectral density, showing that for a single measurement frequency, the 1/f noise power increases as the frequency decreases. This trend aligns well with equation 3.2. Furthermore, across different test frequencies, the same conclusion is drawn: higher test frequencies result in greater ionic current noise.

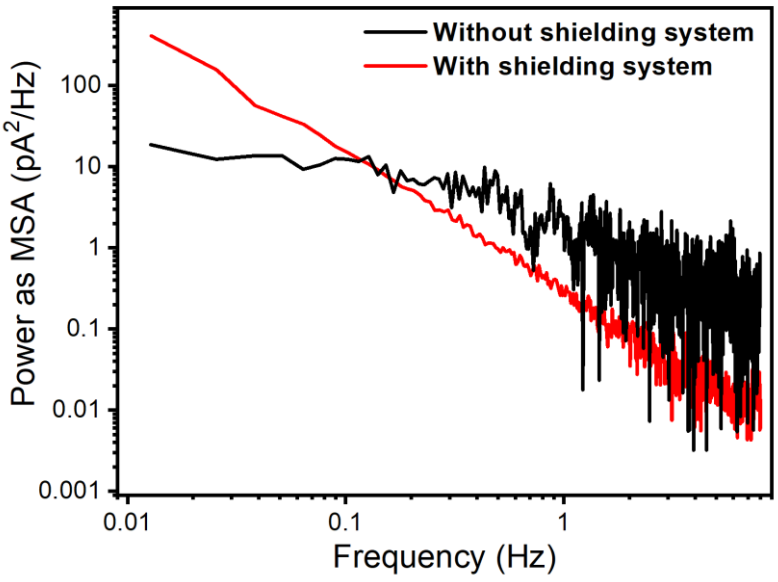

Figure 3.6 Diagram of ionic current noise power spectral density.

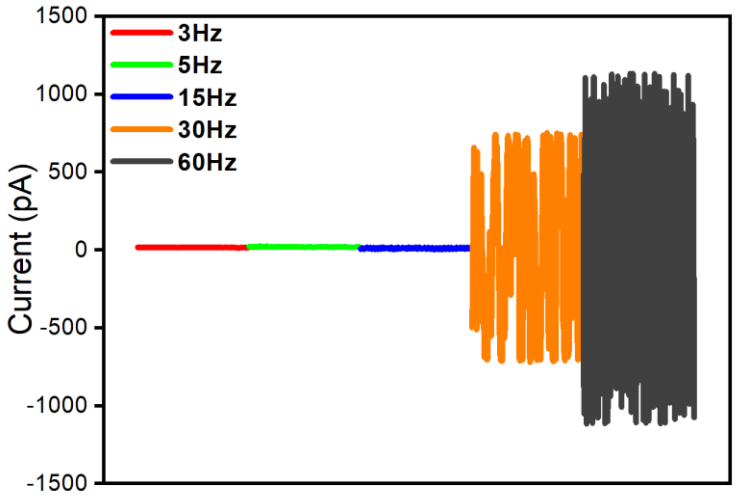

Figure 3.7 Ionic current noise under different measurement frequency.

Based on these findings, we can conclude that the addition of the shielding system significantly reduces external environmental noise, such as vibration, which improves the overall stability of the measurement platform. Additionally, the noise power spectral density analysis demonstrates that at low frequencies, such as 3 Hz and 5 Hz, the ionic current noise is minimal, approximately 2 pA. This confirms that the ionic current measurement platform constructed in this study exhibits excellent low-noise performance, fully meeting the noise requirements for fabricating nanopores with extremely small sizes.

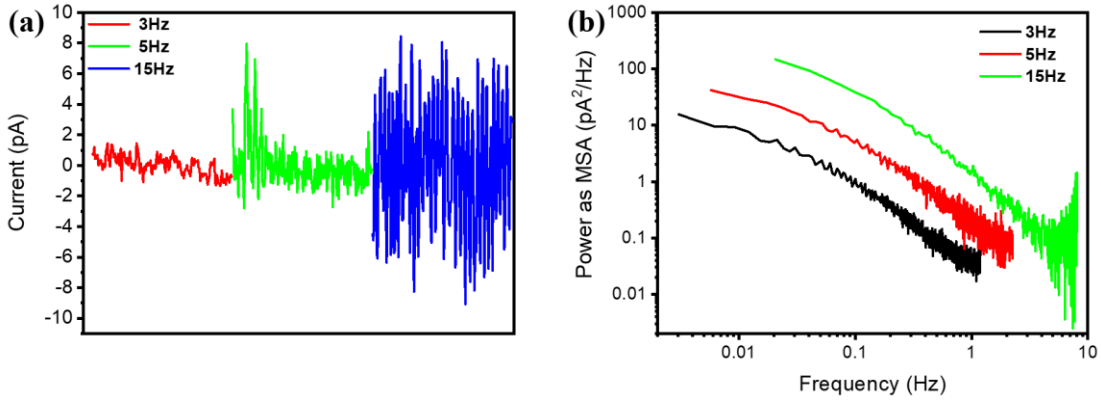

Figure 3.8 Ionic current noise of different measurement frequency and the corresponding noise power spectrum.

This study lays a solid foundation for subsequent nanopore fabrication using the ionic current-monitored TSWE method. It should be noted, however, that while low frequencies minimize noise, higher measurement frequencies are preferable for timely detection of pore-opening events, provided that the noise remains within acceptable

limits. Balancing frequency and noise are thus essential for achieving precise and efficient nanopore fabrication.

3.3. FABRICATION OF NANOSLITS WITH (111) ETCHING TSWE METHOD

3.3.1. INTRODUCTION

As previously discussed, the primary challenge in fabricating extremely small single-crystal silicon nanopores using wet etching is over-etching. To address this issue, we propose a modified TSWE method, specifically designed for fabricating silicon nanoslits, in combination with the ionic current-monitored technique. Unlike the bottom-up etching of the (100) crystal plane used to open nanopores introduced in chapter 2, the slit-opening process in this method involves top-down etching of the (111) crystal plane.

Due to the anisotropic etching properties of KOH solution on silicon, the etching rate of the (111) crystal plane is significantly slower—approximately 1/45th of the etching rate of the (100) crystal plane. Leveraging this slow etching characteristic of the (111) crystal plane enhances the controllability of the slit-opening process, minimizing the over-etching. Experimental results demonstrate that the slow etching of the (111) crystal plane effectively reduces over-etching, enabling precise control over the fabrication process. As a result, perfectly rectangular nanoslits of varying sizes were successfully fabricated, showcasing the potential of the improved TSWE method for producing high-precision nanostructures.

3.3.2. FABRICATION PROCESS

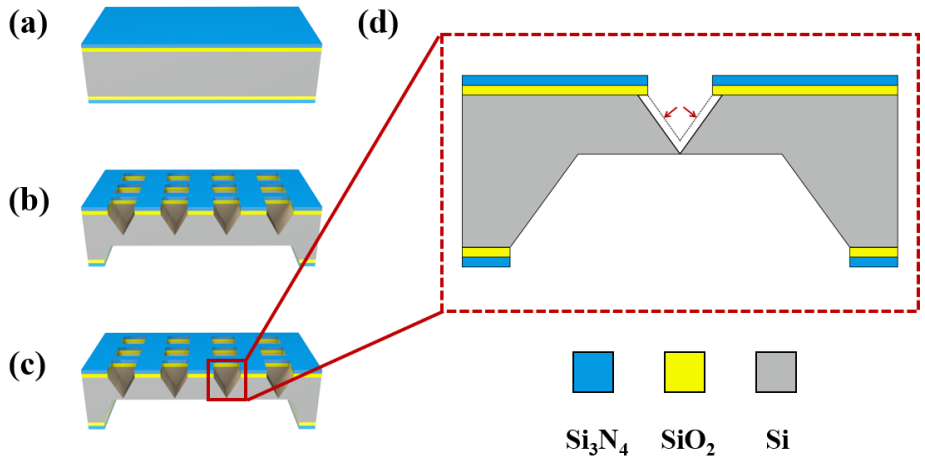

Figure 3.9 Schematic illustration of the main process steps of the TSWE method: a) double-sided SiO_2 and Si_3N_4 deposited b) the front cavity array and the back side

etching window formed c) the back-side thinning of silicon d) etching model of the (111) planes.

The main process steps of the TSWE method are illustrated in Fig. 3.9. Single-crystal silicon wafers with a diameter of 4 inches and a thickness of 300 μm were used as the original substrates. All wafers were double-polished, N-type silicon. The concentration of the KOH etching solution used in each step was maintained at 33 wt%. Initially, SiO_2 and Si_3N_4 layers were deposited on both sides of the silicon wafers using thermal oxidation and LPCVD, respectively. These layers served as stress buffers and mask layers, as shown in Fig. 3.9a. Subsequently, the front-side etching cavity array and backside etching windows were formed using 33 wt% KOH solution (Fig. 3.9b). In the next step, backside thinning of the silicon wafer was carried out using the same KOH solution until the silicon thickness was reduced to approximately 2 μm. Finally, slow-rate wet etching through the (111) crystal plane was performed until the nanoslits were fully opened. The slow etching rate of the (111) crystal plane can be explained by its unique crystallographic properties. In the (100) crystal plane, two adjacent crystal planes separate by breaking two chemical bonds, which results in a higher density of dangling bonds and correspondingly higher surface energy and lower activation energy. In contrast, in the (111) crystal plane, separating two adjacent planes requires breaking only one chemical bond. Consequently, the (111) plane has a lower density of dangling bonds, lower surface energy, and higher activation energy. Each silicon atom in the (111) plane is connected by three chemical bonds, further contributing to its high activation energy.

Since the etching rate increases with the density of dangling bonds, the etching rate of the (111) crystal plane is significantly slower than that of the (100) crystal plane. Experimental results indicate that at room temperature, the etching rate of the (111) crystal plane is approximately 1/45th of that of the (100) crystal plane. This remarkably low etching rate effectively reduces over-etching, enabling precise and controllable fabrication of nanoslits.

3.3.3. RESULT AND DISCUSSION

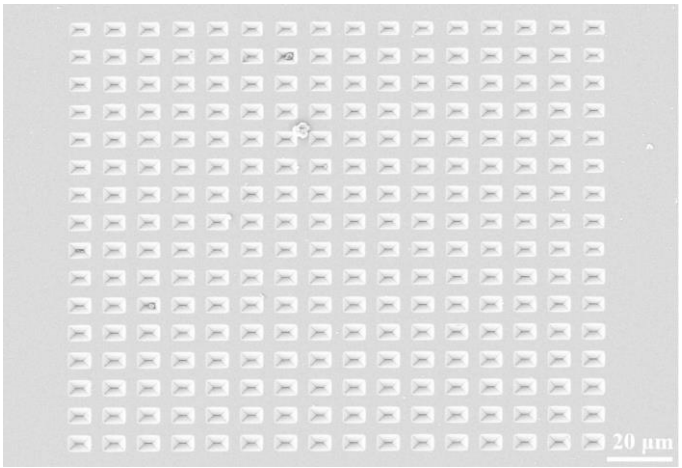

Figure 3.10 SEM micrograph of the 16 × 16 etching cavity arrays.

After the first step of the wet etching process, Figure 3.10 presents a scanning electron microscope micrograph of a 16 × 16 etching cavity arrays, demonstrating that the front-side etching cavities were successfully fabricated over a large area. Each cavity measures approximately 8 × 4 μm, showcasing the capability of the method for precise large-area patterning. Figure 3.11 illustrates a backside etched window with a 0.5 × 0.5 mm² exposed area. From the enlarged view, it is evident that some nanoslits have already been opened, validating the effectiveness of the proposed method in nanoslit fabrication.

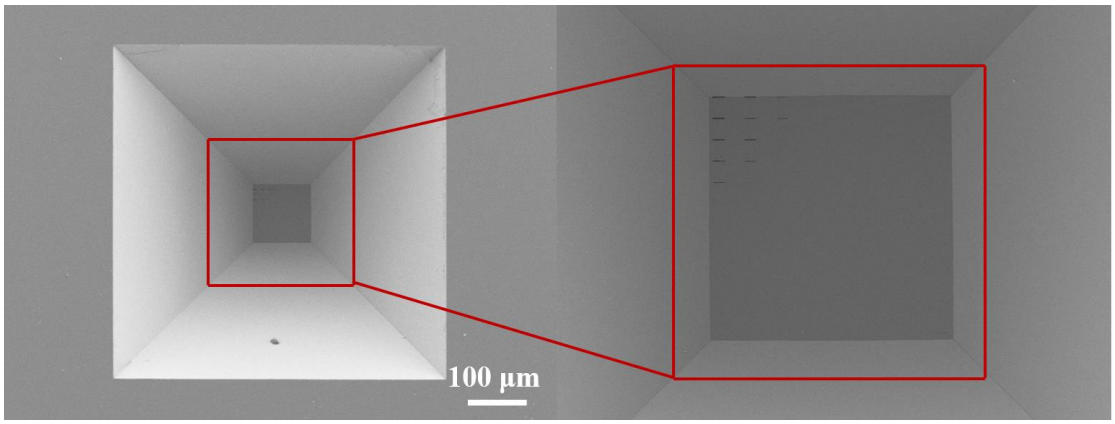

Figure 3.11 SEM micrograph of the back etching window.

Figure 3.12 provides a close-up view of the fabricated nanoslits, revealing their rectangular shape, which aligns with the designed mask pattern. The measured distance between the upper and lower nanoslits is 8.035 μm. However, some nanoslits deviate from the strict rectangular shape. This discrepancy can be attributed to inhomogeneous etching, where variations in the slit-opening time across different areas and differences in over-etching after the slit-opening event occur. These findings highlight the need for improved uniformity and controllability during the wet etching process.

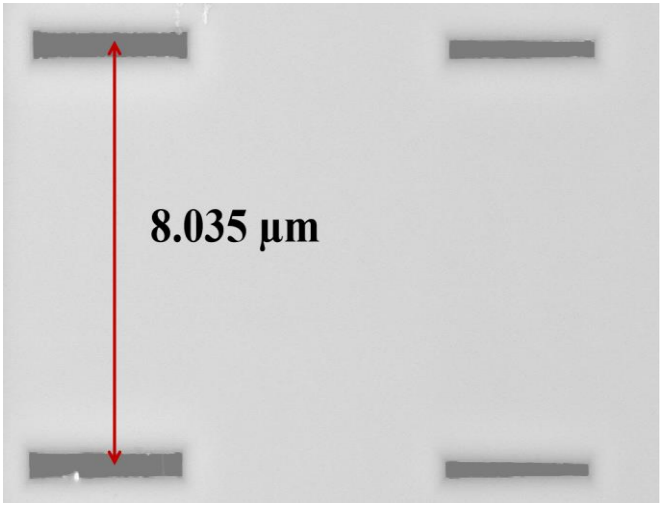

Figure 3.12 SEM micrograph of the fabricated nanoslits array.

The best result with 7 s over-etching is shown in Fig. 3.13, where the smallest feature size achieved for a nanoslit is 8.3 nm. The slow etching rate of the (111) crystal plane (~0.04 μm/h) effectively reduced over-etching, enabling precise and reproducible control over the nanoslit sizes.

To further investigate the morphology and dimensions of fully opened nanoslits, Figure 3.14 exhibits an SEM micrograph of a fully etched (1 h) nanoslit array. An 8 × 8 nanoslit array was successfully fabricated, with all nanoslits maintaining the rectangular shape defined by the front-side etching cavities shown in Fig. 3.10. These results confirm that all nanoslits were completely opened as intended.

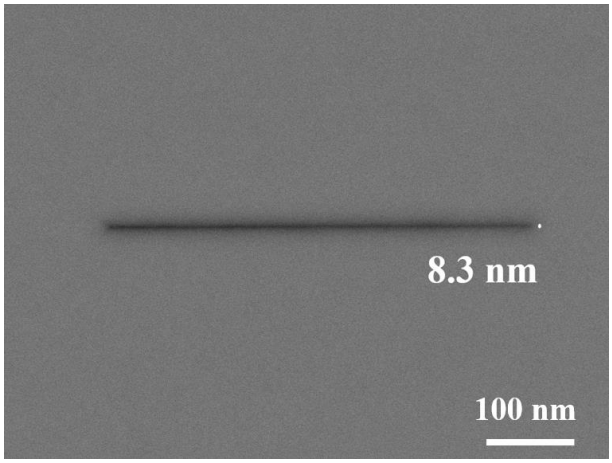

Figure 3.13 SEM micrographs of individual nanoslit fabricated by the TSWE method, with a feature size of 8.3 nm.

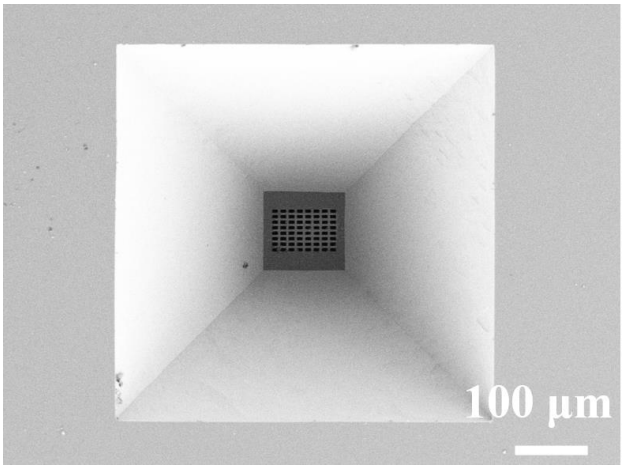

Figure 3.14 SEM micrographs of fully opened nanoslit array.

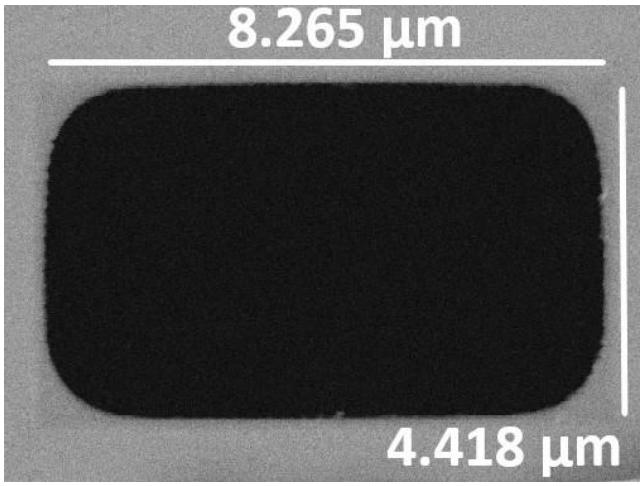

Figure 3.15 SEM micrographs of a fully opened individual nanoslit.

Finally, sufficient etching (30 min) was conducted after the slit-opening, the nanoslit dimensions were fully realized. Figure 3.15 displays a completely opened nanoslit with dimensions of 8.265 µm in length and 4.418 µm in width, corresponding to the front-side cavity dimensions. As a conclusion, this study reports a modified TSWE method for fabricating solid-state silicon nanoslits. The slit-opening process utilizes (111) crystal plane etching. Due to the relatively slow etching rate of the (111) crystal plane compared to the (100) crystal plane (~0.2 µm/h), over-etching was significantly reduced, resulting in good controllability of the slit-opening process. Perfectly rectangular nanoslits with various dimensions were successfully fabricated, achieving a smallest feature size of 8.3 nm. However, some deviations from the rectangular shape were observed, primarily due to inhomogeneous etching. The proposed method offers a controllable and reproducible approach for fabricating diverse silicon-based nanostructures, paving the way for advanced applications in nanotechnology [14].

3.4. FABRICATION OF SILICON NANOPORE/NANOSLIT WITH EXTREMALLY SMALL FEATURE SIZE BY A FAST-STOP IONIC CURRENT-MONITORED TSWE METHOD

3.4.1. INTRODUCTION

In last section, we have proposed achieving the fabrication of extremely small nanopores/nanoslits by alleviating over-etching through the slow etching of the (111) crystal plane. Additionally, Siwy et al. utilized a stopping medium (acid) to mitigate over-etching [15], while Park et al. employed a similar approach for silicon nanopores, manually halting the reaction after the pore-opening [16]. Although these methods improve precision to some extent, they still have notable limitations. Specifically, the addition of a stopping medium merely slows the etching rate rather than stopping the reaction entirely, allowing over-etching to persist. Moreover, the heat released during

the neutralization reaction between acid and alkali can accelerate the etching process and induce ionic current fluctuations, complicating current-based controllable fabrication. Meanwhile, manual intervention to stop the reaction after pore-opening increases the likelihood of over-etching and is incompatible with large-scale manufacturing processes based on MEMS technology.

To address these challenges. Here, we report the integration of the TSWE method with a fast-stop, highly sensitive ionic current-monitored system for fabricating single-crystal silicon nanopores and nanoslits with various dimensions. In the third step of the TSWE method, pore-opening etching is meticulously monitored using a highly sensitive ionic current detection process, and the etching reaction is governed by a fast-stop system. This approach significantly enhances fabrication accuracy, precision, and reproducibility while enabling the reduction of the minimum achievable feature size. By quantitatively analyzing the relationship between ionic current and nanopore size, and setting different current jump ratios, nanopores of precise dimensions were successfully fabricated. The smallest deviation between the obtained and theoretical sizes was as low as 1.4 nm. These results demonstrate that the proposed fast-stop ionic current-monitored TSWE method enables the efficient fabrication of individual SCS nanopores and nanoslits with extremely small sizes.

3.4.2. FABRICATION SYSTEM

In the fabrication process of extremely small nanopores and nanoslits using the fast-stop ionic current-monitored TSWE method, the initial steps including film deposition, double-sided lithography, dry etching to form an etching window, the first step of the TSWE method to create a pyramid structure on the wafer's front side, and the second step to etch a back cavity. This section will focus on the third step of the TSWE method. In the third step, a fast-stop highly sensitive ionic current-monitored etching system was developed to precisely detect the pore-opening event, as illustrated in Fig. 3.16. The system consists of two Teflon-fabricated etching chambers separated by a silicon chip. The front-side chamber is filled with 1 M KCl solution, while the back-side chamber contains 33 wt% KOH solution. Ag/AgCl electrodes, connected to a Keithley 2450 source meter, are placed in both chambers to continuously monitor changes in ionic current during the etching process.

Additionally, a pipe for pumping the etching solution is integrated into the chamber design. To minimize environmental interference during measurements, the entire setup is enclosed within a Faraday cage. According to the etching rate and thickness of the remained silicon membrane, the pore-opening process typically requires approximately 45 minutes. Once the nanopore or nanoslit is opened, the monitored ionic current reaches a predefined current jump ratio, defined as the current ratio after the pore opening to the background current before the pore opening. Unlike previous fabrication methods for extremely small nanopores and nanoslits, a fast-stop system is employed here to minimize over-etching once the pore-opening event is detected. Upon detecting the pore-opening event, the connected computer automatically triggers the fast-stop

system. Simultaneously, the water pump is activated at a flow rate of ~60 mL/min to extract ~0.2 mL of the etching solution from the chamber. This precise and automated control mechanism significantly reduces over-etching and enables the fabrication of nanopores and nanoslits with accurately defined dimensions, improving the overall reproducibility and precision of the fabrication process.

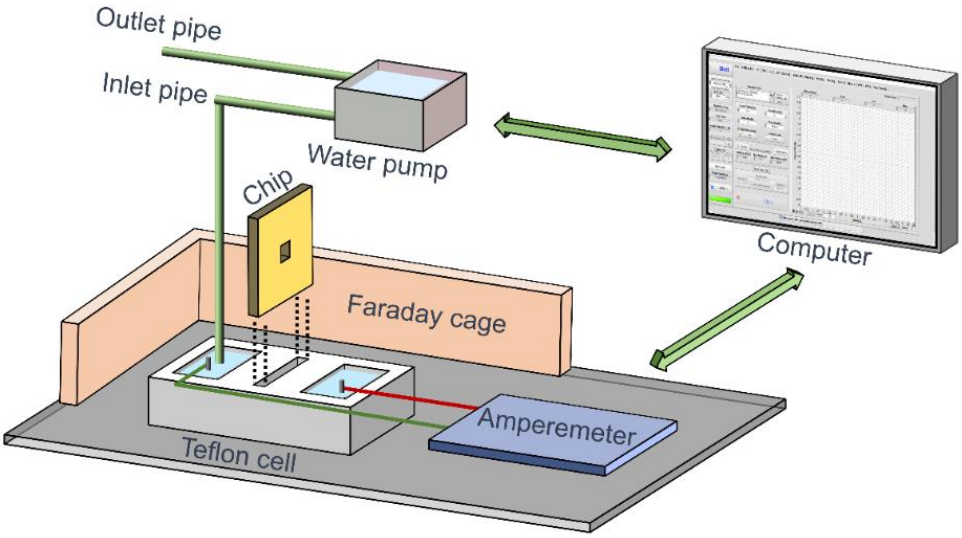

Figure 3.16 Schematic illustration of the fast-stop highly sensitive current-monitored etching system.

3.4.3. CHARACTERISTICS OF THE OBTAINED RESULT

Figure 3.17a shows a photograph of the wafer (with its front side), which contains 88 chips of size 9 × 9 mm, as shown in the inset image. Here, we use three kinds of mask patterns to prepare different nanostructures, as described in Table 3.1. Figure 3.17b shows a scanning electron microscope micrograph of a pyramid pit, which is obtained after the first step of wet etching in a chip with an individual nanopore. Rounded corners in the hard-mask layer are observed. Figure 3.17c exhibits a cross-sectional SEM image of a pyramid pit array, showing good coincidence, and the morphology of the pits conforms to anisotropic etching theory. In fact, considerable geometric diversity is observed after careful measurements. After the second step of the TSWE method, on the backside of the chip, a larger wet etching window than that on the front side is opened. The bottom size of the window is 87.7 × 89.9 μm^2, and this area contains an array or individual pre-etched pyramidal pits on the other side of the chip. Finally, Figure 3.17e shows a cross-sectional SEM image of an individual nanopore with a size of 15 nm. The pyramidal structure with an angle of 54.7° is preserved. The anisotropic wet etching results in undercutting under the hard mask layer, even though the etching rate ratio of the (111) crystal plane to (100) is as high as 1/50 at room temperature with 33% wt KOH.

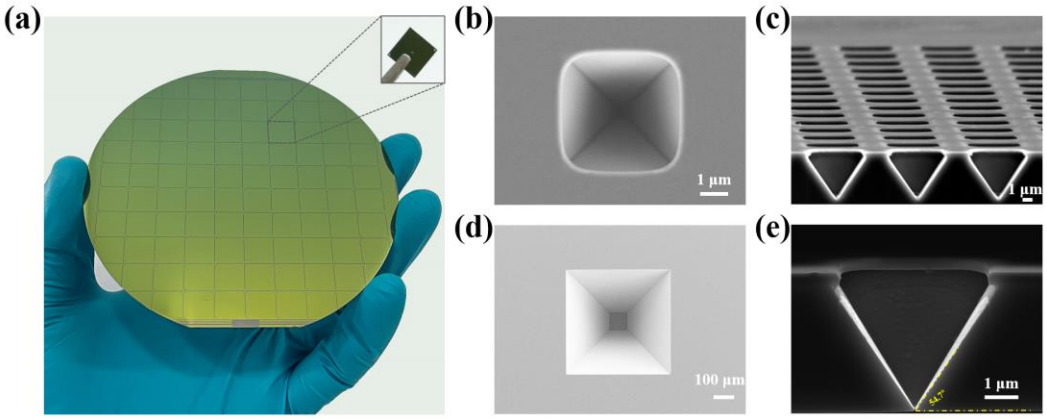

Figure 3.17 a) Photograph of a wafer after the first step b) SEM micrograph of a pyramid pit c) Cross-sectional SEM image of a pyramid pit array d) SEM micrograph of the back etching window e) Cross-sectional SEM image of an individual nanopore with a size of 15 nm.

Table 3.1 Three types of front-side mask patterns

Mask Type	Number (in one chip)	Size
Nanoslit Array	16*16	4 × 4.5 µm
Nanopore Array	16*16	4 × 4 µm
Individual Nanopore	1	4 × 4 µm

Controlling over-etching is always a major challenge in fabricating nanopores with extremely small sizes. Improving the monitoring sensitivity of the pore-opening event and utilizing a fast-stop system can effectively reduce over-etching and guarantee a small size. During the experiment, a large zero-bias current spontaneously flows through the silicon chip as soon as the chip is brought into contact with the two electrolytes (KCl and KOH solution). This is due to electrons that are generated at the interface between Si and the KOH solution during the etching process. By applying a 0.8 V bias voltage between the two Ag/AgCl electrodes, the electrochemical potential difference at the KCl/Si interface and the KOH/Si interface is counterbalanced, thereby minimizing the zero-bias current.

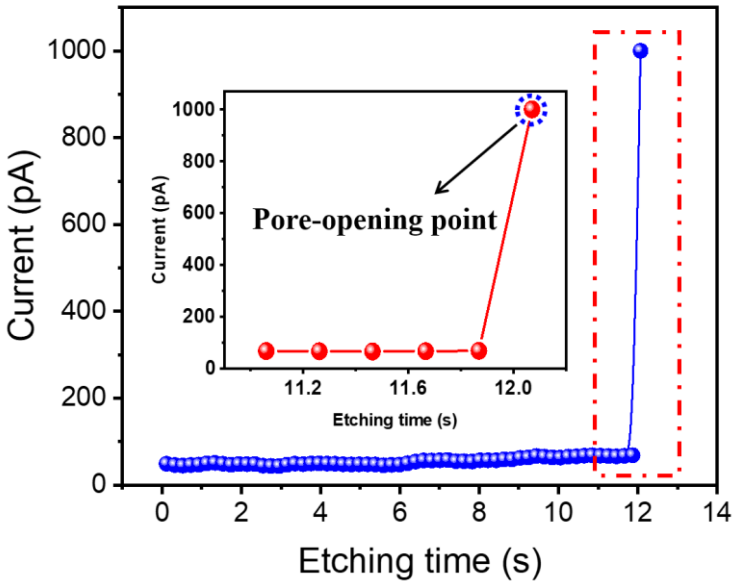

Figure 3.18 Current-time curves recorded during the slit-opening event.

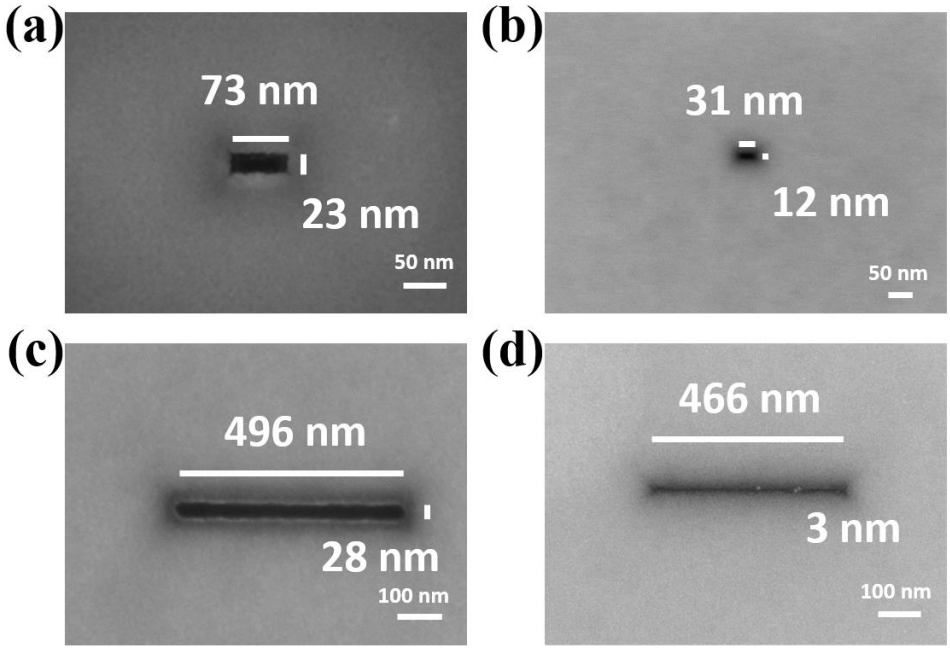

Figure 3.19 SEM micrographs of nanopores and nanoslits fabricated by the TSWE method.

Here, we use the chips of nanopores and nanoslit array masks to fabricate nanopores and nanoslits. Figure 3.18 shows the variation in current based on the fast-stop ionic current-monitored method during the pore-opening event. Before the pore-opening event, the background current is stable and is approximately 50 pA. Once the pore-opening event takes place, the current immediately increases and reaches the set current jump ratio of 20 (current after pore-opening ~1000 pA). This is caused by the exchange of electrolyte solutions on both sides of the chip once the nanopores or nanoslits are

opened. Obviously, the mechanism fails if the current jump ratio setting is small due to possible noise current pulses. On the other hand, a large current jump ratio delays the feedback of the pore-opening event, increasing the over-etching time. Therefore, to controllably fabricate nanopores or nanoslits with specific sizes, setting a precise current jump ratio is an extremely critical step. With the reported fast-stop highly sensitive current-monitored TSWE method, nanopores and nanoslits with nanoscale features are successfully realized. Figure 3.19 shows the SEM images of the obtained nanopores with feature sizes of 23 and 12 nm. It should be noted that for most obtained nanopores, the shape of the as-etched nanopore is a rectangle rather than a square due to the imperfect hard mask and photolithography. Nanoslits with feature sizes of 28 and 3 nm are also obtained. To the best of our knowledge, this is the smallest feature size (3 nm) of a nanoslit obtained by the TSWE method. It is worth noting that the slit has a length of 500 nm, which is controlled by the size of the front pyramid pit. The pictures clearly show the SCS nanopore/slit fabrication capability of the proposed method and that it is possible to manufacture nanopores/slits with extremely small feature sizes.

3.4.4. ANALYSIS OF THE CONTROLLABLE FABRICATION OF NANOPORES

To study the controllability of fabricate individual nanopores with accurate dimensions by the proposed current-monitored TSWE method, the relationship between the size of the nanopore and the current must be understood. According to the previous reports [17,18], this relationship can be described by Equation 3.4:

$$\boldsymbol{i = V\frac{d_{pore}^2}{L_{eff}}\left[(\mu_k + \mu_{Cl})n_{kCl}e + \mu_k\frac{4\sigma}{d_{pore}}\right]} \tag{3.4}$$

Here, $\boldsymbol{d_{pore}}$ is the equivalent length ($\sqrt{\boldsymbol{area}}$) of the nanopore/nanoslit. It should be noted that for most obtained nanopores, the shape of the as-etched nanopore is a rectangle rather than the square, as indicated by the initial lithographic pattern. This is caused by imperfections in the mask and the photolithography process, so here, we use the equivalent length to facilitate the analysis (rectangular nanopore length equivalent to the square nanopore length, $\boldsymbol{ab = d_{pore}^2}$). $\boldsymbol{V}$ is the bias voltage between the two electrodes. $\boldsymbol{n_{kCl}}$ is the number density of potassium or chloride ions, e is the elementary charge, and $\boldsymbol{\mu_k}$ and $\boldsymbol{\mu_{Cl}}$ are the electrophoretic mobilities of potassium and chloride ions, respectively, while $\boldsymbol{\sigma}$ is the surface charge density. The first term in Equation 3.4 represents the current contributed by the bulk conductance, and the surface charge conductance contribution to the current in the nanopore is represented by the second term. We can use it to analyse the relationship between nanopore sizes and the current of two nanopores as follows:

$$\frac{\boldsymbol{i_{exp}}}{\boldsymbol{i_{ref}}} = \frac{\boldsymbol{V\frac{d_{pore_{exp}}^2}{L_{eff}}\left[(\mu_k+\mu_{Cl})n_{kCl}e+\mu_k\frac{4\sigma}{d_{pore_{exp}}}\right]}}{\boldsymbol{V\frac{d_{pore_{ref}}^2}{L_{eff}}\left[(\mu_k+\mu_{Cl})n_{kCl}e+\mu_k\frac{4\sigma}{d_{pore_{ref}}}\right]}} \tag{3.5}$$

Here, i_{exp} and i_{ref} represent the current of an expected nanopore and a reference nanopore, respectively. To simplify Equation 3.5, we measure the ionic current through a nanopore (~18 nm) for different KCl electrolyte concentrations. In the high concentration region (Debye length ≤ nanopore diameter), the ionic current is linearly dependent on the electrolyte concentration, which is indicative of bulk behaviors and properties, as shown in Fig. 3.20. However, as the concentration decreases, the current deviates from the bulk properties near 10^{-3} M and saturates to yield another slope, which corresponds to a surface charge-governed region (<10^{-3} M). The inset images schematically depict the formation of electrical double layers (red color region) consisting of counterions that screen the surface charge. At low concentrations, a long-range screening region allows the nanopores to be dominantly filled with counterions by overlapping the double layer, which causes the saturation of the ionic current. It could be demonstrated that for the high-concentration (1 M) KCl solution, the current contributed by the bulk conductance dominates, which means that the first term in Equation 3.4 dominates the current [19]. Thus, Equation 3.5 can be simplified as follows:

$$\frac{i_{exp}}{i_{ref}} = \frac{V\frac{d^2_{pore_{exp}}}{L_{eff}}[(\mu_k+\mu_{Cl})n_{KCl}e]}{V\frac{d^2_{pore_{ref}}}{L_{eff}}[(\mu_k+\mu_{Cl})n_{KCl}e]} = \frac{d^2_{pore_{exp}}}{d^2_{pore_{ref}}} = \frac{A_{exp}}{A_{ref}} \tag{3.6}$$

Here, A is the area of the nanopore, and d_{pore} is the equivalent length ($\sqrt{A}$) of the nanopore/nanoslit**.** According to Equation (3.6), once a nanopore with a specific area and the corresponding current are defined, then an appropriate current jump ratio can be set according to the current to obtain expected nanopores with a specific area to achieve the controllable preparation of nanopores. Consequently, we set different current jump ratios and obtain different nanopores with equivalent lengths.

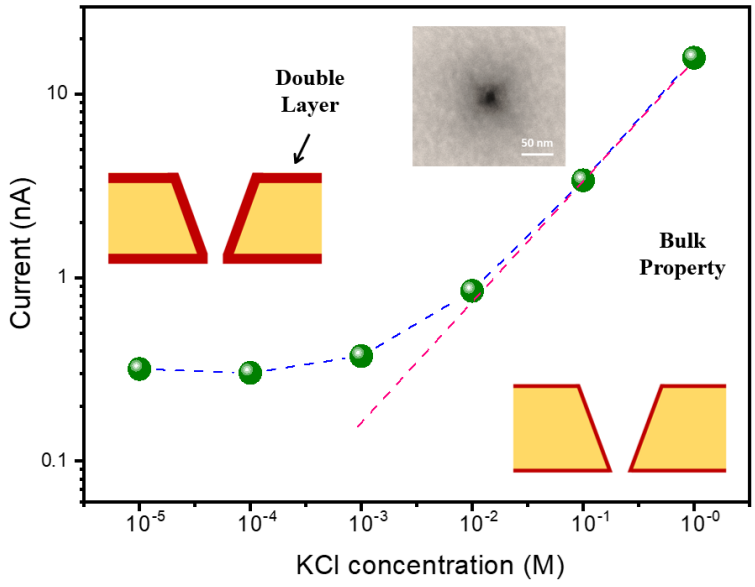

Figure 3.20 Relationship between the ionic current and KCl electrolyte concentration.

From Equation 3.6, it appears that the current of two different nanopores is proportional to the area. Here, we use an individual nanopore (obtained under the same experimental conditions) of a known area and corresponding current (area of 846 nm^2 and current of 2100 pA) as a reference. By setting the current jump ratio to 5, 10, 20, 40 and 80 (background current is approximately 50 pA), individual nanopores with equivalent lengths ($\sqrt{\boldsymbol{ab}}$) of 11, 15, 28, 35 and 44 nm are obtained, and the related ionic currents are also recorded, as shown in Fig. 3.21.

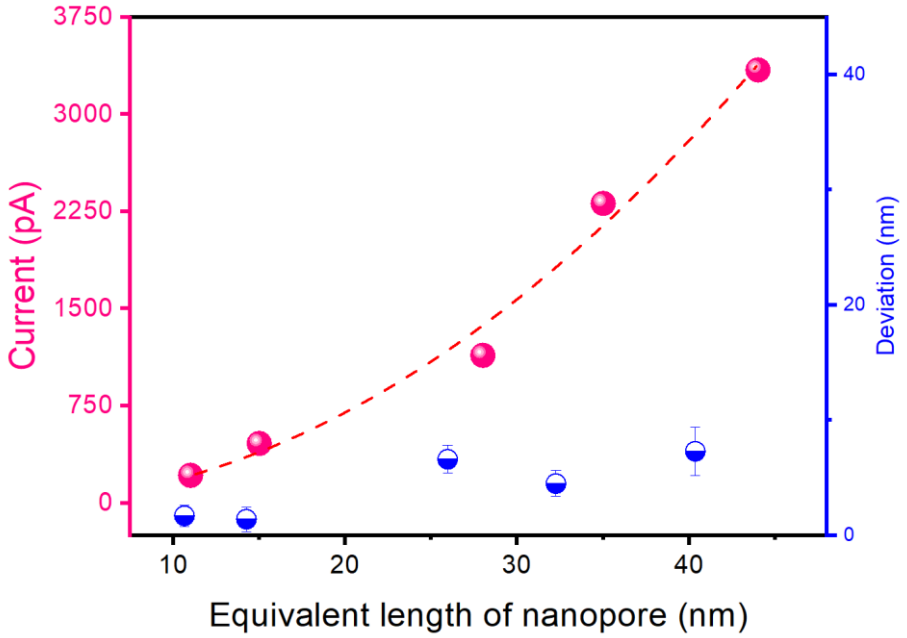

Figure 3.21 Relationship between the size of individual nanopores and the ionic current and the deviation between the equivalent length of the obtained nanopores and the theoretical value.

The fitting curve demonstrates that the relationship between the equivalent length of the nanopores and the current follows Equation 3.6, where the fitting equation is $y = 1.74 * x^2$ and the fitting R-squared value is 0.99. Then, we use the obtained five currents shown in Fig. 3.20 to calculate the corresponding theoretical length of the five nanopores. The theoretical equivalent lengths of the five nanopores are 9.3, 13.6, 21.4, 30.5 and 36.7 nm, and the deviations between the obtained and theoretical lengths are 1.7, 1.4, 6.6, 4.5, and 7.3 nm, respectively, as shown in Fig. 3.21. The actual length of all the obtained nanopores is larger than the theoretical value because there is still less than 0.2 s of over-etching time after triggering the fast-stop system, which pumps out the etching solution to stop the reaction. In addition, we find that the error increases as the length of the nanopore increases. Different from the anisotropic etching properties before pore opening, in which the etching is mainly dominated by the (100) plane, the (100), (110) and (111) planes apparently contribute to the expansion of the nanopore

after pore opening with an etching rate of approximately 3 nm/s. In fact, more planes, such as (210), (211), (310) and (311), are also simultaneously etched after pore opening, resulting in an acceleration of the expansion of the nanopore area. Therefore, a longer over-etching time causes a more significant error. It is predictable that when the jump ratio is as small as 1, the corresponding current of an expected nanopore is only approximately 50 pA. According to the above theory, we can controllably obtain an individual nanopore with an area of approximately 20.1 nm^2, with an equivalent length of only 4.5 nm. While maintaining the area under the same value, the shape (length-width ratio) of the nanopore can be easily tuned by changing the layout of the wet etching mask. If the background current can be further reduced, the size of the controlled nanopore can be further reduced. Here, we demonstrated that the proposed TSWE method has the potential to fabricate extremely small dimensions, which can be adjusted by tuning the aspect ratio of the mask to produce nanopores with extremely small feature sizes. As a conclusion, with the well-controlled experimental procedure described in this study, the accuracy of fabrication was improved effectively, and extremely small nanoslits (down to 3 nm) were obtained. According to the relationship between the ionic current and the size of nanopores, different current jump ratios were selected to produce nanopores with a specific size. Compared with the theoretical size, the smallest deviation was 1.4 nm, which indicates that this method is an effective method for the controllable fabrication of nanopores/nanoslits with specific sizes. In addition, we believe that the proposed method can be further used to controllably fabricate individual nanopores with an equivalent size of approximately 4.5 nm and is expected to allow the preparation of nanopores of smaller size through the reduction of the zero-bias current.

3.4.5. NANO-MASK LITHOGRAPHY BASED ON SILICON NANOPORES

Nano-mask lithography is a crucial nanofabrication technique widely employed in the semiconductor industry, photonics, and material science. It enables the patterning of nanoscale features on various substrates by using a mask to expose or shield areas during etching or deposition processes selectively. This method has been pivotal in advancing nanotechnology, providing a scalable and cost-effective approach to fabricating high-resolution nanostructures [20].The concept of lithography dates back to the early days of semiconductor processing, with traditional photolithography techniques instrumental in microelectronics manufacturing. However, as the demand for smaller feature sizes increased, the limitations of photolithography, primarily due to diffraction limits, became evident. To address these challenges, nano-mask lithography emerged as a viable alternative, leveraging masks with nanoscale features to achieve patterns beyond the resolution of optical lithography.

Nano-mask lithography involves the use of a nano-patterned mask to define precise features on a target substrate. These masks are often fabricated using electron beam lithography (EBL), focused ion beam, or advanced self-assembly methods. The process typically combines techniques such as anisotropic etching, atomic layer deposition, and

reactive ion etching (RIE) to transfer the patterns onto the underlying materials with high fidelity. Nano-mask lithography is particularly advantageous for its ability to achieve High resolution, ensure reproducibility, and enable versatility. Despite its potential, nano-mask lithography faces several challenges including mask fabrication and durability. For mask fabrication, the fabrication of high-quality nano-masks is time-consuming and resource-intensive, particularly for complex or customized designs. For durability, nano-masks, particularly those made from soft materials, may degrade during prolonged use, affecting pattern fidelity [21].

Silicon nanopores fabricated via wet etching exhibit significant advantages, including the capability for large-scale and controlled preparation. Additionally, these structures possess exceptional physical and chemical stability, attributed to the inherent semiconductor properties of silicon. Furthermore, silicon nanopores can be seamlessly integrated with semiconductor processing and MEMS technology, enabling the customization of nanopore-based masks to cater to a diverse range of applications and requirements. Therefore, silicon nanopore/slit has emerged as one of the most promising candidates for nano-mask lithography.

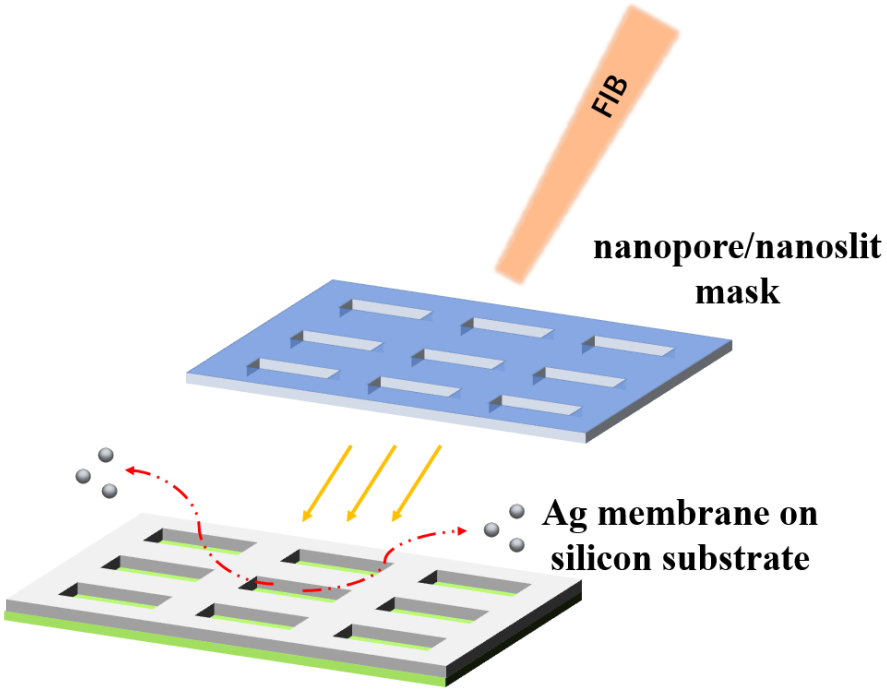

Figure 3.22 Illustration of nano-mask lithography based on nanopore/nanoslit.

Figure 3.22 illustrates the schematic diagram of lithography using a fabricated nanopore mask. In this process, the nanopore mask is closely adhered to the substrate, which has an aluminum film deposited on its surface. The aluminum film is subsequently etched through the hollow mask using a focused ion beam. Under the action of the FIB, the exposed regions of the aluminum film are gradually etched away, resulting in a pattern that mirrors the structure of the nanopore mask.

Figure 3.23 demonstrates the dynamic changes in the substrate material during the lithography (etching) process, with images captured at intervals of approximately 30 seconds. In these SEM images, the black region corresponds to the nanopore mask, while the rectangular pattern in the center represents the nanopore structure. Through the nanopore mask, the aluminum film deposited on the substrate beneath the mask is clearly visible. Gallium ions were employed as the ion beam source, with an acceleration voltage of 30 eV and a beam current of 100 pA. Due to their large mass and high momentum, gallium ions efficiently etch the aluminum film. The SEM images reveal that the exposed aluminum film is rapidly removed by the ion beam, and the remaining areas are subsequently etched, exposing the underlying substrate material (silicon). The nano-mask exhibits high etching selectivity due to the silicon nitride film deposited on its surface. Once the etching process is complete, the silicon substrate beneath the aluminum film is fully exposed. This nano-mask lithography approach successfully transfers the pattern from the mask onto the substrate with high fidelity.

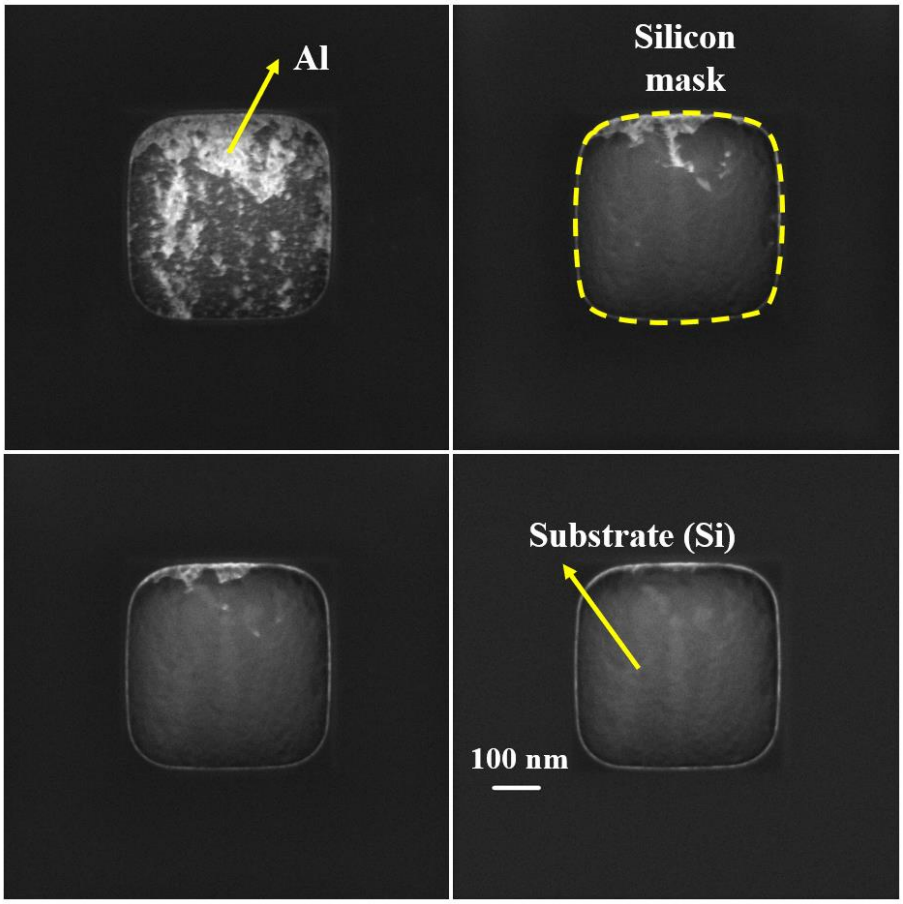

Figure 3.23 Dynamic changes in the Al film during the lithography process.

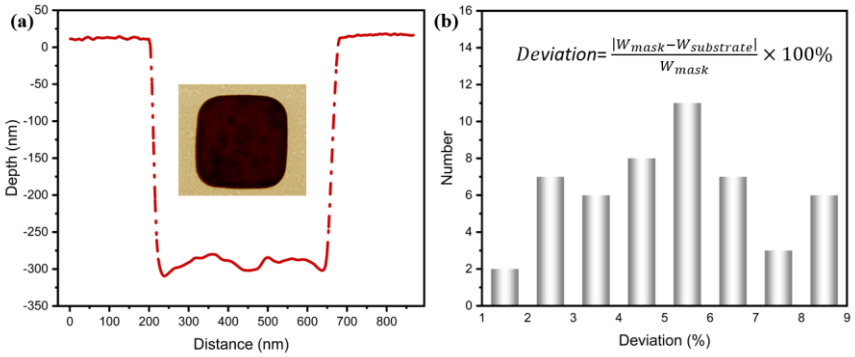

Figure 3.24 a) AFM of obtained patter by nano-mask lithography b) Statistics of nano-mask lithography accuracy

To assess the accuracy of the lithographic patterns, we characterized the resulting etched patterns using atomic force microscopy (AFM). As shown in Fig. 3.24a, the pattern obtained after lithography is consistent with the mask pattern, confirming its reproducibility. To further evaluate the precision of the nano-mask lithography process, we repeated the experiment 50 times using identical masks and lithography parameters. A statistical comparison of the sizes of the etched patterns with the original mask pattern is presented in Fig. 3.24b. The analysis indicates that the deviation of the lithographic patterns is within 10%, with errors following a Gaussian distribution. Most deviations are concentrated between 5% and 6%. These results demonstrate that single-crystal silicon-based solid-state nanopores can be effectively used as nano-masks for focused ion beam lithography, enabling accurate and reproducible pattern transfer. The high fidelity and precision of this technique highlight its potential for applications requiring nanoscale patterning.

3.5. CHAPTER SUMMARY

In this chapter, we proposed and detailed the TSWE method enhanced by ionic current monitoring. By enabling real-time monitoring of the ionic current, this method facilitates precise detection of pore-opening events, thereby significantly reducing the impact of over-etching. To further mitigate over-etching, a slow etching process for the (111) crystal plane and a fast-stop system were combined with the TSWE method, respectively, enabling the successful fabrication of nanoslits with extremely small feature sizes, down to 3 nm.

Additionally, a quantitative relationship between the ionic current of nanopores and their dimensions was established, forming a theoretical basis for the controllable fabrication of nanopores. By leveraging this relationship, a precise and reproducible fabrication approach was developed to achieve nanopores with desired dimensions.

The fabricated nanopores were further utilized as nano-masks in a nano-mask lithography process, effectively transferring patterns onto substrates with high accuracy and fidelity. Experiment results demonstrate the excellent potential of fabricated nanopores in various applications.

REFERENCE

[1] Galenkamp, N.S., Soskine, M., Hermans, J. et al. Direct electrical quantification of glucose and asparagine from bodily fluids using nanopores. Nat Commun, 2018, 9, 4085.

[2] Schmid, S., Stömmer, P., Dietz, H. & Dekker, C. Nanopore electroosmotic trap for the label-free study of single proteins and their conformations. Nat. Nanotechnol, 2021, 16, 1244-1250

[3] Lee, K. et al. Recent progress in solid-state nanopores. Adv. Mater, 2018, 30, 1704680.

[4] Wen, L., Zhang, X., Tian, Y. Quantum-confined superfluid: From nature to artificial. Sci. China Mater. 2018, 61, 1027-1032.

[5] Zhang Y L, Liu Y Q, Han D D, et al. Quantum-confined-superfluidics-enabled moisture actuation based on unilaterally structured graphene oxide papers. Advanced Materials, 2019, 31(32), 1901585.

[6] Ma B, Ma J N, Song P, et al. Quantum-Confined-Superfluidics-Enabled Multiresponsive MXene-Based Actuators. ACS Applied Materials & Interfaces, 2024, 16(12), 15215-15226.

[7] Hong, H., Wei, J., Lei, X. et al. Study on the controllability of the fabrication of single-crystal silicon nanopores/nanoslits with a fast-stop ionic current-monitored TSWE method. Microsyst Nanoeng, 2023, 9, 63.

[8] Deng, Tao et al, Controllable Fabrication of Pyramidal Silicon Nanopore Arrays and Nanoslits for Nanostencil Lithography, Journal of Physical Chemistry C, 2014, 118, 18110-18115.

[9] Shiquan Lin, Xiangyu Chen, and Zhong Lin Wang. Contact Electrification at the Liquid–Solid Interface. Chemical Reviews, 2022, 122 (5), 5209-5232.

[10] Kyeong-Beom Park, Hyung-Jun Kim, Hyun-Mi Kim, Sang A Han, Kang Hyuck Lee, Sang-Woo Kimb and Ki-Bum Kim. Noise and sensitivity characteristics of solid-state nanopores with a boron nitride 2-D membrane on a pyrex substrate. Nanoscale, 2016,8, 5755-5763.

[11] Jeffrey D. Uram, Kevin Ke, and Michael Mayer. Noise and Bandwidth of Current Recordings from Submicrometer Pores and Nanopores. ACS Nano, 2008, 2 (5), 857-872.

[12] V Dimitrov, U Mirsaidov, D Wang, T Sorsch, W Mansfield, J Miner, F Klemens, R Cirelli, S Yemenicioglu and G Timp. Nanopores in solid-state membranes engineered for single molecule detection. Nanotechnology, 2010, 21, 065502.

[13] Shihao Su, Xun Guo, Yanjun Fu, Yanbo Xie, Xinwei Wang and Jianming Xue. Origin of nonequilibrium 1/f noise in solid-state nanopores. Nanoscale, 2020,12, 8975-8981.

[14] H. Hong, L. Ye, K. Li, P. M. Sarro, G. Zhang and Z. Liu, Fabrication of Nanoslits with (111) Etching TSWE Method, 2021 IEEE 16th International Conference on Nano/Micro Engineered and Molecular Systems (IEEE NEMS), Xiamen, China, 2021.

[15] Z. Siwy, D. Dobrev, R. Neumann, C. Trautmann, K. Voss. Electro-responsive asymmetric nanopores in polyimide with stable ion-current signal. Appl. Phys.A, 2003, 76, 781-785.
[16] S. R. Park, P. Hongbo, S. Xinsheng, L. S. Xinsheng. Fabrication of Nanopores in Silicon Chips Using Feedback Chemical Etching. Small, 2007, 3, 116-119.
[17] S. S. Zeng, C. Y. Wen, P. Solomon, S. L. Zhang, Z. Zhang. Rectification of protein translocation in truncated pyramidal nanopores. Nat. Nanotechnol, 2019, 14, 1056–1062.
[18] Ralph. M. M. Smeets, Ulrich. F. Keyser, Diego. Krapf, Meng-Yue. Wu, Nynke. H. Dekker, Cees Dekker. Salt Dependence of Ion Transport and DNA Translocation through Solid-State Nanopores. Nano Lett, 2006, 6, 89-95.
[19] Sung-Wook N, Michael J. R Ki-Bum K, Stephen M. R. Ionic Field Effect Transistors with Sub-10 nm Multiple Nanopores. Nano Letters, 2009, 9, 2044-2048.
[20] T. Deng, Y. F. Wang, Q. Chen, H. J. Chen, Z. W. Liu. Massive fabrication of silicon nanopore arrays with tunable shapes. Applied Surface science, 2016, 390, 681-688.
[21] Byron D. Gates, Qiaobing Xu, Michael Stewart, Declan Ryan, C. Grant Willson, and George M. Whitesides. New Approaches to Nanofabrication: Molding, Printing, and Other Techniques. Chemical Reviews, 2005, 105 (4), 1171-1196.

4

CONTROLLABLE FABRICATION OF SILICON NANOPORE USING AN ELECTROCHEMICAL PASSIVATION ETCH-STOP STRATEGY

4.1. INTRODUCTION

4.1.1. BACKGROUND

Solid-state nanopore technology has emerged as an efficient single-molecule-based analytical tool for the separation and analysis of nanoparticles [1,2]. Among the available materials, silicon-based nanopores and nanoslits have garnered special attention due to their advantageous geometric and material properties, including short channel lengths, ease of surface modification, and seamless compatibility with semiconductor technology [3]. The three-step wet etching method has demonstrated great potential in the fabrication of silicon nanopores. However, challenges in achieving precise control over the silicon etching process and realizing an effective etch-stop remain significant bottlenecks for the scalable and controllable fabrication of silicon nanopores.

To address these limitations, researchers have developed various approaches. For instance, Shuang et al. utilized the anisotropic etching characteristics of the (111) crystal plane to achieve better control over nanopore size, successfully fabricating sub-5 nm nanopores in ultrathin single-crystal silicon membranes [4]. Similarly, Yang et al. employed photoinhibition-assisted KOH etching to reduce etching rates, enabling greater precision in silicon etching [5]. Additional strategies, such as manual or automated separation of the silicon chip and etchant [6,7], and resist- or photovoltaic electrochemical suppression [8], have also been explored to achieve rapid etch-stop. Despite these advancements, there remains a pressing need for scalable, semiconductor-compatible methods that can precisely control both silicon etching and etch-stop processes. Such methods are essential for advancing solid-state nanopore technology and expanding its applications across various fields.

4.1.2. OBJECTIVE

It has been evidenced that heavy doping and applied electrochemical passivation potential are used to prepare thin silicon film by reducing the silicon etching rate [9,10]. In this work, we address these challenges by improving the controllability of silicon etching through heavy boron doping, combined with electrochemical passivation etching techniques to precisely regulate the etching process and further achieve an etch-stop. Both heavy boron doping and electrochemical passivation etching leverage the unique semiconductor properties of silicon and are fully compatible with semiconductor processing and MEMS technology. By integrating these approaches with the TSWE method, we aim to achieve the controllable fabrication of nanopores with extremely small feature sizes.

4.2. EFFECT OF BORON DOPING ON SILICON ETCHING

4.2.1. PREPARATION OF SAMPLES WITH DISTINCT BORON CONCENTRATION

A 4-inch silicon (100) wafer with a resistivity of 1-10 Ω·cm was selected as the substrate for preparing experimental samples with varying boron concentrations. The silicon wafer was first cleaned using a standard HNO_3-based cleaning process to remove surface contaminants. A silicon oxide barrier layer with a thickness of approximately 20 nm was grown on the silicon surface through thermal oxidation to minimize physical damage during ion implantation. Ion implantation was then performed to achieve different boron doping levels in the silicon substrate, with implantation parameters optimized using SRIM simulations to precisely control the doping concentration and depth distribution. Following ion implantation, high-temperature rapid thermal annealing (RTA) was conducted at 1000° C for 15 seconds to repair lattice defects and dislocations in the silicon crystal caused by implantation and to activate the implanted boron atoms by incorporating them into lattice positions, enhancing electrical conductivity. Finally, the boron concentration in the prepared samples was characterized using Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS), providing high-resolution depth profiling to verify the doping accuracy and confirm the intended boron concentration distributions.

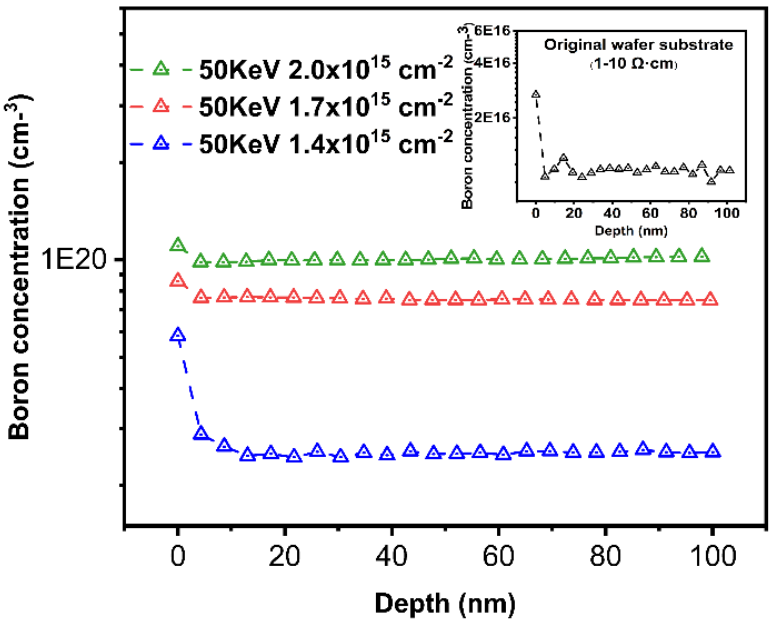

Figure 4.1 Boron concentration of different samples produced with distinct boron implantation parameters.

Figure 4.1 illustrates the boron concentration profiles of various prepared silicon samples as characterized by TOF-SIMS. The samples, prepared with boron implantation densities of 2.0×10^{15}, 1.7×10^{15}, and 1.4×10^{15} cm^{-2} at an implantation energy of 50 keV, exhibited boron concentrations of 1.0×10^{20}, 7.5×10^{19}, and 2.5×10^{19}

cm^{-3}, respectively. In comparison, the boron concentration of the original silicon substrate (resistivity: 1-10 Ω·cm) was measured to be 1.0×10^{16} cm^{-3}. In the ion implantation process, the implantation energy determines the effective implantation depth, while the implantation density governs the ion concentration within the targeted region.

4.2.2. SILICON ETCHING RATE MEASUREMENT AND DISCUSSION

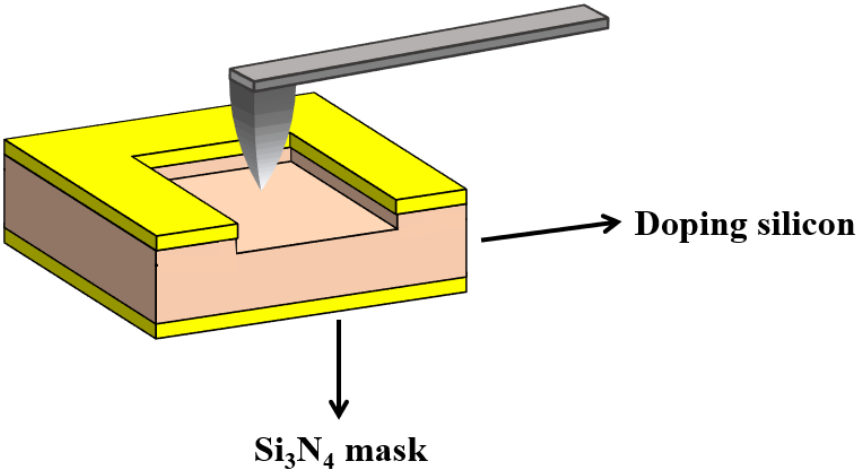

Figure 4.2 Illustration of silicon etching rate measurement.

To measure the etching rate of boron-doped p-type silicon in a KOH aqueous solution, the experimental setup and procedure are illustrated in Fig. 4.2. First, a 100 nm silicon nitride layer was deposited on the silicon wafer by LPCVD to act as an etching mask. Using photolithography, a pattern of etching windows measuring 100 × 100 μm^2 was transferred onto the wafer, and the silicon nitride in the window areas was partially removed by dry etching to expose the underlying silicon. Before proceeding with KOH aqueous solution etching, any natural oxide layer present on the exposed silicon surface was removed using a buffered hydrofluoric acid solution to ensure accuracy. Wet etching was then conducted in the 33 wt% KOH aqueous solution with different temperatures. After the etching process, the depth of the etched silicon was measured using a step profiler to determine the etching rate.

As introduced in chapter 2, the silicon etching rate in the KOH solution starts to decrease at a boron concentration of approximately 2.0×10^{19} cm^{-2}. The Arrhenius plot of the etching rates for prepared samples with distinct boron doping concentrations is shown in Fig. 4.3. The results indicate that for all samples, the etching rate increases with rising temperature. This phenomenon occurs because higher temperatures enhance molecular motion, leading to more frequent and energetic collisions between reactive species. Additionally, an increase in temperature enables a larger fraction of molecules to overcome the activation energy barrier, as described by the Arrhenius equation (eq 2.6), thereby accelerating the reaction rate. However, samples with higher boron

concentrations exhibited significantly lower etching rates. This behavior can be attributed to the following mechanisms.

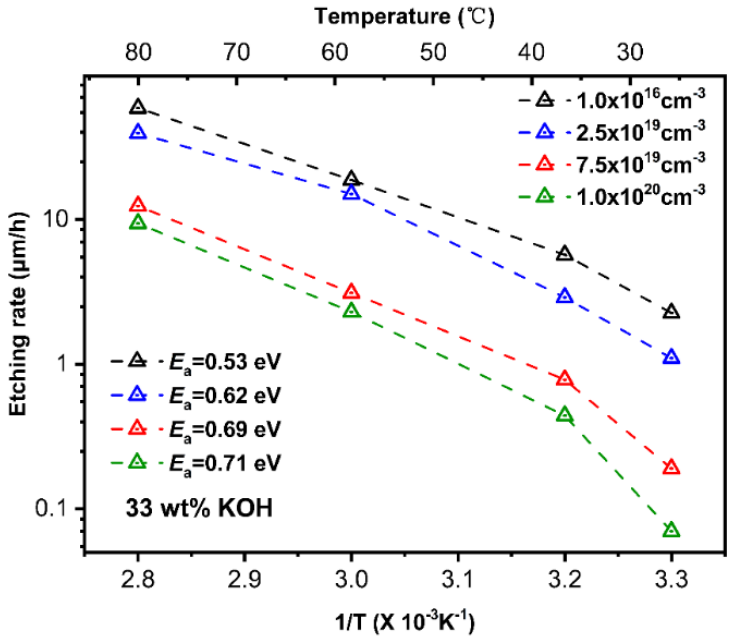

Figure 4.3 Arrhenius diagram of the silicon etching rate for various boron concentrations.

The Fermi level drops into the valence band due to the heavy boron-doped, inducing a sharp shrinkage of the space charge layer. This leads to an equivalent narrowing of the potential well given by the downward bending of the energy bands on the silicon surface. As a result, electrons, generated from an oxidation reaction (eq 2.7), injected into the conduction band cannot be confined and easily tunnel through the SCL into the deeper regions of the silicon. The high hole concentration in the heavy boron-doped silicon promotes electron-hole recombination, thereby depleting the electrons available for subsequent reduction reactions (eq 2.8) and further impeding the silicon etching reaction. Alternatively, the phenomenon can also be explained by a strain model. The density of surface defects increases above the intrinsic surface defect density for the heavy B-doped, facilitating the formation of the passivation that halts the etching reaction. Furthermore, Raley et al. proposed a composite model to explain the relationship between doping concentration and etching rate in heavily boron-doped silicon etched in an EPW solution [11]. According to this model, the etching rate is more closely associated with the hole concentration than the doping concentration itself. The model highlights that redox processes during etching involve the participation of both electrons and holes. The high concentration of holes on the silicon surface leads to the recombination of electrons generated during the oxidation reaction. This recombination depletes the available electrons, slowing down subsequent reduction reactions, and ultimately resulting in a reduced etching rate. Finally, the activation energy (*E*a), as determined from the Arrhenius equation ($R = A\mathrm{e}^{-E_a/KT}$), increases

with the higher boron concentration, indicating the increasing energy required for the etching reaction, as a result, the etching reaction is suppressed. The above analysis provides a comprehensive explanation of the mechanisms by which doping concentration affects the etching rate, from multiple perspectives, including the space charge layer model and strain model. It also validates the effectiveness of using heavy doping to regulate the etching process. In this study, heavy doping not only helps regulate the etching rate but also facilitates the formation of ohmic contacts, enabling efficient potential conduction. This is particularly beneficial for subsequent nanopore fabrication based on the electrochemical potentials.

4.3. CONTROLLABLE FABRICATION OF SILICON NANOPORE USING AN ELECTROCHEMICAL PASSIVATION ETCH-STOP STRATEGY

4.3.1. SILICON ETCHING RATE WITH APPLIED ELECTROCHEMICAL POTENTIALS

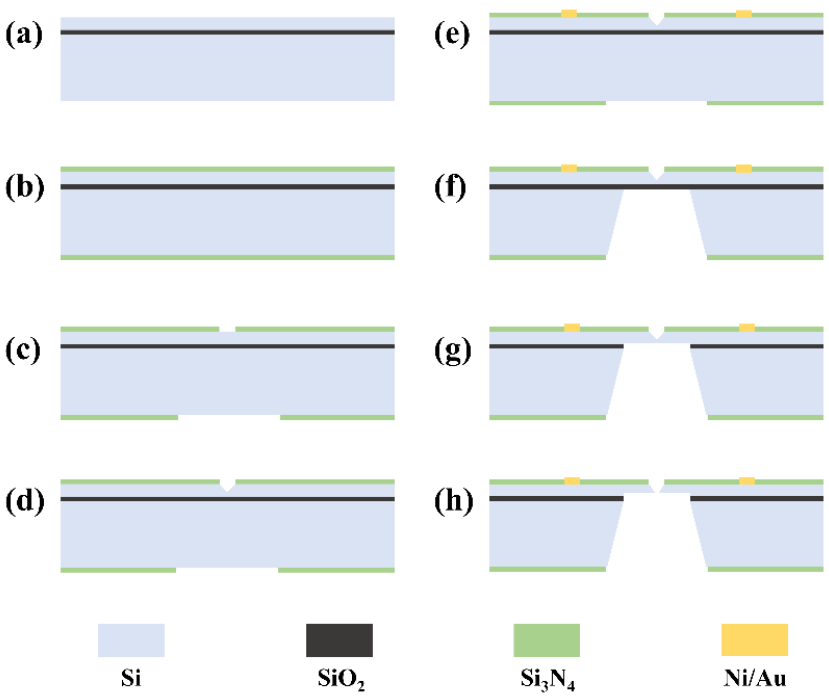

Figure 4.4. Demonstration of the fabrication process of the silicon nanopores using electrochemical passivation etch-stop. a) clean of wafer b) Si_3N_4 mask layers deposition on the SOI wafer c) transfer of patterns by photolithography and removal of mask layers d) formation of pyramid-shaped pit e) Ni/Au electrode deposition on the silicon f) formation of back etching window g) removal of buried oxide layer h) fabrication of nanopores based on electrochemical passivation.

A SOI silicon wafer with a boron concentration of 3.5×10^{19} cm^{-3} was utilized for electrochemical passivation and silicon nanopore fabrication. This sample cannot only facilitate the accurate control of the etching process due to its lower etching rate

compared to lightly boron-doped silicon but also enable an ohmic contact to conduct the electrochemical passivation. Before the etching rate measurement, the fabrication process is briefly demonstrated in Fig 4.4. Figure 4.4 illustrates the fabrication process for silicon nanopores based on the TSWE method. At first, the substrate wafer was cleaned using a standard cleaning process. As shown in Fig. 4.4b, 100 nm Si_3N_4 films were deposited on both sides of the cleaned SOI wafer by low-pressure chemical vapor deposition as a mask layer. Subsequently, double-sided photolithography was used to transfer the etching window patterns onto the wafer. Then inductively coupled plasma was utilized to partially remove masks to structure the etching windows as depicted in Fig. 4.4c. Next, the first anisotropic wet etching was conducted to develop pyramid-shaped pits in the front of the wafer as exhibited in Fig. 4.4d. Then metal electrodes (Ni 10 nm/Au 100 nm) were deposited near the pit as shown in Fig. 4.4e. It's unnecessary to conduct the extra doping process to make sure the ohmic contact since the wafer was heavy dopped. The second wet etching was conducted to build the back-side cavity, and the etching stopped at the buried oxide layer as demonstrated in Fig. 4.4f. The exposed oxide layer was then removed by buffered hydrofluoric acid as shown in Fig. 1g. Finally, before the fabrication process the wafer was divided into many small chips (0.9×0.9 cm^2) to conduct the precise pore-opening experiment, the third wet etching was conducted to open the tip of the pyramid-shaped pit and the nanopores were successfully fabricated.

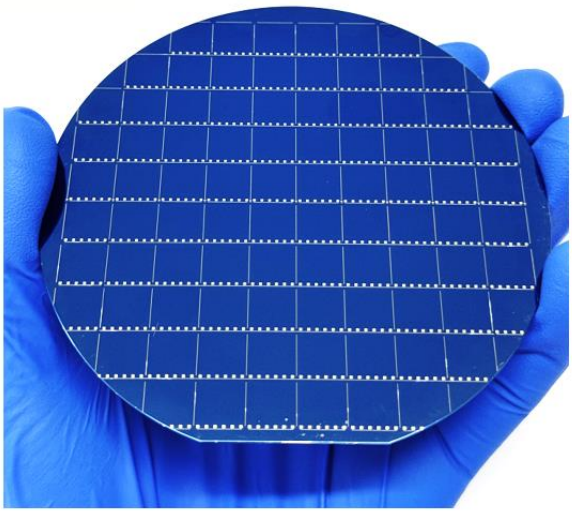

Figure 4.5. Photograph of the silicon wafer during the fabrication process.

Figure 4.5 shows a photograph of the silicon wafer during the fabrication process, which corresponds to Fig. 4.4g. It can be observed that approximately 76 complete chips (excluding chips with broken edges) were contained in the 4-inch wafer, and each chip can be used in fabricating a nanopore with an extremely small size by the proposed method, which proves the high yield of the procedure to fabricate nanopores. It can be predicted that a cost-effective fabrication of nanopores based on MEMS technology can

be realized. Besides, 6 metal electrodes are deposited in each chip to ensure the electrochemical passivation experiment.

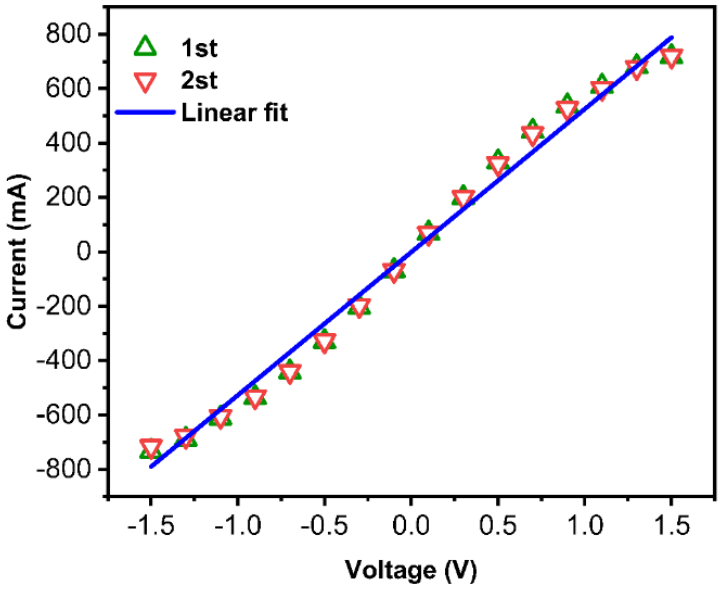

Figure 4.6. Cyclic current-voltage curve between two metal electrodes deposited on silicon chips.

To effectively apply electrochemical potentials to the silicon chip, 6 metal electrodes were deposited on each silicon chip. From the cyclic current-voltage curve between two metal electrodes shown in Fig. 4.6, it can be observed a non-rectified contact with a 1.5 Ω resistance has been realized, which proves the ohmic contact between the metal electrodes and silicon has been developed.

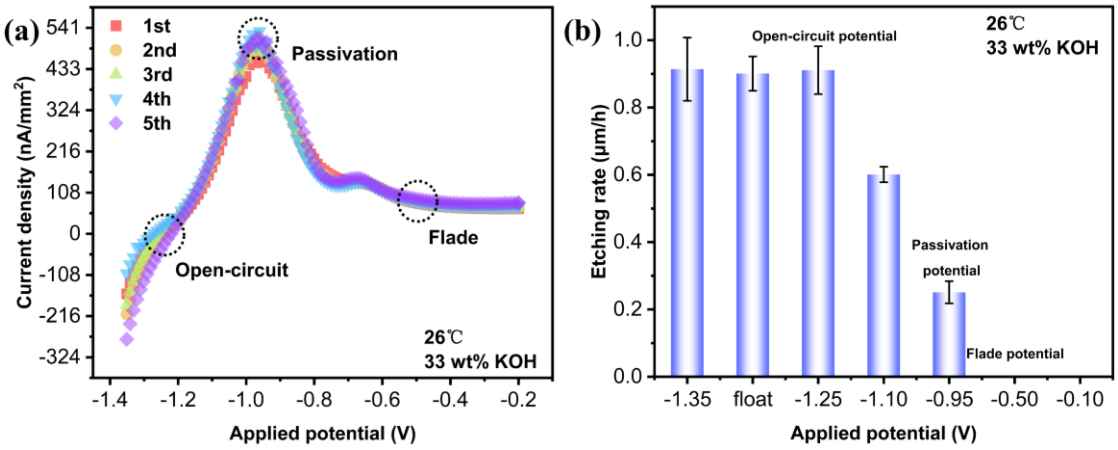

Figure 4.7. Effect of the electrochemical potential on the silicon etching. a) Current-potential curves obtained from linear scan voltammetry during the silicon etching process b) Silicon etching rates regarding to different applied potentials.

The electrochemical potential was applied to the silicon during the etching process to achieve precise regulation of the silicon etching process. Figure 4.7a exhibits the

corresponding current-potential curves obtained from linear scan voltammetry. The measurement starts at -1.35 V and scans positively at a rate of 1 mV/s. The open-circuit , passivation, and Flade potential for this sample were determined to be -1.25, -0.95, and -0.50 V by repeated measurements. As the potential scans positively, the current transitioned from cathodic to anodic at the OCP, where no net charge transfer occurs, resulting in a near-zero current.

Beyond the OCP, the anodic current increased with the potential, driving oxide growth on the silicon surface in contact with the etchant, reducing the silicon etching rate. Further potential increases will facilitate the formation of an oxide layer covering the silicon surface and lead to a sudden current drop at the PP. A stable oxide layer forms at the Flade potential, where the current stabilizes at a minimal but nearly constant value due to the insulating effect of the passivation layer. The established oxide layer provides a practical approach to realize the etch-stop for silicon. Additionally, the formation process of the oxide/passivation layer once the potential beyond the FP is defined as a passivation process. It can be predicted that the silicon etching rate can be regulated by the variation in the oxide growth during the etching process.

To ascertain the effect of different potentials on the silicon etching rate. Figure 4.7b illustrates the silicon etching rates under different applied electrochemical potentials. While the silicon etching rates remained approximately equal (~0.90 μm/h) at potentials of -1.35 and -1.25 V (OCP), as well as in float condition (no applied electrochemical potential), the cathodic current was only observed at -1.35 V. This cathodic current regarding -1.35 V will be served as a basis for determining whether the oxide was being etched off in the subsequent experiment. As the potential further increased, the growth of the oxide was gradually dominant and resulted in a reduction in the silicon etching rate (both at -1.10 V and the PP). It's worth noting that the decreasing silicon etching rate culminated in an etch-stop at Flade potential and the same phenomena can be observed at a more anodic potential (-0.10 V). It can be concluded that when the applied potential exceeds the Flade potential, the etch-stop will invariably remain due to the oxide layer formed during the passivation process.

4.3.2. FABRICATION SYSTEM AND PROCESS

The detailed fabrication process and corresponding chip images are provided in Fig. 4.4 and 4.5, respectively. Figure 4.8 illustrates the fabrication system of silicon nanopores based on electrochemical passivation, which corresponds to Fig. 4.4h. During the final fabrication step, a measuring unit was used to monitor the current across the silicon chip in real-time under a bias voltage of 0.8 V. As silicon etching progressed in the 33 wt% KOH solution at room temperature, the pore-opening event was indicated by a simultaneous increase in ionic current. A second measuring unit, as an electrochemical workstation, was used to apply electrochemical potentials (all potentials are with respect to a Hg/HgO electrode). Silicon chip, platinum electrode, and Hg/HgO electrodes served as the working, counter, and reference electrodes, respectively. A predefined passivation potential was automatically applied to realize an

etch-stop of the silicon etching once the nanopore reached the desired size. It's worth noting that to minimize possible current interference, the two measuring units operated alternately. The switching time between the current measurement and the potential application was less than 30 ms. This setup ensured precise etch-stop and reproducible nanopore fabrication. Figure 4.9 illustrates the fabrication principle of silicon nanopores using the TSWE-based electrochemical passivation method. During the pore-opening process, a measuring unit continuously monitors the ionic current across the silicon chip in real time. Electrodes from the measuring unit are positioned on the front and back sides of the silicon chip, as shown on the left side of Fig. 4.9. Simultaneously, the electrochemical workstation regulates the electrochemical passivation process. In this setup, the counter electrode is connected to the silicon chip, forming a closed circuit where a current is generated upon applying a potential. This applied potential and the resulting current allow precise control over silicon etching and passivation process. Additionally, the reference electrode is also connected to the silicon chip to provide a stable potential reference, ensuring accurate measurement and regulation of the working electrode's potential. Upon detection of a pore-opening event, feedback from the ionic current immediately triggers the electrochemical passivation process. This rapidly induces the formation of a passivation layer (illustrated in red) on the sidewalls, specifically on the (100) and (111) crystal planes of the nanopore, effectively achieving an etch-stop. This efficient etch-stop strategy enables the precise fabrication of silicon nanopores with minimal over-etching, ensuring excellent dimensional control and reproducibility.

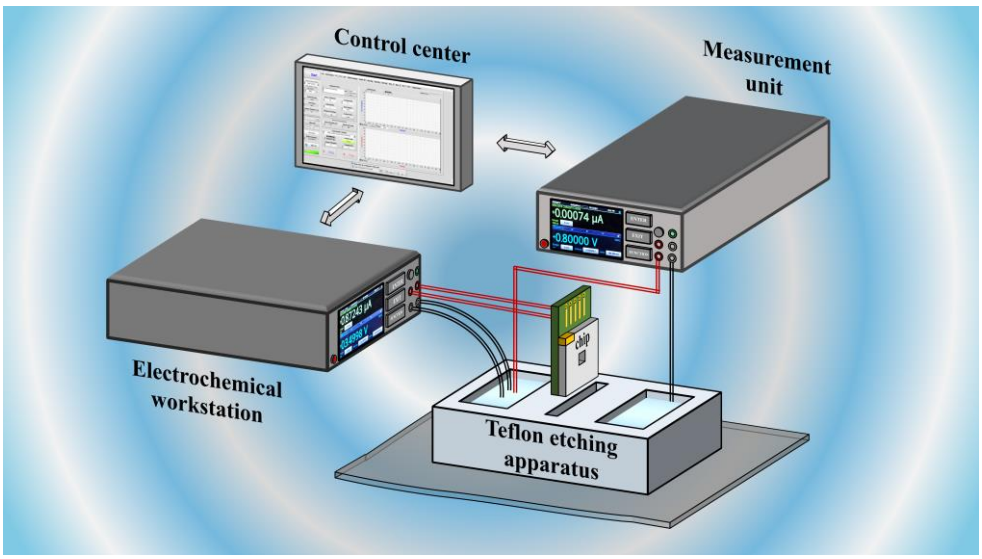

Figure 4.8. Illustration of the fabrication system of silicon nanopores based on the electrochemical passivation.

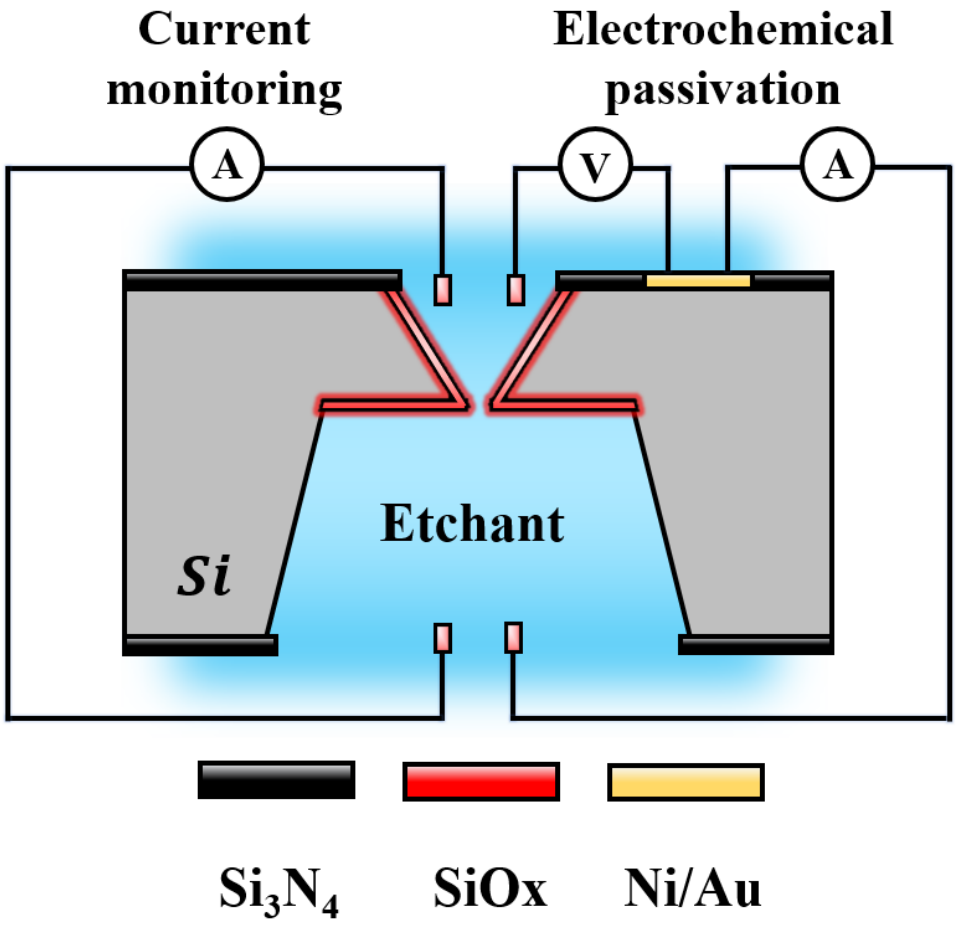

Figure 4.9 Principle of the fabrication of nanopores based on electrochemical passivation.

4.3.3. RESULT AND DISCUSSION

To confirm the nature of the oxide formed during the passivation process, an in-situ characterization of the oxide layer was carried out. Figures 4.10a, b, and c show the cross-sectional TEM images of the oxide layer following 1 h passivation at potentials of 1.5, 2.5, and 3.5 V, respectively. Uniform oxide layers were observed to fully cover the silicon surface, with thicknesses of 2.5, 3.6, and 5.2 nm corresponding to passivation potentials of 1.5, 2.5, and 3.5 V, respectively. The elevated passivation potential notably promoted the formation of a thicker oxide layer. It's worth noting that the slight divergence (less than 2 nm) in oxide thickness caused by 1 V highlights the capability of realizing precise control over the passivation layer thickness, which enables precise regulating of the nanopore size through the oxide layer.

Figure 4.10d, e, and f depict the atomic resolution high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM) image of the formed oxide, along with the corresponding EDS elemental mappings. The two-layer structure visible in Fig. 4.10d aligns with the TEM findings, and the white granule is Pt which

was deposited to cover the formed oxide as a protective layer. The elements of silicon (shown in blue) and oxygen (shown in red) are distributed homogeneously in the lower and upper layers, respectively. It can be evidenced that the oxide formed by electrochemical passivation primarily consists of SiO_x.

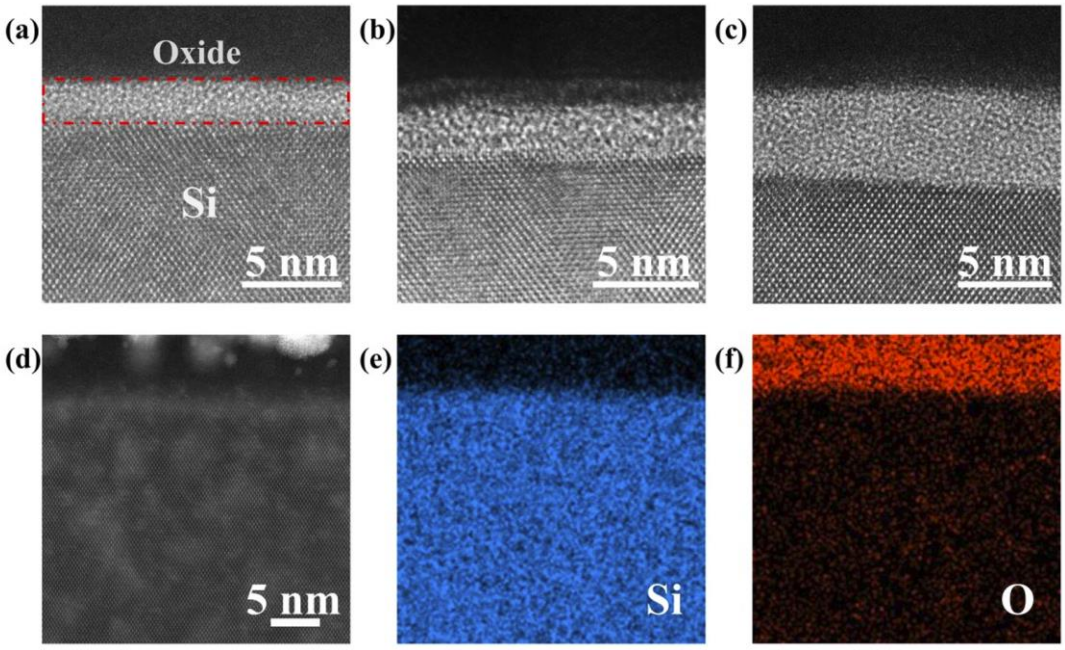

Figure 4.10 Characterization of the oxide layer formed during the passivation process. Cross-sectional TEM image of the formed oxide after 1 h passivation with a potential of a) 1.5 V b) 2.5 V and c) 3.5 V d) STEM images of the formed oxide and corresponding EDS elemental mapping of e) Si and f) O.

Given that silicon oxide exhibits a significantly lower etching rate in KOH solution compared to silicon, even a thin oxide layer effectively delays etching, thereby providing a reliable etch-stop mechanism. Furthermore, atomic force microscopy (AFM) images of oxide layers formed by electrochemical passivation and thermal oxidation was exhibited in Fig. 4.11a and b. The oxide was formed by a 1 h passivation process with a potential of 3.5 V and thermal oxidation, respectively. The roughness of the silicon oxide surface is 2.32 and 0.217 nm. It can be predicted that the oxide formed through electrochemical passivation has a less dense structure. This observation indicates that the chemical stability of the passivated oxide layer is inferior to that of thermally grown oxide.

In-situ characterization of the formed oxide confirmed that a stronger passivation potential leads to a thicker oxide layer. To elucidate the relationship between passivation and oxide formation, etch-back measurements were performed. Figures 4.12, 13, and 14 illustrate the scanning current-potential curves (red lines) during passivation from -1.4 V to final potentials of 1.5, 2.5, and 3.5 V (scanning rate: 1 mV/s) alongside the corresponding etch-back time-current curves (green lines). The current-potential profiles exhibit similar trends of the current, with characteristic potentials

(OCP, PP, and FP) aligning with those in Fig. 4.7. Notably, a sharp current increase occurs beyond ~2.1 V. It can be speculated that after the establishment of a certain oxide layer thickness, the growth rate of the oxide no longer increases proportionally with the gradually increasing potential due to the insulating effect of the existing oxide layer. This leads to only a marginal increase in oxide thickness even as the potential continues to rise. Eventually, the continuously increasing potential may exceed the dielectric strength of the oxide, resulting in local dielectric breakdown and a sudden rise in leakage current, without a corresponding increase in oxide thickness.

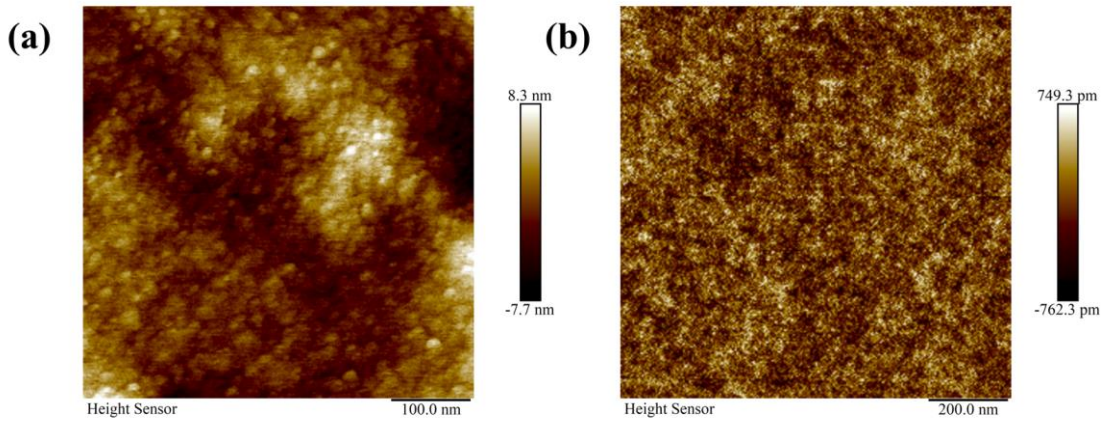

Figure 4.11 AFM image of the silicon oxide form by a) passivation and b) thermal oxidation.

Following the passivation process, an etch-back measurement was conducted, that is, a fixed potential of -1.35 V was immediately applied to etch the oxide formed during the former passivation process. Due to the insulation of the formed oxide layer, a consistently small current during the initial stage of etch-back measurement can be observed. The slow etching of the oxide continues until the depletion, at which point the current begins to increase towards the cathode. This point, where the current changed, was identified as a symbol of the start of silicon etching, and the cathodic current regarding -1.35 V also ascertained the switch from oxide etching to silicon etching. The time consumed to reach this turning point represented the duration of the oxide etching process, also called etch-back time. The etch-back time of the oxide layer which was established by the passivation process at the potential of 1.5 V, 2.5 V, and 3.5 V, was found to be 2317, 3541, and 4374 s, respectively. A longer etch-back time can be verified as a consequence of cooperation of higher potential and longer passivation time.

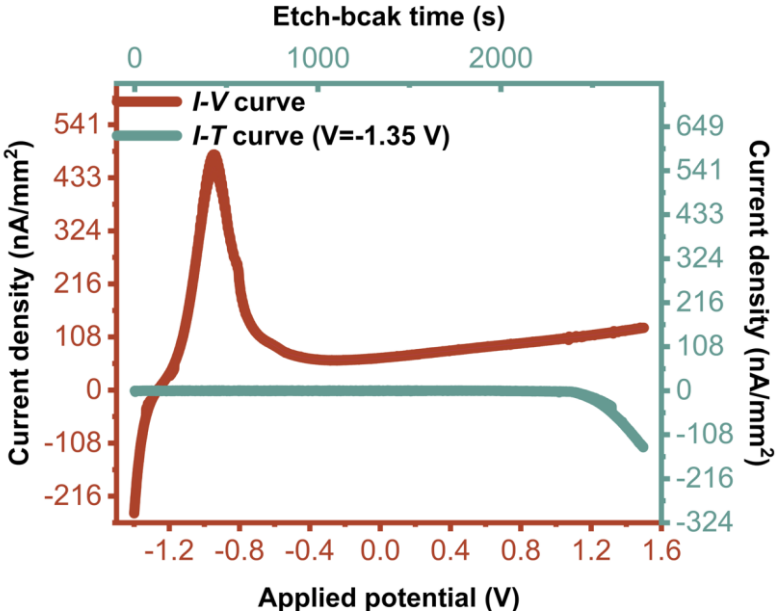

Figure 4.12 Scanning current-voltage curve for passivation process with a final potential of 1.5 V and the corresponding etch-back current-time curve after the passivation.

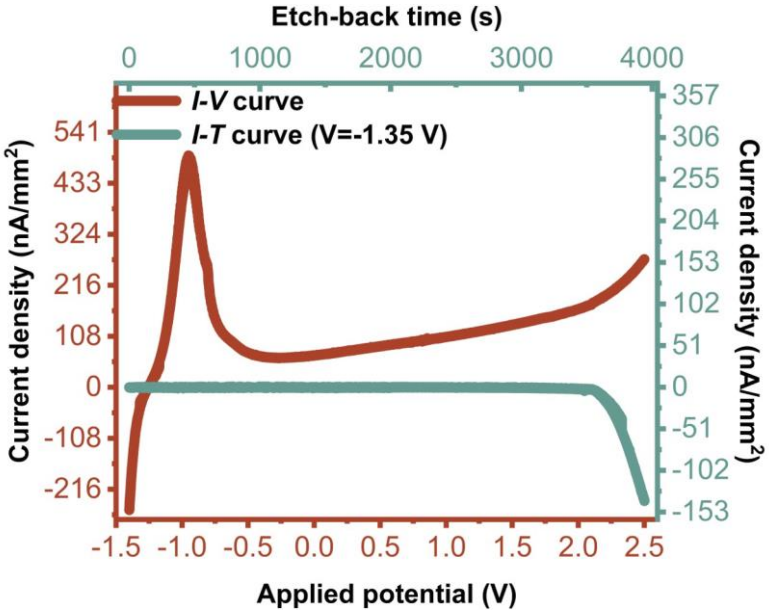

Figure 4.13 Scanning current-voltage curve for passivation process with a final potential of 2.5 V and the corresponding etch-back current-time curve after the passivation.

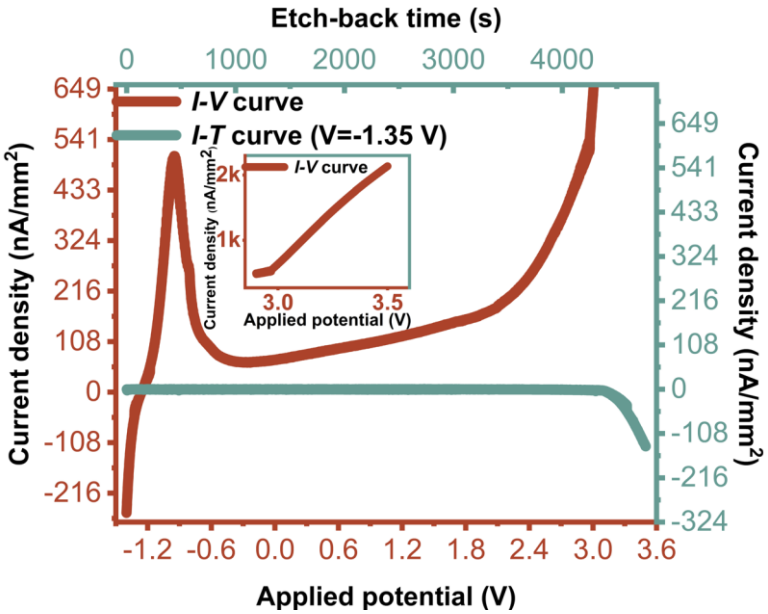

Figure 4.14 Scanning current-voltage curve for passivation process with a final potential of 3.5 V and the corresponding etch-back current-time curve after the passivation.

To compare oxide formation under different passivation modes, etch-back times for oxides formed by scanning-potential and fixed-potential models were evaluated, as presented in Fig. 4.15. For the scanning-potential model, scanning starts at -1.35 V while for the fixing-potential model the passivation times are all 1 hour. It can be concluded that the etch-back time increased with the increasing potential, which means that the higher passivation potential contributed to a thicker oxide layer. While both modes demonstrate increased oxide thickness with higher potentials, for potential with the same value, the fixed-potential model results in longer etch-back time due to prolonged exposure to high potentials. However, this difference in the etch-back time degenerates with increasing potential, as the scanning mode extends the passivation duration, reducing the disparity.

For subsequent investigations aimed at realizing the etch-stop in a short time to improve nanopore fabrication controllability, the fixed-potential model was adopted. Based on the measured etch-back time and the thickness of the oxide characterized by TEM, the etching rates for the oxide formed by different potentials are calculated and shown in Fig. 4.16. No significant difference was observed in the etching rate of the formed oxide, indicating oxides formed at different potentials have the same properties. It's worth noting that the average etching rate is about 0.5 Å/min, which is higher than the oxide formed by thermal oxidation (~0.1 Å/min). This indirectly leads to the same conclusion as indicated by the AFM images (Fig. 4.11) that the oxide formed by the passivation process possesses a less dense structure than the oxide formed by thermal oxidation, resulting in a higher etching rate. Indeed, as discussed in the previous chapter, the SiOx layer formed through electrochemical passivation exhibits a porous structure. This

porosity makes it more susceptible to etching, resulting in a significantly faster etch rate compared to the denser, thermally grown silicon oxide.

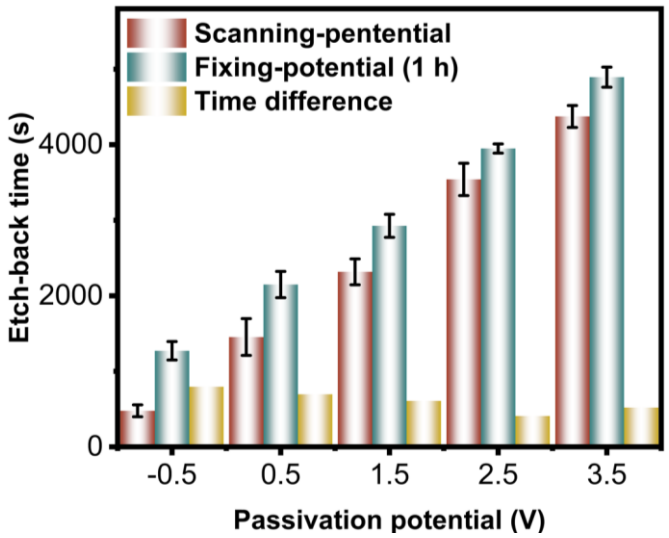

Figure 4.15 Etch-back time of oxide layers formed by scanning-potential and fixing-potential model.

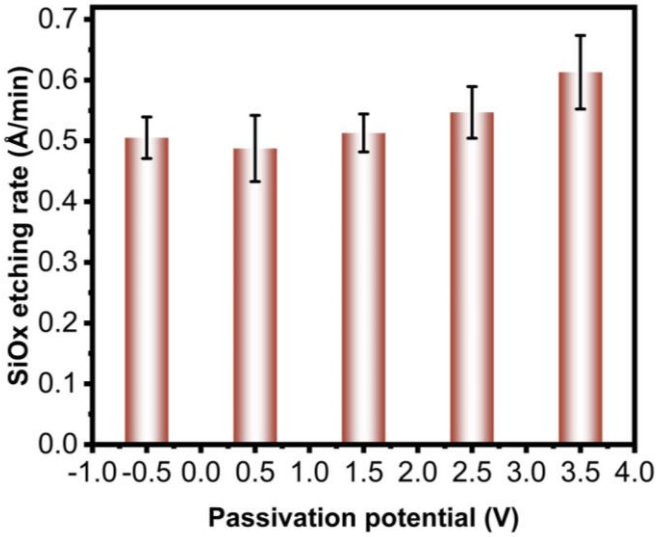

Figure 4.16 Etching rate of SiOx formed by 1 h passivation with different potentials.

The above investigations primarily focus on the influence of passivation potential on oxide formation. Subsequently, the effect of passivation time on oxide growth was examined, as shown in Figure 4.17. It was observed that passivation for just 4 s yielded oxide layers with 61.8%, 73.5%, 77.8%, 84.2%, and 87.3% of the etch-back times corresponding to 1 h passivation at potentials of -0.5, 0.5, 1.5, 2.5, and 3.5 V, respectively. These findings confirm that oxide formation is rapid upon applying a passivation potential, achieving an etch-stop within seconds. As illustrated in Figure 3b, the silicon etching rate without any applied electrochemical potential is approximately 0.9 μm/h, indicating that silicon is theoretically etched by no more than 1 nm during the 4 s d passivation process. This demonstrates that the deviation in nanopore size

caused by over-etching during passivation is negligible, and the etching is effectively stopped immediately upon initiating passivation.

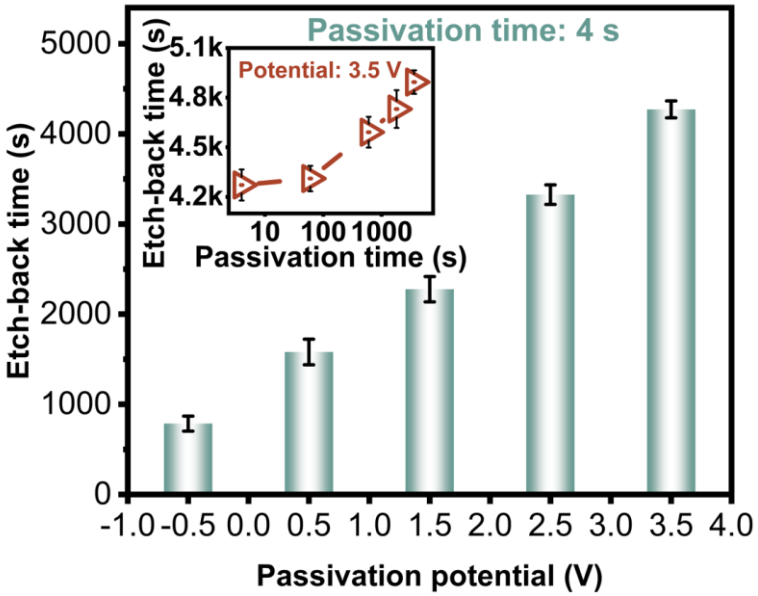

Figure 4.17 Etch-back time of oxide layer formed by passivation process with different potential and time.

Moreover, the inset figure shows the corresponding etch-back times after passivation for different times (4, 60, 600, 1800, and 3600 s) at 3.5 V. Oxides formed by passivation for 4, 60, 600, and 1800 s required 87.3, 88.1, 93.8, and 96.7% of the etch-back time for 1 h passivation, respectively. The results demonstrate that the oxide layer forms rapidly, and the growth rate diminishes over time after the formation of a certain thickness oxide layer. Once an appropriate passivation potential was applied, a protective oxide layer was quickly established, with subsequent growth plateauing.

So far, these findings establish that silicon surfaces can be rapidly passivated during the initial stages of passivation, effectively achieving etch-stop without significant over-etching. This approach leverages silicon's conductive properties to enable precise, controllable etching, paving the way for high-precision nanopore fabrication.

Finally, the controllable fabrication of silicon nanopores was achieved using the TSWE method with the investigated etch-stop strategy. Figure 4.18a shows a representative current-time curve during the pore-opening process. As the silicon chip was progressively thinned by KOH-based wet etching at room temperature, a steady and minor increase in current was observed (green dots), corresponding to the gradual reduction in silicon thickness. Upon the pore-opening, the etchant separated by the silicon chip is connected through the newly formed nanochannel, leading to a pronounced increase in ionic current (red dots) due to the nanopore expansion.

To effectively stop the silicon etching, a predefined passivation potential (0.5 V) was automatically applied by the electrochemical workstation following the pore-opening, initiating the etch-stop process. The current-time curve corresponding to this passivation process is shown in Fig. 4.18b. It's worth noting that the size can be

recognized by the corresponding ionic current as reported in our previous work, as well as through controlling the over-etching time with a low silicon etching rate.

To ascertain the effectiveness of the etch-stop process, the ionic current of the fabricated nanopore was measured following the completion of the passivation process, and the results are presented in Fig. 4.18c. It can be observed that the ionic current of the nanopore before and after the passivation process is nearly identical, indicating that the nanopore size does not undergo a notable change, this can be attributed to the negligible over-etching and accurate control of the oxide layer. Following the completion of the passivation process, the ionic current corresponding to the fabricated nanopore did not increase sharply with the continuous etching compared with the pore-opening process. It turned out that applying the appropriate passivation potential quickly formed the oxide layer and effectively realized the etch-stop while the size of the nanopore remained approximately constant due to the slow etching rate of the oxide after passivation.

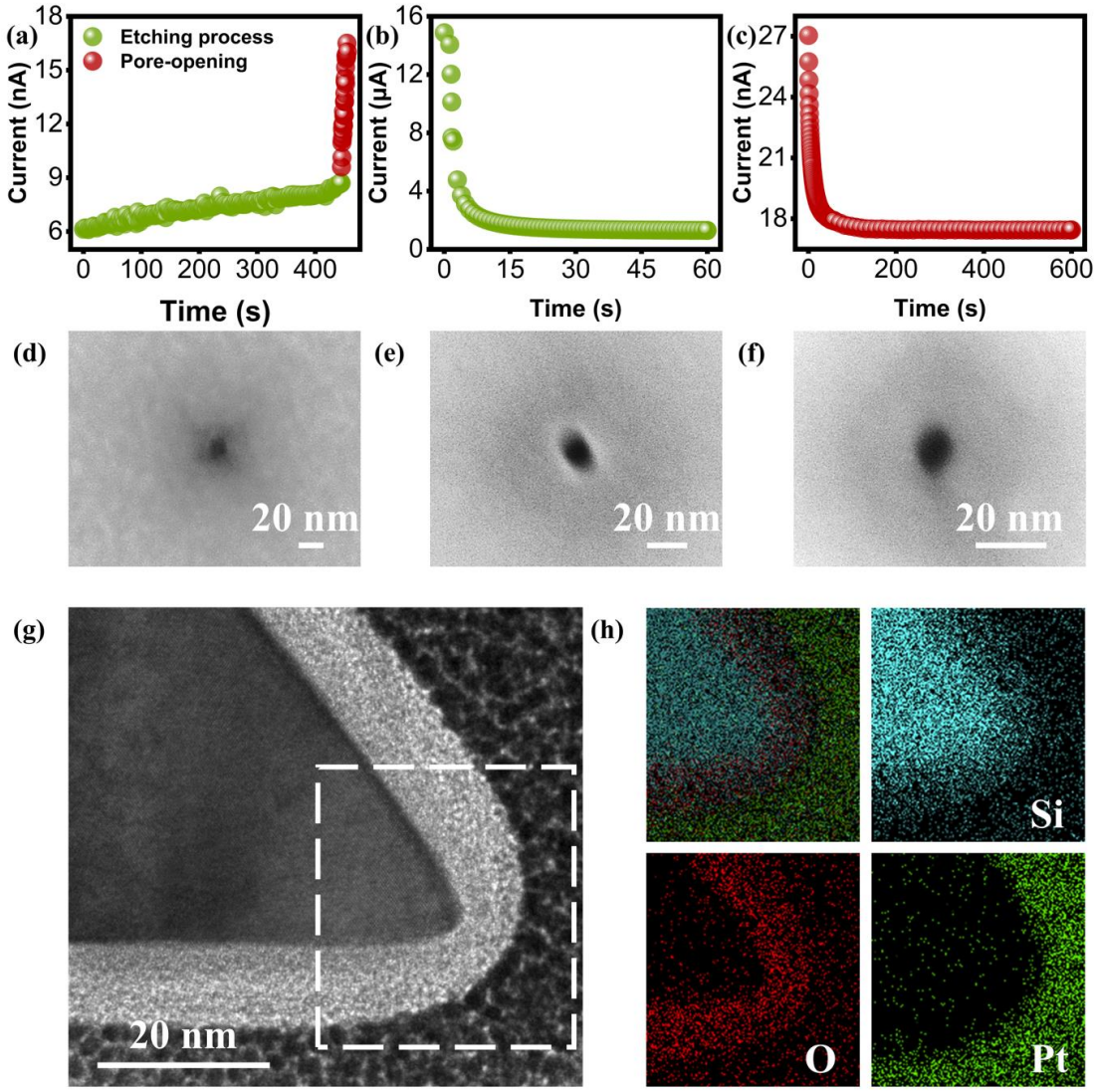

Figure 4.18 Controllable fabrication of silicon nanopores based on electrochemical passivation and the characterization of the obtained nanopores. Current-time curve of

the a) pore-opening process, b) passivation process and c) fabricated nanopore d, e, f) SEM image of the fabricated nanopores based on passivation with different potentials g) Cross-sectional TEM image a nanopore fabricated with a passivation process and corresponding f) EDS elemental mapping.

Following the above-described process flow, conducting passivation with distinct potentials, nanopores with sizes of 11.9, 10.8, and 8.9 nm were obtained and the corresponding SEM images are exhibited in Fig. 4.18d, e, and f, respectively. The fabrication process used an identical over-etching time (~10 s) after the pore-opening event to ensure the nanopores had approximately the same size before passivation. Different passivation potentials of 0.5, 1.5, and 2.5 V were employed to induce oxide layer formation of varying thicknesses and etch-stop rapidly. An elevated passivation potential can be found, resulting in a reduction in final nanopore size. This phenomenon can be attributed to the forming of an oxide layer on the silicon, which conducts a shrinkage of the nanopore, and a higher potential leads to a thicker oxide layer. Furthermore, an increase in the potential of 1 V induced a slight alteration (less than 2 nm) of the nanopore size, which allows nanopore size shrinkage with a precision better than 2 nm.

To further validate that the etch-stop mechanism relies on oxide layer formation, the in-situ characterization of the nanopore fabricated with passivation of 5.0 V is shown in Fig. 4.18g. The cross-sectional TEM image of the nanopore shows that an oxide layer with a thickness of approximately 8 nm, formed by the passivation process, completely covered the silicon surface including (100) and (111) crystal planes, which can effectively realize the reliable etch-stop. This presented structure of a sloped sidewall with an angle of 54.7° was developed by the well-established anisotropic wet etching. Besides, the corresponding EDS analysis of the circled area (white dashed line) in Fig. 4.18h was conducted. The distribution of the three elements (silicon, oxygen, and platinum), as well as the total elemental mapping, are in perfect agreement with the TEM image. These results underscore the ability to regulate oxide growth and thickness by tuning the applied electrochemical potential during the etching process. This enhanced control over oxide layer formation enables precise manipulation of nanopore size and geometry, making the etch-stop strategy based on electrochemical passivation a controllable and scalable method for nanopore fabrication.

4.4. CHAPTER SUMMARY

In this study, we demonstrated the successful fabrication of silicon nanopores using a novel etch-stop strategy based on electrochemical passivation in the TSWE method. The proposed strategy effectively regulated the silicon etching process by dynamically regulating the oxide growth, which enabled precise control over nanopore size. First, the effect of heavily doped boron on the etching rate and its mechanism were studied. The experimental results showed that heavily doped boron on the surface can effectively modulate the etching process. The electrochemical analysis confirmed that

applying a passivation potential regulated the silicon etching rate and further induced the formation of a stable oxide layer, which significantly suppressed silicon etching, achieving a rapid and reliable etch-stop. This mechanism was validated by cross-sectional TEM imaging, which revealed the formation of a uniform passivation layer across the nanopore surface. This reported approach, with a high-precision size shrinkage of silicon nanopores achieved by adjusting the passivation potential, with an accuracy better than 2 nm, enables the controllable fabrication of sub-10 nm silicon nanopores. The integration of electrochemical passivation into the TSWE method offers a scalable, and precise approach for producing nanoscale structures. This method holds substantial potential for applications in nanofluidic, biosensing, and other fields requiring precise nanopore engineering. Future work will focus on optimizing the process for more complex geometries and exploring its applicability to different materials and device architectures.

REFERENCE

[1] Lei, X. Zhang, J. Hong, H. Yuan, Z. Liu, Z. Controllable Shrinking Fabrication of Solid-State Nanopores. Micromachines 2022, 13, 923.

[2] Jiangtao Wei, Hao Hong, Xing Wang, Xin Lei, Minjie Ye and Zewen Liu. Nanopore-based sensors for DNA sequencing: a review. Nanoscale, 2024, 16, 18732-18766.

[3] Liu Zewen, Wang Yifan, Deng Tao, Chen Qi, Solid-State Nanopore-Based DNA Sequencing Technology, Journal of Nanomaterials, 2016, 5284786, 13.

[4] Zeng, S., Wen, C., Solomon, P. et al. Rectification of protein translocation in truncated pyramidal nanopores. Nat. Nanotechnol, 2019, 14, 1056-1062.

[5] Yang, J., Pan, T., Xie, Z. et al. In-tube micro-pyramidal silicon nanopore for inertial-kinetic sensing of single molecules. Nat Commun, 2024, 15, 5132.

[6] Park, S.R., Peng, H. and Ling, X. Fabrication of Nanopores in Silicon Chips Using Feedback Chemical Etching. Small, 2007, 3, 116-119.

[7] Hong, H., Wei, J., Lei, X. et al. Study on the controllability of the fabrication of single-crystal silicon nanopores/nanoslits with a fast-stop ionic current-monitored TSWE method. Microsyst Nanoeng, 2003, 9, 63.

[8] Siwy, Zuzanna S. et al. Electro-responsive asymmetric nanopores in polyimide with stable ion-current signal. Applied Physics A, 2003, 76, 781-785.

[9] S. S. Wang, V. M. McNeil and M. A. Schmidt, An Etch-stop Utilizing Selective Etching Of N-type Silicon by Pulsed Potential Anodization, Journal of Microelectromechanical Systems, vol. 1, no. 4, pp. 187-192, 1992.

[10] Ma Z, Liu Y, Deng L, Zhang M, Zhang S, Ma J, Song P, Liu Q, Ji A, Yang F, Wang X. Heavily Boron-Doped Silicon Layer for the Fabrication of Nanoscale Thermoelectric Devices. Nanomaterials. 2018, 8(2), 77.

[11] N, F, Ralay, et al. (100) silicon etch-rate dependence on boron concentration in EPW solutions. J. Electrochem. Soc, 1984, 132,161.

5

IONIC FET BASED ON SILICON NANOPORE

5.1. INTRODUCTION

5.1.1. BACKGROUND

Ionic channels and nanopores embedded in cell membranes are vital for living organisms as they support normal physiological processes through functions like ion selectivity [1]. The first reported use of a biological nanopore for bio-sensing in 1996 demonstrated an ionic current drop when single-stranded DNA (ssDNA) translocated through the nanopore [2]. Over the past few decades, nanochannels and nanopores have become indispensable tools and platforms across various disciplines.

Solid-state nanopores have since been introduced to overcome the inherent limitations of biological nanopores, such as fixed pore size, and their mechanical and chemical instability. These solid-state structures have significantly broadened the scope of applications beyond biotechnology. In biotechnology, they are used for DNA identification and protein profiling. Beyond this field, they have enabled advancements in molecular separation, ion selectivity, energy generation, nanopatterning, and nanostencil lithography. Solid-state nanopores, with their tunable properties and robust performance, have thus established themselves as a versatile tool in both scientific research and technological innovation.

5.1.2. STATE OF ART

Ionic current rectification (ICR) in nanopores has been extensively explored due to its broad applications including energy conversion, sensing, and ionic circuits. This phenomenon is mainly caused by the asymmetric surface charge distribution and is commonly observed in nanopores with asymmetric structures such as conical nanopores [3]. These nanopores manifest preferential conduction of the ionic current, that is, diode-like I-V characteristics [4]. Many methods used to regulate the ICR have been reported since the ICR was highly related to the nanopore structure, surface charge, electrolyte species, and pH [5]. Daiguji et al first introduced a nanofluidic diode to achieve a stronger ICR [6], and the nanofluidic diode was further explored by Vlassiouk et al later [7,8]. After that, Nam et al introduced an ionic FET based on multiple nanopores with an embedded electrode, the ionic current of the device can be efficiently manipulated by the gate voltage. The results suggested that the ICR in ionic FETs can be regulated by gate voltage [9]. Then Ai et al used a continuum model to comprehensively investigate the ICR in conical nanofluidic FETs and predicted the gate voltage can tune the preferential current direction [10]. Expecting the mentioned devices based on nanopores, the researcher also tried to utilize other strategies to realize effective regulation of the ICR. For example, Cao et al regulated the ICR by applying a salt gradient and explained the ICR caused by the ion concentration difference in asymmetric nanochannels [11,12]. Lin et al utilized the modified surface charge to enable further control of the ICR in nanopores and realized the ICR in large size

nanopores by highly charged surfaces [13]. In addition, many efforts were paid to the controlling pH of the electrolytes and modification of the sidewalls by chemical strategies to implement the regulation of the surface charge [14-16]. However, both acidic and alkaline environments may destroy the structure of the biological molecule to be detected, the stability and repeatability of chemical modifications also need to be addressed. Thanks to the semi-conductivity of silicon, and benefitting from the effective three-dimensional gating modulation to electrical characteristics of the nanopore channels [17,18], the ionic FETs based on silicon nanopores are an excellent candidate for several applications such as energy conversion, sensing, and ionic circuits.

5.1.3. OBJECTIVE

In this chapter, we introduce an ionic field-effect transistor based on a single-crystal silicon nanopore fabricated using the TSWE method. Importantly, all the fabrication processes are compatible with conventional semiconductor processes and microelectromechanical systems technologies, demonstrating the potential for low-cost, large-scale production of the reported device. This FET features a unique three-dimensional gating configuration, which allows the surface charge of the nanopore channel to be precisely modulated by adjusting the gate voltage. This modulation effectively regulates the FET's electrical characteristics, such as ionic current and rectification behavior. Furthermore, this chapter explores the factors influencing the rectification effect, including parameters such as electrolyte concentration, surface charge density, and channel geometry. The impact of gate voltage on rectification behavior is systematically studied, with experimental results compared to Comsol Multiphysics simulations to validate the findings. Finally, the potential application of the fabricated FETs in biosensing is investigated, demonstrating their feasibility and functionality in detecting biomolecules with high sensitivity and precision.

5.2. RECTIFICATION IN NANOCHANNEL

5.2.1. RECTIFICATION IN SILICON NANOPORE

The rectification effect in nanopores has been utilized to study of microfluidic circuits, nanopore sensors, and energy conversion devices. It refers to the asymmetric ionic current characteristics observed when a voltage is applied across the nanopore. As exhibited in Fig. 5.1. It resembles a diode-like behavior, where the ionic current in one direction is significantly higher than in the opposite direction. This effect arises due to the geometrical asymmetry of the nanopore structure and the uneven surface charge distribution. In conical nanopores, this effect is particularly prominent due to the asymmetry between the narrow and wide openings. To analyze the rectification effect, the current rectification factor (RF, $\frac{|i_{-V}|}{|i_{+V}|}$) is defined as the ratio of ionic currents in nanopores under a pair of bias voltages of the same magnitude but opposite directions.

This factor serves as a quantitative measure of the degree of rectification effect. The larger the RF, the stronger the rectification effect exhibited by the nanopore.

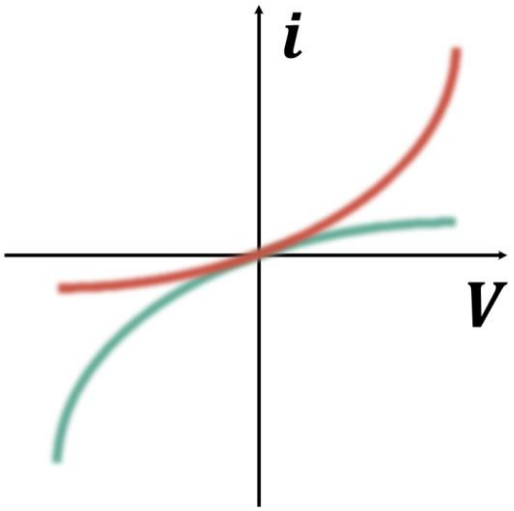

Figure 5.1 Typical current-voltage curve diagram with rectification effect.

Here are the main factors which affect the rectification:

Geometric Asymmetry:
The tapered shape creates an uneven electric field distribution within the nanopore. The narrow opening (the tip) experiences a stronger electric field, while the wide opening has a weaker field. This electric field gradient influences the ion migration speed and direction, causing an asymmetry in the overall ionic current.

Asymmetry in Surface Charge:
The nanopore surfaces typically carry charges (e.g., negatively charged silica). The charge distribution attracts counterions (opposite charges) and repels co-ions (like charges). The difference in surface charge density between the narrow and wide ends results in an asymmetric ion concentration within the nanopore, directly impacting the ion flux and current.

Electrical Double Layer (EDL) Overlap:
When the nanopore diameter is close to or smaller than the Debye length (thickness of the EDL), the EDL at the narrow tip overlaps. This overlap causes the selective accumulation of counterions, enhancing ion selectivity. Under different polarizations, the efficiency of ion migration changes significantly, producing the rectification effect.

Ion Concentration Polarization:
At high electric fields, the ion concentration at the narrow tip may polarize, deviating further from a uniform distribution. This polarization effect amplifies the asymmetry in ion migration, further enhancing rectification. Next, we will examine the impact of the

electric double layer on ionic currents and the rectification effects in nanopores. This analysis will help elucidate how the interplay between the EDL and nanopore geometry contributes to the observed ionic transport behaviors and rectification phenomena.

5.2.2. ELECTRICAL DOUBLE LAYER

In the study of silicon nanopore fabrication using the ionic current-monitored TSWE method discussed in Chapter 3, we previously noted that the electrical double layer has a negligible effect on the nanopore ionic current when the size of the EDL is much smaller than the nanopore size. However, when the electrolyte concentration is very low, the EDL thickness becomes comparable to the nanopore size, resulting in the EDL-dominated surface conductance significantly influencing the ionic current through the nanopore. In this section, we will briefly introduce the principle of the electrical double layer and its impact on the ionic current in the nanopore. By understanding the formation and behavior of the EDL under different conditions, we aim to provide insights into its mechanism and the ways it influences the ionic conductance in nanopores and nanopore-based ionic FET, particularly when the size of the EDL becomes comparable to the dimensions of the nanopore. This understanding is critical for accurately interpreting the ionic current and for optimizing the nanopore-based sensing.

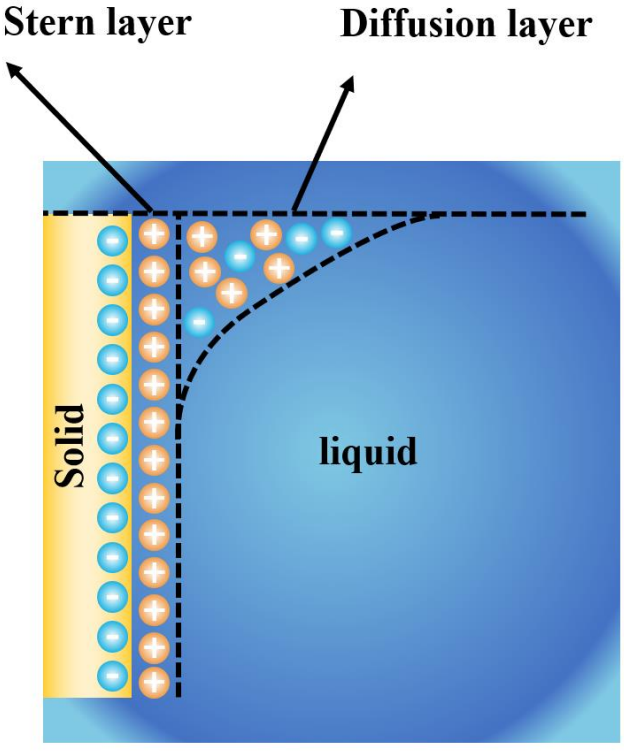

Figure 5.2 Traditional model for the EDL.

As a central topic in electrochemistry, the model of the electrical double layer is widely used to describe the distribution of charges and potential at the liquid-solid interface. The concept of the EDL was first introduced by Helmholtz, who discovered that two

layers of opposite charges form at the electrode/electrolyte interface, separated by a small distance [19]. This initial model was later refined by Gouy and Chapman, who proposed that ions are not rigidly attached to the solid surface but are instead distributed within a thin region near the surface, giving rise to what is now known as the diffuse layer [20,11]. In 1924, Stern combined the Helmholtz model with the Gouy-Chapman model [22], introducing the concept of two distinct charge regions: the Stern layer (SL) and the diffuse layer (DL), as illustrated in Fig. 5.2. The Stern layer consists of ions, often hydrated, that are strongly adsorbed onto the charged electrode surface. In contrast, the diffuse layer comprises ions of opposite polarity to the electrode's charge, whose concentration decreases with increasing distance from the surface. This combined model more accurately represents the charge and potential distribution at the interface, providing a deeper understanding of the EDL's structure and behavior.
The thickness of the electrical double layer formed at the solid-liquid interface, often referred to as the Debye length, can be derived from the Poisson-Boltzmann equation. The final formula for the Debye length, λ_D, is given by:

$$\boldsymbol{\lambda_D} = \sqrt{\frac{\boldsymbol{\varepsilon_0 \varepsilon_r K_B T}}{\boldsymbol{2 c_{(KCl)} e^2}}} \tag{5.1}$$

5

Where c, ε_0, ε_r represents the concentration of the electrolyte solution, permittivity of free space and relative permittivity (dielectric constant) of the medium, respectively. The Debye length (λ_d) represents the characteristic distance over which electric potential decays in the EDL. It quantifies the thickness of the diffuse layer and depends on the electrolyte concentration, temperature, and permittivity of the medium. A higher ionic strength leads to a smaller Debye length, indicating a thinner EDL. Conversely, lower ionic strength results in a thicker EDL. When the concentration of the electrolyte solution is very low, the corresponding Debye length increases significantly as indicated in table 5.1. Especially when the Debye length becomes equal to or even larger than the nanopore size, the surface charge induced by the EDL will substantially affect the ohmic properties of the nanopore (ionic channel).

Table 5.1 Reference of Debye length corresponding to different electrolyte solutions

Concentration (M)	1	0.1	0.01	0.001	0.0001	0.00001
$\boldsymbol{\lambda_D}$ **(nm)**	0.30	0.96	3.10	9.60	30.5	96.3

Here, we can further analyze the effect of a double electric layer on the ionic current through of nanopore using Equation 3.4. To simplify the analysis, Equation 3.4 can be simplified as:

$$i = V\frac{d_{pore}^2}{\rho L_{eff}} + V\mu_k\sigma\frac{d_{pore}}{L_{eff}} \quad (5.2)$$

As described in Equation 5.2, the ionic current in a nanopore comprises two primary components. The first component, represented by the initial term of the equation, is primarily determined by the conductivity of the electrolyte solution, assuming a fixed nanopore size. The second component, described by the second term, is mainly influenced by the surface charge density (σ). This behavior is illustrated in Fig. 5.3. In the high-concentration region, where the Debye length is smaller than or comparable to the nanopore diameter, the ionic current exhibits a linear relationship with the electrolyte concentration, reflecting bulk ionic transport properties. However, as the concentration decreases and the Debye length becomes comparable to or larger than the nanopore diameter, the ionic current deviates from bulk behavior and transitions into a surface charge-governed regime with a lower slope. In this low-concentration region, the electrical double layer extends further into the nanochannel, resulting in overlapping EDLs that dominate ion transport. This overlap leads to counterion enrichment and saturation of the ionic current, as the bulk contribution becomes negligible compared to the surface charge effect.

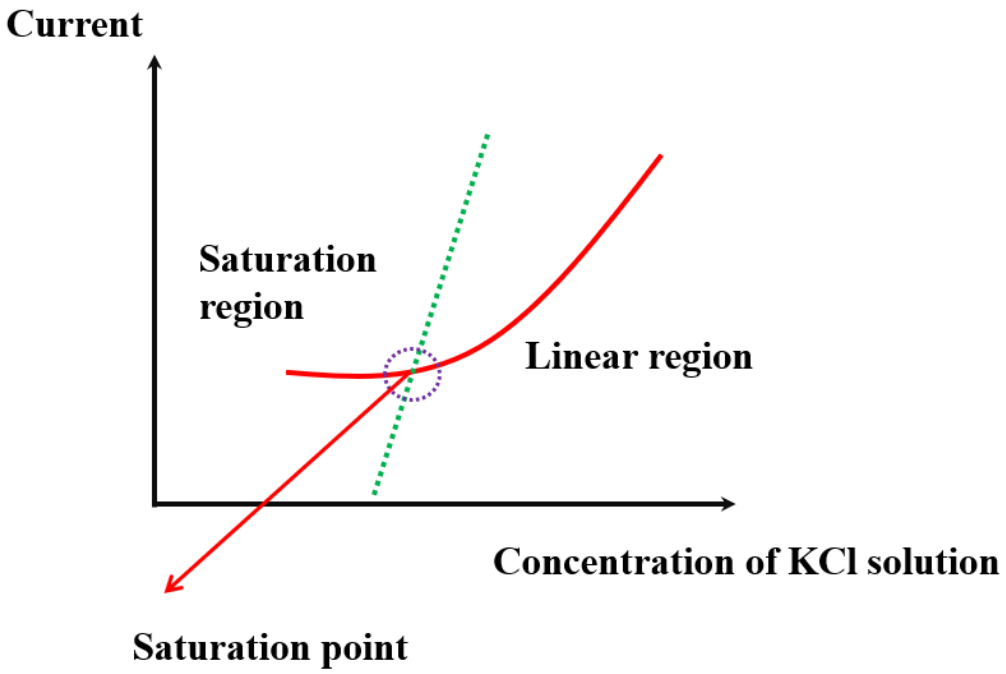

Figure 5.3 Relationship between the ionic current and KCl electrolyte concentration of the nanopore.

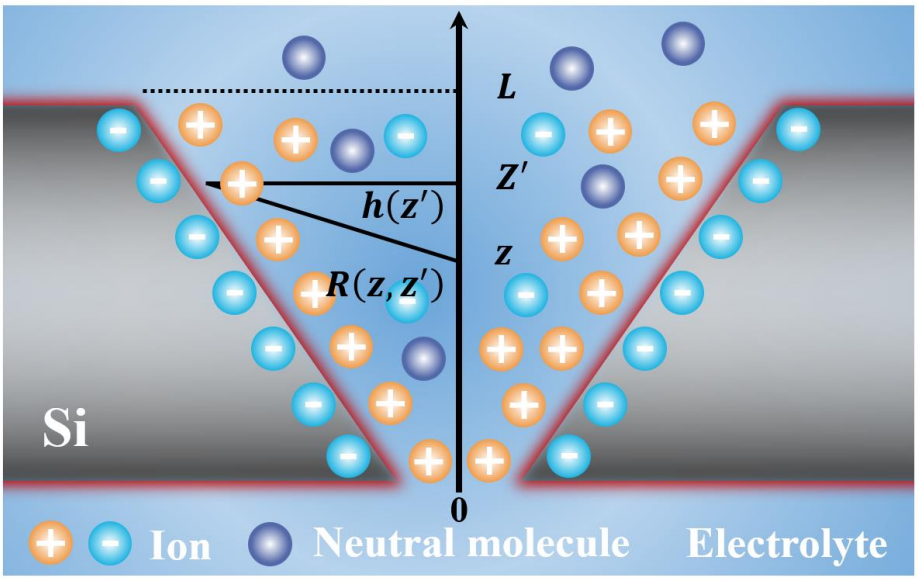

Figure 5.4 Model of ion distribution inside the nanopore with EDL.

To model the electrostatic potential profile inside a silicon nanopore, we considered a cation moving along the pore axis and interacting with the negative charges on the pore walls. Figure 5.4 demonstrate the model of ion distribution inside the nanopore with EDL. The interaction between the cation and the surface charges was assumed to follow Debye-type interactions, which account for the screening effect in an electrolyte solution. This interaction is significant only in nanopores that are sufficiently narrow, with diameters comparable to the thickness of the electrical double layer (Debye length). The short-range nature of electrostatic interactions in an electrolyte is attributed to the strong screening effect caused by the presence of other ions.

To calculate the electrical potential of a cation at a specific position z along the pore axis, the following formula was used:

$$V(z) = -2\pi\rho \int_0^L \frac{h(z')e^{-\lambda R(z,z')}}{R(Z,Z')} dz' \tag{5.3}$$

where ρ is the surface charge density at the pore wall, R is the distance between the cation on the pore axis and negative charges on the pore walls (Fig. 5.4), L stands for length of the pore, $h(z')$ is the radius of the pore at point z' and λ indicates the inverse screening length related to the thickness of the electrical double layer. The integration indicates that thepotential of a cation at a given position z results from interactions with carboxylate groups on the entire surface of the nanopore. For conical nanopores including silicon nanopore, without any voltage applied from the outside, the shape of the internal potential has been shown to be asymmetric, reminiscent of the shape of a ratchet potential (Fig. 5.5). The potential minimum is situated at the narrow opening of a conical nanopore. Assuming a simple superposition of the externally

applied voltage with the internal electric field, one can obtain the resultant potential profiles for the two polarities of the applied voltage.

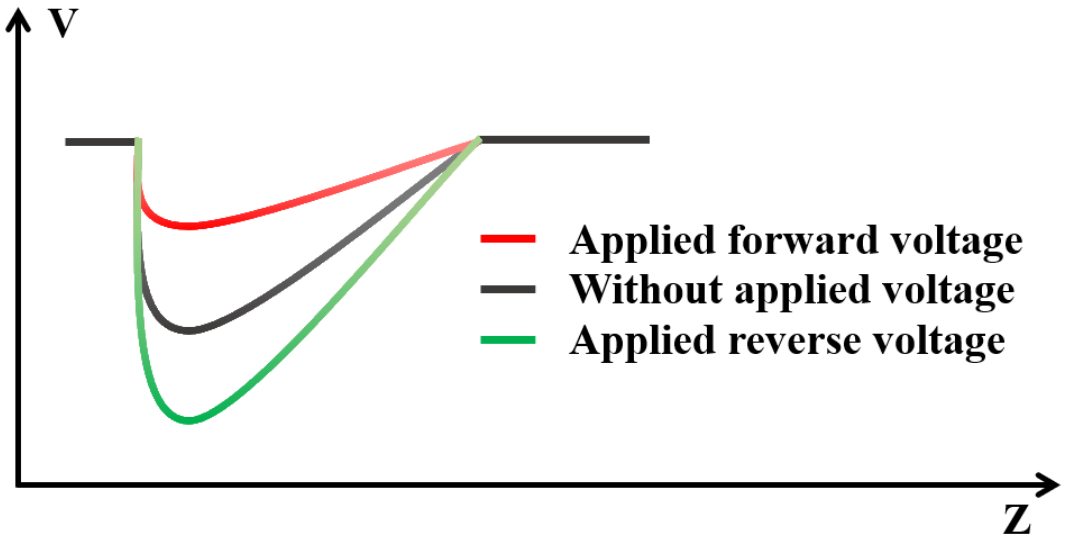

Figure 5.5 Electrostatic potential distribution along with the nanochannel.

Figure 5.5 illustrates the distribution of the electric potential around the nanopore under conditions with and without an applied voltage. As shown in the figure, there is a noticeable reduction in the electric potential at the nanopore channel in the absence of an applied bias voltage. This phenomenon arises from the combined influence of the asymmetric structure of the silicon nanopore and the electric double layer. The lowest potential point corresponds to the narrow opening the nanopore, with the potential gradually increasing along the positive Z-axis (away from the narrow opening).
Due to the presence of this potential well, an additional electric field induced by the applied bias voltage superimposes onto the existing potential profile, either amplifying or diminishing the potential well. This modulation results in either a reduction or enhancement of the ionic current under the applied bias. Specifically, a deeper potential well requires ions to possess higher energy to traverse the nanopore channel, reducing the ionic current. Conversely, a shallower potential well facilitates easier ion transport, increasing the ionic current. The asymmetry in ionic current observed under forward and reverse bias voltages of the same magnitude arises from this varying energy barrier and forms the basis of the rectification effect. From the above analysis, it is evident that the applied bias voltage can regulate the rectification effect. Additionally, the electric double layer itself influences the potential well. The thickness of the double layer, in turn, is primarily controlled by the electrolyte concentration, making the electrolyte solution a crucial parameter for regulating the rectification effect. In the subsequent sections, we will investigate the impact of various factors on the rectification effect.

5.2.3. COMSOL SIMULATION

To further verify the rectification effect in silicon nanopores, we utilize Comsol Multiphysics software to simulate the ion concentration distribution within the

nanopore channel under an applied bias voltage. The simulation results aim to demonstrate the existence of the rectification effect in the silicon nanopore channel. In this context, the Poisson-Nernst-Planck (PNP) model is employed, a widely used framework in nanopore research for characterizing ion distribution and transport within nanochannels.

The default nanopore model is a 2D-axisymmetric geometry, simplifying the computational process while enabling the generation of full 3D solutions through axisymmetric revolution. The simulation system incorporates the Electrostatics Module and the PNP Module, the Electrostatics Module describes the potential distribution in the system while the PNP Module characterizes the interplay between ionic migration, concentration, and electrostatic potential. The governing equations for the PNP module are as follows:

$$\nabla^2 V = -\frac{F}{\varepsilon}\sum_i z_i c_i \tag{5.4}$$

$$J_i = -D_i \nabla c_i - \frac{z_i F}{RT} D_i c_i \nabla V \tag{5.5}$$

where i represents the ionic species in electrolyte solution; J_i, D_i, c_i and z_i are the ionic flux vector, the diffusion coefficient, the concentration, and the valence of i in solution, respectively; ε is the permittivity of the KCl solution; V is the electrostatic potential; and F, R, and T are Faraday's constant, the gas constant, and the temperature, respectively. The parameter settings used in the simulation are shown in Tables 5.2.

Based on the above model and parameters, the ion concentration distribution in the nanopore was simulated under an applied bias voltage of ±0.8V. Figure 5.6 displays the total ion distribution within the nanopore after applying the bias voltage, while Fig. 5.7 and 5.8 illustrate the concentration distribution of Cl^- and K^+ ions, respectively. As evident from Fig. 5.6, the ion concentration at the narrow opening of the nanopore varies significantly depending on the polarity of the applied bias voltage. A more detailed examination reveals that under positive bias, the ion concentration at the narrow opening is substantially higher compared to the negative bias condition. This behavior is further supported by the individual ion distributions shown in Figures 5.7 and 5.8, which demonstrate similar trends, indicating asymmetrical ion accumulation driven by the bias voltage polarity.

The enrichment of ions, such as cations, at the narrow opening of the nanopore results in an electrostatic repulsion effect that facilitates the passage of anions through the nanopore, thereby making the nanopore selectively permeable to anions. Conversely, the accumulation of anions at the narrow opening would favor the passage of cations due to similar electrostatic interactions. This ion accumulation asymmetry under voltages of opposite polarity leads to differing ion selectivity, ultimately causing the ionic current at the same voltage magnitude but opposite polarity to vary significantly, a phenomenon referred to as the rectification effect. The above simulation results further confirm that the rectification effect arises from the combined influences of the

asymmetric silicon nanopore structure, the applied bias voltage, and the electric double layer. Applying a bias voltage with the same magnitude but opposite polarity results in a non-uniform ion concentration distribution along the nanopore channel, thus inducing distinct ion selectivity and contributing to the observed rectification effect.

Table 5.2 Main parameter in the COMSOL simulation

Parameter	Value	Unit	Description
Pore diameter	20	nm	
Bias potential	0.8	V	Applied potential
Surface charge density	-0.06	C/m^2	
D1	1.956×10^{-9}	m^2/s	Diffusion coefficient (K^+)
D2	2.031×10^{-9}	m^2/s	Diffusion coefficient (Cl^-)
Z1	1	-	Valence (K^+)
Z2	-1	-	Valence (Cl^-)
Electrolyte concentration	100	mol/m^3	

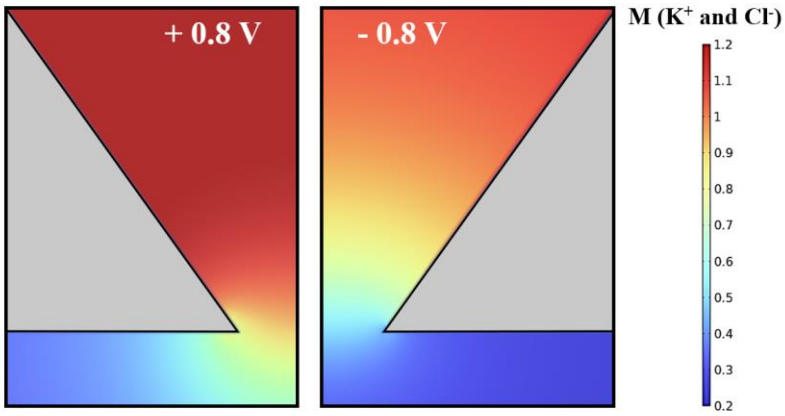

Figure 5.6 Ion concentration distribution inside the nanopore.

It should be noted that, in this simulation, the thickness of the electrical double layer (~0.96 nm) is significantly smaller than the nanopore diameter (20 nm), leading to negligible effects on ion distribution and rectification directly attributed to the EDL. However, as shown in Figures 5.7 and 5.8, a noticeable depletion of Cl^- ions and enrichment of K^+ ions occur along the nanopore sidewalls, which can be attributed to the negative surface charge on the nanopore walls. This surface charge influences ion distribution, contributing to selective ion transport within the channel. Subsequent sections will experimentally investigate the influence of applied voltage, EDL thickness, and surface charge density on the rectification effect observed in silicon nanopores to provide a more comprehensive understanding of these parameters.

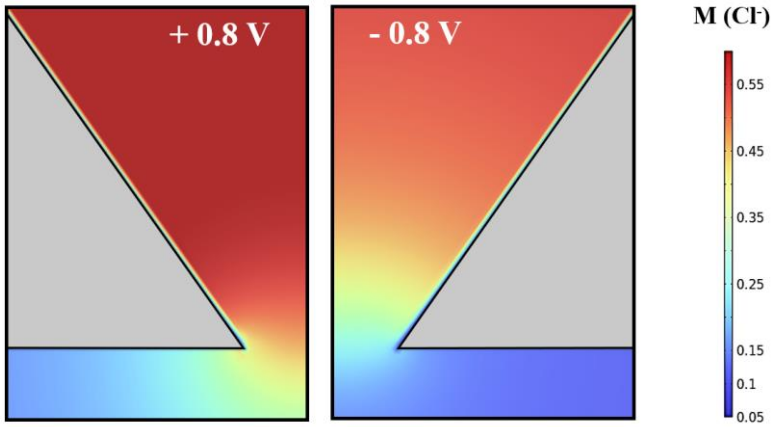

Figure 5.7 Cl^- concentration distribution inside the nanopore.

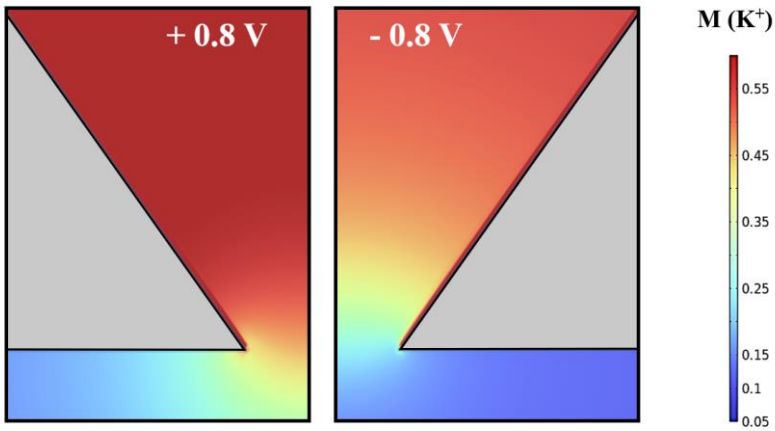

Figure 5.8 K^+ concentration distribution inside the nanopore.

Based on the simulated ion concentration distribution in the nanopore channel, the corresponding ionic current can be calculated using the following formula, and subsequent simulations of the rectification coefficient are based on these results.

$$\boldsymbol{I = N_A \times e \int (J_{K^+} - J_{Cl^-})\, dS} \tag{5.6}$$

Where N_A is the Avogadro constant, e is the amount of charge per electron, J_{K^+} and J_{Cl^-} are the fluxes of potassium ions and chloride ions respectively, and S is the cross section of the nanopore.

5.3. ELECTRICAL CHARACTERISTICS OF IONIC FET BASED ON SILICON NANOPORE

5.3.1. FABRICATION OF IONIC FET

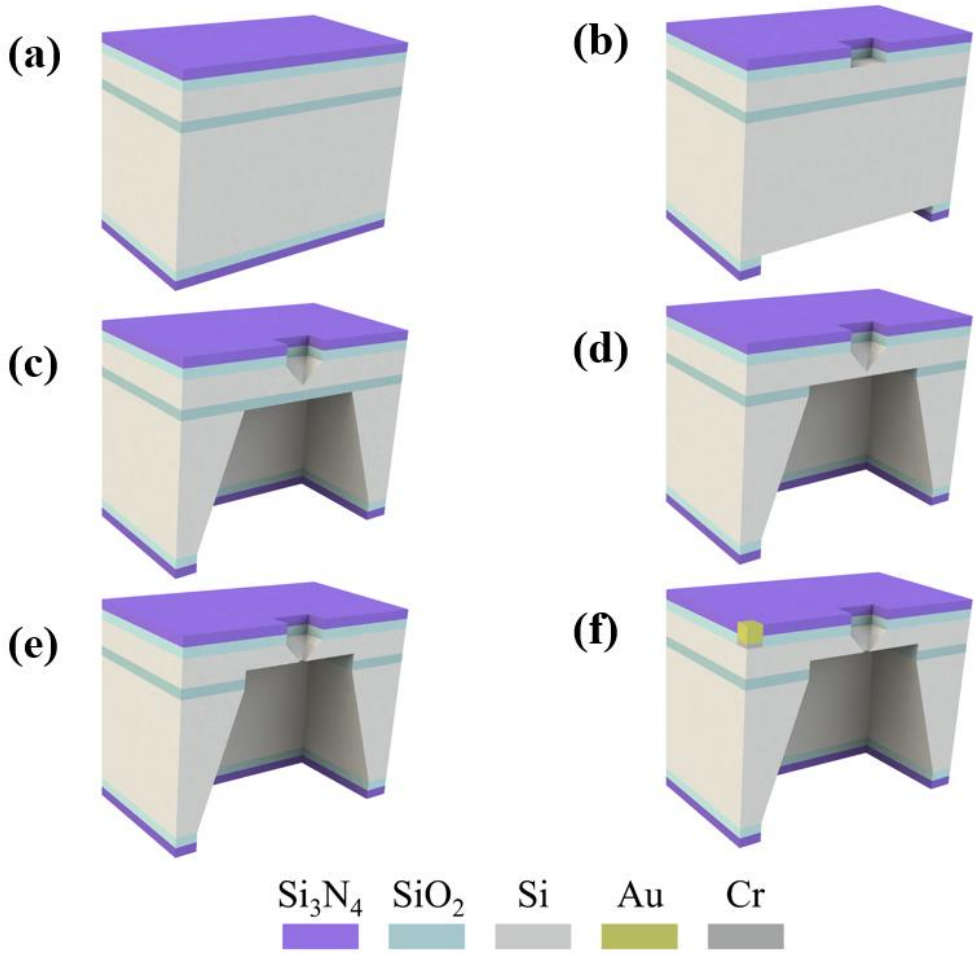

Figure 5.9 Schematic of the critical fabrication process of the ionic FET based on silicon nanopores. (a) Si_3N_4 and SiO_2 mask layers deposition on the SOI chip (b) transfer of patterns by photolithography and removal of mask layers (c) formation of pyramid-shaped pit and back etching window (d) removal of buried oxide layer (e) fabrication of nanopores by TSWE method (f) Cr/Au electrode deposition on the silicon

The fabrication of ionic field-effect transistors based on single-crystal silicon nanopores involves several critical steps, as shown schematically in Fig. 5.9. First, photolithography was used to transfer the patterns of etching windows onto the silicon chip. Inductively coupled plasma was then employed to partially remove the Si_3N_4 and SiO_2 mask layers, creating etching windows on the chip. Anisotropic wet etching was subsequently performed on both sides of the silicon chip, forming pyramid-shaped pits

on the front side and large cavities on the back side. To expose the silicon substrate, the buried SiO_2 layer was removed using buffered hydrofluoric acid, and silicon nanopores were fabricated using the TSWE method. A Cr/Au electrode was then deposited onto the silicon surface as the gate electrode. To ensure ohmic contact between the silicon and the Cr/Au electrode, the mask layers (Si_3N_4 and SiO_2) in the electrode region were removed using ICP, and heavy boron doping was performed on the exposed silicon via ion implantation with a density of 2×10^{15} cm^{-22} and an energy of 30 keV. Pretreatment of the nanochannel, including oxygen plasma (50W, 10min) and piranha etch (H_2SO_4:H_2O_2 = 3:1, 30 min), was carried out to clean the channel and enhance its hydrophilicity. Electrical measurements were conducted using two source meter units (Keithley 2450), one to record the ionic current and the other to apply the gate voltage, with Ag/AgCl electrodes serving as drain and source electrodes. Due to polarization or trapping/de-trapping effects, hysteresis was observed in the field-effect response depending on the voltage sweep direction. To mitigate this, data for all electrical measurements were collected 30 seconds after the start of each measurement. Through this process, ionic FETs based on single-crystal silicon nanopores were successfully fabricated and characterized.

5

5.3.2. RECTIFICATION EFFECT IN IONIC FET

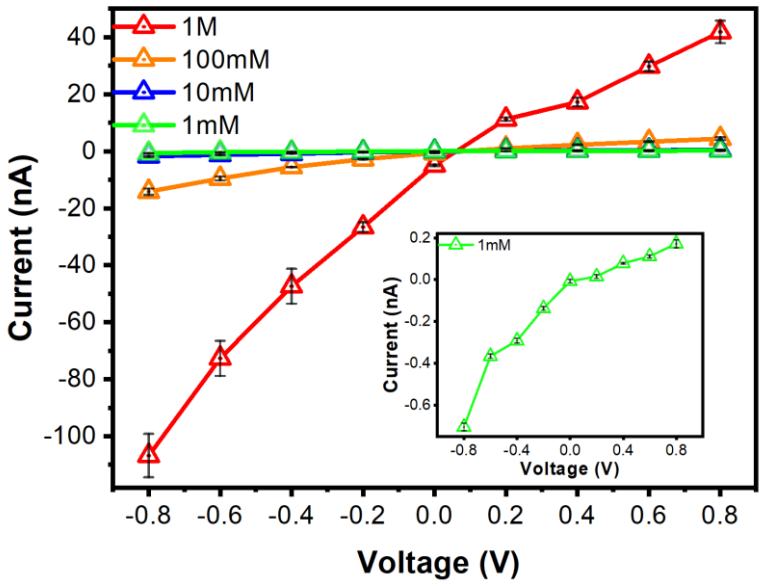

Figure 5.10 Typical current-voltage curves of an ionic FET based on silicon nanopore with a feature size of 6 nm in KCl electrolyte concentration from 0.001 to 1 M (pH=7.2) and applied bias voltage from −0.8 to 0.8 V.

The electrical characteristics of the fabricated ionic FETs without gating were first investigated. Figure 5.10 presents the recorded current-voltage (I-V) curves of an ionic FET based on a silicon nanopore with a feature size of 6 nm under various concentrations of KCl solution. The 6 nm nanopore was fabricated by the well-designed TSWE method and the SEM image was exhibited in Fig 5.11. It should be noted that

for most obtained nanopores by the TSWE method, the shape of the as-etched nanopore is a rectangle rather than the perfect square, as indicated by the initial lithographic pattern. This is caused by imperfections in the mask and the photolithography process. The ionic current increased with the KCl concentration due to the higher conductivity of more concentrated solutions, which enhances the nanochannel conductance and results in a greater ionic current at the same applied bias voltage. For the lowest concentration, 1 mM KCl, the ionic current was negligible due to the low conductivity; thus, the inset figure provides a magnified view of its I-V curve for clarity.

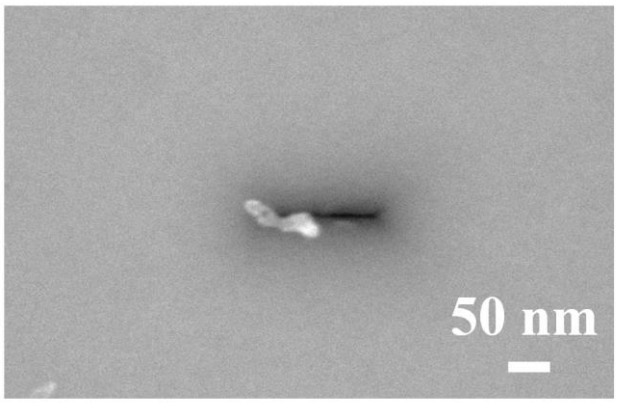

Figure 5.11 SEM image of an individual nanopore with a feature size of 6 nm.

As demonstrated in Fig. 3.20. At higher KCl concentrations, the electrical double layer effect is negligible because the Debye length is smaller than the nanopore diameter. In this regime, the ionic current exhibits a linear dependence on the solution's conductivity. However, as the solution concentration decreases sufficiently to dilute levels, the ionic current saturates and remains nearly constant.

Notably, the ionic current displays significant asymmetry for voltages of the same magnitude but opposite polarity. At any given absolute bias voltage, the ionic current is higher at negative voltages (representing the "on" state) than at positive voltages (representing the "off" state). This behavior demonstrates ion selectivity and rectification effects. For asymmetrically conical nanopores, the rectification arises from establishing an electrostatic field within the nanochannel due to the asymmetric surface charge distribution. This field causes cations to accumulate and anions to deplete at the nanopore tip (or vice versa), resulting in ionic current rectification based on the bias polarity.

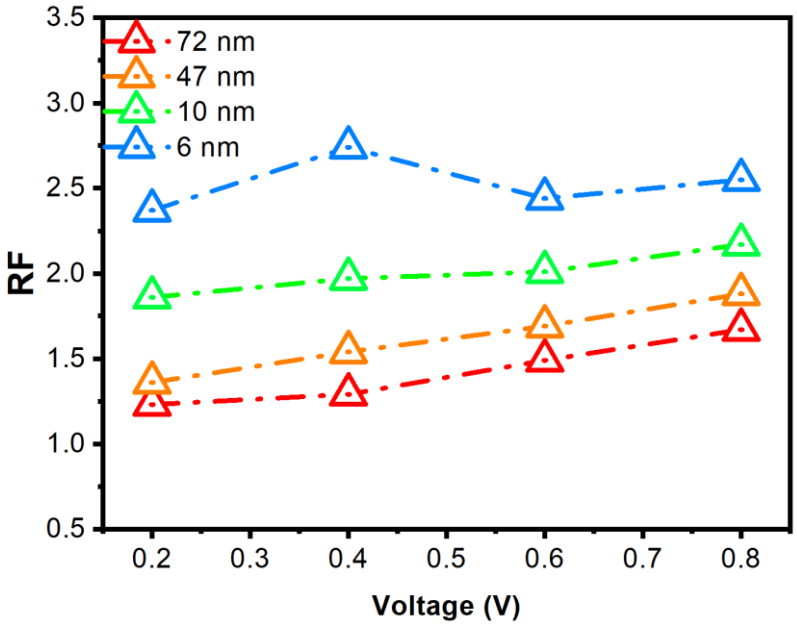

Figure 5.12 RF of the ionic FETs based on silicon nanopores with different feature sizes (1M KCl solution, pH=7.2).

Next, the ionic current rectification characteristics of the fabricated ionic FETs based on silicon nanopores without gating, along with the factors influencing ICR, were analyzed and discussed. Figure 5.12 presents the rectification factor (RF) for ionic FETs with feature sizes of 6, 10, 47, and 72 nm, respectively, in a 1 M KCl solution. The figure shows that stronger ICR is observed at higher applied bias voltages. A larger applied bias voltage enhances ion enrichment and depletion at the nanopore tip, thereby amplifying the rectification effect. Theoretical studies also confirm that in addition to cation/anion selectivity decreasing with increasing ion concentration at a given voltage, ion selectivity and ICR are also functions of the applied voltage [23].

Simultaneously, the rectification factor exhibited a gradual increase with decreasing nanopore size. For an applied bias voltage of 0.8 V, the RF values of the ionic FETs with feature sizes of 72 nm, 47 nm, 10 nm, and 6 nm were 1.7, 1.9, 2.2, and 2.6, respectively. This trend can be attributed to the increasing influence of the electrical double layer as the nanopore size approaches the Debye length. When the nanopore diameter becomes comparable to the Debye length, oppositely charged ions dominate the nanochannel, leading to enhanced preferential ion conduction and, consequently, stronger rectification effects in smaller nanopores.

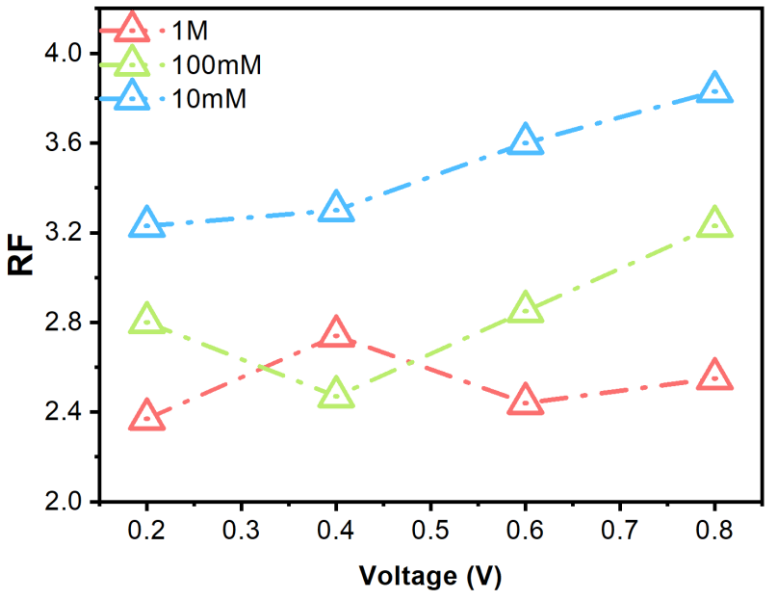

Figure 5.13 RF of the ionic FET based on silicon nanopore with 6 nm feature size in KCl solution (pH=7.2) with different concentrations.

The influence of KCl concentration on ionic current rectification was also studied. Figure 5.13 presents the RF values for an ionic FET with a feature size of 6 nm at varying solution concentrations. Since the Debye length (λ_D) is inversely proportional to the square root of the ionic strength of the solution, lower concentrations result in a longer Debye length, which extends the influence of surface charges on ion transport. This extended screening effect allows more counter-ions to accumulate in the nanochannel, thereby enhancing ion selectivity and rectification effects. At a KCl concentration of 10 mM, the RF reached 3.8 at an applied bias voltage of 0.8 V. Notably, under these conditions, the EDL nearly overlaps with the nanopore dimensions ($2\lambda_D \approx 6$ nm), resulting in the nanochannel being predominantly filled with counter-ions, further amplifying ion selectivity and rectification. However, this overlap also causes ionic current saturation, as the bulk conductance contribution becomes negligible at such low concentrations.

The inset in Fig. 5.10 shows that at a KCl concentration of 1 mM, the ionic current at positive bias voltage is minimal. Under such low concentrations, the ionic current is strongly influenced by noise in the electrical characterization, making accurate measurements difficult. Therefore, rectification results at these lower concentrations were excluded from further analysis.

As mentioned earlier, modulating the surface charge of nanopores is recognized as a practical and effective strategy for controlling ionic current rectification . In this study, we introduced an ionic field-effect transistor based on the previously described silicon nanopores and successfully demonstrated ICR modulation through gate voltage control. The intrinsic semiconductor properties of single-crystal silicon allow direct modulation of surface charge without the necessity for additional conductive layers. Furthermore, during the pretreatment process involving oxygen plasma and piranha etching, a thin

oxide layer (SiO_2) naturally forms on the sidewalls of the nanochannel [24]. This inherent formation of an insulating layer eliminates the need for extra dielectric coatings, such as Al_2O_3, HfO_2, or TiO_2, which are commonly required in other ionic FET designs. This streamlined approach simplifies the device architecture while maintaining effective gating control for ionic current regulation.

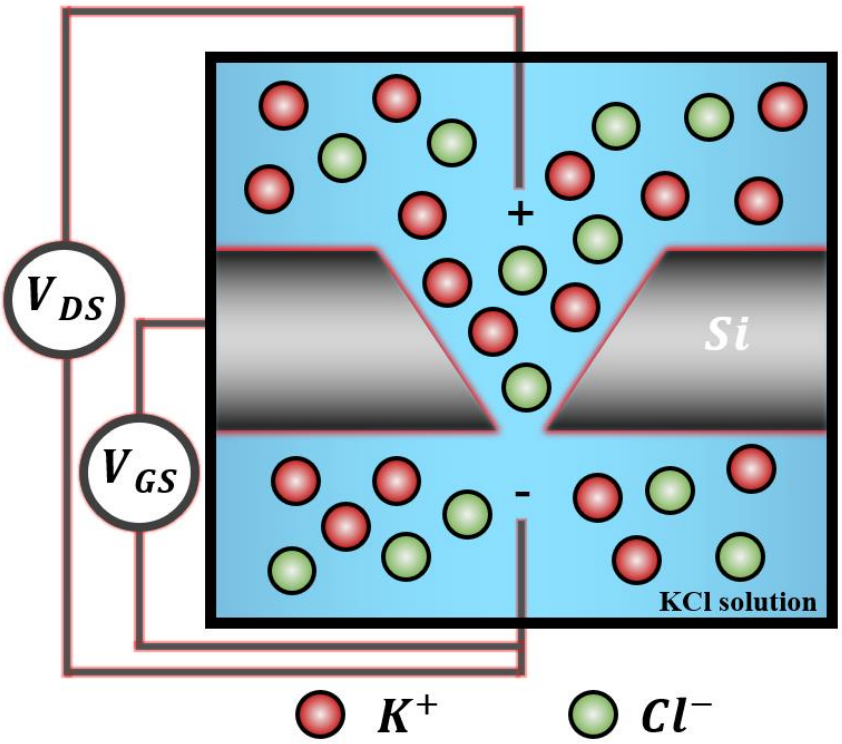

Figure 5.14 Illustration of the ionic FET electric characterization measurement.

This design concept is analogous to a MOSFET, except that in the ionic FET, the medium in the nanochannel is replaced by electrolyte ions. The unique architecture of the ionic FET, where the nanochannel is surrounded by a gate dielectric (SiO_2), enables more efficient three-dimensional gating control over the nanochannel's conductivity compared to devices with partial gating structures. Figure 5.14 schematically illustrates the modulation mechanism of the ionic FET. The gate voltage, applied through the gate electrode, induces a redistribution of charges on the silicon surface, effectively modulating the surface charge density within the nanochannel. The magnitude and polarity of the surface charge density significantly influence the ion distribution within the nanochannel, which directly impacts the ion selectivity of the nanopore and, consequently, alters its rectification effect.

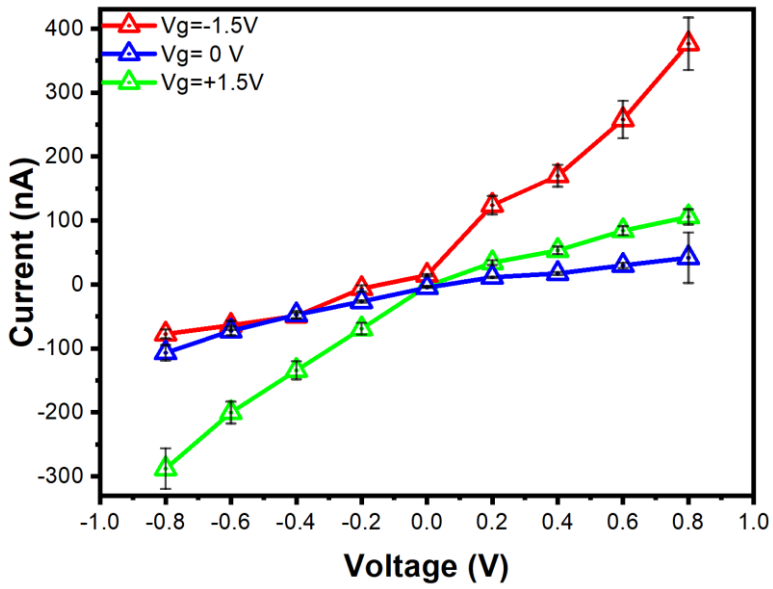

Figure 5.15 Typical current-voltage curves of the nanopore-based ionic FET in 1M KCl solution (pH=7.2) at different gate voltages.

Figures 5.15, 5.16, and 5.17 show the recorded current-voltage curves of the ionic FET with a nanopore diameter of 6 nm under different gate voltages and varying KCl solution concentrations (1 M, 100 mM, and 10 mM, respectively). To ensure accurate electrical characterization and eliminate the potential interference caused by leakage current or dielectric breakdown, the gate voltage was restricted to within ±1.5 V, as indicated in Figure 5.18, which shows the I_D-V_g sweeping curve from -10 V to 10 V along with the leakage current characteristics.

Under the application of a negative gate voltage (red line), the ionic current at positive bias voltages increases significantly, a phenomenon consistent with previously published findings [25]. Similarly, when a positive gate voltage is applied (green line), the ionic current at negative bias voltages exhibits a corresponding significant increase. This change in ionic current is attributed to the enhancement of concentration polarization within the nanochannel, induced by the gate voltage.

Remarkably, as the gate voltage transitions from +1.5 V to -1.5 V, a shift from cation selectivity (characterized by higher ionic current at negative bias voltage) to anion selectivity (marked by higher ionic current at positive bias voltage) is observed. This transition indicates that the majority carrier type within the nanochannel can be dynamically switched between cations and anions by modulating the gate voltage. This controllability highlights the potential of the ionic FET in applications requiring precise ion selectivity and current rectification modulation.

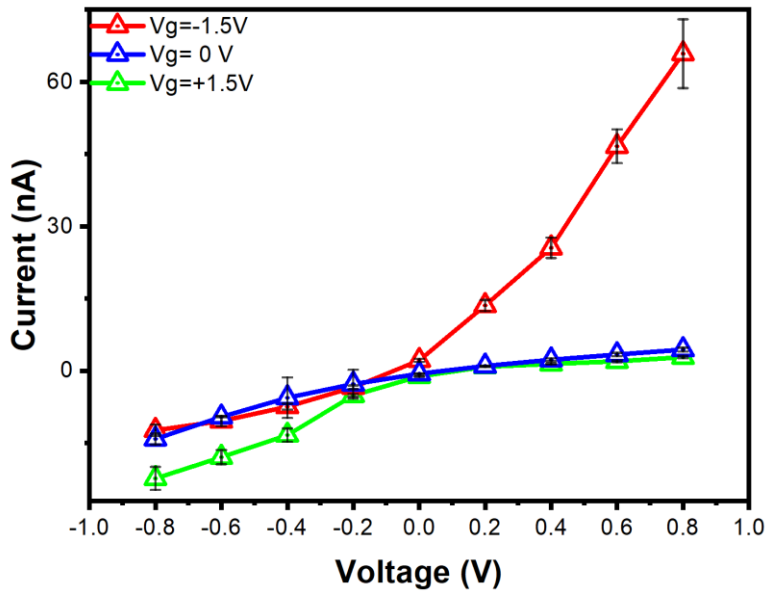

Figure 5.16 Typical current-voltage curves of the nanopore-based ionic FET in 100mM KCl solution (pH=7.2) at different gate voltages.

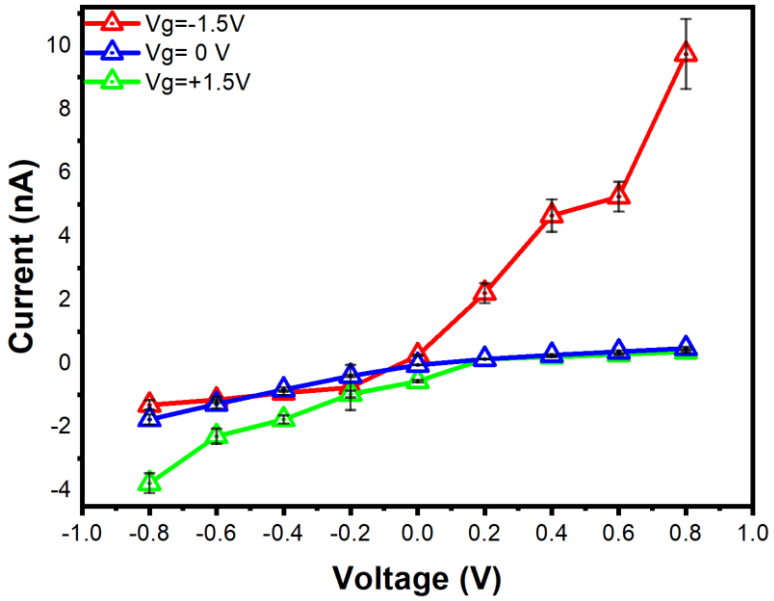

Figure 5.17 Typical current-voltage curves of the nanopore-based ionic FET in 10mM KCl solution (pH=7.2) at different gate voltages.

To investigate the effect of gate voltage on the ionic current rectification of nanopore-based ionic FETs in detail, the relationship between the rectification factor and gate voltage is plotted in Fig. 5.19, with an applied bias voltage of 0.8 V. The extracted RF values from Fig. 5.15, 5.16 and 5.17 reveal that, at a gate voltage of 1.5 V, RF values corresponding to KCl solution concentrations of 10 mM, 100 mM, and 1 M are 10.5, 8.0, and 2.4, respectively. This demonstrates a pronounced modulation effect at lower concentrations due to the thicker electrical double layer.

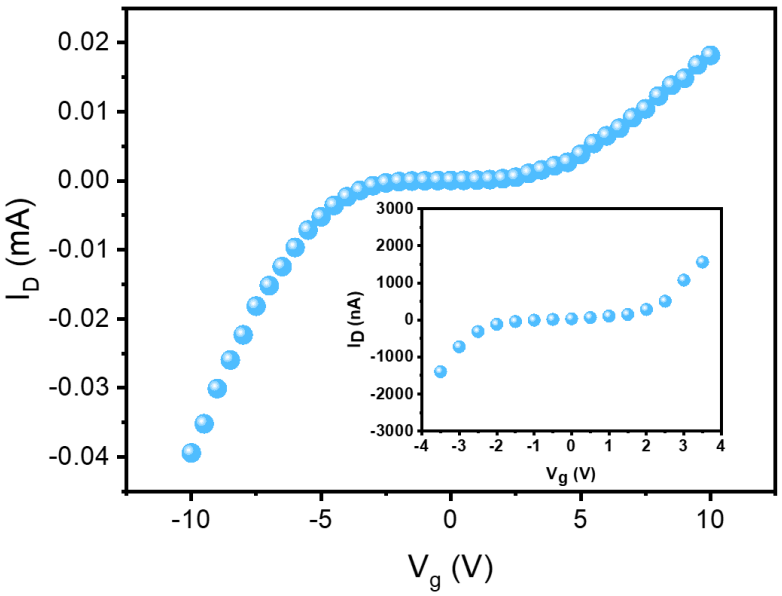

Figure 5.18 The current measurement between drain reservoir and gate electrode (in 1M KCl concentration).

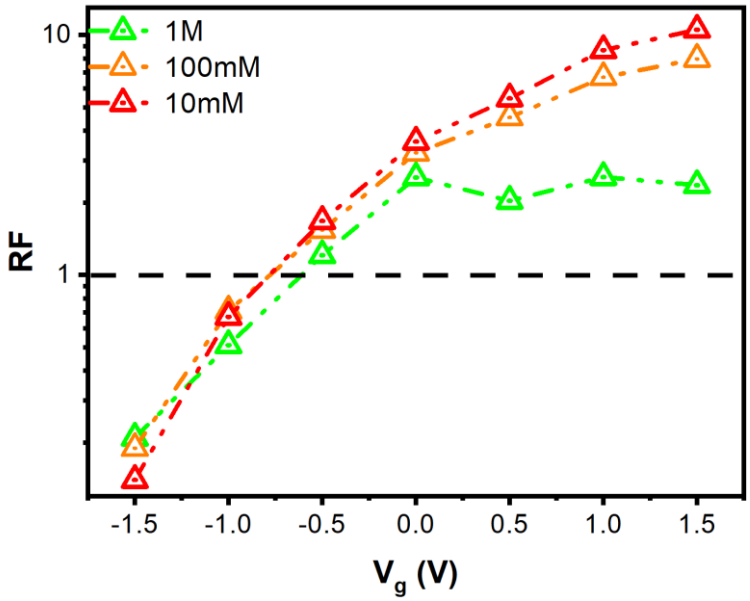

Figure 5.19 Effect of gate voltage on RF of the nanopore-based ionic FET.

As previously mentioned, in the absence of gate voltage, the surface charge present on the nanopore sidewalls induces a slight rectification effect, consistent with earlier reports [26]. To better understand the impact of gate voltage, the effective surface charge density (σ_w^*) can be defined as:

$$\sigma_w^* = \sigma_w + \varepsilon_o E_g \quad (5.4)$$

Here, σ_w, ε_o, and E_g g represent the initial surface charge density (without gate voltage), the permittivity of the nanopore wall, and the electric field generated by the lateral gate voltage, respectively. This relationship highlights that σ_w^* can be regulated in both magnitude and polarity by the gate voltage. Consequently, applying a

sufficiently high gate voltage can overcome the size limitations imposed by the rectification effect, enabling enhanced ICR in larger nanopores.

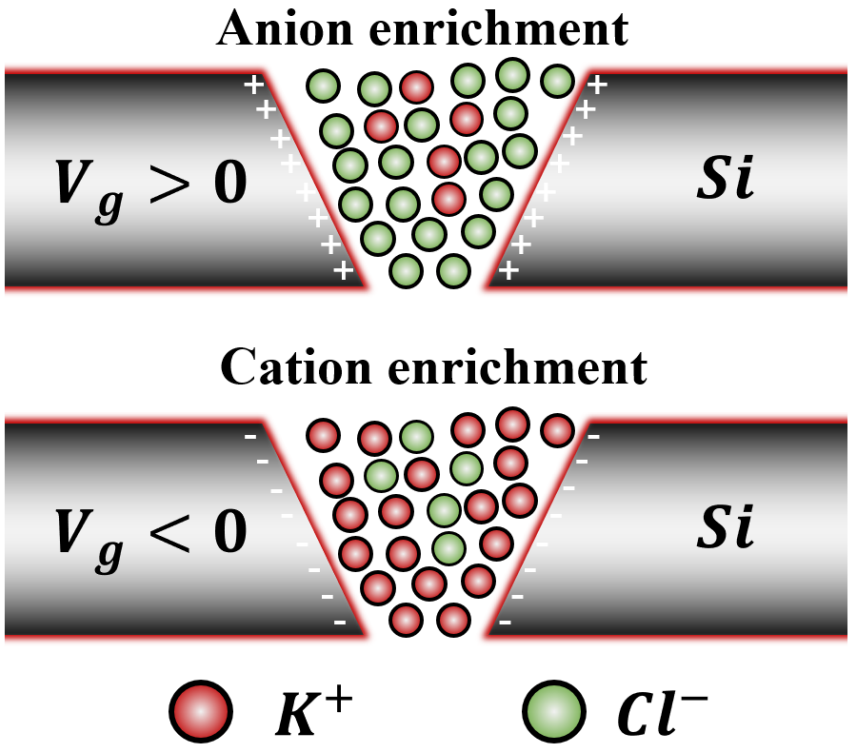

Figure 5.20 Schematic of the majority carrier for the contrary gate voltages.

As shown in Fig. 5.20, a positive gate voltage enhances the surface charge effect, increasing the anion concentration while decreasing the cation concentration in the nanochannel. Conversely, a negative gate voltage reduces anions and enriches cations, altering ion selectivity. Notably, when the gate voltage is approximately -0.75 V, the ionic FET loses its rectification effect (RF = 1), indicating no ion selectivity. At this point, the concentrations of anions and cations in the nanochannel are theoretically equal, and the ionic current follows ohmic current-voltage characteristics. However, as the gate voltage decreases further (less than -0.75 V), the surface charge becomes negative, leading to cation enrichment. In this scenario, RF drops below 1, signifying a switch in ion selectivity from cations to anions.

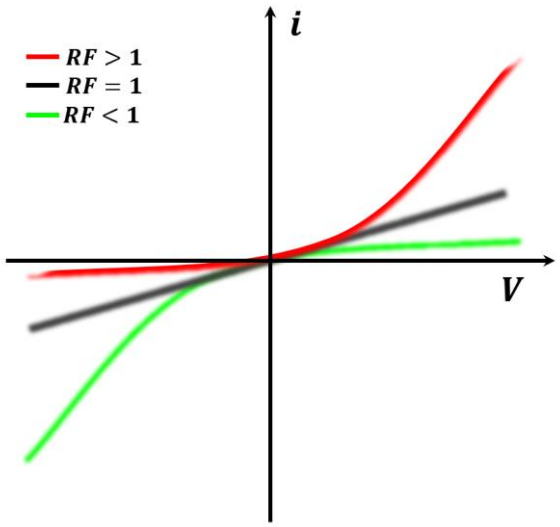

Figure 5.21 Schematic diagram of the current-voltage curves corresponding to different RF.

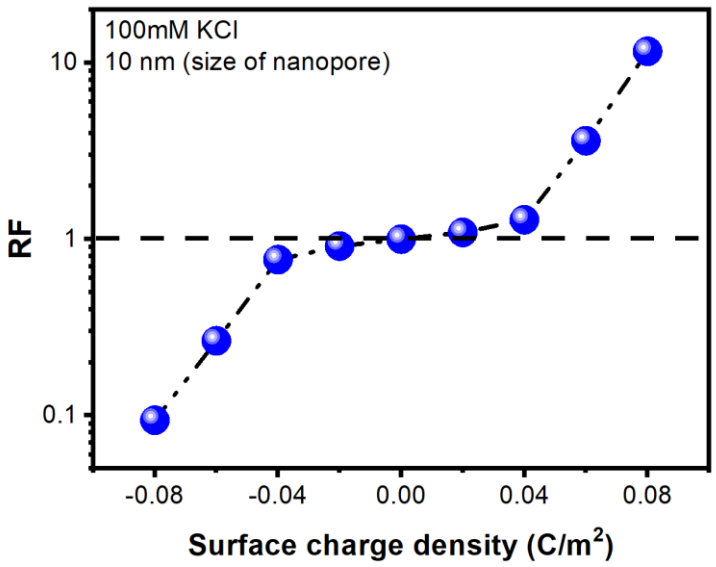

Figure 5.22 COMSOL simulation result of variation of RF in different surface charge density.

In summary, the ionic current of the fabricated ionic field-effect transistor demonstrates the capability to transition between distinct operational regimes, including ohmic (RF = 1) and diode-like (where RF > 1 or RF < 1), which depends on the applied gate voltage. This behavior is driven by the modulation of surface charge density on the nanopore sidewalls, controlled by the gate voltage, which influences both ionic selectivity and current flow within the nanochannel. Figure 5.21 schematically illustrates the voltage-current characteristics for these three RF regimes. In the ohmic regime (RF = 1), the ionic current exhibits a linear relationship with the applied bias voltage, indicating no preferential ion flow direction. Conversely, in the diode-like regimes (RF > 1 or RF < 1), the current responses become asymmetric for voltages of the same magnitude but

opposite polarities, reflecting a preferential conduction pathway caused by surface charge modulation. This controllability presents significant potential for tuning the device for various advanced applications, including biosensing, energy conversion, and ionic circuits.

To further validate the modulation of ionic current rectification by surface charge regulation through gate voltage, COMSOL simulations were conducted. The previous chapter described how ion concentration distributions were simulated by varying surface charge density along the nanopore sidewalls. Based on the ion distributions, the corresponding ionic currents were calculated using Equation 5.6, ultimately enabling the determination of RF. Figure 5.22 displays the simulated variations in RF under different surface charge densities. The results confirmed that RF is directly proportional to the gate voltage, with the rectification direction reversing as the surface charge polarity shifts. Furthermore, when the surface charge on the nanopore sidewalls becomes neutral (no net surface charge), the ionic FET loses its rectification effect (RF = 1). This observation closely aligns with the experimental data, reinforcing the role of surface charge modulation in controlling ionic rectification behavior in nanopore-based ionic FETs.

5.3.3. BIOSENSING

Biosensing is a critical application of nanopores, and the ability to effectively detect biomolecules serves as a key benchmark for evaluating nanopore performance. The primary parameters used to characterize biomolecule translocation events are blockage current and dwell time. In this section, we will validate the biosensing capabilities of single-crystal silicon nanopores fabricated using the TSWE method.

As introduced earlier, biosensing based on solid-state nanopores relies on the specific detection of ionic current changes caused by biomolecular translocation events. Given the small dimensions of the nanopores, the blockage currents induced by biomolecule translocation typically range from tens of picoamps to a few nanoamps. Simultaneously, biomolecules exhibit relatively short translocation times in solid-state nanopores, normally tens of microseconds to a few microseconds. These factors impose stringent requirements on the current resolution, time resolution, and signal-to-noise ratio of the measurement platform.

To meet these demands, in addition to the shielding system previously described, a single-probe ultra-low-noise patch clamp amplifier (Axon Axopatch 200B) will be employed to monitor and record ionic current changes associated with biomolecular translocation through the nanopores. This amplifier has a cooling system that effectively reduces thermal noise, enabling superior low-noise performance across different recording modes. For instance, it achieves noise levels as low as 0.55 pA in whole-cell recording mode (B = 1) and 1.6 pA in whole-cell recording mode (β = 0.1), making it well-suited for the highly sensitive measurements required in this study.

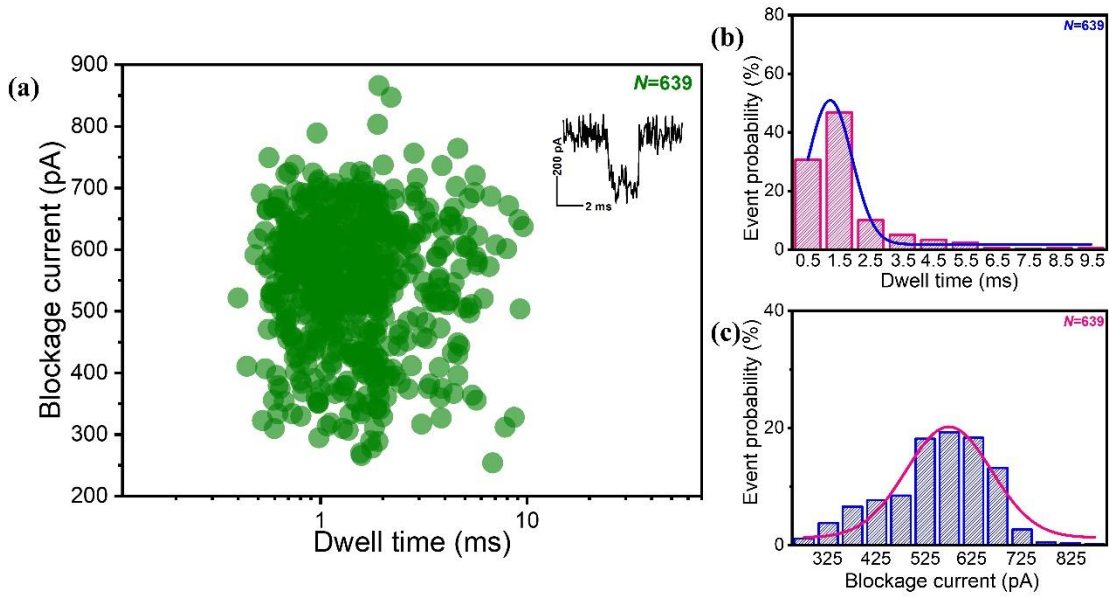

Figure 5.23 DNA translocations through a nanopore with feature size of 11.3 nm. (a) Corresponding event density plot constructed from 639 translocations events at 0.4V applied bias (b) Dwell time and (c) blockage current histogram.

To demonstrate the potential of nanopores with pyramid structures in biosensing, tests were conducted using the ionic current blocking method. Blockage currents during biomolecular translocation events were measured with a patch-clamp amplifier. The signal data was sampled at a rate of 500 kHz and low-pass filtered at 10 kHz. The analog signals were then digitized using a data acquisition module (Digidata 1440A, Axon Instruments, USA). All experiments were performed within the shielding system to minimize noise interference.

Figure 5.23a illustrates the dwell time and blockage current distribution of λ-DNA (48.5 Kbp, 1 ng/μL) translocating through a pyramidal nanopore with a feature size of 11 nm under a 0.4 V bias. The nanopore was immersed in a buffer electrolyte comprising 1 M KCl, 10 mM Tris, and 1 mM ethylenediaminetetraacetic acid (EDTA) at pH = 8.0. Ionic current-time curves were recorded between two Ag/AgCl electrodes placed across the single-crystal silicon nanopore. The scatter plot in Fig. 5.23a reveals that the dwell times and blockage currents of biomolecules are concentrated in the dark region of the graph. Variations in blockage current and dwell time are partly attributed to phenomena such as DNA folding, strand breaks, or overlapping DNA during translocation. The inset figure provides a closer look at a representative ionic current signal. Figures 5.23b and 5.23c separately present the dwell time and blockage current distributions corresponding to Fig. 5.20a. After analysis, the average blockage current was determined to be 548.9 pA, with a transit time of 1.77 ms. This implies a biomolecular translocation rate of approximately 27.4 Kbp/ms. It is worth noting that numerous studies have demonstrated that DNA translocation through nanopores can be slowed by electrically modulating the surface charge of the nanopore walls. This modulation relies

on the careful analysis of induced electroosmotic flow and the electrostatic interactions between DNA molecules and the nanopore [27-29]. The silicon nanopores fabricated in this study also exhibit the ability to reduce the translocation rate of DNA molecules by applying a gate voltage [30]. Here, the mechanism of control through gate modulation in silicon nanopores is briefly discussed.

The translocation rate of molecules, such as DNA, through silicon nanopores can be effectively regulated by applying a gate voltage. This control mechanism leverages the semiconductor properties of silicon nanopores and the electrostatic interactions between the nanopore walls and the translocating molecules. By applying a gate voltage, the surface charge density on the nanopore walls can be modulated. Positive gate voltages increase the positive surface charge, which enhances the electrostatic attraction between the negatively charged DNA molecules and the nanopore walls, thereby slowing down the translocation. Conversely, negative gate voltages amplify the repulsive force, potentially accelerating the translocation or even preventing the DNA from entering the pore.

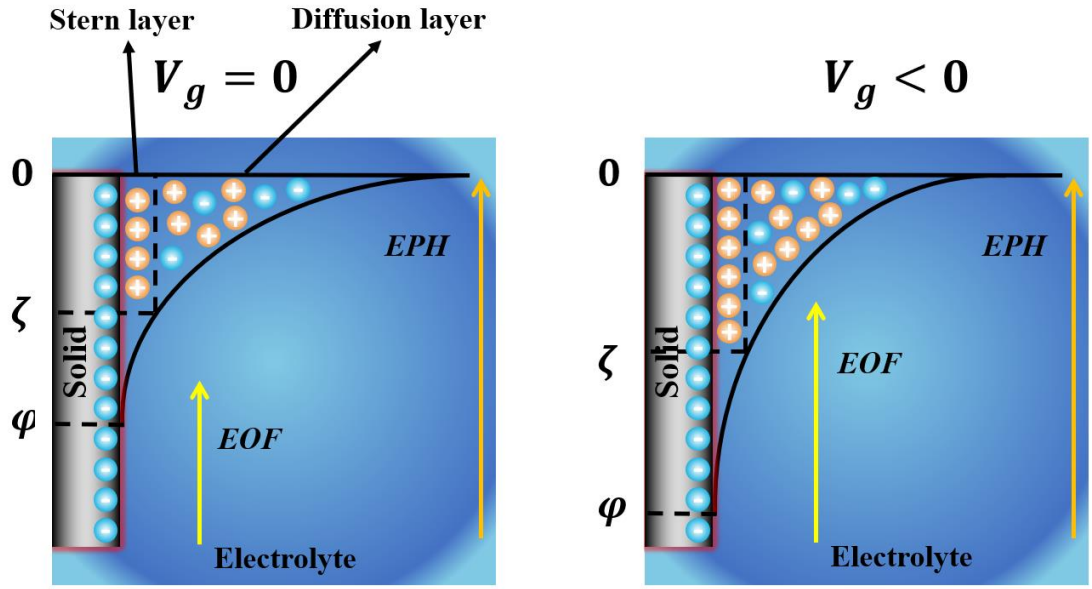

Figure 5.24 Illustration the mechanism of gate voltage controlling molecule translocation through a nanopore.

Another key factor is the effect of gate voltage on the electroosmotic flow (EOF) as demonstrate in Fig 5.24. The translocation rate of a molecular process is determined by both electrophoresis (orange) and electroosmosis (yellow). EOF arises due to the movement of counterions in the electrical double layer along the nanopore walls while EPH arises by the bias voltage. A negative gate voltage can align EOF with the electrophoretic force, accelerating DNA movement through the nanopore. On the other hand, a Positive gate voltages may induce an EOF that opposes the DNA's electrophoretic motion, further reducing its speed. Additionally, gate voltage affects the rectification properties of the nanopore, altering the ionic selectivity. By favoring cationic or anionic currents, gate modulation indirectly changes the ionic environment

inside the nanopore, impacting the DNA's translocation dynamics. This ability to precisely regulate molecular translocation through gate voltage makes silicon nanopores a powerful platform for single-molecule sensing, offering the potential to slow down DNA translocation for more accurate analysis and improved signal resolution.

5.4. CHAPTER SUMMARY

This chapter introduces an ionic field-effect transistor based on a single-crystal silicon nanopore. First, the ionic current characteristics and rectification effects of the silicon nanopore are studied, and the mechanism of rectification and its influencing factors are analyzed in detail. Additionally, the rectification effect is validated through COMSOL simulations. Building on this, the ionic current behavior of the fabricated ionic FET is further explored. Leveraging the semiconducting properties of silicon, the magnitude, and polarity of surface charges on the nanopore sidewalls can be effectively modulated by applying a gate voltage. As a result, the ionic current of the FET can transition between ohmic and diode-like regimes, with the rectification effect adjustable via specific gate voltages. It is anticipated that using materials with higher permittivity as insulating layers could enhance the gate voltage range, allowing for a stronger ionic current rectification. This improvement would enable ICR to be extended to nanopores far larger than several hundred times the thickness of the electrical double layer, thereby addressing size limitations for various applications. Lastly, the chapter demonstrates the application of the fabricated silicon nanopores in biosensing and investigates the principle of gate voltage modulation for controlling molecular translocation through the nanopore. In summary, the proposed ionic field-effect transistor provides a novel platform for studying ion transport properties and holds significant potential for large-scale ion circuits due to its low-cost manufacturing process and excellent electrical performance.

REFERENCE

[1] Y. E. Korchev, C. L. Bashford, G. M. Alder, P. Y. Apel, D. T. Edmonds, A. A. Lev, K. Nandi, A. V. Zima, C. A. Pasternak. A novel explanation for fluctuations of ion current through narrow pores. FASEB J. 1997, 11, 600.

[2] Kasianowicz, J. J. Brandin, E. Branton, D. Deamer, D. W, Proc. Characterization of individual polynucleotide molecules using a membrane channel. Natl. Acad. Sci. USA. 1996, 93, 13770.

[3] Zuzanna Siwy, Elizabeth Heins, C. Chad Harrell, Punit Kohli, Charles R. Martin. Conical-nanotube ion-current rectifiers: the role of surface charge. Journal of the American Chemical Society. 2004, 126, 10850.

[4] Pavel. Yu. Apel. Effect of nanopore geometry on ion current rectification. Nanotechnology. 2011, 22, 175302.
[5] Siwy. Z. Ion-Current Rectification in Nanopores and Nanotubes with Broken Symmetry. Adv. Funct. Mater. 2006, 16, 735.
[6] Hirofumi Daiguji, Yukiko Oka, Katsuhiro Shirono. Nanofluidic diode and bipolar transistor. Nano Letters. 2005, 5, 2274.
[7] I. Vlassiouk, Z. S. Siwy. Nanofluidic diode. Nano Lett. 2007, 7, 552.
[8] I. Vlassiouk, T. R. Kozel, Z. S. Siwy. Biosensing with nanofluidic diodes. J. Am. Chem. Soc. 2009, 131, 8211.
[9] Sung-Wook Nam, Michael J. Rooks, Ki-Bum Kim, Stephen M. Rossnagel. Ionic field effect transistors with sub-10 nm multiple nanopores. Nano Letters. 2009, 9, 2044.
[10] Ye Ai, Jing Liu, Bingkai Zhang, Shizhi Qian. Ionic current rectification in a conical nanofluidic field effect transistor. Sensors and Actuators B: Chemical. 2011, 157, 742.
[11] Liuxuan Cao, Wei Guo, Yugang Wang, Lei Jiang. Concentration-gradient-dependent ion current rectification in charged conical nanopores. Langmuir. 2012, 28, 2194.
[12] L.-H. Yeh, F. Chen, Y.-T. Chiou, Y.-S. Su. Anomalous pH-Dependent Nanofluidic Salinity Gradient Power. Small, 2017, 13, 1702691.
[13] Chih-Yuan Lin, Li-Hsien Yeh, Zuzanna S. Siwy. Voltage-Induced Modulation of Ionic Concentrations and Ion Current Rectification in Mesopores with Highly Charged Pore Walls. The Journal of Physical Chemistry Letters. 2018, 9, 393.
[14] Jyh-Ping Hsu, Shu-Tuan Yang, Chih-Yuan Lin, Shiojenn Tseng. Voltage-controlled ion transport and selectivity in a conical nanopore functionalized with pH-tunable polyelectrolyte brushes. Journal of Colloid and Interface Science. 2019, 537, 496.
[15] Liu, M., Zhang, H., Li, K., Heng, L., Wang, S., Tian, Y. and Jiang, L. A Bio-inspired Potassium and pH Responsive Double-gated Nanochannel. Adv. Funct. Mater, 2015, 25, 421-426.
[16] Jyh-Ping Hsu, Yu-You Chu, Chih-Yuan Lin, Shiojenn Tseng. Ion transport in a pH-regulated conical nanopore filled with a power-law fluid. Journal of Colloid and Interface Science. 2019, 537, 358.
[17] Kalman. E. B, Sudre. O, Vlassiouk. I. Control of ionic transport through gated single conical nanopores. Anal Bioanal Chem. 2009, 394, 413.
[18] Gregorio Laucirica, Waldemar A. Marmisollé, María Eugenia Toimil-Molares, Christina Trautmann, Omar Azzaroni. Redox-Driven Reversible Gating of Solid-State Nanochannels. ACS Applied Materials & Interfaces. 2019, 11, 30001.
[19] Sutka, A.; Malnieks, K.; Lapcinskis, L.; Kaufelde, P.; Linarts, A.; Berzina, A.; Zabels, R.; Jurkans, V.; Gornevs, I.; Blums, J.; Knite, M. The Role of Intermolecular Forces in Contact Electrification on Polymer Surfaces and Triboelectric Nanogenerators. Energy Environ. Sci. 2019, 12, 2417−2421.
[20] Gouy, M. Sur La Constitution De La Charge Electrique a La Surface D'Un Electrolyte. J. Phys. Theor. Appl. 1910, 9, 457−468.

[21] Chapman, D. L. A Contribution to the Theory of Electrocapillarity. Philos. Mag. 1913, 25, 475−481.
[22] Stern, O. The Theory of the Electric Double Layer. Electrochemistry 1924, 30, 508.
[23] P. Ramirez, S. Mafe. Pore structure and function of synthetic nanopores with fixed charges: tip shape and rectification properties. Nanotechnology. 2008, 19, 315707.
[24] Zeng. S, Wen. C, Solomon. P. Zeng. S, Wen. C, Solomon. P, Nat. Nanotechnol. 2019, 14, 1056. Nat. Nanotechnol. 2019, 14, 1056.
[25] Sung-Wook Nam, Min-Hyun Lee, Seung-Hyun Lee, Do-Joong Lee, S. M. Rossnagel, Ki-Bum Kim. Sub-10-nm nanochannels by self-sealing and self-limiting atomic layer deposition. Nano Letters. 2010, 10, 3324.
[26] Yifan Wang, Qi Chen, Tao Deng, Zewen Liu. Self-Aligned Nanopore Formed on a SiO2 Pyramidal Membrane by a Multipulse Dielectric Breakdown Method. The Journal of Physical Chemistry C. 2018, 122, 11516.
[27] He, Y. H, Tsutsui, M, Fan, C, Taniguchi, M. & Kawai, T. Controlling DNA translocation through gate modulation of nanopore wall surface charges. ACS Nano. 2011, 5, 5509–5518.
[28] Ai, Y., Liu, J., Zhang, B. K. & Qian, S. Field effect regulation of DNA translocation through a nanopore. Anal. Chem. 2010, 82, 8217–8225.
[29] Jou, I. A., Melnikov, D. V., McKinney, C. R. & Gracheva, M. E. DNA translocation through a nanopore in a single-layered doped semiconductor membrane. Phys. Rev. E. 2016, 86, 061906.
[30] Yifan, L. & Levent, Y. Slowing DNA translocation in a nanofluidic field-effect transistor. ACS Nano. 2016, 10, 3985–3994.

6

Conclusions

6.1. SUMMARY OF ACHIEVEMENTS

This thesis focuses on the controllable fabrication of single-crystal solid-state silicon nanopores with extremely small sizes using the TSWE method and proposes an ionic field-effect transistor based on these nanopores. Additionally, the ionic current characteristics of these devices were thoroughly studied, enabling applications in nano-mask lithography and biosensing. The main achievements of the study are as follows:

Mechanism and Factors Affecting Nanopore Fabrication: The formation mechanism of nanopores through wet etching was analyzed based on the atomic-layer structure of single-crystal silicon. The relationship governing size variation during the etching process was summarized, and key factors influencing nanopore fabrication were identified.

Quantitative Model and Controllable Nanopore Fabrication: A model of the nanopore microfluidic channel was developed, and the quantitative relationship between nanopore size and ionic current during the wet etching process was established. This enabled the precise fabrication of 10 nm nanopores. Using this method, a single-crystal silicon nanoslit with a feature size of 3 nm was fabricated for the first time.

Etch-Stop System Using Electrochemical Passivation: By heavily doping silicon with boron, the width of the potential barrier at the silicon-liquid interface was adjusted to reduce the etching rate. Electrochemical passivation using a three-electrode system was then employed to control the growth of nanoscale porous SiO_x at the solid-liquid interface via passivation voltage, achieving a controllable etch-stop mechanism. By combining heavy doping and electrochemical passivation, a complete etch-stop system was established, enabling the controllable fabrication of sub-10 nm nanopores using the TSWE method. This system offers the potential for prototyping and mass production.

Development of Ionic FETs Based on Silicon Nanopores: The fabricated nanopores were integrated with metal electrodes as gates, enabling three-dimensional control of the nanochannel (nanopore channel) to form an ionic FET. By adjusting the gate voltage, the surface charge density at the silicon interface was modulated, achieving surface charge inversion. This allowed for precise regulation of the I-V characteristics, facilitating transitions between Ohmic and bipolar diode regimes.

Applications in Nano-Mask Lithography and Biosensing:

Biosensing: The fabricated nanopores were used to detect biomolecules (ssDNA) by monitoring ionic current blockages caused by molecular translocation. Techniques such as surface charge modulation via gate voltage and enhanced electroosmosis were explored to reduce the translocation rate and improve detection success rates.

Nano-Mask Lithography: The nanopores were utilized as hard masks in focused ion beam lithography, successfully achieving precise and reproducible pattern transfer. The high fidelity and accuracy of this method demonstrated the effectiveness of solid-state nanopores on single-crystal silicon substrates as nanopatterning tools, showcasing their potential for applications requiring nanoscale pattern precision.

6.2. RESEARCH OUTLOOK

Building on the achievements and insights from this thesis, future research can be focused on but not limited to the following aspects:

1 Fundamental Studies on Ion Transport

-Exploration of Extreme Conditions: Investigating ion transport under extreme conditions, such as mixed electrolytes, or confinement within nanopores of extremely small dimensions (Angstrom-scale), is crucial for uncovering the nuanced interplay between physical and electrochemical phenomena. These studies could reveal non-classical transport behaviors and deviations from established models like the Poisson–Nernst–Planck equation, leading to a deeper understanding of nanoscale ionic conduction.

-Coupled Effects in Nanopores: Future research should focus on the coupled effects of ion hydration, surface charge interactions, and EDL overlap in these extreme regimes. Such studies will shed light on phenomena like steric effects, and selective ion transport, which are essential for tuning the performance of nanopore-based devices.

2 Advancing Fabrication Techniques

-Scalability and Reproducibility: While the TSWE method demonstrated controllable fabrication of sub-10 nm nanopores, scaling this approach for high-throughput production remains a challenge. Future research could focus on integrating TSWE with advanced automation and feedback systems to enhance yield and reproducibility on industrial scales.

-Precision Control: Techniques like real-time monitoring using ionic currents or advanced machine-learning-based predictive models could further refine the precision of nanopore fabrication, enabling tailored structures for specific applications.

3 Enhancing Device Functionality

-Optimized Ionic FET Design: Future studies could explore alternative gate materials and insulating layers with higher permittivity to extend the modulation range of ionic FETs. This would facilitate stronger rectification effects and broaden their application scope, particularly for energy storage and conversion.

-Multi-Pore Systems: Scaling up from single nanopores to arrays or networks could unlock applications in parallel processing for biosensing, filtration, and ionic circuits. Research into optimizing the interconnectivity and uniformity of such systems is needed.

ACKNOWLEDGEMENTS

As I write the final words of this dissertation, I cannot help but look back on the five-year journey of my PhD with deep emotion. This path of scholarship has been filled with countless challenges and setbacks, also with indescribable joy, gratitude, and growth.

First and foremost, I would like to express my heartfelt thanks to my two promotors, Prof. Lina and Kouchi. It was their support and trust that gave me this invaluable opportunity to pursue a PhD at one of the world's finest universities—Delft University of Technology. I am truly honored to have studied under their guidance.

I am especially grateful to my supervisor, Prof. Zewen Liu from Tsinghua University. Since 2018, when I first joined his group, he has not only guided me academically, but also supported me immensely in my personal life. His patient mentorship and personal example have served as a beacon on both my academic and life journeys. There is a well-known Chinese saying: "Once a teacher, always a father." I will always consider myself incredibly fortunate to have such a teacher in my life.

I would also like to sincerely thank all the teachers, colleagues, and friends who have helped me throughout my PhD journey. My thanks go to Jianwen Sun, Yulong Zhang, Minjie Ye, Jiangtao Wei, Xin Lei, Jiayan Zhang, and Yang Zhang from the liulab at Tsinghua University. Your encouragement and companionship brought warmth and joy during the most difficult times of this academic journey. The time spent with you will always remain among my fondest memories. Furthermore, I am also thankful to Yaqian Zhang, Xinrui Ji, and Rui Guan, among others, for their kind help during my time in the Netherlands. I am especially grateful to the engineers at the Tsinghua University Micro and Nano Fabrication Platform for their valuable assistance with my experiments.

My sincere appreciation goes to the members of my defense committee: Prof. Jansen, Prof. French, and Prof. Steeneken from TU Delft, Prof. Xuejun Fan from Lamar University, and Dr. Sten. Thank you all for taking the time to review my thesis and provide your insightful comments.

Finally, and most importantly, I want to thank my parents. Thank you for bringing me into this beautiful world and for raising me with endless love and sacrifice. To my wife, Yurong Liu, I am forever grateful for your unwavering support and quiet strength. Your love and dedication have propelled me to reach ever higher and go ever further.

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LIST OF PUBLICATIONS

Journal articles

1. **H. Hong**, X. Lei, J. Wei, Y. Zhang, Y. Zhang, J. Sun, G. Zhang, P. M. Sarro, Z. Liu, *Investigation on fabrication of silicon nanopores using an electrochemical passivation etch-stop strategy*. Microsyst Nanoeng. 2025. (accept)
2. X. Lei, J. Zhang, **H. Hong**, Z. Liu, Y. Huang, F. Xia, L. Mao, L. Jiang, *Ultrahigh-Performance Osmotic Power Generation in Gate-Controlled Nanopores*. Adv. Funct. Mater. 2025, 2500989.
3. Jiangtao Wei, **Hao Hong**, Xing Wang, Xin Lei, Minjie Ye and Zewen Liu. *Nanopore-based sensors for DNA sequencing: a review*. Nanoscale. 2024, 16, 18732-18766.
4. **H. Hong**, X. Lei, J. Wei, Y. Zhang, Y. Zhang, J. Sun, G. Zhang, P. M. Sarro, Z. Liu, *Rectification in Ionic Field Effect Transistors Based on Single Crystal Silicon Nanopore*. Adv. Electron. Mater. 2024, 10, 2300782.
5. X. Lei†, Jiang, Z†, **H. Hong**†, Wei, Z. Liu, L. Jiang, *Controllable Fabricati on and Rectification of Bipolar Nanofluid Diodes in Funnel-Shaped Si3N4 Nan opores*. Small. 2023, 19, 2303370.
6. **Hong, H**, Wei, J, Lei, X. *et al. Study on the controllability of the fabrication of single-crystal silicon nanopores/nanoslits with a fast-stop ionic current-monitored TSWE method*. Microsyst Nanoeng. 2023, 9, 63.
7. Lei, X. Zhang, J. **Hong, H**. Yuan, Z. Liu, Z. *Controllable Shrinking Fabrication of Solid-State Nanopores*. Micromachines. 2022, 13, 923.

Conference papers

1. **H. Hong**, L. Ye, K. Li, P. M. Sarro, G. Zhang and Z. Liu, "*Fabrication of Nanoslits with (111) Etching TSWE Method*"2021 IEEE 16th International Conference on Nano/Micro Engineered and Molecular Systems (IEEE NEMS), Xiamen, China, 2021.
2. Li Ye, **Hao Hong**, and Zewen Liu, "*Fabrication of single-crystal silicon nanoslits with feature sizes down to 4 nm and high length-width ratios*" 33rd IEEE International Conference on Micro Electro Mechanical Systems (IEEE MEMS), Vancouver, 2020.

Patents

1. Zewen Liu, **Hao Hong**. Method for fabricating nanopores, nanopore structure, and single nanopore sensor. ZL2021 1 1588323.3 (2023).
2. Zewen Liu, **Hao Hong**. Method for fabricating nanopore arrays and nanopore array sensors. ZL2021 1 1587794.2 (2024).
3. Jianwen Sun, **Hao Hong**. A biomolecular sensor based on a GaN transistor and the fabrication method. ZL2023 1 1513538.8(2024).

-Chinese innovation patents