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Ultra-Low-Power Graphene-Nanoribbon-Based Current-Starved Ring Oscillator

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***Abstract*—Identifying methods to further push the boundaries of existing low-power designs has gained new traction, driven by the wide-scale use of large language models. Graphene is well-suited for ultra-low-power nano-electronics due to its exceptional characteristics like ballistic transport, flexibility, and bio-compatibility. In this paper we investigate the feasibility of using ultra-low-voltage GNR structures, in conjunction with power reduction techniques to implement a GNR-based current-starved ring oscillator. By exploiting their low operating voltage and attofarad range intrinsic capacitances we achieve a $1.89\times$ higher output frequency while simultaneously reducing the power consumption by $553.8\times$ and achieving a $812\times$ higher power efficiency.**

***Index Terms*—GNR, graphene, current-starved, ring oscillator, low-power.**

I. Introduction

In the current technological environment, which is defined by the integration of CMOS and emerging technologies for portable ultra-low-power electronic devices, there is a continuous effort to assess the advantages of transitioning from power-intensive, robust, and resilient CMOS-based circuits to the energy-efficient emerging technology alternatives.

Graphene has emerged as a highly promising material for ultra-low-power nano-electronics, owing to its exceptional characteristics such as ballistic transport, flexibility, and bio-compatibility [1, 2]. These unique properties have spurred the exploration of graphene nanoribbons (GNR) based Boolean logic gates together with spiking and McCulloch-Pitts and spiking neurons and synapses [3–9]. In [3], a comparative analysis was conducted between GNR-based logic gates (GNR-L) and $7\,\mathrm{nm}$ FinFET CMOS counterparts. Simulation results show that GNR-L offers two orders of magnitude lower power consumption, six times lower propagation delay, and two orders of magnitude active area reduction. Moreover, [10] proposed a GNR-based 5-bit DAC achieving comparable INL and DNL performance to that of the FinFET variant, i.e., DNL of [-0.196, 0.088] LSB and INL of [-0.809, 0.364] LSB, while operating at only $0.2\,\mathrm{V}$.

The existence of a clock source is necessary both in the digital domain, i.e. clock source for the CPU, implementing timers, memory access, etc., as well as in the analog domain for A/D and D/A data converters, PLLs, monitoring process variation etc. Ring oscillators are favored for their ability to provide a wide tuning range, compact layout, fast startup, and the versatility to generate multiple phases simultaneously [11].

In this paper, we build upon the current source developed in [10] and the GNR structures developed in [9] to design and implement an ultra-low-power GNR-based current-starved oscillator. When supplied at $0.2\,\mathrm{V}$, the GNR oscillator exhibits a power consumption of less than $1\,\mu\mathrm{W}$ at a maximum frequency of $88.4\,\mathrm{GHz}$. By contrast with classical CMOS ring oscillator implementations, determining the propagation delay which characterizes a stage requires us to determine the value of the quantum capacitance associated with the graphene layer in addition to the well understood insulator capacitance of the backgate. The calculation of the quantum capacitance was integrated in the existing conductance computation algorithm and returns a capacitance value which accounts for both the GNR device's geometry as well as the bias conditions it is subjected to for each individual timestep of the simulation.

Our simulation results after accounting for both these capacitances indicate three orders of magnitude lower power consumption for the GNR design when compared with a $7\,\mathrm{nm}$ FinFET counterpart.

The rest of this paper has the following structure: Section II presents an overview of related work on graphene, GNR conductance computation, GNR simulation methodology, logic circuits using GNRs, and current-starved oscillators. Section III describes the GNR-based current-starved oscillator concept. Section IV presents the results of our simulations for the GNR and FinFET oscillators and compares their performance. Finally, the paper ends with some concluding remarks in Section V.

II. Background

This section provides ring oscillator background, highlighting the current-starved topology, as well as insight about GNR devices and their simulation framework.

A. Basic ring oscillators

Given the most rudimentary ring oscillator, the frequency f can be determined knowing the number of stages N, and the propagation delay of each stage t_d using Equation 1. Furthermore, if the load capacitance of the inverter, C_L, the activity factor, α, and the supply voltage, V_{supply}, are known,

then we can approximate the power consumption of the circuit using Equation 2.

$$f = \frac{1}{2 \cdot N \cdot t_d} \tag{1}$$

$$P = \alpha \cdot N \cdot C_L \cdot V_{supply}^2 \cdot f \tag{2}$$

The main drawback of this implementation is the variability induced by t_d into the oscillation frequency, which will vary linearly with V_{supply} and non-linearly through drain currents I_{PMOS} and I_{NMOS} against process, temperature and V_{supply} variations, as shown in Equation 3.

$$t_d \approx \ln(2) \cdot \frac{C_L \cdot V_{supply}}{2} \cdot \left(\frac{1}{I_{PMOS} + I_{NMOS}} \right) \tag{3}$$

B. Current-starved ring oscillators

The propagation time variability can be partially mitigated using the current starving technique. This works by enforcing a maximum current, I_{bias}, through the inverter's transistors by adding a current source in series and yields Equation 4. Equation 2 remains applicable for calculating power consumption.

$$f = \frac{I_{bias}}{2 \cdot N \cdot C_L \cdot V_{supply}} \tag{4}$$

C. GNR based devices

Configuring the geometrical parameters of the generic non-rectangular GNR-based device, illustrated in Figure 1, allows us to induce a bandgap and achieve various analog behaviors.

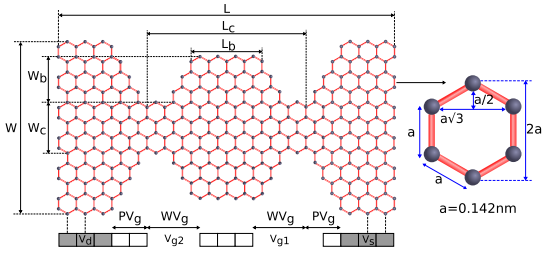
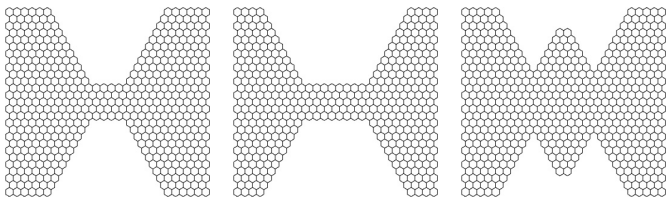


Fig. 1: GNR Geometry Description Parameters [12].

A set of three GNR geometries, capable of fulfilling the roles of current source and low-side and high-side switches [9] is illustrated in Figure 2. The exact structure geometries, identified through iterative conductance map plot evaluations [3], are detailed in Table I.



(a) GNR_{ISRC} (b) GNR_{DOWN} (c) GNR_{UP}

Fig. 2: Graphene-based device topologies

TABLE I: Dimensions of GNR structures [9]

	(W,L)	(W_c,L_c)	$(W_b,\ L_b)$	$(P_{V_G},\ W_{V_G})$
GNR_{ISRC}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(2\sqrt{3}, 6\sqrt{3})$
GNR_{UP}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(9, 2\sqrt{3})$	$(12\sqrt{3}, 6\sqrt{3})$
GNR_{DOWN}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(3\sqrt{3}, 6\sqrt{3})$

D. Simulation framework

The assessment of the GNR-based circuits is conducted using a hybrid simulation framework that combines Cadence Spectre's mixed-signal environment with Matlab's parallel computing toolbox. This co-simulation methodology enables SPICE-level circuit simulations alongside precise atomistic-level GNR computations in Matlab.

To calculate the electronic transport properties of GNRs, we use the tight-binding Hamiltonian approach to characterize their structure. Additionally, the Non-Equilibrium Green Function (NEGF) quantum transport model is applied to solve the Schrödinger equation and, using the Landauer formalism, compute the GNRs' conductance [13, 14] using Equation 5.

$$G = \frac{q \cdot \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E - \mu_1) - f_0(E - \mu_2)) dE}{h \cdot (V_d - V_s)}, \tag{5}$$

where q is the electron charge, h is the Planck constant, $T(E)$ is the transmission function, $f_0(E)$ is the Fermi-Dirac distribution function at temperature T, and $\mu_{1,2}$ denote the Fermi energy of the source and drain contacts.

In addition, the back-gate's insulator capacitance, C_{ins}, and the graphene's quantum capacitance, C_{ins}, should be determined to generate accurate transient simulation results.

The insulator capacitance, C_{ins}, can be modelled using the fundamental parallel plate capacitor equation where we provide the equivalent permittivity μ_{eq}, the oxide thickness, t_{ox}, and the area of the GNR device, A_{gnr}.

The quantum capacitance, C_q, is then calculated using Equation 6 by integrating the product of the density of states, $DOS(E)$, and the thermal broadening function, $F_T(E)$, over all energy levels E [15, 16]. This determines the quantum capacitance based on the distribution of energy states.

$$C_q = q^2 \int_{-\infty}^{+\infty} \mathrm{DOS}(E) \cdot F_T(E - (\mu_1 - \mu_2))\, dE \tag{6}$$

III. Designing a GNR-based current-starved ring oscillator

In this section we present the proposed GNR-based and FinFET current-starved ring oscillator and discuss its functionality.

A. GNR-based and FinFET oscillator stage

The implementations of the ring oscillator stages using GNR-based devices and FinFETs together with a 5-bit DAC used for frequency tuning are depicted in Figure 3.

The reason for the DAC's presence is the lack of an $180°$ phase-shift at low frequency for signals propagating from the

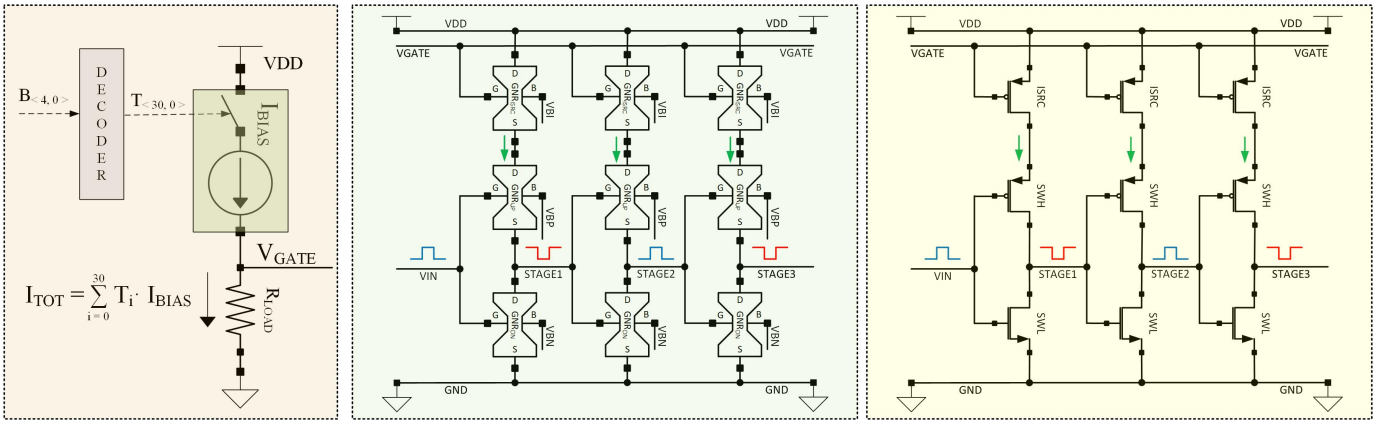


Fig. 3: a) 5-bit DAC (left) for frequency tuning b) GNR-based (middle) and FinFET (right) ring oscillator sections

gate to the *drain* terminal of the GNR device shown in Figure 2a. An immediate consequence is that a classic current mirror configuration cannot be used to implement a current source.

To overcome this limitation we propose modulating the current through the GNR device by driving its gate using the output voltage of the previously developed 5-bit DAC [10].

By contrast, a classic current mirror could be used for the FinFET implementation, but the granularity provided by the already implemented 5-bit FinFET DAC is sufficient for trimming the ring oscillator's frequency. Moreover, while a current mirror can achieve very high mirroring precision in CMOS, deep sub-micron devices provide weak output resistance that negates the advantage of using mirrors.

To avoid doubling the device count of the proposed design, we chose to apply current starving only to the high side of the inverter. The absence of an NMOS current source equivalent on the low side of the inverter stages will result in the overall propagation delay (t_d) being primarily influenced by the I_{PMOS} term during the rising edge of the output signal. This will be complemented by a rapid falling edge of negligible duration generated by the I_{NMOS} term.

A disadvantage of using a current DAC to configure the ring oscillator is the quiescent current consumption of the active current sources which reaches a maximum of $31 \cdot I_{bias}$ for the maximum DAC input code. This quiescent current can be eliminated by adding a storage capacitor for sampling the analog value applied to V_{gate} and disconnecting it with a GNR device similar to that used for the access transistors in the GNR-based SRAM presented in [3].

B. GNR current-starved ring oscillator

The complete implementation of the GNR-based current-starved ring oscillator is shown in Figure 4 and is comprised of 8 inverter-like stages. The last 180° phase shift is ensured by a GNR NAND gate which constitutes the circuit's enable. The oscillator's frequency can be modulated by adjusting the current DAC input code, which, in turn, regulates the gate voltage of the current source device.

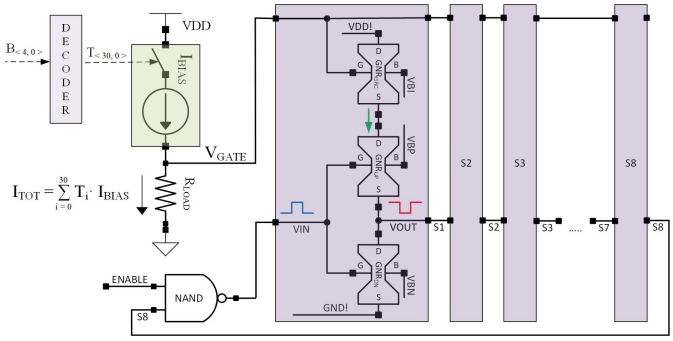


Fig. 4: GNR-based current-starved ring oscillator

IV. Results

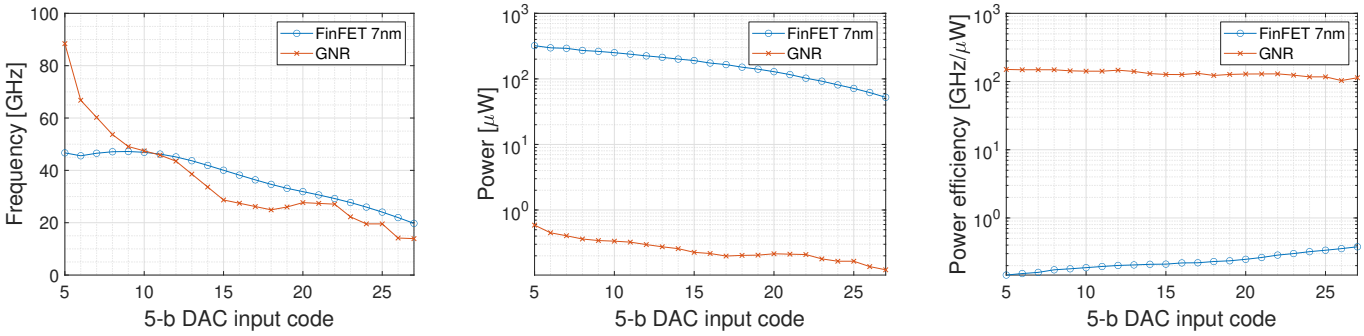
The simulation framework outlined in II-D was utilized to assess the performance of the proposed GNR-based current-starved oscillator, while SPICE simulations were employed to evaluate the operation of the FinFET-based counterpart.

The simulation results obtained for the GNR-based and FinFET ring oscillators are compared in terms of frequency range, power consumption, and power efficiency. The variation of these three parameters with the DAC's input code is presented in Figure 5.

The code range applied at the input of the DAC is intentionally limited, given that for the lower range of V_{gate} voltages the FinFET PMOS device would enter the linear region and compromise current starving. Similarly, the upper range of V_{gate} would cause the device to enter the cut-off region.

Reviewing the results from Table II, we observe that the oscillation frequencies of the GNR-based and 7 nm FinFET-based ring oscillator implementations are closely matched. This resemblance can be attributed primarily to the relatively low 1.2 µA current flowing through the GNR device.

When comparing the GNR-based and 7 nm FinFET-based implementations, the GNR starved ring oscillator demonstrates significantly lower power consumption, nearly three orders of magnitude less, thanks to its smaller parasitic capacitances.



(a) *Frequency* (b) *Power* (c) *Power efficiency*

Fig. 5: Performance comparison of GNR-based and 7 nm FinFET ring oscillators: a) frequency, b) power, c) power efficiency

This leads to nearly three orders of magnitude superior power efficiency despite similar oscillation frequencies.

TABLE II: GNR-based vs. FinFET ring oscillator results

	Frequency [GHz]	Power consumption [µW]	Power efficiency [GHz/µW]
FinFET	19.7 - 46.7	52.2 - 321.2	0.14 - 0.40
GNR	13.9 - 88.4	0.12 - 0.58	113.7 - 150.4

V. Conclusion

In this paper, we investigated the potential of GNR devices to implement high-frequency ultra-low-power internal oscillators for multi-technology ICs. We explored the frequency range over which we can tune the oscillator by driving the gate of the current source GNR-based device. The dynamic power consumption was reduced by applying the current starving technique to the ring oscillator topology. The proposed GNR-based design was compared with a 7 nm FinFET counterpart and achieved a $1.89\times$ higher output frequency while simultaneously reducing the power consumption by $553.8\times$ and achieving a $812\times$ higher power efficiency.

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