A 0.5-3 GHz I/Q Interleaved Direct-Digital RF Modulator with up to 320 MHz Modulation Bandwidth in 40 nm CMOS

Shen, Yiyu; Bootsman, Rob; Alavi, Morteza S.; De Vreede, Leonardus

DOI
10.1109/CICC48029.2020.9075949

Publication date
2020

Document Version
Final published version

Published in
2020 IEEE Custom Integrated Circuits Conference, CICC 2020

A 0.5–3 GHz I/Q Interleaved Direct-Digital RF Modulator with up to 320 MHz Modulation Bandwidth in 40 nm CMOS

Yiyu Shen, Rob Bootsman, Morteza S. Alavi, Leonardus de Vreede
Electronic Circuits and Architectures (ELCA) Research Group, Delft University of Technology

***Abstract*—This paper presents a wideband, 2×12-bit I/Q interleaved direct-digital RF modulator (DDRM) realized in 40 nm CMOS technology. The proposed digital-intensive quadrature up-converter features an advanced I/Q-mapping unit cell to boost RF power, in-band linearity, and out-of-band spectral purity. The modulator provides more than 14 dBm RF peak output power. It achieves an ACLR of -52 dBc and an EVM of -40 dB when applying a 20 MHz 256 QAM signal at 2.4 GHz. When applying a 320 MHz 256 QAM signal at 2.4 GHz, the measured ACLR and EVM are better than -43 dBc and -32 dB, respectively, without applying any digital pre-distortion.**

***Index Terms*—DDRM, RFDAC, quadrature up-converter , IQ-Mapping, Digital-Intensive Transmitter, DPD-free.**

I. Introduction

The ever-increasing demand for fast data access and high throughput is driving wireless communication towards its 5th generation, which utilizes larger modulation bandwidth and MIMO operation while demanding higher system efficiency and integration. To address this demand, in recent years, extensive research has been directed towards digital-intensive transmitters (TXs). The key building block of these architectures is the RF modulator, which can be realized as either a Cartesian (I/Q) modulator or its polar counterpart. Due to the linear summation of the in-phase (I) and quadrature (Q) signals, an I/Q digital transmitter (DTX) is the best candidate to handle the large modulation bandwidth of a 5G mobile network. In view of this, among several I/Q DTX architectures, the direct-digital RF modulators (DDRM) are rapidly gaining interest due to their natural compatibility with nanoscale CMOS, small chip area, potential to offer high output power, excellent spectral purity, and frequency-agile operation [1]-[4]. Fig. 1(a) depicts a conventional DDRM, which comprises a pair of current-steering I/Q mixing DACs. In this context, the unsigned complementary I and Q baseband signals are first digitally interpolated to adequately suppress sampling spectral replicas and locate them further away from the original complex modulated baseband signal (i.e. digital low-pass filter operation). Next, they are up-converted by two pairs of 50 % complementary quadrature clocks. The resultant high-speed bit-streams are subsequently converted into two separate I/Q RF signals by exploiting current-steering (mixing) DACs. Eventually, they are combined in an analog fashion by hardwiring their I and Q RF signals. Unfortunately, existing DDRMs still suffer from the following limitations.

First, as discussed and shown in Fig. 1(a), conventional DDRMs are typically realized using two (separate) banks of current-steering mixing-DACs, just like analog up-converters,

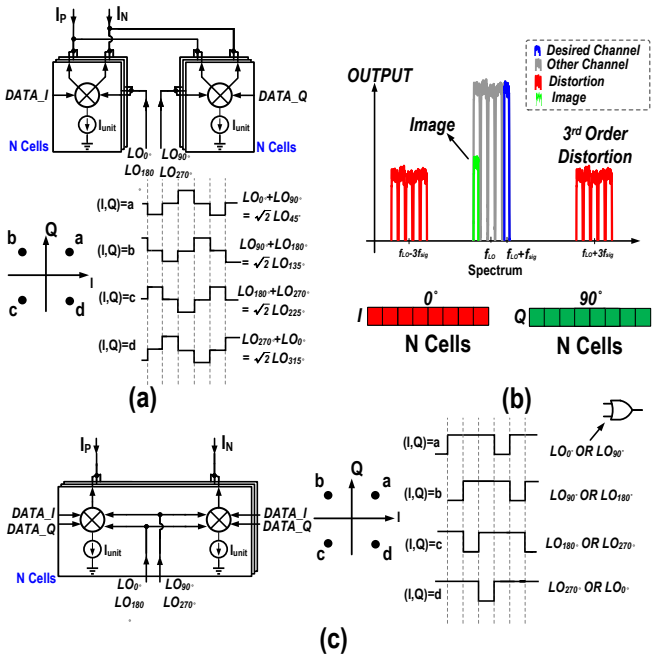

Fig. 1. (a) Conceptual diagram of conventional DDRMs ([1]); (b) its spectrum; (c) Conceptual diagram of the IQ-interleaving DDRM ([2]).

which exhibit I-Q mismatch that results in an unwanted IQ-image component [1]. To address this issue, [5] proposed an IQ-sharing topology whose I and Q banks can share the same unit cell. However, this technique requires 25 % quadrature clocks, which, in turn, generate less RF power. Moreover, when driven with 50 % quadrature clocks effectively ternary-state up-converted current pulses with 75 % duty cycle are generated that causes I-Q interaction which degrades in-band linearity and out-of-band signal purity especially for wideband signals (Fig. 1(b)).

Second, while the IQ-interleaving DDRM concept introduced in [2] improves odd-order distortion and IQ image rejection, it also uses two separate current-mode XOR/XNOR complementary IQ banks with distinct current sources to generate its differential RF output signal (Fig. 1(c)). Any mismatch among these current sources contributes to even-order distortion [2]. Furthermore, its bit-wise XOR operation of the I/Q vectors produces binary output current pulses with a 75 % duty-cycle. This exacerbates the impact of the finite settling times for the unit-cells, which limits the achievable spectral purity for wideband signals.

978-1-7281-6031-3/20/$31.00 ©2020 IEEE

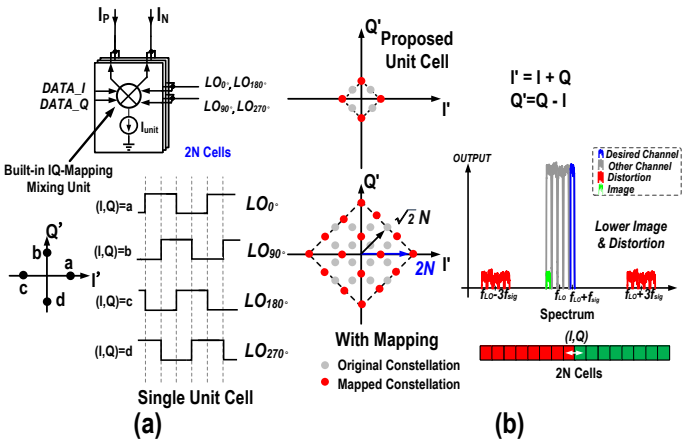

Fig. 2. The proposed IQ-mapping DDRM: (a) conceptual diagram; (b) its constellation diagram and spectrum.

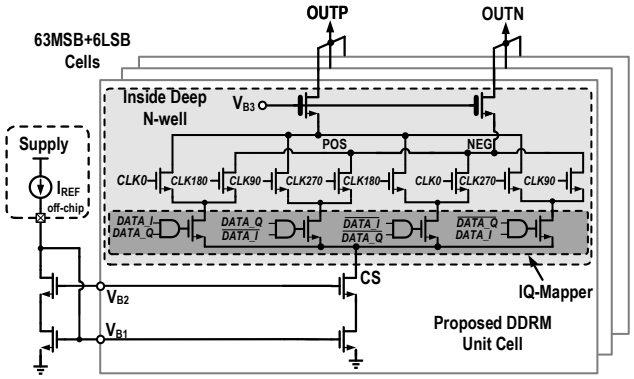

Fig. 3. The detailed unit-cell schematic of the proposed DDRM.

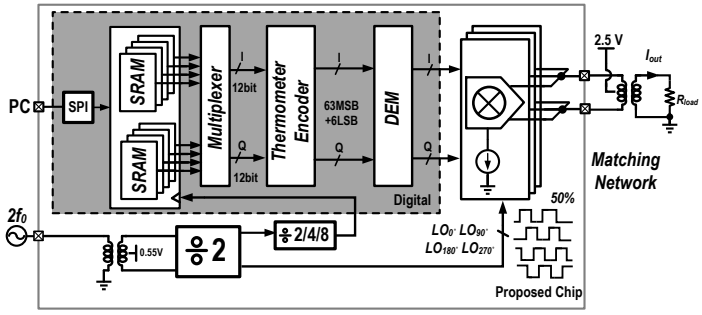

Fig. 4. The block diagram of the proposed DDRM.

II. IQ-Mapping Techniques

To improve DDRM performance in terms of modulation bandwidth, RF output power, and most importantly, spectral purity, this work presents a novel wideband "unsigned" IQ-mapping DDRM, which consists of an IQ mixing-DAC whose unit-cells generate binary up-converted current pulses with 50 % duty-cycle at the highest current levels. To achieve this, the original square-shaped four-point constellation (diagonal points) of prior art DDRMs is mapped into a diamond-shaped counterpart (orthogonal points). Mathematically, this operation can be viewed as a mapping of the traditional I/Q vectors into two new orthogonal vectors, i.e.(I'=I+Q, Q'=Q-I). Although [6] also introduces a mapping technique for a signed-IQ digital PA that results in an IQ diamond-shape profile, it can suffer from distortion due to the IQ clipping operation, which requires 2-dimensional (2D) digital pre-distortion (DPD). Moreover, the mapping was realized in the digital domain by pre-processing of IQ data prior to the mixing-DAC operation. In contrast, the proposed mapping technique is a linear operation and directly implemented into the unit cell of the proposed DDRM resulting in less signal processing overhead as well as faster data throughput, which enables its use at very high signal bandwidths (Fig.2(a)). Additionally, the generation of binary current pulses with 50 % duty cycle, compared to prior art DDRMs with 75 % current pulses, relaxes settling behavior constraints and also contributes to improved spectral purity for complex modulated signals with large bandwidth. In addition, the proposed unsigned IQ-mapped DDRM in this work allows its full current capability to be used for the orthogonal (outer) constellation points, rather than just the four diagonal corner points, which is the case with the separate I and Q banks of conventional designs as well as the I/Q interleaved DDRM of [2]. In other words, in prior art DDRMs, theoretically, the maximum output current is proportional to $|N+jN| = \sqrt{2}N$. In contrast, in the proposed DDRM, the maximum current capability occurs at orthogonal points, which is proportional to $N + N = 2N$ (Fig. 2(b)), resulting in a 3 dB higher peak RF output power. Consequently, a larger IQ plane area can be addressed with a given current capability, enhancing the output power and efficiency of the proposed unsigned IQ DDRM (Fig. 2(b)). Finally, opposed to prior art DDRMs, the proposed IQ-mapping technique provides lowest I/Q interaction at the highest current levels, which, in turn, improves output signal spectral purity.

III. Circuits Implementation Detail

The operating principle of the proposed unit cell, which is depicted in Fig. 3, can be understood by considering the mapping of the original IQ data by simple AND gates. Here, the bit-wise ANDing of $(DATA\_I,\ DATA\_Q)$, $(\overline{DATA\_I},\ DATA\_Q)$, $(\overline{DATA\_I},\ \overline{DATA\_Q})$, $(DATA\_I,\ \overline{DATA\_Q})$, and subsequent bit-wise multiplication using current-mode XOR/XNOR logic, with 50 % quadrature LO clocks whose phases are 0, 90, 180, and 270 degree, a four-point diamond-shaped constellation diagram is created. In this way, the proposed circuit inherently creates the desired IQ-mapping (i.e. 45-degree rotation respect to the original constellation points) without using any additional clock phases. By using 50 % LO clocks, the duty cycle of the resultant upconverted IQ current pulses is also precisely 50 % at highest current levels. Even more important, in the proposed structure, a single current source is used for generating both the I' and Q' signals, thus minimizing any mismatch problems (Fig. 3).

In each unit cell, a thick-oxide cascode transistor at the top is employed, which boosts the output impedance of the unit cell and enables high output-voltage swings. In each MSB cell, the current source consists of a large transistor (800u/2.5u) to

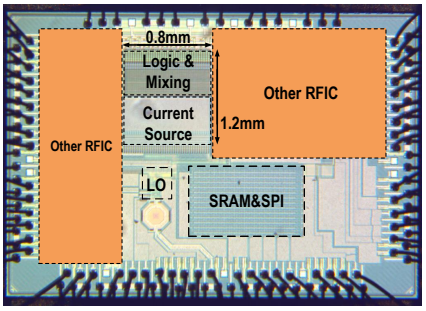

Fig. 5. Chip micro-graph.

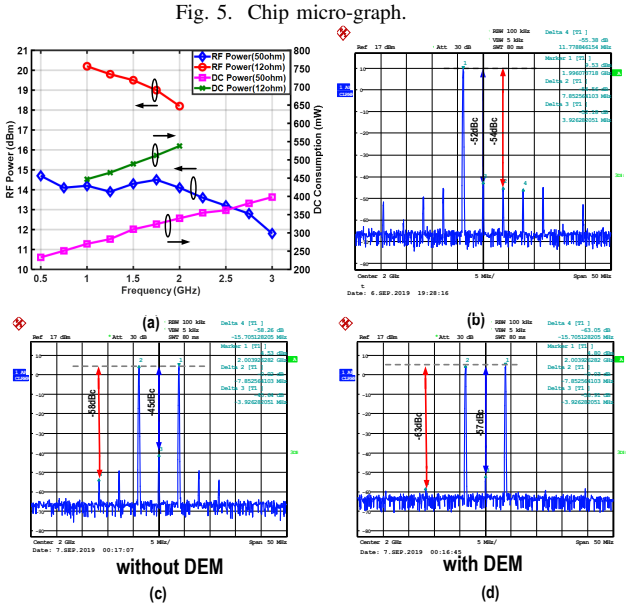

Fig. 6. (a) Measured peak output power and DC power consumption (with 50Ω and 12Ω) vs. frequency; measured spectrum in (b) the single-tone test, (c) the two-tone test when DEM is disabled, and (d) the two-tone test when DEM is enabled.

meet the 12-bit resolution requirement. What's more, in this compact unit cell, thanks to the inherent IQ mapping operation, the current source is always on, which significantly enhances the resulting spectral purity for wideband signals compared with [2].

It is worth mentioning a somewhat similar cell topology has been reported in [7] for a neural recording system while using an offset quadrature phase-shift keying (O-QPSK) modulation with constant amplitude. In our proposed generic high resolution IQ mixing-DAC, however, CMOS AND gates are utilized before the mixing-DAC unit cells to improve the voltage headroom and, thus, to boost the in-band linearity and out-of-band spectral purity.

Fig. 4 depicts the overall system building-block diagram. It features digital-intensive quadrature up-conversion, with all signal processing realized in the digital domain. The TX data is fed to SRAMs using an SPI. To support large modulation bandwidth, four on-chip SRAMs are multiplexed to allow the bit-stream throughput to become equal to a half of the center frequency, f_{LO}. The external LO signal is divided on-chip to generate the required four IQ clock phases, each with 50 % duty-cycle. The 12-bit DDRM is implemented in a segmented structure, with 6 bits thermometer-coded MSBs

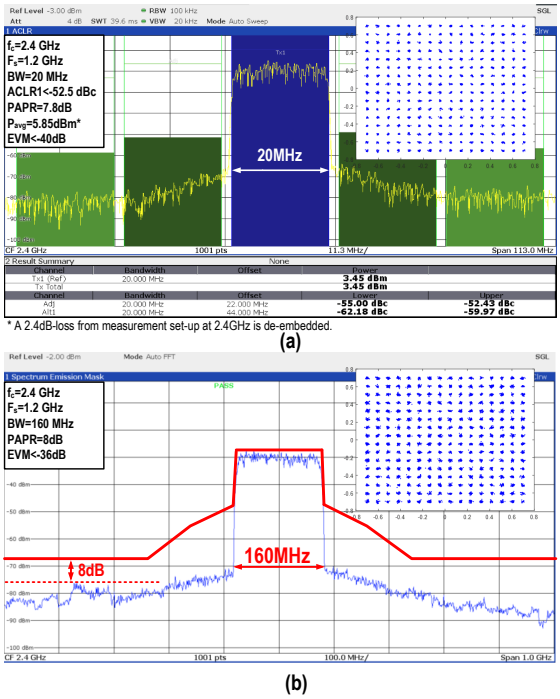

Fig. 7. (a) The measured spectrum and EVM of the 20MHz 256 QAM signal and (b) the measured spectrum and EVM of the 160 MHz 256 QAM signal at 2.4 GHz.

and 6 bits binary-weighted LSBs. Preceding to the proposed unsigned IQ-mapping DDRM, there are thermometer encoders and dynamic element matching (DEM) circuitry. DEM is employed to randomize mismatches toward the goal of improving adjacent channel leakage ratio (ACLR) levels for signals with smaller bandwidths (BW<10 MHz). The output signal of the DDRM is fed to an off-chip matching network, as shown in Fig. 4.

IV. Measurements Results

The proposed DDRM was implemented in a 40 nm CMOS bulk process. It occupies a core active area of 1.1 mm^2 (Fig. 5) excluding the SRAMs and input balun which are only present for testing purpose and shared with other front-end circuitry. Note that in our measurements, we have not used any type of DPD. Fig. 6(a) shows the peak output power P_{out} versus f_{LO} while driving a 50 Ω differential load. At 2 GHz, the peak P_{out} is 14.1 dBm, and the DC power consumption P_{DC} is 340 mW (excluding the testing SRAMs). When the differential load is set to 12 Ω , the peak P_{out} exceeds 18 dBm, and subsequently, the overall system efficiency η can be >24 % at 1 GHz, which indicates the current handling capability of the proposed DDRM when used as a pre-driver stage. At 2 GHz the IQ image and IM3 are lower than -54 dBc and -58 dBc, respectively when DEM is disabled. The IM3 is improved by 5dB thanks to DEM, and Fig. 6(b), (c) and (d) demonstrate the output spectrum of the single-tone and two-tone tests at 2 GHz, respectively.

The performance of the proposed DDRM has also been verified using complex modulated signals with large bandwidth. Fig. 7(a), depicts the spectral purity of a 20 MHz bandwidth

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART MODULATORS

Specification		This Work			[3]	[2]	[4]	[5]	[6]	[8]	[9]
Architecture		IQ-Mapping DDRM			DDRM	DDRM	DDRM	DPA	DPA	Analog	Analog
Technology	[nm]	40			28	40	65	28	40	28	14
Frequency	[GHz]	0.5-3			0.9/2.4	0.9-3.1	0.9-5.2	0.8	2.4	3.3-4.2	0.5-6
Peak P_{out}	[dBm]	14.1/18.2@2GHz[1]			3.5	9.2	15[4]	13.9	27	5[6]	7[6]
DC Power	[mW]	340/540@2GHz[1]			24.8[2]	146[3]	1300[5]	62.5	2230	596	291
f_{LO}	[GHz]	2.4			2.4	3	2.4	0.8	2.4	3.7	3.5
Bandwidth	[MHz]	**20**	**160**	**320**	20	57	20	10	40	200	100
Modulation Type		**256 QAM**	**256 QAM**	**256 QAM**	64 QAM	64 QAM	256 QAM	LTE-10MHz	802.11ac	64QAM -OFDM	Sub-6G NR
ACLR1	dBc	**-52**	**<-48**	**-43**	-47	-44	-42	-32	<-40	<-42	-41
EVM	dB	**-40**	**-36**	**-32**	-36	-30	-42	N/A	<-30	-32	-34
DPD	Y/N	**No**			Yes	No	No	N/A	Yes	N/A	No

[1] Measured at 50Ω and 12Ω, respectively [2] Measured at -3.5dBm Output Power [3]Not include LO generation circuits. [4]Measured at 2.4 GHz [5]Power Consumption at 1G Hz. [6] Average Power.

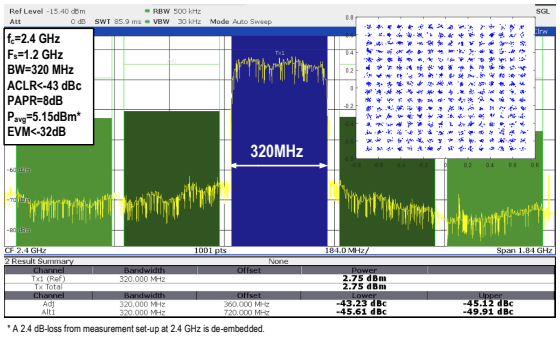

Fig. 8. The measured spectrum and EVM diagram of the 320 MHz 256 QAM signal at 2.4 GHz;

single-carrier 256 QAM signal at 2.4 GHz. With more than 5 dBm average output power and 7.8dB Peak-to-Average Power Ratio (PAPR), it achieves an ACLR of -52dBc and an EVM of -40 dB. The measured spectrum of 160 MHz bandwidth single-carrier 256 QAM signal is shown in Fig. 7(b). The corresponding out-of-band spectral purity is better than -48 dBc while its EVM is better than -36 dB. Finally, in Fig. 8, the spectrum of a 320 MHz bandwidth single-carrier 256 QAM signal with an ACLR better than −43 dBc and the related EVM of −32 dB are shown. The performance of the proposed DDRM is summarized in Table I and compared to that of prior art DDRMs and conventional analog modulators. This chart indicates that the proposed DPD-free DDRM, which operates at frequency bands of 0.5 up to 3 GHz, can achieve superior spectral purity up to 320 MHz signal bandwidth with the peak RF output power of more than 14 dBm.

V. CONCLUSION

In this work, a wideband linear I/Q interleaved DDRM is presented. It features a novel IQ-mapping unit cell to boost the RF output power, in-band linearity, and out-of-band spectral purity. The proposed quadrature RF modulator operates over 0.5–3 GHz frequency range while generating +14 dBm peak RF output power with DC power consumption of only 340 mW at 2 GHz. With more than 5 dBm average output power, the ACLR is better than −43 dBc when applied to a 320 MHz 256 QAM signal. This DDRM, which is realized in 40 nm CMOS process, can act as an energy-efficient driver for the 802.11ax WLAN application or pre-driver of PA in the 5G cellular network.

ACKNOWLEDGMENT

This research was supported by NWO project SEEDCOM and DIPLOMAT. The authors would like to thank Ampleon B.V., and acknowledge contribution of A. Akhnoukh, M. Pelk and Z. Chang for their support. Also, the authors would like to acknowledge Prof. Makinwa, Prof. McCune and M. Mehrpoo in TU Delft for their helpful technical discussions.

REFERENCES

[1] E. Roverato, et al., “All-Digital RF Transmitter in 28nm CMOS with Programmable RX-Band Noise Shaping,” *IEEE ISSCC*,pp. 222-223, Feb 2017.
[2] M. Mehrpoo, et al., “A Wideband linear I/Q-Interleaving DDRM,” *IEEE JSSC*, vol. 53, no. 5, pp. 1361-1373, MAY. 2018.
[3] P. Paro Filho, et al., “A 0.22mm^2 CMOS Resistive Charge-Based Direct-Launch Digital Transmitter with -159 dBc/Hz Out-of-Band Noise,” *IEEE ISSCC*, pp.250-251, Feb. 2016
[4] S. Su, et al., “A 1–5 GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM,” *IEEE Symp. on VLSI Circuits*, 2019
[5] H. Jin, et al., “Efficient Digital Quadrature Transmitter Based on IQ Cell Sharing” *IEEE ISSCC*, pp.168-169, Feb. 2015
[6] Z. Deng, et al., “A dual-band digital-WiFi 802.11a/b/g/n transmitter SoC with digital I/Q combining and diamond profile mapping for compact die area and improved efficiency in 40nm CMOS” *IEEE ISSCC*, pp.172-173, Feb. 2016
[7] Y. Liu, et al., “A 200pJb MUX-Based RF Transmitter for Implantable Multichannel Neural Recording,” *IEEE TMTT*, vol. 57, no. 10, pp. 1361-1373, OCT. 2009.
[8] B. Jann, et al., “A 5G Sub-6GHz Zero-IF and mm-Wave IF Transceiver with MIMO and Carrier Aggregation,” *IEEE ISSCC*, pp.352-353, Feb. 2019
[9] J. Lee, et al., ”A Sub-6GHz 5G New Radio RF Transceiver Supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL in 14nm FinFET CMOS” *IEEE ISSCC*, pp.354-355, Feb. 2019