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Micromachining for Advanced Terahertz
Interconnects and Packaging Techniques at Terahertz Frequencies

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Micromachining for Advanced Terahertz

Maria Alonso-del Pino, Cecile Jung-Kubiak, Theodore Reck, Choonsup Lee, and Goutam Chattopadhyay

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It is difficult to package and interconnect components and devices at millimeter-waves (mm-waves) due to excessive losses experiences at these frequencies using traditional techniques. The problem is multiplied manifold at terahertz (THz) frequencies. In this article, we review the current state of THz packaging and describe several novel techniques. As we will show, micromachined packaging is emerging as one of the best choices for developing advanced THz systems.

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Emerging Applications

Mm-wave and THz frequencies are finding ever-increasing usage in a multitude of areas spanning scientific, military, commercial, defense, security, and biological instrumentation [1]–[4]. The reason for this surge in interest is the specific inherent advantages of mm-wave, sub-mm-wave, and THz frequencies, i.e., larger available bandwidth, compact size, higher spatial resolution for a given antenna size, better temporal resolution, and the reusability of frequencies. These have given rise to a plethora of emerging application areas, such as passive and active imagers (for both close-range and stand-off distances) for security as well as biological, health science, and space-based instrumentation. Very-high-speed wireless communication, which includes 5G and other areas such as indoor Wi-Fi, long-distance line of sight, environmental monitoring, and so on [5], [6], have also been employed.

All of these areas require the development of a high-performance, highly compact system. Any system used for communication, sensing, and imaging requires the synergistic coexistence of hardware and software, and it is no different at mm-wave and THz frequencies. However, implementing the hardware portion of these systems at high frequencies has been challenging. A key obstacle is the availability of low-loss packaging and the integration of components at the system level. A dramatic improvement of component and subsystem technologies at mm-wave and THz frequencies has occurred over the last decade [7]; however, integrating the various components to build a compact, high-performance system remains a challenge.

Traditionally, most of the techniques that address these challenges are similar to the techniques used at microwave frequencies, adapted to higher frequencies. Because of the greater effect of parasitics and mechanical limitations, this did not always result in an acceptable solution. With the recent surge of interest in THz imaging and communications, packaging and interconnect technologies at mm-wave and THz frequencies have been evolving rapidly in recent years. For multifunctional and complex systems, system-on-chip solutions were developed. They have come a long-way at mm-wave frequencies but are still not mature enough at higher mm-waves and THz frequencies. Techniques include system-on-package (SOP), where multichip module and integrated substrate technologies utilizing multilayer processing are employed at mm-waves [8], [9]. Figure 1 displays a few details of the SOP concepts developed by different groups. Due to increased loss at higher mm-wave and THz frequencies, however, low-loss alternatives such as nonradiative dielectric guide (NRD-guide) structures, substrate integrated waveguides (SIWs), and liquid crystal polymer-based multilayer technologies were investigated [10]–[12].

Because of higher dielectric loss at higher frequencies, NRD-guide structures are not practical at THz frequencies.

NRD-guide structures are typically made of dielectric strips that function as waveguides, where two parallel plates clamp the dielectric strips. In recent years, NRD-guide structures have been integrated with other planar transmission lines to develop components such as filters, oscillators, and mixers at mm-wave frequencies. However, because of higher dielectric loss at higher frequencies, NRD-guide structures are not practical at THz frequencies. Conversely, SIW techniques for interconnects and packaging have proved to be very versatile and beneficial due to their ease of integration with monolithic microwave integrated circuits (MMICs) and other components, simple fabrication process, and integration suitability of a wide range of SIW-based components into a single substrate [13]. SIWs, which are similar to metal waveguide

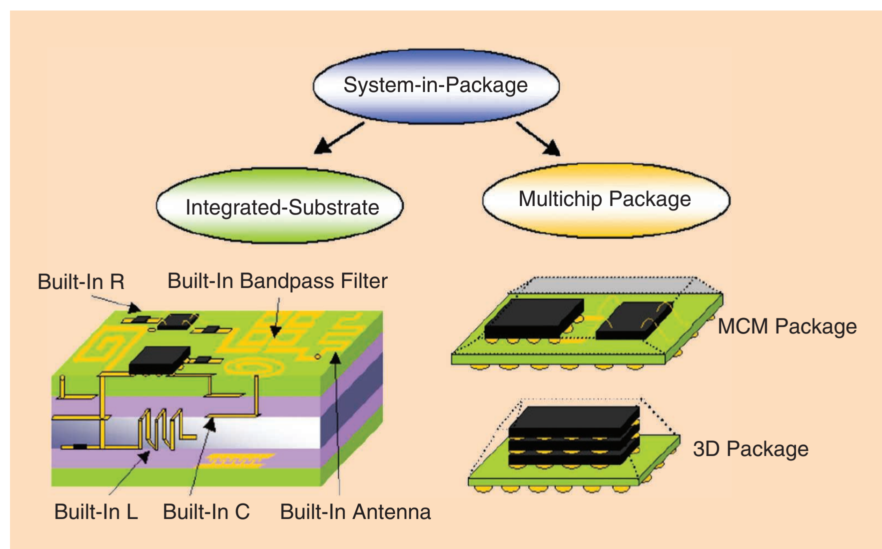

Figure 1. *A schematic of the various SOP technologies currently being investigated [9]. MCM: multichip module; R: resistor; C: capacitor; L: inductor.*

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With MMIC technology, where devices and passive circuits also scale with frequency, microstrip and CPW losses are manageable.

structures, are fabricated using two parallel metal plates connected by two rows of metallic cylinders or slots embedded in a dielectric that fills the two parallel plates. The advantage of this technique is that one can fabricate nonplanar, metallic, waveguide-like structures using planar fabrication techniques. The best feature of SIWs is that they exhibit propagation characteristics including field patterns and dispersion characteristics similar to standard rectangular, metallic waveguides. It is generally difficult, however, to achieve fine conductor geometries that realize trench-filled vias and compact high-performance passive components at frequencies beyond 100 GHz. Nevertheless, the use of advanced, multilayer, thick-film, photo-imageable ceramic technology works at frequencies of up to 200 GHz. With this technique, instead of utilizing standard SIWs with metallic-cylinder vias, advanced, photo-imaged, trench-filled vias form continuous metal side walls, which enables SIWs to provide low loss and extend their frequency of operation [14]. Note that all of the different technologies discussed in this section are limited to up to 100–200-GHz frequency of operations.

Packaging and interconnecting technologies at frequencies beyond 200 GHz still remain challenging. The primary packaging techniques at higher mm-wave and THz frequencies have been metallic,

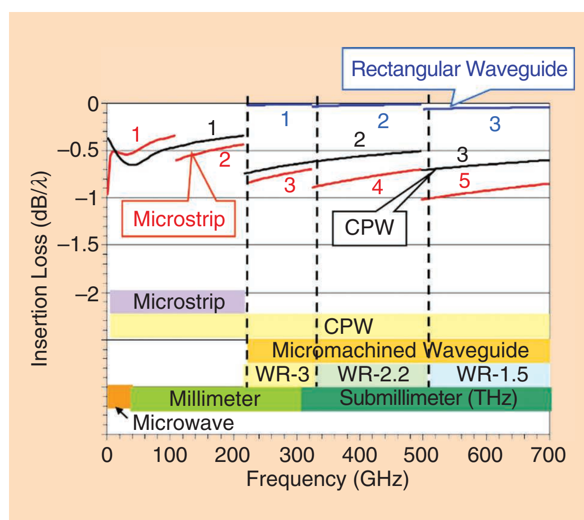

Figure 2. *A comparison of insertion loss normalized by wavelengths between microstrip, CPW, and rectangular waveguides [21].*

waveguide-based architectures, where components are hand assembled in hollow, metal-machined waveguides. Traditionally, these metal waveguides are fabricated using computer numerically controlled (CNC) milling. Not only do these waveguide-based packaging solutions not provide a compact solution for packaging and interconnects; they become complicated and expensive as the system's complexity grows. One of the methods used to address this problem is exploiting vertically stacked component architectures. In this architecture, a 3D arrangement of active and passive components is coupled with micromachined waveguides fabricated on thin layers of metals or substrates. The metal milling of waveguide packaging, preferred at THz frequencies, is not suitable for this architecture because of aspect ratio limitations and the planarity of metal-machined parts [15].

Micromachining has the most potential for developing low-loss packaging and interconnect technologies at higher mm-wave and THz frequencies. There are several micromachining techniques that can be used for THz systems, e.g., permanent thick resists [16], thick-resist electroforming [17], laser micromachining [18], and silicon deep-reactive ion etching (DRIE) [19]. Good results have been reported for all of these various techniques; however, DRIE-based silicon micromachining has exhibited the most potential for solving packaging and interconnect technology at THz frequencies. The waveguide circuits developed using DRIE-based silicon micromachining have demonstrated low loss, similar to that of metal-machined waveguides, but provide a very high level of integration solutions. Moreover, they are capable of integrating complex passive circuits with active components. As a result, we focus here primarily on DRIE-based circuits, interconnects, and packaging.

We demonstrate how metal waveguide-based packaging technologies have performed admirably by facilitating the design and packaging of high-performance mm-wave and THz systems. As mm-wave and THz technologies have matured, however, new applications have emerged, and systems have become more complex and multifunctional; therefore, a new integration and packaging platform is needed to effectively address these challenges. Because waveguides still provide the lowest transmission loss, micromachined waveguide packaging techniques (DRIE-based, silicon micromachined packaging, in particular) are most suitable to achieving low-loss, highly functional, and fully capable instruments at high-mm-wave and THz frequencies.

Metal Machining

Today, nearly all sub-mm-wave and THz components are packaged in metal waveguides. These packages

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are machined from metal utilizing CNC milling. Advancements in equipment and software have supported this manufacturing technique to achieve the 2–10-μm accuracy usually needed at THz frequencies, while being flexible and affordable enough to deliver parts reliably. At the same time, microtooling has also advanced, allowing for 5-μm-wide channels and aspect ratios as high as 10:1. These extremely small tools have enabled the use of the CNC milling as high as 4.7 THz [20].

At THz frequencies, transmission line losses become increasingly higher due to shallow skin depths. Figure 2 compares the losses of microstrip, coplanar waveguide (CPW), and rectangular waveguides normalized by their wavelength. At frequencies above 100 GHz, rectangular waveguides are orders of magnitude more efficient than planar transmission lines. With MMIC technology, where devices and passive circuits also scale with frequency, microstrip and CPW losses are manageable. But, for packaging, the distances required between devices become much larger because of standard interfaces and bias connections that do not scale with frequency; therefore, the lowest-loss transmission line is normally required. As a result, the E-plane split-waveguide housing has evolved into the standard packaging solution for high-frequency components because it is a versatile method for integrating devices with rectangular waveguides. Figure 3 depicts the cross section of such a waveguide. By splitting the waveguide at the same level as that of the peak in the electric field, currents across the split are minimized, thereby relaxing the flatness and roughness tolerances on this split interface. This structure is also directly compatible with CNC machining and typically requires only a tool of aspect ratio slightly greater than 1:1.

The primary advantage of the E-plane split package is the ease of coupling between planar transmission lines and rectangular waveguides. A vast library of transitions exists, enabling low-loss coupling between MMICs and waveguide. The most common is the E-plane probe, but other, more exotic transitions to finline or stripline are well documented. Figure 4(a) presents the most common of these E-plane waveguide transitions. Finite element-simulation tools facilitate the refinement of this simple probe design of full-band waveguide coverage to microstrips [22]. At frequencies below 300 GHz, short, low-loop wirebonds can be used to connect MMICs to waveguide transition probes [23]. The module shown in Figure 4(b) demonstrates how the dc bias can be routed to the split plane vertically with dc feed-through pins. These feed throughs can connect directly to bias printed circuit boards, which generate the appropriate bias voltages and protect the circuit from exposure to electrostatic discharge [24].

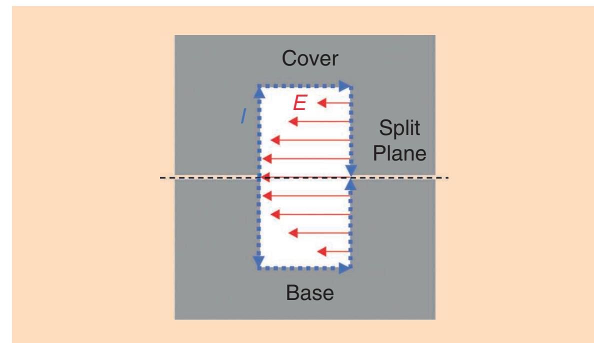

Figure 3. *The E-plane split waveguide. The E-field and currents are shown in red and blue, respectively. By splitting the waveguide at the peak of the E-field, the current across the split is avoided, thus reducing losses and easing fabrication tolerances across the split plane.*

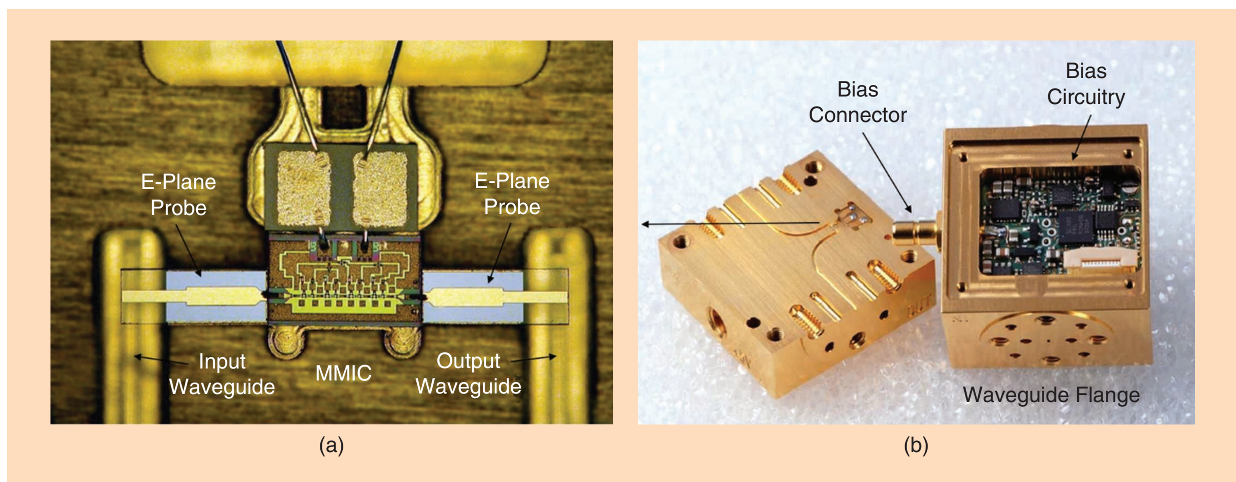

Figure 4. *(a) A 300-GHz MMIC housed in an E-plane split package, with the E-plane split probe on either side of the MMIC. (b) The E-plane split package contains the waveguide flange, bias connector, and biasing printed circuit boards.*

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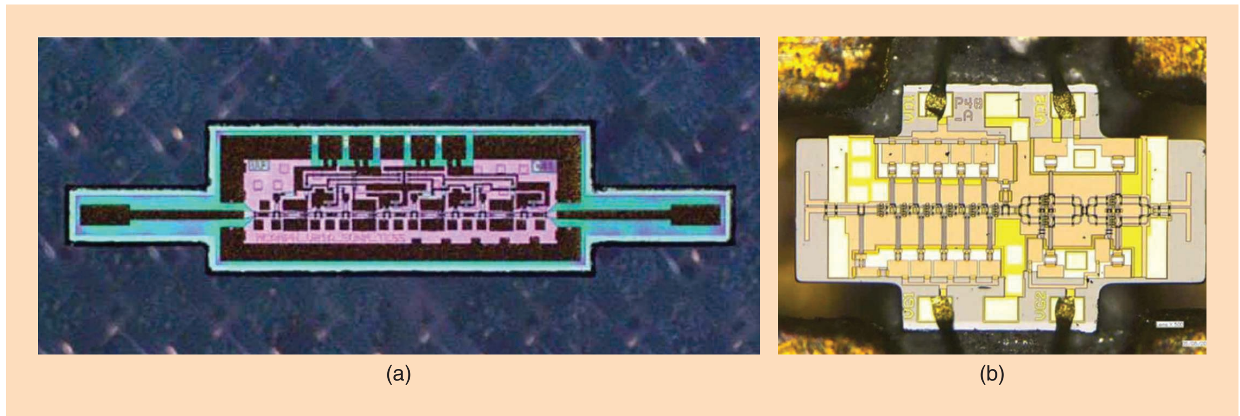

Figure 5. *THz MMICs with integrated probes. (a) A 220–320-GHz MMIC amplifier with integrated waveguide probes [24]. (b) A 650-GHz power amplifier, which uses a more compact dipole to couple to the waveguide [25].*

At higher frequencies, integrating the waveguide transition probe with MMICs becomes essential to efficient coupling. Several examples of these integrated probes are shown in Figure 5. Because the MMIC widths usually support substrate modes, most of these devices require nonrectangular substrate borders that narrow the width of the substrate around the E-plane probe. This complicates fabrication, requiring the chemical etch release of devices or laser etching instead of dicing. Finally, probe integration prohibits on-wafer probing of the device before packaging, which results in discrete probe assembly and MMICs being preferred.

Nontransistor-based devices, such as Schottky diodes or superconducting detectors, often use a beamlead-based architecture to operate as high as 4.7 THz. This approach suspends substrates 5–15-μm thick with free-hanging metal beamleads, as revealed in Figure 6. These beamleads provide a path for grounding, biasing, and intermediate frequency (IF) signals. By suspending ultrathin substrates in channels, higher-dielectric substrates that do not support substrate modes can be used. The Jet Propulsion Laboratory's diode process uses gold beamleads with thin gallium arsenide substrates that create multipliers of up to 2.7 THz, as represented in Figure 6. The grounding and suspension of the device are created by clamping the gold beamleads between the two halves of the E-plane split block. Bias is provided by another beamlead, which is tack-bonded to a bias capacitor. Highly sensitive superconducting THz detectors, such as superconducting-insulator-superconducting junctions or hot electron bolometers (HEB), often use beamleads to achieve operation in the 0.5–5-THz region. In this case, 2–3-μm-thick silicon substrates are used because of their superior superconducting material quality (which can be grown on silicon) and ease of silicon micromachining.

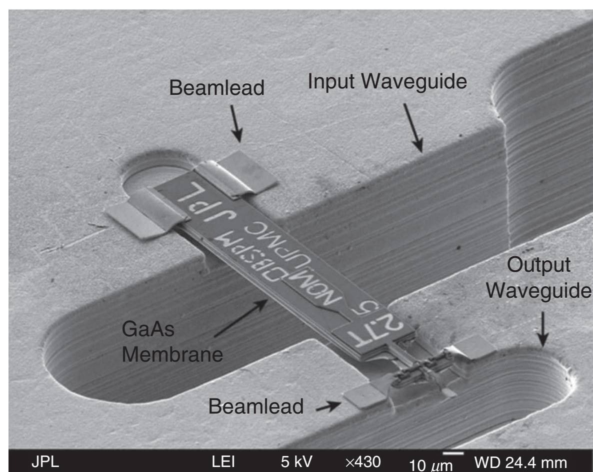

Figure 6. *A 2.7-THz beamlead Schottky multiplier that shows the gallium arsenide (GaAs) chip suspended on the CNC-milled E-plane split block [26].*

Micromachining Fabrication Processes

Metal machining of E-plane split blocks is not without its challenges. Although the accuracy of CNC milling has advanced tremendously over the past few decades, aligning the two halves exacts a toll on existing machining capabilities. See "Alignment Techniques for Metal-Machined and Silicon Micromachined Components" for more information about these techniques. Another issue is that milling is a serial process, and, as the complexity of the circuit design increases, so too does the cost. The serial nature of CNC-milled components means that the cost will not scale with volume production the same way that MMIC technology would. Finally, the vertical integration of complex waveguide structures on multilayer stacks is nearly impossible above 300 GHz because, if the metal layers are too thin, they cannot be machined through the use of a milling machine. On the other hand, if the metal layers are too

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thick, the through-hole vertical waveguide sections cannot be machined because the milling tools do not work when the aspect ratio is more than 10:1.

Nano and microfabrication technologies, when used at higher-frequency regimes such as photonics or infrared, naturally offer accuracies superior to those required for THz. For the sub-mm-wave regime, microfabrication has been explored to provide new packaging solutions that will reduce the cost, volume, and power of future systems. This technology is also referred to as *micromachining* because the thicknesses produced are orders of magnitude greater than the typical "thin-film" processes. As it relies on photolithographic processes, micromachining produces entire batches of devices in a single run, which results in lower cost per device when produced in volume. Vertical, multilayer stacks of integrated waveguide structures become a possibility because their layers can be thin wafers of a few hundred microns and also because of the higher aspect ratios achievable with these processes compared to metal machining. Finally, the direct integration of devices with the package could eventually be considered because they share many of the same processing techniques, although nothing like this has been demonstrated yet.

DRIE micromachining is a dry-etching technique that relies on bulk silicon plasma etching, which can be implemented cryogenically or at room temperature by following a Bosch process. Both are known to produce near-vertical sidewalls as well as high aspect ratio features and are applicable to mass production [27], but a Bosch process is more commonly used to fabricate THz components. It employs a sequence of sulfur hexafluoride plasma for etching and octafluorocyclobutane plasma for passivation [28] with various masks, including photoresist, oxide/nitride, or metals. In many cases, mask thickness must be determined by accounting for the silicon etch depth and the DRIE process selectivity toward the mask material.

Single-step DRIE processes are well documented and typically use the same process flow: photoresist is spun onto a flat silicon wafer, and the resist is exposed by applying conventional photolithography to reveal the patterns. The resist is then used as the etching mask in the DRIE. After the desired depth is reached, the resist is stripped from the surface, and the structure can then be metalized if desired. Several millimeter and submillimeter components have been fabricated by exploiting single-step DRIE processes, including passive E-plane waveguide components at WR-3 to WR-1.5 [19], [29], [30], a double H-plane waveguide at WR-3 [31], hybrid couplers at WR-10 [32], and E-/H-plane filters at WR-1.5 and WR-1 [33], [34]. Silicon microlenses have also been fabricated by employing this technique [35], [36], but the work is still under development and so not as predictable as other serial processes, as it is harder to control the shape of the lens accurately.

At frequencies below 300 GHz, short, low-loop wirebonds can be used to connect MMICs to waveguide transition probes.

More complicated circuits have been fabricated utilizing multiple DRIE etches, where each etch depth is patterned with a separate resist mask, i.e., where each etch depth requires its own resist spin. But, after two or more deep etches are performed, the wafer is no longer flat enough to achieve uniform resist coverage during spinning. As a result, during the long DRIE etches required for deeper waveguides, silicon areas at the edge of the patterns and the inside of preformed waveguides become exposed and etched. Although promising results were presented at 540 and 900 GHz [37], [38], both suffered from high surface error as well as pitting and pattern deformation due to spinning resist on an uneven surface, all of which degraded the performance.

To maintain the surface regularity for a high number of etching steps, a more complex process was developed [39]. One approach relies on silicon dioxide masks of varying thicknesses, where each thickness corresponds to one etch depth in silicon. In this case, all of the lithographic steps are performed on the silicon dioxide mask prior to DRIE. This avoids any photoresist coverage issue, and, because the selectivity of the DRIE process on the silicon dioxide is very high, the oxide needs to be only a few micrometers thick. The DRIE depths are divided in sequence so that each pattern is gradually etched to the appropriate depth. Figure 7 depicts the processing steps and scanning electron microscope images of fabricated structures using this multietching technique. Additional details of this process are presented in [39], with state-of-the-art losses of 0.07 dB/mm at 500–600 GHz.

As noted previously, other silicon microfabrication techniques are available, sometimes for a lower investment. Several of these techniques use thick resist as a decoy mask or permanent structure. Epoxy-like resists (up to 1 mm) such as SU-8 and KMPR are capable of aspect ratios as high 50:1, while maintaining dimensional accuracy to within 10 μm. One of the most attractive features of these techniques is that processing is possible with only standard ultraviolet photolithography equipment.

Nonetheless, employing SU-8 as a permanent part of the structure is often undesirable, primarily because of its mechanical characteristics [42]. Its

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Employing SU-8 as a permanent part of the structure is often undesirable, primarily because of its mechanical characteristics.

thermal conductivity is very low, i.e., 100-times less than copper, and the glass transition temperature is also low; thus, the thermal dissipation or localized heating derived from active devices could deform the device packaging. Additionally, the thermal expansion coefficient of SU-8 is relatively high, so delamination from the carrier at cryogenic temperatures is a concern [43].

Electroforming through the use of photolithographically patterned resists has the advantage of forming the structure completely in metal with micrometer precision. Unlike permanent resist packaging, a purely metal structure avoids the thermal issues and CTE mismatch problems. Figure 8 expresses the typical process flow for each of these techniques and shows photos of waveguides fabricated using this process at THz frequencies.

Finally, laser micromachining is another silicon micromachining technique that has come a long way since its first introduction. It does not require the use of photoresists but uses an argon-based laser in a chlorine environment, which locally heats the silicon substrate. This technique is capable of producing complex 3D structures with small feature sizes and good mechanical tolerances. It is also used for specific THz components, such as silicon lens arrays [45], [46]. The process could be used for vertically stacked systems, but, because of the serial nature of the process, its cost is relatively high compared to CNC milling or other silicon micromachining techniques.

THz System Packaging and Integration

The typical development cycle of THz systems consists of the design, fabrication, and testing of the initial

Alignment Techniques for Metal-Machined and Silicon Micromachined Components

The E-plane split structure requires alignment between the two halves for proper operation, which can be challenging at terahertz frequencies, where the width of the waveguide can be 50 μm or lower. Depending on the type of waveguide structures used and its frequency of operation, alignment

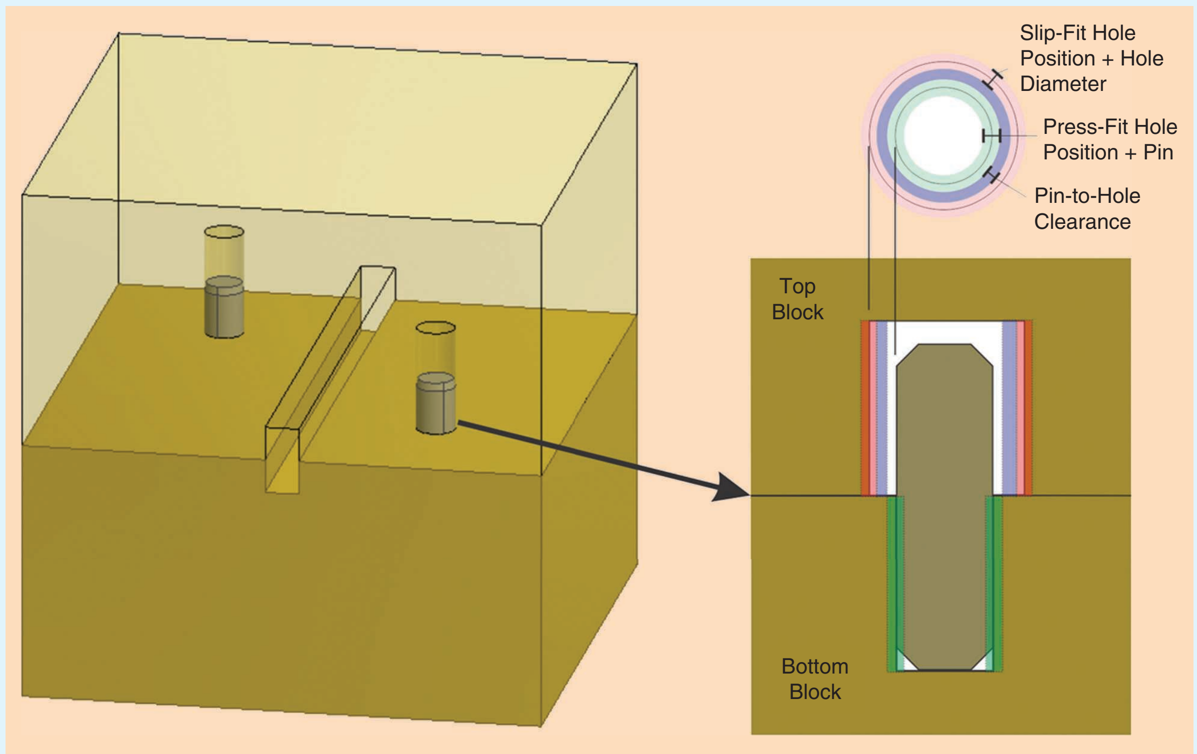

Figure S1. *A schematic depicting the E-plane split metal-machined waveguide block. The two halves are aligned using press-fit pins in one half and slip-fit holes in the other.*

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stand-alone components, followed by a fully integrated package with all the interfaces. Testing the active and passive structures individually reduces the risk of such "all-in-one" systems, especially when developing a new fabrication process or packaging technique. Each of the passive components and active devices is packaged individually and then connected through a waveguide flange. This reduces the complexity of each package and allows for component-level testing of each construct; however, if the individual components are all cascaded to develop the entire instrument, it radically increases the size and mass of the system. This is because the waveguide flanges are large compared to wavelengths at THz frequencies, which forces a minimum volume upon each component or device. Custom flanges can be adopted, but with the loss of interoperability that accompanies existing testing infrastructure. The spacing forced upon the system by the flanges also becomes an issue above 500 GHz, where a 1-cm run on waveguide results in 1 dB of loss.

In the next section, we discuss the two primary packaging and integration techniques at these frequencies: CNC metal milling based and silicon micromachined waveguide based. We provide several examples of these packaging techniques.

Metal Machining-Based System Integration

The primary fabrication technique for packaging THz components is CNC milling. Although packaging and interconnecting technologies at frequencies beyond 200 GHz remain challenging, CNC milling has advanced far enough so that higher levels of system integration into a single package are now possible. The package shown in Figure 9 is a 1.2-THz Schottky diode-based receiver, where each front-end element was individually packaged and assembled with standard flanges [47]. Note that, despite the good performance of the overall receiver, the size of the overall structure is high compared to the more integrated approach

precision on the order of 5–10 μm is often required, and 2 μm is required when operating above 1 THz. For metal E-plane split blocks, the two halves are aligned by press-fit pins in one half and mating slip-fit pins on the other. Two pins are used to fix the position and rotation of the halves to each other, which align with tight tolerance holes that accept the pins, as displayed in Figure S1. The press-fit pin can be set more accurately because the primary uncertainty is in the location of the hole that the pin will be pressed into. The hole can be slightly undersized, and the metal is compliant enough to allow for the pin to be pressed into place. The slip-fit pinhole has tolerances on the location and diameter of the hole. The hole must be slightly larger than the pin to allow the pin to fit into it without too much force, but this oversizing will determine the alignment precision of the top and bottom halves. It is a testament to the advances of modern machining that alignments better than 5 μm can be achieved.

The alignment of silicon E-plane split components presents a unique challenge because of the brittle nature of silicon. Pressing pins into silicon is not feasible because the wafer would simply shatter; however, as it is a brittle material, slip-fit pinholes etched into the wafers must be larger than what would be used on metal devices to avoid cracking while inserting the pin into the silicon hole. Using silicon instead of metal for the alignment feature has helped solve this

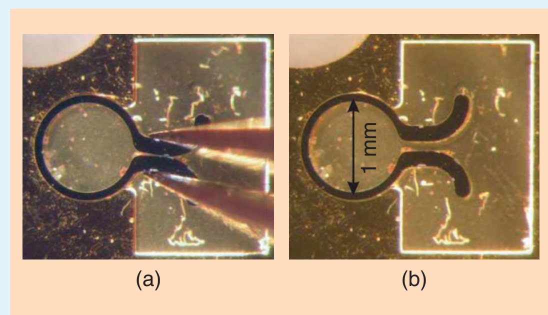

Figure S2. *A silicon pin used for silicon micromachined E-plane split alignment. (a) A pair of tweezers compresses the pin during placement. (b) The pin is released into the pocket.*

problem. Figure S2 shows a compressible ring of silicon a few hundred microns thick that can be compressed while being inserted into a pocket that is etched into the silicon wafer. This pin is designed to be slightly larger than the pocket and is slightly compressed when put into place, thus removing the gap required to insert the pin into the pocket. By utilizing this technique, alignments on the order of 1 μm have been achieved [19]. These pins were extended to the alignment of the silicon-to-metal housings, although, here, tolerances are not quite as satisfactory because the positional accuracy of the computer numerically controlled milling is less than that of silicon micromachining.

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presented in Figure 10. With the increased demand and maturity of THz products, now new systems with higher levels of integration can be offered. Figure 9(b) displays a 680-GHz polarimeter developed by Virginia Diodes, Inc. [48]. This metal block integrates an orthomode transducer (OMT) that separates both polarizations, the subharmonic mixers, two sets of doublers, the IF low-noise amplifiers, the 80-GHz power amplifier, and the local oscillator (LO) driver, all on a single split block architecture.

Increasingly, multipixel instruments are needed for imaging or other applications. With multipixel architectures, a high level of integration between pixels is essential. The pixels must be closely packed to have a fully sampled imaging system. A good packaging example, as depicted in Figure 10, is a 4 × 4 transmitter pixel array at 1.9 THz. This configuration avoids the standard waveguide flanges by having the four rows of multipliers integrated on a single block, and the base of one of the layers acts as the cover of the next row. With this 3 × 3 × 3 multiplication scheme arrangement, each stage of the frequency multiplier chain may be tested individually, while achieving a peak power of 40 μW/pixel with a dc power consumption of 2.6 W/pixel [49].

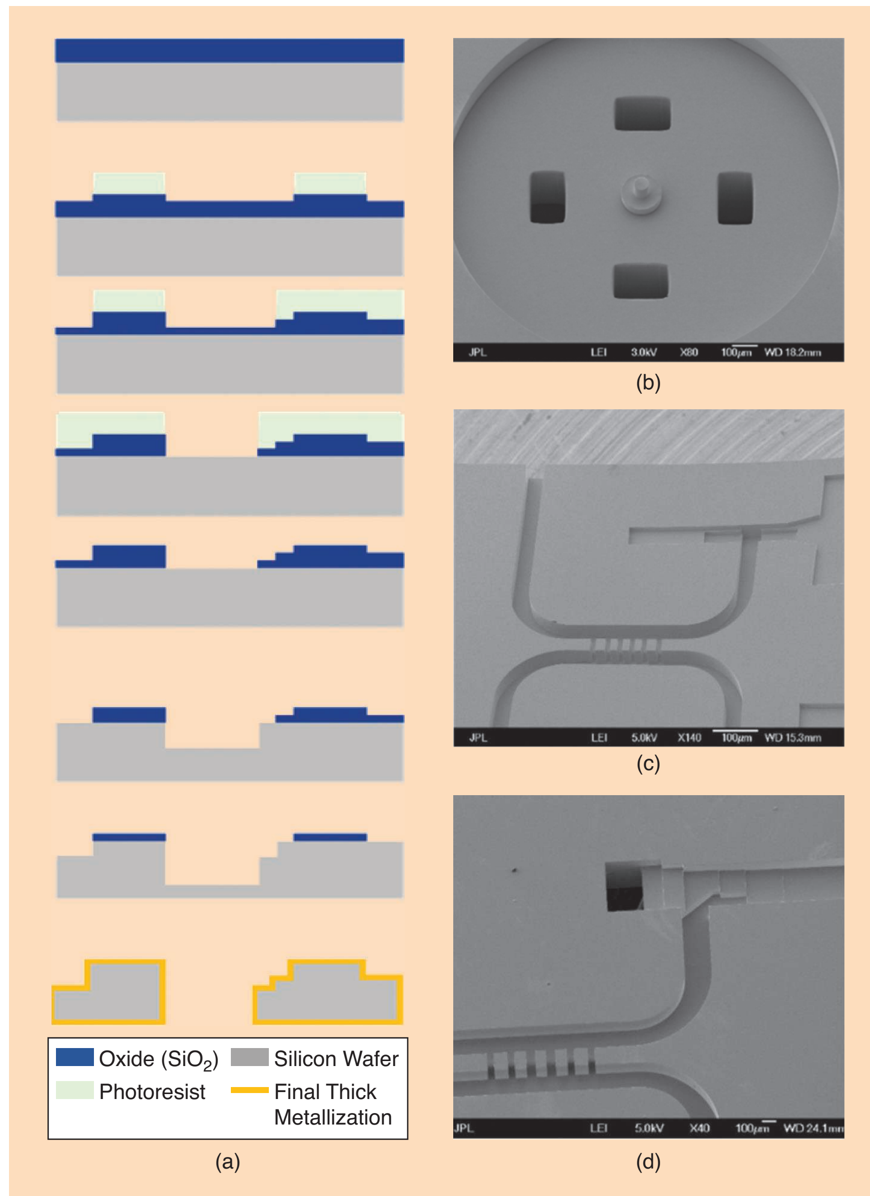

Figure 7. *(a) A multistep DRIE process flow that relies on oxide masks. The several-micron-thick oxide layer is prepatterned in multiple steps using conventional lithography. Each oxide mask corresponds to one silicon etch. Silicon etches are then added to produce the desired final depth, in sequence. The scanning electron microscope images of fabricated structures obtained using this technique. (b) A 1-THz turnstile orthomode transducer [40], (c) a 2.7-THz HEB mixer block [41], and (d) an eight-step OMT at 500–600 GHz. SiO_2: silicon oxide.*

Silicon Micromachined-Based System Integration

Silicon micromachining packaging offers new capabilities beyond metal-based packaging. The use of photolithographic processes can, e.g., produce entire batches of devices in a single run, and the complexity of the circuits does not affect the fabrication time. This is particularly attractive if large, multipixel arrays are being considered. Conversely, vertical transitions can be achieved using ultraflat silicon wafers as thin as 200 μm. This enables the system's vertical integration, making the transitions very short with low loss, thus radically reducing the area required for each device, which is crucial for a multipixel architecture.

Several adjustments must be made to the circuit's design to ensure that it is compatible with silicon micromachining. In particular, the circuit structure must be designed on discrete etching steps (i.e., no bends or curvatures in the

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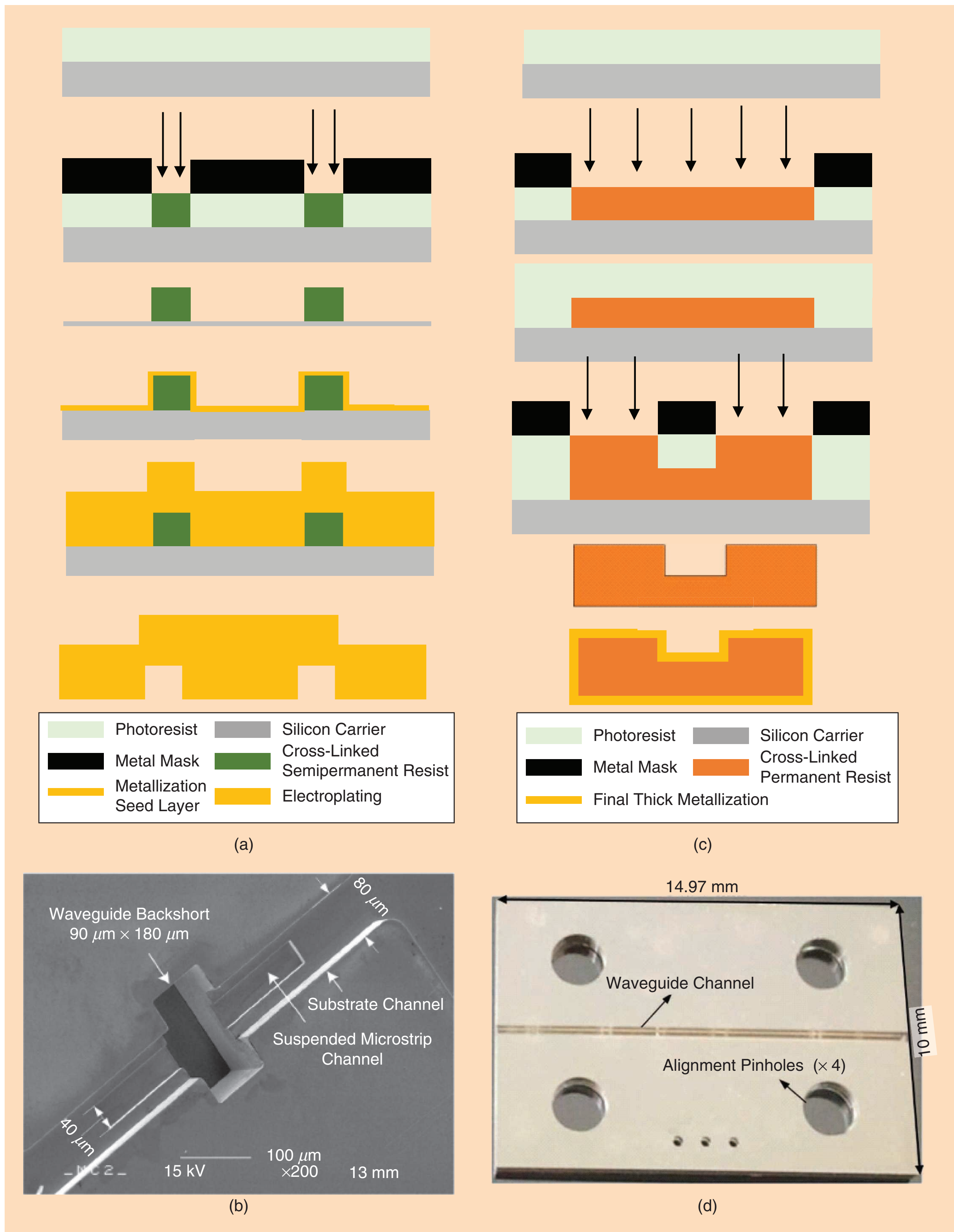

Figure 8. *(a) The schematic of a multistep, semipermanent, thick-resistant process flow. The resistance is used as a mold for electroplating, with silicon as the carrier, and removed at the end. (b) An example of a fabricated 1.3-THz waveguide housing that uses this technique [17], [44]. (c) The schematic of a multistep, permanent, thick-resistant process flow. The resistance is spun hundreds of microns thick and exposed, in sequence, using a metal mask and silicon as a carrier. After the carrier is removed, the whole structure is metalized. (d) An example of a fabricated waveguide filter at WR-3 [16].*

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Testing the active and passive structures individually reduces the risk of such "all-in-one" systems.

transverse dimensions). An example of the design process of a dual-polarized balanced receiver front end at 1.9 THz is shown in Figure 11. Its waveguide structure consists of a vertical, 90° hybrid OMT mixer channel (which, in this case, is an HEB mixer) and a 634-GHz Schottky diode-based tripler. The design is optimized to use a minimum number of etch steps to reduce fabrication complexity. For the components displayed in Figure 11, the maximum number of etch steps on a wafer surface was six. The fabrication of such a system requires a total of six silicon wafers with a thickness between 300 and 400 μm each, amounting to an overall thickness of 2 mm for the stack. Vertically integrating components in this manner allows for the arraying of multiple pixels in a highly compact wafer stack.

Alignment between the silicon layers is performed utilizing the silicon pins previously described. And, to build the silicon layers with the low-frequency LO, biasing, and IF circuity, it is possible to use auxiliary metal fixturing. Note that the alignment between the silicon and the low-frequency LO, which has a metal-based package, is also accomplished using silicon pins. Figure 12(a) presents the assembly of a silicon-based, 1.9-THz tripler with a low-frequency pump signal, while Figure 12(b) depicts the assembled transmitter. The top layer is an integrated microlens antenna also fabricated by implementing silicon micromachining techniques, which are discussed in the following sections.

Antenna Feed Integration and Packaging

As with any system at lower frequencies, receiver and transmitter systems at mm-wave and THz frequencies also require antennas. Microstrip patches and other planar elementary antennas such as dipoles or slots, which are popular at lower frequencies, are very lossy at mm-wave and THz frequencies. They suffer from high losses due to substrate modes that are excited inside the dielectric substrates and from the transmission lines losses that feed them.

The transmission line losses are because of the finite conductivity of the metal conductor employed and the absorption losses of the dielectric substrates. Consequently, phased arrays are impracticable at THz frequencies if traditional methods are utilized. These losses can be mitigated only when exploiting superconducting lines on high-resistivity substrates. For example, the BICEP2 [51] instrument that was applied for cosmic microwave background polarization measurement installed transition edge sensor bolometer detectors coupled to 150-GHz dual-polarized phased arrays of 10 × 9 slots for each polarization on a 10 × 10-mm area using superconducting feed lines. The main limitation of superconductors is that they

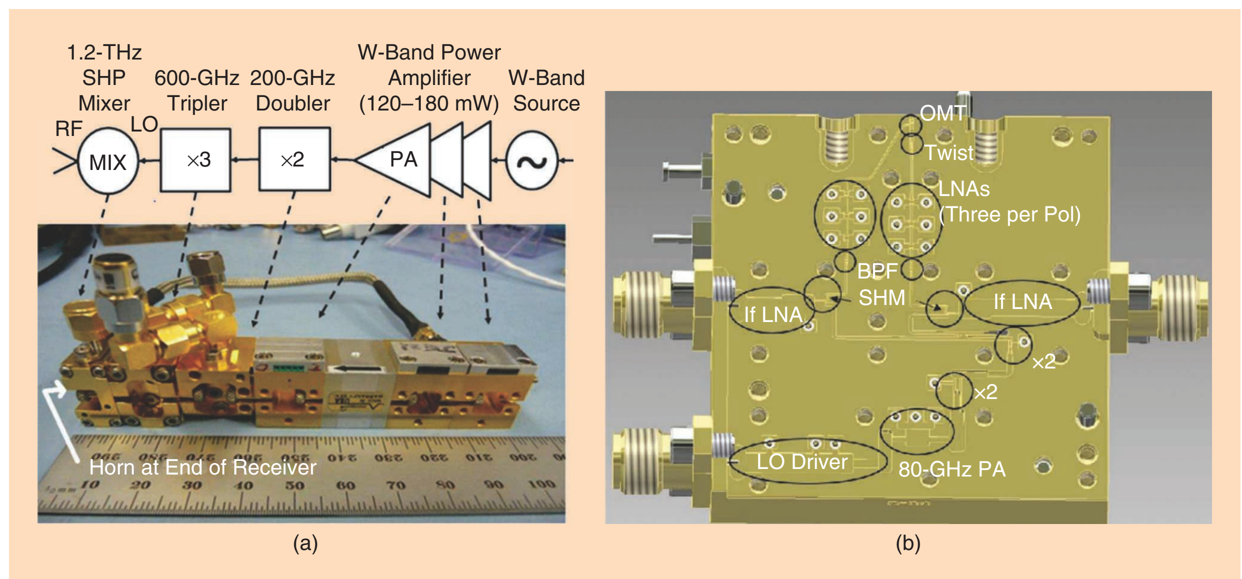

Figure 9. *(a) The architecture of a 1.2-THz Schottky diode-based receiver design in [47]. (b) A full 670-GHz polarimeter system integrated into a single E-plane split block. By integrating the local oscillator (LO) drive chain directly with the mixers, bandpass filters, low-noise amplifiers (LNAs), and OMT, only one waveguide flange is required, thus radically reducing the system size to fewer than 4 cm × 4 cm × 2.5 cm [48]. PA: power amplifier; pol.: polarization; BPF: band pass filter; SHM: subharmonic mixer; SHP: subharmonically pumped.*

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require cryogenic cooling and are therefore not suited to many applications.

The power loss caused by multiple substrates modes in the dielectric is due to the use of electrically thick substrates to sustain the antenna. The substrate modes can be avoided if the substrates are made thinner than 0.04–0.01 times the wavelength in the dielectric for an elemental slot or a dipole antenna, respectively [52]. One way to solve this is to use thinned, suspended membranes, which are manipulated for the majority of waveguide-based active circuit devices, i.e., MMIC amplifiers, Schottky diode-based mixers and multipliers, and waveguide HEB mixers, as mentioned previously. These membrane-based devices can couple to a waveguide through an E-probe and, ultimately, can be coupled to a horn. Another approach is to use an integrated lens on the back of the circuit to radiate the power through the substrate and lens to free up space. In the following sections, we give a brief overview of the fabrication and integration technologies used for horn and lens antennas.

Horn Antennas

Horn antennas are widely used because of their high performance and straightforward integration with waveguide-based receivers. Corrugated horns are highly desirable as reflector feeds due to their nearly ideal performance, i.e., high-axial beam symmetry, bandwidth, low cross polarization, and low sidelobe level. The most common fabrication method applied for these horns as stand-alone antennas in the mm-wave and THz bands is electroforming, where the internal geometry of the horn and waveguide is machined on a mandrel (see Figure 13). The horn is obtained by electrochemically depositing the gold or copper present on this surface to the desired wall thickness.

For systems in the high mm-wave and THz bands, integrating the horn with the detector element (often a

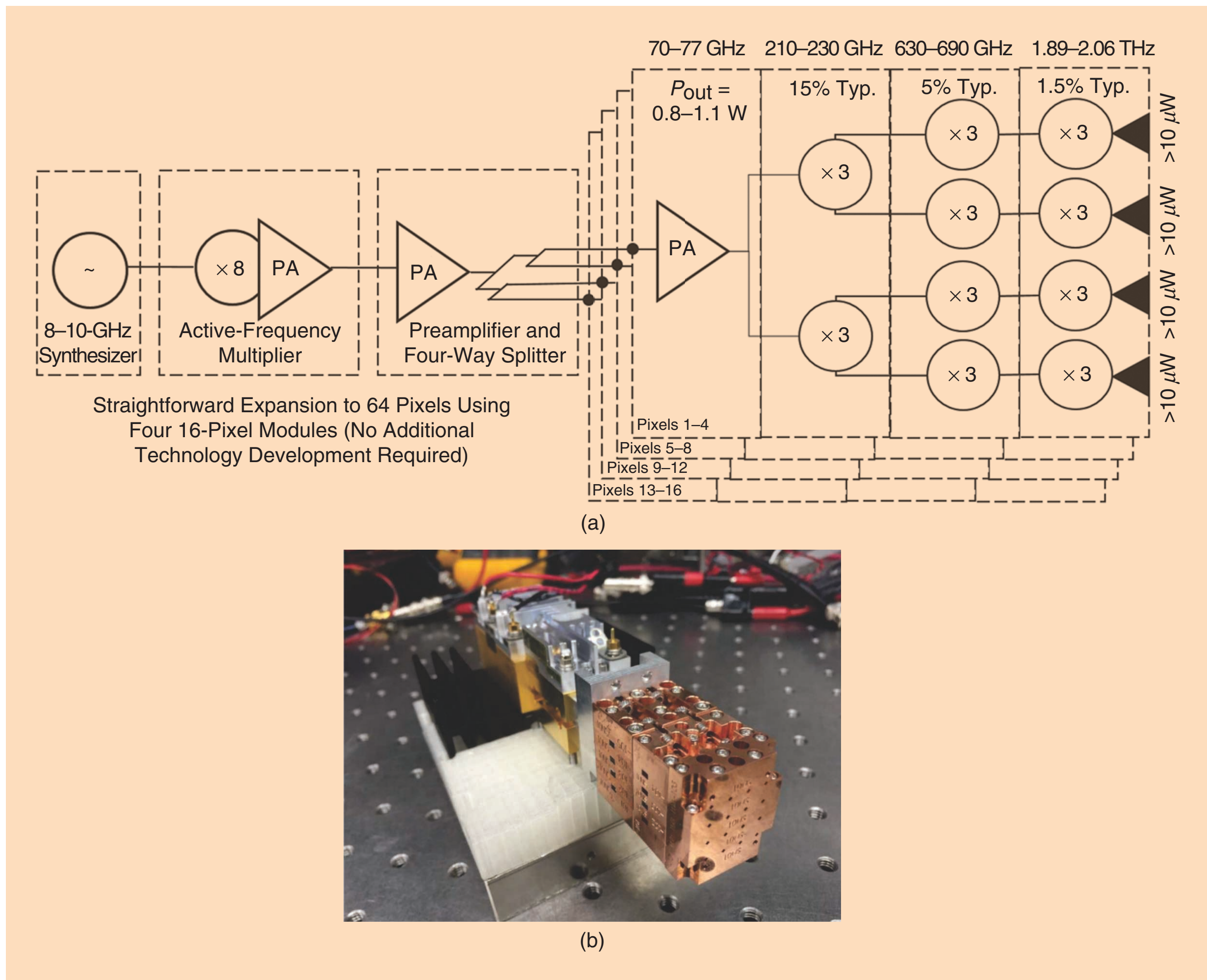

Figure 10. *A 16-pixel, 1.9-THz multiplier array. (a) By avoiding a standard flange, the three 4 × 4 multiplier stages can be integrated with 5-mm spacing between each pixel. (b) The three central layers of the multiplier array are both the base for one row and the cover for the row below it [49].*

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Figure 11. *The silicon micromachined front-end design process of a dual-polarized balanced receiver at 1.9 THz. (a) A block diagram of the system's front-end architecture to be synthesized on silicon wafers. (b) The waveguide design structure. (c) The discretization among different silicon wafers of a certain thickness and the minimization of etch depths. (d) The resulting stack of silicon wafers. Note that, after the etching process, the wafers are gold plated. SOI: silicon on insulator.*

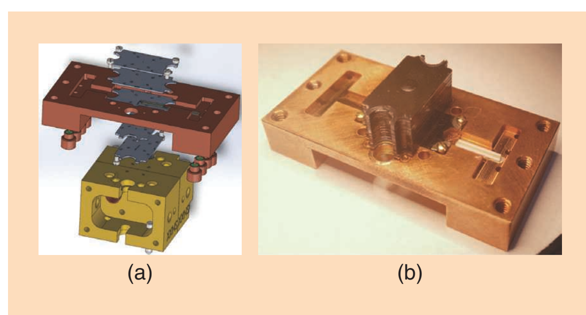

Figure 12. *(a) A silicon-based, 1.9-THz tripler assembly with a low-frequency pump signal. (b) A photo of the assembled transmitter at 1.9 THz [50].*

mixer at these frequencies) is necessary to minimize the ohmic losses associated with the waveguide interconnection. Thus, the horn and detector unit are machined on an E-plane, split-block configuration. In these cases, Potter-type horns are preferred because they are easier to fabricate in a split-block and are comparable in performance to the corrugated horn over a reasonable bandwidth. Potter horns consist of a smooth-walled conical horn, with a single step at the throat that excites both the fundamental TE_{11} and TM_{11}. In this additional mode, the radiation pattern of the horn becomes circularly symmetric and low cross polarization. The main disadvantage of the Potter horn [53] is its narrow operating bandwidth of between 5 and 7%. This can be improved by increasing the number of discontinuities while maintaining the radiation properties [54]. The shapes of the horn's interior are numerically optimized by mode-matching techniques used to generate the number of modes, which create the desired performance. Another horn antenna variation is the spline profile feed [55], which has a polynomial function that contains a high degree of smoothness; although it does not perform as well as a corrugated horn, it can achieve high bandwidths and cross-polarization levels below –30 dB.

In an array configuration, corrugated horns are being fabricated by implementing multiple metal layers

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with holes that are aligned and stacked together. These layers can be developed by milling holes on brass plates [56]. At higher frequencies, they can be synthesized by exploiting gold-plated silicon micromachined wafers [54]. Figure 14(a) shows the corrugated horn array of 84 elements at the W-band that were developed in [57]. It used a silicon micromachining DRIE process to etch the holes of the corrugations of the horn onto various wafers. The silicon wafers are gold plated after etching and formed together utilizing screws.

An alternative method for developing arrays is to directly mill the horn on an aluminum piece using a custom drill bit [54] [see Figure 14(b)]. This practice requires a linear profile type of horn, which makes a Potter horn the ideal candidate. This technique eases the assembly process and is suitable for fabricating multiple horns on the same metal block.

Silicon Lens Antennas

With the rise of silicon micromachining as a packaging technique and the difficulties involved with coupling between silicon and metal, integrated silicon lenses have reemerged as an attractive antenna. Silicon lenses have been used for many years as a technique to improve the efficiency of planar antennas. The antenna is typically printed on the back of a high-dielectric thick substrate, and an elliptical lens is mounted, placing the planar antenna in the second focus of the ellipse (see Figure 15). This approach is used extensively in the literature thanks to its good performance, simplicity, and mechanical robustness compared to that of the use of membranes.

Float-zone silicon is the preferred material for synthesizing these lenses because of its low dielectric loss, as one can achieve a resistivity on the order of 10,000 kΩ·cm. However, the silicon's high permittivity ($\varepsilon_d \approx 11.9$) has a drawback: At each silicon air surface, there is a 30% reflection for normal incidence. This reflection between the lens and air interface can be mitigated over a reasonable bandwidth by the deposition of an antireflective (AR) layer on top of the lens. The optimum AR layer (i.e., coating) that performs a perfect cancellation of these reflections at a certain frequency requires a permittivity of $\varepsilon_m = \sqrt{\varepsilon_d}$ and a thickness of $\lambda_0 / 4\sqrt{\varepsilon_m}$), where λ_0 is the free-space wavelength at that frequency. For silicon lenses, it is common to perform the synthesis of this layer by depositing a uniform layer of Parylene-C (with a permittivity ≈ 2.7) through the use of vapor deposition. This technique provides a conformal deposition with an accurate control of the thickness within a few microns. Another option is to use materials based on mixed epoxies such as Stycast [58], which achieve a closer match to silicon. For applications that require

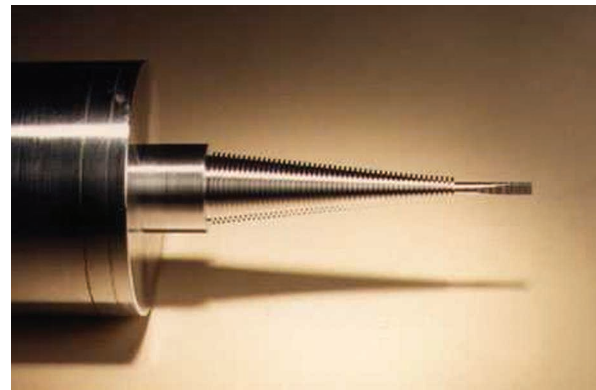

Figure 13. *A corrugated horn mandrel at 190 GHz by ZAX Millimeter Wave Corporation.*

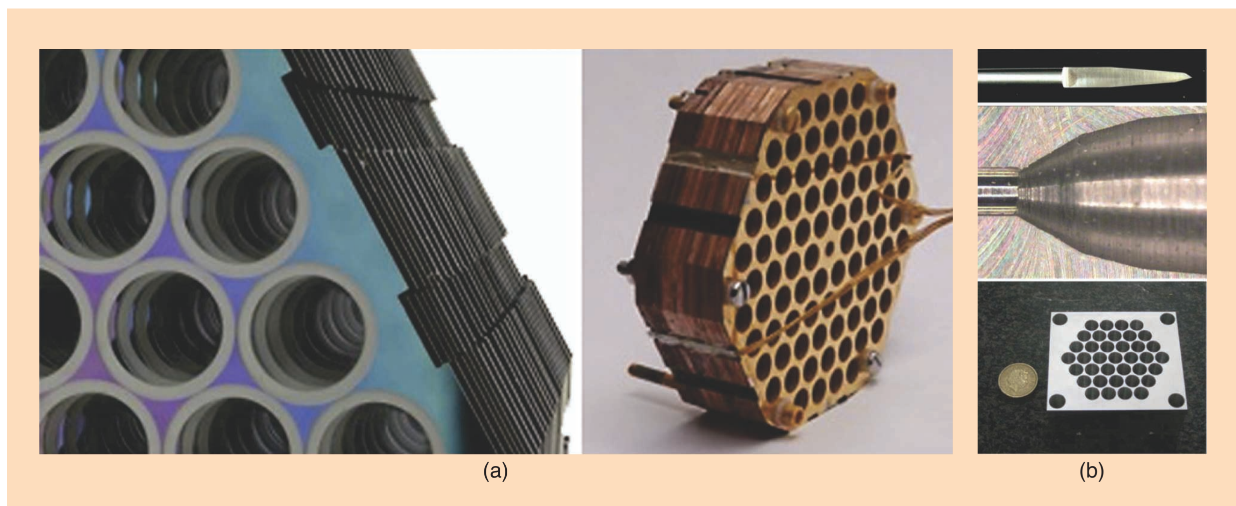

Figure 14. *(a) A corrugated horn array fabricated using micromachining techniques at 150 GHz [57]. (b) A drill bit (top view), cross section (middle view), and array (bottom view), of a multiflare angle horn at 230 GHz.*

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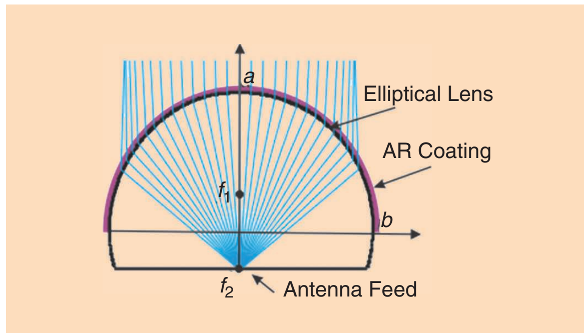

Figure 15. *The sketch of an elliptical lens with an AR coating layer. The ellipse collimates the rays incoming from the antenna feed placed on the second focus of the ellipse.*

a perfect cancellation, patterned subwavelength features on top of the lens may be manipulated to create a perfect AR coating [59].

Although individual elliptical lenses or extended hemispherical lenses are commercially available and easily machined, arrays of lenses are more challenging to fabricate. There are arrays of lenses that have been individually assembled at 350 GHz [60]. But, currently, one can use silicon laser or photolithographic techniques that allow for fabrication of the full lens arrays on a silicon block. Laser micromachining has enabled the accurate fabrication of 3D geometries and has shown great success with the development of stand-alone lens arrays for a high number of pixels. In [61], an array of 880 silicon lenses integrated with microwave kinetic inductance detectors was developed at 350 GHz. Another technique that fabricates lens arrays is DRIE-based silicon micromachining. This method only allows for the fabrication of shallow lenses; hence, a highly directive feed is required to efficiently illuminate them [62]. This technique is still under development because it is harder to accurately control the lens shape.

Although different techniques have been used in the past, the alignment between the lens and antenna is crucial for achieving a perfectly collimated beam at the broadside direction. One alignment method used in photoconductive antennas is to place the silicon lens on a manual x-y mount with a micrometer, where one can manually tune the position of the lens with respect to the center of the feed. Currently, a more common method is to draw alignment marks on the antenna plane, optically align both pieces, and glue or clamp them together. Another alignment method that permits the stacking of a higher number of wafers and has proven its good performance at frequencies up to 1.9 THz is the use silicon alignment pins to arrange the multiple silicon wafers of a lens antenna. Figure 16 shows two lens antennas at 1.9 THz that were synthesized on 12 and 32 high-resistivity silicon wafers, respectively. All of the wafers, including the lenses, were fabricated using a DRIE silicon micromachining process, configured employing the silicon-alignment pin method, and glued together. An alignment of better than 2 μm was achieved across the wafer stack [38].

Unlike horn antennas, lens antennas provide beam-scanning capabilities by translating the antenna feed

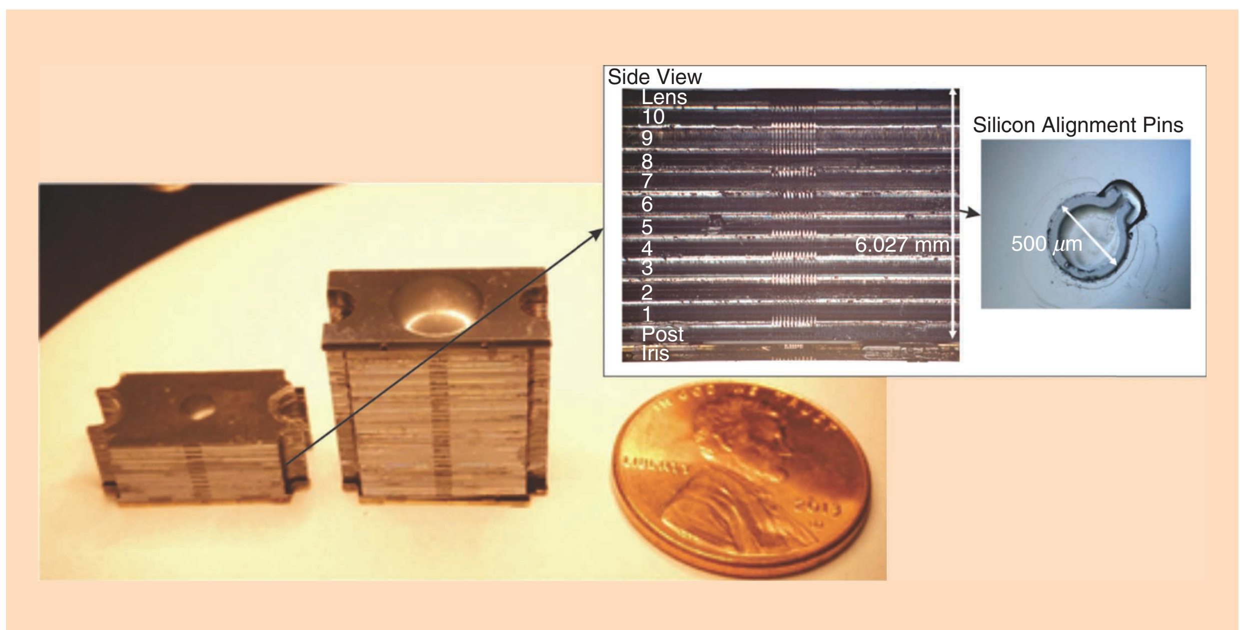

Figure 16. *High-resistivity silicon lenses fabricated using a silicon DRIE micromachining process at 1.9 THz. The alignment between the layers is achieved using silicon-alignment pins.*

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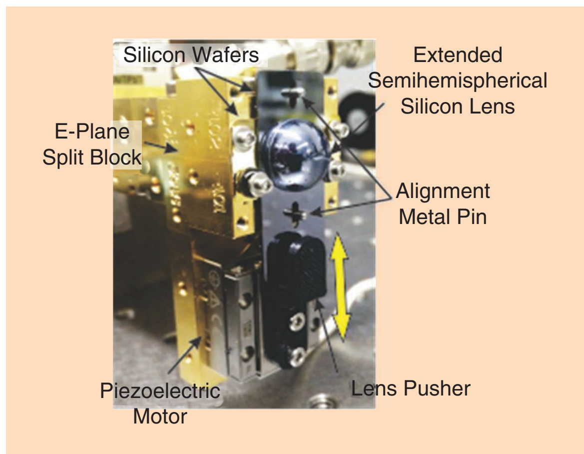

Figure 17. *A silicon lens antenna with an integrated piezoelectric motor at 550 GHz in [63]. The lens antenna provides a field of view of 50°, which corresponds to a lens displacement of approximately 2 mm, with a maximum scan loss of 1 dB.*

from the focus of the lens. The miniaturization and reliability of piezoactuator technology, together with advances in silicon microfabrication, have enabled the integration of a scanning mechanism on the lens antenna. Recently, in [63], a highly integrated beamscanning lens antenna using a piezoelectric motor was demonstrated, operating at 550 GHz (Figure 17). The lens was glued on top of a silicon wafer containing alignment marks processed through the use of DRIE silicon micromachining. The piezoelectric motor displaced the lens near ±1 mm from the center position of the lens, providing a beam scan of ±25°. Not only can this method be exploited for improving the alignment of the lens with the feed; it has the potential to enable beamscanning capabilities on the system's front end for future THz imaging systems.

Conclusions

The packaging of systems has been a stumbling block for mm-wave and THz frequencies for many years. Although CNC milling has steadily advanced to allow for higher levels of integration, it can never achieve the volume scaling that is possible with semiconductor processes. Micromachining offers new capabilities, such as lithographic precision and vertical integration, that provide new types of THz systems. To couple to these micromachined systems, new antennas that offer the same performance as metal-machined horns, in addition to new capabilities such as beamsteering, have been developed. We see that, as demand grows for THz applications, the volume of components will require a shift toward more integration and compact packaging systems. Micromachining-based packaging will address some of these concerns, resulting in decreasing costs and maintaining the same performance.

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