TU Delft

Bachelor Thesis

Transcutaneous Vagus Nerve Stimulation Through an In-Ear Device For Epilepsy Treatment

By,

K. Broek
J. Teurlings
B. Zuidema

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Delft University of Technology

Faculty of Electrical Engineering, Mathematics and Computer Science

Electrical Engineering Programme

Abstract

Several studies have illustrated that Transcutaneous Vagus Nerve Stimulation (t-VNS) is an effective method for epileptic treatment. In contrast to the classical invasive Vagus Nerve Stimulation (VNS) which is already a Food and Drug Administration (FDA) approved therapy for epileptic treatment, t-VNS does not require surgical intervention. However, t-VNS has still not been evolved into an application which can be used in clinical practise due to a lack of power efficiency or size constraints. In this bachelor graduation project, an electrical circuit has been designed and implemented for stimulating the auricular branch of the vagus nerve. This circuit is part of a larger project where an ear piece is developed which is able to process Electroencephalogram (EEG) signals as well. The main design goals of the stimulator were power efficiency and safety. Furthermore, a design for an integrated circuit has been proposed resulting in an power efficient method for controlling the electrical stimulation circuit. The integrated circuit has, among other things, built in safety features and closed loop stimulation capabilities. Simulations showed that the designed circuit is able to successfully stimulate with current amplitudes up to 8 mA when taking worst case values for an impedance model of the electrode-skin interface. However, the implemented physical design was planned to be tested after the thesis submission. In other words, this thesis only contains the design and simulation phase of the stimulator. The design was found to be safe and power-efficient and could lay the basis for future development in the field of wearable in-ear stimulation devices.

Abbreviations

ABVN Auricular Branch of the Vagus Nerve

ADC Analog to Digital Converter

AED Anti-Epileptic Drugs

ASIC Application Specific Integrated Circuit

BJT Bipolar Junction transistor

DAC Digital to Analog Converter

DC Direct Current

DRE Drug Resistant Epilepsy

EEG Electroencephalogram

FDA Food and Drug Administration

FPGA Field Programmable Gate Array

FSM Finite State Machine

GND Ground

IC Integrated Circuit

LC Locus Coeruleus

LDO Linear Dropout regulator

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

NTS Solitary Nucleus

OCI Overcurrent Indicator

PCB Printed Circuit Board

PNS Peripheral Nerve Stimulation

PWM Pulse-Width Modulation

SUDEP Sudden Unexpected Death Epilepsy

t-VNS Transcutaneous Vagus Nerve Stimulation

TENS Transcutaneous Electrical Nerve Stimulation

UCI Undercurrent Indicator

VHDL VHSIC Hardware Description Language

VN Vagus Nerve

VNS Vagus Nerve Stimulation

WHO World Health Organization

Contents

Chapter 1

Introduction

1.1 Epilepsy and Current Treatments

Epilepsy is a neurological disorder that causes the brain to act abnormally. Epilepsy causes as a result of these recurring epileptic seizures. These seizures can range from mild to severe, in some cases resulting in physical injury. If left untreated, seizures can occur in sleep which could result in Sudden Unexpected Death Epilepsy (SUDEP). According to the World Health Organization (WHO) [1], nearly 50 million people of all ages around the world suffer from epilepsy. This condition significantly impacts the quality of life for these people.

Current treatment options for epilepsy are mostly found in drugs. These Anti-Epileptic Drugs (AED) work by controlling the seizures or by preventing them. AED works for 7 out of 10 people, making sure that they have no more severe seizures or stop seizures completely. However, for some people, these AED do not have the desired effect. This form of epilepsy is called Drug Resistant Epilepsy (DRE). For these people, other methods are possible to control the seizures. In general, AED is also known for the side effects that are rather unpleasant and can also alter a person's quality of life. Well-known side effects due to these drugs are tiredness, headaches, and nausea.

Other treatments are more invasive. One of these treatments, also known as resective surgery, is the removal of a part of the brain that is responsible for the seizures. These surgeries are often effective but have potentially severe implications. They could influence the way your brain works, with possible implications such as loss of vision, speech, memory, or movement. The other potential form of treatment is Vagus Nerve Stimulation (VNS). VNS works by sending small electrical pulses through the vagus nerve. A device is implanted under the chest with a connection to the vagus nerve in the neck. An example is shown in Figure 1.1. The device sends regular pulses to this nerve which as a result can lessen seizures and their severity. Although VNS is a lot less risky than the other options listed before, the price is often too high for many people and is therefore still not considered too often in practice.

Figure 1.1: Sentiva VNS, adapted from [2]

Less invasive methods for VNS have been researched to stimulate the vagus nerve in a similar fashion. Transcutaneous Vagus Nerve Stimulation (t-VNS) is a method of stimulating the vagus nerve without the need for invasive procedures. t-VNS can be applied to the Auricular Branch of the Vagus Nerve (ABVN) that is found in the ear. From here it travels through the vagus nerve to the Solitary Nucleus (NTS). t-VNS is used now more in a clinical setup and is as of now not approved for the treatment of epilepsy by the Food and Drug Administration (FDA). Besides that, there are not as many dedicated t-VNS devices that use a stimulation device intended for t-VNS solely. The goal of this project is to design a dedicated small and

power-efficient t-VNS device that would lay the basis for future development in the field of portable and wearable stimulators inside the ear.

1.2 State of the art for t-VNS

t-VNS is still in very early development, and although VNS has been FDA approved for the treatment of DRE, t-VNS still lacks the data to conclude that it has the same working as the original VNS [3]. An early proof of concept study had shown that seizure frequency was reduced in 5 out of 7 patients after 9 months of t-VNS therapy [4]. Another study had shown that after 8 weeks of treatment, t-VNS applied in the ABVN treatment resulted in a 42.6% average reduction in seizure frequency but it is not as potent as VNS [5]. Although VNS might be more potent, t-VNS is more cost-efficient and more accessible.

t-VNS has not only been researched for purposes of epilepsy treatment but could also be effective in the treatment of depression [6]. The devices that are used for t-VNS are mostly centered around a Transcutaneous Electrical Nerve Stimulation (TENS) device. A TENS is used not only for t-VNS but also for other forms of stimulation such as Peripheral Nerve Stimulation (PNS). The device that is most commonly used for t-VNS in the ABVN is the NEMOS Cerbomed [7]. However, this device has been discontinued from production due to undisclosed reasons. Other than the Cerbomed, a set-up with an ordinary TENS device and custom-made electrodes are often used in practice. However, none of these setups except for the NEMOS Cerbomed are specifically designed for t-VNS of the ABVN. This would mean that the current t-VNS setups cannot be translated to outside clinical practices.
Another shortcoming of most of the current devices for stimulation is the fact that they are all open-loop controlled [8]. This means that they stimulate at regular intervals throughout the day but not specifically when it is needed. Through the reading of biomarkers, the stimulation can be done in instances where it is needed the most.

1.3 Overview of the whole project

The stimulator is a subset of a bigger project where a brain-computer interface is made for an earpiece. Figure A.1 shows the different groups. The phantom group is responsible for making an *in vitro* resemblance of the electrical properties of human skin. The authentication group reads the Electroencephalogram (EEG) signals and based on these signals can perform authentication operations. Signal processing also reads EEG signals. But their goal is to detect and perhaps predict seizures in the onset of an epileptic attack. The stimulator operates based on the signals sent out by the signal processing group. This group sets the parameters and tells the stimulator device when it should or should not stimulate. This thesis will solely focus on the stimulation but it does take into account the different signals it will receive from the signal processing group.

1.4 Document lay-out

This thesis describes the design process and the implementation of the t-VNS device. Chapter 2 gives some important background information for the project that is required for the design of the device. Chapter 3 gives a list of requirements that were followed when considering the different implementation options for the stimulator. Chapter 4 gives an overview of the entire device and the different components it consists off. After that, the components from the overview are taken a closer look at and are described with the considerations and choices that was made in Chapter 5. Chapter 6 discusses the integrated circuit design for controlling the stimulator. In Chapter 7, the simulation results are discussed. The following chapters will describe the Printed Circuit Board (PCB) implementation and conclusions drawn from the results as well as recommendations for future work.

Chapter 2

Background

The overall simplified overview of the system is seen in Figure A.2. To verify the correct working of the circuit, a testing set up is required. This testing set up will be consisting of the stimulation PCB attached to a phantom which mimicks the electrical properties of the human skin. However, in the beginning stages of the project, there is no actual human skin phantom to test with yet. Therefore, an electrical impedance model of the skin has to be made which is a simplified representation of the human skin. This model is also important for the design phase of the system, since the load gives an indication on how much voltage is needed to correctly stimulate the ear.

2.1 Impedance of the Skin

The skin is a layered system. In total, there are three prominenent layers: epidermis, dermis and hyperdermis. However, the hyperdermis is not of significance since this is too deep in the skin and it does not contain any nerves to stimulate. Therefore, only the epidermis and dermis will be considered. The epidermis consists of multiple sublayers. The most relevant to the impedance model is the stratum corneum. This layer is predominantly responsible for the high impedance of the skin and should therefore be considered in the circuit [9]. It is also important to note that the stratum corneum does not have the same thickness everywhere on the skin. It is a lot thicker on the arm than it is on the forehead for instance.

The skin has been studied thoroughly and different representations have been made on how to model the electrical properties. The most commonly used model is the Montague Model, depicted in Figure A.3. This model captures the capacitive behaviour and the resistive behaviour of the epidermis. This model has been used in a variety of studies [10], [11].

There is also a non-linear model (seen in Figure A.4) which is based on the Montague model with the difference being that the resistivity of the epidermis is now a variable resistance [12], [13]. These models capture more of the non-linear behaviour of the skin due to the current intensity. Although these models might be more effective at capturing the non-linear behaviour, the models are too sophisticated and lack the relevant data to use it in this testing set up.

Although more models have been proposed for the modelling of the electrical behaviour of the skin [9], the Montague model is widely used to this day and is still shown to be sufficient enough to model most of the important characteristics. Therefore, the Montague impedance model is the model which will be used throughout the rest of this paper.

2.2 Electrodes

For stimulating the vagus nerve through the ear, electrodes can be placed in different positions. The goal is to optimally stimulate the vagus nerve.The location to place the electrodes needs to be found in which we

can both still use the earbud as a functional earphone and be able to still stimulate the vagus nerve properly. Comfort is an important factor for clinical practice.

The neural anatomy of the nerves inside the body is quite complex. The ear is connected to the NTS by the vagus nerve. The branch that is focused on is the auricular branch of the vagus nerve. This branch is the one that has the most afferent Vagus Nerve (VN) distribution which indicate that through this branch external stimuli can be exerted on the central nervous system.

The question on which side the stimulation should occur is also an important one. The left ear is chosen as the most common side of application because the right-side vagus has efferent fibers connected to the heart, which might result in cardiovascular side-effects [14]. Therefore stimulation will also occur through the left-ear only, since the safety is a very important requirement.

Research has indicated that stimulating the cymba conchae provides the most activiations in the NTS [15] and that the general concha area is very suitable for stimulation [16]. Stimulation of both the cymba and cavum conchae in the ear have been shown to have even more promising results [17]. The reason for this is that it is one of the main ABVN stimulation sites that is available in the ear and when stimulated this area produces the largest amount of activated ABVN fibers. What is also an important reason is the results that were found with the analysis of the different locations if the amount of activity that was found in the important areas connected to the vagus nerve, namely the Locus Coeruleus (LC) neurons and the NTS. This is an indication that stimulation at this spot resulted in the strongest vagal afferent pathway in the brainstem. It was found that the cymba conchae and cavum combination were capable of receiving a stronger intensity and, thus may offer an advantage over the inner tragus during long-term t-VNS treatment.

Not only is this position optimal for stimulation, it is also an ideal location to place the electrode considering it will be used in earphones. Earphones are often already placed against the cymba conchae and the addition of electrodes on the earphone can be placed in a manner that makes for a good integration. Therefore, the cymba conchae is the optimal place for the electrode to be placed. The size of the electrodes have to be in accordance with what would fit in the ear. The area that is desired is roughly 1 cm^2. This would fit in the ear in the desired areas, namely one in the cavum conchae and one in the cymba conchae [17].

There are a variety of different types of electrodes: surface-electrodes (dry or wet), capacitive electrodes and needle electrodes. What distinguishes these electrodes is mostly in the the way they are connected through the skin. Surface electrodes are connected to the top of the skin with either no conductive gel or with conductive gel. Needle electrodes are electrodes that have very small needles that penetrate through the top-layer of the epidermis: the stratum corneum. In terms of impedances, electrodes can be considered as good conductors. This means that they have considerably low resistances. However, there are situations in which it does not just operate as a resistance.

2.3 The electrode-skin model for the testing ground

The connection between electrode and skin can be done in a variety of ways. As indicated, for each different type of electrodes there is a different model that is created. The model that will not be considered is the capacitive electrode. This is because capacitive electrodes for stimulating purposes require very high voltages that exceed levels that would be able to generate in a small earpiece. Therefore these forms of electrodes will not be used.

The wet surface electrode can be found in Figure A.5. The electrode in this model has a parallel capacitance. This originates from the double layer capacitance that occurs when an electrode comes into contact with an electrolyte gel. This causes a charge separation and therefore a capacitance. The electrolyte itself has a resistance and the impedance model is as was mentioned before in section 2.1.

The dry surface electrode can be found in Figure A.6. The reason that this electrode is purely modelled as a resistance is because the double layer capacitance is too small to consider. Therefore it is displayed as a

pure resistor.

Skin abrasion is not an option in the case of developing the model. The reason for this is that this would not be a suitable option since the stratum corneum regenerates regularly [18]. This would mean that every so often, the skin has to be abraded inside the ear. Skin abrasion is not comfortable and has to be repeated since the stratum corneum regenerates, which would make it a cumbersome activity.

Since skin abrasion is not an option, the stratum corneum will remain as an impedance in the model. Since the dry electrode does not improve the stratum corneum the impedance for this model will be too large to be considered [19]. The electrolyte for the wet electrode improves the impedance of the stratum corneum. This gives values that are better suited for the project [19]. The wet electrodes are suited for the project but they have problems. First and foremost is that gel has to be applied to the ear each time it is applied. The second is that they probably would not stick quite well when wearing them in the desired location, which makes it difficult to put them in the ear. For these reasons, wet and dry electrodes will not be considered for this project.

Then the only option that is left is that of a needle electrode. This electrode works by penetrating the top layer of the skin, which would cause it to skip the top layer of skin, the stratum corneum. The layers underneath the stratum corneum are far less resistive and is therefore a suitable final option. Since this can be seen as removing the stratum corneum (such as abrasion), values taken from [20] and using the same model for the needle electrode as for the dry electrode in Figure A.6, the used final model can be seen in Figure 2.1. Values can be found in Table A.1. Important to note is that there are different values noted that paper. The worst case scenario is taken so that the circuit can stimulate for all cases mentioned in that paper.

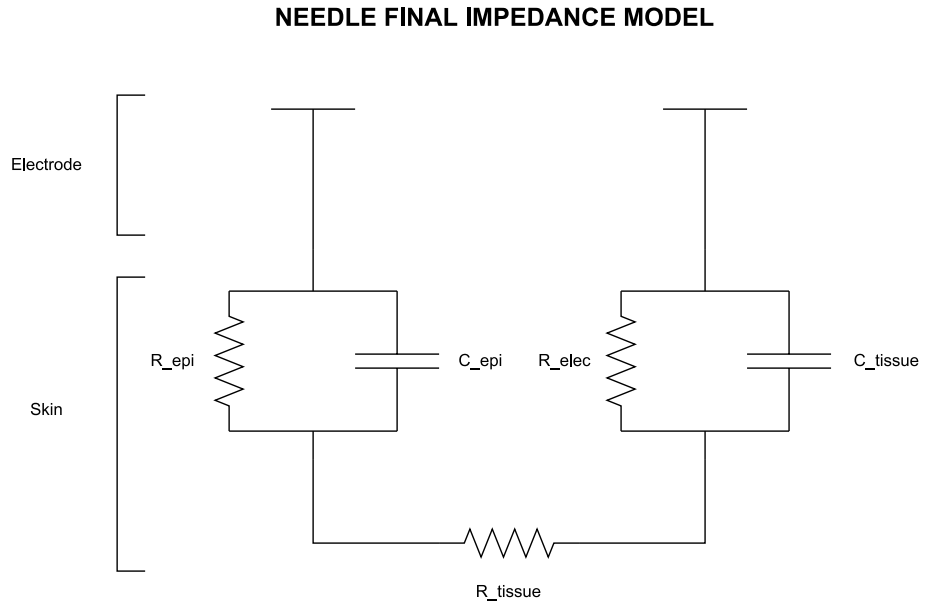

Figure 2.1: Final impedance model accounting for 2 electrode connections

The reason that there is no R_{elec} is because relative to the other resistances, this is negligible. An electrode is considered a good conductor and is therefore not considered in this impedance model.

Although this is the correct model that should have been used, a different model was used to calculate the design parameters of the circuit elements. As such it will be used as the load characterization for the rest of the thesis. This old impedance model, however, did not differ a significant amount from the correct impedance model. This old model is shown in Figure A.7. The reason this model is wrong is because of

the fact the way the electrodes are modelled. The electrodes as they are depicted here resemble more of the impedance model as shown in Figure A.5. However, this only occurs when there is an electrolyte of significance in the layer underneath the electrode or when these values are known. During the process of designing this model, a confusion lead up to this mistake. Unfortunately, there was not enough time in the end to change this and therefore recommendations will be given for the future in chapter 10.

2.4 Wave Characteristics

Electrical nerve stimulation can be done with different stimulation wave forms. A large variety of research shows that square waves are commonly used for vagus nerve stimulation just like existing devices on the market. In addition, most research is available for the stimulation parameters of square waves [21], [22]. Furthermore, from the electronic design point of view a square wave is easier to generate in contrast to other wave forms like sine waves or triangular waves. As a result less components are required for generating the wave which could safe power as well. Therefore the stimulation waveform generated by the stimulator will be a biphasic square wave. The wave parameters of the square wave that will be used in this report are defined in Figure 2.2.

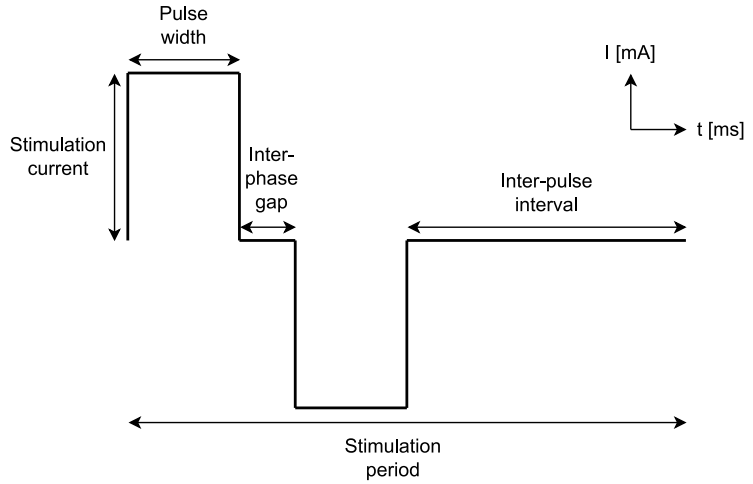

Figure 2.2: Definition of wave parameters

Research has shown that stimulation currents in the range of 1 mA until 10 mA are the most effective for t-VNS. However, Stimulation currents above 10 mA have to be avoided [17]. Stimulation frequencies in the range of 20-30 Hz are optimal for t-VNS, but stimulation frequencies of 50 Hz or higher have to be avoided since this can cause major and irreversible damage to the vagus nerve [23].

Regarding the pulse width of the stimulation wave form, the optimal value is still not known. However, pulse widths in the range of 100-500 μs are proven to be effective for epileptic treatment. According to [24], a variety of research confirms that a pulse width around 200 μs must work for epileptic treatment. Therefore a pulse width of 200 μs is chosen for the stimulator.

Inter-phase gaps are often used in electrical stimulation devices to try to enhance neural stimulation efficiency by reducing the action potential. However, research has shown that introducing an inter-phase gap requires higher stimulation intensities compared to stimulation without an inter-phase gap to obtain the same results [25]. As a result, more power is consumed to achieve the same results. Since power efficiency is the main focus of this project, the inter-phase gap will not be present.

When stimulating human nerves, charge balancing is the most important safety factor. Applying a DC current to the skin for a longer period can cause pH change, electrode dissolution and tissue damage [26].

In order to avoid charge buildup, the stimulation waveform must be biphasic such that net zero charge appears on the electrode-skin interface. However, due to the capacitive electrode-skin interface, electric charge is stored during stimulation which can be solved by introducing passive charge balancing [27]. In other words, the load must be fully discharged before sending a new stimulation pulse to prevent charge buildup. Therefore the inter-pulse interval must be longer than 5 times the time constant of the electrode-skin interface such that the system is in steady state before simulating again to prevent charge buildup.

To get insight on the required voltage over the load for the discussed waveform, the following measurements have been done in simulations: Using the impedance model created in section 2.1 and a current source the voltage over the load can be measured. Due to the capacitive properties of the load, it is important that the current pulses sent through the load are similar (especially the pulse width) to the current pulses that were previously discussed. Measurements are done at the end of each pulse at the peak of the voltage. As described in section 2.1, the parameters for the load can be divided in three categories: The minimum load case, the general case and the maximum load case. The voltages at different drive currents for these cases can be found in table A.3. In conclusion, when taking worst case values for the load a maximum voltage of 65.8 V is required for stimulating with 8 mA.

Chapter 3

Programme of Requirements

The requirements listed out in this chapter offer a basis as to how the stimulation should perform based on the research discussed in Chapter 2. The requirements are categorized in functional and non-functional. The functional requirements indicate how the stimulator must work where as the non-functional requirements indicate how the stimulator must perform. The functional and non-functional requirements are listed in sections 3.1 and 3.2, respectively. The requirements are explained in Section 3.3.

3.1 Functional Requirements

1. The system should be powered by a battery
2. The stimulator must be able to read the required stimulation current and frequency as input parameters at 3.3 V from a microcontroller
3. The stimulator must not inflict pain or cause an unpleasant feeling when used as indicated

3.2 Non-Functional Requirements

1. The stimulator must output a biphasic current-mode square wave
2. The current amplitude must not exceed 10 mA
3. Using the previously described impedance model of the skin as a load, the current amplitude must be adjustable in a range from 0 mA to 8 mA with a step size of 1 mA
4. The pulse frequency must be adjustable in a range from 10 Hz to 40 Hz with a step size of 5 Hz
5. The pulse width of the stimulation pulse must be 200 μs
6. The inter pulse interval must be chosen such that the system is in steady state before simulating again
7. Active power consumption must be less than 1 W
8. Active and static power consumption must be minimized without compromising safety
9. The size of the stimulator must be minimized without compromising power consumption

3.3 Requirement Explanation

As mentioned earlier, the stimulation circuit will be placed in a wearable application. Therefore the power source has to be a compact battery.

Since the impedance of the ear is dependent of multiple factors and is highly subject to change, it is of high importance that the stimulator generates a constant current that is independent of the load in the range that is applicable for this in-ear application. As discussed in Chapter 2.1, in worst case a maximum of 65.8 V is required to stimulate with 8 mA. In other words, the stimulation current must remain constant in this voltage range.

Currents above 10 mA, or frequencies above 50 Hz must be avoided since adverse effects due to electrical stimulation are mainly caused by stimulating with higher currents or frequencies [17]. Therefore the stimulating device must shut down automatically when currents higher than 10 mA are measured. In addition, the device must send a fault signal indicating that it is not stimulating anymore.

For both research and clinical purposes, the device must have both adjustable stimulation current and frequency. The effectiveness for a certain stimulation current can differ per person. Therefore the stimulation current must be adjustable in a range from 0 mA until 8 mA with a step size of 1 mA. The frequency must be adjustable in a range from 10 Hz until 40 Hz with a stepsize of 5 Hz. So the device must able to read the required values for the stimulation current and frequency from a micro controller.

The main design focus of the stimulator is power efficiency. To be able to use an in-ear t-VNS device in practice, the device must be able to operate for a day or longer without replacing the battery. Therefore minimizing the power consumption is the most important factor when designing the stimulator. However, minimizing the power consumption must never affect the safety of the device.

Chapter 4

Design Overview

The entire design overview of the stimulation device is depicted below. This overview shows all the components involved in the stimulator. These components will be briefly covered in this section and most of them will be elaborated further in other sections. The components that are not mentioned in future chapters are not designed by us and will therefore be covered in this chapter.

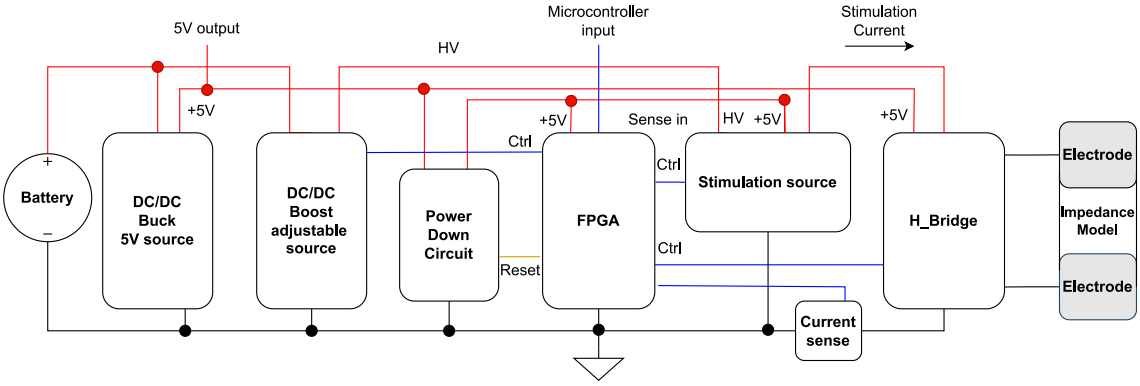

Figure 4.1: The design overview of the stimulator

Battery
The battery will provide the stimulator circuit and other all other components with power. Since the goal is to make this device portable and wearable, it is important to select a battery that has a high energy density, meaning that it takes up minimal area while still providing sufficient energy.

Lithium batteries are currently the best in terms of power and energy density on the market and is the most commonly used form of battery in modern technology [28]. One lithium polymer cell can deliver between 3.2 V - 4.2 V. The technology of lithium polymer is ideal for this project because it provides high energy density and is very lightweight. For wearable applications, this is ideal. They can also be very versatile in shape and size, which would make it very suitable for shaped earpieces and more

Since a high voltage of precisely 65.8 V (as can be seen in A.3) is required for the current source and a low voltage of 5 V is required for controlling the Field Programmable Gate Array (FPGA), a 3s Li-battery with a voltage between 9.6 V and 12.6 V will be used. This is suitable middle ground between the high and low voltage required for the operation of this device.

Buck and Boost Converter
Different components on the board operate at different voltages. 5 V is used to operate logic level components in the current source, H-bridge and other components in the ear piece. A high voltage (more than 65.8 V) is required to drive the load. Therefore, a buck and boost converter are both necessary to regulate the voltage from the battery (9.6 V - 12.6 V). The designs of these converters can be found in the Sections 5.4 and 5.5

Impedance Model & Electrodes
The stimulation will happen to the skin of a human being, specifically the ear. To accurately determine whether the design is working and the stimulation is according to the requirements a testing site has to be made. The electrodes that will be used for the stimulation also influence the impedance model. An in-depth explanation of this is already given in section 2.3

Stimulation Source
The stimulation source is responsible for safely sending an accurate current through the electrodes through the skin. To get an accurate current, a variety of measures have to be taken to make sure that the current through the skin does not depend on the impedance of the skin itself. A more in-depth explanation is given in section 5.1

H-bridge
In chapter 3, it was listed that the stimulation wave has to be biphasic and square. The H-bridge (also known as full-bridge) is a method of alternating the current through a load, thereby creating the biphasic behaviour that is desired. The design will be explained in section 5.3.

Current Sense
The current sense circuit is the part of the circuit that is responsible for measering the current through the H-bridge. The reason of implementation of this component is efficiency (which will be discussed in sections 5.5 and C.5) and safety of the device. The design and working of the circuit will given in section 5.2.

FPGA & Integrated Circuit
The FPGA will be responsible for housing all the control logic. The FPGA will be used as testing device to make sure that not only the circuit but also the code that is going to be written is correct. The model that will be used for testing is the Digilent CMOD A7 [29]. Although an FPGA is used, it will only be used for testing. The goal is to house all the logic that will be written on the FPGA on a dedicated Application Specific Integrated Circuit (ASIC). This would remove the circuit board of the FPGA.

For writing the VHSIC Hardware Description Language (VHDL) code, Finite State Machine (FSM)'s are designed. This information can all be found in chapter 6

Power Down
The power down circuit is responsible for making sure that not only there is almost no static power dissipation but for also assuring that the FPGA starts up properly when it receives power. This is important as power efficiency is a big factor for this project as well as safety. This small component improves both of these factors and will be further explained in section 5.6.

Chapter 5

Circuit Design

5.1 Stimulation Source

To send electrical pulses through the skin an electrical source has to be chosen. The stimulation source can be either a voltage source or a current source. Current amplitude is a very important parameter for stimulating the vagus nerve. The current controlled stimulation showed to have better controllability [30] [31] which is an important consideration since the human body is used as load. Also, current sources are in general load independent given the correct range of impedances that the load can achieve. Of course, if the load exceeds the maximum permissible amount and the voltage reaches a limit then the current will drop. Considering the fact that the stimulator should be load independent for the given range and given the controllability advantages of a current source, this will be the one that is used for the stimulator.

The current source has to adhere to the following characteristics:

- The current source has to be easy to control by an FPGA
- The current source should deliver a current with a margin of $\pm$ 0.2 mA
- The current source should have a very high output impedance making it independent of the load
- The current source must be adjustabel in a range from 0 mA to 8 mA with a step size of 1 mA.

5.1.1 Current Source Implementations

The first option that was considered is the Howlard current pump. This is a very precise current source that is both able to sink and source current. A schematic can be seen in Figure 5.1.

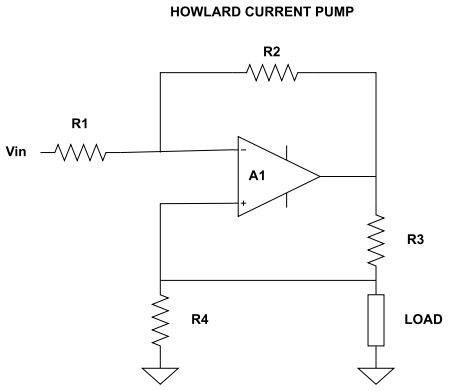

Figure 5.1: Howlard Current Pump

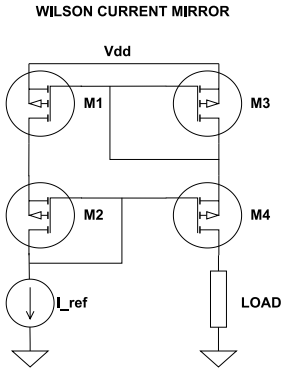

Figure 5.2: Wilson Current Mirror

The Howlard current pump can do both things for the use case of a vagus nerve stimulator, since it can generate a biphasic wave without the need for other components. However, there are some difficulties for

the usage of a howlard current pump for the purposes of the stimulator. First of all it requires a very high supply voltage to the amplifiers operate, which should be substantially higher than the voltage required over the load. Since the voltage that should be aimed for is around 65.8 V for maximum load, this would mean that a power supply voltage of roughly 70 V is required. Op amps with these specifications are extremely hard to find and consume a lot power. Besides that the resistors in the setup for the Howlard current pump required to be very precise since the feedback would otherwise be off which would result in an inaccurate gain. Due to these issues the Howlard Current Pump will not be used as the current source.

The other option that was found is a current mirror seen in Figure 5.2. A current mirror means that the desired current is "mirrored" to the other side of the circuit. The reference current pulls the transistors to a gate voltage such that the gate to source voltage is at the value for the reference current to flow through them. At the same time, it pulls the mirrored gate to the same voltage, forcing it to conduct the same reference current. As such, the current is mirrored. Important for the correct working of the mirror is that all transistors are in saturation and required gate to source voltage determining the current that flows through them. The Wilson current mirror is an adaptation of the original current mirror which improves the output impedance of the original current mirror.

The current mirror can be made with either a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) or a Bipolar Junction transistor (BJT). To choose the right transistor for this purpose, the requirements are checked. The main requirement is power efficiency. As BJTs draw base current, power is dissipated for turning on the BJT. MOSFETs are more power efficient than BJTs and they are smaller in size as well. Although BJTs are faster, switching of the current mirror does not happen very quickly and is therefore not a priority for the design. Therefore, MOSFETs are chosen as the transistor technology

Multiple versions of current mirrors can be made. Besides the Wilson current mirror, the cascode current mirror is also an option. However, it was stated in a paper that a Wilson current mirror had the highest bandwidth out of the two mirrors with negligible differences in other areas [32]. Since the cascode current mirror had similar performance in terms of output impedance and error accuracy, this could have also been used. Both adaptations are acceptable in terms of performances.

To further improve the Wilson current mirror, it can be modified to provide multiple outputs (BJT wilson current mirror with multiple outputs given in [33]). This mirror can be seen in Figure 5.3. The reason for adding multiple outputs is because the reference current can then be smaller. The reference current also consumes power but that power is considered wasted as it is not directed towards the load. The efficiency of the Wilson mirror in Figure 5.2 is roughly 50%, since the same current flows through both reference and output both originating from the Vdd. With the improved version in Figure 5.3, this efficiency rises to roughly 83.3%. This is a significant improvement over the original amount. However, this brings up the question why not add in more than 5. This is due to the constraints of size and efficiency. Adding additional transistors would significantly limit the amount of space on the board. This would also not increase the amount of efficiency that significantly. Doubling the amount of outputs would give an increase of 6.7%.

In a current mirror, the reference current determines the current that is mirrored to the other parts of the mirror. It is important that this reference current can be controlled. This would require a variable voltage source to be used. The current range that is given in chapter 3 mentioned that stimulation from 0 to 8 mA should be controlled in steps of 1 mA. The solution for this problem is given below.

The Digital to Analog Converter (DAC) takes a serial bit value as its input from which the reference voltage can be derived. This gives the corresponding output voltage which maps to the desired current with the following formula:

$$I_{ref} = \frac{V_{in}}{R_1} \tag{5.1}$$

To calculate the resistance value R_1, the equation above is used. Given the maximum value of the DAC (which is 1.24V) and the maximum reference current, a value of 775 Ω is retrieved. To make sure that the resistance always falls in the range of the DAC, a resistance of 681 Ω is used as the reference resistance. The complete current source is displayed in Figure 5.3 with the reference current source

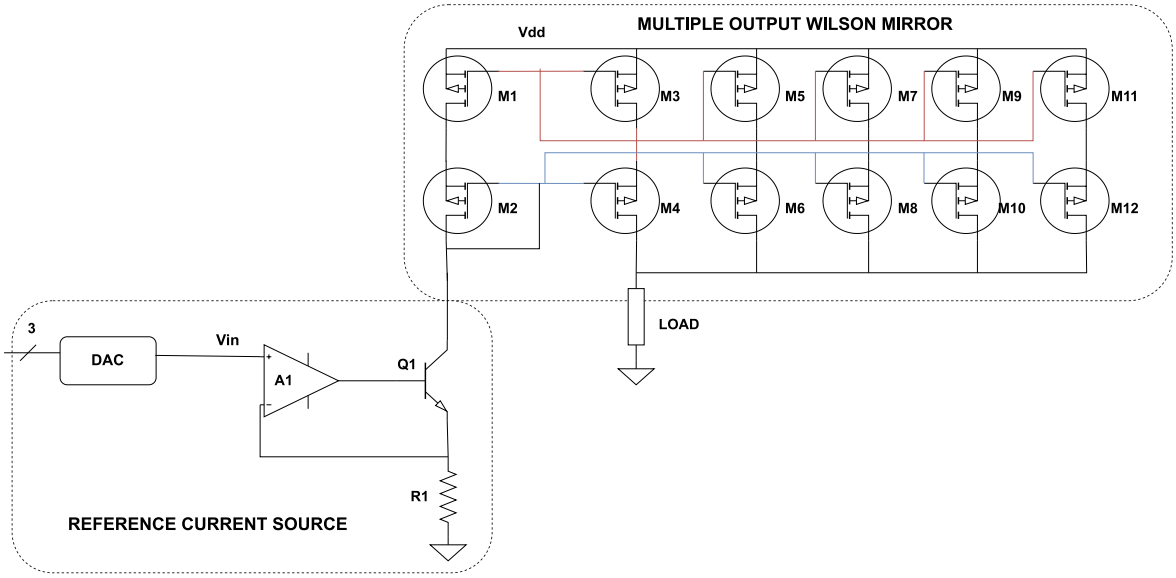

Figure 5.3: Complete current source with current mirror and reference current

5.1.2 Results

The power efficiency is almost always exactly the 83.3% that was mentioned before. Figure 5.4 shows that the current is correctly mirrored. It can be seen that at the timestamp shown, the current is almost exactly 5 times the reference current. This means that it is working as expected. Noteworthy is the delay between the reference current going to its appropriate value and then the current mirror going to the appropriate value. This delay is most likely an issue due to the fact that the gates of the mirrors need to be pulled to the

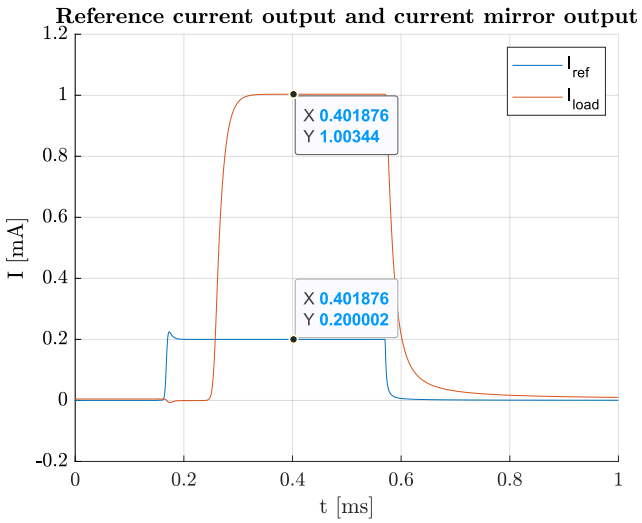

Figure 5.4: Reference current of 0.2 mA mirrored and multiplied 5 times

level needed to conduct the reference current. This takes time since there are a lot of gates that need to be charged. In the final design this will not be much of an issue since the current mirror has a startup phase before going through the load. This means that the current is at the correct level as soon as stimulation is supposed to occur. This will be further explained in section C.2.

Table B.2 in the appendix shows the currents and the error that are measured through the old load model as indicated in section 2.3 with the maximum voltage of 70 V as supply as indicated in section 5.5. The shift from positive undershoot to negative undershoot is one that is difficult to explain. A possible explanation for this might be due to the fact that when there is more current flowing through the transistors, the gates of the transistors need higher voltages for the currents to match up proportionally. This draws current away from the other gates, which could result in the drop in the current. These deviations can be accounted for by changing the value through the DAC, which gives a slightly higher or lower reference voltage to get a higher or lower reference current. The table does indicate that the current source in Figure 5.3 is working correctly.

In terms of power dissipation, Table B.1 shows the results measured for different currents with a constant voltage source of 75 V. Noteworthy is the fact that the power efficiency decreases a lot when the stimulation current is low. This is mostly due to the fact that there is a lot of dissipation in the mirror when there is stimulation from a constant voltage source. When the maximum current is achieved, the power efficiency is at a very reasonable value of roughly 75%. With this comes a power drawn from the source of 351.73 mW.

5.2 Current Sense

The current sense accurately measures the current through the H-bridge and current mirror which corresponds to the current through the load during a stimulation pulse. With this information, the FPGA can detect undercurrent and overcurrent which is necessary for proper functionality of the circuit and to satisfy the mandatory safety requirements.

The FPGA which is used in this design has a built in Analog to Digital Converter (ADC) which translates voltages between 0 V and 1 V to a 12-bit binary number. It will be used to create binary information from the current. The ADC expects an input of 0 V to 1 V which means that the current range that is of interest should be mapped to this voltage range. In this case we will consider a current range of 0 mA to 10 mA since 0 mA to 8 mA is the active current range in which stimulation takes place and 10 mA is the maximum allowed current according to the requirements.

5.2.1 Current Sense implementations

Mapping current to voltage can be done with a sensing resistor, which is a small resistor in the series path of the current that has to be measured to induce a small voltage over it. Three different implementations were considered. They can be found in figure 5.5.

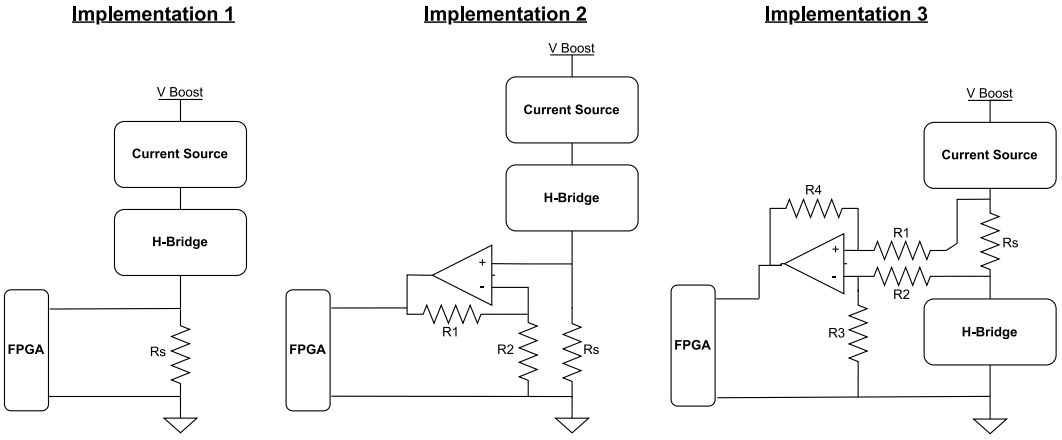

Figure 5.5: The three considered current sense implementations

The first and the simplest implementation chooses Rs in such a way that 10 mA of current through Rs will create 1 V over Rs (Rs=V/I). This implementation is only accurate if the FPGA's ADC has a high input impedance and thus draws an insignificant amount of current. However, this is not the case, the on-board ADC functions by charging and discharging a capacitor which consumes current. How much is not stated in the datasheet [29]. Measurements will be less accurate when not adding a buffer. Placing the sensing resistor under the H-bridge also increases the ground potential seen by the H-bridge. In this case by 1 V in case of a 10 mA current relative to the real ground. Depending on the transistors used in the H-bridge, this could influence performance. Excluding the power consumption of the ADC, the circuit would dissipate at most 8 mW.

The second implementation seperates the output voltage and the voltage over Rs by means of an operational amplifier. Because of the high input impedance on the input of the amplifier, current over Rs is mapped to a voltage in a very accurate way since practically all current flows through Rs. Furthermore, the operational amplifier is able to amplify the voltage over Rs which allows Rs to be smaller to get the same voltage range of 0 V to 1 V on the output of the amplifier which reduces the power dissipation in Rs. Decreasing Rs reduces the rise of the ground potential seen by the H-bridge which allows for faster switching times and an increase of the rise and fall time. This implementation trades Rs size and simplicity for a more accurate current measurement and a decreased voltage rise of the ground seen by the H-bridge.

In the third implementation option, the sensing resistor is placed above the H-bridge eliminating the voltage rise of the ground seen by the H-bridge which means that the gate to source voltages on the MOSFETs are always exactly the same and as high as possible. However, this method comes with a significant trade off which is introduced by the differential amplifier. This amplifier needs to handle the voltage levels at Rs relative to real ground which could be as high as 70 V. These high voltage amplifiers are very inefficient, often not rail to rail, very large and they are due to the chip shortage often not available. Therefore this is not an option for this project.

To maximize power efficiency (to satisfy the requirements in chapter 3.3) and minimize the rise of the ground potential of the H-bridge, implementation 2 will be chosen. Rs will be minimized and the voltage gain of the amplifier will compensate for the decrease in voltage over Rs. A 10x gain was chosen since from a simulation it appeared that the difference in circuit characteristics of the H-bridge was negligible at 100 mV ground potential compared to 0V ground potential. The component values for this implementation can be found in the appendix in table B.5.

5.2.2 Simulation Results

The designed circuit was modelled in LTspice (without a model for the FPGA) for currents between 1 mA and 10 mA. For each measurement, the output voltage, the current supplied to the operational amplifier and the voltage over Rs were measured. With these measurements, the total power consumption has been calculated. The results can be found in table B.6.

As can be seen from the last column, the maximum power dissipation in the active stimulation range occurs at 8 mA drive current and is equal to 1.8 mW which means that this implementation surpasses the first implementation when considering power consumption. Important to note is that the bias voltage of the amplifier is clearly visible in the output voltage which is read by the FPGA. The output voltage is in most cases 2 mV and in some cases 1.9 mV lower than calculated. This deviation can be accounted for in the FPGA.

5.3 H-bridge

An H-bridge is a simple and power-efficient way of transforming a Direct Current (DC) into a square wave through the load. Therefore, an H-bridge circuit will be used for transforming the DC current generated by the current source into a biphasic square wave through the load. However, due to the high voltages regulated by the current source in the order of 66 V, the high-side MOSFETs require high gate voltages to operate. This is a problem since the control signals generated by the FPGA will operate at only 3.3 V. There are multiple solutions to tackle this problem.

5.3.1 H-Bridge Implementations

Two possible implementations of high-side switching circuits are shown in Figure 5.6 and 5.7.

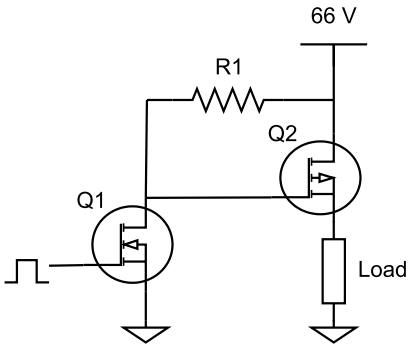

Figure 5.6: High-side switching circuit with a P-channel MOSFET

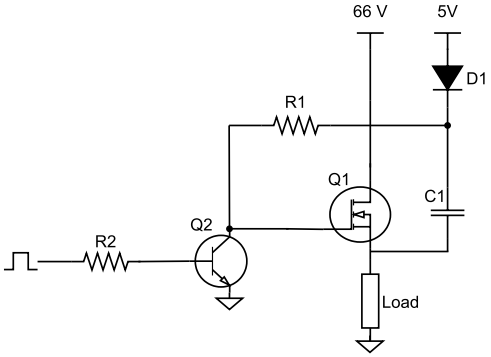

Figure 5.7: High-side switching circuit with bootstrap

In Figure 5.6 a high-side switching circuit based on a P-channel MOSFET is shown. Here, V_{gs} is either 0 V or the negative supply voltage generated by the current source. However, power efficiency is a problem when high voltages in the range of 66 V or even more are regulated by the current source. Simulations showed that R1 must not exceed 10 kΩ to achieve acceptable switching times. As a result, as soon as the gate of Q2 is pulled to Ground (GND), a current of 6.6 mA is leaking straight to GND at 66 V. The power loss due to the current leakage to the GND with R1 = 10 kΩ is calculated below. The power loss due to Q1 is neglected.

$$P_{loss} = \frac{V_{source}^2}{R_1} = \frac{66^2}{10 \cdot 10^3} = 435.6\ mW \tag{5.2}$$

Another possible solution is using a bootstrap circuit to drive the gate of an N-channel MOSFET as shown in Figure 5.7. This circuit operates as a step-up charge pump which adds the supplied voltage over C1 to the applied voltage at the drain of Q1 resulting in the gate to source voltage being equal to the voltage over C1. Simulations showed that R1 should have a value of at most 10 kΩ to achieve fast switching times. This implementation is way more power-efficient since the voltage drop over R1 is approximately 4.3 V when shorted to GND (assuming a voltage drop of 0.7 V over D1), resulting in a power loss due to the current leakage to the GND through R1 of only 2.73 mW when taking the base current of Q2 into account as well.

Finally, optocouplers were considered for high side switching. However, optocouplers typically require more than 1 mA forward current which will leak straight to GND. At 3.3 V the power loss for this application will be 3.3 mW or more, which is already higher than the power loss of the bootstrap application due to current leakage to the GND. In addition, optocouplers with low forward current were mostly not available at this moment.

In conclusion, the bootstrap circuit is the most power efficient way for driving the high-side MOSFETs. The final implementation of the h-bridge with bootstrap circuits is shown in Figure 5.8.

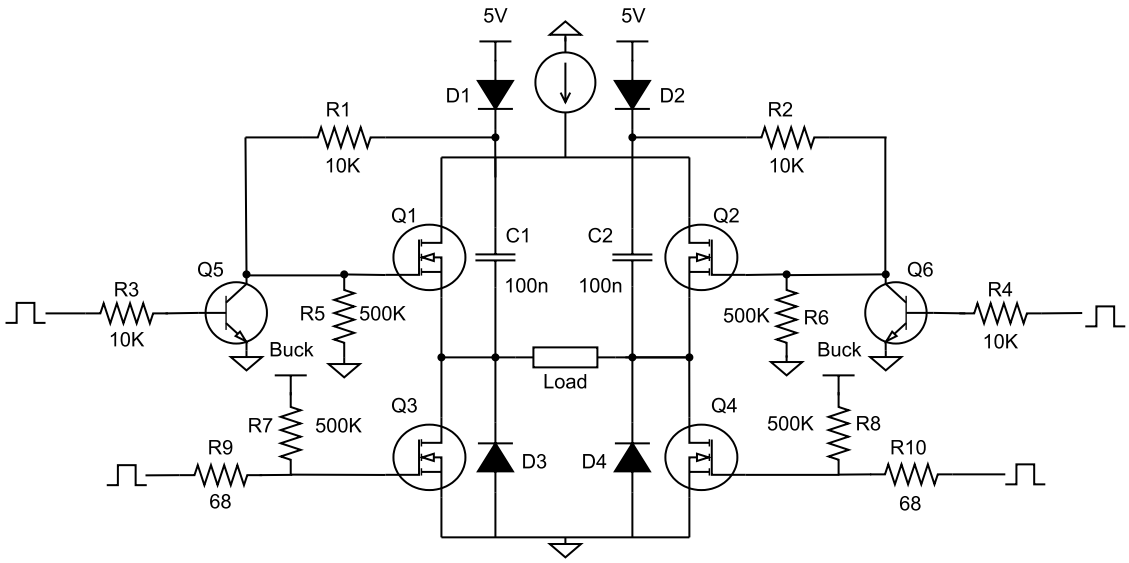

Figure 5.8: H-bridge with bootstrap circuit

As can be seen in Figure 5.8, the bootstrap circuits are connected to a 5 V supply coming from the Power Down Circuit, which will be discussed in Section 5.6. The MOSFETs are all separately controlled by the FPGA to be able to control switching timing independently. The switching timing will be discussed extensively in Section C.2. Furthermore, the gates of the high-side MOSFETs are connected to a pull-down resistor and the gates of the low-side MOSFETs are connected to a pull-up resistor. The pull-up resistors are connected to the 5 V buck converter which is always turned on in contrast to the 5 V supply from the power down circuit. As a result, when no simulation is performed the high-side MOSFETs will act as an open circuit and the low-side MOSFETs act as a short circuit. This way the capacitive load is able to discharge through either D4 and Q3, or D3 and Q4 to ensure charge balance in the skin.

5.3.2 H-Bridge Simulations

The h-bridge as shown in Figure 5.8 is simulated together with the current source as discussed in Section 5.1, and the impedance model with worst case values as discussed in Section 2.3. The final selected components are summarized in Table B.4. The current source is configured such that it produces a current of 8 mA. The simulation results are shown in Figure B.1. As can be seen in the figure, the h-bridge approximately generates a square wave through the load. However, a current peak is present at 0.4 ms which can be explained by the discharging capacitive load. From 0.2 ms until 0.4 ms the capacitive load is charged resulting in a current peak due to discharging when the polarity is switched. Furthermore, at 0.6 ms the discharging effect of the load can be observed as well. Therefore the inter-pulse interval is required to ensure charge balance.

The power loss of the h-bridge can be obtained by comparing the power generated by the sources and the power dissipated by the load. The average power generated by the sources and the power dissipated by the load were found by measuring the average voltages and currents during continuously stimulation. The cumulative average power generated by the sources is 235.8 mW while the power dissipated by the load is 231.2 mW resulting in a power efficiency of 98.05%

5.4 Buck Converter

The FPGA, the H-bridge, the Stimulation source and other potential circuitry that will be present in the ear-piece (which is out of scope for this thesis) all require a stable 5 V supply voltage for proper operation. It is therefore essential to regulate the voltage of the battery. Besides the requirements discussed in chapter 3, this DC/DC converter has the following requirements:

- Input voltage range of 9.6 V - 12.6 V
- Output voltage regulated at 5 V with a maximum deviation of 100 mV
- Maximum output current should be 3 A

5.4.1 Buck Converter Implementations

Since battery voltage is in all cases higher than the output voltage, a step down voltage regulator will be used. Two different implementations have been considered in the design.

The easiest way to step down voltage is by using a linear regulator. A Linear Dropout regulator (LDO), is an example of such a linear voltage regulator. They are small in size, very accurate, available as an Integrated Circuit (IC) and they are often used when the supply voltage is close to the regulation voltage. This is usually the case since the power consumption of the LDO increases linearly with the difference between the supply and output voltage. According to [34], the power dissipation can be described by the following formula where I_o and V_o are the output current and voltage, V_i is the input voltage and I_q is the quiescent current of the regulator.

$$\eta_{LDO} = \frac{I_o V_o}{(I_o + I_q)V_i} \cdot 100\% \tag{5.3}$$

From this equation can be derived that in the best case, with a battery voltage of 9.6 V and no quiescent current, the efficiency is 52.1% and only decreases when the battery voltage becomes higher.

Another option is to use a switch mode step down converter such as a buck converter. Buck converters consist out of an electrical switch, a diode, an inductor and a capacitor. They are relatively large in size but they can, depending on the load conditions, reach an efficiency of over 90%. Since efficiency is the main focus of this thesis, the buck converter implementation is chosen. The LM2576 regulator IC is used to minimise the size of the buck converter and reduce the designs complexity. Due to the chip shortage, higher efficiency buck converter topology IC's were not available. The efficiency at 12 V input and 3 A load current is 75% according to its datasheet [35]. The typical 5 V application circuit schematic from the datasheet can be found in figure 5.9 and the corresponding component values can be found in table B.7

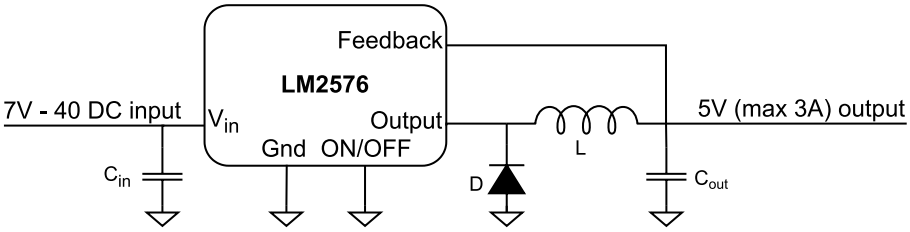

Figure 5.9: LM2576 5 V regulator schematic

5.5 Boost Converter

The boost converter will supply the voltage that is required by the load and current source to be driven at the specified drive current. From the results in table A.3 it becomes clear that the voltage range over the load at the desired stimulation currents is very large and ranges from 2.16 V and 65.8 V. A practical, non-ideal current source such as the Wilson current mirror that was discussed in section 5.1, 'absorbs' the difference between the supply voltage and the voltage over the load at the required drive current which means that there is power dissipation in the current mirror which is linearly proportional to the difference between the supply voltage and the voltage over the load. To minimize power dissipation and improve the efficiency of the design, a digitally adjustable voltage regulator which minimizes the voltage over the current mirror is implemented in the design.

The following requirements are relevant for the design of the boost converter:

- Input voltage range of 9.6 V - 12.6 V
- Output current of 0 mA to 8 mA
- Design for the complete load voltage range but optimize for the average case.

5.5.1 Boost Converter Implementations

Considering the battery has a voltage between 9.6 V and 12.6 V and the voltage range of the load is between 2.16 V and 70 V one could say that it is straightforward to use a buckboost converter which is able to step up and step down the voltage. This is not necessarily the case. The converter should be designed to provide a high enough voltage to provide the load over the entire impedance range to ensure the stimulation current range but for better power characteristics, the general case should be optimized. Having the option to step down power only optimizes the general case with a drive current of 1 mA. However, this is not directly a reason to not use buckboost. The downside of using a buckboost converter is it's duty cycle which is always larger than the duty cycle of a boost converter. Large duty cycles cause larger power losses. Furthermore, buckboost converters require an electrical switch which is not connected to ground. This complicates the circuit, takes up space and consumes power as well. For these reasons, a boost converter is chosen.

Boost converter IC's similar to the buck converter IC discussed in section 5.4 are unfortunately not available due to the chip shortage. There are very few IC's available that can handle 70 V output voltage and many of them were out of stock or could not deliver the desired voltage range. Therefore, the choice was made to generate the Pulse-Width Modulation (PWM) signal for the switch on the FPGA. This also makes it easy to actively change the duty cycle to control the output voltages according to the load. The circuit schematic of the boost converter can be found in figure 5.10

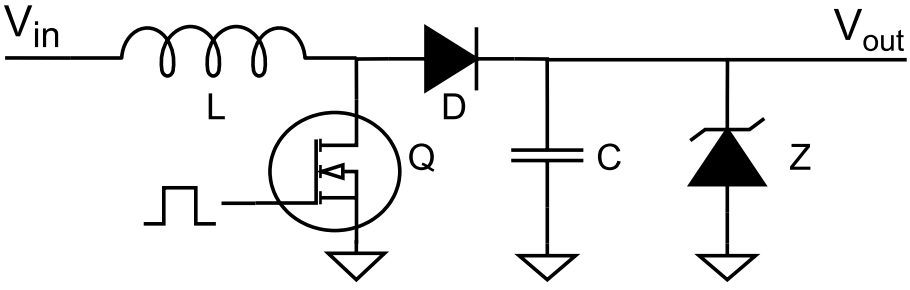

Figure 5.10: General Boost converter circuit schematic

5.5.2 Simulation results

Simulations have been done in LTspice. A non ideal current source has been connected as the load to simulate the load the boost converter should be able to handle in the real application. The simulations are done with LTspice models of real components. A list of those can be found in table B.8 and their value calculations can be found in the appendix in section B.5.1. The values for the capacitor and inductor are larger than calculated to create headroom for possible inaccuracy in the components or in the formula's. To determine the worst case performance of the boost converter, simulations were done for every possible duty cycle and drive current with an input voltage of 9.6 V. The following parameters were measured: output voltage (table B.10), current through the zener diode (table B.11) and input current (table B.14). From these simulations, the efficiency can be calculated which can be found in table B.15.

These same simulations have been done for the maximum input voltage of 12.6V but only for the the high duty cycle cases to get insight in excessive voltages and currents. These results can be found in the tables B.16, B.17, B.18, B.19 and B.20.

The first thing that should be noted is the steady state current in the zener diode. When currents become too high for an extended amount of time, the power rating of the zener diode may be exceeded. The power rating of the used diode is 1 W which relates to 13.3 mA at the zener voltage of 75 V. This value for the current is only exceeded at 85% duty cycle at 12.6 V input. Running the boost converter at this duty cycle will damage the circuit. A possible solution for this problem would be to allow a higher voltage output by replacing the zener diode by one with a higher zener voltage. However, this is not possible due to high voltage limitations in the current mirror and H-bridge. It was decided to change the maximum duty cycle to 80%. As a result, with a worst case load and a 9.6 V battery, a drive current of 8 mA cannot be achieved. This is acceptable since the entire general case drive current range can be achieved together with 1 mA - 7 mA drive current with the worst case load conditions. Furthermore, the FPGA has a safeguard against undercurrent and will shut off when undercurrent is detected during multiple consecutive pulses.

Furthermore, the voltage peaks and the average current peaks through the zener diode should be considered. As can be seen in B.17, the average current during the initial peak is currently 60 mA. This exceeds the power rating of the zener diode. A solution for this is a soft start sequence in which the duty cycle is slowly stepped up to prevent voltage overshoot and thus decrease the current peak through the zener diode. Such a Soft start sequence with a maximum duty cycle of 80% and an input voltage of 12.6 V can be found in the appendix in Figure B.2. The average peak current with this sequence is 12 mA which is within specifications of the selected zener diode.

To further decrease power consumption of the design, the maximum duty cycle at which the soft start sequence ends depends on the drive current. Using the worst case voltage output results of the boost converter, which can be found in Table B.10, to look up the minimum duty cycle required to achieved the worst case load voltages which were presented earlier in Table A.3, a table for D_{max} as a function of drive current has been constructed. This table can be found in the Appendix C.2.

The power consumption and efficiencies for the general case are evaluated as well. A summary of the calculated efficiencies for the general case boost converter output power can be found in Table B.9. The efficiency of the output power compared to the input power of the boost converter can be found in the fourth column, the efficiency of the load power compared to the input power can be found in the fifth column.

Lastly, the no load power consumption was measured. Current measurements were done in LTspice with several duty cycles and input voltages. The results can be found in Table B.21. It can be observed that for the absolute largest range of the duty cycle and input voltage, there is no load power dissipation. This is due to the fact that the voltage does not rise fast enough to exceed the 75 V zener voltage. Furthermore the power dissipation is within specs of the Zener diode dissipation of 1 W.

5.6 Power Down Circuit

The power down circuit is responsible for making sure that when there is no power needed for the stimulator, no unnecessary power will flow. The reason this component is put in there is because of the power efficiency. Disconnecting the power source from all the components in the circuit is a very safe method of making sure no static dissipation occurs. As can be seen in Figure 4.1, when the battery is disconnected from the circuit, none of the components will have any supply connected to them. This is shown in figure 5.11.

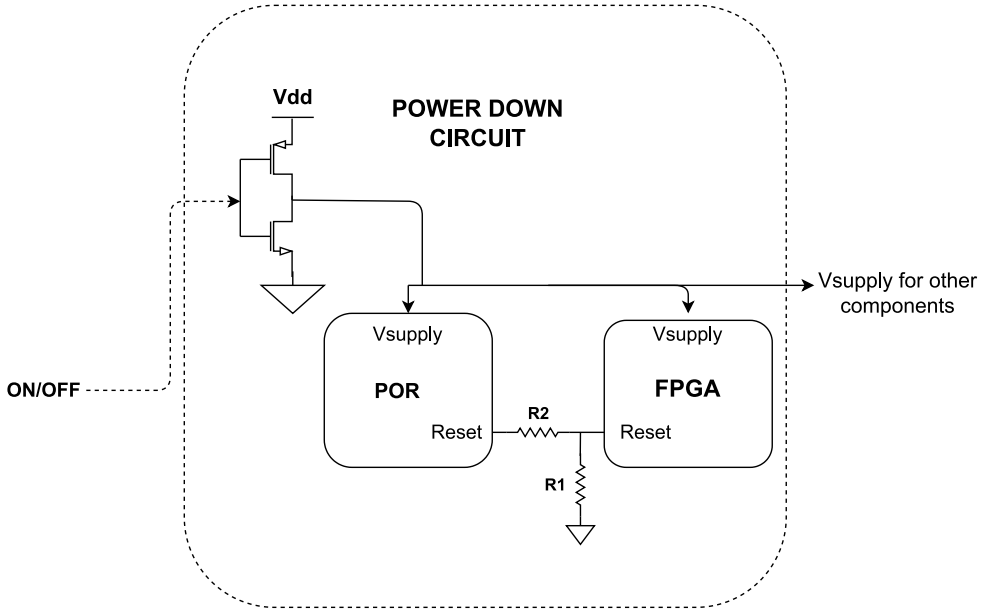

Figure 5.11: Diagram of the connection of the power down circuit

The most important factor that needs to be taken into account is the FPGA losing power. When the FPGA loses power, the states don't automatically return to the reset state. Turning on the power suddenly can cause the circuit to exhibit behaviour that is undesired. Therefore, a reset has to be implemented such that the circuit goes into a known state from which it can go to other states.

Although a reset circuit could be designed from scratch, it is more space and power efficient to use a power on reset timer that is readily available on a chip. The chip that is used for that purpose is the MAX810 by OnSemi [36]. The chip works by getting the supply voltage of the FPGA as an input which it compares to a given reference voltage (in this case 4.5V). When the supply voltage exceeds this voltage, a rail to rail input amplifier initiates a timeout counter. This counter makes sure that the reset is high on the FPGA for a given time, fulfilling the role of having a reset when the circuit is just powered on.

The amount of consumed power is difficult to estimate, since it would require knowledge about the exact static power dissipation of the other components in the circuit. The power down circuit draws power when there is the need for switching from the off to on state or vice versa. A CMOS is known for its high input impedance which results in practically zero gate current. Therefore, the power dissipation in the power down circuit only uses power for switching which would be a lot smaller than continuously connecting the battery to the components.

Chapter 6

Integrated Circuit

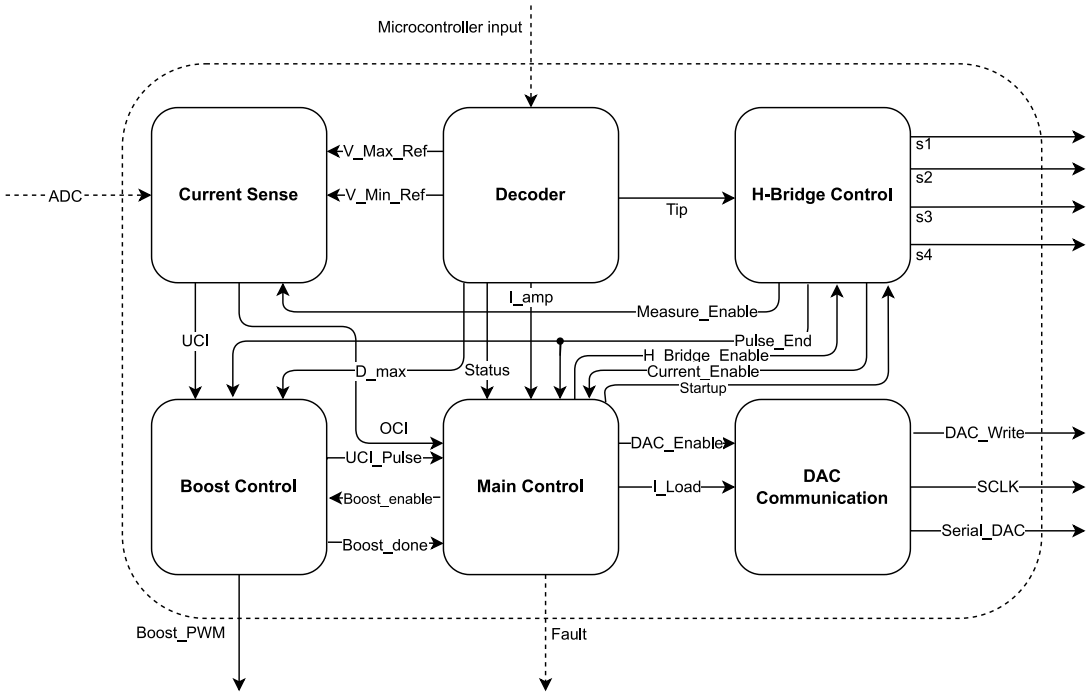

Figure 6.1: Submodule layout of the integrated circuit

In this chapter, the IC's functionality will be discussed. The entire overview of the to be designed integrated circuit can be found in Figure 6.1. This shows how the different sub-modules are interconnected with one another. The dotted lines are signals that are sent or received from outside components. Note that the microcontroller listed in this figure equals the signals received from the signal processing group as mentioned in section 1.3. The ADC is located on the FPGA and the microcontroller is a stand-alone circuit. The arrows going out of the box but solid are the lines that are sent to the actual stimulator circuit.

The IC has control over the amplitude of the stimulation current, all four branches of the H-bridge and the output voltage of the boost converter. In addition, it reads the current through the H-bridge and it is able to read commands from the microcontroller controlled by the signal processing group. It is also able to detect improper functionality by interpreting the measured current and it will send a fault signal to the microcontroller if this is the case. During the design, special attention was give to guarantee safety and power efficiency.

6.1 Safety

The microcontroller has no direct control over the control signals going to the circuit. Instead, they are decoded into safe parameters. Implementing this in hardware guarantees safe operation of the electronics in the stimulator and makes the design robust against potential hacks of the microcontroller.

Furthermore, the main control sub-module will disable stimulation automatically when the measured current deviates from the expected current range. This makes the system robust against circuit failure in the current source and boost converter. It also prevents unsafe operation when the device is misused by a patient or when the device operates in other load circumstances than those that were accounted for in the design. For example when the electrodes are connected to a load which is too large.

Lastly, During the inter-pulse interval, the H-bridge control will configure the H-bridge in such a way that the load is completely disconnected from the boost converter but stays connected with ground. This way, any charge left in the skin can safely discharge via ground.

6.2 Efficiency

As discussed in section 5.5, for higher efficiency the boost converters output voltage should be as close as possible to the voltage over the load. The control logic is implemented in the Boost control sub-module. The algorithm works as follows: Initially, the duty cycle is stepped up gradually until it reaches the maximum allowed duty cycle indicated by the decoder (which depends on the drive current). Then, the duty cycle is slowly stepped down after every stimulation pulse until undercurrent is detected. When undercurrent is detected, the duty cycle control sets its value to last duty cycle when no undercurrent was detected. The duty cycle optimization is done and the value for the duty cycle is maintained. Another undercurrent event will reset the algorithm. Furthermore, to save additional power, the current source will be disabled during the inter-pulse interval.

Chapter 7

Discussion of the Results

7.1 Simulated Results

Estimates of the total average power dissipation of the entire circuit have been given in previous chapters. It is important that the power consumption requirement as indicated in chapter 3 of 1 W is adhered. Therefore the different components maximum power dissipation will be checked. Table B.9. For the current of 8mA, the boost converter uses a power of 439.7 mW. In reality, however, if the loads draws 8 mA then the current drawn from the boost converter is roughly 9.6 mA since the reference current also needs to be generated. So using linear extrapolation on the 439.7 mW for 8 mA, the power for 9.6 mA is roughly 527.64 mW. This is the power supplied by the battery of the circuit during stimulation. The average power over the load during maximum current amplitude stimulation is according to Table B.1 around 212.83 mW. Also using the efficiency of 98.05% calculated in section 5.3, the total power amounts to 538.41 mW The requirement that the total power during active stimulation is under 1 W has been validated since the power used is around the 538.41 mW for maximum stimulation.

This does not account for static power dissipation in the components that are not included in this analysis. The power consumption of the current sense is minimal as indicated in section 5.2. The power the current sense uses is in the orders of 1.8 mW for maximum drive current. The power the buck converter consumes is highly dependent on how much the FPGA drains it but also the op amp that is used for the reference circuit. The op amp itself draws about 50 μA of quiescent current with a voltage of 5 V. This amounts to roughly 0.25 mW of turn on power for the op amp, which is negligible relative to the main circuit. This analysis so far only looks at the period when there is current flowing, not the entire stimulation period. When there is no active stimulation (meaning that the circuit is in the inter-pulse interval) the boost converter still supplies power to keep the voltage high. This can be found in Table B.12. The worst case average power dissipation is roughly 811 mW during the inter-pulse time . Sine the inter-pulse time is longer than the pulse times, this is also the average power during stimulation for the worst case. This is significantly higher than required for the future purposes but still remains under the 1 W requirement that was given before. For a general case, the no load average power dissipation is around the 160 mW for 9.6V with 75% duty cycle.

Unfortunately, due to issues with the simulating software there is no simulation of the entire circuit. When analyzing the behaviour of the simulations of the total circuit, the op-amp of the reference current source stopped functioning and started clipping. Also connecting a large current mirror to the H-bridge caused current spikes and drops that were not in line with the expectations. It was seemingly like the H-bridge was acting like a load seen from the current mirror which is not how an H-bridge should act.

7.2 Prototype Results

The results of the prototype were not according to the expectations. Mostly due to the short span of time to test and implement the prototype there was no option to go in-depth into each separate component to

debug it.

The most thoroughly tested component was the H-bridge which had the most unexpected results arise. The setup was as follows:

- 5 V supply for the bootstrap network
- 20 V supply for the load
- 124 Hz signal for the H-bridge gates
- 18 kΩ functioning as the load

On power up, the system did not behave as expected. The circuit consumed more current from the 5 V rail than previously expected. Performing several measurements confirmed that there was a short circuit caused by a PCB fabrication error at a MOSFET from the power down circuit. This component was desoldered which solved the short circuit.

However, after fixing this problem, there was current flowing through the H-bridge that was not going through the load which should not be possible in the test setup that was used. Testing indicated that when all transistors were open circuited, there was no current flow. However, when the high-side transistors were closed, there was current flow which in theory should not happen. Therefore, the lower side of the H-bridge was identified to be the issue. The bottom-left part of the H-bridge always gave 0 V meaning that this was the side that was connected to ground and caused the short circuit. So it was either the transistor or the diode. Having both diodes from the H-bridge removed did not fix the problem. A possible cause is a nonfunctional MOSFET on the left side of the H-bridge. Unfortunately, this theory could not be confirmed due to time constraints.

VHDL was written for the FPGA to implement the integrated circuit as indicated in chapter 6. Although the VHDL worked correctly in simulations, the synthesis of the VHDL on the FPGA was not as successful. First issue was that the ADC was not easily connected and mapped to the VHDL which gave as a result that the entire circuit could not be tested since so many components depend on the current sense, directly or indirectly. A separate testbench for the boost converter was written to test the soft start functionality. However, the FPGA did not generate the expected PWM frequency for the boost converter that was confirmed by simulations. The frequency was around 4 MHz instead of 600 kHz. This caused the inductor to heat up and break. Also what did not help is that when the bitstream was written to the FPGA through JTAG, it did not flash it properly and the programming was gone.

The current mirror was also tested without the use of the DAC (due to the FPGA not working as expected). A voltage reference was manually generated by adding a voltage source. Results indicated that the op amp did get power, however, it did not supply any voltage to the BJT, causing no reference current to be generated. Since the reference current is the main factor for the functioning of the current mirror, there was no indication whether the mirror actually functioned. The expected culprit is the op amp due to perhaps poor connection or overheating during fabrication, since an identical op amp was used to the ones in simulations.

Chapter 8

Prototype implementation

The discussed design of which its functionality is proven by simulation will be implemented on a PCB. To make the design functional and power efficient, all available time until the thesis deadline for the project was used for design and simulation. According to the planning, the time between the thesis deadline (June 13th 2022) and the defense (June 20th 2022) will be used to construct the prototype PCB, write VHDL and perform tests so that results can be presented during the thesis defense (June 20th 2022). In this chapter, the PCB design will be briefly discussed.

8.1 PCB Design

Due to the complex design, it was chosen to design a 4 layer PCB. The top and bottom layers will be used for traces between the components, while the middle two layers will be used as a ground plane and a 5 V plane to power all 5 V components. In addition, all free space left in the top and bottom layers of the PCB will be filled with ground planes to ensure minimal impedance from components to ground.

The circuits with their corresponding components can be subdivided in three categories: digital (FPGA and DAC), stimulator (Current source, H-bridge Current sense) and power (Power down, Boost converter and Buck converter) To avoid interference between different components, special care is taken to separate high current and EMF producing components from low voltage and digital signals. This can be seen in the separation of ground planes. The three categorized circuits are all connected to a different part of the ground plane and only connect to each other close to the ground of the supply voltage (battery) connection. Furthermore, the inductors from the boost and buck converter have been placed on the backside of the PCB to separate them from the digital and low voltage components to avoid interference from EMF waves.

The PCB has been designed in such a way that all different sub-circuits can be disconnected and tested separately through pin headers. In addition, the MOSFETs controlled by the integrated circuit can be disconnected from the FPGA and connected to a micro controller in case the integrated circuit fails. Furthermore, test pads were added at all relevant nodes for testing purposes. As a result, the PCB is much larger than in a design where no testing capabilities are required. In practice the FPGA would be replaced by a much smaller integrated circuit as well. Furthermore, due to the chip shortage, multiple IC's were used with P-channel and N-channel MOSFETs combined. In multiple cases only one of the two was used. In a later final design this could be prevented, or multiple used P-channel and N-channel MOSFETs could be combined on one integrated circuit to save space.

Chapter 9

Conclusion

For this TU Delft bachelor graduation project an electrical circuit for t-VNS has been designed and implemented on a PCB. Test results of the PCB were not included since testing was scheduled in the period between the bachelor thesis deadline and the thesis defence. The electrical stimulation circuit was designed around an impedance model of the skin. A large variety of research has proposed different impedance models. However, the stimulator circuit was designed around the Montague impedance model taking the worst case impedance values into account. Simulations showed that the stimulator is able to approximately generate a current-mode biphasic square wave through the load. However, since passive charge balancing has been applied the generated square wave was not perfect due to capacitive behaviour of the load.

The stimulator is able to accurately stimulate with currents until 8 mA when taking worst case values for the impedance of human skin and general case values for the battery. However, Due to the limitation in duty cycle of 80% of the boost converter, a drive current of 8 mA could not be achieved with a worst case load and a 9.6 V battery. However, this is acceptable since the requirement of 8 mA can be achieved in the most cases and safety measures are in place to guarantee safe stimulation. However, all other requirements regarding the wave parameters such as the pulse width, stimulation frequency and thus stimulation current in general case have been met.

Overall, the individual components are performing as intended. The current mirror is correctly multiplying the reference current and giving the desired magnitude for the current. Improvements can be made in terms of the pace at which it goes to the correct current. The reference current source is very stable and behaves according to expectations as shown in Figure 5.4. The H-bridge is successful in alternating the current as shown in Figure B.1. The power down circuit unfortunately did not have a spice model to simulate with and was therefore not able to be fully verified. However, taken the assumption that it is from a verified company, this should work as intended.

Furthermore, an integrated circuit has been designed for controlling the stimulating circuit based on required input parameters. The integrated circuit has not yet been implemented. However, this will be implemented on an FPGA for the thesis defence. The integrated circuit has, among other things, built in safety features such as over-current protection due to closed loop feedback in current sense.

Together, these functioning submodules make for a portable, power efficient and very safe transcutaneous vagus nerve stimulation device. This device is suitable to lay the basis for future development in the field of portable and wearable stimulators inside the ear.

Chapter 10

Recommendations & Future Work

The designed stimulator circuit is very much designed around the impedance of the skin. The research done for this device with regards to the impedance was numerous but detailed information was not found. Assumptions were made with regards to the impedance. Aspects such as different thicknesses of different layers in various parts of the body were not taken into account. In the future this model has to be made more accurate and has to be made to resemble the skin in the ear. When this model is clearer and the values are more accurate, a better estimation can be made on the requirements of the skin. The electrodes that are used are also made with the assumption that their resistance can be dismissed. In reality, this can be a safe assumption since the impedance of the skin is significantly higher. Well suited electrodes for t-VNS have to be designed to both minimize the voltage requirement of the circuit but also make it suitable for wearing for longer periods of time. Most of the choices in the design process took this impedance model into account.

Although several studies have illustrated that t-VNS is an effective method for epileptic treatment with certain stimulation parameters, the optimal stimulation parameters are still unknown. More research needs to be done regarding the optimal stimulation current, frequency and pulse width. However, the designed circuit has the capability to stimulate with different stimulation parameters for future testing purposes.

For the designed circuit, size is an issue due to all testing capabilities. The size of the stimulator can be decreased in later versions by removing all testing capabilities going in the direction of a final product. Size can be reduced further by fabricating the designed integrated circuit and integrating it with the electrical circuit or by combining multiple MOSFETs into one integrated circuit.

Furthermore, power consumption can be reduced by replacing the diode of the boost converter with a MOSFET to bypass the voltage drop of 0.7 V over the diode. To improve the efficiency of the circuit even further, the option to disable the PWM signal to the boost converter can be explored. It is known by the FPGA when a no load situation occurs. The capacitor will stay charged when the switch stays open. This way, no load power dissipation can be avoided. It was also observed that for higher duty cycles, the zener diode started to dissipate energy because of the high output voltage of the boost converter. These costs can be avoided by selecting components in the H-bridge and current mirror that are rated for higher voltages than 80 V. Then, the zener voltage of the zener diode can be further increased which increases the conduction threshold. This makes the design more efficient and could be the solution for the specific case of the 8 mA drive current and 9.6 V input at maximum load that could not be achieved with the current design.

In the stimulator, passive charge balancing has been applied meaning that the load will be shorted to GND to prevent charge buildup resulting in an imperfect biphasic square wave. Instead, active charge balancing could be applied to improve the stimulation wave form. When applying active charge balancing, the stimulation current is regulated in a way that expected deviations are compensated for resulting in a more perfect biphasic square wave.

Appendix A

Background

A.1 Project Overview

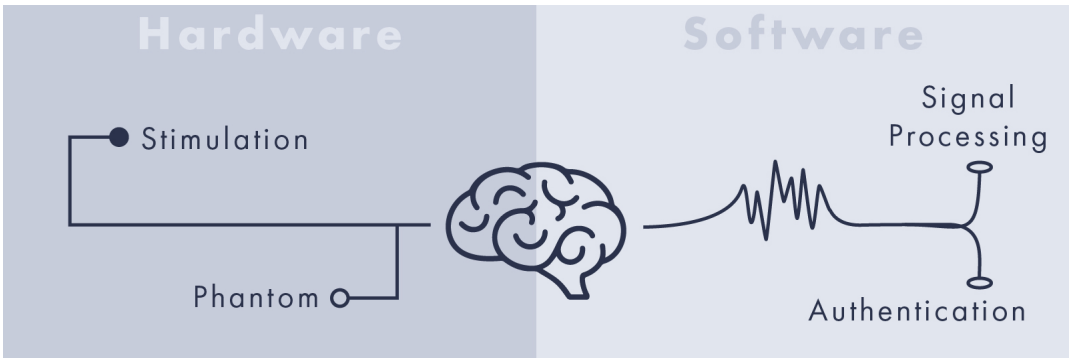

Figure A.1: Project groups overview

A.2 Impedance Model & Electrodes

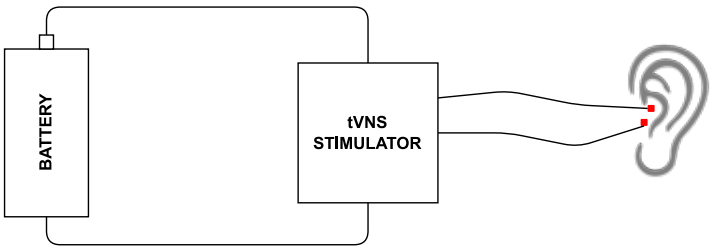

Figure A.2: Connection of the system

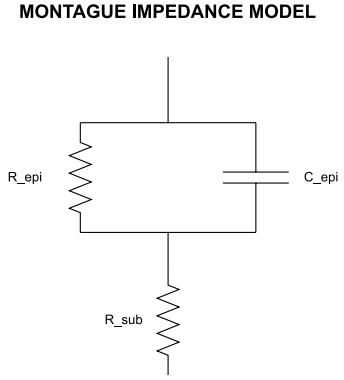

Figure A.3: Montague Impedance Model

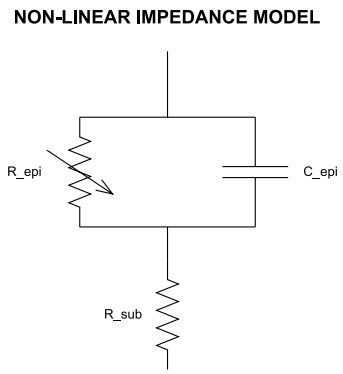

Figure A.4: Non-linear Impedance Model

Table A.1: Table with values for Figure A.7 and Figure 2.1

	Low	Average	High
R_{elec} [$k\Omega$]	10	10	10
C_{elec} [uF]	4.6	4.6	4.6
R_{epi} [$k\Omega$]	0.88	2.27	3.66
C_{epi} [nF]	48.8	28.28	7.63
R_{tissue} [$k\Omega$]	0.4	0.67	0.89

Equation for calculating the resistance (R) in Ω where ρ is the resistivity in $\Omega \cdot m$, l is the length in m and A is the cross section area in m^2:

$$R = \rho \frac{l}{A} \tag{A.1}$$

Equation for calculating the capacitance (C) in F where ϵ is the permittivity in F/m, l is the distance of separation between the plates in m and A is the area of the plates in m^2:

$$C = \epsilon \frac{A}{l} \tag{A.2}$$

Table A.2: Values used for calculating R_{elec} and C_{elec} with Equation A.2 and Equation A.1

Variable	Value used
ϵ	44 nF/mm
ρ	1kΩ/mm
A	1 cm^2
l	0.1 cm [37]

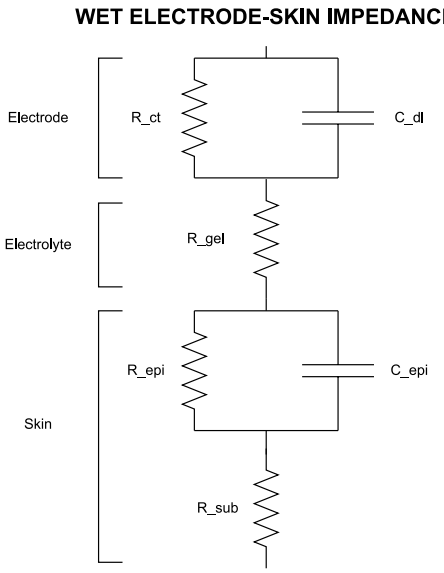

Figure A.5: Electrode-skin impedance model for wet electrode

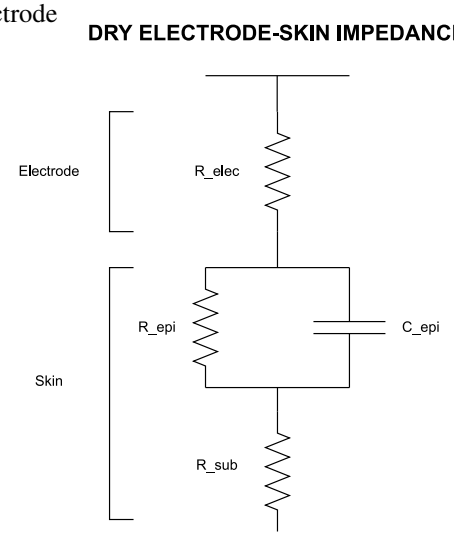

Figure A.6: Electrode-skin impedance model for dry electrode

Table A.3: Corresponding voltage over the load to drive current

I_{load} [mA]	V_{load} [V] best case	V_{load} [V] general case	V_{load} [V] worst case
1	2.2	5.0	8.2
2	4.3	10.0	16.4
3	6.5	15.1	24.7
4	8.6	20.1	32.9
5	10.8	25.1	41.1
6	13.0	30.1	49.3
7	15.1	35.2	57.5
8	17.3	40.2	65.8

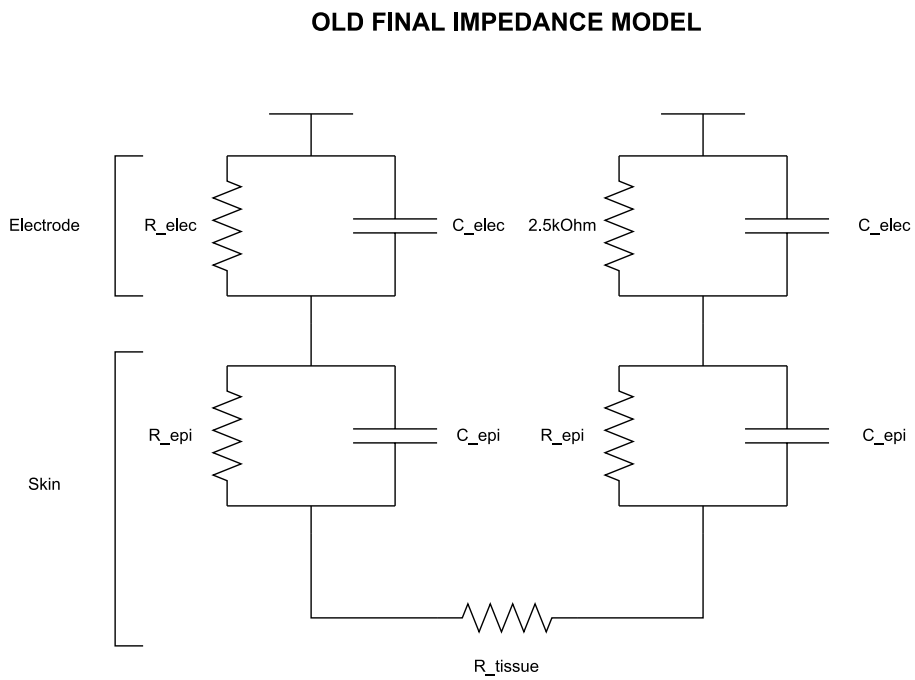

Figure A.7: Old model on which values were based

Appendix B

Circuit Design

B.1 Stimulation Source

Current Amplitude [mA]	Power to load [mW]	Power supplied [mW]	Efficiency [%]
1	2.76	34.38	8.0
2	12.43	74.70	16.64
3	29.01	115.04	25.22
4	52.12	154.83	33.66
5	82.12	194.86	42.14
6	120.00	236.00	50.85
7	163.18	275.60	59.21
8	212.83	315.12	67.54
8.8 (MAX)	261.89	351.73	74.46

Table B.1: Average power of the current source during 1 stimulation cycle

Table B.2: Table of measured currents with respect to desired current

Desired I [mA]	Measured I [mA]	Error [%]
1	1.003	0.3
2	2.004	0.2
3	3.004	0.13
4	4.001	0.025
5	4.996	-0.08
6	5.989	-0.18
7	6.98	-0.29
8	7.965	-0.4375

Table B.3: Components for the current source

Component	Value/name
NPN	2N222AUB
OP AMP	LT1490ACD
Reference resistor	681 Ω
PMOS for Mirror	SH8M41TB1

B.2 H-Bridge

Table B.4: Components for h-bridge

Component	Value/name
BJT	2SCR514RTL
NMOS	BST82,215
Diode	STPS2H100AFY
R1,R2,R3,R4	10 kΩ
R5,R6,R7,R8	500 kΩ
R9,R10	68 Ω
C1,C2	100 nF

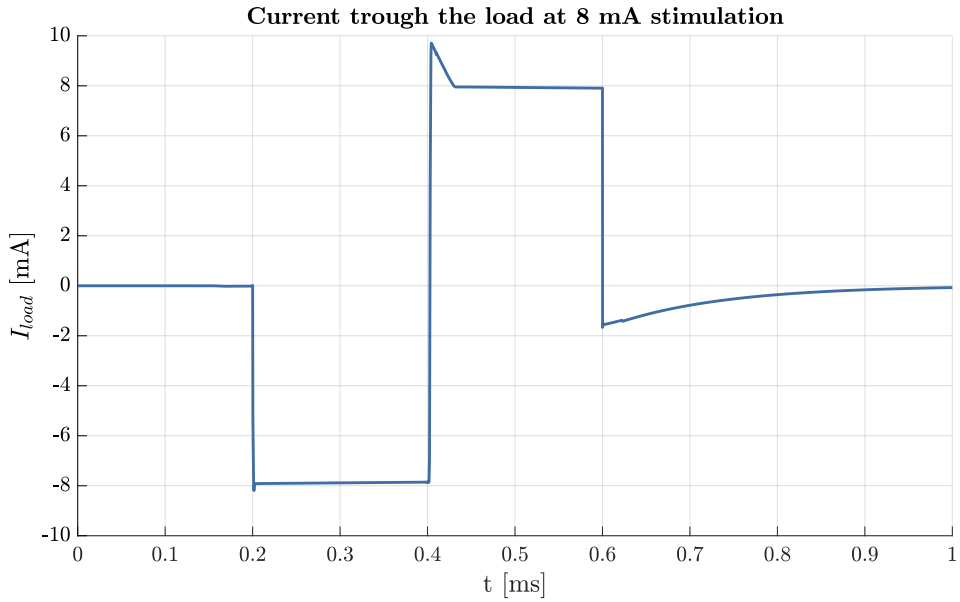

Figure B.1: Current through the load at 8 mA stimulation

B.3 Current Sense

Table B.5: Component values for the current sensor

Component	Value
Op-amp	MCP601
Rs	10 Ω
R1	90.9k Ω
R2	10.1k Ω

Table B.6: Simulation results of Current Sense

Drive current [mA]	Output voltage [mV]	amplifier source current [uA]	V_{Rs} [mV]	Power dissipation [mW]
10	998.0	227	100	2.1
9	898.0	226	90	1.9
8	798.0	225	80	1.8
7	698.0	224	70	1.6
6	598.0	223	60	1.5
5	498.0	222	50	1.4
4	398.0	221	40	1.3
3	298.0	220	30	1.2
2	198.1	219	20	1.1
1	98.1	218	10	1.1

B.4 Buck Converter

Table B.7: LM2576 5V regulator componen values

Component	Value
C_in	100uF
C_out	1000uF
L	100uH
D	SD2010S040S3R0

B.5 Boost Converter

B.5.1 Component Values Calculation

According to [38], the output voltage, the critical inductance and the critical capacitance are given by formulas B.1, B.4 and B.5. The output voltage can be rewritten as equation B.3 to calculate the required duty cycle for the desired voltage output. Assuming a diode voltage of 0.6 V, a duty cycle of 0.864 is needed to step the minimum battery voltage up to 70 V and 0.822 to step the maximum battery voltage up to 70 V.

$$V_o = \frac{V_{in}}{1-D} - V_{diode} \tag{B.1}$$

For the design it is important to determine the switching frequency. Boost converters with higher frequencies have less switching losses and can hold smaller components. However, in this application, high switching frequencies come at the cost of a lower duty cycle control resolution. The FPGA which is used to generate the PWM signal has an internal clock of 12 MHz. The resolution of the duty cycle is given by equation B.2. A switching frequency of 600 kHz brings a good balance between the size of the components and the duty cycle resolution of 5%.

$$Resolution_D = \frac{f_{switch}}{f_{clock}} * 100\% \tag{B.2}$$

$$D = 1 - \frac{V_{in}}{V_o + V_{diode}} \tag{B.3}$$

To calculate the minimum inductance needed, the largest critical inductance within the specification range should be derived. According to equation B.4 this value can be found by optimizing $D(1-D)^2$ and filling in the largest possible load value. Optimizing the value of $D(1-D)^2$ yields a value of $\frac{1}{3}$ for the duty cycle. The maximum load occurs at 70 V and 8mA and is equal to 8750 Ω. Plugging in these values yields a minimum inductance of 1.1 mH.

$$L_C = \frac{RD(1-D)^2}{2Fs} \tag{B.4}$$

The minimum value for the capacitance can be derived by using equation B.5. This value can be found by optimizing $\frac{V_o}{R}$ which occurs at the largest possible output current which is 8 mA in this application. V_o is at most 70 V and the allowed ripple voltage is chosen to be at most 100 mV since there is no hard requirement but does keep the voltage steady. Plugging in these values together with the switching frequency of 600 kHz and the maximum duty cycle of 0.864 yields a minimum value of 112 nF for the capacitor

$$C_B = \frac{V_o D}{Fs \Delta V_o R} \tag{B.5}$$

The diode that is selected for the design is a Schottky diode because of its low forward voltage drop. The diode should be able to handle current peaks of 490 mA. The electrical switch that is selected for the design is an N-Channel MOSFET with a very low gate charge for fast switching. The MOSFET can be directly controlled from the FPGA at 600 kHz frequency. Lastly, a zener diode is needed to fulfill the requirement regarding 0 mA output current. Actively switching boost converters require a load for proper functionality. If no load is connected, the capacitor will rise until the circuit breaks. A zener diode functions as a load above a certain specified voltage(zener voltage) to prevent overvoltage by only dissipating power when needed. Due to the maximum drain to source voltage specifications of 80 V in the current mirror, a 75 V zener diode is chosen.

Table B.8: Boost converter component list

Component	Value
L	2.1mH
C	180nF
Q	IRLML0100TRPBF
D	STPS2H100AFY

B.5.2 Simulation results

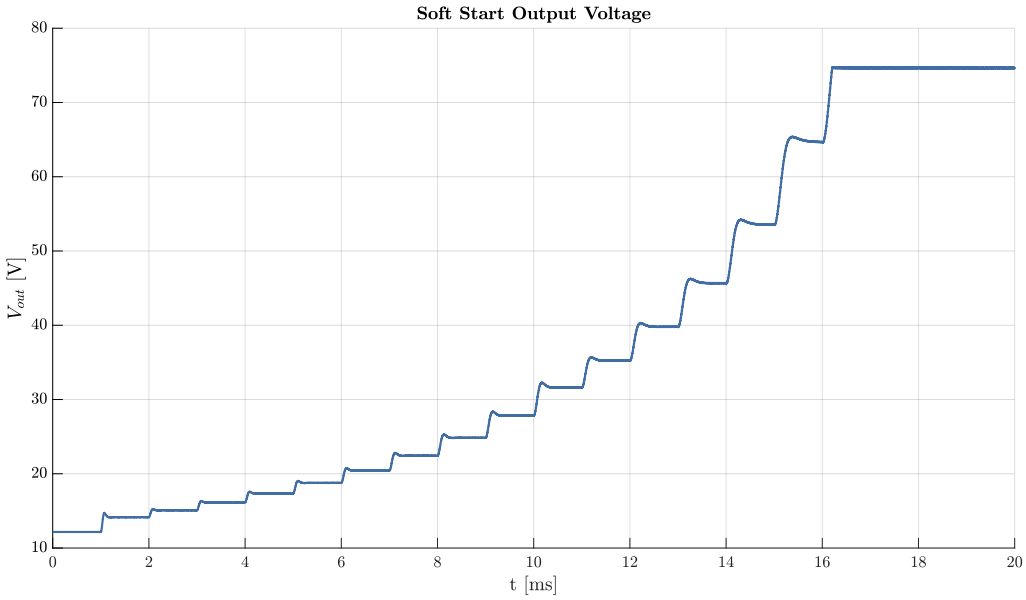

Figure B.2: Example output voltage of a soft start sequence

Table B.9: Simulated efficiencies [%] as a function of drive current [mA] for a general case load and a 9.6V battery

Current [mA]	Duty cycle [%]	Input Power [mW]	Output efficiency [%]	Load efficiency [%]
1	0	9.6	96.9	52.1
2	5	38.4	66.7	52.1
3	40	69.1	77.9	65.5
4	50	104.6	78.3	76.8
5	60	158.4	79.1	79.2
6	65	241.9	80.9	74.7
7	70	325.4	80.7	75.7
8	75	439.7	81.0	73.1

Table B.10: Simulated output voltage [V] as a function of drive current [mA] an duty cycle [%] for a 9.6V input voltage

Current [mA] / D	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	85%	off
1	14.6	15.3	16.1	17	18.2	19.6	21.2	23.3	25.7	29	32.8	37.5	42.9	50.9	62	78.4	74.6	12.3
2	12.8	13.4	14.3	15.2	16.3	17.6	19.1	21	23.2	26	29.2	33.3	38.5	45.6	55.8	71.3	74.6	12.2
3	11.9	12.6	13.4	14.3	15.3	16.5	18	19.7	21.9	24.5	27.4	31.2	36	42.6	51.9	66.2	74.6	12.2
4	11.4	12.1	12.9	13.7	14.8	15.9	17.3	19	21	23.5	26.3	29.9	34.5	40.6	49.3	62.7	74.6	12.2
5	11.1	11.8	12.5	13.4	14.4	15.5	16.9	18.5	20.5	22.9	25.6	29	33.4	39.3	47.6	60.2	74.6	12.2
6	10.9	11.5	12.3	13.1	14.1	15.2	16.6	18.1	20	22.4	25	28.3	32.6	38.3	46.3	58.5	74.6	12.2
7	10.7	11.4	12.1	12.9	13.9	15	16.3	17.9	19.7	22	24.6	27.8	31.9	37.5	45.3	57.1	74.4	12.2
8	11.2	11.2	11.9	12.8	13.7	14.8	16.1	17.6	19.5	21.7	24.3	27.4	31.5	36.9	44.5	55.9	74.3	12.2

Table B.11: Simulated output zener diode current (peak [mA], average peak [mA], average steady state [mA]) as a function of drive current [mA] an duty cycle [%] for a 9.6V input voltage

Current [mA] / D	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	85%	off
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	47 15 0.5	320 40 10	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	45 15 0	320 40 8	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	45 15 0	320 40 6	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	39 15 0	320 40 4	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	35 14 0	320 40 4	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32 13 0	320 40 0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	27 12 0	320 40 0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	23 10 0	320 40 0	0

Table B.12: Simulated Boost converter power consumption [mW] as a function of duty cycle and input voltage [V] for a no load case

Input [V] / D	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	off
9.6	38.4	39.36	35.52	36.48	38.4	38.4	42.24	44.16	49.92	55.68	66.24	77.76	95.04	121.92	163.2	259.2	0
11.1	48.84	45.51	46.62	45.51	45.51	49.95	52.17	54.39	58.83	68.82	77.7	93.24	117.66	150.96	202.02	428.46	0
12.6	59.22	57.96	55.44	55.44	57.96	59.22	60.48	64.26	69.3	81.9	91.98	114.66	139.86	181.44	294.84	811.44	0

Table B.13: Simulated peak output voltage [V] as a function of drive current [mA] an duty cycle [%] for a 9.6V input voltage

Current [mA] / D	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	85%	off
1	x	x	x	x	x	x	x	x	x	x	x	38	44.1	52	62.6	x	74.7	x
2	x	x	x	x	x	18	20.1	22.5	25.4	29	32.9	37.7	43.7	51.6	62.2	77	74.7	x
3	x	x	13.6	14.7	16.1	17.8	19.9	22.3	25.2	28.7	32.6	37.4	43.4	51.3	61.8	76.6	74.7	x
4	11.5	12.40	13.4	14.6	16	17.7	19.7	22.1	25	28.5	32.4	37.2	43.2	50.9	61.4	76	74.7	x
5	11.4	12.3	13.2	14.4	15.9	17.5	19.6	22	24.9	28.3	32.2	36.9	42.7	50.5	60.9	75.5	74.8	x
6	11.3	12.2	13.2	14.3	15.8	17.4	19.5	21.8	24.6	28.1	31.9	36.6	42.5	50.3	60.5	75	74.7	x
7	11.2	12.1	13	14.2	15.6	17.3	19.3	21.6	24.5	27.9	31.7	36.4	42.2	49.7	60.2	74.6	74.7	x
8	12.1	12	12.9	14.2	15.6	17.2	19.2	21.5	24.3	27.7	31.5	36.1	37.8	49.6	59.7	74.1	74.7	x

Table B.14: Simulated input current [mA] as a function of drive current [mA] an duty cycle [%] for a 9.6V input voltage

Current [mA] / D	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	85%	off
1	2.4	2.5	2.6	2.9	3.4	3.5	4	4.5	5.2	6	6.9	8.3	10.3	13.1	17.8	25.5	84.1	1
2	4	4.3	4	4.2	4.5	5	5.5	6.1	7	8.1	9.4	10.8	13.3	16.4	20.8	28.8	84.1	2
3	4.6	4.8	5	5.5	5.9	6.5	7.2	7.9	8.9	10.1	11.7	13.4	16.4	19.6	24.9	33.1	84.3	3
4	5.6	6	6.3	6.7	7.4	8	8.8	9.7	10.9	12.5	14.1	16.3	19.2	23.5	29.3	38.2	84.5	4
5	6.8	7.1	7.5	8.1	8.5	9.4	10.5	11.6	12.7	14.5	16.5	19.1	22.3	26.6	33.3	44	85.7	5
6	7.8	8.2	8.8	9.4	10.1	10.9	12	13.2	14.8	16.9	18.7	21.7	25.2	30.1	37.7	48.9	86.7	6
7	9.1	9.3	9.9	10.7	11.5	12.4	13.5	15	16.8	19	21.4	24.4	28.3	33.9	41.6	54.4	84.9	7
8	10.5	10.5	11.1	11.9	13	13.9	15.1	16.7	18.7	21.1	23.6	26.9	31.4	37.3	45.8	59.4	86	8

Table B.15: Simulated efficiency [%] as a function of drive current [mA] an duty cycle [%] for a 9.6V input voltage

Current [mA] / D	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	85%	off
1	63.4	63.8	64.5	61.1	55.8	58.3	55.2	53.9	51.5	50.3	49.5	47.1	43.4	40.5	36.3	32.0	9.2	97.6
2	66.7	64.9	74.5	75.4	75.5	73.3	72.3	71.7	69.0	66.9	64.7	64.2	60.3	57.9	55.9	51.6	18.5	96.8
3	80.8	82.0	83.8	81.3	81.0	79.3	78.1	77.9	76.9	75.8	73.2	72.8	68.6	67.9	65.1	62.5	27.7	96.8
4	84.8	84.0	85.3	85.2	83.3	82.8	81.9	81.6	80.3	78.3	77.7	76.4	74.9	72.0	70.1	68.4	36.8	96.8
5	85.0	86.6	86.8	86.2	88.2	85.9	83.8	83.1	84.1	82.3	80.8	79.1	78.0	77.0	74.4	71.3	45.3	96.8
6	87.3	87.7	87.4	87.1	87.3	87.2	86.5	85.7	84.5	82.8	83.6	81.5	80.9	79.5	76.8	74.8	53.8	96.8
7	85.7	89.4	89.1	87.9	88.1	88.2	88.0	87.0	85.5	84.4	83.8	83.1	82.2	80.7	79.4	76.5	63.9	96.8
8	88.9	88.9	89.3	89.6	87.8	88.7	88.9	87.8	86.9	85.7	85.8	84.9	83.6	82.4	81.0	78.4	72.0	96.8

Table B.16: Simulated output voltage [V] as a function of drive current [mA] an duty cycle [%] for a 12.6V input voltage

Current [mA] / Duty cycle	80%	85%
1	74.7	74.7
2	74.7	74.8
3	74.6	74.8
4	74.6	74.7
5	74.6	74.8
6	74.6	74.7
7	74.6	74.8
8	74.5	74.8

Table B.17: Simulated output zener diode current (peak [mA], average peak [mA], average steady state [mA]) as a function of drive current [mA] an duty cycle [%] for a 12.6V input voltage

Current [mA] / Duty cycle	80%	85%
1	360 60 9	550 x 70
2	360 60 7	550 x 70
3	360 60 6	550 x 55
4	360 60 5	550 x 73
5	360 60 4	550 x 60
6	360 60 3	550 x 57
7	360 60 2	550 x 55
8	360 60 1	550 x 58

Table B.18: Simulated peak output voltage [V] as a function of drive current [mA] an duty cycle [%] for a 12.6V input voltage

Current [mA] / Duty cycle	80%	85%
1	74.8	74.8
2	74.8	74.8
3	74.8	74.8
4	74.8	74.8
5	74.7	74.8
6	74.7	74.9
7	74.9	74.8
8	74.7	74.9

Table B.19: Simulated input current [mA] as a function of drive current [mA] an duty cycle [%] for a 12.6V input voltage

Current [mA] / Duty cycle	80%	85%
1	64.2	394
2	64.3	417
3	64.2	417
4	64.4	404
5	64.6	400
6	64.7	396
7	64.9	394
8	65.2	400

Table B.20: Simulated efficiency [%] as a function of drive current [mA] an duty cycle [%] for a 12.6V input voltage

Current [mA] / Duty cycle	80%	85%
1	12.1	2.0
2	24.2	3.7
3	36.3	5.6
4	48.3	7.7
5	60.1	9.7
6	72.1	11.8
7	83.8	13.8
8	95.2	15.6

Table B.21: Simulated Zener current [mA] and power [mW] as a function of duty cycle and input voltage [V] for a no load case

Input [V]	Current [mA] (80% Duty cycle)	Current [mA] (75% Duty cycle)	Current [mA] (<75% Duty cycle)
9.6	1.5	0	0
11.1	3.6	0.8	0
12.6	8.3	1.9	0
Input [V]	Power [mW] (80% Duty cycle)	Power [mW] (75% Duty cycle)	Power [mW] (<75% Duty cycle)
9.6	112.5	0	0
11.1	270	60	0
12.6	622.5	142.5	0

Appendix C

Integrated Circuit

The sub-modules of the integrated circuit will be explained in more detail in the following sections. More information about the signals displayed in the figures can be found in section C.7.

C.1 Decoder

The decoder is responsible for translating the messages from the microcontroller to appropriate signals. The messages contain the stimulation parameters that are forwarded to their respective components after their decoding. The decoder receives the following signals from the microcontroller:

- Stimulation intensity ranging from 0 to 8 mA. For this, 3 bits are enough to read the signal.
- Stimulation frequency ranging from 10 Hz to 40 Hz in steps of 5 Hz. This will again require 3 bits to be send to determine the correct frequency.

The frequency needs to be converted to a time value since it will be directly passed through a timer. The formula for converting a frequency is: $T = \frac{1}{f}$.

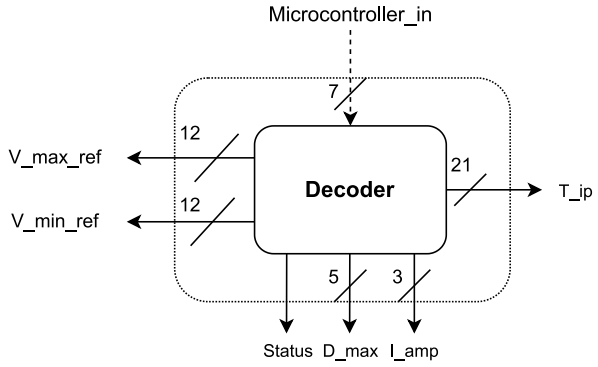

Figure C.1: Decoder diagram

The look-up tables are made to decode the signals accordingly and they can be found in Table C.3. The bit column indicates what options there are with 3 bits, the I_{amp} column indicates what those values would mean for the current and the T_{ip} column indicates the pulse times that are required. T_{ip} is the time between the biphasic stimulation pulse and the next start of the following pulse.

The T_{ip} needs a subtraction of two times the pulse time for each one. This is because as indicated in the figure in Figure 2.2, first two pulses have passed of each 200μs. Therefore this still has to be taken into

Table C.1: Decoding of the corresponding bits for each important signal

Bits	I_{amp} [mA]	Tip [ms]
000	1	100
001	2	67
010	3	50
011	4	40
100	5	33
101	6	29
110	7	25
111	8	No Stimulation

account in the form of removing the time that has already elapsed from the time in Table C.1.

The D_{max} is a value that is required for the boost converter to have optimal power consumption. More info can be found in the section that covers boost control in section C.5. The decoding table can be found in Table C.2.

Table C.2: Decoding of the reference current to the minimum reference and maximum reference voltage

I_{amp} [mA]	D_{max} [clock cyles]	D_{max} [%]
1	0	0
2	6	30
3	11	55
4	13	65
5	15	75
6	16	80
7	16	80
8	16	80

The other use case that is specified is a simple turn off the circuit signal. When this signal is received from the microcontroller it will be considered as a faulty signal and then the circuit will power down. V_{max} and V_{min} reference signals are the signals from which undercurrent and overcurrent are determined. The decoding table for this can be found in Table C.3

Table C.3: Decoding of the reference current to the minimum reference and maximum reference voltage

I_{amp} [mA]	V_{max} [V]	V_{min} [V]
1	0.12	0.08
2	0.22	0.18
3	0.32	0.28
4	0.42	0.38
5	0.52	0.48
6	0.62	0.58
7	0.72	0.68
8	0.82	0.78

C.2 H-bridge Control

The H-bridge control sub-module with its corresponding in- and outputs is shown in Figure C.2.

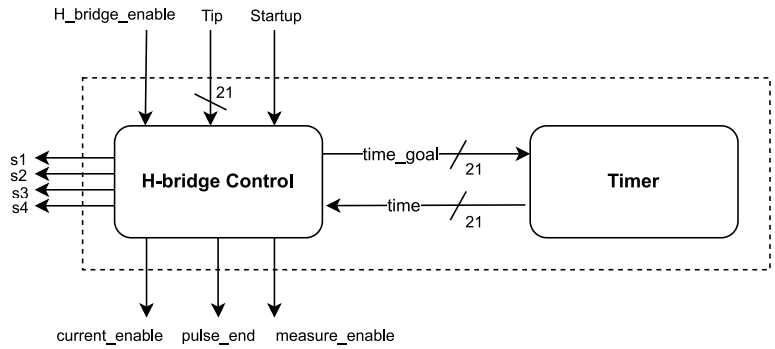

Figure C.2: H-bridge Diagram

It has predetermined times (the pulse width) and times provided from the outside (inter-pulse time). The reason that the H-bridge control has its own timer is because it has many states that it has to keep track of. These all progress automatically based on if a pre-indicated time has passed. This is the time_goal that is passed from the H-bridge control into the timer.

The reason that the control has so many states is because of the relation it has with the current source. The first reason is that the current source should start up. This is done by shorting the gates of the H-bridge but leaving one gate open. As a result, only one other gate has to be opened to let the current. When the current is flowing and the corresponding lower gate is opened, it can start pushing current through the load. When the time has passed of the first pulse, again a short circuit is done for a brief period of time. This is implemented because otherwise high voltage spikes would occur which is very undesired given the load that is being used. Then the other pulse is send for the time of 1 pulse width and after that another pause to make sure that no more current flows through the load. Then the current source is turned off and the H-bridge is placed in the inter-pulse time in which the load is discharged. When this time has passed, the cycle starts over again. This process can be seen in Figure C.5.

During some of these periods, the current through the sensing resistor becomes quite large due to the short circuits that occur. These are important moments because that is when the measure_enable signal is turned off. The reason for this is because the current that is being measured is simply not going through the load. Therefore, this signal is important to turn off when the short circuit occurs.

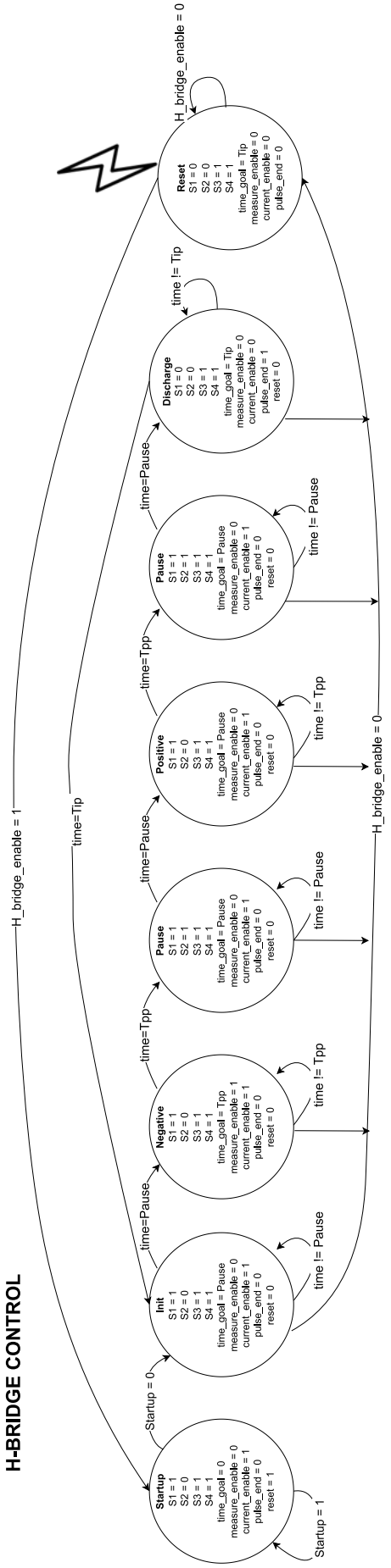

Figure C.3: H-bridge FSM

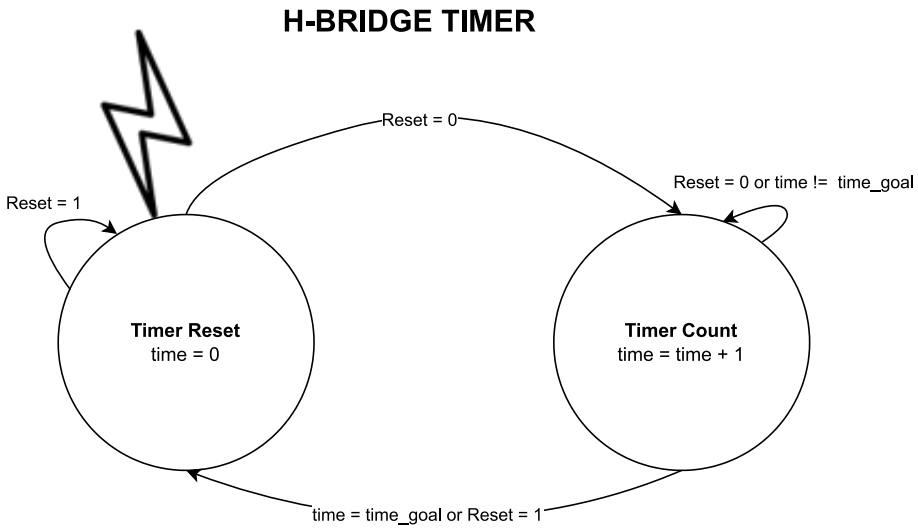

Figure C.4: H-bridge-timer FSM

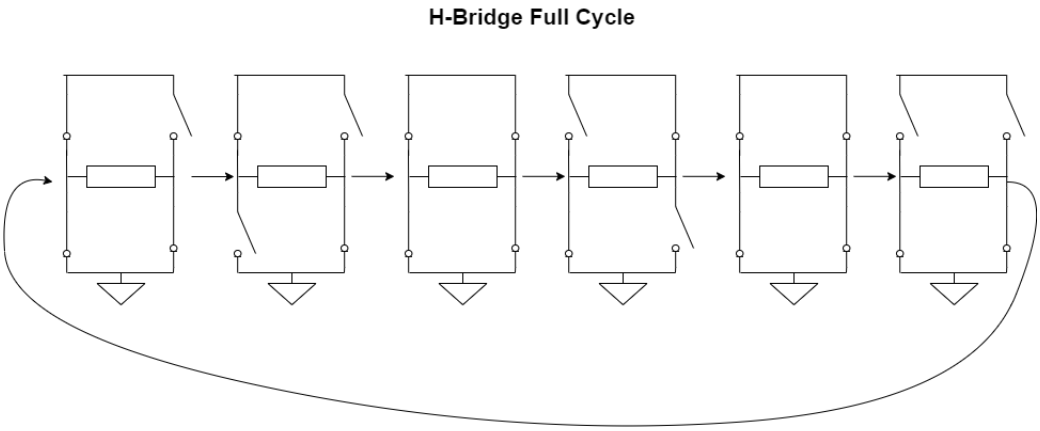

Figure C.5: H-bridge cycle

C.3 Current Sense Control

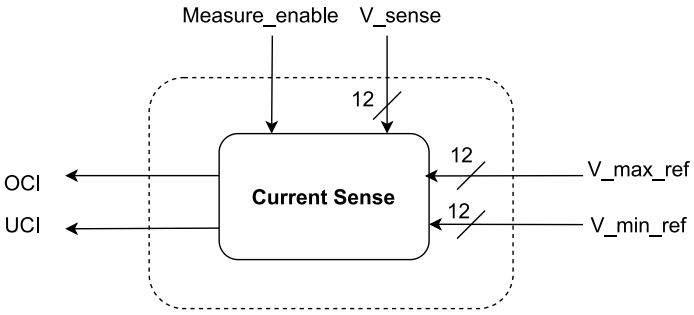

Figure C.6: Current sense diagram

The current sense control in Figure C.6 is responsible for the processing of the voltage that is measured over the sensing resistor. This voltage will be compared with both the maximum and the minimum reference voltage. When the voltage that is sensed is higher than the maximum reference voltage, this means that the current through the sensing resistor is too high. In this situation, the Overcurrent Indicator (OCI) signal will be high. When the voltage is lower than the minimum reference voltage, the current through the sensing resistor is lower than should be. This is a situation of undercurrent, in which the Undercurrent Indicator (UCI) signal is high. When neither is the case, it should be in between the safety margins and therefore no need for any action.

The measure_enable signal is the signal that is received from the H-bridge. The explanation for this signal can be found in section C.2. The signal is a basic indication on whether the signal from the sensing resistor should be taken into account. The FSM can be found in Figure C.7.

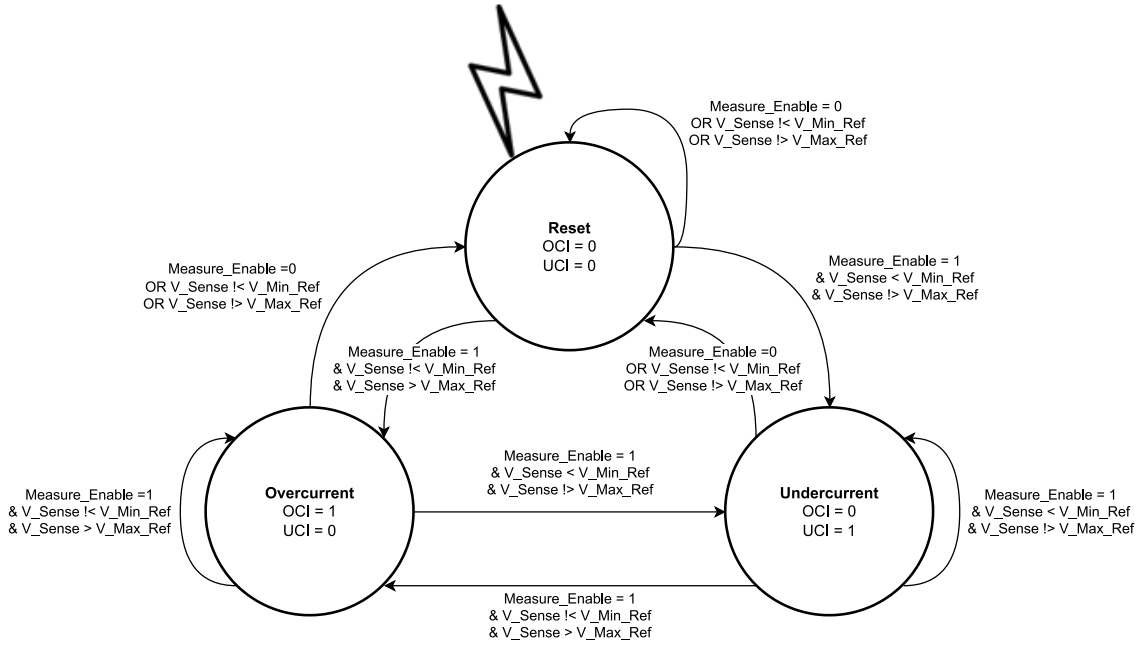

Figure C.7: Current Sense FSM

C.4 DAC

As mentioned in Section 5.1, the current source requires a variable voltage source to generate the reference currents. In order to translate the binary value of the stimulation current into the required input voltage of the current source an DAC is used. For this the MAX5513 [39] was chosen, which is a power efficient DAC with an 8-bit resolution with respect to the reference voltage. To drive the DAC with the integrated circuit, the DAC communication sub-module is required. The DAC expects a serial input including control bits, data bits and sub-bits. In addition, it expects the serial communication clk and a signal which indicates that a command is being sent. An overview of the sub-module with its corresponding in- and outputs is shown in Figure C.8.

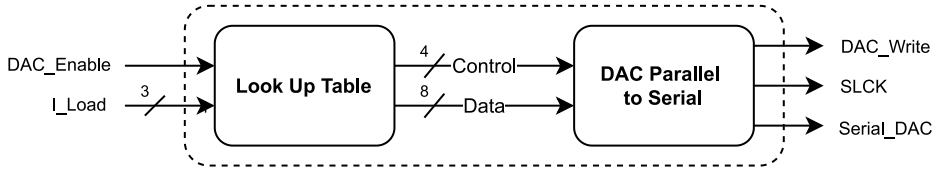

Figure C.8: Overview of the DAC sub-module

The sub-module expects an 3-bit binary number for the required stimulation current (I_Load) and an 1-bit signal which enables the serial communication (DAC_Enable). The Look Up Table translates the 3-bit binary value for the stimulation current into the required 8 data bits. Furthermore, the Look Up Table sends the required control bits. The required timing of the serial communication is shown in Figure C.9.

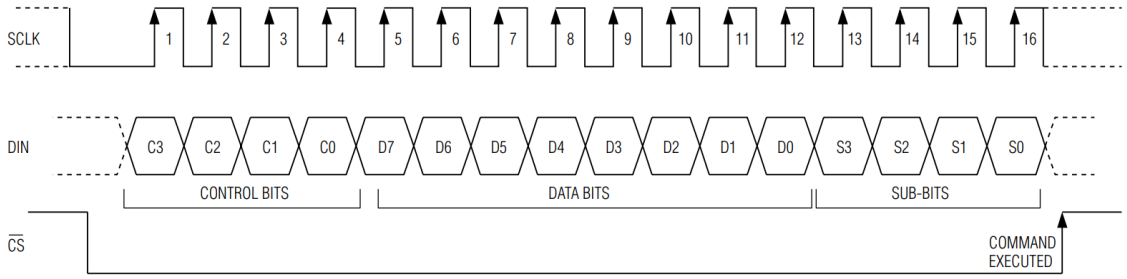

Figure C.9: DAC register loading diagram [39]

The DAC Parallel to Serial module consists of an FSM for sending the serial communication. The FSM is shown in Figure C.10. It consists of 18 states. One reset state, one enable state and then 16 states for sending all bits.

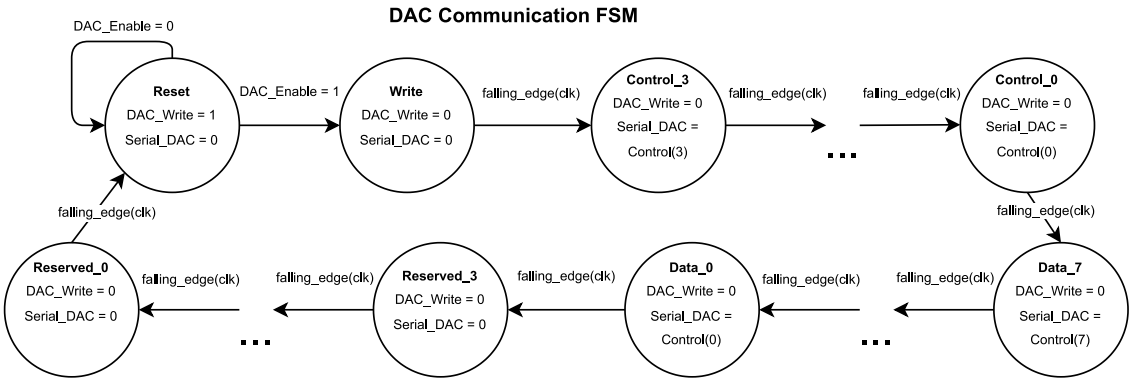

Figure C.10: DAC communication FSM

C.5 Boost Control

The boost control module actively controls the voltage output of the boost converter by changing the PWM signal of it's N-channel MOSFET. Information about the effect of changing about the PWM signal can be found in section 5.5. The sub-module decomposition of the boost control module can be found in figure C.16.

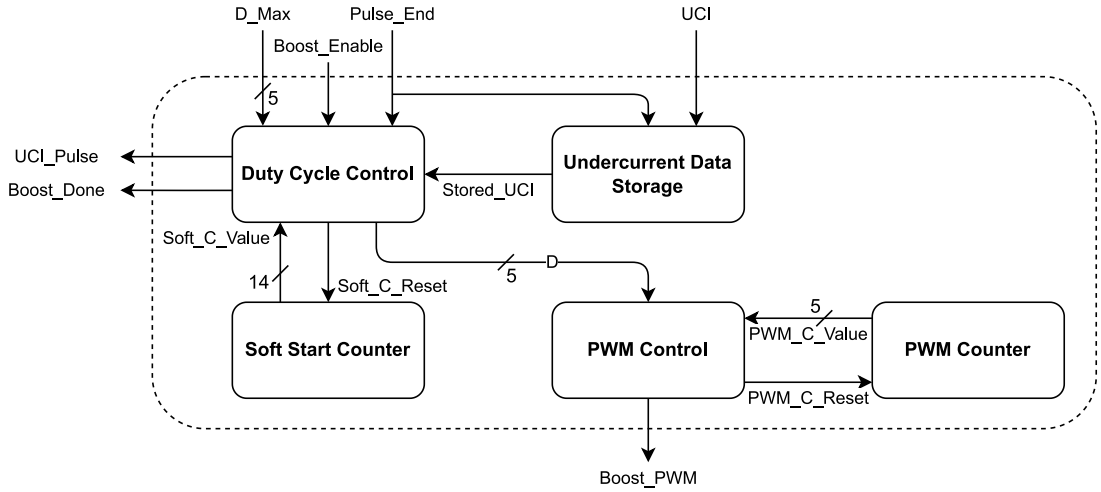

Figure C.11: The Boost control sub-module overview

As described in section 5.5, the boost converter output voltage needs to match the load for the highest efficiency. An algorithm has been implemented in the Duty cycle Control sub-module to find the corresponding duty cycle. This algorithm works as follows: Initially the duty cycle is stepped up gradually until it reaches the maximum allowed duty cycle indicated by the decoder (which depends on the drive current). Then, the duty cycle is slowly stepped down after every stimulation pulse until undercurrent is detected. The undercurrent data storage sub-module makes sure that every undercurrent event will be detected by Duty cycle control. When undercurrent is detected, the Duty cycle control sets its value to last duty cycle when no undercurrent was detected. The duty cycle optimization is done and the value for the duty cycle is maintained. Another undercurrent event will reset the algorithm. With the Duty cycle and a counter, PWM Control will create the desired signal. To avoid an excessive amount of arrows in the duty cycle control FSM, one conditions has been skipped in the figure. All states will have the condition that when that when the 'Enable' signal becomes a logical 0, the Reset state will be entered during the next clock cycle.

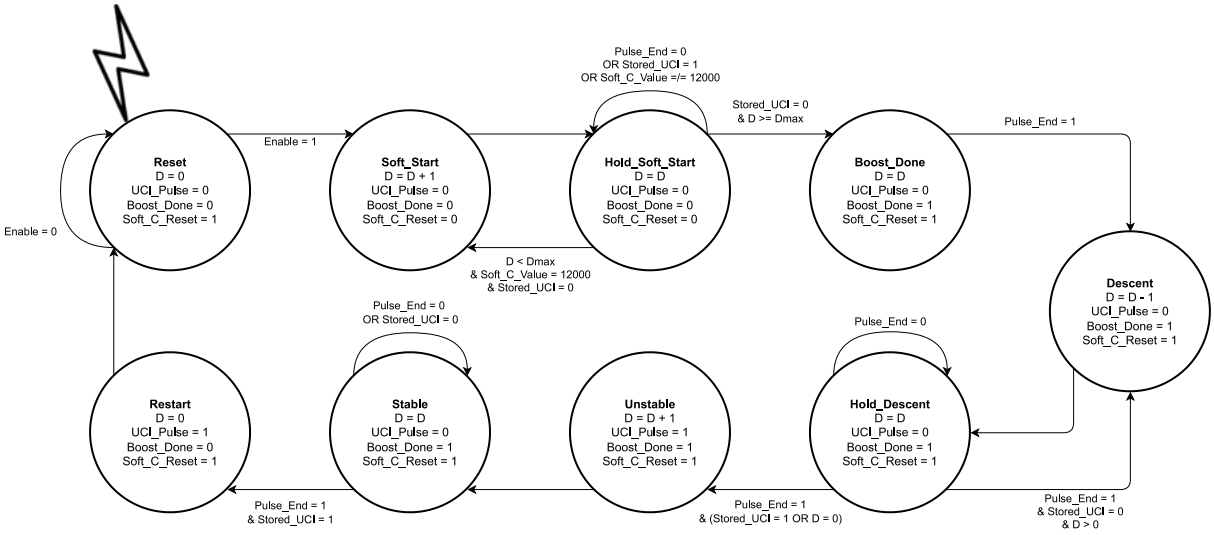

Figure C.12: Duty Cycle control FSM

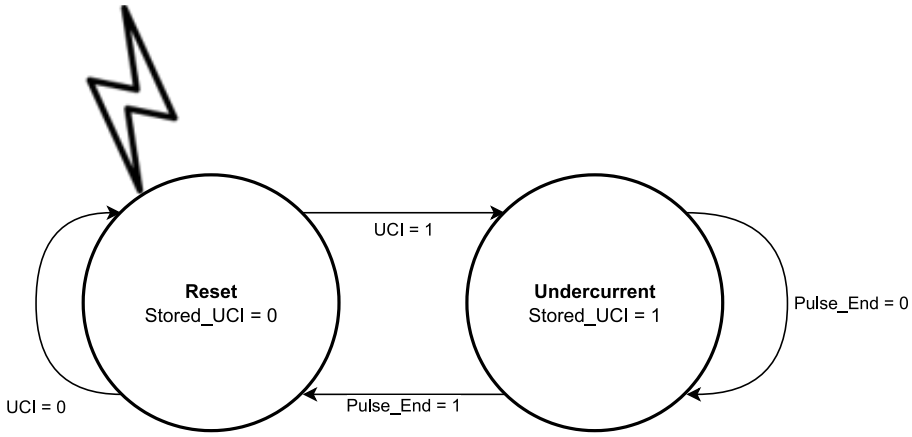

Figure C.13: Undercurrent Data Storage FSM

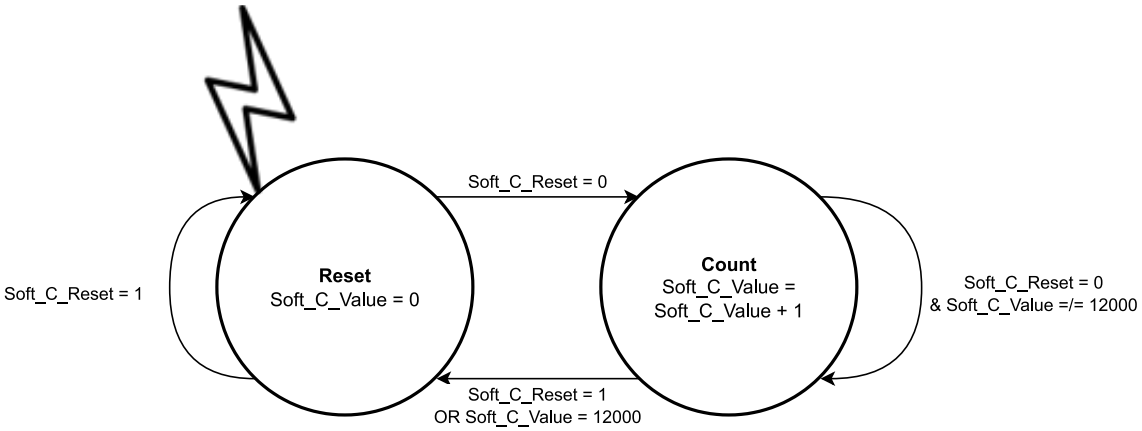

Figure C.14: Soft Start Counter FSM

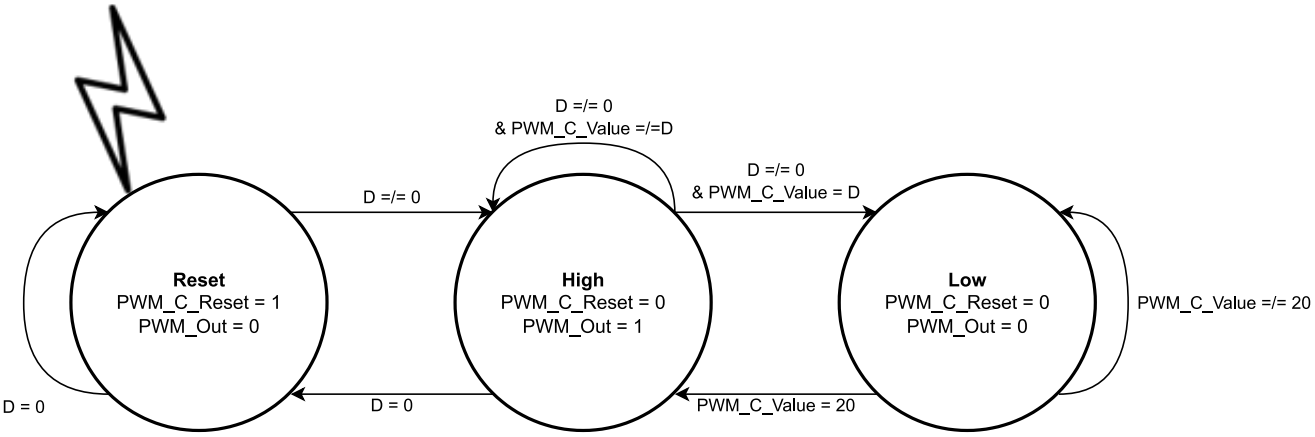

Figure C.15: PWM Control FSM

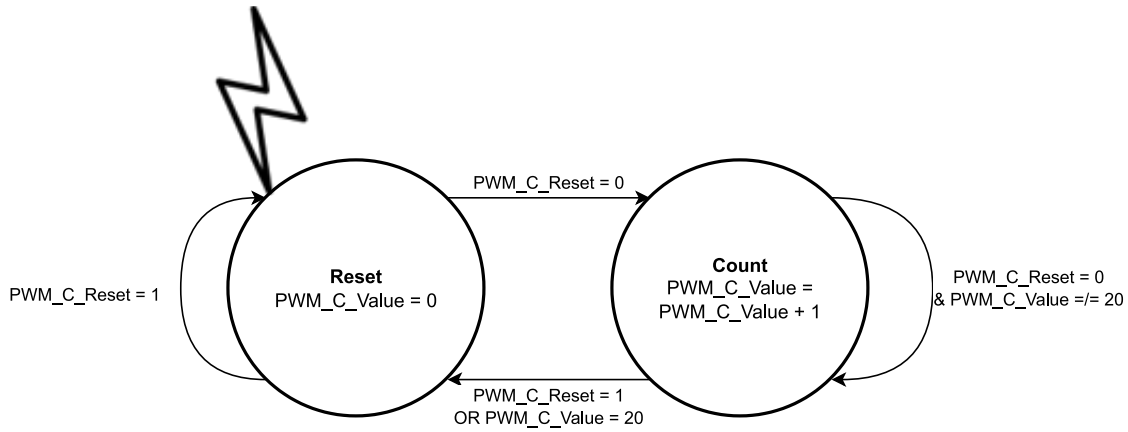

Figure C.16: PWM Counter

C.6 Main Control

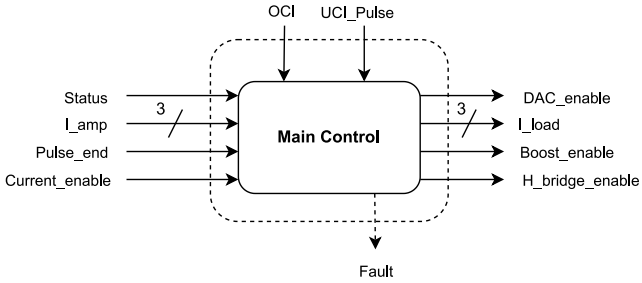

Figure C.17: The Main Control unit with inputs and outputs

The main control unit is responsible for processing the information that is externally received from the microcontroller through the decoder and for responding to signals involving the components. Although it is a very important element in itself, it does not consist of a lot of difficult logic. Its main purpose is to respond to overcurrent from the current sense or a message from the boost converter specifying a situation of undercurrent and the need to up the load. The main control unit is the only way for other control units to communicate with the DAC. Other than listening to those parameters, it is also responsible for turning on other control units such as the H-bridge and the boost converter. The FSM can be found in Figure C.18 and the accompanying FSM in Figure C.19.

In a situation of undercurrent, the boost converter sends a digital 1 to the main control. This pulse is read and is checked with the current undercurrent counter. The undercurrent counter is a measure to check if there are too many consecutive undercurrent pulses. Too much undercurrent means that the impedance of the load is too high which could be due to the fact that the electrodes are poorly connected. As a threshold, receiving 5 undercurrent pulses in a row would indicate that something is wrong which would put the main control in a different state. From this state, a signal is send back to the microcontroller to indicate that something went wrong and that the device needs to be shut down. It is important that the device is shutdown manually because it is important to follow the startup process for the boost converter to build up voltage.

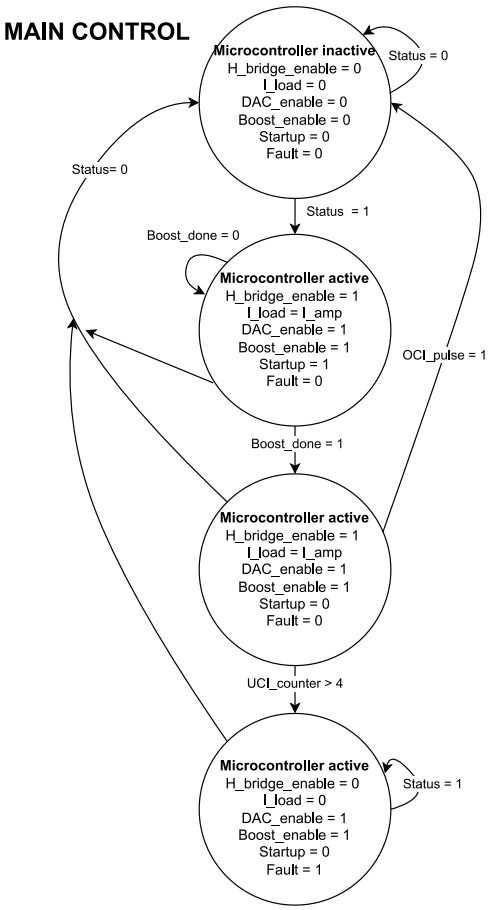

Figure C.18: Main Control FSM

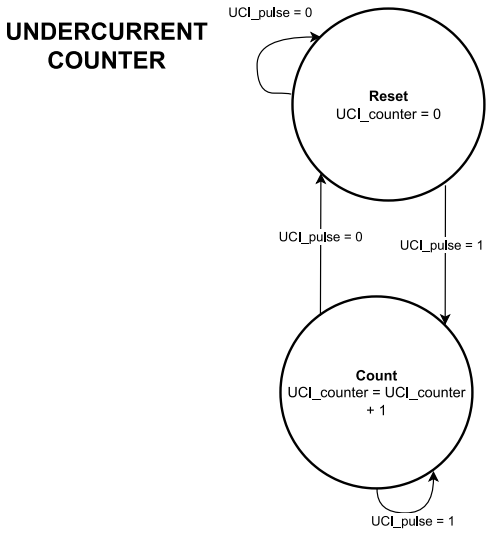

Figure C.19: Control counter for Main Control

C.7 Signal Declarations

Table C.4: IC Signal Declarations

Signal Name	Bits	Explanation
Boost_Done	1	Signal which indicates whether or not the boost startup sequence is completed
Boost_Enable	1	On / off signal for the Boost conrol
Boost_PWM	1	PWM output connected to boost converter
Control	4	DAC communication settings
Current_enable	1	Indication that the H-bridge is in a state in which it can conduct current
DAC_enable	1	Signal to enable or disable current source
D	5	Duty cycle counter value for PWM generation
D_max	5	Maximum allowed duty cycle
DAC_SLCK	1	1 out of 3 DAC communication signals
DAC_Write	1	1 out of 3 DAC communication signals
Data	8	Data to be transmitted to DAC
Fault	1	Error flag which can be read by the microcontroller
H_bridge_enable	1	On / off signal for the H-bridge
I_amp	3	Current magnitude to stimulate with (0 to 8)
I_load	3	Signal to set the current of the current source
Measure_Enable	1	Signal that indicates when accurate current measurements can be taken
Microcontroller_in	6	Encoded stimulation current and frequency
OCI	1	Over Current Indicator,
Pulse_End	1	End of a biphasic pulse indicator.
PWM_C_Reset	1	digital 1 Resets the PWM counter, 0 allows counter to run
PWM_C_Value	5	Value of the PWM counter
Serial_DAC	1	1 out of 3 DAC communication signals
Soft_C_Value	14	Counter value from soft start counter - Boost control
Soft_C_Reset	1	Reset signal for soft start counter - Boost control
Startup	1	Signal indicating startup sequence of boost control
Status	1	Signal which indicates wether or not stimulation is needed
Stored_UCI	1	Stored Under Current Indicator Value. Remembered for 1 stimulation period
s1	1	H Bridge transistor signal 1
s2	1	H Bridge transistor signal 2
s3	1	H Bridge transistor signal 3
s4	1	H Bridge transistor signal 4
Tip	21	Timer value for interpulse time
time	21	timer value - H-bridge control
time_goal	21	The time for which a given state should last inside the H-bridge control
UCI	1	Under Current Indicator
UCI_Pulse	1	Under Current Indicator Pulse
V_Max_Ref	12	Maximum Allowed value for the ADC (to detect overcurrent)
V_Min_Ref	12	Minimum Allowed value for the ADC (to detect undercurrent)
V_sense	12	ADC value

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