

## A Supply Pushing Reduction Technique for LC Oscillators Based on Ripple Replication and Cancellation

Chen, Yue; Liu, Yao-Hong; Zong, Zhirui; Dijkhuis, Johan; Dolmans, Guido; Staszewski, Robert Bogdan; Babaie, Masoud

**DOI**

[10.1109/JSSC.2018.2871195](https://doi.org/10.1109/JSSC.2018.2871195)

**Publication date**

2019

**Document Version**

Accepted author manuscript

**Published in**

IEEE Journal of Solid-State Circuits

**Citation (APA)**

Chen, Y., Liu, Y.-H., Zong, Z., Dijkhuis, J., Dolmans, G., Staszewski, R. B., & Babaie, M. (2019). A Supply Pushing Reduction Technique for LC Oscillators Based on Ripple Replication and Cancellation. *IEEE Journal of Solid-State Circuits*, 54(1), 240-252. Article 8486740. <https://doi.org/10.1109/JSSC.2018.2871195>

**Important note**

To cite this publication, please use the final published version (if applicable).  
Please check the document version above.

**Copyright**

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

**Takedown policy**

Please contact us and provide details if you believe this document breaches copyrights.  
We will remove access to the work immediately and investigate your claim.

# A Supply Pushing Reduction Technique for $LC$ Oscillators Based on Ripple Replication and Cancellation

Yue Chen<sup>1</sup>, Student Member, IEEE, Yao-Hong Liu<sup>2</sup>, Senior Member, IEEE,  
 Zhirui Zong<sup>1</sup>, Student Member, IEEE, Johan Dijkhuis, Member, IEEE,  
 Guido Dolmans, Robert Bogdan Staszewski<sup>3</sup>, Fellow, IEEE,  
 and Masoud Babaie<sup>4</sup>, Member, IEEE

**Abstract**—In this paper, we propose a method to suppress supply pushing of an  $LC$  oscillator such that it may directly operate from a switched-mode dc–dc converter generating fairly large ripples. A ripple replication block (RRB) generates an amplified ripple replica at the gate terminal of the tail current source to stabilize the oscillator’s tail current and thus its oscillating amplitude. The parasitic capacitance of the active devices and correspondingly the oscillation frequency are stabilized in turn. A calibration loop is also integrated on-chip to automatically set the optimum replication gain that minimizes the variation of the oscillation amplitude. A 4.9–5.6-GHz oscillator is realized in 40-nm CMOS and occupies 0.23 mm<sup>2</sup> while consuming 0.8–1.3 mW across the tuning range (TR). The supply pushing is improved to <1 MHz/V resulting in a low < -49-dBc spur due to 0.5–12-MHz sinusoidal supply ripples as large as 50 mV<sub>pp</sub>. We experimentally verify the effectiveness of the proposed technique also in face of saw-tooth, multi-tone, and modulated supply ripples.

**Index Terms**—Common-mode resonance, current-biased oscillator, dc–dc converter, digitally controlled oscillator (DCO), foreground calibration,  $LC$  oscillator, power supply rejection (PSR), ripple replication and cancellation, supply pushing, voltage-controlled oscillator (VCO).

## I. INTRODUCTION

**P**ORTABLE internet-of-things (IoT) devices powered by batteries or energy harvesters generally need buck and/or boost switching dc–dc converters to transform the output levels of energy sources to the nominal supply voltage of IoT electronic circuitry [1]. Due to the switching operation of dc–dc converters, the resulting output ripples can severely

Manuscript received March 5, 2018; revised June 24, 2018 and September 4, 2018; accepted September 7, 2018. This paper was approved by Associate Editor Pietro Andreani. This work was supported in part by the China Scholarship Council under Grant 201406280031 and in part by the Netherlands Organization for Scientific Research under Project #13598. (Corresponding author: Yue Chen.)

Y. Chen, Z. Zong, and M. Babaie are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: y.chen-1@tudelft.nl).

Y.-H. Liu, J. Dijkhuis, and G. Dolmans are with imec-nl, Holst Centre, 5656 AE Eindhoven, The Netherlands.

R. B. Staszewski is with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, Ireland.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2018.2871195

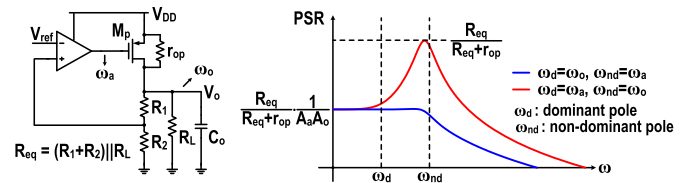


Fig. 1. Block diagram and PSR response of typical LDO topologies.

degrade the performance of the supply sensitive circuitry, such as  $LC$ -tank oscillators, when connected directly.<sup>1</sup> To avoid this, a low dropout (LDO) linear regulator is typically inserted after the switching converter to stabilize the supply voltage [2], [3]. However, the extra voltage overhead ( $\sim 200$  mV) will worsen the system’s power efficiency ( $\sim 80\%$  under 1-V supply). This will make it even more critical with the supply scaling down with technology.

There are two main types of LDO topologies, as determined by whether the dominant pole ( $\omega_d$ ) is at the LDO output ( $\omega_o$ ) or the output of the error amplifier ( $\omega_a$ ) (see Fig. 1) [4], [5]. For the  $\omega_o$ -dominant topology, the large  $C_o$  needed for loop stability can lead to integration difficulties, though a flat power supply rejection (PSR) response (blue curve in Fig. 1) is obtained. The  $\omega_a$ -dominant topology avoids the use of large  $C_o$ , but the PSR starts to degrade after  $\omega_a$  and shows a peak at a higher frequency (red curve in Fig. 1). This appears to be in conflict with the current trend of full system integration, which favors switched-capacitor (SC)-based dc–dc converters clocked at much higher frequencies than with the traditional inductor-based converters. The higher switching frequencies now benefit the dc–dc converters but require large LDO currents and/or complex circuit techniques [6], [7].

From the opposite perspective, techniques have also been proposed in the literature to reduce supply pushing of the oscillator [8]–[16]. In [8], the oscillator is deliberately biased at the point of the lowest sensitivity. The sharp slope of frequency versus current curve around this optimum point makes this approach only practical for tiny ripples (i.e., 1 mV

<sup>1</sup>For example, supply pushing  $K_{\text{push}} = 10$  MHz/V would generate  $-18$ -dB spur under 50 mV<sub>pp</sub> 1-MHz ripple.

in [8]). In [9] and [10], two constant- $g_m$  bias circuits with different current sensitivities to supply are employed in a ring oscillator (RO) to generate a more stabilized current under supply variations. Furthermore, in [10], a calibration loop was added to obtain a more accurate current sensitivity ratio between the two constant- $g_m$  stages. However, the spur-level improvement is limited to  $\sim 10$  dBc for low ripple frequencies ( $f_{\text{ripple}} < 1$  MHz) and gets even worse when  $f_{\text{ripple}}$  increases [10]. Moreover, even when applied to an LC oscillator, the mismatches in the current mirroring ratios limit the spur level to no better than  $-35$  dBc under a  $50\text{-mV}_{\text{pp}}$  ripple. There are also some frequency compensation techniques based on a phase-locked loop (PLL). In [13], the supply induced frequency variation is compensated by adding a replica generation block to the reference path. However, the additional block is bulky and power hungry, while the PLL bandwidth may also restrict the maximum ripple frequency that can be handled. A noise suppression loop was implemented in [14]. It detects the ripple-induced frequency variation by comparing the inverter delay in an RO with a voltage-controlled delay cell and corrects it through a feedback control. However, for LC oscillators that do not provide multiple phases, the delay cell should cover the full oscillation period, thus increasing its power and area consumption.

In this paper, we propose a feed-forward supply ripple replication and cancellation technique wholly contained within an LC oscillator in order to make it *practically* insensitive to supply ripples of switching dc–dc converters. The proposed technique manipulates the gate voltage of the customarily used tail current transistor and does not require any extra voltage headroom. The paper is organized as follows. Section II discusses the operating principles of the proposed technique, while detailed circuit design is given in Section III. Measurement results are disclosed in Section IV.

## II. FEED-FORWARD RIPPLE REPLICATION AND CANCELLATION

As mentioned earlier, the supply pushing of LC-tank oscillators, even those at state of the art, needs to be substantially reduced to allow them to operate *directly* from dc–dc converters, which naturally contain a high level of ripples. In this section, the operating principle of the proposed supply pushing reduction technique based on the ripple replication and cancellation will be elaborated.

### A. Mechanism of Supply Pushing

The variation of oscillating frequency  $f_{\text{osc}}$  with the supply voltage,  $V_{\text{DD}}$ , is mainly caused by the variation of parasitic capacitances seen by the resonant tank [17]. The cross-coupled transistors provide a negative transconductance to sustain the oscillation and will experience cutoff, saturation, and triode operating regions during each oscillation cycle. When  $V_{\text{DD}}$  varies, the tail current,  $I_0$ , and the corresponding oscillation amplitude,  $V_{\text{osc}}$ , will also vary. Thus, it will change the time interval during which the transistors stay in each operating region. Since the gate capacitance of MOS transistors shows the nonlinear dependence on the voltages at their terminals

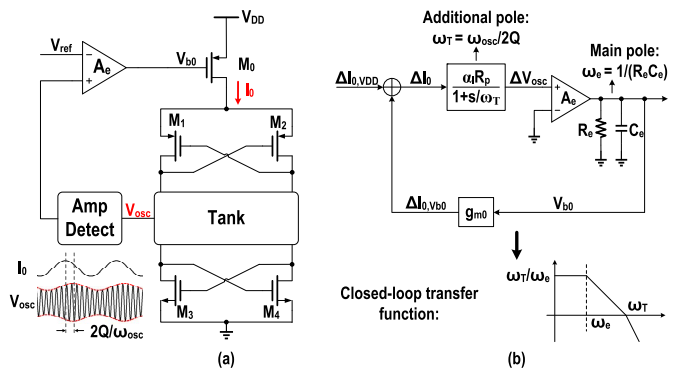


Fig. 2. (a) Schematic and (b) block diagram of an LC oscillator with amplitude tracking loop.

(i.e.,  $V_{\text{gs}}$  and  $V_{\text{ds}}$ ), the change in their operating states would vary the equivalent parasitic capacitance,  $C_{\text{par, equ}}$  [18]. Thus, the oscillating frequency will be pushed. If a periodical ripple is on  $V_{\text{DD}}$ ,  $I_0$  and  $V_{\text{osc}}$  will also show periodical variations. Therefore, the change of  $C_{\text{par, equ}}$  will also be periodical and could manifest itself as large spurs in the output spectrum of the oscillator. To be able to obtain a clean output spectrum when  $V_{\text{DD}}$  contains ripples,  $I_0$  and  $V_{\text{osc}}$  should be stabilized under  $V_{\text{DD}}$  variations.

### B. Amplitude Tracking Loop

Conventional solutions to stabilize the oscillating amplitude of an LC oscillator resort to employing an amplitude tracking loop across process, voltage, and temperature (PVT) variations [19] and to bias the oscillator at the optimum operational point [best figure-of-merit (FoM)] [20]. It is instructive to examine this loop for stabilizing  $I_0$  and  $V_{\text{osc}}$  under supply ripples.

Fig. 2(a) shows the schematic of an LC oscillator with amplitude tracking loop. The tail current source transistor,  $M_0$  is PMOS, which is fairly robust to (local) ground-induced perturbations. Replacing  $M_0$  with an NMOS transistor will not help much as its  $V_{\text{gs}}$  will be now very sensitive to local ground perturbations and its  $I_0$  sensitivity to  $V_{\text{DD}}$  will still be felt through the  $M_0$ 's channel length modulation. The loop first detects the oscillation amplitude, and then compares it with the reference value  $V_{\text{ref}}$ . The comparison outcome will adjust  $I_0$  by varying the gate bias voltage  $V_{b0}$  of  $M_0$ . This feedback loop will keep on working to fix  $V_{\text{osc}}$  at the level corresponding to  $V_{\text{ref}}$ . When  $I_0$  and correspondingly  $V_{\text{osc}}$  are modulated by the supply ripple,  $V_{b0}$  will be modulated in reaction through the amplitude tracking loop. As a result, the variation of  $I_0$  and  $V_{\text{osc}}$  will be reduced by an amount equal to the loop gain of the amplitude tracking loop, thus reducing the variation of oscillating frequency.

Unfortunately, this method is limited by the pole from the resonance tank. When the supply varies,  $I_0$  will follow almost immediately. However, due to a “memory” of the tank, there is a time delay,  $2Q/\omega_{\text{osc}}$ , between the variation of the current flowing through the tank and the subsequent effect on the oscillation amplitude across the tank, as shown in Fig. 2(a) [19]. Such a time delay creates an additional

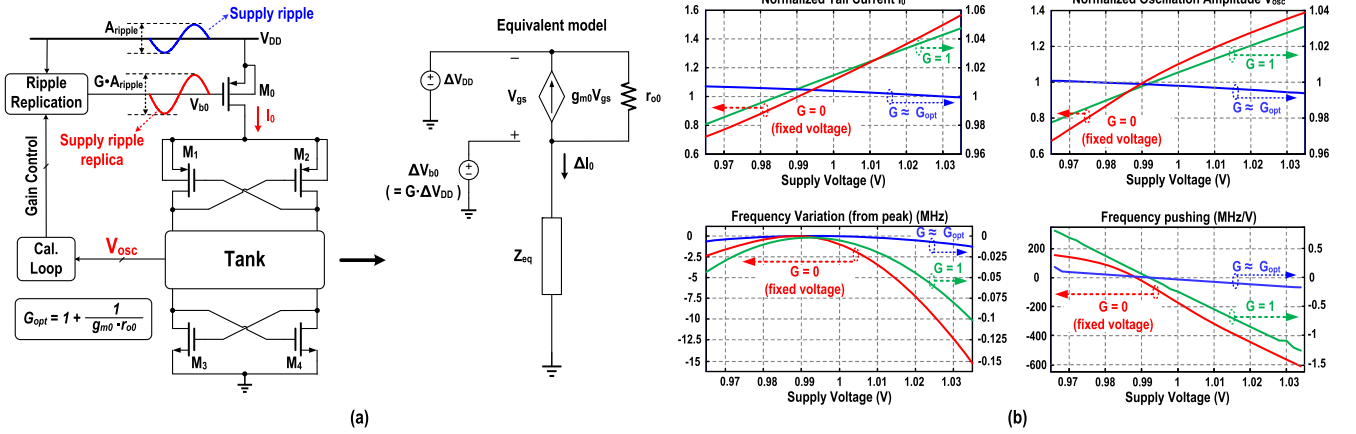


Fig. 3. (a) Conceptual block diagram of the proposed supply pushing reduction technique with the equivalent model to estimate the optimum gain ( $G_{opt}$ ) of the RRB. (b) Simulation results of an *LC* oscillator with the proposed technique.

low-frequency pole located at  $\omega_{osc}/(2Q)$  and will limit the bandwidth of the amplitude tracking loop [see Fig. 2(b)] [21]. This bandwidth limitation could limit the spur level that can be reached with this method. To alleviate this limitation, the pole at the output of the amplifier must be pushed to a very high frequency, since the pole related to the tank is almost fixed. However, this may lead to a significant increase in the current consumption of the loop.

### C. Proposed Technique

In this section, we propose a feed-forward supply pushing reduction technique for *LC* oscillators that entirely avoids the use of the amplitude tracking loop around the oscillator core. Fig. 3(a) illustrates its principle. To stabilize  $I_0$ , and thus  $V_{osc}$ , in face of  $V_{DD}$  variations, a replica of the supply ripple is applied to the gate of PMOS current source  $M_0$  to stabilize its  $V_{gs}$ . As a result, the variation of  $I_0$  and  $V_{osc}$  would be largely suppressed. If  $M_0$  is an ideal device, whose drain current is solely controlled by its  $V_{gs}$  according to the square law, then an exact copy of the supply ripple waveform is required at its gate terminal  $V_{b0}$  to keep  $I_0$  and  $V_{osc}$  constant. As shown in Fig. 3(b), the variations of  $I_0$  and  $V_{osc}$  do get largely suppressed when the waveform applied at  $V_{b0}$  is the same as that of the supply ripple (gain,  $G = 1$ ). Hence, the frequency variations due to the supply voltage are largely reduced, resulting in a much lower supply pushing of the oscillator. However, for nanoscale CMOS technologies, the channel-length modulation effect is not negligible. This means that the drain current of  $M_0$  also depends on its  $V_{ds}$ . Thus, the waveform at  $V_{b0}$  should be an *amplified* replica of the supply ripple to compensate for the residue current variation due to the variation of  $V_{ds}$  of  $M_0$ . Fig. 3(a) also shows the equivalent model to estimate the optimum gain ( $G_{opt}$ ). Based on this model, the supply variation,  $\Delta V_{DD}$ , induced tail current variation,  $\Delta I_0, V_{b0}$ , could be calculated as

$$\Delta I_0, V_{b0} \approx \frac{1 + g_{m0} \cdot r_{o0}}{r_{o0} + Z_{eq}} \Delta V_{DD} \quad (1)$$

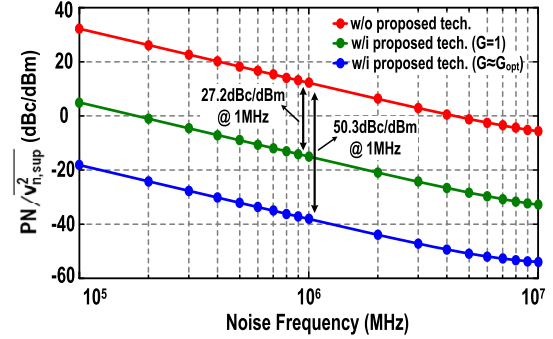


Fig. 4. Simulated transfer function of the supply noise to PN of the oscillator with/without the proposed supply pushing reduction technique.

while the tail current variation induced by  $\Delta V_{b0} = G \cdot \Delta V_{DD}$  is

$$\Delta I_0, V_{b0} \approx -\frac{g_{m0} \cdot r_{o0}}{r_{o0} + Z_{eq}} \Delta V_{b0} \quad (2)$$

where  $Z_{eq}$  is the large-signal equivalent impedance of the cross-coupled transistors  $M_{1-4}$  and the tank that is seen by  $M_0$ , while  $g_{m0}$  and  $r_{o0}$  are the effective transconductance and output resistance of  $M_0$ , respectively. To compensate for the tail current variation due to  $V_{ds}$ , the magnitudes of (1) and (2) should be equal. Hence,  $G_{opt}$  is calculated as

$$G_{opt} \approx 1 + \frac{1}{g_{m0} \cdot r_{o0}}. \quad (3)$$

Since  $g_{m0} \cdot r_{o0}$  is relatively large (e.g.,  $> 10$ ),  $G_{opt}$  is slightly higher than 1. Fig. 3(b) also shows that  $I_0$  and  $V_{osc}$  are further stabilized (i.e.,  $\sim 10\times$  smaller variations compared to  $G = 1$  case) under supply variations when  $G \approx G_{opt}$ , thus the supply pushing of the oscillator becomes much lower. It also translates into a significant reduction in the thermal noise of supply to phase noise (PN) conversion as can be gathered from Fig. 4.

The similar feed-forward principle was applied to LDOs in order to improve their PSR at several megahertz of ripple frequencies [22]–[24]. However, they lack a reliable calibration for the optimum gain, which will be proposed later. Also, they still tend to use large off-chip capacitors [22] or extra

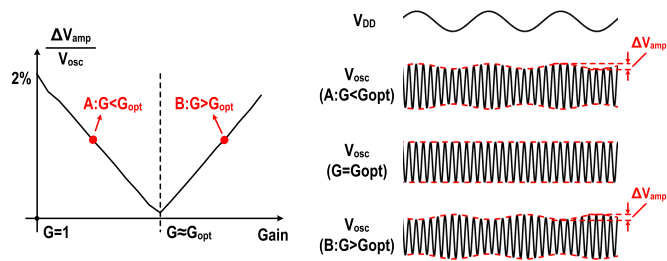


Fig. 5. Operating principle of the calibration loop based on oscillation amplitude variation ( $\Delta V_{amp}$ ).

on-chip capacitance occupying large silicon area [24]. When the LDO is integrated with a current-biased oscillator, the pass transistor should be placed above the tail current source  $M_0$ , thus consuming extra voltage headroom. Merging the pass transistor with  $M_0$  would reclaim this headroom, but the oscillator becomes voltage-biased, whose current is poorly controlled over PVT variations. Also, higher supply sensitivity of a voltage biased oscillator would place higher demands on the PSR performance of the LDO, resulting in large power and area overhead [2].

The amplified supply ripple replica at  $V_{b0}$  is generated by the proposed ripple replication block (RRB). As can be gathered from (3), the optimum gain is prone to PVT variations. Therefore, a calibration loop is also integrated on-die, as indicated in Fig. 3(a). The calibration scheme is based on measuring the variation of the oscillation amplitude,  $\Delta V_{amp}$ , in response to the  $V_{DD}$  perturbations. Fig. 5 shows the operating principle. When  $G < G_{opt}$  (case A),  $\Delta I_{0,V_{b0}}$  is smaller than  $\Delta I_{0,V_{DD}}$ , so  $\Delta V_{amp}$  is in phase with  $\Delta V_{DD}$  and decreases in magnitude as  $G$  gets closer to  $G_{opt}$ . However, when  $G > G_{opt}$  (case B),  $\Delta I_{0,V_{b0}}$  becomes larger than  $\Delta I_{0,V_{DD}}$ . Then,  $\Delta V_{amp}$  is out of phase with  $\Delta V_{DD}$ , and its magnitude increases again with the increase of  $G$ . At the optimum point,  $G = G_{opt}$ , and ideally a constant oscillation amplitude is maintained under supply variations. Thus, the calibration loop measures  $\Delta V_{amp}$  under different gain settings to calculate the optimum operating point for the oscillator circuit.

### III. CIRCUIT IMPLEMENTATION

In this section, we discuss the detailed circuit realization of a 5-GHz  $LC$  oscillator with the proposed feed-forward supply pushing reduction technique and the on-chip calibration loop.

#### A. Ripple Replication Block

Fig. 6 shows the schematic of the implemented  $LC$  oscillator with the RRB. Here, the complementary cross-coupled oscillator structure is chosen due to its lower power consumption compared to its NMOS and PMOS only counterparts at the same  $V_{DD}$  and equivalent parallel resistance of the tank.

The RRB is proposed to bias the gate terminal of a tail current source of the  $LC$  oscillator. To generate the required replica with the desired gain larger than 1, the RRB is logically divided into two parts. The first part (gray-dashed box in Fig. 6) contains a diode-connected PMOS transistor,

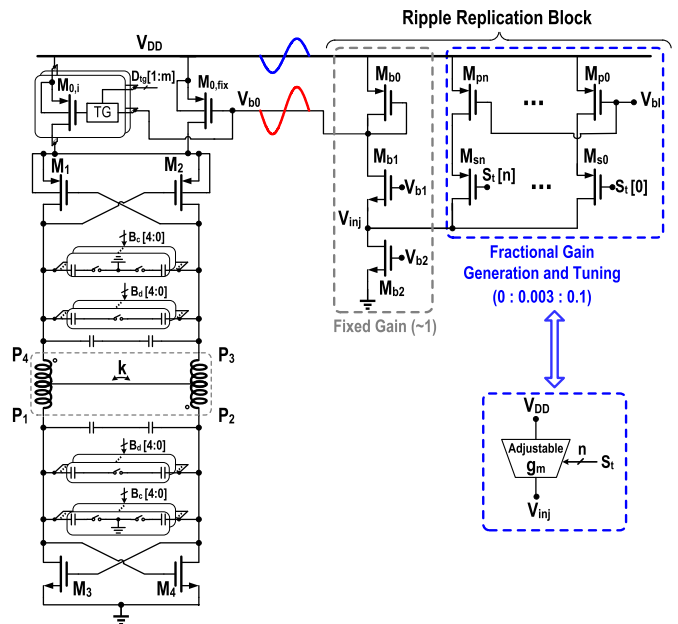


Fig. 6. Schematic of the implemented  $LC$  oscillator with the RRB.

$M_{b0}$ , in series with two cascode NMOS transistors,  $M_{b1,2}$ . Due to the high output impedance of the cascode,  $M_{b0}$  just “replicates” the supply ripple to  $V_{b0}$  with a fixed gain of 1. Thus, the first term on the right-hand side of (3) is covered by this part. To boost the gain above 1, the fractional part (blue-dashed box in Fig. 6) is introduced to inject some extra current proportional to  $V_{DD}$  into the cascode node,  $V_{inj}$ . To digitally control the fractional gain, current sources  $M_{pk}$  ( $k = 0, 1, \dots, n$ ) are individually turned on/off by switch transistors  $M_{sk}$  ( $k = 0, 1, \dots, n$ ) according to the digital code  $S_t$  generated by the calibration loop. The fractional part thus provides an adjustable transconductance between  $V_{DD}$  and  $V_{inj}$ . The final gain  $G$  provided by the RRB could be approximated as

$$G \approx 1 + \frac{g_{m,f}}{g_{m,b0}} \quad (4)$$

where  $g_{m,f}$  and  $g_{m,b0}$  are the total equivalent transconductance of the fractional part and the transconductance of  $M_{b0}$ , respectively. Since  $G_{opt}$  is only slightly larger than 1, the required  $g_{m,f}$  should be much smaller than  $g_{m,b0}$ . Therefore, the total current injected into  $V_{inj}$  is much smaller than the current consumed by  $M_{b0}$ , and would not lead to a large variation of the operating point of the  $LC$  oscillator. In practice, the gain provided by the integer part is slightly lower than 1 due to the finite output impedance of the cascode transistors. Furthermore, for designs with lower  $V_{DD}$ , the cascode transistor  $M_{b1}$  could be removed which would further reduce the gain of the integer part. However, any reasonable (i.e.,  $\sim 5\%$ ) integer gain degradation can be easily covered by the fractional part.

1) *Bandwidth and Power Consumption Tradeoff*: The required bandwidth of the RRB is determined by the maximum spur level allowed at the highest ripple frequency.

Assuming a phase shift of  $\theta$  between the supply ripple at oscillator’s  $V_{DD}$ ,  $0.5 \cdot A_{ripple} \cos(2\pi f_{ripple}t)$ , and the generated

replica at  $V_{b0}$  at the optimum gain, the tail transistor  $M_0$  would experience an effective supply variation of

$$V_{\text{rip,eff}} = -A_{\text{ripple}} \cdot \sin\left(\frac{\theta}{2}\right) \cdot \sin\left(2\pi f_{\text{ripple}}t - \frac{\theta}{2}\right) \quad (5)$$

where  $A_{\text{ripple}}$  is the peak-to-peak amplitude of the supply ripple. Therefore, the spur level in the output spectrum of the oscillator could be calculated as

$$S_{\text{spur-carrier}} = 20 \cdot \log_{10}\left(\frac{K_{\text{push}} \cdot A_{\text{ripple}} \cdot \sin\left(\frac{\theta}{2}\right)}{2f_{\text{ripple}}}\right). \quad (6)$$

To guarantee  $<-50$  dBc spur level at  $f_{\text{ripple}} = 20$  MHz, which is the highest ripple frequency considered in this paper, the maximum tolerable  $\theta$  is calculated to be  $\sim 3^\circ$  under 50-mV<sub>pp</sub> ripple and  $K_{\text{push}} \approx 100$  MHz/V.

In the frequency range of interest, the RRB may be approximated as a single-pole system, with the pole located at  $\omega_p = g_{m,b0}/C_L$ , where  $C_L$  is the capacitive load at  $V_{b0}$ . Thus, to obtain  $\sim 3^\circ$  phase shift at 20 MHz,  $\omega_p \approx 400$  MHz is required. Considering  $\sim 800$ -fF load, the calculated  $g_{m,b0}$  should be about 2.0 mS. With  $g_m/I_{ds} \approx 12$ , the current consumption of the integer part is calculated to be  $\sim 170$   $\mu$ A. Together with  $\sim 12$   $\mu$ A consumed by the fractional part at the maximum  $G$  of  $\sim 1.1$ , the total current consumption of the RRB is around 180  $\mu$ A. The PMOS transistors in the fractional part are sized to achieve tuning resolution of  $\sim 0.003$  as a tradeoff between the resolution and calibration time. Therefore, a 5-bit thermometer code is implemented to cover the aforementioned maximum  $G$ .

Due to the distributed layout design, there could be a delay between the routed  $V_{DD}$  at the oscillator's  $M_0$  source and at the RRB. That delay can increase the ripple phase shift  $\theta$  of the RRB. In this design, since the proposed RRB is simple and compact, it is easily placed next to  $M_0$ . Hence, this effect is negligible, especially at ripple frequencies  $< 20$  MHz.

2) *Sizing and Biasing of Tail Transistor*: The tail current transistor  $M_0$  is designed here with a channel length of 120 nm, contributing to the capacitive load  $C_L$  mentioned earlier. The optimal gain  $G_{\text{opt}}$  is simulated to be in the middle of the 1–1.1 range provided by the RRB, leaving enough margin on both sides. By using  $M_0$  with a shorter channel length,  $C_L$  could be reduced, leading to a lower power consumption. However, the required  $G_{\text{opt}}$  would increase due to a smaller output resistance of  $M_0$ , which could adversely affect the tuning resolution and/or calibration time.

Under the 1-V nominal supply voltage,  $V_{ds}$  of  $M_0$  is chosen to be around 250 mV. A smaller  $V_{ds}$  may allow the oscillator to operate under lower supply voltage, thus reducing its power consumption. However, a larger  $M_0$  would be needed to provide similar tail current, which also generates more noise, degrading the PN and FoM performance of the oscillator [25]. Moreover, with a lower  $V_{ds}$ , the output resistance of  $M_0$  also becomes smaller, leading to an increase in  $G_{\text{opt}}$ . Combined with the increased parasitic capacitance due to the larger device size, the bandwidth of the RRB would be reduced under similar power consumption, thus increasing the phase shift  $\theta$  of the replica at  $V_{b0}$ . As discussed earlier, this would increase

the output spur level of the oscillator. Hence, it is not beneficial to reduce  $V_{ds}$  further.

In the actual design,  $M_0$  is implemented as a parallel combination of a fixed part,  $M_{0,\text{fix}}$ , with a bank of unit transistors,  $M_{0,i}$ , as shown in Fig. 6. Each  $M_{0,i}$  could be switched in separately to tune the oscillation swing by enabling the corresponding transmission gate (TG) before its gate terminal with the control code  $D_{\text{ig},i}$ . The tail current resolution is  $\sim 30$   $\mu$ A to ensure the oscillator operates within 1 dB of its optimum PN across the tuning range (TR). To cover the required current range under PVT variations, 27 such unit transistors are implemented.

## B. Calibration Loop

Fig. 7 shows the block diagram of the integrated calibration loop. As discussed in Section II-C, the perturbation of the oscillation amplitude,  $\Delta V_{\text{amp}}$ , is used in the loop as a stimulus to calibrate  $G_{\text{opt}}$ . Hence, the outputs of the oscillator are first connected to a peak detector. Ideally, the output of the peak detector,  $V_{\text{pd}}$ , contains two frequency components: the desired one at  $f_{\text{ripple}}$ , and the additional one at the second harmonic of the oscillation frequency,  $f_{\text{osc}}$ .  $V_{\text{pd}}$  is then amplified through self-biased inverters. To amplify the small input level at  $V_{\text{pd}}$  (e.g., 1 mV) to a large enough amplitude (e.g., 250 mV) at the output, a large gain (e.g., 48 dB) is needed. Hence, two inverter stages with a bandwidth of  $\sim 20$  MHz are implemented to provide the required gain [see Fig. 9(a)]. The output of the inverter chain,  $V_{\text{inv}}$ , is filtered by a simple RC low-pass filter (LPF). The cutoff frequency of the LPF is set to pass through the desired frequency component at  $f_{\text{ripple}}$ , while the second harmonic at  $2 \times f_{\text{osc}}$  is filtered out. If there is any mismatch in the input differential pair of the peak detector,  $V_{\text{pd}}$  would contain a third frequency component at  $f_{\text{osc}}$ . Since  $f_{\text{osc}}$  (several gigahertz) is much higher than  $f_{\text{ripple}}$  (tens of megahertz), this component is easily filtered out by the inverter chain and the LPF. Hence, the mismatch in the peak detector will not affect the calibration results. The output of the LPF,  $V_{\text{lpf}}$ , is then compared with a reference value,  $V_{\text{ref}}$ , through a comparator.  $V_{\text{ref}}$  is roughly set to a voltage higher than the product of the desired  $\Delta V_{\text{amp}}$  and the dc gain of the peak detector cascade with the inverter stages. The output of the comparator is connected to the clock terminal of a D flip-flop (DFF). When  $V_{\text{ref}}$  is crossed, the comparator's output becomes high, triggering the output of the DFF to flip to "1". The digital algorithm in the loop monitors the latch output,  $\text{Latch\_out}$ , and calculates the optimum control code  $S_t$  for the RRB.

The digital block attempts to find the minimum point of  $\Delta V_{\text{amp}}$  versus the control code [ $\Delta V_{\text{amp,min}}$  in Fig. 8(a)]. However, to precisely detect  $\Delta V_{\text{amp,min}}$ , a set of comparators and DFFs would be needed. The simulated amplitude variation at the output of the LPF is  $\sim 300$  mV. Thus, 20 comparators, followed by a DFF each, are required to realize a voltage resolution of 15 mV. Some offset calibration techniques may also be needed to reduce the input referred offset of comparators to a level much lower than the voltage resolution. The digital algorithm then counts the number of "1" in the output of the DFFs to determine  $\Delta V_{\text{amp}}$ . Such a method could increase the design complexity greatly. To avoid this,

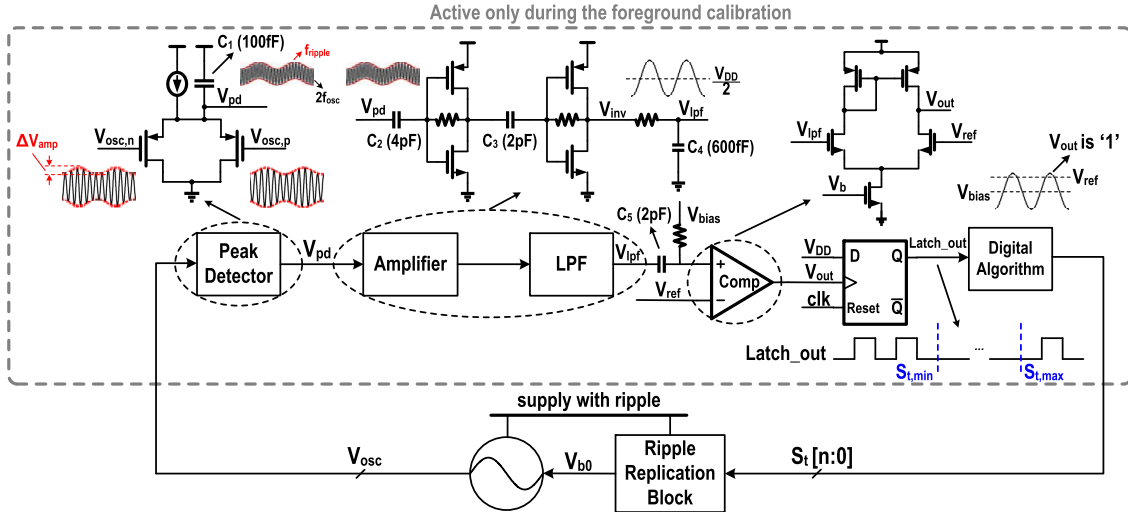


Fig. 7. Block diagram of the calibration loop.

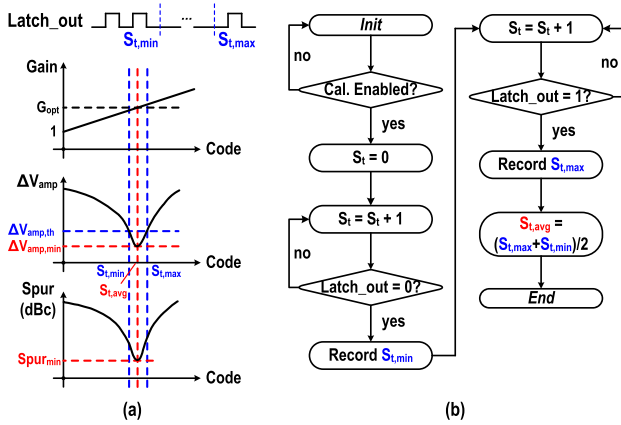
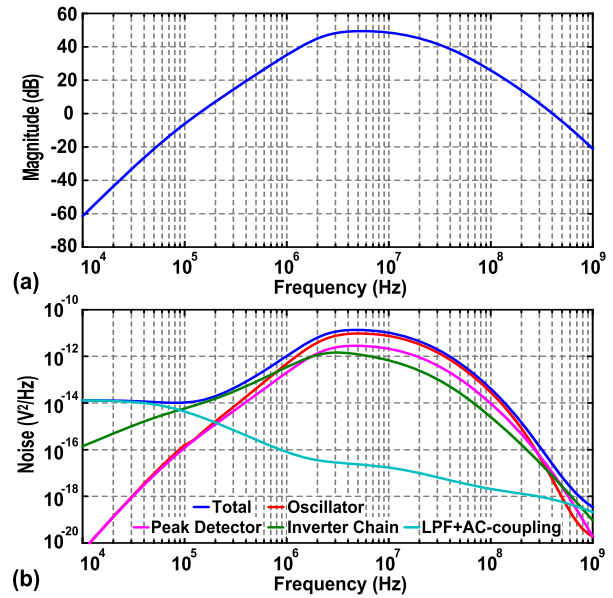


Fig. 8. (a) Operating principle and (b) flowchart of the calibration loop with the proposed algorithm.

a calibration algorithm is proposed whereby only one comparator without any offset calibration could be used in the loop. Fig. 8(a) shows the operating principle of the proposed technique. The reference voltage,  $V_{ref}$ , at the comparator input is roughly set to a value corresponding to an oscillation amplitude variation of  $\Delta V_{amp,th}$ , which is higher than  $\Delta V_{amp,min}$ . The calibration process starts from a small value of  $S_t$ , where  $G < G_{opt}$  and  $\Delta V_{amp} > \Delta V_{amp,th}$ . Thus, the initial value of Latch\_out is “1.” The algorithm keeps increasing  $S_t$ , which decreases  $\Delta V_{amp}$  as  $G$  approaches  $G_{opt}$ . When  $\Delta V_{amp}$  becomes lower than  $\Delta V_{amp,th}$ , Latch\_out changes from “1” to “0.” The algorithm records this code as  $S_{t,min}$ , and then increases  $S_t$  again. When  $S_t$  is large enough,  $\Delta V_{amp}$  would be higher than  $\Delta V_{amp,th}$  again, and Latch\_out switches back to 1. The algorithm records this code as  $S_{t,max}$ , and the optimum code,  $S_{t,avg}$ , is calculated as the average of these two recorded codes. Fig. 8(b) reveals the operational flowchart of this calibration process.

Fig. 9(a) shows the simulated transfer function from the output of the peak detector to the input of the comparator. The lower cutoff frequency of this bandpass response is due to the ac coupling used to accommodate the dc levels of different

Fig. 9. (a) Simulated transfer function from  $V_{pd}$  to comparator input. (b) Simulated PSD of noise at comparator input with the contribution from different noise sources.

stages in the loop. It sets the lowest  $f_{ripple}$  that the loop can handle. In this paper, this frequency is designed to be  $\sim 2$  MHz. Considering the current trend in increasing the switching frequency of the dc–dc converters to several or even tens of megahertz [26]–[29], this value appears reasonable. A lower cutoff frequency could be adopted to detect lower ripple frequencies, but at the expense of increased loop settling time. When  $S_t$  changes in each calibration step, the current injected by the fractional part varies, leading to slight variations in the tail current and the oscillation amplitude of the oscillator. Hence, due to the bandpass characteristic of the loop, it needs a certain time for settling before correctly functioning. With 2-MHz corner frequency, the settling time is  $0.5 \mu s$  per step.

Fig. 9(b) shows the simulated power spectrum density (PSD) of noise at the comparator’s input. The major part

of it is contributed by the oscillator itself. The differential output of the oscillator is less affected by the variation of the common-mode voltage, but the output level of the peak detector would be modulated. Thus, the calibration loop is more sensitive to the common-mode noise from the oscillator, e.g., the noise of the tail current source. After being shaped by the transfer function of the inverter chain and LPF, the common-mode noise is finally passed to the comparator's input. From Fig. 9(b), the integrated noise is around 14 mV, corresponding to  $\sim 0.095$  mV equivalent input noise at the input of the peak detector. To achieve  $< -50$ -dBc spur level,  $\Delta V_{\text{amp}}$  is simulated to be  $\sim 1.8$  mV ( $0.64$  mV<sub>rms</sub>), leading to an SNR of 16.5 dB, which is sufficient for an effective calibration.

The proposed calibration algorithm and RRB are still effective even if the ripple of the dc-dc converter is simultaneously coupled through the supply and other parasitic paths, e.g., into the dc output of the RRB or ground. Since the coupling through both paths would also vary the tail current, and correspondingly the oscillation amplitude, their effect would be detected and minimized by the calibration algorithm through adjusting  $G_{\text{opt}}$ . Besides the supply ripples, interference from other sources with different frequencies may also modulate the oscillation amplitude. However, with proper design techniques, e.g., shielding and placing guard rings, which are common in oscillator design, the effect of these interference should be non-dominant, and the calibrated code is still around the optimum one.

It should be pointed out that the main purpose of this paper is to verify the ripple replication circuitry and the principle of the calibration algorithm. Hence, a quiet supply is used for the calibration loop. If the ripple also exists on the supply of the loop, its effect could be suppressed with *RC* filtering since the power consumption of the peak detector and the amplifier, which are the supply sensitive blocks in the loop, is much smaller compared to that of the oscillator. When used in the whole system, e.g., PLL, the calibration loop may also be powered by the regulators used for other supply sensitive blocks, e.g., time-to-digital converter (TDC) and digital-to-time converter (DTC). Since the loop only operates for a short time ( $\sim 40$   $\mu$ s in the worst case) at system startup or whenever needed at the beginning of IoT packets, it would not affect the system efficiency and the performance of other blocks during the normal operation. If the entire system was to be powered by the SC converter directly, a  $> 40$ -dB PSR ratio would be required for the calibration loop, which is not difficult to achieve with conventional analog design techniques at the relatively low operating frequency of the loop (i.e.,  $< 20$  MHz) [30]–[32].

### C. Oscillator Implementation

The designed oscillator uses a transformer-based resonant tank. Since the RRB is connected to the gate of tail current source  $M_0$ , its output noise [see Fig. 10(a)] will modulate the oscillator's tail current, thus converting into PN. Similar to the tail current noise, only the noise around dc and even harmonics of  $f_{\text{osc}}$  would cause PN degradation [33]–[35]. The thermal noise around the even harmonics of  $f_{\text{osc}}$  is filtered out due to the bandwidth of the RRB, as shown in Fig. 10(a),

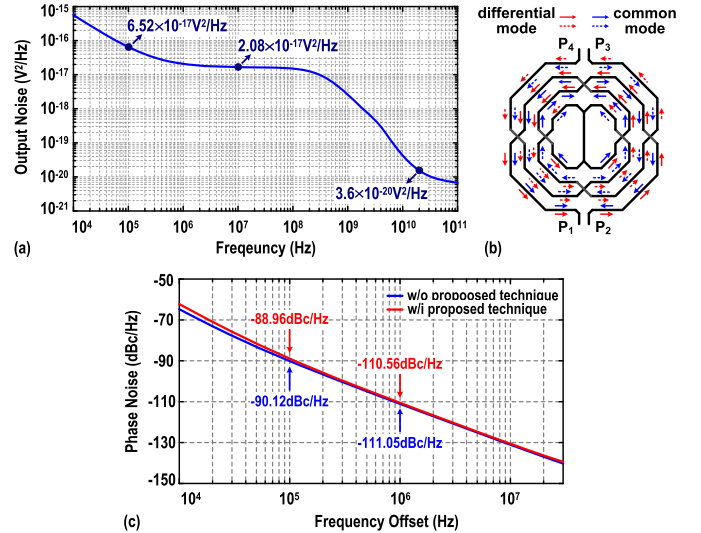


Fig. 10. (a) Output noise of the RRB. (b) Schematic of the symmetrical transformer. (c) Simulated oscillator PN with and without the RRB.

and would not limit the PN performance. For the noise around dc, it is up-conversion into PN is related to the dc component,  $c_0$ , of the impulse sensitivity function (ISF) of the tail current source [36], [37]. To achieve small  $c_0$ , the implicit common-mode resonance technique [38], [39] is employed. Single-ended capacitor banks connected to a symmetrical transformer, as shown in Fig. 10(b), are used to tune the common-mode resonance frequency to around  $2 \times f_{\text{osc}}$ . Hence, the second harmonic component of the oscillation waveform is aligned with the fundamental one, and would not affect the symmetry of the waveform. Therefore,  $c_0$  is kept small and the up-conversion of the low-frequency noise is largely suppressed [36], [40]. Simulation results in Fig. 10(c) show that the PN degradation is only 1.16 dBc at 100-kHz frequency offset. Note that the reported spot noise (as expressed in  $\text{nV}/\sqrt{\text{Hz}}$  unit) of the LDOs in [6] and [7] at 100 kHz is more than  $30\times$  the value shown in Fig. 10(a). Hence, even with the common-mode resonance technique, the oscillator's PN would be greatly degraded when powered by these LDOs.

Both the NMOS and PMOS cross-coupled transistors  $M_{1-4}$  provide the negative transconductance in the complementary structure. The body terminals of the PMOS cross-coupled pair,  $M_{1,2}$ , are deliberately connected to their source terminals to avoid the body effect. Otherwise, their threshold voltage,  $V_{\text{th}}$ , would be modulated under supply variations thus varying the oscillation amplitude  $V_{\text{osc}}$ , consequently pushing  $f_{\text{osc}}$ . Simulation results show that this body effect could limit the supply pushing to no better than 9.5 MHz/V. Note that the above-mentioned NMOS alternative to the tail transistor  $M_0$  would not be effective unless a costly triple-well technology is used.

## IV. MEASUREMENT RESULTS

The *LC* oscillator with the proposed feed-forward ripple replication and cancellation technique is implemented in TSMC 40-nm 1P8M CMOS process without ultra-thick metal layers. The proposed calibration loop is also integrated



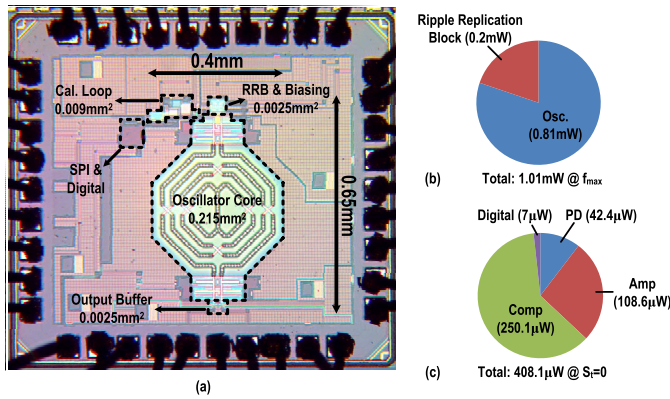


Fig. 11. (a) Chip micrograph of LC oscillator with reduced supply pushing. (b) Measured power breakdown of the oscillator at maximum oscillation frequency during normal operation. (c) Simulated power breakdown of the calibration loop when  $S_t = 0$ .

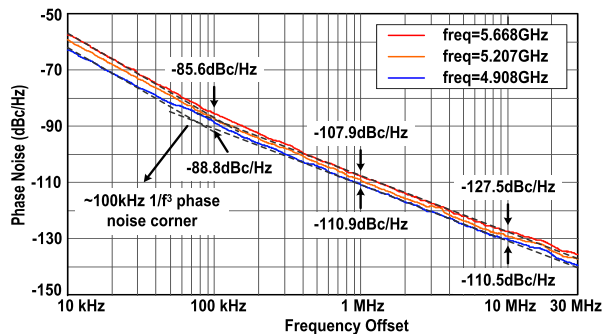


Fig. 12. Measured PN of the oscillator across the TR.

on-die. Fig. 11(a) shows the chip micrograph. The total active area is 0.23 mm<sup>2</sup>, in which the oscillator core occupies about 0.215 mm<sup>2</sup>. The additional area occupied by the RRB with its biasing circuit and the calibration loop is just 0.012 mm<sup>2</sup>, including 8.7-pF capacitance of the calibration loop. To enhance the tank's  $Q$ -factor, the symmetrical transformer is designed by stacking the top two metal layers with the aluminum capping layer. The spacing between each turn of the transformer is optimized for a magnetic coupling factor of 0.31. The simulated differential inductance of the transformer is 1.7 nH.  $Q$ -factor of the whole tank is estimated to be  $\sim 7$ . The capacitor banks are split into a 5-bit differential bank and a 5-bit common-mode bank to tune the common-mode resonance frequency.

The measured power consumption of the oscillator is around 0.81 mW at the maximum oscillation frequency, while the RRB consumes about 0.2 mW, as shown in Fig. 11(b). During calibration, the power consumed by the calibration loop when  $S_t = 0$ , which is the worst case, is around 0.41 mW, and the simulated power breakdown of the loop is also shown in Fig. 11(c).

The measured TR is 4.9–5.7 GHz (15%). Fig. 12 shows the measured PN performance across the TR. PN varies from  $-108$  to  $-111$  dBc/Hz at 1-MHz offset, with a flicker noise corner of around 100 kHz. To verify the concept of the proposed technique, the control code  $S_t$  of the RRB is

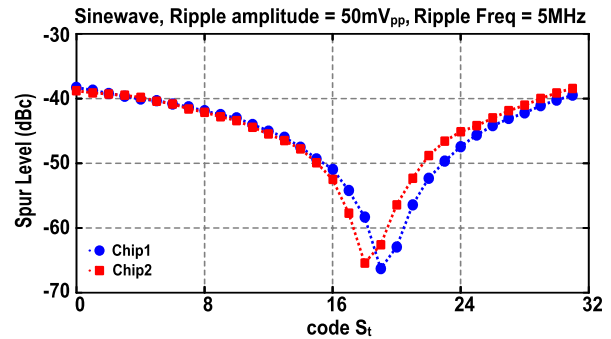


Fig. 13. Measured spur level over the control code  $S_t$ .

manually swept while a 50-mV<sub>pp</sub> 5-MHz sinusoidal ripple is applied on the oscillator supply. As shown in Fig. 13, there exists an optimum code at which the spur level is lower than  $-60$  dBc, corresponding to a  $>27$ -dB improvement over the  $S_t = 0$  case. Note that  $G \approx 1$  when  $S_t = 0$ , and the oscillator already benefits from the significantly reduced supply pushing.

The effectiveness of the automatic calibration loop is verified in Fig. 15 (top), which compares the spectra before and after the calibration. With the supply contamination by a 50-mV<sub>pp</sub> 5-MHz sinusoidal ripple, the spur level is reduced by 30 dBc and reaches  $-68.7$  dBc after the calibration. Fig. 14(a) shows the measured spur level over the frequency of the supply ripple. The proposed technique achieves  $\leq -49$ -dBc optimum spur levels under  $\leq 50$  mV<sub>pp</sub>, 0.5–20-MHz sinusoidal ripples, while the calibrated spur levels closely follow the optimum ones in most cases. In Fig. 14(c), the spur level is measured across the TR of the oscillator. The worst case spur under a 50-mV<sub>pp</sub> 5-MHz sinusoidal ripple is  $\leq 59$  dBc. Fig. 14(b) and (d) displays the oscillator's supply pushing based on the measured spur levels. When the ripple frequency is lower than 12 MHz, the calculated supply pushing is lower than 1 MHz/V for both the optimum and calibrated cases.

Similar measurements are also performed for saw-tooth ripples. Fig. 15 (bottom) compares the spectra before and after the calibration. Under a 50-mV<sub>pp</sub> 5-MHz saw-tooth ripple, the spur at the fundamental offset is reduced by 22.9 dBc and reaches  $-61.7$  dBc after the calibration. For spurs at higher harmonics, the suppression is also observed, but with lower magnitudes (5.8-dBc suppression for the second harmonic reaching  $-59.1$  dBc after the calibration). Fig. 14(e) reports the spur levels over the ripple frequency. The worst case spur of  $-47$  dBc is found under  $\leq 50$  mV<sub>pp</sub>, 0.5–20-MHz saw-tooth ripples, while the calibration results follow the optima. In Fig. 14(f), the spurs are lower than  $-58$  dBc within the entire TR under a 50-mV<sub>pp</sub> 5-MHz saw-tooth ripple.

Fig. 16 (top) shows the measured oscillator spectrum under a 50-mV<sub>pp</sub> 2.5-MHz supply ripple. A spur can also be observed at an offset frequency of 5 MHz (i.e.,  $2 \times 2.5$  MHz). This second ripple harmonic spur mainly comes from the nonlinearity of the fractional part of the RRB. To achieve fine tuning resolution, small transistors with low overdrive voltage are used in the fractional part. Hence, these transistors operate in a moderate or weak inversion region, where the nonlinearity is relatively large. The simulated

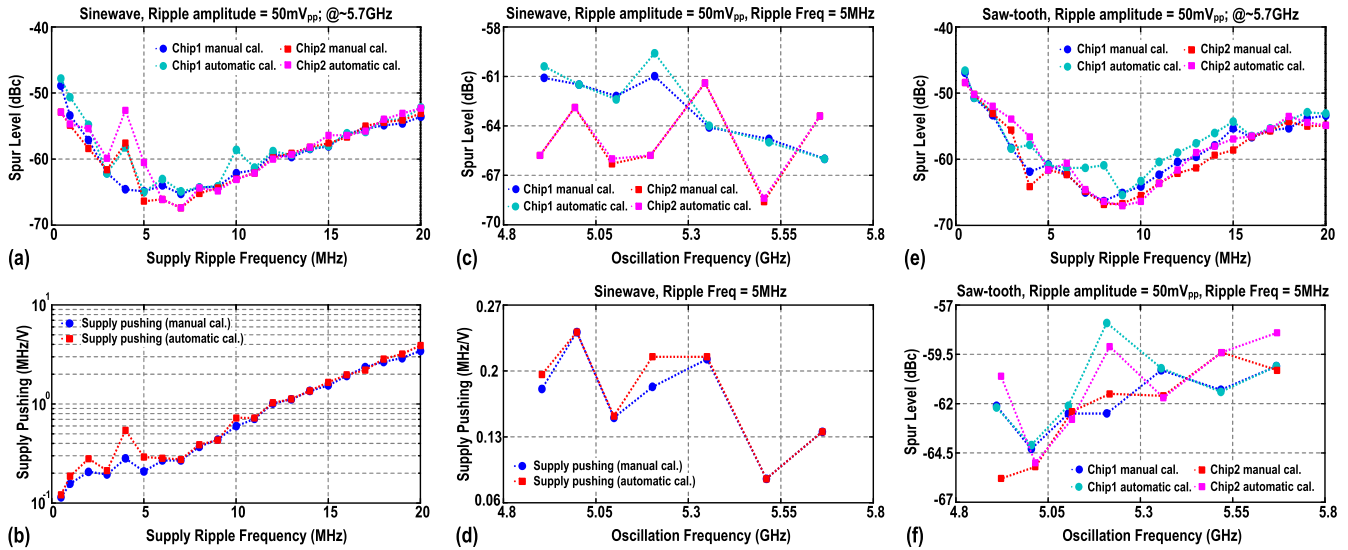


Fig. 14. (a) Measured spur levels over the sinusoidal ripple frequency and (b) corresponding supply pushing for both the manual and automatic calibrations. (c) Measured spur levels over the oscillation frequency under the sinusoidal ripple and (d) corresponding supply pushing for both the manual and automatic calibrations. (e) Measured spur levels over the frequency of the saw-tooth ripple and (f) over the oscillation frequency under the saw-tooth ripple.

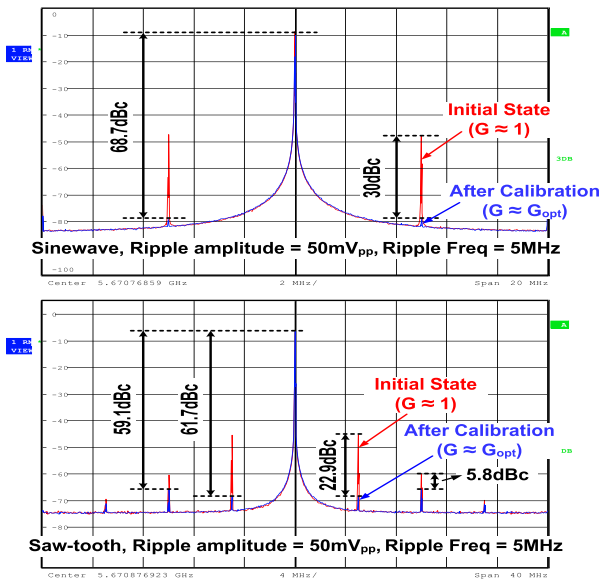


Fig. 15. Measured oscillator spectra before and after automatic calibration under 50 mV<sub>pp</sub> 5-MHz sinusoidal (top) and saw-tooth (bottom) ripple.

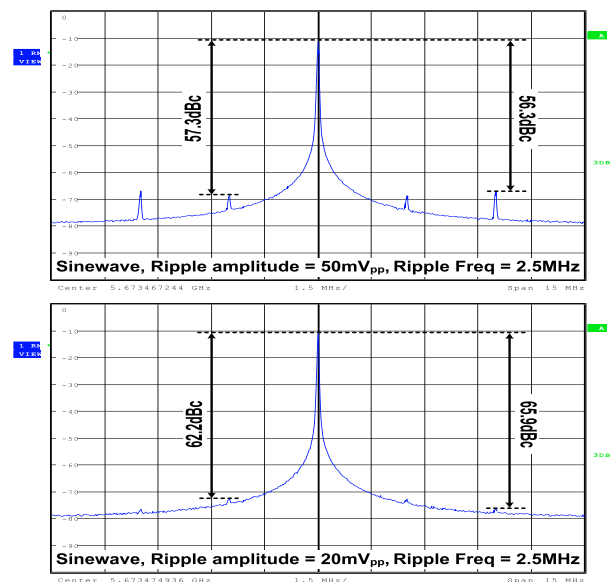


Fig. 16. Measured oscillator spectra under 50 mV<sub>pp</sub> (top) and 20 mV<sub>pp</sub> (bottom) 2.5-MHz sinusoidal ripple.

second harmonic intercept point of these transistors is  $V_{IP2} = 2 \cdot (V_{GS} - V_{TH}) \approx 100$  mV. Consequently, with 50-mV<sub>pp</sub> ripple on supply, which is already comparable to the overdrive voltage of the transistors, relatively large second ripple harmonic spur is generated. To improve the performance at the second ripple harmonic, transistors with a smaller aspect ratio (W/L) and increased overdrive voltage should be used. Simulations show that the spur at  $2 \times f_{ripple}$  is improved by 4.8 dBc when the overdrive voltage of these transistors is increased to 100 mV, while the current penalty is only 3.2  $\mu$ A at  $G_{opt}$ . Also, the spur at the second ripple harmonic falls drastically with a lower ripple amplitude. As shown in Fig. 16, the measured spur level at the second harmonic is reduced to

−65.9 dBc under a 20-mV<sub>pp</sub> ripple, which is a target of our SC converter design, and should bear little practical consequences.

Fig. 17 (top) compares the measured oscillator spectra before and after the automatic calibration when the supply is subjected to a two-tone ripple which consists of 8- and 12-MHz components of equal amplitude. The envelope of the ripple is kept at 50 mV<sub>pp</sub>. The automatic calibration is still effective under this scenario, and the plot shows that the spur at 8/12-MHz offset is reduced by 22.3/20.8 dBc and reach −65.3/−62.4 dBc, respectively, after the calibration. The non-linearity effect not only induces small spurs ( $\leq -64.9$  dBc) at the second harmonics of these two tones but also generates additional spurs at the sum (20 MHz) and difference (4 MHz)

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

		This work	JSSC2017 [38]	ESSCIRC2016 [13]	ISSCC2014 [8]	ISSCC2016 [10]	VLSI2017 [14]	
Description		Feed-forward compensation	$2 \times f_{\text{osc}}$ implicit resonance	FCW compensation	Bias at lowest $K_{\text{push}}$ point	Two constant-Gm biasing	Noise suppression loop	
Osc. Type		LC	LC	LC	Ring	Ring	Ring	
Tech. (nm)		40 (w/o UTM)	28 (w/i UTM)	65	40	40	65	
$V_{\text{DD}}$ (V)		1.0	0.9	1.0	1.1	1.1	1.0	
Frequency Range (GHz)		4.9-5.7 (15%)	2.85-3.75 (27.2%)	3.2-4.8 (40%)	2.418 (NA)	3.2 (NA)	3.2 (NA)	
PN (dBc/Hz) @1MHz		-107.9 to -110.9	-127.5 to -131	-108* @ 3.57GHz	NA	NA	-88*	
Ripple Amplitude		50mV <sub>pp</sub>	NA	NA	1mV <sub>pp</sub>	50mV <sub>pp</sub>	20mV <sub>pp</sub>	
Sinewave	Spur (dBc)	@1MHz	<-54	NA	NA	-45	-25	-57
		@5MHz	<-58	NA	NA	-49	NA	-48
	$K_{\text{push}}$ (MHz/V)	@1MHz	<0.16 <sup>†</sup>	6-30	NA	22.5 <sup>†</sup>	45 <sup>***</sup>	0.63 <sup>***</sup>
		@5MHz	<0.5 <sup>†</sup>	6-30	NA	70.9 <sup>†</sup>	NA	4 <sup>†</sup>
Improv. (dBc)	@1MHz	18-24 <sup>†</sup>	NA	NA	28	10	30	
	@5MHz	24-30 <sup>†</sup>	NA	NA	19	NA	30	
Saw-tooth	Spur (dBc)	@1MHz	<-50	NA	-50	NA	NA	NA
		@5MHz	<-58	NA	-51	NA	NA	NA
	Improv. (dBc)	@1MHz	11.3 <sup>†</sup>	NA	15	NA	NA	NA
		@5MHz	22-27 <sup>†</sup>	NA	12	NA	NA	NA
Osc. Power Cons. (mW)		0.8-1.3	6.6	18.9 <sup>†</sup>	6.4 <sup>†</sup>	2.95 <sup>†</sup>	2.73 <sup>†</sup>	
Power Cons. $K_{\text{push}}$ Reduction Tech. (mW)		0.2	NA	2.4	NA	NA	0.45	
Area of $K_{\text{push}}$ Reduction Tech. (mm <sup>2</sup> )		0.012	NA	0.35 <sup>†</sup>	NA	NA	0.004	
Total Area (mm <sup>2</sup> )		0.23	0.15	0.63 <sup>†</sup>	0.013 <sup>†</sup>	0.0216 <sup>†</sup>	0.047 <sup>†</sup>	

\*Estimated from out-of-band phase noise of PLL \*\*Compared with the case  $S_1=0$  (Gain=1) where the supply pushing of the oscillator is already suppressed

#Calculated value from the spur level

† Power/area of the ADPLL

‡ Estimate from the chip micrograph

\*\*\*Ripple frequency lower than the PLL bandwidth, supply pushing is calculated assuming 20dBc/decade suppression from the loop

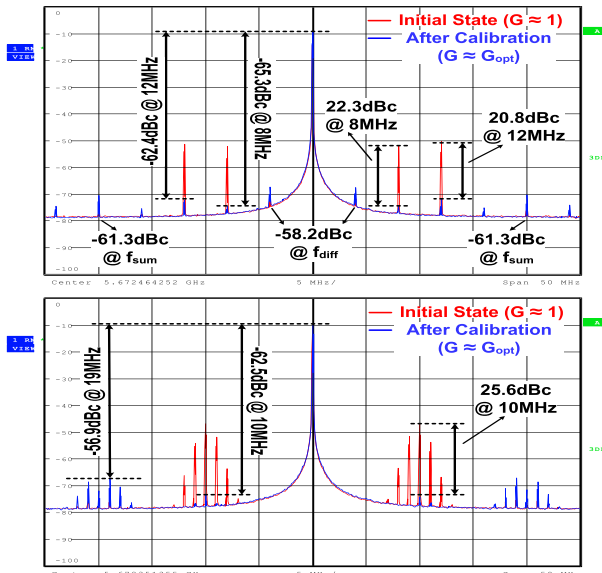


Fig. 17. Measured oscillator spectra before and after automatic calibration under two-tone (top) and frequency modulated (bottom) ripple.

frequencies of these two tones with a level of  $-61.3$  dBc and  $-58.2$  dBc, respectively, which are still far below the  $-50$ -dBc limitation of the IoT applications. Fig. 17 (bottom) compares the measured spectra before and after the automatic calibration when a  $50$ -mV<sub>pp</sub>  $10$ -MHz frequency modulated (FM) ripple is applied to the supply. The modulation rate and maximum frequency deviation are both  $1$  MHz to clearly show the effect of modulation. The plot shows that the spurs around  $10$  MHz are reduced to  $\leq -62.5$  dBc after the calibration, corresponding to a  $25.6$ -dBc reduction at  $10$  MHz, while the spurs induced by nonlinearity around  $20$  MHz are  $\leq -56.9$  dBc.

Fig. 18 shows the measured spur levels under a  $50$ -mV<sub>pp</sub>  $5$ -MHz sinusoidal ripple at different dc supply voltages and

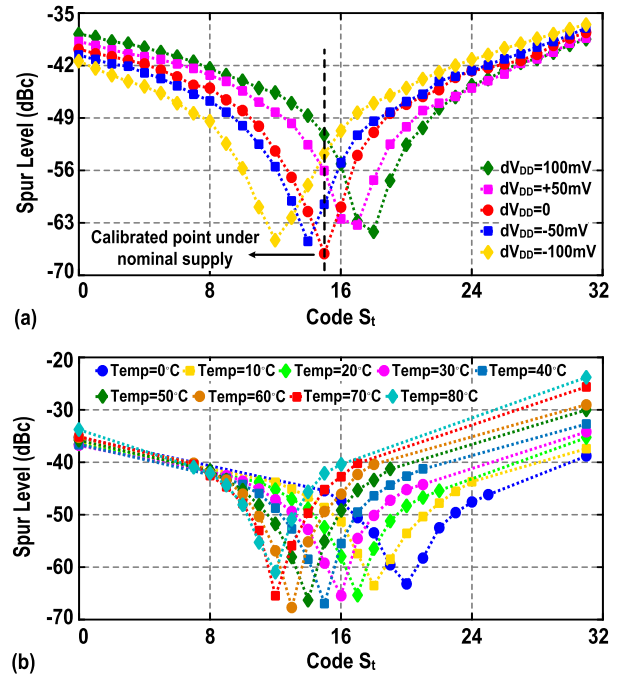


Fig. 18. Measured spur levels over the control code  $S_1$  under different (a) dc supply voltages and (b) temperatures.

temperatures. For the variation of the dc supply voltage, the optimal code varies by  $\sim \pm 3$  under  $\pm 100$ -mV variation, and the spur level remains  $< -50$  dBc without any re-calibrations. Due to a relatively low power consumption of the IoT system, the on-chip temperature variation is very slow [41]. As shown in Fig. 18(b), the optimal code only changes by  $\sim \pm 1$  under  $\pm 10$  °C variation. Hence, the effect of temperature drift is slow enough to be compensated by intermittent re-calibrations.

TABLE II  
COMPARISON WITH LDO DESIGNS

	This work	JSSC'10 [22]	CICC'11 [24]	JSSC'14 [6]	VLSI'17 [7]	JSSC'18 [42]
Tech. (nm)	40	130	180	180	40	65
V <sub>in</sub> (LDO)/ V <sub>DD</sub> (osc.) (V)	1.0	>1.15	1.8	1.8	1.1	1.2
V <sub>out</sub> (LDO) (V)	NA	1	1.5	1.6	1	1
V <sub>drop-out</sub> (LDO)/ V <sub>ds</sub> of M <sub>0</sub> (osc.) (V)	0.25	>0.15	0.3	0.2	0.1	0.2
PSR @1MHz (dBc)	<-55.9	-80	-50	-65	-60	-52
@10MHz	<-42.5	-60	-22	-42	-35	-37
Total Capacitance	8.6pF (on-chip)	4μF (off-chip)	125pF (on-chip)	128pF (on-chip)	104pF (on-chip)	260pF (on-chip)
Additional Current Consumption (mA)	0.2 +0.021#	0.05	0.3	0.08	0.275	0.1535
Additional Power Consumption (mW)	0.2 +0.021#	0.0575	0.54	0.144	0.3025	0.1842
Noise (LDO/RRB) @100kHz (nV/√Hz)	8"	NA	NA	270	274	NA
Total Area (mm <sup>2</sup> )	0.012	0.049	0.041	0.14'	0.008'	0.087

\*100pF on-chip load capacitance not included \*\*Value obtained from post-layout simulation  
#0.2mA(mW) from RRB always exists during normal operation; 0.021mA(mW) is the average power consumption of the calibration loop, when conservatively assuming a calibration is done for every BLE packet (~400μs)

Table I summarizes the performance of the proposed technique and compares it to prior works. When compared to a state-of-the-art LC oscillator in [38], the proposed technique demonstrates >10× improvement of the supply pushing. In comparison with other supply pushing reduction techniques [8], [10], [13], [14], the proposed technique shows the lowest supply pushing, comparable or larger spur reduction, while the additional power is small. The proposed technique is also compared with state-of-the-art LDO designs in Table II. Though [22] achieves higher PSR with a lower power consumption, a large off-chip capacitor is used which is against the IoT miniaturization. Also, it lacks a reliable calibration which could lead to ~20-dB PSR variation under process and temperature changes. In [24], a correlation-based calibration scheme is implemented, but non-ideal effects, such as an offset of the mixer lead to incorrect calibration results. Moreover, compared with other state-of-the-art LDOs with on-chip capacitors [6], [7], [24], [42], our work demonstrates one of the highest PSR at 10 MHz with less or comparable (extra) power. The total on-chip capacitance used in the proposed design is also the lowest, thus occupying the smallest area.

## V. CONCLUSION

This paper presented a method to significantly reduce supply pushing in current-mode LC oscillators while consuming no extra voltage headroom. The proposed RRB generates an amplified supply ripple replica at the gate terminal of the oscillator's tail current source, in order to stabilize the tail current and oscillation amplitude under supply variations. The oscillation frequency is stabilized in turn, leading to <1-MHz/V supply pushing for supply ripples up to 12 MHz. To suppress the PN degradation due to the extra circuitry, implicit common-mode resonance is used in the resonant tank. A calibration loop with a simple and effective algorithm is also integrated on-chip, which effectively finds the optimum gain for the RRB. The operation of the loop is based on detecting and minimizing the variation of the oscillation amplitude.

Hence, it is also effective when the ripple is simultaneously coupled through the supply and other parasitic paths.

## ACKNOWLEDGMENT

The authors would like to thank Y. Wu, M. Mehrpoo, A. Akhnoukh, J. Gong, and B. Patra, all from the Delft University of Technology, for technical discussions and assistance.

## REFERENCES

- [1] J. Prummel *et al.*, "A 10 mW Bluetooth low-energy transceiver with on-chip matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.
- [2] L. Fanori, T. Mattsson, and P. Andreani, "A class-D CMOS DCO with an on-chip LDO," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 335–338.
- [3] H. Yoon *et al.*, "A 0.56–2.92 GHz wideband and low phase noise quadrature LO-generator using a single LC-VCO for 2G–4G multistandard cellular transceivers," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 614–625, Mar. 2016.
- [4] A. Arakali, S. Gondi, and P. K. Hanumolu, "Analysis and design techniques for supply-noise mitigation in phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 11, pp. 2880–2889, Nov. 2010.
- [5] E. Alon, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, "Replica compensated linear regulators for supply-regulated phase-locked loops," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 413–424, Feb. 2006.
- [6] Y.-C. Huang, C.-F. Liang, H.-S. Huang, and P.-Y. Wang, "A 2.4 GHz ADPLL with digital-regulated supply-noise-insensitive and temperature-self-compensated ring DCO," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 270–271.
- [7] J. Liu *et al.*, "A 0.012 mm<sup>2</sup> 3.1 mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 268–269.
- [8] C.-W. Yeh, C.-E. Hsieh, and S.-I. Liu, "A 3.2 GHz digital phase-locked loop with background supply-noise cancellation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 332–333.
- [9] K.-Y. J. Shen *et al.*, "A 0.17-to-3.5 mW 0.15-to-5 GHz SoC PLL with 15 dB built-in supply noise rejection and self-bandwidth control in 14 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 330–331.
- [10] T. Wu, K. Mayaram, and U.-K. Moon, "An on-chip calibration technique for reducing supply voltage sensitivity in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 775–783, Apr. 2007.
- [11] C.-R. Ho and M. S.-W. Chen, "Interference-induced DCO spur mitigation for digital phase locked loop in 65-nm CMOS," in *Proc. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2016, pp. 213–216.
- [12] D. Kim and S. Cho, "A supply noise insensitive PLL with a rail-to-rail swing ring oscillator and a wideband noise suppression loop," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C180–C181.
- [13] S. S. Nagam and P. R. Kinget, "A –236.3dB FoM sub-sampling low-jitter supply-robust ring-oscillator PLL for clocking applications with feed-forward noise-cancellation," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr./May 2017, pp. 1–4.
- [14] A. Elshazly, R. Inti, W. Yin, B. Young, and P. K. Hanumolu, "A 0.4-to-3 GHz digital PLL with PVT insensitive supply noise cancellation using deterministic background calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2759–2771, Dec. 2011.
- [15] B. Soltanian and P. Kinget, "AM-FM conversion by the active devices in MOS LC-VCOs and its effect on the optimal amplitude," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, Jun. 2006, pp. 103–108.
- [16] E. Hegazi and A. A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.

- [19] A. Zanchi, C. Samori, S. Levantino, and A. L. Lacaita, "A 2-V 2.5-GHz-104-dBc/Hz at 100 kHz fully integrated VCO with wide-band low-noise automatic amplitude control loop," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 611–619, Apr. 2001.
- [20] D. Miyashita *et al.*, "A phase noise minimization of CMOS VCOs over wide tuning range and large PVT variations," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2005, pp. 583–586.
- [21] J. W. M. Rogers, D. Rahn, and C. Plett, "A study of digital and analog automatic-amplitude control circuitry for voltage-controlled oscillators," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 352–356, Feb. 2003.
- [22] M. El-Nozahy, A. Amer, J. Torres, K. Entesari, and E. Sánchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010.
- [23] E. N. Y. Ho and P. K. T. Mok, "Wide-loading-range fully integrated LDR with a power-supply ripple injection filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 6, pp. 356–360, Jun. 2012.
- [24] B. Yang, B. Drost, S. Rao, and P. K. Hanumolu, "A high-PSR LDO using a feedforward supply-noise cancellation technique," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2011, pp. 1–4.
- [25] L. Fanori and P. Andreani, "Highly efficient Class-C CMOS VCOs, including a comparison with Class-B VCOs," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, Jul. 2013.
- [26] C. Zheng and D. Ma, "A 10-MHz green-mode automatic reconfigurable switching converter for DVS-enabled VLSI systems," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1464–1477, Jun. 2011.
- [27] O. Trescases, A. Prodic, and W. T. Ng, "Digitally controlled current-mode DC–DC converter IC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 219–231, Jan. 2011.
- [28] M. Du, H. Lee, and J. Liu, "A 5-MHz 91% peak-power-efficiency buck regulator with auto-selectable peak- and valley-current control," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1928–1939, Aug. 2011.
- [29] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 374–375.
- [30] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1749–1760, Aug. 2011.
- [31] J. Yi, W. H. Ki, and C. Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.
- [32] M. Loikkanen and J. Rostamovaara, "PSRR improvement technique for amplifiers with Miller capacitor," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2006, pp. 1393–1397.
- [33] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.
- [34] A. Bevilacqua and P. Andreani, "An Analysis of  $1/f$  noise to phase noise conversion in CMOS harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 938–945, May 2012.
- [35] E. E. Hegazi, J. Rael, and A. A. Abidi, *The Designer's Guide to High-Purity Oscillators*, 1st ed. New York, NY, USA: Springer, 2004.
- [36] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [37] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
- [38] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, Mar. 2017.
- [39] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A  $1/f$  noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov. 2016.
- [40] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.
- [41] B. Yousefzadeh and K. A. A. Makinwa, "A BJT-based temperature sensor with a packaging-robust inaccuracy of  $\pm 0.3$  °C (3s) from  $-55$  °C to  $+125$  °C after heater-assisted voltage calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 162–163.
- [42] Y. Lim, J. Lee, S. Park, Y. Jo, and J. Choi, "An external capacitorless low-dropout regulator with high PSR at all frequencies from 10 kHz to 1 GHz using an adaptive supply-ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2675–2685, Sep. 2018.



**Yue Chen** (S'18) received the B.Eng. degree in microelectronics and the M.Eng. degree in electronic science and technology from Xian Jiaotong University, Xian, China, in 2011 and 2014, respectively. He is currently pursuing the Ph.D. degree in electronic engineering with the Microelectronics Department, Delft University of Technology, Delft, The Netherlands.

His current research interests include frequency synthesizer techniques and integrated circuits for wireless communications.



**Yao-Hong Liu** (S'04–M'09–SM'17) received the Ph.D. degree from National Taiwan University, Taipei, Taiwan, in 2009.

From 2002 to 2010, he was with Terax, Hsinchu, Taiwan, Via Telecom (now Intel), Taipei, and Mobile Devices, Hsinchu, where he was working on various cellular and WiFi SoC products. Since 2010, he has been with imec-nl, Holst Center, Eindhoven, The Netherlands. He is a Principal Membership of Technical Staff with imec-nl, and he is leading the development of the ultralow power (ULP) RFIC design. His current research interests include energy-efficient wireless transceivers and RF sensing for IoT.

Dr. Liu serves as a Technical Program Committee for the IEEE ISSCC and RFIC Symposium.



**Zhirui Zong** (S'12) received the B.Eng. degree (Hons.) in electronic and information engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2012. He is currently pursuing the Ph.D. degree in electrical engineering with the Delft University of Technology, Delft, The Netherlands, with a focus on high-performance phase-locked loops for mm-wave applications.

Since 2018, he has been a Senior RFIC Designer with NXP Semiconductors, Eindhoven, The Netherlands. His current research interests include frequency synthesizer techniques and integrated circuits for wireless communications and mm-wave radars.



**Johan Dijkhuis** (M'10) received the M.S. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1998.

Since 1998, he has been a RF and an Analog Design Engineer with Philips Semiconductor, NXP, Nijmegen, The Netherlands, ST-Ericsson, Nijmegen, and NVIDIA, Nijmegen. Since 2014, he has been with imec-nl, Holst Center, Eindhoven, The Netherlands. His current research interests include RF circuit design and power management circuits for ultralow-power radios.



**Guido Dolmans** received the M.Sc. and Ph.D. degrees in electrical engineering from the Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, in 1992 and 1997, respectively.

From 1997 to 2006, he was a Senior Scientist with Philips Research. Since 2006, he has been a Scientific Director and an R&D Manager with imec-nl, Holst Centre, Eindhoven. In 2014, he joined TU/e, as a Full Professor. He has co-authored over 100 papers in scientific/technical journals and proceedings. He holds 14 U.S. patents. His current

research interests include wireless systems, localization and radar solutions, and new developments such as data analytics and artificial intelligence.



**Robert Bogdan Staszewski** (M'97–SM'05–F'09) was born in Bialystok, Poland. He received the B.Sc. (*summa cum laude*), M.Sc., and Ph.D. degrees in electrical engineering from The University of Texas at Dallas, Richardson, TX, USA, in 1991, 1992, and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, TX, USA, where he was involved in SONET cross-connect systems for fiber optics communications. In 1995, he joined Texas Instruments Incorporated, Dallas, TX, USA, where

he was elected Distinguished Member of Technical Staff (limited to 2% of technical staff). From 1995 to 1999, he was engaged in advanced CMOS read channel development for hard disk drives. In 1999, he co-started the Digital RF Processor (DRP) Group, Texas Instruments with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS technology. From 2007 to 2009, he was appointed as a CTO with the DRP Group, Texas Instruments. In 2009, he joined the Delft University of Technology, Delft, The Netherlands, where he currently holds a guest appointment of Antoni van Leeuwenhoek Hoogleraar Full Professor. Since 2014, he has been a Full Professor with the University College Dublin (UCD), Dublin, Ireland. He has authored or co-authored 4 books, 5 book chapters, 230 journal and conference publications. He holds 170 issued U.S. patents. His current research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers.

Dr. Staszewski has been a TPC member of ISSCC, RFIC, ESSCIRC, ISCAS, and RFIT. He is a TPC Chair of 2019 ESSCIRC in Krakow, Poland. He was a recipient of the 2012 IEEE Circuits and Systems Industrial Pioneer Award.



**Masoud Babaie** (S'12–M'16) received the B.Sc. degree (Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, and the Ph.D. degree (*cum laude*) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2004, 2006, and 2016, respectively.

In 2006, he joined the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication systems. From

2009 to 2011, he was a CTO of that company. From 2013 to 2015, he was consulting for the RF Group of Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, where he was involved in designing 28-nm all-digital phase-locked loop and Bluetooth low energy (BLE) transceiver chips. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA, with the Group of Prof. A. Niknejad. In 2016, he joined the Delft University of Technology, Delft, The Netherlands, as an Assistant Professor. His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications, and cryogenic electronics for quantum computation.

Dr. Babaie has been a Committee Member of Student Research Preview (SRP) of the IEEE International Solid-State Circuits Conference (ISSCC), since 2017. He was a recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award.