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Output blue light evaluation for phosphor based smart white LED wafer level packages

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Abstract: This study presents a blue light detector for evaluating the output light of phosphor based white LED package. It is composed of a silicon stripe-shaped photodiode designed and implemented in a 2 μm BiCMOS process which can be used for wafer level integration of different passive and active devices all in just 5 lithography steps. The final device shows a high selectivity to blue light. The maximum responsivity at 480nm is matched with the target blue LED illumination. The designed structure have better responsivity compared to simple photodiode structure due to reducing the effect of dead layer formation close to the surface because of implantation. It has also a two-fold increase in the responsivity and quantum efficiency compared to previously similar published sensors.

References and links

1. S. Chhajed, Y. Xi, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Influence of junction temperature on chromaticity and color-rendering properties of trichromatic white-light sources based on light-emitting diodes," J. Appl. Phys. **97**(5), 054506 (2005).
2. Y.-C. Lin, J. P. You, N. T. Tran, Y. He, and F. G. Shi, "Packaging of phosphor based high power white LEDs: effects of phosphor concentration and packaging configuration," J. Electron. Packag. **133**(1), 011009 (2011).
3. J. Lau, R. Lee, M. Yuen, and P. Chan, "3D LED and IC wafer level packaging," Microelectron. Int. **27**(2), 98–105 (2010).
4. E. T. A. P. Lighting, "LED lifetime in practice - The ETAP approach" [Online]. Available: http://www.etaplighting.com/uploadedFiles/Downloadable_documentation/documentatie/whitepaper_LED_EN.pdf.
5. R. Zhang, S. W. R. Lee, D. G. Xiao, and H. Chen, "LED packaging using silicon substrate with cavities for phosphor printing and copper-filled TSVs for 3D Interconnection," in *Proceedings of IEEE Conference on Electronic Components and Technology* (IEEE, 2011), pp. 1616–1621.
6. C. T. Tsou and Y.-S. Huang, "Silicon-based packaging platform for light-emitting diode," IEEE Trans. Adv. Packag. **29**(3), 607–614 (2006).
7. J. K. Kim and H. C. Lee, "A photo-sensor on thin polysilicon membrane embedded in wafer level package LED," Proc. SPIE **8431**, 8431–8437 (2012).
8. G. Corporation, "A Silicon ultraviolet detector," Sens. Actuators **23**, 553–558 (1990).
9. N. Kako, N. Tanaka, and C. Suzuki, "Combustion detection with a semiconductor color sensor," Sens. Actuators **4**, 655–660 (1983).
10. A. Pauchard, P. Besse, and R. S. Popovic, "A silicon blue/UV selective stripe-shaped photodiode," Sens. Actuators **76**(1-3), 172–177 (1999).
11. M. Zhang, H. Zhang, K. Lv, W. Chen, J. Zhou, L. Shen, and S. Ruan, "Ultraviolet photodetector with high internal gain enhanced by $TiO_2/SrTiO_3$ heterojunction," Opt. Express **20**(6), 5936–5941 (2012).
12. J. W. Levell, M. E. Giardini, and I. D. W. Samuel, "A hybrid organic semiconductor/silicon photodiode for efficient ultraviolet photodetection," Opt. Express **18**(4), 3219–3225 (2010).
13. J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology Fundamentals, Practice and Modeling* (Prentice Hal, 2000).
14. Z. Kolahdouz Esfahani, A. Rostamian, M. Kolahdouz, T. Ma, H. Van Zeijl, and G. Q. Zhang, "Blue selective photodiodes for optical feedback in LED wafer level packages," in *Proceedings of IEEE Conference on Solid State Device Research-ESSDERC* (IEEE, 2014), pp. 174–177.

15. N. S. Lawand, H. van Zeijl, P. J. French, J. J. Briaire, and J. H. M. Frijns, "Titanium nitride (TiN) as a gate material in BiCMOS devices for biomedical implants," in *Proceedings of IEEE Conference on Sensors* (IEEE, 2013), pp. 1–4.

1. Introduction

There are two major methods to produce white light in LED lighting systems. The first approach is to create white light by the proper mixture of three monochromatic sources, i.e. red, green and blue light (RGB method). These trichromatic LED-based white light sources provide a good control over the light color temperature and luminous efficiency of radiation. However, this method is hardware intensive due to application of three RGB LEDs. Furthermore, these chips show different behaviors at high working temperature conditions and aging characteristics. The system also tends to render pastel colors unnaturally which results in poor color rendering index of RGB white light. Besides, the driving electric circuit for this method is complex to be used for white color production and makes it impractical for general illumination applications [1, 2].

The second approach, entitled the phosphor based white method, is to produce white light by a single short wavelength LED such as blue or UV, combined with a yellow phosphor coating. The blue or UV photons generated in the LED either travels through the phosphor layer without shift, or they are converted into yellow photons in the phosphor coating layer. The combination of the yellow light with the unabsorbed blue light appears as a white light in the human eyes. In some modules, remote phosphor layer is used in which phosphor is placed at a sufficiently large distance from the LED chip. It offers much better color rendering than RGB white, often similar to the fluorescent sources. Furthermore, phosphor converted white light is also much more efficient than RGB white. Because of its high efficiency and acceptable color rendering and lifetime, phosphor white is the most common approach of producing white light for general illumination [2, 3].

The exact shade or color temperature of dichromatic white light is determined by the dominant wavelength of the blue LED and the composition and thickness of phosphor coating. Manufacturers attempt to minimize the color variations by controlling the thickness and composition of the phosphor layer during manufacturing [2].

Despite all advantages these LEDs have, they are suffering from light intensity decay in stress tests. Their light intensity decays during a long operation time or at a high working temperature. Another drawback of phosphor based white method is color shifting due to degradation of the blue LED die and the yellow phosphor over time. It also happens when the device operates at a different current or operating temperature [1].

Some of the manufacturing companies have revealed the data for lifetime prediction of LED chips. As is shown in Fig. 1 from ETAP company [4], the LED performance decays critically over the time which motivates us to develop a system monitoring unit. Although not all the performance falloffs can be compensated, a smart integrated LED power control with light and temperature sensors can compensate for light intensity decay, monitor color shifting and protect for overtemperture problems.

Decay may refer both to phosphor and LED chip performance over the time. While phosphor working mechanism is related to the manufacturing process, we can compensate LED aging and adjust its light intensity by changing the driving current. There are two strategies to alter the current:

1- Feed a forward control based on the lifetime prediction: Increasing current based on the correction values stored in a memory.
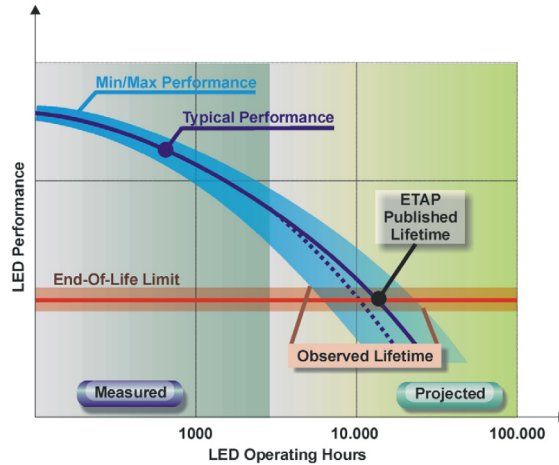
Fig. 1. LED performance report over operating hours from ETAP company [4].

2- Using output light feedback: Including blue light sensors and a control loop circuit.

A smart package with an output light feedback can compensate the brightness variation by changing the driving current. Light sensing can provide information both about light color and intensity. Employing a blue selective photodiode integrated in LED package can be a promising solution.

Silicon based wafer level packaging (WLP) is the technology of choice for broad range of applications. This technology is a key in terms of cost and thermal design. It can provide batch fabrication and component integration, as it is compatible with CMOS technology and thus, can include micro electromechanical systems (MEMS) components as well [5, 6]. Applying these technologies, a smart LED package can be produced that resolves the brightness problems associated with LED intensity decay [7]. There are two categories of silicon-wafer-based wafer level packaging (WLP) LEDs; the surface-mount type, in which electrodes are formed on a silicon wafer and then the LED chip is attached to the wafer; and the cavity type, in which cavities are formed prior to the electrodes [7]. Generally, the cavity is fabricated using KOH wet etching with a (100) silicon wafer. The cavity acts both as a reflector and a holder for filling phosphor and resin.

In this study, we developed a photo sensor appropriate for the target wavelength (470nm) and compatible to the cavity type WLP process and monolithic integration. Basic Silicon photo detectors generally have a poor responsivity to blue and UV light, because these spectra absorbs very close to the surface while the active sensing regions of these devices are usually situated at a certain depth below the device surface [8]. Different structures for silicon photodiodes are used to tune wavelength selectivity . They are all based on wavelength-dependent absorption coefficient of light in silicon. The basic structure is a p-n-p dual-junction photodiode, the active region of the p–n photodiode is limited by a second n–p junction situated below the first one [9]. In this report, the detector doping profile of the photodiode is adjusted in a way to have a sharp and high potential barrier [8], which generates a strong built-in drift field in which photo-generated carriers are separated efficiently. This structure is intrinsically selective but fabricated in a dedicated sensor process, not compatible with CMOS standard processing. Another group proposed a stripe shaped photodiode, compromising shallow P layers implanted in a N-well [10]. The geometry was optimized for better UV/blue responsivity. These devices showed a promising selectivity for blue light. In our work, we used similar structure as in [10],but the size and features were changed to better fit the process and application requirements. All structures are also simulated and the efficiencies of the devices have been thoroughly investigated before fabrication.

There are also some reports on novel works using different substrates or coating to enhance the responsivity to UV and blue spectra . In [11], TiO2 nano-crystalline film was

prepared on SrTiO3 (001) substrate to form an n-n heterojunction active layer and final device shows a good responsivity in UV region. In another work [12] by employing conjugated polymer thin film blends, authors showed improving the ultraviolet response of silicon photodetectors for UV spectra. However these methods are not applicable in standard BiCMOS process.

The photodiode is fabricated in a 5 mask BiCMOS process, used in a LED WLP which can selectively detect the output blue light intensity in a very accurate and efficient way which provides the brightness information of a mounted LED in a package.

2. Photodiode structure

In order to determine the best location to detect the blue light in silicon, light interaction in Si was simulated using COMSOL Multiphysics. To check all physical aspects of the investigation, electromagnetic waves (Frequency domain) and semiconductor physic interfaces were coupled. The light illumination was simulated by solving the Helmholtz equations. This was achieved by analysing the electromagnetic waves when it enters the device. The Fresnel equations were also employed to take multiple reflections of the propagating electromagnetic wave at each interface into account. The transverse mode of electromagnetic wave, which is a particular electromagnetic field pattern measured in a plane perpendicular to the propagation direction of the beam, was applied to solve the mentioned equations. The solution to these equations is the electric field which is needed for calculating the generation term. This electric field was used to calculate the Poynting vector, and hence the optical power. Finally, the generation term, which will be added to the final continuity equation, would be derived from the optical power as shown below:

$$G = -\frac{\partial P_{op}}{\partial y} \times \frac{1}{hf} \tag{1}$$

where h, f, y and P_{op} are respectively Plank's constant, frequency of the incident beam, depth and optical power. As the simulation results demonstrated, blue light ray optical power (470nm) decays dramatically as it enters the silicon [Fig. 2].

In the second photodiode just a single anode but with very large area is used [see Fig. 3(b)]. In this device, the anode geometry is simply a shallow P^+-doped region with a width as long as sum of width all stripes (W) and the distances between them (D). The doping profiles for the N^+, N^--well contact and P^+ substrate contact are the same as the multi-stripe shaped structure, but the anode is a wide P^+ region.

As illustrated in Fig. 2, because the blue and UV spectrum is basically absorbed just beneath the surface, the dead layer formation due to high dose ion implantation decreases the responsivity significantly [13]. Due to a large number of defects in this region, electron-hole generated by target photons can recombine in the dead layer which is not desired and limit the sensitivity. This also creates an electric field which drifts more carriers towards the surface. Thus, by making multi-stripe shaped junction, we can minimize this problem. In this case there is shorter path for carriers to reach to the junction. Therefore, the dead layer in multi-striped structure in comparison to single anode structure is down scaled by W/(W + D) [10], which will improve the blue spectra responsivity. On the other hand, the effective depletion region area for photon absorption and carrier generation will increase in the multi-stripe shaped structure. This occurs due to the sides of the junctions in each P^+ region which are located very close to the surface.

Although decreasing the junction length by converting single to multi shaped structure results in reduced photon absorption but on the other hand the dead layer recombination sites are decreased as well [10, 14].

For the multi-stripe shaped structure, the width of the stripes is 3μm and the distance between two adjacent stripes is 5μm. The stripes' length is 235 μm. According to these dimensions the shallow P-doped region for the single anode geometry is 35μm.
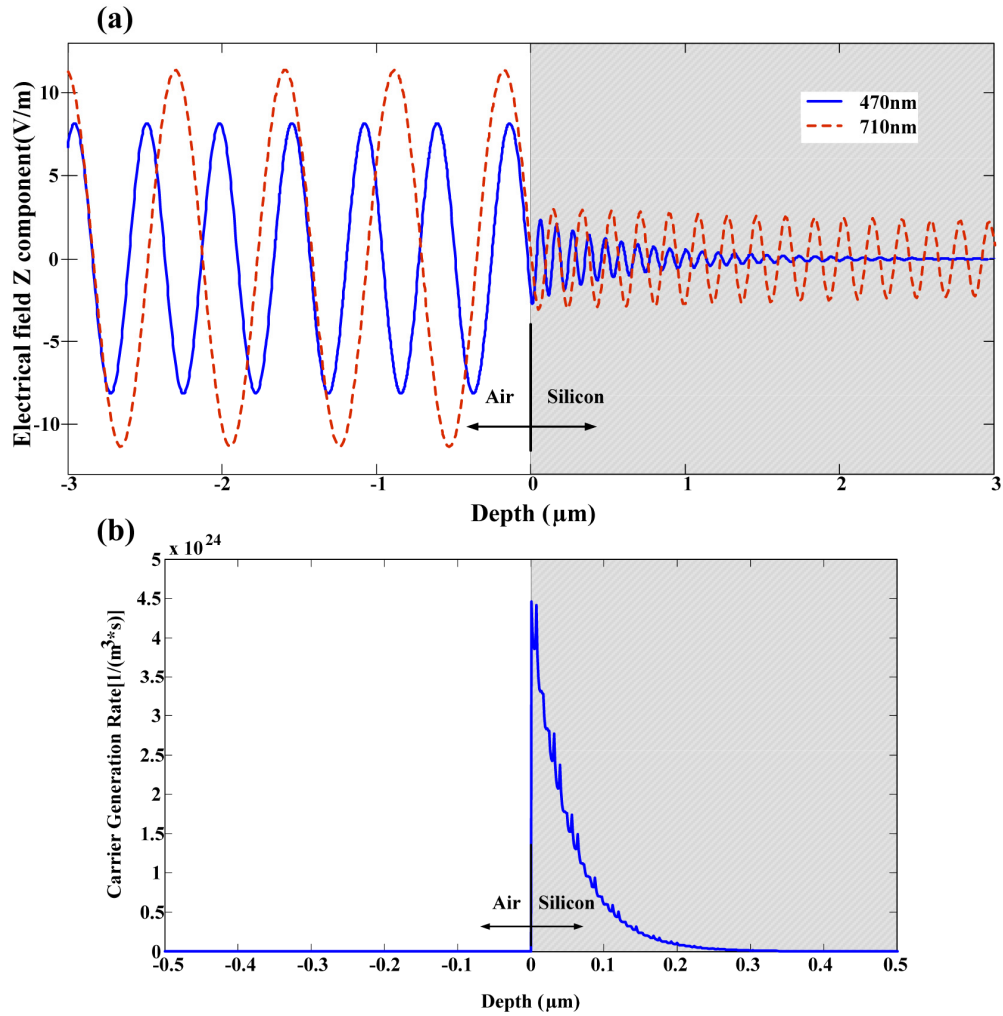
(a)

(b)

Fig. 2. (a) Electrical field for 470 and 710 nm; and (b) carrier generation rate as a function of depth for 470nm light in silicon interface. Si interface is occurring at 0μm for these plots.
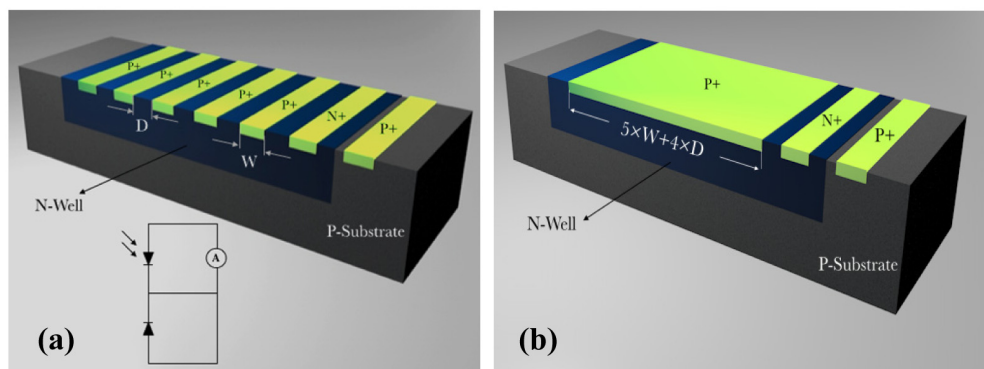

(a)

(b)

Fig. 3. Schematic of (a) a multi-stripe and (b) single anode photodiode and the equivalent circuit.

3. Simulation and discussion

Due to a large amount of surface defect generated during the doping process, Shockley-Read-Hall (SRH) recombination with a very high rate occurs at the surface which creates an electric field toward the substrate. The dead layer formation can be observed in electron concentration profile extracted from simulation as shown in Fig. 4.

As discussed earlier, in order to improve selectivity and responsivity to blue rays, the active junction should be located in the top 300 nm inside the substrates. As shown in Fig. 5, the junction depletion region, where generation occurs, happens mostly inside the n-well region and extends for about 150 nm. According to reports [13], a high level doping in ion implantation and boron redistribution during the annealing process, will cause dopant pileup in an interfacial layer between the top SiO_2 layer and Si. This layer acts as a sink for inactive dopant atoms in this region.
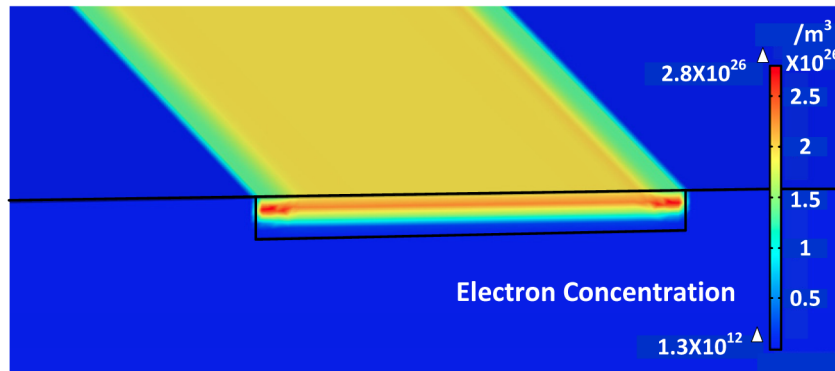

Fig. 4. Electron concentration in the N^+ region of the photodiode structure at 0 V bias condition.
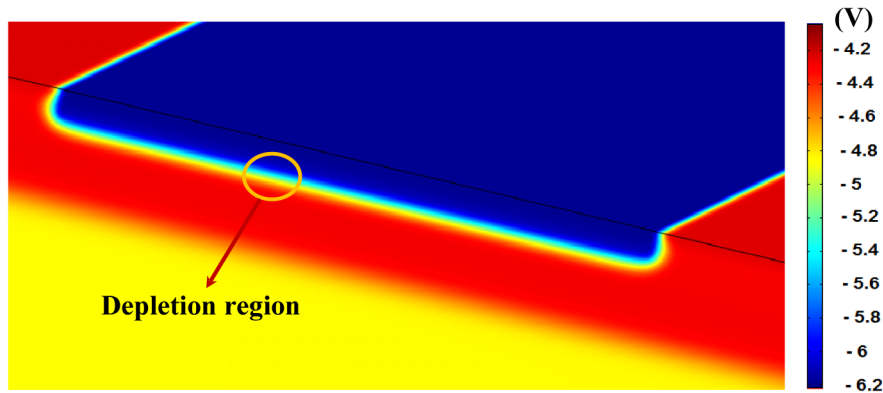

Fig. 5. Electric potential calculated from the vacuum level on a P + stripe to show where in the depletion region generation occurs.

The anode current of the photodiode was simulated using the continuity equation consisting drift-diffusion, generation and recombination rates. Both single- and multi-stripe structures were analyzed w/o 470nm radiation [see Fig. 6(a)]. The resulted I-V shows a bit higher current for single –stripe structure compared to multi-stripe structure under the dark condition due to the higher current cross-section area. However, multi-stripe device showed a 2.5 times improvement in the output current under illumination of 470 nm waves compared to the single anode one, which is a proof of concept for the significance of the dead layer and active depletion region. It is meaningfully matched with the improvement factor [10], we

expected regarding to the designed parameter for D and W dimensions which is $\frac{W+D}{W} = 2.66$.

Figure 6(b) shows the responsivity curve for multi-stripe shaped samples extracted by sweeping the photons' wavelength in the simulation tool. It can be seen that using the real doping values and dimensions, the responsivity is very selective to 470 nm illumination. This can be explained by the fact that at higher wavelengths, the beam can travel a lot more inside the substrate and in order to absorb that range, one might need to increase the depletion width of the junction. But, at lower wavelengths, the junction must be located closer to the surface to have strong generation of carriers which consequently may recombine in the dead layer.
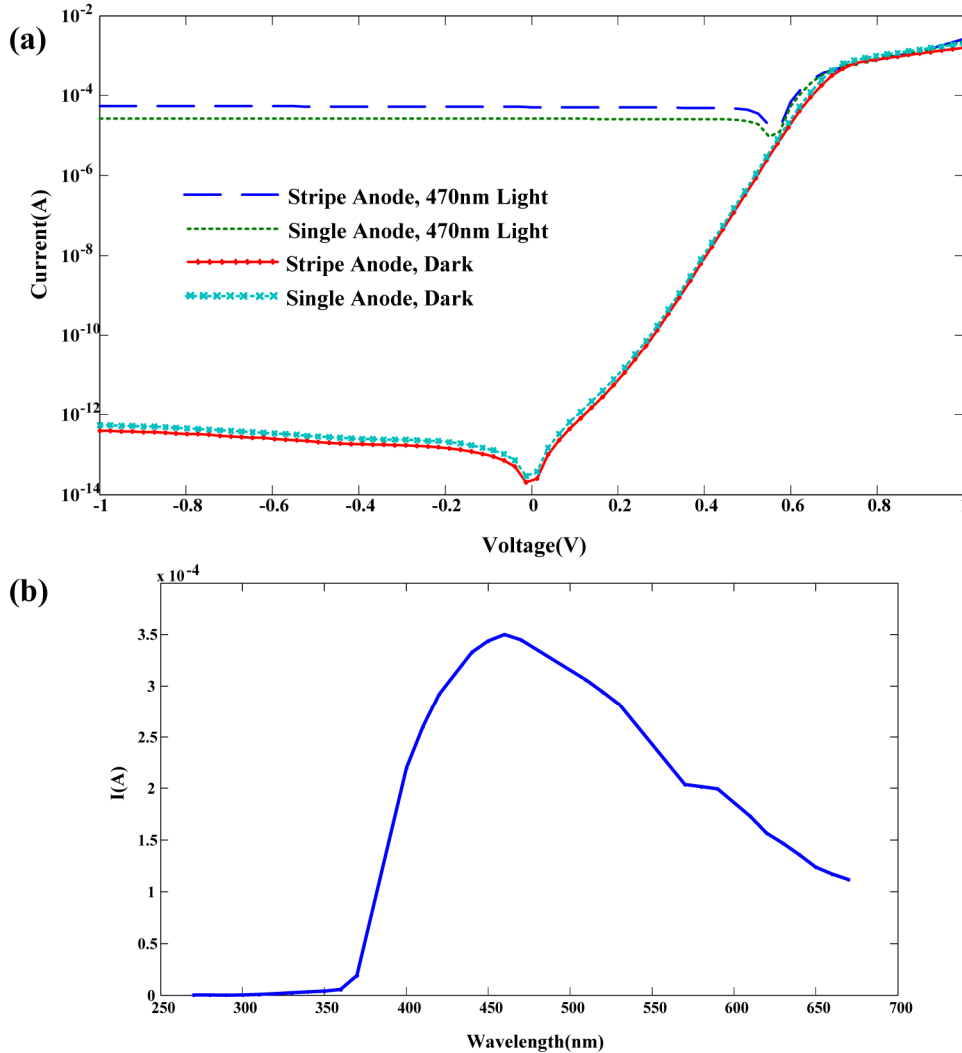

Fig. 6. (a) I-V simulation results of the single- and multi-stripe structures w/o 470nm radiation and (b) the resulted current vs. wavelength for the single- and multi-stripe structures.

4. Device fabrication and characterization

Not only output light detectors but also integrating more functionalities in LED package motivates the use of the Si LED WLP. One of the main challenges in this application is low

integration density for supporting LED bare dies. The dimension of a power LED bare die is usually in millimeter[2] scale which is quite large compared to the current IC transistor size. As shown in Fig. 7, the continuous decrease of the feature size in CMOS planar technology results in boosting the number of masks and the silicon wafer price (cost/cm^2). On the other hand, IC area is shrinking and so there are more dies fabricated on a single wafer which compensate the cost. Considering area limitation in solid state lighting, it seems that the fabrication of LED WLP is extremely cost ineffective by the advanced CMOS process. So a low cost CMOS planar technology is required as a promising option to subordinate the cost.
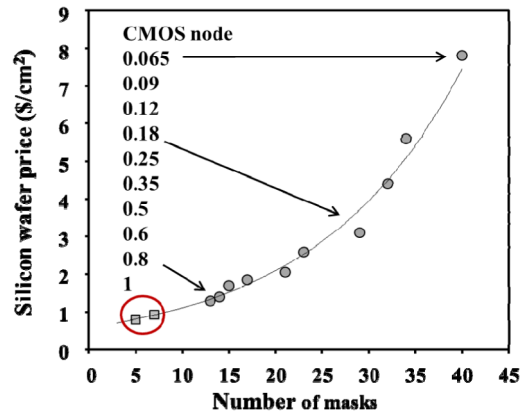
Fig. 7. Silicon wafer price for different number of masks used in IC processing.

The BiCMOS process developed in Dimes Institute of Microsystems and Nanoelectronics (The Dimes Technology Center affiliation is changed to Else Kooi Lab, EKL, from April 2015.) comprises of a 5 masks process that involves both Bipolar and CMOS transistors, which can be later used for feedback and control circuits [15]. It exhibits the two outstanding features; simplicity and cheapness. Although it has a limited performance, it is sufficient to be implemented for LED WLP and some simple IC designs. Figure 7 shows how BICMOS5 and 7 process, which adds 2 more masks for second interconnect layer, can potentially implement a smart LED driver platform for the cost of even less than 1$/cm^2.

This process was primarily developed for education purposes and has the advantage of using both types of BJT and CMOS transistors, but the disadvantage of having a trade-off between the two optimum settings for each type. Figure 8 shows this 5 lithography steps required for this process. The core of the process consists of 5 mask steps, listed in Table 1.
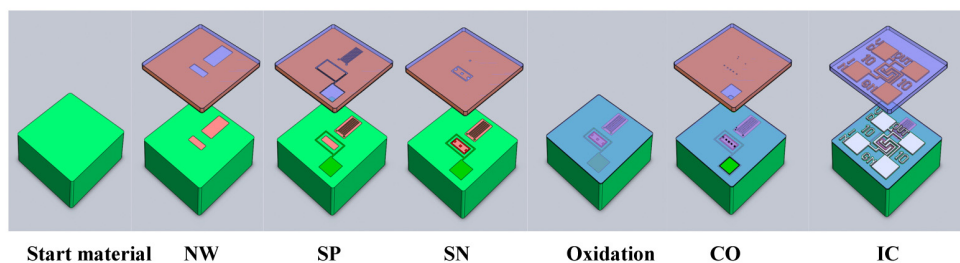
Fig. 8. Process overview of the core mask steps and oxidation process in the BICMOS5 process.

The process is now described using the structure of the photodiodes. It starts with a p-type low resistivity wafer. After growing dirt barrier oxide, in the first Litho step it is patterned for the n-wells of the npn dual junctions following with a phosphor implant and a deep diffusion. The second mask is used to create the p-type regions using a shallow boron implant: the shallow p + area of the detectors, and the contact area to the substrate. The third mask is for

the highly doped n-regions, i. e. contact to the n-well, by a shallow arsenic implant. After this step the wafer is annealed/oxidized for 12 minutes at 1000 °C and an isolation layer of 100 nm silicon dioxide forms on the whole surface (by thermal oxidation). This layer will act as an isolation layer between the interconnects and the substrate (as well as the gate material of the PMOS and NMOS transistors). The fourth mask is used to open the contact openings in the isolation layer. The final mask is used to pattern the interconnect layer and create a circuit by combining the different components.

Table 1. Process Overview

Step title	BiCMOS Processing step	Diode Processing Step
Start Material	p-type wafer	Substrate and lower junction anode
NW: N-well	n-type area for pmos transistor (n-well) and the collector for the bipolar npn	n-type area for the dual pnp junction acting as cathode
N-Well drive in	Annealing step at 1150°C	
SN: Shallow N	n-type source-drain for the nmos transistor and for the emitter of the bipolar transistor, low resistance collector contact and n-type guard ring	Contact to the cathode
SP: Shallow P	p-type source-drain for the pmos transistor and for the base of the bipolar transistor, p-type guard ring	Implantation of the shallow p area for upper p-n junction (anode) and contact to the p type substrate
Anneal/Oxidation	Dopant activation and gate oxide formation	Dopant activation and isolation oxide
CO: Contact	Contact openings	Contact openings
IC: Interconnect	Interconnect and gate material formation	Interconnect

There are several trade-offs in the process design. The first trade-off is between isolation layer thickness and the value for the optimum gate oxide. A transistor has the best characteristics with a low gate thickness, while the isolation layer on the rest of the wafer is preferably thick to minimize the parasitic effects. Another trade-off is the dopant concentrations and parameters of the n- and the p-regions. All parameters, such as the photodiodes junction depth, the responsivity and selectivity of the photodiode and for transistor's threshold voltage and saturation current, are dependent on the doping profile and geometries.

However, the doping parameters applied in this study were adjusted using device and process simulations for the optimum performance of the photodiodes using Synopsys TCAD . Figure 9 illustrates the doping profile of the P + -doped/N-well area measured by electrochemical capacitance-voltage profiler (ECVP). Due to the fact that the ECVP measures the active carrier concentration, the dead layer cannot be observed in this figure. The minimum at 330nm is the P+/N-well junction and the N-well is extended for 1.5µm into the substrate.
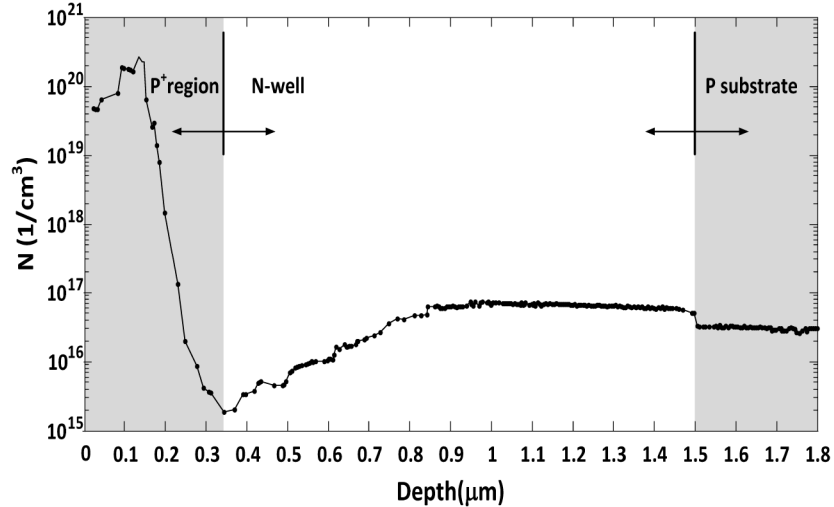
Fig. 9. ECVS profile of shallow P$^+$ region implanted in the N-well. The P$^+$-N junction is formed at 330 nm where the doping profile is first crossing N-well doping level.

The spectral responsivity of photodiode was measured by a solar cell simulator using a monochromatic light with sweeping wavelength in 300-1100 nm range. The responsivity plot shows a peak at λ = 480 nm with 342 mA/W. Figure 10 shows the responsivity of two different photodiodes vs. wavelength at 0 volt bias condition. Comparing to the single anode structure, an improvement in responsivity is observed for the multi-stripe photodiode. IR range responsivity shows a dramatic fall below and above 470 nm range which indicates a high selectivity for the target wavelength. The measured responsivity has a good correlation to the simulation results in Fig. 6(b).
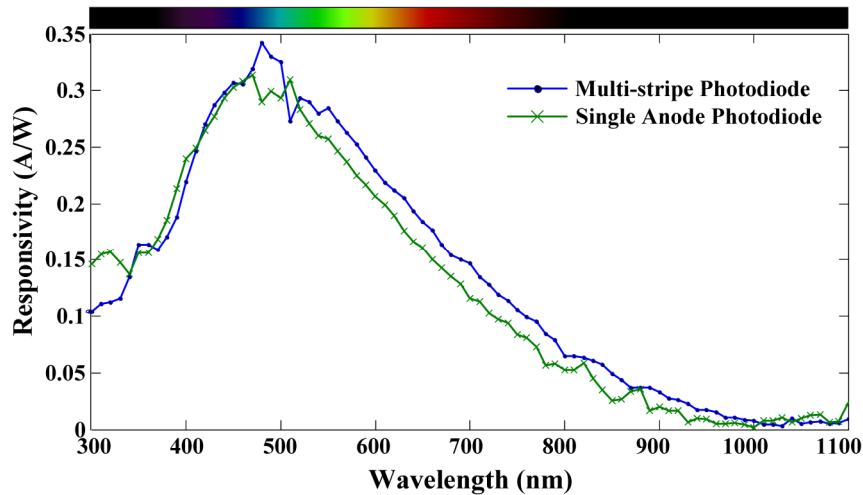

Fig. 10. Responsivity vs. wavelength for multi- and single-stripe shaped photodiodes.

A selectivity parameter can be defined as a ratio of responsivity for different wavelength, that is 42 for λ = 470nm and λ = 1000nm. It was seen that at high bias voltages, the responsivity can increase, while, because of the depletion area extension, selectivity would degrade.

5. Wafer level system integration

The target vertical LED in this study is a BRIDGELUX BLUE POWER DIE which is an In GaN-based blue color LED that can be later combined by a yellowish phosphor to generate the white output light. LED structure and main specifications can be found in Fig. 11 and Table 2. These LEDs are useful in a broad range of applications such as general illumination, automotive lighting, and LCD backlighting.
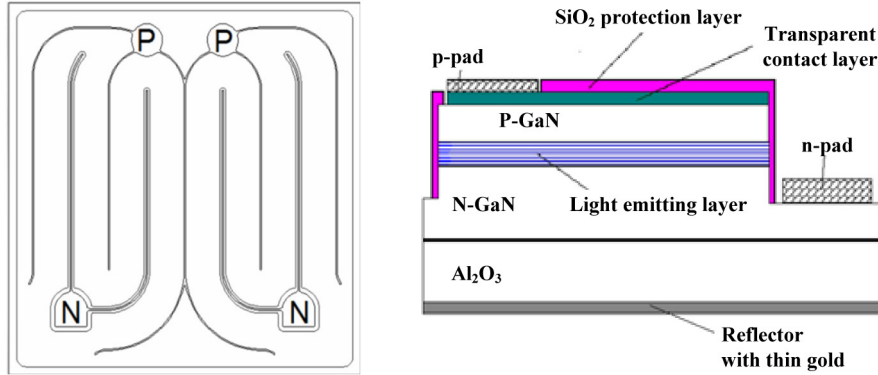

Fig. 11. PN juctions and die structure for Bridgelux blue power LED die.

Table 2. Specification of Target Led

Dimension	$1143 \times 1143 \times 150 \ \mu m^3$
DC Forward current	Max 700mA
Reverse voltage	5V
Working temperature	$-40 - 100°C$
Optical power (min)	340mW
Dominant wavelength	450-470nm

The photodiodes was also measured in the integrated system to study its performance for target LEDs and in real application platform. The package consists of an array of 4 LEDs which can be turned on separately or with different combinations. Figure 12 shows the package picture with off and on LEDs and photodiode positions.
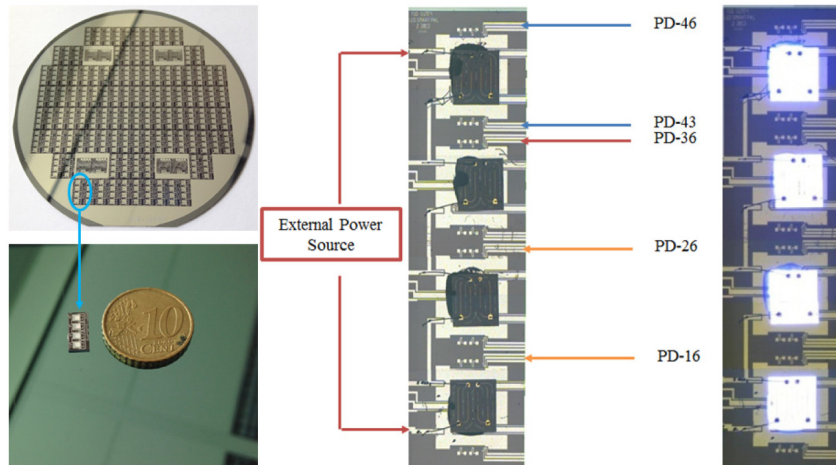

Fig. 12. Photodiodes in LED package. For each LED two sets of photodiodes were used to perform output light measurement.

Each LED chip consists of 2 parallel p-n junctions which we just used one of them in the package. The light intensity of LED was measured with the photodiodes at different driving currents. The results are shown in Fig. 13. When LED is off, the reverse current value is 10^{-12} A. Figure 13(a) shows almost 6 orders of magnitude increase compared to when the LED is off. This difference is governed by the generation of lots of electron-hole pairs in the active part of the device and a numerous recombination dominantly close to the surface. By normalizing the output current and fitting to the datasheet amounts a remarkable consistency can be achieved [see Fig. 13(b)].
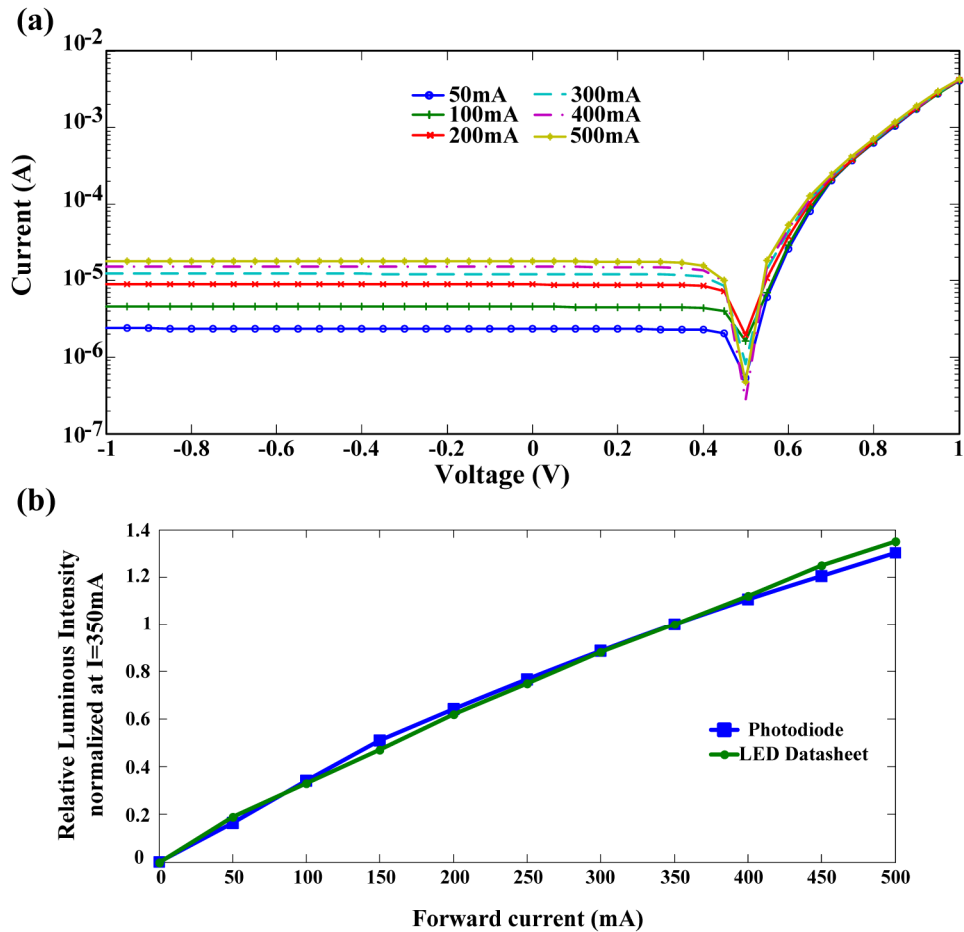

Fig. 13. (a) Photodiode output IV curve at different LED driving current. (b) Relative luminous intensity vs. LED forward current comparing the photodiode performance with the datasheet amounts.

The devices also were examined by some sort of stress test. Relative luminous intensity decays 0.9% within 2 hours with constant input current of 350 mA. This effect is caused by the temperature raise during the lighting [Fig. 14]. This is a proof of sanity for the importance and necessity of an intelligent control system for LEDs. It is worth mentioning that the ambient light rarely affects the performance of photodiode, due to its remarkable blue light selectivity.

(a)

I_f=350mA, 1 LED, PD 16

Legend:
- 1st light off
- 1min
- 10mins
- 30mins
- 60mins
- 120mins
- 2nd light off

X-axis: Voltage (V)
Y-axis: Current (A)

(b)

Y-axis: Relative Luminous Intensity Normalized at 350mA
X-axis: Time (minute)

Data labels: 0.000, 1.000, 0.998, 0.996, 0.995, 0.994, 0.992, 0.991, 0.000
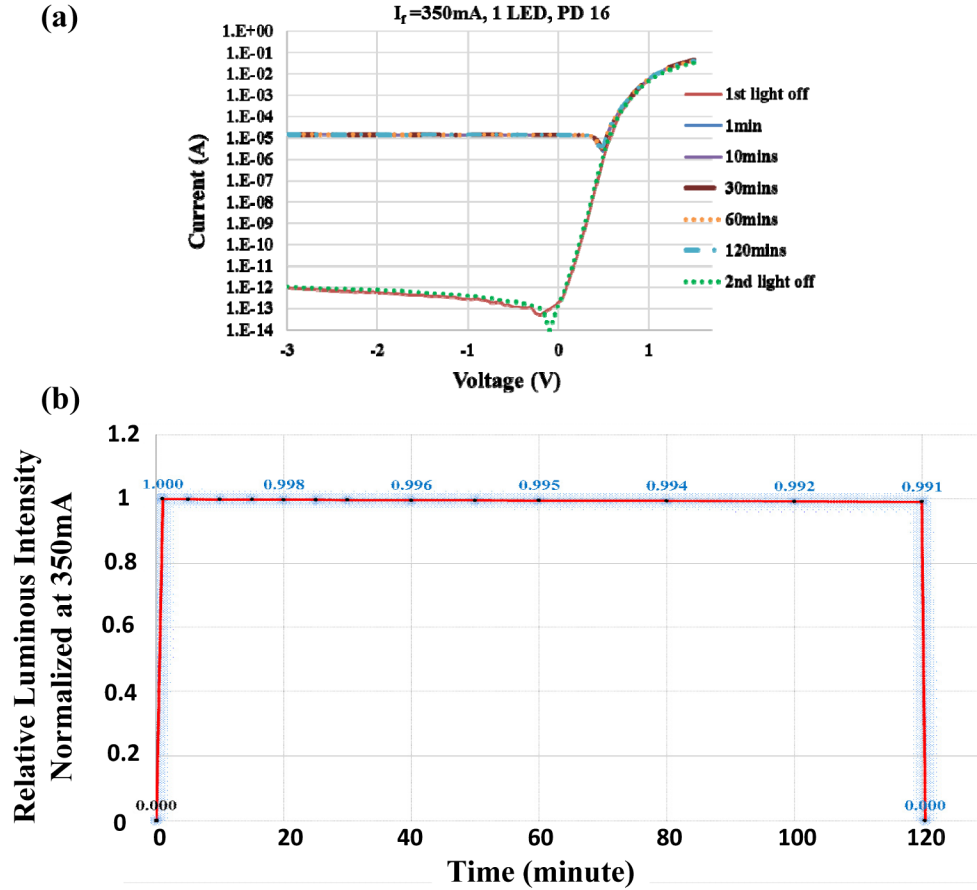
Fig. 14. (a) Photodiode IV characteristics over 120 min LED light exposure. (b) Normalized readout light intensity in LED working period of 2 hours.

Figure 15 compares the spectral responsivities of the fabricated photodiodes here and a calibrated UV-enhanced photodiode from Hamamatsu, S1226-18BQ. The commercial UV-enhanced device with an antireflection coating exhibits an almost non-selective behavior. However, our photodiode and the one manufactured in [10] demonstrate slightly lower responsivity for the deep ultraviolet spectral range. The device fabricated in [10] has a peak at 400nm, while the photodiode in this study has shown a peak at exactly 480nm which is remarkably matched with the illuminated waves from the LED. A rapid decreasing trend is observed for the VIS and IR ranges. Moreover, a two-fold increase in quantum efficiency

($QE_\lambda = \dfrac{R_\lambda}{\lambda} \times (1240W.\dfrac{nm}{A})$)) and comparable selectivity are evaluated for the LEDs fabricated

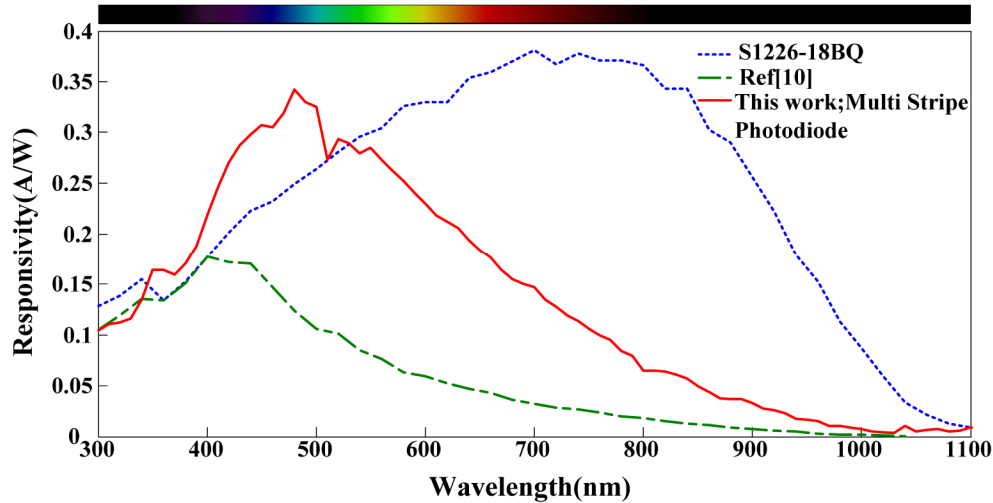in our work compared to the previously published devices.

Fig. 15. Measured responsivity vs wavelength for the multi-stripe photodiode. The spectral response of a published and commercially available UV-enhanced photodiode is also added for comparison.

6. Conclusion

A silicon stripe-shaped photodiode was designed and fabricated for sensing blue light in LED wafer level package. The device dimensions and doping were also designed and simulated using COMSOL Multiphysics. The maximum responsivity was at 480nm which is matched with the blue LED's illumination. The single anode structure due to higher rate of recombination caused by the dead layer formation showed lower responsivity compared to multi-stripe shaped one. The fabrication process was a 5 mask BiCMOS process with 2 μm gate length. This process enable to integrate blue sensitive photodiodes with active devices like BJT and CMOS transistors. It also provides a cost effective integration of large area devices like LED's with other functional devices. The complete wafer level package includes several functional devices such as sensors, power switches and primary logical circuits for a smart wafer level LED packaging. These IC technology compatible photodiodes, with junction at 330 nm, demonstrated a very high selectivity to blue light. The fabricated devices presented a two-fold increase in the responsivity and quantum efficiency compared to similar devices published earlier.

Acknowledgment