New Methods of Texturing Crystalline Silicon For Multi-Junction Solar Cell Applications

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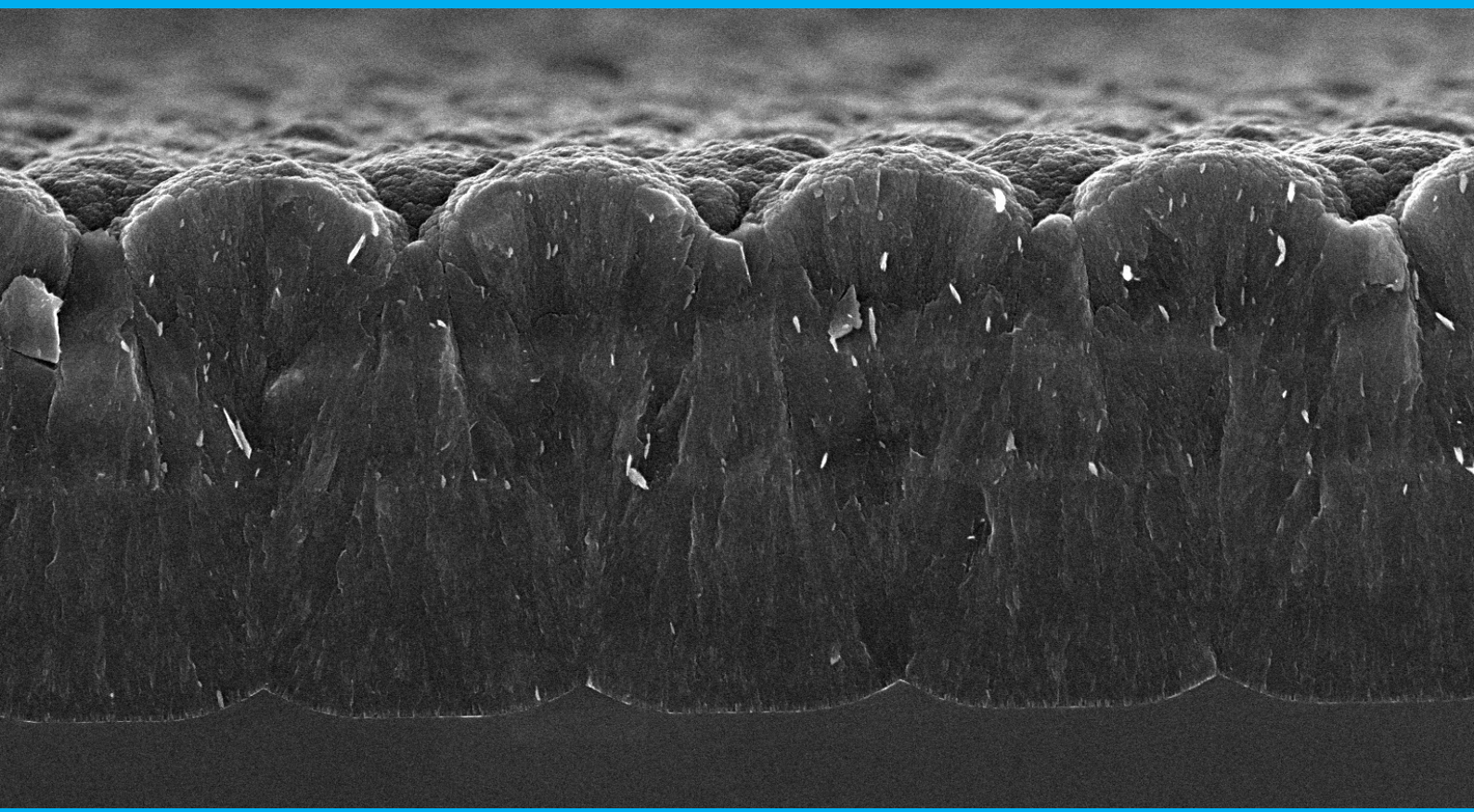

TU Delft

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For Multi-Junction Solar Cell Applications

by

M. Wiering

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Preface

When I graduated high school six and a half years ago, I had no clue what I wanted to do with my life. I only knew that I liked science, so I chose a bachelor's program that promised me this: applied physics. I had a difficult time during the start to my academic life and almost dropped out during the first period, but I found my way and got through it. During the difficult program of applied physics, I learned that my interest had shifted to current world problems. More specifically, the global energy crisis. This caused me to change my focus from pure physics to sustainable energy.

Of course, I want to thank everyone in the PVMD group for their help, but most of all my daily supervisor Thierry de Vrijer. His knowledge and calm personality have helped me through the rough patches of my thesis research. I also want to thank Prof. Arno Smets, both for being my supervisor and for the inspiring lectures during the minor Electrical Sustainable Energy Systems and the first year of my master Sustainable Energy Technology. Also, I would like to thank Dr. Gianluca Limodio for his guidance during my research, especially during my first couple of weeks in the cleanroom. Additionally, I would like to thank Martijn Tijssen and Dr. Gregory Pandraud for their help during the design of the photolithography mask that was needed for my research. Moreover, I want to extend my gratitude to everyone in the Else Kooi Laboratory who helped me. Furthermore, I would like to thank Dr. ir. Chandra Mouli and Dr. Pandraud for their willingness to be part of my thesis committee.

From the bottom of my heart, I want to thank my sweet, loving, and caring girlfriend. Marjolein, I am sure I could not have done this without you. Thank you for all the support during the late hours of studying and for being there for me through all the difficult times that are behind us. I love you for all the time you spent in the train, just to be with me for a couple of hours.

I also want to extend my thanks to all my friends, both in Delft and Heerhugowaard. Especially to Lyndon and Beau, who gave me a place to sleep whenever I needed it. Thanks to everyone who helped me through the stress by listening to me complain, or by having a beer with me.

Last but not least I want to thank my family for being there for me every step of the way. I would not have been at this point in my life without your love and support. I will always be grateful for your help.

M. Wiering
Delft, February 2020

”The good thing about science is that it’s true whether or not you believe in it.”
-Neil deGrasse Tyson

Abstract

In this thesis, two new types of crystalline silicon texturization were developed, eventually aimed to be used in a triple junction solar cell from monocrystalline silicon and two thin film silicon alloy layers. The bottom of the two thin film silicon layers is made of hydrogenated nanocrystalline silicon (nc-Si:H). The current problem with this technology is that the adhesion of the nc-Si:H to a flat surface of crystalline silicon is not always ideal. This can be improved by texturing the monocrystalline silicon. This also improves the optical efficiency. The standard pyramidal texture method of crystalline silicon has proven to be too sharp which leads to cracks in the layer of nc-Si:H during deposition. The two investigated texturing methods are a periodic hexagonal texture with semispherical walls created using photolithography and a random texture of craters using a sacrificial layer of polycrystalline silicon. The effect of different parameters on the textures was investigated and the two textures were compared in terms of their ability to grow crack-free nc-Si:H, their optical characteristics and their performance in a Silicon HeteroJunction (SHJ) solar cell.

For the hexagonal texture, a photolithography process was designed and tested on the ability to grow crack-free nc-Si:H. It was found that a texture period of 3 µm was most suited for the desired nc-Si:H layer thickness of 3-3.5 µm.

For the sacrificial layer process, the effect of the different parameters on the crater size was investigated. These tests showed that an amorphous silicon (a-Si) layer thickness of 1-2 µm gives the largest craters. The ideal implantation energy is dependent on both the implanted ion and the a-Si layer thickness. It was also found that the crater size increases with increasing dopant concentration. An anneal temperature of 950 °C for 60 minutes was determined to result in the largest craters. Furthermore, argon implantation using an energy of 250 keV in 1 or 2 µm of a-Si showed the biggest promise in terms of crater size, with an average hole diameter of around 320 nm. Craters with an average diameter of 430 nm were once found when implanting phosphorus at 5 keV in 1 µm of a-Si but these results were irreproducible.

In terms of optical performance, the hexagonal texture results in a slightly lower mean reflectance over a wavelength range of 300 to 1200 nm. The average reflectance of the hexagonal texture was 37.7%. The large craters of 430 nm diameter showed a reflectance of 38.2% on average compared to 41.5% for the sacrificial layer texture using argon implantation. The angular distribution of the reflectance showed that the reflectance of the hexagonal texture was very dependent on the measured angle and this angular dependence varies for different wavelengths. This indicates good light scattering of this texture. The results for the large craters show light scattering at approximately the same level as the photolithography samples, but more gradual over different angles. The smaller craters from argon implantation show the same gradual scattering of light as the large craters, but at a lower level.

The hexagonal texture with a period of 3 µm and the sacrificial layer texture using 1 µm of a-Si with 250 keV argon implantation were used to create SHJ's. Unfortunately, the minority charge carrier lifetime measurements of these SHJ's showed that the deposited passivation layers were likely to be too thin, which resulted in very low lifetimes: around 2.4 µs for the sacrificial layer texture and between 50 and 150 µs for the hexagonal texture. The effect of these low lifetimes were noticeable in the photovoltaic (PV) performance of the cells. The efficiency of the sacrificial layer SHJ's was only 0.1%. The efficiency of the hexagonal texture SHJ's were much higher, at 10.0%. Still, this efficiency was lower than anticipated. The reflectance measurements of these solar cells showed that the average reflectance of the SHJ's using the photolithography texture was 13.4% with TCO. This is lower than the reflectance of the sacrificial layer SHJ, which was at 14.4% with TCO.

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Introduction

For thousands of years, humans have burned carbon based fuels. The first evidence of control of fire by homo erectus dates back to about a million years ago. This fire was used to cook food and provide warmth.[42] This use of fire did not change until the industrial revolution. During this period, mankind discovered that fire could be used for different purposes with the use of the steam engine. Coal was used to power these engines and blast furnaces for the production of iron. Since the industrial revolution, the use of these fossil fuels has skyrocketed.

There are two major drawbacks to the use of fossil fuels. Firstly, the amount of fossil fuels on earth is finite. Currently, the human race is rapidly depleting the available fossil fuel reserves and it is becoming harder and harder to collect fossil fuels from the earth. With the current rate of consumption, oil and natural gas reserves will be depleted in 50 years, that is if the consumption rate stays constant.[16] However, the fossil fuel consumption is still rising and therefore the reserves can be depleted even faster than the estimates. The second drawback is the effect of the large quantities of carbon dioxide that are released in the earth's atmosphere due to the burning of fossil fuels. Carbon dioxide is known to be a greenhouse gas (GHG). These gasses prohibit heat from leaving the earth. Greenhouse gasses are divided into two groups. "Feedbacks" are gases that respond physically or chemically to changes in temperature. Water vapor is one of these gases. When the earth's atmosphere warms, the amount of water vapor increases, which increases the possibility of clouds and precipitation, which decreases the amount of water vapor in the atmosphere. Carbon dioxide belongs to the second group of greenhouse gases. These gases do not respond to changes in temperature. Releasing large amounts of carbon dioxide into the atmosphere will increase the ability of earth to preserve its warmth. This will cause an increase in temperature around the globe.[39] This increase in temperature can diminish grain yields and rise ocean levels.

Between 1880 and 2012, the average global temperature has increased by approximately 0.85°C. Due to molten ice and increased temperature, the global average sea level has risen by 19 cm. The current goal of the United Nations is to keep the temperature increase under 2°C.[40] To reach this goal, a new energy system has to be adapted which relies almost entirely on the use of renewable energy.

There are a number sources for sustainable energy. Wind energy is one of the most widely known sources of renewable energy. Wind turbines use the energy in the flow of air to rotate large blades. This rotational energy is then converted to electrical energy using a generator. Hydropower uses the flow of water from a high place to a low place to produce electricity. Heat from the earth can be used as a heat source but can also be used to produce electricity in geothermal power plants. Biomass can be grown in the form of wheat or algue which can be burned to produce heat and electricity, or can be used to produce biofuels. A type of renewable energy that is currently being researched for implementation is ocean power. The motion of the tides and waves can be used to produce electricity. Currently, solar power is the world's largest renewable energy source with an installed capacity of 398 GW in 2017 which generated 460 TWh.[1] This is a good start but solar power still has a lot of unrealised

potential. To fulfill that potential, cheap solar cells with a high efficiency need to be developed.

1.1. Solar radiation

Light from the sun has reached the earth since the earth was formed billions of years ago. The light from the sun can be used for energy in two ways. It can be used for heat, or directly converted to electricity. This last method uses the photovoltaic (PV) effect. Before we can understand this photovoltaic effect, it is good to have some more insight in the light we receive from the sun.

1.1.1. Electromagnetic radiation

Light is a form of radiation, specifically electromagnetic radiation. Radiation is the emission or transmission of energy through space or a material in the form of waves. There are different types of radiation: acoustic radiation such as sound, particle radiation such as α and β radiation and electromagnetic radiation.[57] This electromagnetic radiation is in the form of waves and travels with the speed of light, as was predicted by Maxwell in 1861. He was also the first person to realize that light is electromagnetic radiation. Albert Einstein was the first person to understand that light consists of well defined energy quanta, which are called photons. The energy of a photon is defined by

$$E = hv \tag{1.1}$$

where v if the frequency of the electromagnetic wave and h is Planck's constant. Since the speed of light through a medium is constant, the length of one period of light, which is the so called wavelength, can be defined as

$$\lambda = \frac{c}{v} \tag{1.2}$$

Where λ is the wavelength, c is the speed of light in the specific medium and v is the frequency. Therefore, equation 1.1 can be written as

$$E = \frac{hc}{\lambda}. \tag{1.3}$$

These relations show that a larger wavelength corresponds to a higher frequency and therefore a smaller energy. Light has been divided into multiple energy regions. These regions are shown in figure 1.1.

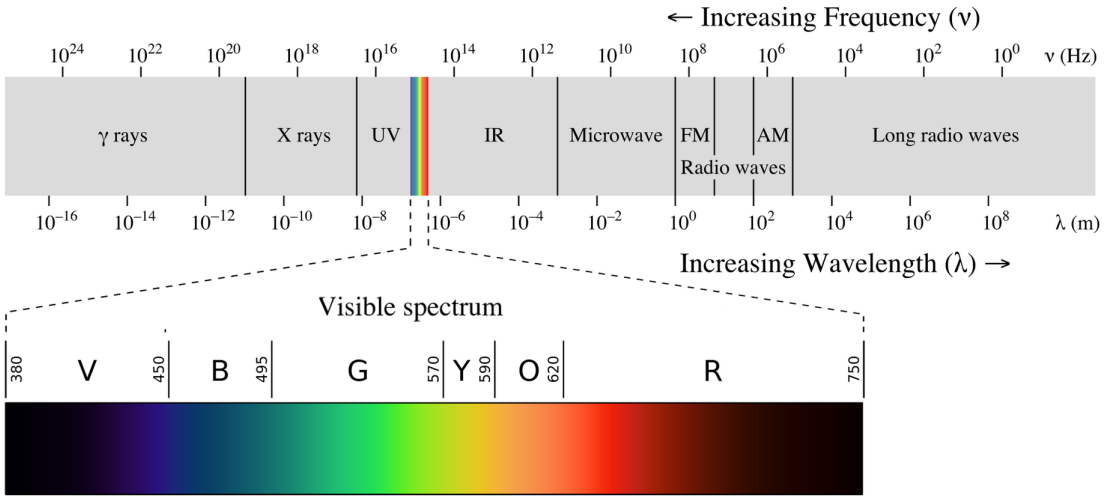


Figure 1.1: Spectrum of electromagnetic radiation.[15]

High energy photons are classified as gamma rays and X-rays. Visible light is only the small region with a wavelength of between 380 and 750 nm. Ultraviolet (UV) and infrared

(IR) are respectively the regions with higher and lower energy than visible light. Radio waves are defined as electromagnetic waves with a wavelength of larger than one meter.

1.1.2. Solar spectrum

If a piece of metal is heated, it starts to glow. This glow starts as red and evolves to yellow and eventually blue if the metal is heated more and more. This piece of metal emits light and therefore electromagnetic radiation which is called thermal radiation. Every object with a temperature above zero Kelvin emits thermal radiation. The concept of a blackbody can be used to describe thermal radiation. A blackbody has a reflectivity of 0 and therefore absorbs all incident radiation. Planck's law for blackbodies showed the relation between the temperature of a blackbody and its emitted spectral distribution. The spectral distribution shows the number of photons of a particular energy emitted by the sun as a function of the wavelength. The spectral irradiance shows the power density per wavelength $[Wm^{-2}m^{-1}]$. If the spectral irradiance is integrated over all wavelengths, the irradiance is obtained in $[Wm^{-2}]$. The surface of the sun has a temperature of about 6000 K and therefore emits thermal radiation. If our sun was a perfect blackbody, its spectral irradiance would look like figure 1.2. This figure also shows the incident solar radiation outside our atmosphere, which is called AM0 radiation. This spectrum has an irradiance of 1361 Wm^{-2}. AM stands for Air Mass. AM1 means that the light has travelled through the atmosphere at a right angle, so it had travelled through the thickness of the atmosphere once. Therefore, the irradiance outside our atmosphere is called AM0. Since the earth has a tilt with respect to the sun, usually AM1.5 is used as a standard test condition. The AM1.5 spectral irradiance is also shown in figure 1.2. The difference between AM0 and AM1.5 is mainly caused by scattering and absorption by dust particles and molecules in the atmosphere. Gaps are also visible in the AM1.5 spectrum compared to the AM0 spectral irradiance. These gaps are caused by water vapor, oxygen and carbon dioxide, which absorb light of specific wavelengths. The total irradiance of the AM1.5 spectrum is 1000 Wm^{-2}.

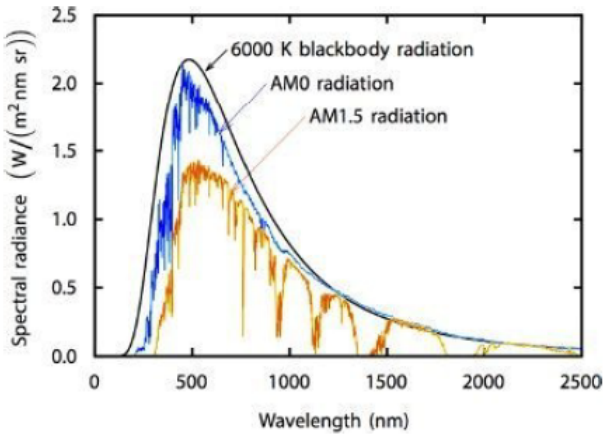


Figure 1.2: Blackbody spectrum of a 6000 K blackbody, the AM0 spectrum and the AM1.5 spectrum.[49]

1.2. Semiconductor physics

The photovoltaic effect occurs in semiconductors such as silicon. Understanding this effect requires knowledge about the atomic structure and electron shell configuration of these materials. Since silicon is studied in this research, this material will be used to explain the photovoltaic effect.

1.2.1. Bohr's model

To understand the atomic structure of silicon, one must first have some knowledge of Bohr's atomic model. This model describes atoms as a nucleus comprised of protons and neutrons with electrons orbiting this nucleus. The electrons can only occupy certain allowed orbitals

with a specific energy. The electrons can only move in between allowed orbitals by jumping from one allowed orbital to another when energy is gained or lost. These orbitals are also called shells and can contain a certain number of electrons which have the same energy. The number of allowed electrons depends on the shell. The rule is that a shell can contain $2n^2$ electrons, where n is the shell number. The first shell can contain 2 electrons, the second shell can contain 8 electrons, the third shell can contain 18 electrons etcetera. The type of element is decided by the number of protons in its nucleus. Since an atom should have neutral charge, the number of electrons that orbit the nucleus should be equal to the number of protons in the nucleus. The chemical behaviour of an atom is mainly determined by the electrons in its outermost shell, which are called the valence electrons. These electrons are bound more weakly to their nucleus. If an atom has three or less electrons in its outer shell, these electrons can be released from their nucleus with very little energy. Therefore, at room temperature, these valence electrons can move freely through the material which is therefore classified as a conductor. An insulator has an outer shell that is almost filled with electrons. Therefore, these electrons are more tightly bound to the nucleus and cannot move through the material freely which makes them an insulator. Semiconductors are in between the conductors and the insulators. The number of electrons in their valence shell is more than 3 but the shell is not close to being filled.[43]

1.2.2. Atomic structure of silicon

Silicon has atomic number 14 and therefore 14 protons in the nucleus and 14 electrons orbiting this nucleus. Thus, in ground state, two electrons fill the first shell. The second shell needs 8 electrons to be filled. This leaves 4 electrons for the third shell, which is therefore the valence shell. These electrons can interact with other atoms to form chemical bonds. Two silicon atoms can form a chemical bond by sharing each other's valence electrons. This bond is called a covalent bond. The four valence electrons of silicon can therefore bond to four other silicon molecules. When silicon atoms bond, they form a crystal in which every silicon atom bonds with four other silicon atoms. These bonds all have the same length and angles between bonds. The angles are all 109.5°. This creates a so called diamond lattice as the structure of crystalline silicon. Figure 1.3 shows the crystalline structure of silicon. The figure on the left is the unit cell of the crystal. The unit cell is defined as the smallest group of atoms in the crystal structure that shows the repeating pattern.

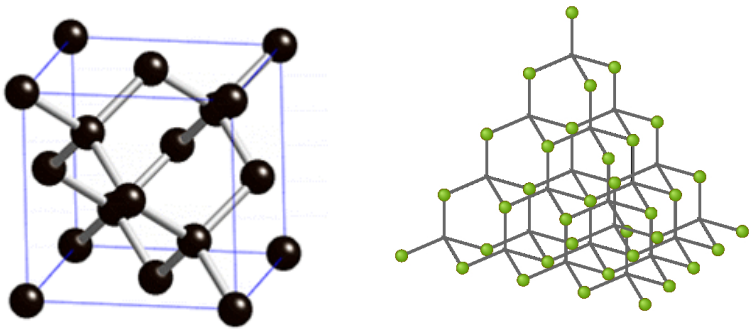


Figure 1.3: Left: Unit cell of a diamond lattice.[58] Right: Atomic structure of a diamond lattice.[22]

1.3. Photovoltaic effect

The photovoltaic effect is the essence of PV modules. This effect occurs in semiconductors when it is illuminated with light with sufficient photon energy. It consists of three stages: the generation of charge carriers, separation, and the collection of these charge carriers.

1.3.1. Generation of charge carriers

The covalent bonds between silicon atoms can be broken if energy is applied. When the covalent bond is broken, the valence electrons are released from their nucleus and can roam freely through the material. These electrons leave ”holes” in their position close to the nucleus. Since a negative charge is missing in this position, this hole is considered positively charged. A nearby valence electron can take the position of this hole, which moves the hole to the original position of this valence electron. This way, holes can move through the material. As mentioned before, electrons in an isolated silicon atom can only have discrete energy values. In monocrystalline silicon, the periodic atomic structure results in ranges of allowed energy states. These ranges are called the energy bands. Between these bands, there are energy gaps that are off limits. These ranges are called band gaps. This is shown in figure 1.4. The highest filled energy band, in which the valence electrons reside, is called the valence band. The lowest empty energy band is called the conduction band. Figure 1.4 also shows that in a metal, the conduction band and the valence band overlap. This shows that the valence electrons in a metal can easily break free from their nuclei and roam freely through the metal. an insulator has a big gap between the valence band and the conduction band. This shows that a relatively large amount of energy is needed for the valence electrons to go from the valence to the conduction band. A semiconductor, like silicon, has a smaller bandgap than insulators. This shows that some energy is needed for electrons to jump from the valence band to the conduction band but that this required energy is much lower than for insulators. Silicon has a bandgap energy of 1.12 electronvolt (eV) at room temperature.

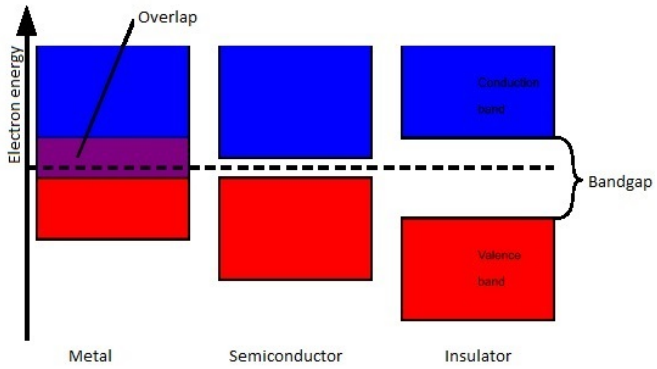


Figure 1.4: Band diagram of a metal, a semiconductor and an insulator.[31]

This small bandgap of semiconductors is what drives solar cells. A photon can be absorbed by the material if its energy is bigger than the bandgap energy. On absorption, the photon energy is transferred to an electron which is excited to the conduction band and can therefore move through the material. The electron leaves a hole behind in the valence band. Therefore, on excitement of an electron to the conduction band, a so called electron-hole pair is created. The electrons and holes are the charge carriers in solar cells.

1.3.2. Separation of charge carriers

If nothing is done to separate the electron and hole, this pair recombines since this is the lowest energy state. During recombination, the electron falls back from the conduction band to the valence band. The energy can then be released as heat or as a photon. In a solar cell, the electron-hole pair is separated by the use of doping.

Doping

Doping is the substitution of silicon by different elements in the crystal lattice. Doping can be used to manipulate the concentrations of electrons and holes in crystalline silicon. Commonly, Boron and Phosphorus are used as dopant materials. Boron has three valence electrons. Therefore, when it is introduced into crystalline silicon, it cannot bond with all four neighbouring atoms. This boron atom can ”accept” an electron from a silicon-silicon bond

that is nearby. This creates a hole that can move around through the crystalline silicon. Boron is called an acceptor. When a semiconductor is doped with boron, it is called p-type since this material has more positively charged holes than intrinsic silicon. Phosphorus has five valence electrons. When phosphorus is introduced into the crystalline lattice, it can bond with the four surrounding silicon atoms. The fifth electron can be freed from the phosphorus atom by absorbing thermal energy. At room temperature, this fifth electron can easily move through the material. The phosphorus atom ”donates” an electron to the crystal lattice and is therefore called a donor. When a semiconductor is doped with phosphorus, it is called n-type since this material has more negatively charged electrons than intrinsic silicon. This doping increases one type of charge carrier, boron doping increases the number of holes in the material and phosphorus doping increases the number of free electrons. Since one of the charge carrier densities is increased, this charge carrier is called the majority charge carrier and the other is called the minority charge carrier. Charge neutrality is maintained since the boron and phosphorus atoms become charged. The boron atoms become negatively charged and the phosphorus atoms become positively charged. The electrical conductivity of semiconductors can be influenced by influencing the concentration of charge carriers in the material. Therefore, doping can be used to increase the electrical conductivity.

P-N junction

P-type and n-type semiconductors can be joined. In the n-type region, the atoms have a positive charge and the number of free electrons is much bigger than the number of holes. In the p-type region, the atoms have a negative charge and the number of holes is much bigger than the number of free electrons. This causes diffusion of the electrons from the n-type region to the p-type region and of holes from the p-type region to the n-type region. In the region around the junction, the electrons and holes meet and recombine, which causes a depletion region. Since the electrons and holes recombine in this depletion region, the only charge left is caused by the atoms. The positive atoms are at the side of the n-type and the negative atoms are at the p-type side. This causes an electric field between the n-type and p-type in the depletion region. This effect is shown in figure 1.5.

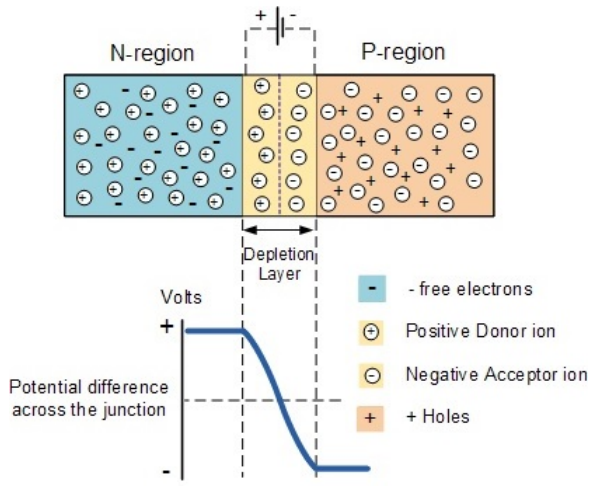


Figure 1.5: P-n junction of a semiconductor.[52]

When a photon is absorbed in the depletion region, an electron-hole pair is formed. The electric field causes this electron and hole to drift. The electron will be drawn to the positive atoms, to the n-type region, and the hole will be drawn to the negative atoms, to the p-type region. Therefore, a p-n junction is used in solar cells to separate the charge carriers.

1.3.3. Collection of charge carriers

Contacts are needed at the front and back of the device. These contacts collect the electrons, for instance at the back. These electrons are then used to perform work and are eventually

returned to the other side of the material to recombine with the holes. In this way, the chemical energy of the electron-hole pairs is converted to electrical energy.

1.4. Efficiency limits of solar cells

The efficiency is one of the most important properties of a solar cell. The efficiency shows how much of the incoming light is converted into electrical energy. The efficiency of a solar cell has physical limitations. For a single junction solar cell, the theoretical maximum efficiency is referred to as the Shockley-Queisser limit. The Shockley-Queisser limit mainly describes the losses that occur due to the spectral mismatch.

1.4.1. Spectral mismatch

As mentioned in section 1.3.1, the semiconductor in the PV cell has a specific bandgap energy. For silicon, this energy is 1.12 eV. Only photons with an energy higher than this bandgap energy can be absorbed to create electron-hole pairs in the semiconductor. If a photon is absorbed with an energy higher than the bandgap energy, the electron is excited higher in the conduction band. This can be seen in figure 1.6. Electrons prefer to be in the lowest energy state possible and will therefore relax until near the bottom edge of the conduction band. The excess energy is then released as heat.

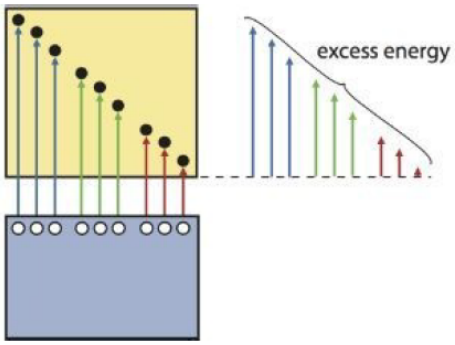


Figure 1.6: Energy loss due to thermalization in solar cell.[49]

Photons with an energy lower than the bandgap energy cannot create an electron-hole pair in the semiconductor material. These photons do not contribute to the production of electrical energy. These two losses combined are called the spectral mismatch. Shockley and Queisser combined the spectral mismatch losses with other losses in the solar cell to find the maximum theoretical efficiency of a single junction solar cell with respect to its bandgap. This is shown in figure 1.7. The other losses taken into account are the losses due to thermal radiation and the fill factor of the device being lower than 100%. The fill factor is defined as practical maximum power output divided by the theoretical maximum power output of the device. The fill factor will be further discussed in section 2.7.2.

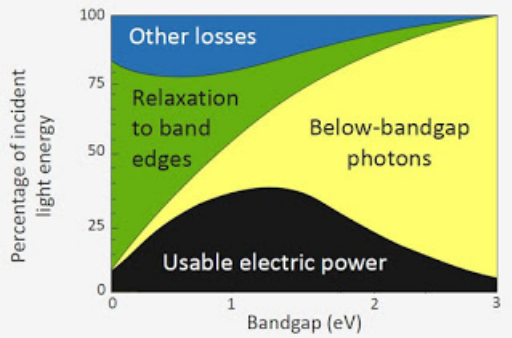


Figure 1.7: Energy loss due to thermalization in solar cell.[30]

Figure 1.7 shows that the maximum efficiency of a single junction solar cell can be obtained by using a semiconductor with a bandgap of 1.26 eV. The theoretical maximum efficiency of this device is 30.1%. This is however, in the case of AM0. For AM1.5, this theoretical maximum efficiency occurs at a bandgap energy of 1.34 eV and has a value of 33.1%. The Shockley-Queisser limit is a very simplified model. There are other losses that have to be accounted for in real solar cells. These losses include optical losses, charge carrier collection losses, losses due to electrical resistance of the device and losses due to leakage currents.

1.4.2. Optical losses

When light is incident upon an interface between two media with different refractive indices, part of the light is reflected and the other part is transmitted. The physics behind this phenomenon will be discussed in section 2.1.1. The reflectivity and transmittance of the material are wavelength dependent. Since a solar cell consists of multiple layers, all reflections and transmissions at the different interfaces have to be taken into account, which leads to a total reflectance of the solar cell. This reflectance causes a lower efficiency since a part of the usable incident light is lost due to reflection. The reflection losses can be decreased by texturization of the solar cell. For texturization of crystalline silicon, the front of the solar cell is exposed to acid in order to create a textured surface which decreases the reflection of the solar cell. This will be further discussed in section 2.2.
As mentioned in section 1.3.3, contacts are needed at the front and back of the solar cell. The front contacts are usually made of thin metal strips, which do not transmit light. Therefore, the covered area decreases the active area of the solar cell, which decreases the efficiency. This loss is called the shading loss. The front contacts should therefore be designed with care since the resistance of the front electrode should be small but the electrode should not cover a big part of the semiconductor.
When light is not reflected by the front contacts and transmitted into the solar cell, it is partially absorbed as it propagates through the material. Thus, a part of the light is absorbed outside of the semiconductor, which is the active part of the solar cell and is called the absorber. All absorption outside the semiconductor material results in losses. This type of loss is called parasitic absorption.
Also, since the absorber is not infinitely thick, some light is transmitted by the absorber. This loss also lowers the total solar cell efficiency.

1.4.3. Charge carrier collection losses

Some of the photon generated electron-hole pairs are not collected at the electrodes. These charge carriers recombine before reaching the contacts and can therefore not contribute to the generated electricity. The recombination rate has a big influence on the performance of a solar cell. The recombination of charge carriers is dependent on for instance the number of defects in the material. A defect is a position in the crystal lattice that misses an atom or is accupied by a foreign atom. These defects are places where an electron or hole can get trapped until an opposite charge carrier causes recombination. Charge carrier recombination will be further discussed in section 2.3.

1.5. Photovoltaic technologies

Some of these losses, for instance the spectral mismatch losses and the optical losses, can be reduced. This is done by creating new technologies that were designed to tackle the problems that cause these losses. This section gives a quick overview of the different generations of PV technologies.

1.5.1. First generation

The first photovoltaic device was built in 1954 and had an efficiency of 6%. This first generation of solar cells was based on wafers of crystalline silicon as the semiconductor material and has a single p-n junction. These solar cells are currently the most efficient technology for residential use. In 2016, over 80% of the installed solar panels was based on this technology. These panels have a relatively high efficiency of up to 22%. The big disadvantage of this

technology used to be the high production cost of these solar cells. This technology requires high purity crystalline silicon of which the production is very energy and material intensive. This caused incentive to explore other, cheaper types of silicon such as polycrystalline or amorphous silicon. These materials are less expensive to produce than monocrystalline silicon but also achieve a lower efficiency. The efficiency of polycrystalline solar panels are on average between 13 and 16%, while the efficiency of amorphous silicon solar panels are 6 to 8 %.[23] In recent years, the methods of producing monocrystalline silicon have improved. This, together with an increase in competition, has caused a significant drop in the price of this technology. The cost of monocrystalline silicon solar cells have dropped from 77$ in 1977 to just 0.36$ in 2014.[11]

1.5.2. Second generation

The second generation consists of thin film solar cells. These are called thin film solar cells since they are made from films that are much thinner than the crystalline silicon wafers that were used in the first generation of solar cells. It was expected that thin film solar cells would become much cheaper than the crystalline silicon solar cells. The price decline of wafer based silicon solar cells has annulled this expectation and therefore thin film solar cells have had trouble becoming economically viable. Thin film solar cells usually have a lower efficiency than crystalline silicon solar cells, except for Gallium Arsenide (GaAs) based thin films. Thin film solar cells can be made from a variety of different materials. Examples of thin film technologies are: III-V technologies including GaAs, thin film silicon solar cells which include thin film silicon alloys, chalcogenide solar cells including copper indium gallium selenide (CIGS) and cadmium telluride (CdTe) PV technologies, organic solar cells, dye sensitized solar cells and perovskite solar cells.

1.5.3. Third generation

Third generation solar cells aim to overcome the Shockley-Queisser limit by using novel approaches. Researchers are aiming to overcome this limit at the lowest possible cost. Some examples of third generation technologies are: spectral conversion, Multi-exciton generation, intermediate band solar cells, hot carrier solar cells and multi-junction solar cells. Spectral conversion works by either combining two low-energy photons into one photon with approximately the bandgap energy or by splitting one high energy photon into two photons with approximately the bandgap energy. Multi-exciton generation uses high energy photons to produce more than one electron-hole pair. In intermediate band solar cells, the photons with an energy lower than the band gap energy are utilized by creating an available electron energy state in between the valence band and the conduction band. The electron can be excited into this intermediate band by a low-energy photon and can then be excited into the conduction band by another low energy photon. Hot carrier solar cells aim to collect the electron-hole pairs just after light excitation but before thermal relaxation to the band edges. This reduces thermal relaxation losses. Multi-junction solar cells use multiple photoactive layers with a different bandgap to utilize the solar spectrum more efficiently. The multi-junction solar cell technology will be used in this research and will therefore be discussed more in depth. For more information about the other third generation technologies, please refer to the book: Solar Energy, The physics and engineering of photovoltaic conversion, technologies and systems.[49]

1.5.4. Multi-junction solar cells

Multi-junction solar cells use multiple semiconductor materials with different bandgaps. This is done to minimize the losses due to spectral mismatch, which is discussed in section 1.4.1. If one semiconductor material is used, the photons with an energy lower than the bandgap are not absorbed and therefore lost, while a large fraction of the energy of energetic photons is lost as heat due to thermalization. These losses can be decreased by using a semiconductor with a small bandgap, to utilize most of the low energy photons, in combination with semiconductors with a higher bandgap, to minimize the thermalization losses. In a multi-junction solar cell, the semiconductor material with the biggest bandgap is at the top of the solar cell. This is done since the semiconductor with the biggest bandgap ideally only absorbs high

energy photons and transmits the photons with energy below the bandgap. The second semiconductor material utilizes the photons with energies between the bandgap of the top semiconductor material and its own bandgap energy, etcetera. A comparison of the spectral utilization of a single-junction silicon solar cell and a triple-junction thin film solar cell is shown in figure 1.8.

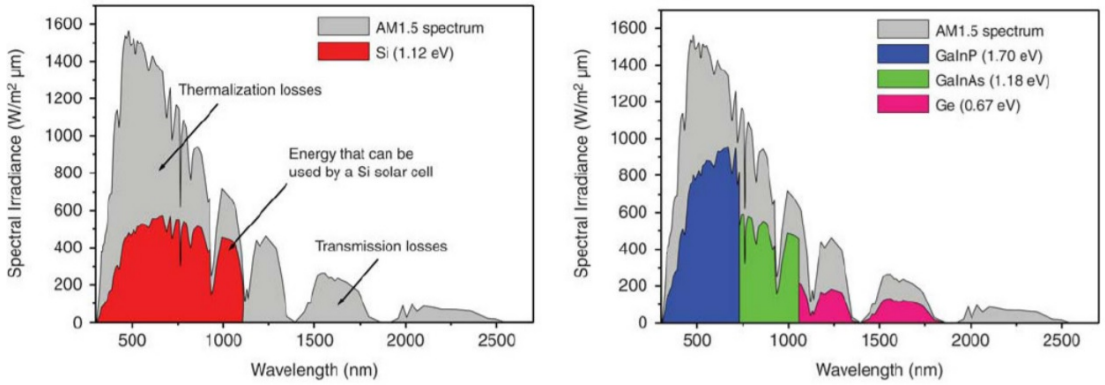


Figure 1.8: Comparison of spectral utilization of silicon solar cell and multi-junction thin film solar cell.[59]

1.6. Project description and outline

The main goal of this research is to develop two new types of crystalline silicon texturization, eventually aimed to be used in a triple junction solar cell from monocrystalline silicon and two thin film silicon alloy layers. These new types of texturing crystalline silicon can also be used in other devices, such as topcon designed crystalline silicon solar cells or perovskite combined with crystalline silicon solar cells but this is outside the scope of this research. In the created triple junction cell, the bottom of the two thin film silicon layers is made of hydrogenated nanocrystalline silicon (nc-Si:H). The current problem with this technology is that the adhesion of the nc-Si:H to a flat surface of crystalline silicon is not always ideal. This causes low electrical conductivity and therefore bad electrical properties. A solution to this poor adhesion would be changing the deposition conditions. Unfortunately, the quality of the nc-Si:H is very dependent on these conditions and a small change could ruin this layer. Also, a flat interface is not optically efficient, as will be explained in section 2.2.2. Texturing the crystalline silicon will both improve the optical efficiency and the adhesion between the crystalline silicon and the nc-Si:H. The standard texturing method of crystalline silicon is creating inverted pyramids on the surface, which improves light incoupling of the material. However, these pyramids are quite sharp which leads to stress during material growth and eventually cracks in the layer of nc-Si:H during deposition. This disastrously decreases the performance of the solar cell. Therefore, new methods of crystalline silicon texturing should be developed. In this research, two new methods are investigated. The first way is by using photolithography to create a hexagonal texture with semi-spherical walls on the monocrystalline silicon wafer with multiple feature sizes. The second way is creating a polycrystalline silicon layer on top of the monocrystalline silicon wafer. This polycrystalline silicon layer is then etched away, which creates a random texture on the monocrystalline silicon wafer. Hence, the first subgoal of this research is to develop a process that results in a hexagonal texture on crystalline silicon. The second subgoal is to design a photolithography mask that creates this hexagonal texture without generating cracks in a deposited layer of nc-Si:H. The third subgoal is to investigate the effect of different parameters, such as layer thickness and implantation energy, on the grain size of the crystals in the sacrificial polycrystalline silicon layer. The fourth subgoal is to compare the resulting textures in terms of optical performance. The fifth and final subgoal is to use these new texturing methods in the production of Silicon HeteroJunction (SHJ) solar cells and to compare the performances of these solar cells.

This thesis is set up in the following manner. Chapter 1 is designated to give the reader an

introduction in the basics of photovoltaic technologies and introduce the problem statement. Chapter 2 will provide a theoretical background for the research done in this thesis. Chapter 3 is used to discuss the equipment used to produce the crystalline silicon textures, the solar cells, and to measure the optical and electrical properties of the solar cells. In chapter 4, the results of this research will be described and discussed. The conclusions of this thesis can be found in chapter 5.

2

Theory

This chapter includes the theory needed to understand the research done in this thesis. For this purpose, a short introduction to optics is given first in section 2.1. After this, light management techniques in solar cells are discussed in section 2.2, followed by a section about charge carrier recombination, section 2.3. Then, section 2.4 is devoted to thin film silicon. This is followed by an explanation of photolithography and the different options that are available within this technology in section 2.5. After this, etching is explained in section 2.6. Finally, section 2.7 discusses the electrical properties of solar cells.

2.1. Optics

The behaviour and properties of light are studied in the field of optics. Light management is an important design parameter for solar cells. Reflection and transmission can be crucial losses in a solar cell as mentioned in section 1.4.2. Interactions between light and matter are discussed in this section.

2.1.1. Flat interfaces

The speed of light in a medium is different from its speed in vacuum. This difference is measured as the refractive index. The refractive index is defined as the ratio of the speed of light in vacuum to that in matter and usually denoted as n. The refractive index is usually bigger than 1 and not constant for different wavelengths.[20]

When light is incident on the surface of a material, a part of the light is reflected and the rest is transmitted into the material. This is shown on the left in figure 2.1. For the part of the light that is reflected, the angle of reflection θ_r is equal to the angle of incidence θ_i. The part that is transmitted is also called the refracted part. The angle of transmission θ_i is related to the angle of incidence using Snell's law:

$$n_i sin(\theta_i) = n_t sin(\theta_t) \tag{2.1}$$

Where n_i is the refractive index of the original medium in which the light propagated and n_t is the refractive index of the medium in which the light is transmitted. The fraction of light that is reflected or transmitted can be calculated using the Fresnel equations. For use of the Fresnel equations, it is important to know that light is electromagnetic radiation. This means that light is described by an oscillation in the electric and magnetic field, which are perpendicular to each other. This is shown on the right in figure 2.1. This means that the waves can have a certain orientation, which is called the polarization.[20]

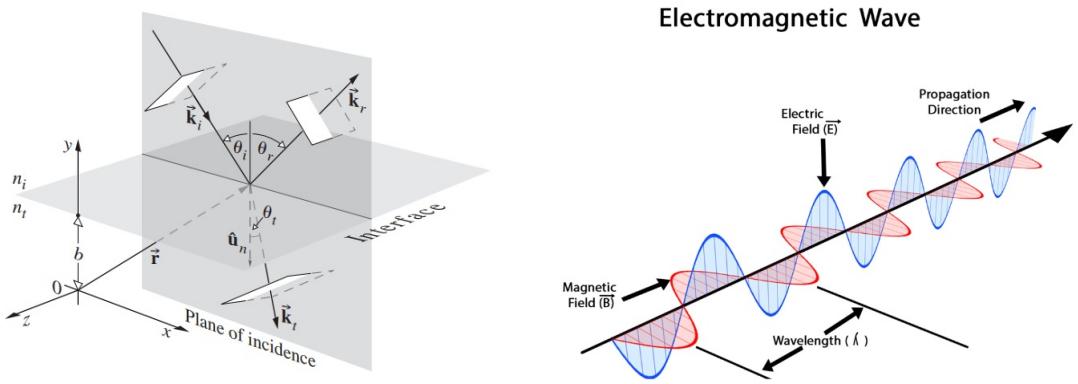


Figure 2.1: Left: Reflection and transmission of light on a flat surface.[20] Right: Propagation of electromagnetic waves.[4]

For reflection and transmission calculations, two types of light have to be distinguished: parallel and perpendicular polarized light. Parallel polarized light indicates that the light has its electric field parallel to the plane of incidence, while perpendicular polarized light indicates that the light has its electric field perpendicular to the plane of incidence. The reflectivity and transmittance are respectively the part of the incoming electromagnetic energy that is reflected and the part of the incoming electromagnetic energy that is transmitted. These parameters are dependent on the polarization. The transmittance and reflectivity derived from the Fresnel equations are as follows[20]:

$$T_{\perp} = \left(\frac{2n_i \cdot cos\theta_i}{n_i \cdot cos\theta_i + n_t \cdot cos\theta_t} \right)^2 \tag{2.2}$$

$$R_{\perp} = \left(\frac{n_i \cdot cos\theta_i - n_t \cdot cos\theta_t}{n_i \cdot cos\theta_i + n_t \cdot cos\theta_t} \right)^2 \tag{2.3}$$

$$T_{\parallel} = \left(\frac{2n_i \cdot cos\theta_i}{n_i \cdot cos\theta_t + n_t \cdot cos\theta_i} \right)^2 \tag{2.4}$$

$$R_{\parallel} = \left(\frac{n_i \cdot cos\theta_t - n_t \cdot cos\theta_i}{n_i \cdot cos\theta_t + n_t \cdot cos\theta_i} \right)^2 \tag{2.5}$$

Where $T_{\perp}$ is the transmittance of perpendicular polarized light, $R_{\perp}$ is the reflectivity of perpendicular polarized light, $T_{\parallel}$ is the transmittance of parallel polarized light and $R_{\parallel}$ is the reflectivity of parallel polarized light. It was found that for unpolarized light, such as light from the sun, the total reflectance equals half of the sum of the parallel and perpendicular polarized light reflectance.[20] This gives the next equation:

$$R_{total} = \frac{1}{2}(R_{\perp} + R_{\parallel}) \tag{2.6}$$

For normal incidence, equations 2.3, 2.5 and 2.6 can be combined and simplified to:

$$R(\theta_i = 0) = \left(\frac{n_i - n_t}{n_i + n_t} \right)^2 \tag{2.7}$$

Since the light is either transmitted or reflected, the sum of the reflectivity and transmittance should be equal to 1:

$$R + T = 1 \tag{2.8}$$

This can be used to find the transmittance for normal incident light[20]:

$$T(\theta_i = 0) = \frac{4n_1 n_2}{(n_1 + n_2)^2} \tag{2.9}$$

2.1.2. Light in absorptive media

One of the fundamentals of solar cells is that the incoming light has to be absorbed in the semiconductor material. Non-absorptive media have a real refractive index while absorptive media have a refractive index that contains a real and imaginary part, and is therefore complex:

$$\tilde{n} = n + i\kappa \tag{2.10}$$

Where n is the real and κ is the imaginary part of the refractive index. The fact that the refractive index is complex, causes the material to absorb light according to the Lambert-Beer law:

$$I(z) = I_0 exp(-\alpha z) \tag{2.11}$$

Where I is the intensity of the light as a function of the penetration depth z, I_0 is the light intensity upon entering the material and alpha is the absorption coefficient. Alpha is related to the imaginary part of the refractive index as shown in the next equation:

$$\alpha = \frac{2\pi\kappa}{\lambda_0} \tag{2.12}$$

Where λ_0 is the wavelength of the light in vacuum. This shows that the absorption is dependent on the wavelength of the incoming light since it is directly dependent on the incoming wavelength and since the complex refractive index is also dependent on the wavelength. Since a part of the light is absorbed in the medium, equation 2.8 is not valid anymore and absorption should be included. The fraction of electromagnetic energy that is absorbed (A) can be calculated using[49]:

$$R + T + A = 1 \tag{2.13}$$

2.2. Light management of solar cells

A part of the light incident of the solar cell is reflected as mentioned in section 2.1.1. Light management techniques can be used to design a solar cell with the lowest possible reflectivity. This can be done in a number of ways.

2.2.1. Absorption of semiconductors

Ideally, a solar cell absorbs all light that is incident on the surface. The Lambert-Beer law from section 2.1.2 shows that the biggest part of the electromagnetic energy of the incoming light is absorbed at the front side of the material. This is because the intensity of the light decays exponentially. The absorbed light can be calculated by subtracting the intensity transmitted through the absorber layer from the light intensity entering the absorber layer. This results in the following equation:

$$I_{abs}(d) = I_0[1 - exp(-\alpha d)] \tag{2.14}$$

Where d is the thickness of the material. Ideally, a solar cell should absorb all incoming light. These absorbers are called optically thick and have a transmittance of close to zero. Equation 2.14 shows that these layers can be achieved by either a very high thickness d, or a large absorption coefficient α. The wavelength dependent absorption coefficient of different types of semiconductor materials that are used in solar cells is shown in figure 2.2. This figure shows that compared to other absorbers, silicon has a low absorption coefficient in the visible part of the spectrum (between 300 and 700 nm). Therefore, to absorb the same fraction of light, silicon absorber layers need to be thick compared to other technologies.

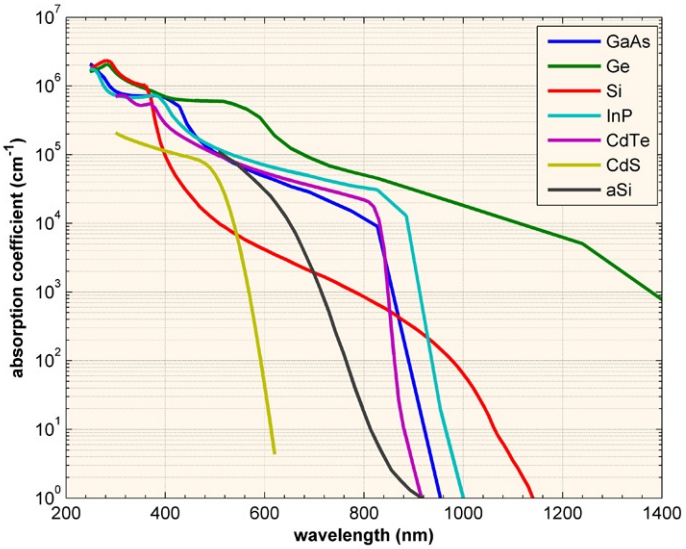


Figure 2.2: Absorption coefficient of different types of semiconductor materials that are used in solar cells.[8]

2.2.2. Light management techniques

As a result of this relatively low absorption, it is important to increase absorption by reducing reflection of the solar cell or increasing the distance light travels through the semiconductor, which is called the optical path length. These methods are light management techniques. The reflection can be reduced by implementing an anti-reflective coating (ARC). The first method of ARC uses an extra layer between air and silicon to minimize the reflection losses. Silicon has a refractive index n_s of 4.3 while air has a refractive index n_0 of 1. From equation 2.7 it can be shown that the reflectivity for an air-silicon interface is 38.8%. If a third layer is used between air and silicon with a reflective index between n_s and n_0, the reflectivity can be reduced. The reflectivity is minumum when:

$$n_l = \sqrt{n_0 n_s} \tag{2.15}$$

This results in a refractive index for the intermediate layer of n_l = 2.1. The reflectivity of the material drops from 38.8% to 22.9% when this intermediate layer is used.
The second method uses constructive and destructive interference of light. Section 2.1.1 discussed that light is considered to be an electromagnetic wave. Waves have a number of interesting properties, including interference. When two waves meet, they interfere with each other. Depending on the phase difference between the waves, this can have multiple effects. If the waves are in phase, the interference results in a wave with twice the magnitude. If the waves are 180°out of phase, the waves cancel each other. This is shown in figure 2.3.

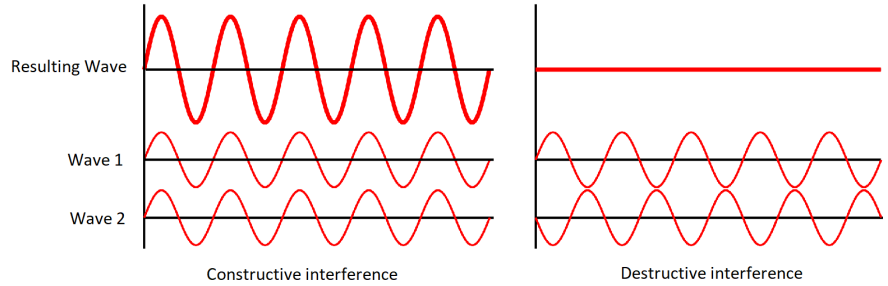


Figure 2.3: Interference of two waves. Constructive interference on the left and destructive interference on the right. Adapted from [17].

Since electromagnetic waves are still waves, they also have this property. This can be used in an anti-reflective coating by tuning the thickness of this coating. By tuning the thickness, the light rays reflected at the ARC surface and the light rays reflected at the ARC-substrate interface become 180°out of phase, which causes destructive interference. This decreases the reflection losses and therefore increases the amount of light that is transmitted into the absorber material. This is depicted in figure 2.4.

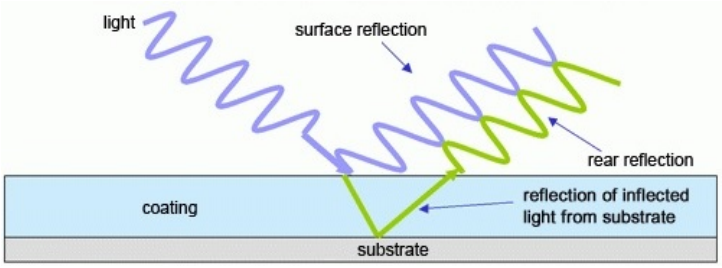


Figure 2.4: Anti-reflective coating by using destructive interference of light. Adapted from [6].

The ideal thickness of the ARC is therefore dependent on the wavelength and can be calculated using equation

$$n_l d = \frac{\lambda_0}{4} \tag{2.16}$$

Where n_l is the refractive index of the ARC, d is the thickness of the ARC and λ_0 is the wavelength of the light. This shows that the use of an ARC based on destructive interference needs a thickness in the order of the wavelength of the incoming light.
The third method makes use of a textured interface. This method uses textures that are much bigger than the wavelength of the light and therefore light is considered to be a ray and not a wave. Thus, these rays follow Snell's and Fresnel's laws which were shown in equations 2.1, 2.2. 2.3, 2.4 and 2.5. Figure 2.5 illustrates the effect of textured surfaces. For untextured surfaces, the light that is reflected of the top surface is reflected and irreversibly lost. Light that is reflected of a textured surface is incident on a new part of the surface, where it can be transmitted. This increases transmission as light has two chances of being transmitted into the surface.

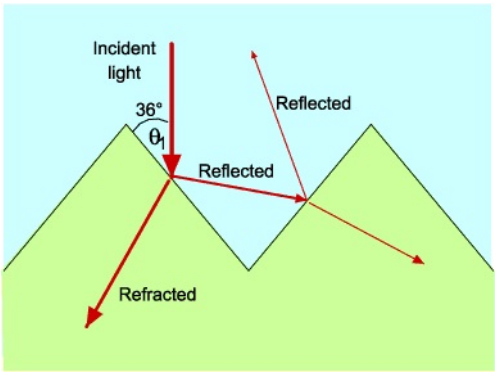


Figure 2.5: The effect of texturing illustrated.[9]

2.3. Charge carrier recombination

As mentioned in section 1.4.3, charge carrier recombination is has a big influence on the performance of a PV cell. There are three types of charge carrier recombination: direct recombination, Shockley-Read-Hall recombination and Auger recombination. Before the recombination processes can be discussed, the difference between direct and indirect bandgap materials should be distinguished.

2.3.1. Direct and indirect bandgap

The difference between a direct bandgap and an indirect bandgap can be shown with an electronic dispersion diagram. This diagram shows the energy-momentum space of electrons. An example of electronic dispersion diagrams is shown in figure 2.6. The vertical axis shows the energy state in the electronic band diagram and the horizontal axis shows the momentum of the charge carrier. The electronic dispersion diagram is different for each semiconductor. Figure 2.6 shows that an indirect bandgap material has the highest point of its valence band vertically aligned with the lowest point of its conduction band. This indicates that only energy is needed to move an electron from the valence band to the conduction band. However, an indirect bandgap material has a lowest point of the conduction band and highest point of the valence band that are not vertically aligned. This indicates that both energy and momentum are required to move an electron from the valence band to the conduction band in an indirect bandgap material. The momentum is provided by vibrations in the crystal lattice. Consequently, excitation of an electron due to photon absorption is more likely to happen in direct band gap materials than in indirect bandgap materials.

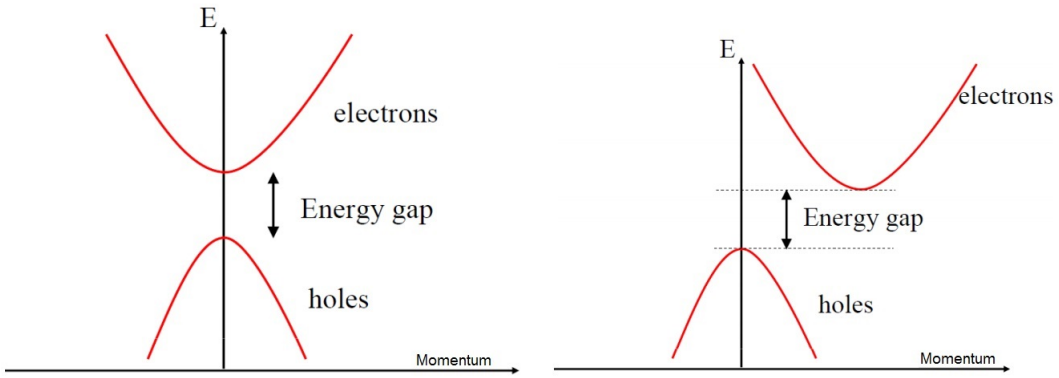


Figure 2.6: Left: Electronic dispersion diagram of a direct bandgap material. Right: Electronic dispersion diagram of a direct bandgap material. Adapted from [51].

2.3.2. Types of charge carrier recombination

There are three types of charge carrier recombination: direct recombination, Auger recombination and Shockley-Read-Hall recombination. The three recombination mechanisms are shown in figure 2.7. Direct recombination is also called radiative recombination. In direct recombination, an electron falls from the conduction band back to the valence band and emits a photon with an energy equal to the bandgap. This type of recombination is more dominant in direct bandgap materials than in indirect bandgap materials since this process also requires a momentum transfer in indirect bandgap materials. Since radiative recombination is unlikely in indirect bandgap materials, Auger recombination becomes important. Auger recombination is a three particle process, in contrast to direct recombination which is a two particle process (an electron and a hole). This type of recombination transfers energy and momentum from the recombining hole and electron to a third particle, which can be an electron or hole. If the third particle is an electron, it is excited further into the conduction band and the extra energy is released as heat when it relaxes back to the edge of the conduction band. If the third particle is a hole, this hole is excited deeper into the valence band and also releases the extra energy as heat when it relaxes back to the edge of the valence band. The third recombination process is Shockley-Read-Hall (SRH) recombination. In SRH recombination the electrons and holes do not recombine directly from bandgap to bandgap. This type of recombination is facilitated by impurity atoms and lattice defects. These impurity atoms and lattice defects introduce trap states, allowed energy levels within the forbidden energy gap. A charge carrier can get trapped in these states and recombine with a passing electron or hole. The excess energy is usually released as heat.

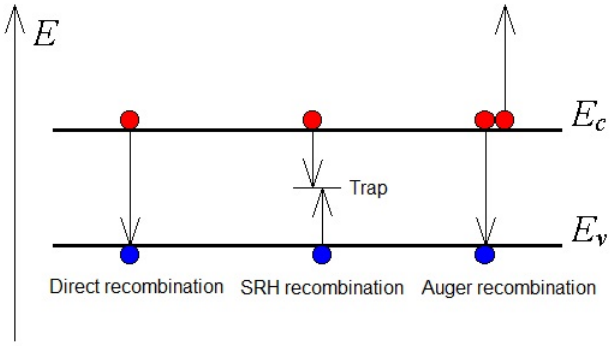


Figure 2.7: Schematic illustration of direct, Shockley-Read-Hall and Auger recombination. Adapted from [54].

2.3.3. Defects

Since SRH recombination is highly dependent on the defect density, it is desirable to keep the defect density as low as possible in the semiconductor material. There are two of different defects in silicon: dangling bonds and the incorporation of foreign atoms in the material. As mentioned in section 1.2.2, each silicon atom is connected to four other silicon atoms to form a crystal lattice in crystalline silicon. When a silicon atom is not connected to four other atoms but for example three, one valence electron is still available. This results in a dangling bond. Dangling bonds can trap charge carriers and are therefore undesirable in the material. Foreign atoms can be incorporated in the material in two different ways, either interstitial or substituted for a silicon atom. An interstitial foreign atom is not incorporated in the crystal lattice but exists in between the atoms of the lattice. These two types of defects facilitate charge carrier recombination, which decreases the lifetime of the charge carriers. A short lifetime indicates that only charge carriers that are generated close to the contacts are used for electricity generation.

2.4. Thin film silicon

As mentioned in section 1.6, this thesis will focus on monocrystalline silicon solar cells combined with thin film silicon alloys. The benefit of these technologies is that the materials are abundantly available and silicon alloys have tunable bandgaps.

2.4.1. Structure of thin film silicon

In crystalline silicon, each silicon atom is connected to four other silicon atoms to form a crystal lattice as was explained and discussed in section 1.2.2. However, the crystalline structure of silicon is not always perfect. Sometimes, the material consists of pieces of crystalline structures that do not match. These pieces are called grains. The borders of these grains contain defects and mismatches which degrades the quality of the silicon. The size of these grains define the type of crystalline silicon. Monocrystalline silicon consists of one silicon crystal and therefore has the highest quality. Multicrystalline silicon is not made of one crystal, it consists of grains larger than 1 mm. Silicon materials with grains between 1 mm and 1 µm are in the polycrystalline silicon range. Nanocrystalline or microcrystalline silicon consists of grains smaller than 1 µm. The last type of silicon is amorphous silicon. The atoms in amorphous silicon do not form a perfect crystal lattice but instead form a disordered lattice. Therefore, some silicon atoms are not bound to four other silicon atoms which results in dangling bonds, as mentioned in section 2.3.3. This is shown in figure 2.8. Dangling bonds are shown in red in this figure. Dangling bonds are undesirable and can be passivated by hydrogenation of the material. The hydrogen atoms bond to the leftover valence electron of a silicon atom with less than four bonds. This is shown in the figure as the small white dots. The atomic hydrogen content in passivated amorphous silicon is usually between 5 and 15%. Since amorphous silicon has a higher absorption coefficient in the visible part of the spectrum than crystalline silicon, as shown in figure 2.2, amorphous silicon

can be used to produce thin film silicon solar cells. Nanocrystalline silicon also possesses this higher absorption coefficient (even though it is much closer to the absorption coefficient than amorphous silicon) and is therefore also used in thin film silicon solar cells.

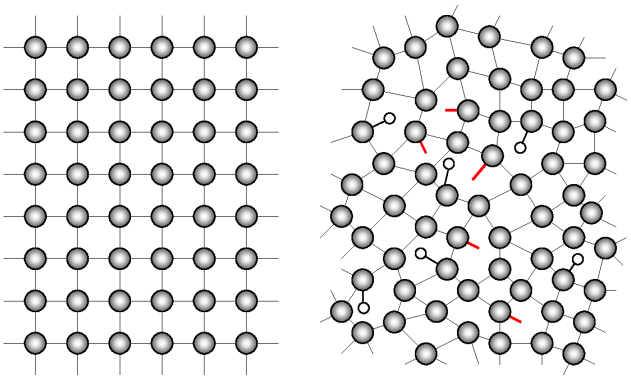


Figure 2.8: Crystalline silicon compared to amorphous silicon. Adapted from [50].

2.4.2. Characteristics of thin film silicon materials

Thin film silicon solar cells are generally made from amorphous silicon (a-Si) or nanocrystalline silicon (nc-Si). These materials can be produced using plasma enhanced chemical vapour deposition (PECVD). Nanocrystalline silicon consists of grains of crystalline silicon embedded in amorphous silicon. The crystalline structure causes the bandgap to be close to the bandgap of silicon (1.12 eV). The bandgap of amporphous silicon can be tuned between 1.6 and 1.8 eV by changing the amount of hydrogen embedded in the material. Thin film silicon has an important disadvantage. The efficiency of these solar cell degrades over time due to light exposure. This effect is called light-induced degradation (LID) or the Staebler-Wronski effect (SWE). The recombination of light-excited charge carriers causes defects in the amorphous silicon absorber layers. This increases the defect density of the material which leads to increased electron-hole recombination. Since this happens in amorphous silicon, nanocrystalline silicon is less affected by LID. The efficiency of amorphous silicon solar cells generally stabilizes around 85-90% of the initial efficiency after 1000 hours of illumination.[49]

2.4.3. Design of thin film silicon solar cells

Amorphous and nanocrystalline silicon have a high defect density compared to monocrystalline silicon. Therefore, the diffusion length of charge carriers is only between 100 and 300 nm in hydrogenated amorphous silicon, and around 1 µm in hydrogenated nanocrystalline silicon.[47] This is very small compared to the diffusion length of around 500 µm in crystalline silicon.[48] As a consequence, the transport of charge carriers in these materials can not rely solely on diffusion. Thus, amorphous and nanocrystalline silicon solar cells are based on a p-i-n junction instead of a p-n junction which is used in monocrystalline solar cells. This means that an undoped (intrinsic) layer is enclosed by a p-type layer and an n-type layer. The intrinsic layer is the main absorber and is usually several hundreds of nanometres thick while p- and n-type layers are only tens of nanometres thick. The doped layers create a built-in electric field across the undoped absorber layer. This electric field drives the charge carriers to the collectors. A schematic representation of an amorphous silicon solar cell is shown in figure 2.9. The TCO layer in this figure stands for transparent conductive oxide. The TCO layer laterally conducts the electrons from the semiconductor material to the front contacts. Since this material is at the front of the solar cell, it should not only be highly conductive but also transparent. TCO layers are usually made from aluminium doped zinc oxide (ZnO:Al) or indium tin oxide (ITO). The thickness of the TCO can be optimized to also function as an ARC.

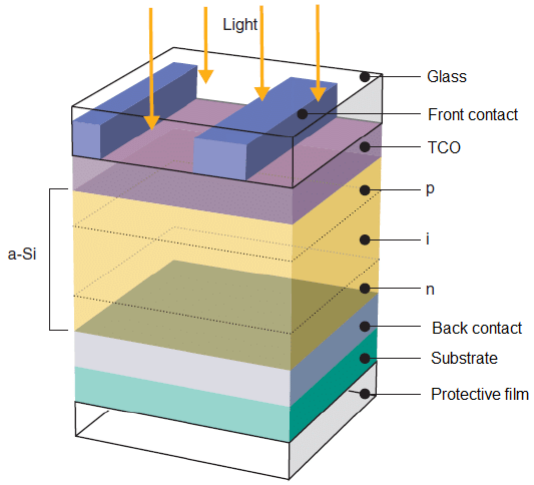


Figure 2.9: Schematic representation of an amorphous silicon solar panel. Adapted from [13].

Since amorphous silicon and nanocrystalline silicon have a different bandgap, they are often used to create thin film tandem solar cells. A tandem solar cell is a multi-junction solar cell that consists of two absorber materials. The tandem solar cell of a-Si:H and nc-Si:H, the so called micromorph cell, consists of two p-i-n junction, the top one is made of hydrogenated amorphous silicon and the bottom one consists of hydrogenated nanocrystalline silicon. If an electron-hole pair is formed in the top absorber layer of amorphous silicon, the hole moves to the p-type, which is located at the front contact of the device, and the electrons move to the n-type layer. The same happens in the bottom layer of nanocrystalline silicon. The generated hole in the a-Si:H and the electron from the nc-Si:H are respectively collected at the front and back contact. The electron generated in the a-Si:H and the hole generated in the nc-Si:H meet at the interface between the amorphous silicon and nanocrystalline silicon. To stimulate the recombination, a thin and defect-rich layer can be used between the a-Si:H and nc-Si:H.

2.5. Photolithography

Photolithography uses a light sensitive polymer to produce patterns. In the case of semiconductor lithography, these patterns are usually made on silicon wafers. Photolithography is mainly used for the fabrication of integrated circuits such as chips. Photolithography is used to build the complex structures of transistors and to connect these transistors to form a chip. The light sensitive polymer used in photolithography is called the photoresist. Before the photoresist can be deposited on the substrate, the substrate needs to be prepared first.[32]

2.5.1. Substrate preparation

Substrate preparation is done by using a number of the following processes: cleaning of the substrate to remove contamination, removing water by a dehydration bake, and use of an adhesion promoter. The substrate can be contaminated by particles or a film. Particles can cause defects in the final pattern and usually originate from airborne particles. Both particles and films can be organic and inorganic. To remove these particles, chemical or mechanical cleaning can be used. Oils and polymers are organic materials that can create films on the material and can originate from machinery or body oils. These films can cause adhesion of the photoresist to be poor. They can be removed by chemical, ozone and plasma stripping. Chemical and plasma stripping can also be used to remove inorganic films. A dehydration bake can be used to remove absorbed water from the substrate. A dehydration bake removes water from the substrate by warming it to temperatures of 200-400 °C for 30-60 minutes. After this, the substrate is cooled in a dry environment. A dehydration bake usually does not remove all water from the surface. The silicon atoms at the surface bond strongly with a

monolayer of water. This forms silanol groups (SiOH). This layer could be removed by a bake above 600°C or by chemical means. The silanol groups are used by adhesion promoters. These promoters react with the silanol and replace the hydroxyl group with an organic group that adheres to the used photoresist. Usually, silanes are used as an adhesion promoter, specifically hexamethyl disilizane. The adhesion promoter is usually applied by subjecting the substrate to a vapor containing the promoter at elevated temperatures and at reduces pressure. After the substrate is cleaned, dehydration baked and/or and adhesion promoter is applied, the photoresist coating can be applied.[32]

2.5.2. Photoresist coating

The photoresist coating is applied using either spin coating or spray coating to obtain a thin, uniform coating of which the thickness can be controlled. The photoresist is dissolved in in a solvent. Solvent and photoresist are then poured or sprayed onto the wafer, which is spinning on a turntable at high speed in order to obtain the desired thin, uniform coating. A large number of parameters influence the thickness and uniformity of the photoresist coating, spinning speeds and times for example. The variation of thickness and uniformity of the photoresist with the process parameters have to be determined experimentally.
After the spin or spray coating, the photoresist film contains 20-40% solvent. This solvent can be removed by a softbake. If the solvent is not removed, it will gradually evaporate if it is kept at room temperature, which changes the properties of the film over time. After the softbake, most of the solvent is evaporated and the coating becomes stable at room temperature. However, removing the film does have some effects. First of all, the thickness of the film is reduced. Secondly, the adhesion is improved. Finally, the film becomes less sensitive to contamination. However, there are some negative side effects to baking the photoresist. If the temperature is greater than 70°C, some of the components of the photoresist begin to decompose or oxidize. This degrades the quality of the photoresist. Therefore it is important to search for optimum softbake conditions that maximize the benefits of the solvent removal and keep the decomposition of the film at a minimum. This bake used to be done in an oven during the 1970s. Currently, the hot plate method is widely used due to its short bake time. With this method, the wafer is brought into contact with or in close proximity to a hot plate made from high-mass metal. Silicon has a high thermal conductivity which allows the photoresist to rise to high temperatures quickly. After the hotplate process, the wafer is still hot and therefore the baking continues. Consequently, the temperature of the wafer should be controlled. Hence, the wafer is usually cooled by bringing it close to a cool plate. When the wafer is back to room temperature, the photoresist is ready for the lithographic exposure. [32]

2.5.3. Alignment and lithographic exposure

Photolithography is possible due to a change in the solubility of the photoresist upon exposure to light or other types of radiation. For a standard positive photoresist, the photoactive compound is not soluble in the developer before exposure to UV light. During exposure, the photoresist is converted to carboxylic acid which is soluble in the used developer. There are three methods for photolithographic exposure: contact, proximity and projection lithography. A schematic representation of these methods is shown in figure 2.10.

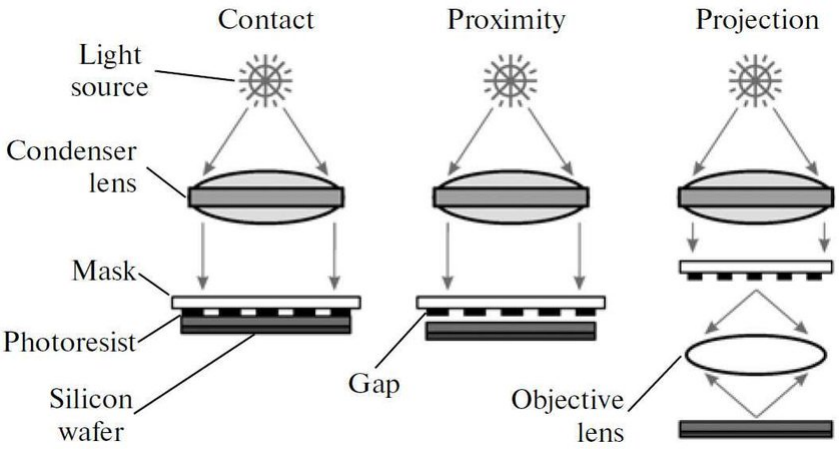


Figure 2.10: Methods for lithographic exposure.[18]

With contact lithography, the mask is placed in contact with the photoresist. This offers a high resolution of about the radiation wavelength. Unfortunately, some practical problems arise when using this technique such as damage and contamination of the wafer. This damage can be reduced by using proximity printing. The mask is kept at a distance above the wafer of approximately 20 μm. This method does decrease the resolution to greater than 2 μm. This resolution is too big for current technologies and therefore a third technique was developed, projection photolithography. This method uses a lens to project an image of the mask onto the wafer. Projection photolithography can be divided into two classes: the scanning method and the step-and-repeat method. Scanning projection photolithography uses mirrors to project a slit of radiation while the mask and wafer are moved simultaneously under the slit and are therefore irradiated. The radiation dose is determined by the light intensity, the width of the slit and the scanning speed. The mask and image size are equal while using this method. The step-and-repeat method uses lenses to expose one rectangular section of a wafer at a time. The wafer is then moved and a different section is exposed. This method can have an identical mask and image size or reduction of the image size. Therefore, this method can have a better resolution than the scanning method and can create feature sizes of 250 nm. The technology of choice today for the smallest resolution is a combination of the scanning method and the step-and-repeat method. This method can create features of below 250 nm.[32]

2.5.4. Resolution

The smallest printable feature is called the resolution. The resolution has two basic limits: the smallest projection that can be made on the wafer and the solubility of the photoresist. The resolution of projection imaging is determined by both the numerical aperture of the projection lens and the wavelength of the used light. The resolution follows the Rayleigh criterion:

$$R \propto \frac{\lambda}{NA} \tag{2.17}$$

Where R is the resolution, λ is the wavelength and NA is the numerical aperture of the lens. This indicates that the use of a smaller wavelength results in a better resolution. As the resolution is becoming smaller, one effect is becoming more dominant: the standing wave effect. This effect is caused by monochromatic light travelling through the photoresist, being reflected by the substrate and travelling back up through the photoresist. This caused interference with the incoming light, which creates a standing wave pattern in the photoresist. This wave pattern can be reduced by doing a post-exposure bake of between 100 and 300 °C. This causes diffusion in the photoresist layer which smoothens out the standing wave pattern in the resist.[32]

2.5.5. Development

After light exposure, the photoresist has to be developed. Development is the most important and critical step in this photolithography process. Usually, an aqueous base is used as a developer, tetramethyl ammonium hydroxide (TMAH) for instance. There are different methods for applying the developer. Which method is used is important for controlling both the uniformity and process latitude. The methods are: batch development, spin development, spray development and puddle development. Batch development was the most predominant method in the early stages of photolithography. This method develops between 10 and 20 wafers simultaneously in a large beaker. Currently, in-line techniques are more dominant since these techniques can be used in modern factories. The process of spin development is quite similar to the spin coating technique that was mentioned in the coating subchapter. The wafer is spun and the developer is poured onto the wafer. Rinsing and drying of the wafer is also done while spinning. Spray development shows good results when developers are used that are specifically made for this method. This process is similar to spin development but rather than poured, the developer is sprayed onto the wafer by a nozzle. This method uses less developer and also produces a developer coverage that is more uniform. The final in-line development method is puddle development. The development is again specifically made for this process. The wafer is kept stationary and the developer is poured onto the wafer. The developer is then kept motionless on the wafer for the entire development time. After this, the wafer is rinsed and dried. These techniques are frequently combined since the used equipment is very similar.
After the development, the remaining photoresist is hardened using a postbake so it can withstand ion implantation and etching. The temperature is relatively high during this bake, between 120 and 150 °C, in order to crosslink the resin polymer in the resist. This crosslinking makes the photoresist more thermally stable. This bake can also remove water, residual solvent and gasses in the resist. Also, it usually improves the adhesion between the photoresist and the substrate. Another way to harden the remaining photoresist is exposure to high intensity deep-UV light. This causes crosslinks in the resin polymer in the resist. Photoresist that is hardened by deep-UV light can withstand temperatures above 200 °C.[32]

2.5.6. Pattern transfer

Now that the pattern is printed in the photoresist layer, it can be transferred to the substrate. This can be done using three methods. The first method is subtractive transfer, which is also called etching. Etching is also the most common method. Usually, the material to be patterned is deposited on the wafer or substrate as a uniform layer before photolithography. During photolithography, the photoresist is patterned in such a way that the areas that should be etched are left exposed. Two types of etching are used: wet etching and dry etching. Wet etching uses wet chemicals such as bases and acids. Dry etching uses a plasma environment to do the etching. These techniques will be further discussed in section 2.6 The photoresist protects the covered material while etching. After the etching is done, the photoresist is removed and the desired pattern is left in the active material. The second method is additive transfer, which is also called selective deposition. This method is used when the metal interconnections are made. Photolithography is used to free the areas where the metal layer should be grown. When the resist is stripped, it leaves the new material in the places where the active material is unprotected by the photoresist. The third and final method is impurity doping by ion implantation. This method adds controlled amounts of contaminants to the active material. The conductive properties of a semiconductor are changed when dopant atoms are added. After creating a photoresist layer, this method accelerates a beam of dopant ions at the substrate. The ions are embedded in the unprotected areas while the ions are blocked by the photoresist in the covered areas. This creates doped regions, which are essential for transistors.[32]

2.5.7. Stripping the photoresist

After processing, the remaining resist has to be removed. This stripping can be done using two techniques: wet stripping and dry stripping. Wet stripping is done by using inorganic or organic solutions. Acetone can be used as an organic stripper but this has a disadvantage,

namely that it leaves residues on the wafer and therefore it cannot be used for semiconductor processing. Inorganic acid-based solutions are usually used for positive photoresists. These strippers are used at elevated levels. The problem with wet stripping is that it is almost impossible to strip the last monolayer of resist from the wafer using this technique. Therefore, plasma stripping is needed to remove this final layer. Also, if deep-UV hardening or ion implantation were used on the resist, the wet stripping method can be unable to remove the resist. Consequently, plasma stripping is currently the universally used method. An oxygen plasma can easily react with organic polymers and leaves the inorganic materials untouched. After the photoresist is stripped, the photolithography process is done.[32]

2.6. Etching

As mentioned in section 2.5.6, the photolithographic process is used to transfer a pattern onto a substrate. This will be done in this research using etching. As mentioned in section 2.5.6, there are two types of etching, wet etching and dry etching.

2.6.1. Wet etching

Wet etching is a technique that uses liquid chemicals to remove materials from a wafer. This material is in this case silicon. To etch a specific pattern into the wafer, a photoresist can be used as a mask. There are two types of wet etching, anisotropic wet etching and isotropic wet etching. Some liquid etchants have a different etch rate depending on the crystal face of the structure. These etchants are called anisotropic etchants. The result of anisotropic wet etching is shown in figure 2.11 on the left and in the centre. For silicon, commonly used anisotropic wet etchants are potassium hydroxide (KOH), ethylenediamine pyrocatechol (EDP) and tetramethylammonium hydroxide (TMAH). If an (100) silicon wafer is etched with these materials, the result is a pyramid shaped structure of which the walls have an angle to the surface of 54.7°. This technique can be used to create pyramid structures to decrease light reflection as was shown in section 2.2.2. Isotropic wet etching etches all crystal faces with the same etch rate. This results in shapes as shown on the right in figure 2.11. Usually, a mixture of hydrofluoric acid, nitric acid and acetic acid is used for isotropic wet etching. The etch rate can be influenced by tuning the concentrations of the three etchants. Silicon nitride or silicon dioxide are commonly used as masks.[41]

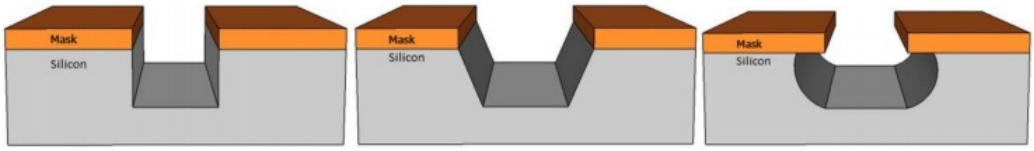


Figure 2.11: Left: Completely anisotropic wet etching. Centre: Partially anisotropic wet etching. Right: Isotropic wet etching.[41]

2.6.2. Dry etching

Dry etching uses plasmas or etchant gasses to remove the undesired material. This type of etching uses high kinetic energy of particle beams, a chemical reaction or a combination of the two. There are three types of dry etching: physical dry etching, chemical dry etching and reactive ion etching.

Physical dry etching utilizes high kinetic energy beams to etch the undesired atoms. These beams can consist of ions, electrons or photons. The high energy particles knock out the undesired atoms which then evaporate. There is no chemical reaction in this process so only the unmasked material is removed.

Chemical dry etching is based on a chemical reaction between the used etchant gasses and the silicon surface. The etchant gasses react with the surface to remove the silicon from the surface. This process is usually isotropic and has a high material selectivity. Some gasses that are used as etchants are tetrafluoromethane (CH_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), chlorine gas (Cl_2), or fluorine (F_2). Anisotropic dry etching can be used to etch with finer resolution than isotropic dry etching.

Reactive ion etching combines the techniques of physical and chemical dry etching. By combining these techniques, even higher resolutions can be obtained while using a much faster etch rate. Therefore, this technique is most widely used, both for industry and research purposes. Reactive ion etching accelerates reactive gasses which are used to bombard the target silicon. Commonly used gasses are CF_4 and SF_6.[41]

2.7. Electrical properties of solar cells

The electrical properties of a solar cell are critical since they govern the performance of a solar cell. The photon-excited charge carriers can only generate power if they are collected. A high conductivity is therefore a must in a solar cell.

2.7.1. Ohm's law and resistivity

A solar cell produces electrons that move through an external circuit and deliver work. The flow of charge, in this case electrons with each a charge of $1.602 \cdot 10^{-19}$ coulomb, creates a current. Current (I) is defined as the net charge crossing an area and is expressed in Ampère (A). Therefore, the electric current is directly related to the amount of electrons flowing through the external circuit. Every object has a certain resistance (R). This resistance indicates how much the flow of charge is resisted by the object and is expressed in Ω. Metals have a low resistance due to the fact that they have free electrons at room temperature, as was explained in section 1.2.1. This section also explains that insulators have electrons that are very tightly bound to their nucleus, which causes a high resistance. If a potential difference (voltage) is applied over an object, the resulting current can be found by using Ohm's law:

$$I = \frac{V}{R} \tag{2.18}$$

Ohm's law indicates that a given voltage results in a larger current if the resistance becomes smaller. The resistance of an object can be calculated using the resistivity ρ. The resistivity is material dependent and has the unit $\Omega \cdot m$. The resistance of an object can be approximated using:

$$R = \frac{\rho L}{A} \tag{2.19}$$

Where L is the length of the object and A is the area of the object. The resistance of an object can also be calculated by using the conductivity. The conductivity is the inverse of the resistivity and is a measure of how easy charge carriers can flow through a material. Conductivity is measured in Siemens.[43] For solar cells it is important to have a large conductivity since the photon-excited charge carriers should be able to reach the contacts to be collected.

2.7.2. Solar cell parameters

The performance of solar cells is characterized by four parameters: the peak power P_{max}, the short circuit current density J_{sc}, the open circuit voltage V_{oc} and the fill factor FF. The efficiency of a solar cell η can be determined from these parameters. In order to compare different solar cells, certain standard conditions are used in the whole solar cell industry. These conditions are called the standard test conditions (STC). The STC are: an irradiance of 1000 Wm^{-2}, the spectrum should resemble the AM1.5 spectrum and the cell temperature should be constant at 25 °C. The peak power is the maximum power that a certain device generates at STC. The short circuit current density is the current that flows through the circuit when the solar cell is short circuited, divided by the area of the solar cell. The short circuit current density is the maximum current that can be delivered by one square meter (or square centimeter) of the specific solar cell. Similar to the current density, the voltage of a solar cell also has a maximum, which is the open circuit voltage. The open circuit voltage is the potential difference between the two electrodes of the solar cell when no load is connected. When a load is attached to an illuminated solar cell, a current will start to flow through the circuit. This current is dependent on the resistance of the load as shown in equation 2.18.

An I-V curve can be constructed by using different load resistances. A typical I-V curve is shown in figure 2.12.

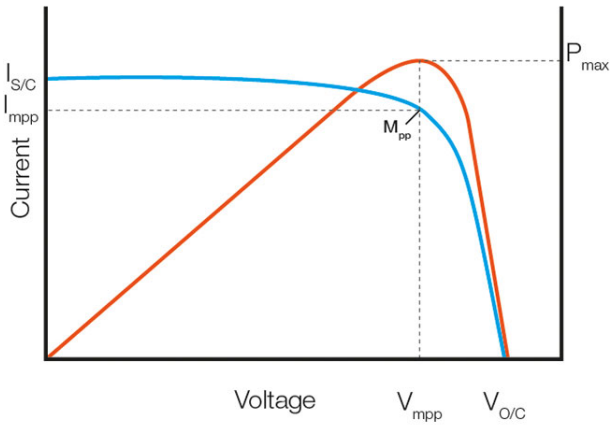


Figure 2.12: Typical I-V and P-V curves of a solar cell.[53]

This figure also shows the power generation at different voltages. This power is calculated by multiplying the voltage and current, as shown in equation 2.20.

$$P = V \cdot I \tag{2.20}$$

Where P is the power, V is the voltage and I is the current. As shown in figure 2.12, the generated power by the solar cell has a maximum. This maximum is usually called the maximum power point (MPP). The maximum power point has a corresponding voltage (V_{MPP}) and current (I_{MPP}). As mentioned before, the solar cell has a maximum voltage (V_{OC}) and maximum current (I_{SC}) it can produce. Therefore, the theoretical maximum power of the device can be found by multiplying these parameters, as is shown in equation 2.20. The fill factor is defined as the ratio between the actual maximum power divided by the theoretical maximum power. This is shown in equation 2.21.

$$FF = \frac{P_{MPP}}{V_{OC} \cdot I_{SC}} \tag{2.21}$$

The efficiency of the solar cell is defined as the ratio between the power of the incident light and the maximum power produced by the solar cell. This is shown in equation 2.22.

$$\eta = \frac{P_{MPP}}{P_{in}} \tag{2.22}$$

Using the definition of the fill factor in equation 2.21, equation 2.22 can be rewritten as:

$$\eta = \frac{FF \cdot V_{OC} \cdot I_{SC}}{P_{in}} \tag{2.23}$$

Ideally, a fill factor of 1 is desired for a solar cell. In this case, the maximum theoretical power is produced by the solar cell, which is the multiplication of the open circuit voltage and the short circuit current. There are two parameters that prohibit this: the series resistance (R_S) and the shunt resistance (R_{SH}). Since a solar cell is a non-perfect conductor, the device has an internal resistance which is called the series resistance. The effect of the series resistance on the I-V curve is shown in figure 2.13 on the left. This figure shows that an increasing series resistance has a negative influence on the I-V curve and therefore also on the P-V curve. The other parameter, the shunt resistance, can be used as an indication of the current leakage within the PV device. A high shunt resistance indicates a low level of current leakage, which is desirable for the PV device. The effect of the shunt resistance on the I-V curve of a solar cell is shown in figure 2.13 on the right. This shows that a decreasing shunt resistance has a

negative effect on the I-V curve and therefore also on the P-V curve and the maximum power the solar cell can produce.

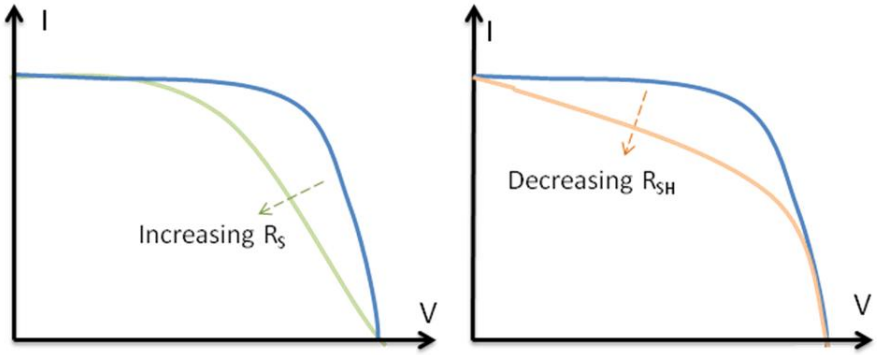


Figure 2.13: Left: The effect of the series resistance. Right: The effect of the shunt resistance.[25]

The final important solar cell parameter is the external quantum efficiency (EQE). The EQE is the fraction of incident photons that create electron-hole pairs in the semiconductor which are then successfully collected. The EQE is measured as a function of the wavelength since it is wavelength dependent. It is measured by illuminating the PV cell with monochromatic light of a certain wavelength while measuring the photocurrent produced by the solar cell. Ideally, the EQE would be 1 for all wavelengths. The EQE curve is a useful tool that provides insight in optical and electrical losses in the solar cell. Some examples of these losses are: parasitic absorption losses, recombination losses, transmission losses and losses due to reflectivity.

3

Methodology

This chapter contains information on the equipment used during this project. This includes equipment for the fabrication and measurement of the photovoltaic devices. The first type of texturization of the photovoltaic device will be done using photolithography. Therefore, section 3.1 will consist of an explanation of the equipment used for the photolithography and etching process, followed by a detailed description of the creation of this hexagonal texture. The second type of texturization uses a sacrificial layer of polycrystalline silicon. This layer is created using Low Pressure Chemical Vapour Deposition (LPCVD), ion implantation and high temperature annealing. Therefore, these techniques will be explained followed by a flowchart for the creation of this texture in section 3.2. After this, the techniques used for the manufacturing of the solar cells are explained in section 3.3. This includes the plasma enhanced chemical vapour deposition (PECVD) setup, to produce the different layers of the photovoltaic cell, and the Physical Vapour Deposition (PVD) setup, which is used to create metal contacts of the solar cell. Next, the measurement equipment is explained in section 3.4, starting with Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM), which were used to image the textured surfaces. Afterwards, the reflectance measurement setup is explained, which was used to compare the reflectance of the created textures. This is followed by the measurement setups that are designed to measure the photovoltaic device parameters. These parameters were explained in the previous chapter, section 2.7.2.

3.1. Photolithography

This section is dedicated to the equipment and methods that are used for the photolithography process. An overview of the options available for photolithography was given in section 2.5. The photolithography equipment used in this research is located in the cleanroom 100 of the Else Kooi laboratory in Delft. The class 100 indicates the allowed number of particles with a diameter of greater than 0.5 µm per cubic foot.

3.1.1. Cleaning

Multiple wafer cleaning steps are performed during both the photolithography process and the sacrificial layer method. Cleaning is done to remove any organic contamination and metal contamination that could be present on the wafer. Therefore, this cleaning method is explained first. Wafer cleaning is done in two steps. The first step of this cleaning is a ten minute 99% nitric acid (HNO_3) bath at room temperature to remove the organic contamination. This is followed by a five minute DI water bath to remove the acid from the wafers. After this, the metals are removed using a bath of 69.5 % HNO_3 at a temperature of 110 °C, also for ten minutes. This is again followed by a five minute bath in DI water to remove the acid, after which the wafers are rinsed and dried in an Avenger Ultra-Pure 6 Rinser/Dryer. This concludes the cleaning step.

3.1.2. Coating/developing

Coating and developing of the photoresist is done in the EVG120 Coater-Developer, located in the cleanroom 100 of the Else Kooi Laboratory (EKL). This machine can simultaneously coat wafers with photoresist, and develop wafers after lithographic exposure. Up to 25 wafers can be inserted in the machine for coating. The same number of wafers can be simultaneously inserted for development. This machine offers a positive photoresist as a standard while other photoresists can be added upon request. It is equipt with hexamethyl disilizane (HMDS) chambers, which are used to promote adhesion between the wafer and the photoresist. The HMDS is supplied using nitrogen as a carrier gas. The standard photoresist is the Shipley SPR3012 positive resist, which is applied using spin coating. Development of the photoresist is done in this machine using puddle development with the Shipley MF322 developer. This can be done using one or multiple repetitions of the puddle development, depending on the thickness of the resist. The coater-developer is equiped with hot- and coolplates. The hotplates are used for the soft bake after coating, for the post-exposure bake, and for the hard bake after development. The coolplates are used to bring the wafer temperature back to room temperature.

3.1.3. Lithographic exposure and mask design

The lithographic exposure is done on an ASML PAS5500/80 automatic wafer stepper. This machine uses the step-and-repeat projection method, which was explained in section 2.5.3. The resolution of this machine is approximately 0.4 µm. The image that this machine makes of the mask on the wafer has a reduction of 5.

The texturization of the crystalline silicon using photolithography can be designed in any way desirable. The only limitation is the resolution of the machine that is used. In this research, a hexagonal texture was chosen, which is shown in figure 3.2. This texture was chosen since it was used in the world record efficiency, single-junction µc-Si:H solar cell reported by Sai et al. [46]. This texture has two parameters that can be changed: the height difference between the corner of the hexagon and the centre (H), and the period of the texture (P). Also, the aspect ratio is defined as the ratio between the peak height H and the period of the textured substrate P, This is shown in equation 3.1. Earlier work by Manea et al. [33] showed that an aspect ratio of around 0.25 is desired in hexagonally textured back reflectors for thin film microcrystalline solar cells.

$$Aspect\ ratio = \frac{H}{P} \tag{3.1}$$

This hexagonal texture is made by photolithography. The mask used in this photolithograpy process has small holes that are uniformly spaced in the vertexes of an equilateral triangle, as shown in figure 3.1. This figure also shows an approximation of the resulting hexagonal texture in red.

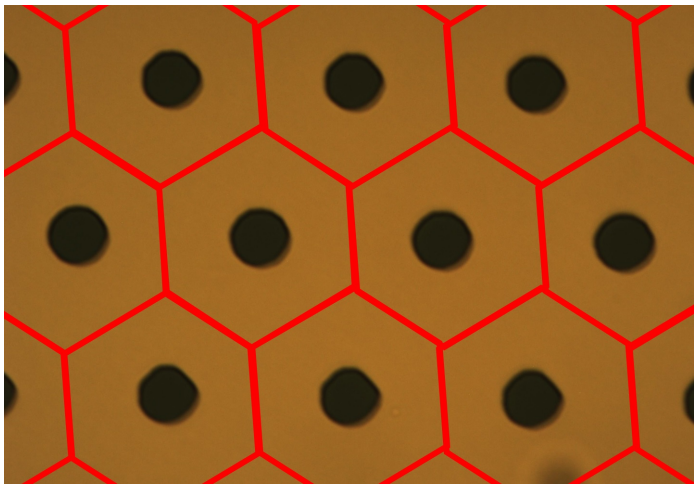


Figure 3.1: Mask used for photolithography. The red overlay shows an approximation of the resulting hexagonal texture.

Two parameters can be tuned in this mask, the distance between the holes (the period) and the size of the holes. It was shown by Sai et al. [45] that the photocurrent density delivered by the thin film microcrystalline silicon is maximized if the period of the texture is about 0.5 micrometer larger than the thin film microcrystalline silicon layer that is deposited on top of the textured silicon. Since this layer will be between 2.5 and 3 micrometer, the optimum texturing period should be between 3 and 3.5 micrometer. Figure 3.2 shows an example of a honeycomb structured silicon dioxide substrate. Since an aspect ratio of 0.25 is desired as mentioned before, the height difference between the lowest point (the centre of a hexagon) and the highest point (the corners of the hexagon) should be a quarter of the period. The hole size can be tuned to obtain this desired height. An isotropic etchant is used which etches the material in all directions at an equal rate. This indicates that the texture depth is equal to the length that should be etched sideways before creating a corner of the hexagon. This can be used to show that the pattern height will be equal to the distance from the centre of the hexagon to the corner minus the radius of the hole. The distance from the centre of a hexagon to the corner of the hexagon can be mathematically proven to be $\frac{P}{\sqrt{3}}$. The hole radius can therefore be found by using equation 3.2.

$$R = \frac{P}{\sqrt{3}} - H \tag{3.2}$$

Where R is the radius of the hole, P is the texturing period and H is the height. Since the ideal height is equal to a quarter of the texturing period, equation 3.2 can be simplified to

$$R = \left(\frac{1}{\sqrt{3}} - \frac{1}{4}\right) \cdot P \tag{3.3}$$

For a texturing period between 3 and 3.5 micrometer, the hole radius should be between 0.98 and 1.15 micrometer.

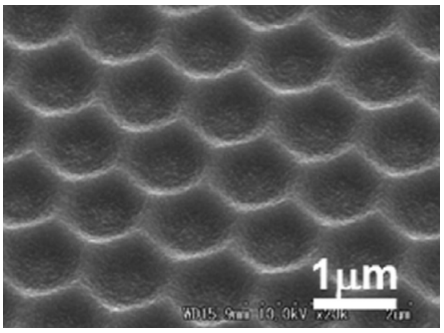


Figure 3.2: Scanning electron microscopy image of a textured silicon dioxide surface.[44]

3.1.4. Photolithography process

This section is dedicated to give a detailed description of the photolithography process. The photolithography process starts with cleaning the wafers as explained in section 3.1.1 to remove any organic contamination and metal contamination. A schematic overview of the process after cleaning is shown in figure 3.3.

After cleaning, a 300 nm layer of silicon dioxide is created. This layer is used as a mask for etching since the acids used for the isotropic etching of crystalline silicon are known to attack the photoresist, but the rate of photoresist removal is unknown. Therefore, the photoresist cannot be used as a mask for this etching step so silicon dioxide is used, since the etch rate of these acids for silicon dioxide is known. The silicon dioxide is created by oxidizing the top layer of silicon using water. This is done at a temperature of 1100 °C. Since water is used instead of oxygen, this process is called wet oxidation.

After oxidation, the wafers are coated with photoresist. This process starts with an HMDS treatment. After, an 1.4 µm layer of the standard positive resist is applied. This is followed by a a soft bake at 95 °C for 90 seconds to remove the solvent present in the photoresist.

After coating, the lithographic exposure is done. The masks that were used for this exposure

were designed as explained in section 3.1.3. In short, the mask used in this photolithograpy process has small holes that are uniformly spaced in the vertexes of an equilateral triangle. Two parameters can be tuned in this mask, the distance between the holes (the period) and the size of the holes. The original tests were done using two masks, both with a hole diameter of 5 µm. The difference is in the period. The first mask has a period of 10 µm while the second has a period of 15 µm. Since the automatic wafer stepper uses the step-and-repeat projection method, the image projected on the wafer is a 5 times reduction. This results in a hole diameter of 1 µm and a period of 2 or 3 µm. The mask with a period of 2 µm will hereafter be referred to as mask 1, while the mask with the period of 3 µm will be referred to as mask 2.

After the exposure, the photoresist needs to be developed immediately. Since a positive photoresist is used, the irradiated areas are removed during development. The development starts with a post-exposure bake at 115 °C for 90 seconds. This is done to reduce the standing wave pattern that results from interference of incoming and reflected light, which was explained in section 2.5.4. Then, the developer is poured onto the wafer in a single puddle process. This is followed by a hard bake at 100 °C for 90 seconds to harden the photoresist and improve the adhesion to the wafer.

When the development is done, the pattern created in the photoresist needs to be transferred to the layer of silicon dioxide. This is done by etching the oxide through the holes of the photoresist. The etching is done in two steps. The first step is a bath of H2O/Triton X-100. This bath contains 1 ml Triton X-100 per 5000 ml deionized water. Triton X-100 is used to help the acids reach into the small holes of the photoresist. The second step is a bath of Buffered HydroFluoric acid 1:7 (BHF 1:7), which is also known as Buffered Oxide Etch (BOE). BHF etches thermally created oxide at a rate between 75 and 90 nm/minute. Therefore, the etch time should be at least four minutes. To be sure the holes are etched in the oxide, the etch time is increased by 30 seconds to a total of four minutes and 30 seconds. Afterwards, the acid is removed by rinsing the wafers with DI water in a Quick Dump Rinser and dried using an Avenger Ultra-Pure 6 Rinser/Dryer.

Now that the pattern created in the photoresist is transferred to the silicon dioxide layer, the photoresist can be removed. This is done using a bath of acetone at 40 °C. The acetone removes the photoresist in 1 minute, after which the wafers are taken from the bath slowly. The wafers are then left to rest in the wetbench for 5 minutes so the acetone evaporates completely. This is done because acetone mixed with HNO_3 creates an exothermal reaction that can lead to an explosion.

The wafers are then cleaned to remove the leftovers of the photoresist from the wafers.

Now that the silicon oxide etching mask is created and the photoresist is removed, the crystalline silicon can be etched through the mask. This is done in the cleanroom of EKL using an etch called ”poly-Silicon etch”. This is an isotropic etch that is mainly used for etching polycrystalline silicon. It consists of nitric acid, hydrofluoric acid and DI water in the following concentrations: $HNO_3(69.5\%) : HF(40\%) : H_2O$ $525 : 15 : 210$. This solution is known to have an etch rate of about 9 nm/min for silicon dioxide, so the mask of 300 nm can be used for about 30 minutes. The etch rate of crystalline silicon was estimated to be around 100 nm/min but this was never measured. Therefore, the etch time was found experimentally. This is shown in section 4.1.1.

After etching the crystalline silicon, some silicon dioxide might still be present on the wafer. This is removed using a bath of BHF 1:7. The etch time is again four minutes and 30 seconds to make sure that all silicon oxide is removed. This concludes the photolithography process for creating a hexagonal structure in crystalline silicon.

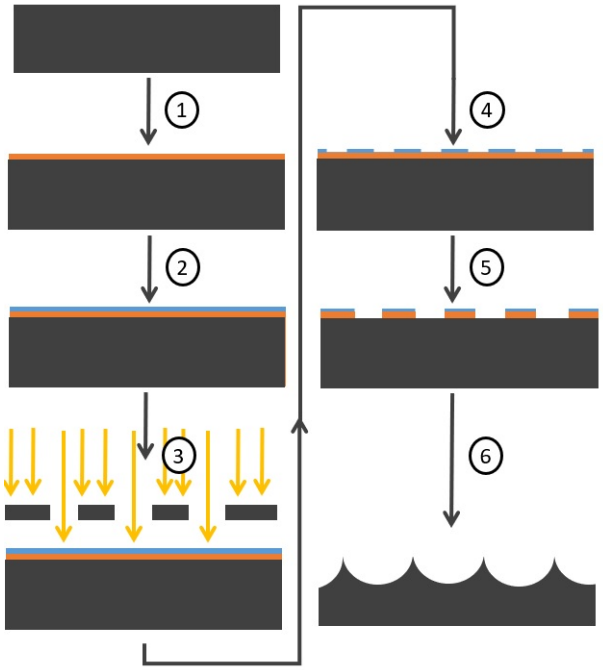


Figure 3.3: Schematic representation of the photolithography process. Step 1, create 300 nm of silicon dioxide on crystalline silicon wafer. Step 2, add photoresist. Step 3, Lithographic exposure. Step 4, photoresist development. Step 5, pattern transfer to silicon dioxide. Step 6, photoresist removal and isotropic etch.

3.2. Sacrificial layer

The sacrificial layer process uses a layer of polycrystalline silicon to create a random texture in crystalline silicon. This is done by etching this layer of polycrystalline silicon using an isotropic etch which leaves craters in the crystalline silicon located underneath the polycrystalline silicon layer. This section describes the equipment used for this method and gives a flowchart of this process.

3.2.1. Marangoni drying

When silicon is exposed to oxygen, the top layer oxidizes. This layer of silicon dioxide is between 0.2 and 0.8 nm thick for n-type silicon in air, depending on the exposure time.[37] This layer can be removed using the Marangoni drying setup in the cleanroom 100 of EKL. Six wafers can be loaded into this setup. The method starts by filling the bath with 0.55 % HF. This solution is used to remove the native oxide from the wafer, which takes 4 minutes. Afterwards, the wafers are rinsed using DI water, also for 4 minutes. While the wafers are rinsing, Isopropyl alcohol (IPA) carried by nitrogen vapour is led along the water surface. This causes the IPA to dissolve into the water which creates a gradient in the surface tension of the water film on the wafers. This causes the water to drain backwards into the bath when the wafers are slowly removed.[29] The result is that the wafers emerge completely dry from the DI water bath.

3.2.2. Low pressure chemical vapour deposition

Low Pressure Chemical Vapour Deposition (LPCVD) is used to create the sacrificial layer of amorphous silicon that will help create a random texture on the crystalline silicon surface. This layer is used to retain the ions that will be implanted. LPCVD is a form of Chemical Vapor Deposition (CVD). Chemical vapour deposition (CVD) is a process where a solid material is deposited by a chemical reaction of a vapour on a substrate surface. The substrate is usually heated during this process. This results in a solid material which can be in the form of a powder, single crystal or, in the case of this project, a thin film. This process usually occurs at high temperatures to break the chemical bonds of the used gasses. Temperatures between 600 and 650 °C are used for silane (SiH_4), which is the precursor gas generally used for the

production of silicon films.[35] The chemical reaction is shown in equation 3.4. LPCVD is a form of CVD that functions at pressures below atmospheric pressure. This reduced pressure improves uniformity of the film across the wafer.[14]

$$SiH_4 \Longrightarrow Si + 2H_2 \tag{3.4}$$

3.2.3. Ion implantation

Ion implantation is a technique that bombards a solid material with a beam of ions. Ions that originate from the ion source of these machines are accelerated using an electric field. The accelerated ions penetrate the solid material and slow down due to interaction with the atoms in the solid. The penetration depth of the ions depends on the kinetic energy and the weight of the ions. If the kinetic energy is higher, the implantation depth will be larger. If the ion is heavier, the implantation depth will be smaller. Ion implantation is used to alter the properties of thin films, bulk materials and even nanostructures. The energy with which these ions hit the surface of the solid material, which hereafter is referred to as the implantation energy, can range from keV to hundreds of MeV. For ion doping in semiconductors, low energy ion implantation is used.[2] The Varian Implanter E500HP was used during this research. This implanter can accelerate ions with an energy up to 250 keV. The number of ions per square centimeter can be controlled, with a maximum of 10^{16} ions/cm^2. The available implantation ions are: boron, phosphorus, argon, arsenic and boron difluoride.

3.2.4. High temperature annealing

polycrystalline silicon can be obtained by creating a layer of amorphous silicon and then performing one of two available crystallization methods. These methods are thermal annealing and laser crystallization. This research uses thermal annealing for the crystallization process. Temperatures for this process usually range from 700 to 1100 °C. The high temperature anneal was done in an environment of nitrogen to prevent oxidation.[34]

3.2.5. Sacrificial layer process

This process starts with a cleaning step to remove any contamination that might be present on the wafers. A schematic representation of the steps after cleaning is shown in figure 3.4. The cleaning step is followed by Marangoni drying since the native oxide on the crystalline silicon wafers can prevent the creation of craters during the etching process. This is caused by the fact that it behaves differently to the used etch than silicon. Therefore, this layer should be removed.

After Marangoni drying, the wafers are loaded into the LPCVD to deposit a layer of amorphous silicon. The thickness of this layer of amorphous silicon can be controlled by changing the deposition time. The layer thickness scales linearly with deposition time. For example, a deposition time of 1 hour and 53 minutes is needed to deposit 250 nm of a-Si.

When the amorphous silicon is deposited, the wafers are ready for implantation. This implantation is done since it is believed to increase the grain size of the polycrystalline silicon that is obtained after annealing.[55][5][27]

After implantation, the wafers are contaminated with metal residues that are present in the ion implanter. Therefore, a cleaning step is performed.

This cleaning step is followed by a high temperature anneal to crystallize the amorphous silicon which creates polycrystalline silicon.

Now, the wafers are ready to be etched. The same polycrystalline silicon etch is used as was explained in section 3.1.4, which contains the following chemicals and concentrations: $HNO_3(69.5\%) : HF(40\%) : H_2O$ $525 : 15 : 210$. The etch time is dependent on the thickness of the created polycrystalline silicon. The etch rate is known to be around 350 nm/min for poly-Si. This concludes the sacrificial layer process for creating a random texture on crystalline silicon.

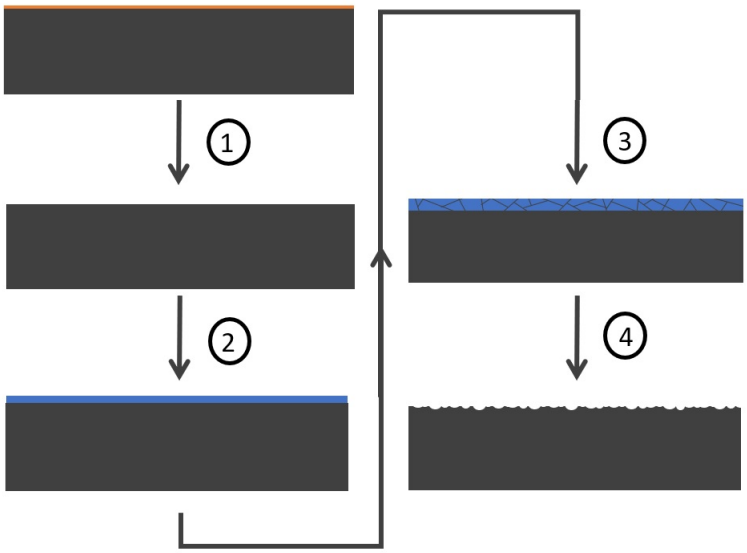


Figure 3.4: Schematic representation of the sacrificial layer process. Step 1, native oxide removal. Step 2, deposit a-Si on crystalline silicon wafer. Step 3, Ion implantation and anneal to create poly-Si. Step 4, poly-Si etch to create craters in crystalline silicon.

3.3. Solar cell production

The created textures were used to produce heterojunction solar cells. The equipment used for the production of these cells is explained in this section together with an account of the steps performed to create these solar cells.

3.3.1. Plasma enhanced chemical vapour deposition

Plasma Enhanced Chemical Vapour Deposition (PECVD) is used to deposit the different layers of nanocrystalline silicon that are needed to create the solar cell. PECVD is also a form of CVD, which was explained in section 3.2.2. As mentioned before, CVD is usually at temperatures between 600 and 650 °C for the creation of thin film silicon. This temperature can be reduced to between 200 and 300 °C by creating a plasma from the gasses. A plasma is a partially ionized gas that contains approximately an equal number of positive and negatively charged species. This plasma is much more reactive than the original gasses. Therefore, a lower temperature can be used for deposition. A plasma is used in plasma enhanced chemical vapour deposition (PECVD), of which a schematic representation is shown in figure 3.5. The plasma is created by using a radiofrequency generator or a Very High Frequency (VHF) generator to apply a high frequency voltage to a low pressure gas. The generator is connected to an electrode while the substrate holder is kept grounded. This alternating electric field causes the valence electrons to be released from their nucleus. These electrons have high kinetic energies and can therefore split the precursor gasses into individual atoms. The used precursor gasses are silane (SiH_4), hydrogen (H_2), which are split into (ionized) Si and H. These ionized atoms are called radicals. Diborane (B_2H_6) and Phosphine (PH_3) can also be used to introduce doping in the material. The ionized radicals drift to the substrate and create the desired material. When the desired thickness is reached, the radiofrequency generator is switched off. This causes the plasma particles to revert to the gas stage and these gasses are then pumped out of the deposition chamber. The properties of the created layers can be adjusted by varying the precursor gas flow rates, radiofrequency generator power and the ambient pressure and temperature.[56] The PECVD setup used in this research is called the AMIGO setup, which is an RF-PECVD Cluster tool by Elettrorava s.p.A.. This setup is located in the cleanroom 10000 of the Else Kooi Laboratory of the TU Delft. To produce the layers in AMIGO, the substrates are placed inside a load lock chamber. The air is then purged from this chamber until the pressure reaches 15-25 mbar. The substrate is then transported

to one of the six heated vacuum chambers. Each chamber has different gas inlets to create different layers to minimize cross contamination.

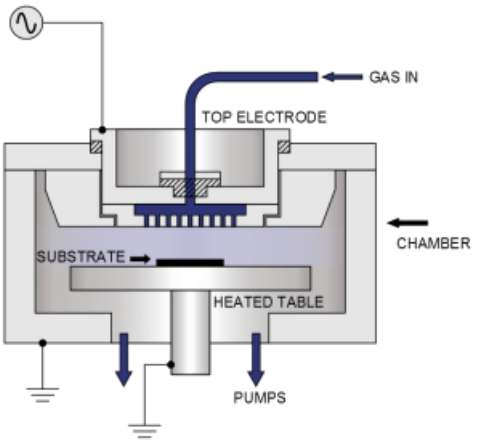


Figure 3.5: Schematic view of a PECVD deposition chamber.[19]

3.3.2. Sputtering

Sputtering is a form of Physical Vapour Deposition (PVD). Sputtering is used to create the TCO layer of the PV cell. In contrast to chemical vapour deposition, no chemical reaction takes place during PVD. Sputtering uses an RF generator to create a plasma. Accelerated particles from this plasma are used to bombard a target, which is made of a solid material. If the energy of the plasma is high enough, atoms are dislodged from the target and attracted to the substrate, which is electrically charged. This results in a thin layer of the desired material.[36] A schematic overview of sputtering is shown in figure 3.6. Sputtering is done on the machine called zorro, which is a Polyteknik AS cluster tool. This machine has two deposition chambers. The target used for the ITO deposition consists of 10 % SnO2 and 90 % In2O3. During the deposition, the temperature is 196 °C, the pressure is 0.022 mbar and a power of 135 W is used.

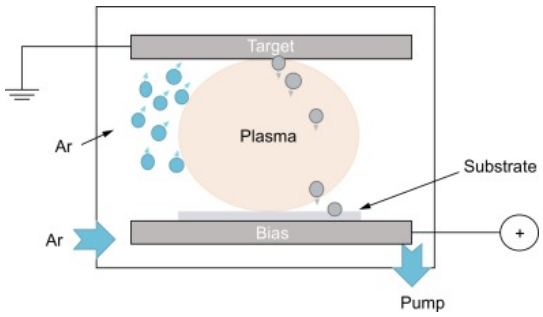


Figure 3.6: Schematic representation of the sputtering process.[60]

3.3.3. Electron beam evaporation

Electron beam evaporation is used to create the metal contacts. Electron beam evaporation is a form of PVD. The target is bombarded with a beam of electrons that originate from a charged tungsten filament, which takes place under high vacuum conditions. This beam causes the target to heat and therefore (partially) evaporate. This evaporated material then precipitates to form a thin film on the wafer. A schematic representation of this technique is shown in figure 3.7. This method has some advantages compared to sputtering. For instance, the direct energy transfer between the beam and the target allows the use of metals with a high melting point and results in a layer with high purity material. Also, electron beam evaporation has a high material utilization efficiency compared to sputtering, which makes it ideal for depositing layers of expensive metals. Moreover, this method has a relatively high

deposition rate of between 0.1 and 100 nm/minute.[21] The machine used for this technique is the Provac PRO500S. This machine can hold 4 wafers which are covered with a shadow mask so the desired pattern of metal contacts is created. This machine also allows the use of a rotating sample stage to increase the uniformity of the deposited layer. This stage rotates with 10 to 20 rotations per minute. The thickness of the layer is measured during deposition using a crystal type film meter. When the desired thickness is reached, the electron beam is switched off.

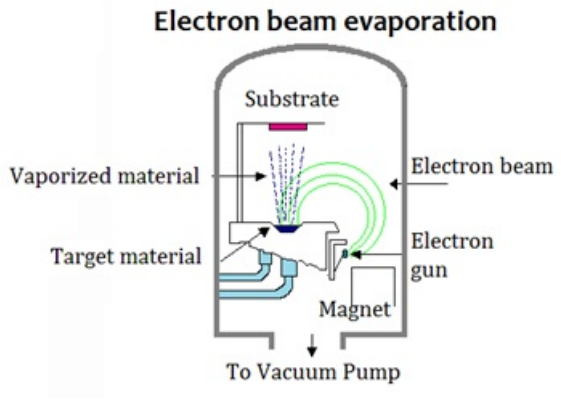


Figure 3.7: Schematic representation of electron beam evaporation. Adapted from [28].

3.3.4. Solar cell flowchart

After the textures are created, the wafers are cleaned three times. The cleaning is done in the same way as was explained in section 3.1.1, but a step is added. This step is the removal of the native oxide using a 0.55 % HF bath. Thus, the cleaning involves a bath of 99 % HNO_3, a bath of 69.5 % HNO_3 at 110 °C, and a 0.55 % HF bath. During the third time cleaning, the last step (the 0.55 % HF bath) is replaced with Marangoni Drying, which was explained in section 3.2.1.

After the cleaning is done, the wafers are loaded into AMIGO to start the deposition steps. A schematic overview of these steps is shown in figure 3.8. Since the wafers are textured, the surface is covered with dangling bonds. Therefore, the PECVD process is started by depositing a passivation layer of hydrogenated intrinsic amorphous silicon, which is aimed to be approximately 5 nm. The deposition conditions for all mentioned layer are shown in table 3.1. All gas flows in this table are in standard cubic centimeter (scc) per minute. This is done at the n^+ type side first, which will be the back of the solar cell, since the depositions are done at temperatures of around 200 °C. At this temperature, small atoms like boron can diffuse easily which can lead to unwanted doping of sensitive sections of the solar cells. Phosphorus atoms diffuse slower and therefore the n^+ type side is done first.

On top of this intrinsic layer of amorphous silicon, the n^+ a-Si is deposited. The thickness of this layer is aimed to be approximately 6 nm.

Afterwards, the wafers are flipped and the intrinsic amorphous silicon passivation layer is added to the top op the cell. This layer is also aimed to be approximately 9 nm. This wafer is then subjected to a hydrogen plasma treatment which removes about 3 nm of the intrinsic amorphous silicon and promotes passivation. The hydrogen plasma treatment conditions are also shown in table 3.1.

This is followed by the deposition of a nanocrystalline seed layer of 2 to 3 nm, which is used as a support for the p type nanocrystalline silicon oxide that is deposited at the top of the solar cell. P type nanocrystalline silicon oxide is used for two reasons. The first reason is the light transmittance of this material. If amorphous silicon was used, a large portion of the light would be absorbed in this layer due to the high absorption coefficient. Fortunately, the light absorption of silicon oxide is much lower than the absorption of amorphous silicon. Also, the nanocrystalline properties of p type silicon oxide are desirable. This material creates vertical ”highways” for charge carriers, which are in this case holes.

Next, the TCO layer is deposited on both sides of the solar cell. This layer is used for the

lateral conduction of charge carriers to the electrodes. This layer is 70 nm thick and consists of Indium Tin Oxide (ITO).
Finally, the electrodes are created using electron beam evaporation. These electrodes are made from aluminium and have a thickness of 500 nm. This concludes the solar cell flowchart.

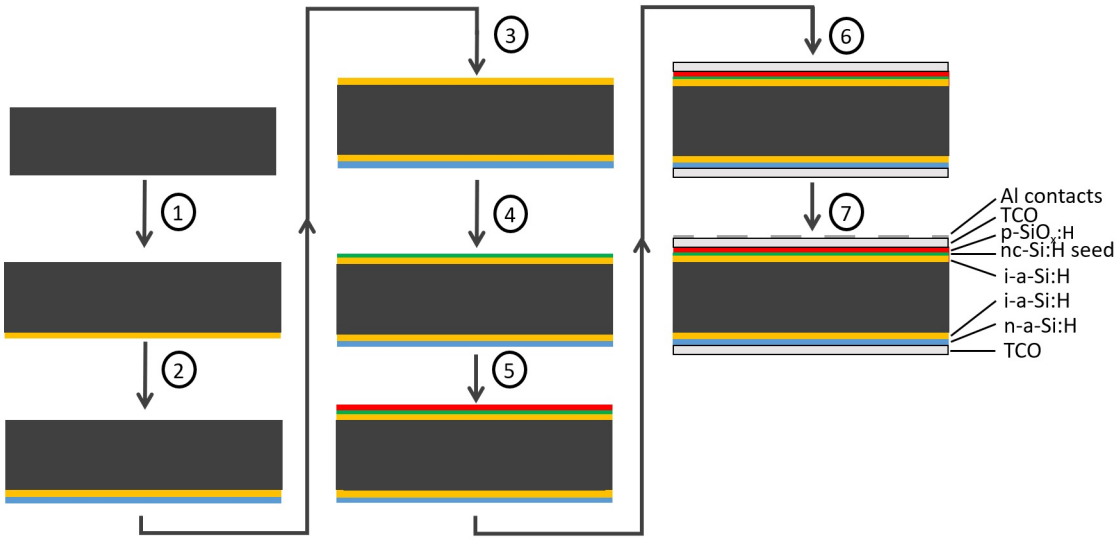


Figure 3.8: Schematic representation of the solar cell flowchart. Step 1, deposit 5 nm thick layer of i-a-Si:H on backside on crystalline silicon wafer. Step 2, deposit 6 nm thick layer of n-a-Si:H. Step 3, deposit 9 nm thick layer of i-a-Si:H on front side, followed by hydrogen plasma treatment. Step 4, deposit 2-3 nm of nc-Si:H as a seed layer. Step 5, deposit 4 nm thick layer of p-SiO_x. Step 6, Deposition of 70 nm of TCO. Step 7, deposit aluminium contacts of 500 nm thick.

Layer	Thickness (nm)	SiH_4	H_2	PH_3	B_2H_6	CO_2	Pressure(mbar)	RF Power(W)
n-a-Si	6	40	-	11	-	-	0.6	4
i-a-Si:H	5	10	30	-	-	-	1.4	3
n-type wafer								
i-a-Si:H	9	10	30	-	-	-	1.4	3
H_2 Plasma treatment	-	-	200	-	-	-	2.2	11
nc-Si Seed	2-3	1.2	120	-	-	-	4	13
p-SiO_x:H	4	0.8	170	-	10	1.4	2.2	11

Table 3.1: Deposition conditions for the production of the solar cells. All gas flows are in standard cubic centimeter (scc) per minute. The phosphine flow consists of 2% PH_3 in H_2 and the diborane flow is 200ppm B_2H_6 in H_2.

3.4. Measurement equipment

The measurement equipment that is used to image the created textures, to find the reflectance of these textures, and to characterize the solar cell parameters are explained in this section.

3.4.1. Scanning electron microscopy

Scanning electron microscopy (SEM) is used to create images of the textured surfaces. Electron microscopes use a beam of accelerated electrons as a source of illumination. Electrons are used because they have a shorter wavelength than visible light, which increases the resolution. There are different types of electron microscopes. For example: Transmission Electron Microscopes (TEM), Scanning Electron Microscopes (SEM), Reflection Electron Microscopes (REM), and Scanning Tunneling Microscopes (STM). In this research, SEM is used. A schematic representation of this type of microscope is shown in figure 3.9. SEM uses a focused beam of electrons to scan the surface. These electrons originate from an electron source. They are emitted from the source material when their thermal energy becomes larger

than the work function of the material. These electrons are then accelerated using the positive charge of the anode and focused on the sample using a set of electromagnetic lenses. The electrons first pass through the condenser lens. This lens influences the width of the electron beam, which defines the resolution of the image. Then the beam passes through the scan coils, which are used to move the beam across the surface. Before reaching the sample, the electrons pass through the objective lens. This lens focuses the beam onto the sample. When the beam reaches the sample, many different interactions between the beam and the material take place. These interactions result in different types of irradiation and electrons. For SEM, two different types of resulting electrons are used to create an image: the secondary electrons and back scattered electrons. Back scattered electrons are electrons which originate from the electron beam. These electrons are reflected from the sample after elastic collisions. The secondary electrons originate from the sample atoms. Inelastic collisions between the electron beam and the sample cause electrons from the sample to be dislocated from their atom. These are the secondary electrons. Back scattered electrons penetrate further into the material than secondary electrons. Hence, the two different types contain different information. Back scattered electrons can give information about the different materials in a sample. The brighter the image, the higher the atomic number is. On the other hand, secondary electrons give a more detailed view of the surface of the sample.[38]

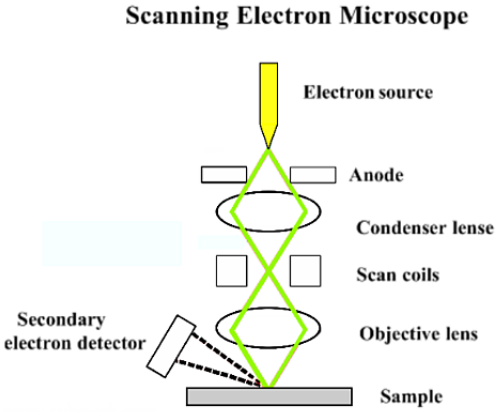


Figure 3.9: Schematic representation of a SEM.[38]

The SEM used in this research is the Nova NanoSEM 50 Series from the company FEI. This SEM is located in the Kavli Institute of Quantum Nanoscience in Delft. The specifications of this machine can be found in [12].

3.4.2. Atomic force microscopy

Atomic Force Microscopy (AFM) is used to create a depth profile of the created surface textures. This type of microscope uses a sharp tip to make a raster-scan of the surface. When the tip is moved along the sample, atomic forces cause the tip to be attracted by the surface. When this happens, the tip bends towards the surface. A laser is used to measure the tip deflection, which can then be translated to a force using Hooke's law shown in equation 3.5

$$F = -kz \tag{3.5}$$

Where F is the atomic force, k is the stiffness of the tip and z is the distance between the tip and the sample. The AFM measures a force-distance curve for multiple points on the sample. An example of a force-distance curve is shown in figure 3.10. When the tip is in hard contact with the surface, it is pushed away which leads to a force greater than 0. This is shown in red. When the tip is just above the surface, the atomic forces attract the tip. This is shown in blue. These curves are used to find the position of the surface. After scanning multiple points of a surface, a 3D image can be made.[24] Two different atomic force microscopes were used during this study. The first one is located in room lb00.640 in the lower building of the

Electrical Engineering, Mathematics and Computer Sciences (EEMCS) faculty in Delft. This AFM is an Ntegra Probe NanoLaboratory, which uses a semicontact mode. The second AFM is the Bruker Dimension Icon with Scan Assist. This AFM is located in the Kavli Institute of Quantum Nanoscience in Delft. The mode used on this AFM is the ScanAsyst mode, which is a peak force tapping mode with automatic optimization of the parameters.

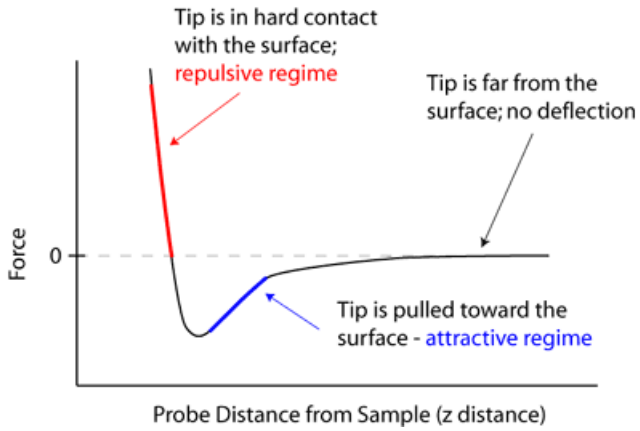


Figure 3.10: Example of a force-distance curve measured by an AFM.[24]

3.4.3. Reflectance measurements

As mentioned in section 2.1.2, light that falls onto the wafer is either reflected, transmitted or absorbed. If the Lambert-Beer law (equation 2.11) is used in combination with a wafer thickness of 280 µm and the absorption coefficient for visible light from figure 2.2, the result shows that the transmission of light is very close to zero. Therefore, if the reflectance is measured, conclusions can be made about the light absorption of the wafer. These measurements are performed using the lambda 950 and 1050 from the company PerkinElmer. These machines use deuterium and tungsten halogen light sources in combination with highly sensitive light detectors that can measure the reflectance of the samples over a wavelength range of 175 to 3300 nm. The lambda 950 can be equiped with an Automated Reflectance/Transmittance Analyzer (ARTA). The ARTA can be used to measure the reflectance and transmittance for a range of different angles. This can be used to find the angular distribution of reflectance and transmission of a sample.

3.4.4. Solar cell parameter measurements

The properties of the produced semiconductor layers and cells were investigated using various measurement setups available at the TU Delft. This section is used to explain these setups.

I-V curve

The I-V curve is obtained by connecting the PV cell to a load, while the PV cell is illuminated. The resistance of this load is then incrementally changed and the produced current is measured at the different voltages. This IV curve can then be used to calculate other solar cell parameters, such as the efficiency and the fill factor. The PV cell was illuminated by a simulated AM1.5 spectrum while the cell was kept at 25 °C. The AM1.5 spectrum was simulated using the WACOM class AAA device, which uses xenon and halogen lamps. These lamps were calibrated using two crystalline silicon solar cells which were manufactured by the Fraunhofer Institute for Solar Energy Systems.

Minority charge carrier lifetime

The minority charge carrier lifetime gives an indication of the number of defects in a material. This lifetime is measured using the Eddy-current method. A coil is used to send

electromagnetic waves into the silicon. Light is then pulsed onto the wafer, which creates excess charge carriers. The coil measures the increase in conductance of the wafer due to the excess charge carriers. This data is analyzes uding the Quasi-Steady-State Photoconductance (QSSPC) method.[26] This method relies on the amount of minority charge carriers present when the sample is illuminated with a steady light source. The intensity of the flash is assumed to change slow enough to keep the minority and majority charge carriers in steady state. By measuring the amount of light coming from the cell and correcting for the reflectivity and absorption coefficient, the generation rate can be determined. This is used to determine the lifetime of the minority charge carriers.[10] The lifetime measurements are performed on the Sinton WCT-120 made by Sinton Instruments.

4

Results and Discussion

The created textures using the photolithography method and sacrificial layer method are presented in this chapter, along with the performance of the solar cells manufactured on these textures. As mentioned in section 1.6, this research has 4 subgoals. Firstly, to create a hexagonal texture process. Secondly, to design a mask for this process that results in a crack-free nc-Si:H layer. Thirdly, to investigate the effect of the different parameters on the grain size of polycrystalline silicon for the sacrificial layer method. Finally, to compare the two textures in optical performance and solar cell performance. The latter is done by producing Silicon HeteroJunction (SHJ) solar cells using these textures.
The same order is used in this chapter. Therefore, the results of the photolithography method will be shown first, in section 4.1. This includes the optimization of the hexagonal texture method using surface measurements (SEM) and the nanocrystalline silicon crack test. The second section, section 4.2, will show the results of the sacrificial layer method. This includes the investigation of the effect of the different parameters on the size of the craters that originate from this method. This is done using surface measurements (SEM and AFM). This is followed by section 4.3, which will include the optical measurement results for both textures. Finally, the results of the photolithography and sacrificial layer method are compared in terms of SHJ solar cell performance.
The texturization methods in this research are tested on four inch (99.8-100.2 mm) crystalline silicon wafers. These wafers are supplied by the company Topsil. The wafers are n-type, doped with phosphorus. The thickness is between 260 and 300 µm, the orientation is <100> and the wafer is polished on both sides.

4.1. Photolithography

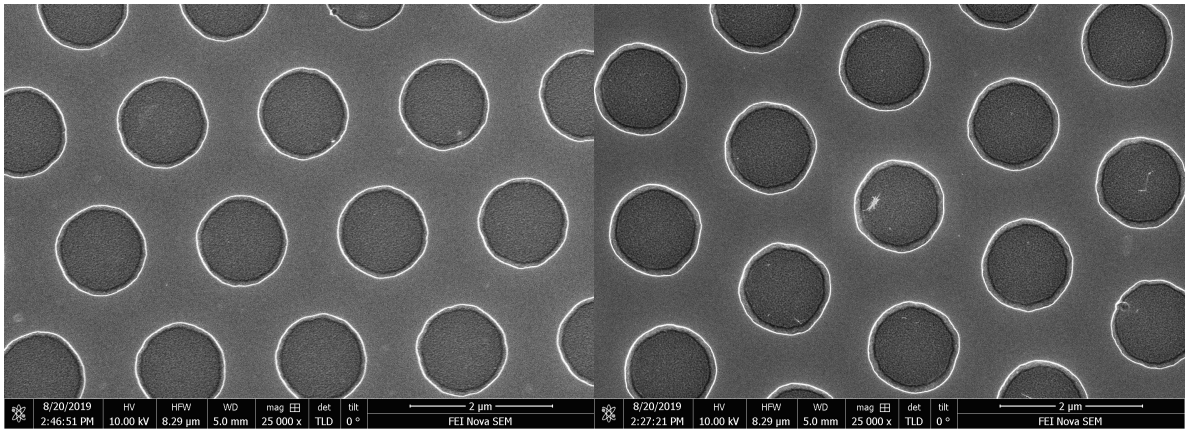
As mentioned in section 2.5, photolithography uses a light sensitive polymer to produce patterns. This method is mainly used for the fabrication of integrated circuits. In this research, photolithography is used to create a hexagonal texture in crystalline silicon. This process was optimized and the results are shown in this section.

4.1.1. Optimizing hexagonal texturing

As mentioned in section 3.1.4, two masks were used for the creation of a hexagonal texture on crystalline silicon. The crystalline silicon etch times for these masks had to be determined experimentally. Even though the etch rate of crystalline silicon by the used etchant was unknown, it was estimated to be 100 nm/min by researchers from the Else Kooi Laboratory. This was used in combination with the etch distance, which was determined in section 3.1.3. This etch distance is equal to the distance from the centre to the hexagon to the corner minus the radius of the hole. Since the distance from the centre to a hexagon to the corner is equal to the period divided by the square root of three, the etch distance is equal to equation 4.1.

$$D = \frac{P}{\sqrt{3}} - R \tag{4.1}$$

Where D is the etch distance, P is the period of the hexagonal texture, and R is the radius of the hole. When the parameters of the available masks are used (radius of 0.5 µm and period of 2 µm for mask 1 and 3 µm for mask 2), the resulting etch distances are around 0.65 and 1.2 µm, which corresponds to an estimated etch time of 6.5 minutes for mask 1 and 12 minutes for mask 2.
Mask 1 was chosen to do the initial etch rate test. For this test, etch times of 2, 4, 6 and 8 minutes were tested and the results were inspected using SEM. The SEM images are shown in figure 4.1. These images show that even after 8 minutes of etch, the corners of the hexagon are still not reached. Using the measurement tool of the SEM, it was found that the average etch rate is about 50 nm/min, so half of what was estimated. This lower etch rate could be related to accumulation of etching reactants in the holes of the silicon dioxide mask. These etching reactants can prevent the etching of new parts of silicon, which results in a lower etch rate.



(a) Etch time of 2 minutes.

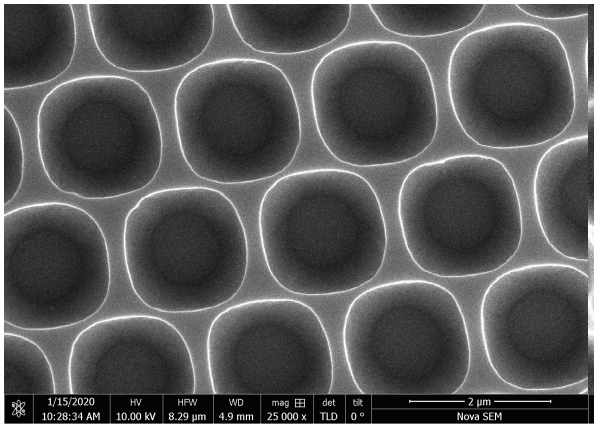
(b) Etch time of 4 minutes.

(c) Etch time of 6 minutes.

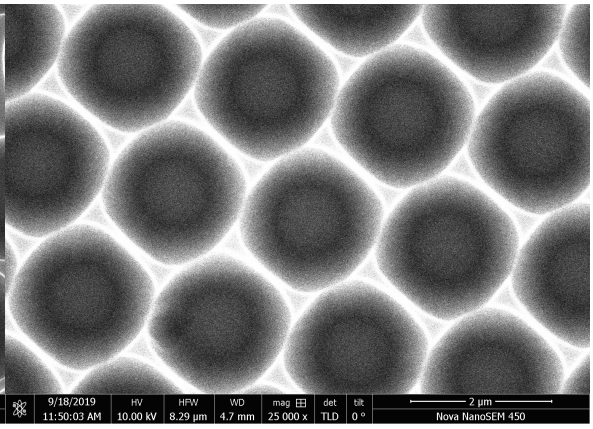
(d) Etch time of 8 minutes.

Figure 4.1: SEM images of different etch times using photolithography mask 1.

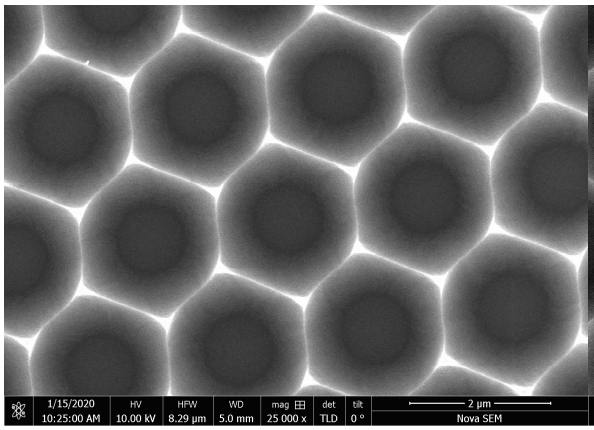
This results in an etch time of 13 minutes for mask 1 and 24 minutes for mask 2. To account for fluctuations in the etch rate for longer etch times, four different etch times were used for both mask 1 and mask 2. For mask 1, the etch times of 10, 12, 14 and 16 minutes were used. For mask 2, etch times of 21, 23, 25 and 27 minutes were used. The results of mask 1 are shown in figure 4.2. These SEM images show that the minimum etch time for mask 1 is 16 minutes.



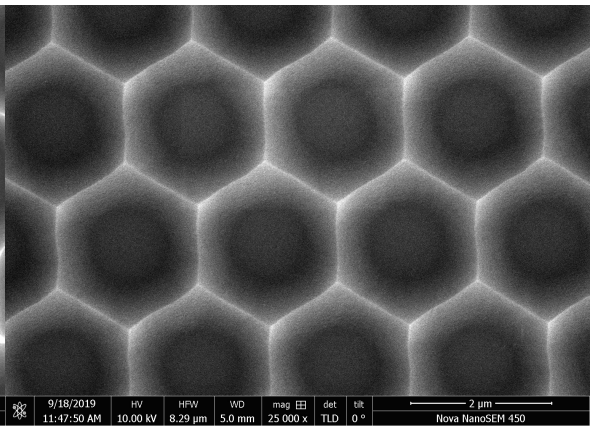
(a) Etch time of 10 minutes.



(b) Etch time of 12 minutes.



(c) Etch time of 14 minutes.



(d) Etch time of 16 minutes.

Figure 4.2: SEM images of different etch times using photolithography mask 1.

The result for the longest etch time of mask 2 is shown in figure 4.3. This figure shows that even after the long etch time, the etch distance was nowhere near reaching the edges of the hexagon. This could, as mentioned before, be related to the accumulation of etching reactants in the holes of the silicon dioxide mask, which decreases the etch rate.

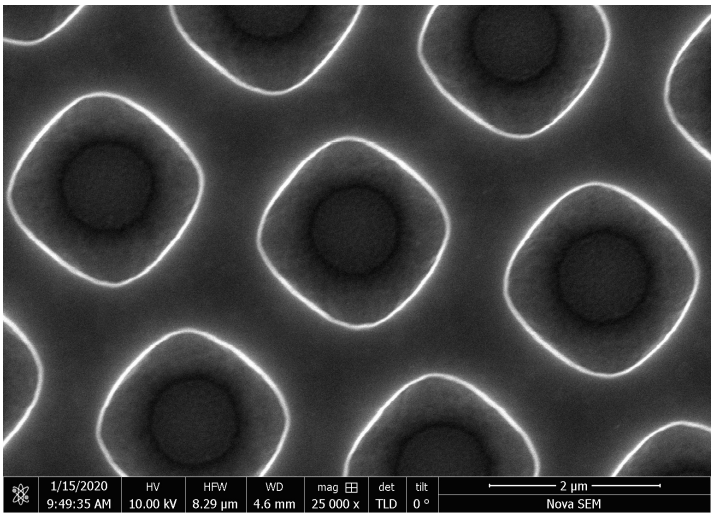
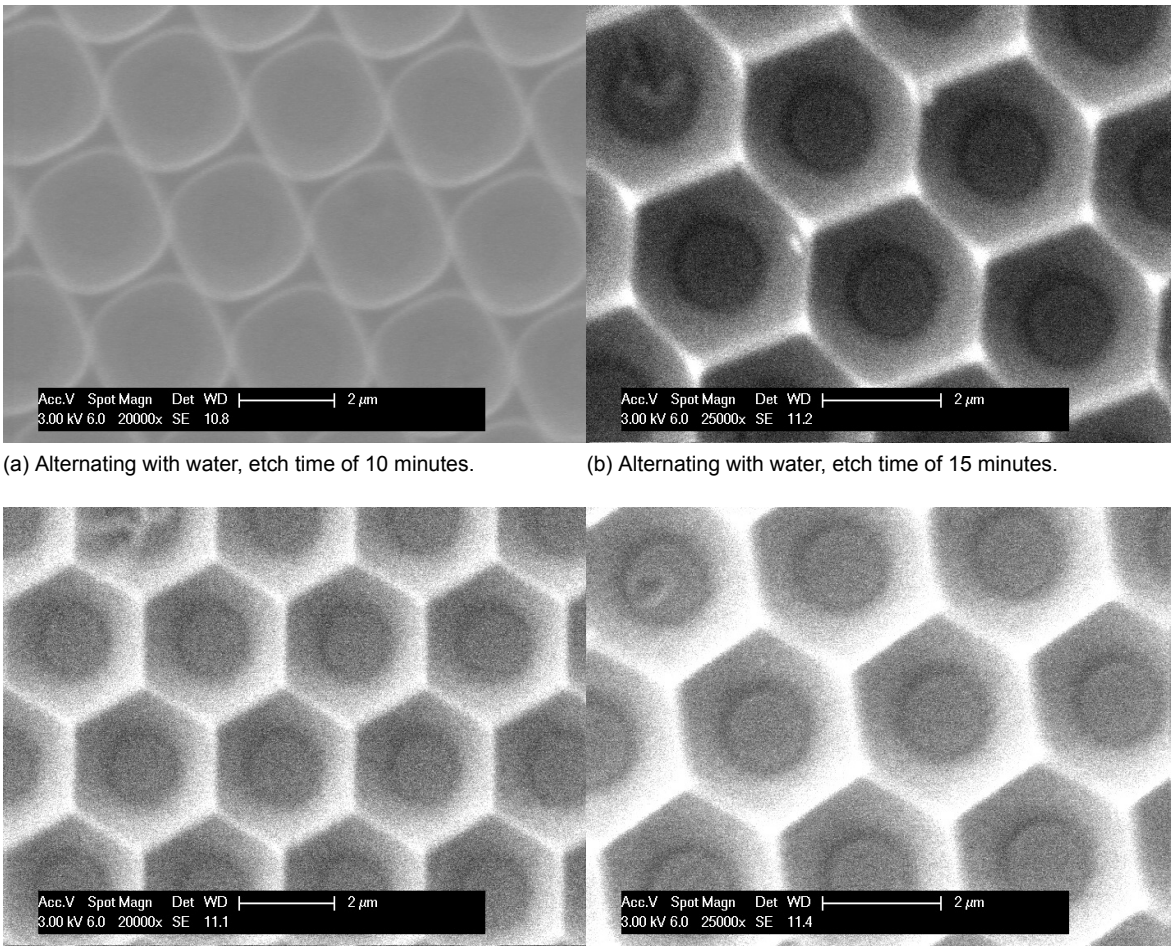


Figure 4.3: SEM image of 27 minute etch time using photolithography mask 2.

Since the tested etch times were close to the maximum etch time of 30 minutes, related to the thickness of the silicon dioxide mask, a longer etch time was not possible. Therefore, the etch rate needed to be increased. This can be done in three ways. The first option is related to the etch rate of the solution. This can be increased by heating the solution to a temperature above room temperature. The disadvantage of this heating is that the etch rate increases exponentially with temperature. Thus, this idea would require extensive testing to find the optimal temperature and etch time. Furthermore, the etch rate of the silicon oxide mask would also increase. This reduces the maximum etch time and could therefore lead to the same problem, that the mask is dissolved before the hexagonal texture is created. The second and third options are related to accumulation of etching reactants in the holes of the silicon dioxide mask. These etching reactants can prevent the etching of new parts of silicon. A solution for this would be either stirring of the etchant or alternating between etching of the wafers and rinsing in water. Since this last option was the easiest to try, this was tested first. The results of this test is shown in figure 4.4. The wafers were alternated between etch and water every 5 minutes. These figures show that this method works and that the minimum etch time is between 10 and 15 minutes.



(a) Alternating with water, etch time of 10 minutes.

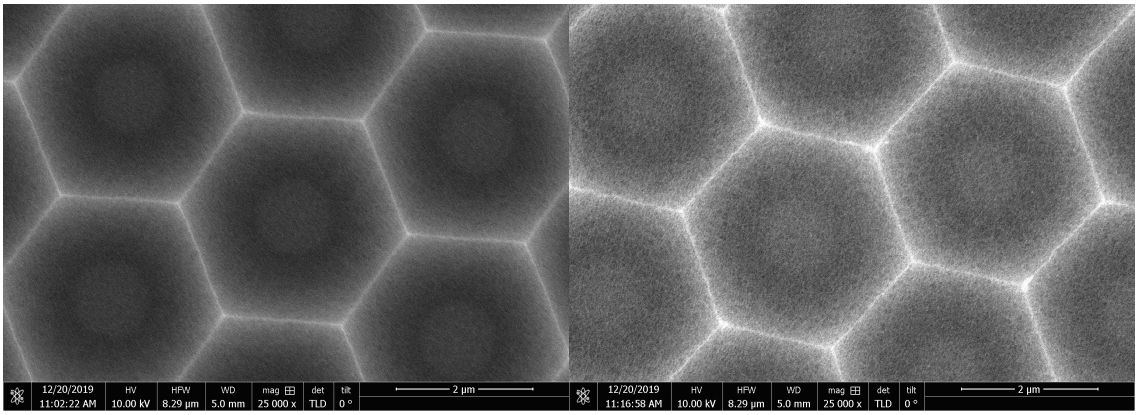
(b) Alternating with water, etch time of 15 minutes.

(c) Alternating with water, etch time of 20 minutes.

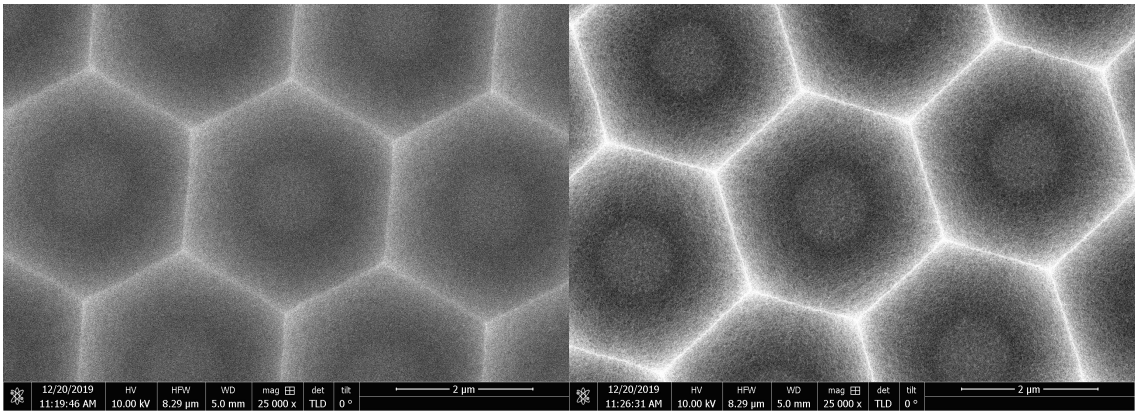
(d) Alternating with water, etch time of 25 minutes.

Figure 4.4: SEM images of different etch times, alternating with water, using photolithography mask 2.

To refine the minimum etch time a bit further, four more etch times were tested using the water method on mask 2. These times were 12, 14, 16, and 18 minutes. The results are shown in figure 4.5. This shows that after a minimum of 12 minutes, the hexagonal texture is created.



(a) Alternating with water, etch time of 12 minutes. (b) Alternating with water, etch time of 14 minutes.



(c) Alternating with water, etch time of 16 minutes. (d) Alternating with water, etch time of 18 minutes.

Figure 4.5: SEM images of different etch times, alternating with water, using photolithography mask 2.

To show the three-dimensional shape of the hexagonal texture, an extra SEM picture was taken using a tilt of the sample of 40 °. The result is shown in figure 4.6. This shows that the walls are not straight, but have a conical shape which is desirable for light scattering and incoupling.

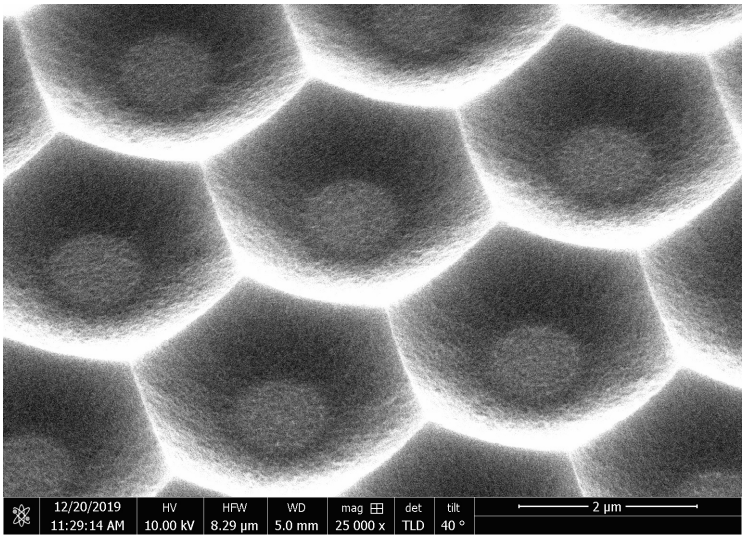
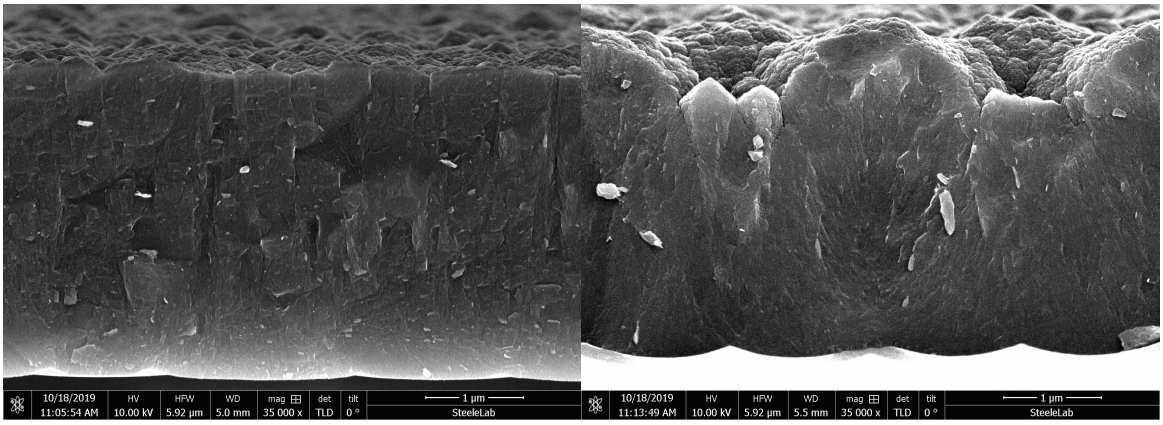


Figure 4.6: Tilted SEM image of hexagonal texture.

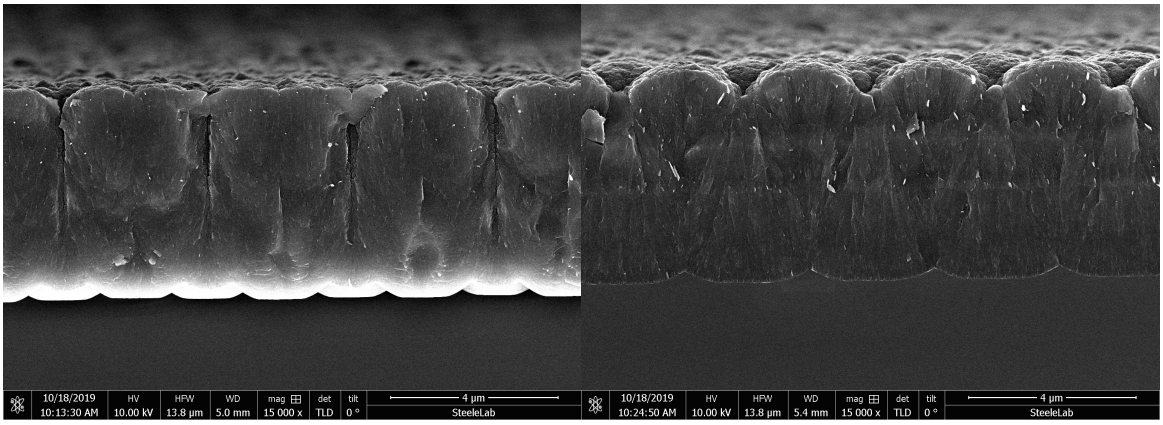
4.1.2. Nanocrystalline silicon test

After the optimization of the photolithography process for two different masks, the quality of the nc-Si can be examined when it is deposited on the hexagonal structure. For this purpose, two different thicknesses, 3 µm and 5 µm, were grown using the AMIGO setup and cross-section images are made using SEM. The results are shown in figure 4.7. These images show that the height of the hexagonal texture is very low compared to the height of the texture using mask 2. This could be caused by over-etching of the sample. When the sample is etched too long, the edges of the craters are more exposed to the etchant compared to the bottom of the crater since the etching reactants are expelled from the surface more easily. Therefore, the sides are more vulnerable to being etched. The consequence of this effect is that over-etching causes the surface to flatten. Even though the texture was small, figure 4.7c shows clear cracks in the nc-Si. As mentioned in section 1.6, this is detrimental for the performance of the PV cell. Figure 4.7d shows that these cracks do not develop when the hexagonal figures of mask 2 are used. Therefore, it was decided to use the period of this mask (3 µm) for mask design that will be used for the creation of the solar cells. For the hole diameter of the mask, it was shown in section 3.1.3 that the height difference in the texture should be around a quarter of the period. If the vertical and horizontal etch rates are equal, this results in an optimum hole diameter of 2 µm. However, it was decided to use a hole diameter of 1 µm for the designed mask. This was done since the difference between the horizontal and vertical etch rate was not known. If, for example, the horizontal etch rate is larger than the vertical etch rate, the texture becomes too shallow. This can be avoided by using a smaller hole diameter. If the hexagonal texture turns out to be too steep, this can be resolved by over-etching of the texture, which flattens it. Figure 4.7d shows that the top of the nc-Si layer is not flat. When the layer is deposited on top of the hexagonal texture, the top of this layer shows this texture, but reversed.



(a) Cross-section of mask 1 hexagonal texture with 3 µm nanocrystalline silicon.

(b) Cross-section of mask 2 hexagonal texture with 3 µm nanocrystalline silicon.



(c) Cross-section of mask 1 hexagonal texture with 5 µm nanocrystalline silicon.

(d) Cross-section of mask 2 hexagonal texture with 5 µm nanocrystalline silicon.

Figure 4.7: SEM images of 3 and 5 µm of nc-Si on hexagonal textures created using mask 1 and mask 2.

4.2. Sacrificial layer

The second texturing method is the sacrificial layer method. This process uses a sacrificial layer of polycrystalline silicon to create a random texture in crystalline silicon. When this polycrystalline silicon layer is etched, the etchant goes through porous regions, such as grain boundaries, in the polycrystalline silicon faster than through the crystalline tissue. This creates craters in the mono-crystalline silicon underneath. As mentioned in section 3.1.3, the optimum size of the hexagonal texture is dependent on the thickness of the thin film silicon layer that is deposited on top of it. It was shown by Sai et al. [45] that the texture width should be 0.5 µm larger than the thickness of the deposited layer. It is assumed that this effect is similar for the craters that are created by the sacrificial layer method. Thus, the desired average crater size is between 3 and 3.5 µm. Therefore, the effect of the different parameters on the crater size of this texture was investigated, after which the most promising samples were used to create a solar cell. The research in this section was done using SEM and AFM. SEM is great for accurate imaging of a sample surface, while AFM is used to examine different characteristics of the surfaces, such as average crater size, roughness, mean slope and height differences. These characteristics are found using the software NanoScope. For this section it was decided to only show the mean crater size and average roughness, since these are suitable to show the trends that are important to this research. Also, the mean slope and height differences mainly follow the same trends as the other two parameters. An example of this is shown in appendix A. The results of the sacrificial layer experiments will be shown in this section.

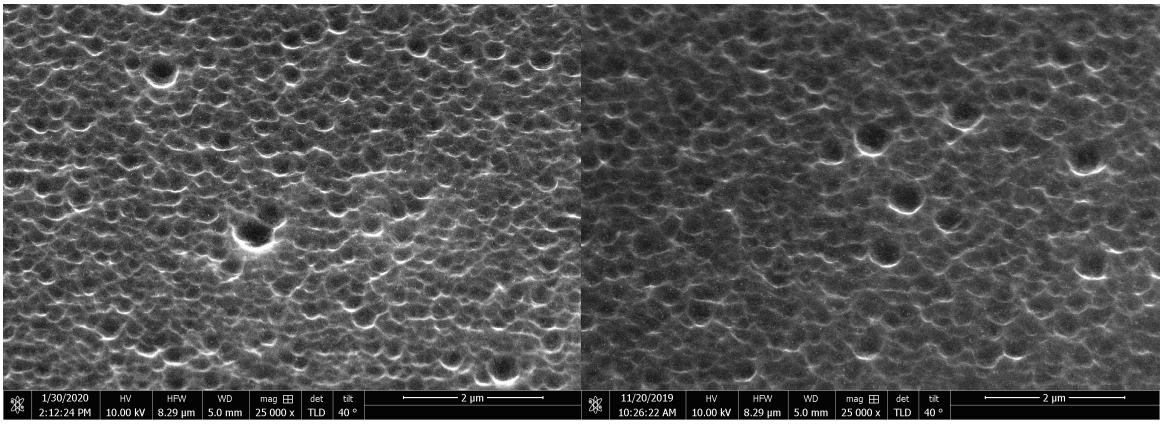
4.2.1. Sacrificial layer parameters

The sacrificial layer method was described in section 3.2.5. This process depends on a number of variables. Changes in these variables presumably influence the size of the grains in the sacrificial layer of polycrystalline silicon. How these parameters affect the resulting polycrystalline, and therefore also the size of the created craters, was examined. The parameters that were investigated in this research are: the amorphous silicon layer thickness, the anneal temperature, the anneal time, the implanted ion, the ion implantation energy and the ion implantation dose.

Layer thickness

The first parameter that was investigated is the effect of the layer thickness. For this part of this sacrificial layer research, phosphorus was used for the implantation since this atom shows great promise for the creation of large grain poly-silicon (above 1 µm in grain size).[3][5] This ion was implanted at an energy of 5 keV. These layer thickness tests were done using the highest dopant concentration possible of 10^{16} ions/cm^2, the upper limit of the E500HP Varian Implanter. This was decided since an increase in impurity concentration in silicon has been linked to an increase of the diffusion coefficient of silicon, which results in larger poly-Si grain sizes.[55][5] The anneal temperature and time for these tests were 950 °C for 60 minutes. These were determined to be favorable during initial tests.

The used amorphous silicon layer thicknesses were 0.5 µm, 1 µm, 2 µm and 4 µm. The results are shown in figure 4.8. The first thing that can be noticed is that the craters of the 0.5 µm samples (figure 4.8a and b) are more defined compared to the 2 µm samples (figure 4.8c and d). This could be caused by over-etching of the sample. This causes the surface to flatten, as was explained in section 4.1.2, which makes it harder to distinguish the craters. Nevertheless, the crater size seems to increase when the thickness increases from 0.5 to 1 µm, and decreases again for larger thicknesses. AFM analysis showed that the conclusion drawn from figure 4.8 was correct. The results of the AFM measurements are shown in table 4.1. Unfortunately, the AFM measurement of the 4 µm sample was dominated by noise which made it impossible to extract any useful information. The crater size increases from about 257 nm to 277 nm when the amorphous silicon layer is increased from 0.5 µm to 1 µm. The crater size decreases when the a-Si layer is increased to larger thicknesses than 1 µm. More specifically, from 277 nm to 260 nm for the a-Si increase from 1 to 2 µm. This could be caused by the dopant concentration in the a-Si layer. If the layer is too thick, the phosphorus concentration near the crystalline silicon surface is too low. The poly-silicon grain size is dependent on the implanted impurity concentration. For larger a-Si thicknesses, the dopant concentration near the crystalline silicon surface might be lower compared to the concentration for smaller thicknesses. This could result in smaller polycrystalline silicon grains, which results in smaller craters. The average roughness is also shown in this table 4.1. This roughness gives an indication of the optical properties of this layer. A higher roughness is more likely to result in higher levels of light incoupling. This is not particularly useful for this layer since it is the bottom cell of the eventual triple junction solar cell, but because the texture is copied automatically by the layers deposited on top, this is an important feature. For reference, the average rougness of the standard pyramid structure for crystalline silicon, which creates cracks in the nc-Si deposited on top, is around 390 nm. The AFM measurements show that the roughness is maximum for the 1 µm thick layer, but is still a factor 15 smaller than the pyramid texture roughness. It is also good to notice that the average roughness of the 2 and 4 µm samples is much lower than the average roughness of the 0.5 µm sample, even though the mean pore diameters are similar. This is likely to be caused by over-etching of the larger samples.



(a) Amorphous silicon layer of 0.5 µm.

(b) Amorphous silicon layer of 1 µm.

(c) Amorphous silicon layer of 2 µm.

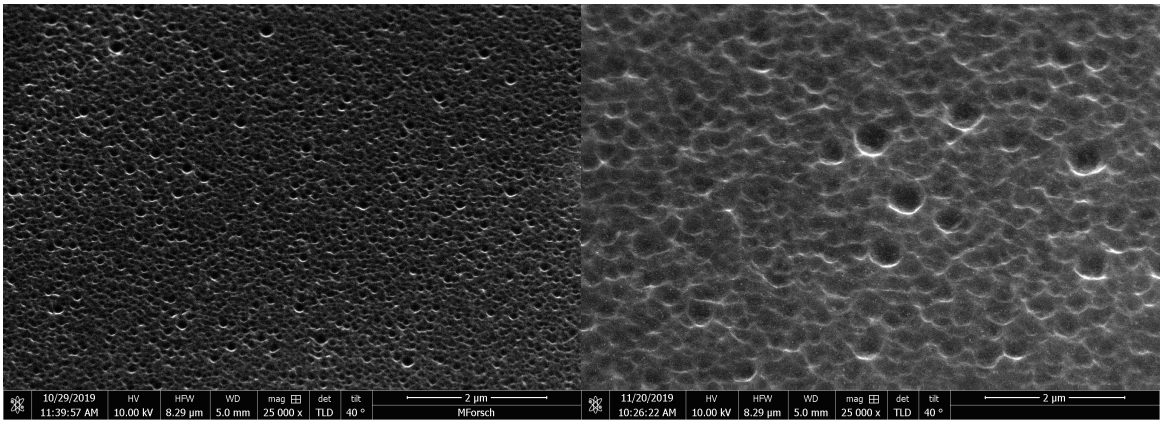
(d) Amorphous silicon layer of 4 µm.

Figure 4.8: SEM images of the effect of different a-Si layer thicknesses used in the sacrificial layer process.

Layer thickness (µm)	Implantation	Mean pore diameter (nm)	Average roughness (nm)
0.5	P 5 keV	256.9 ± 8.4	9.5
1	P 5 keV	276.6 ± 8.0	15.9
2	P 5 keV	260.0 ± 8.0	8.0

Table 4.1: AFM analysis of a-Si layer thickness series.

For completeness, the process was also done without a layer of amorphous silicon. Thus, the ions were directly implanted in the crystalline silicon wafer. The result is shown in figure 4.9. This figure shows that the craters in the texture using amorphous silicon are much larger than the craters from the process without amorphous silicon. This indicates that the initial layer of amorphous silicon is important for the creation of large grain poly-silicon. Since the implantation without a layer of amorphous silicon resulted in much smaller craters, these were not examined using the AFM since the outcome would be evident.



(a) No a-Si layer. (b) 1 µm a-Si.

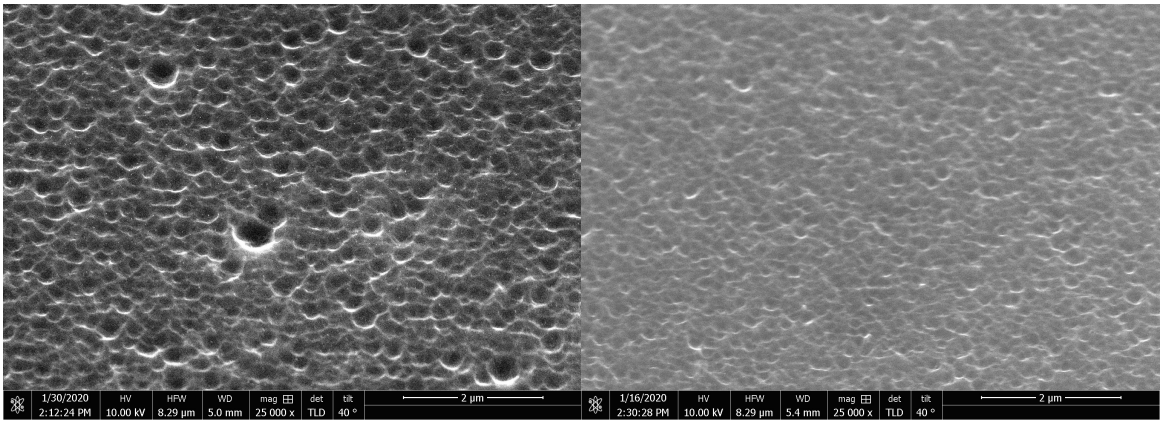
Figure 4.9: SEM images of the result of using no a-Si compared to 1 µm of a-Si in the sacrificial layer process.

Ion implantation energy

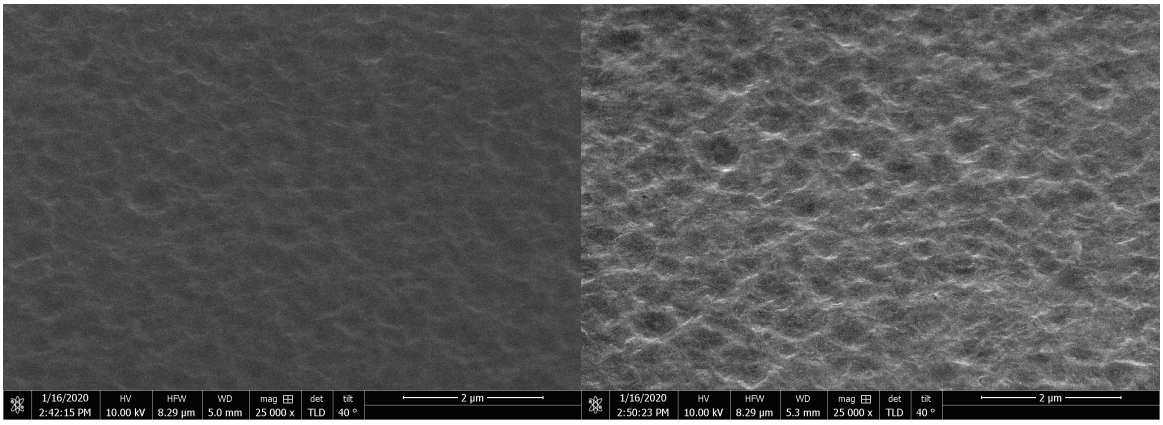
The effect of the energy used for implantation was also examined. This was done for phosphorus and argon implantation. For phosphorus, two energies were used: 5 and 50 keV. Larger energies could cause the ions to penetrate far into the crystalline silicon. This decreases the dopant density in the amorphous silicon layer, which is likely to lead to smaller grains in the polycrystalline silicon according to Wada et al. [55] and Carabelas et al. [5]. More importantly, higher energies would lead to unwanted doping in the crystalline silicon, which has a negative effect on the eventual solar cell performance. For argon, this problem does not arise since argon is an inert gas. Therefore, higher energies can be used for argon implantation. Thus, 5 energies were used for argon: 5, 50, 100, 150 and 200 keV. All implantations were performed using a dose of 10^{16} ions/cm^2. The results for the phosphorus implantation are shown first.

The two phosphorus implantation energies were tested for two a-Si thicknesses, 0.5 and 2 µm. The results are shown in figure 4.10. For the 0.5 µm samples it is evident that the crater size reduces with higher implantation energies. The AFM analysis in table 4.2 shows that this is indeed the case. When the implantation energy increased from 5 to 50 keV, the mean crater diameter decreased from around 257 nm to 240 nm. As mentioned before, higher implantation energies causes the phosphorus to penetrate further into the a-Si layer, and eventually into the crystalline silicon layer. Since the same implantation of 10^{16} ions/cm^2 is used for both energies, the dopant density in the a-Si decreases for larger energies. Lower dopant densities are likely to lead to smaller grain size of the created polycrystalline silicon.[55][5] This would explain the reduction in crater size for the 0.5 µm a-Si samples. For the 2 µm samples, the higher implantation energy seems to lead to a small increase in the crater size. This is again confirmed by the AFM analysis which shows that the mean crater diameter increased from 260 nm to 274 nm. An explanation for this could also be related to the implantation depth of the phosphorus. For small implantation energies, the phosphorus ions do not reach the bottom of the a-Si layer during the anneal. Therefore, for the silicon atoms in the a-Si that are close to the crystalline silicon surface, there are no phosphorus atoms to facilitate diffusion which leads to smaller grains in the resulting polycrystalline silicon.[55][5] At higher implantation energies, these phosphorus atoms are more likely to be present, which could increase the grain size of the polycrystalline silicon close to the surface of the crystalline silicon.

The AFM measurements also show that the average roughness of the 0.5 µm, 5 keV P implantation is the largest of the four samples. However, the low roughness of the 2 µm samples could be explained by over-etching.



(a) Phosphorus 5 keV implantation in an a-Si layer of 0.5 µm. (b) Phosphorus 50 keV implantation in an a-Si layer of 0.5 µm.



(c) Phosphorus 5 keV implantation in an a-Si layer of 2 µm. (d) Phosphorus 50 keV implantation in an a-Si layer of 2 µm.

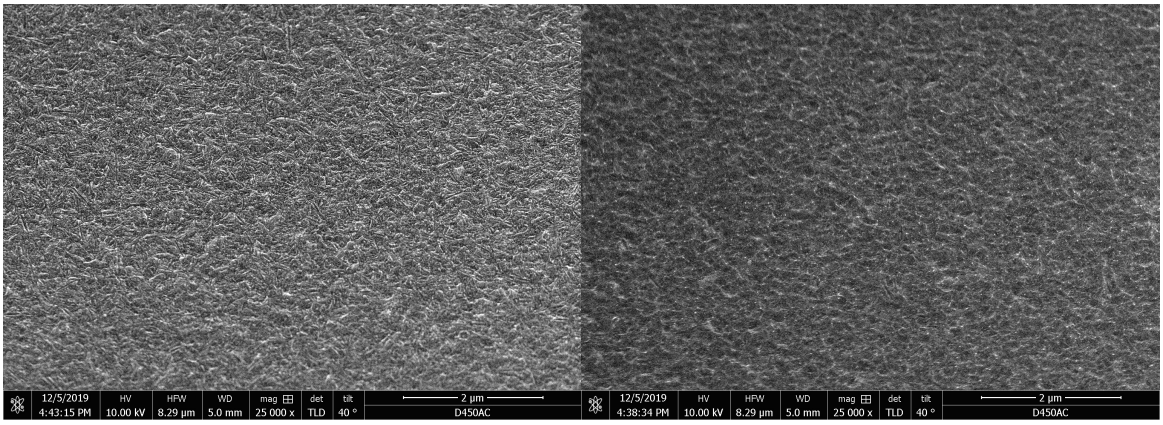
Figure 4.10: SEM images of different phosphorus implantation energies used in the sacrificial layer process.

Layer thickness (µm)	Implantation	Mean pore diameter (nm)	Average roughness (nm)
0.5	P 5 keV	256.9 ± 8.4	9.5
0.5	P 50 keV	239.8 ± 5.6	8.1
2	P 5 keV	260.0 ± 8.0	8.0
2	P 50 keV	273.8 ± 9.0	8.2

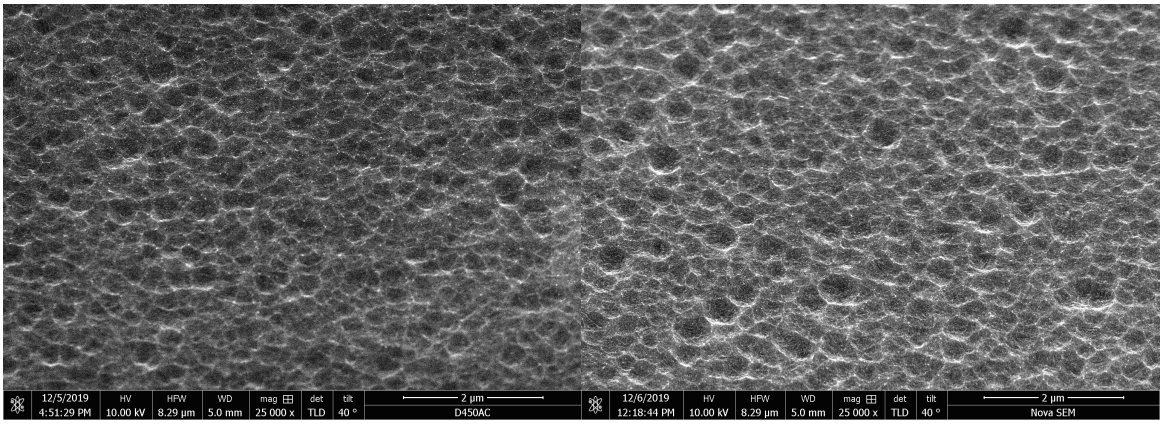
Table 4.2: AFM analysis of phosphorus implantation energy series.

The argon energy series was performed using 1 µm layers of a-Si, since this thickness showed the best results in the thickness series. The results are shown in figure 4.11. These SEM images show that for an implantation energy of 5 keV, no craters are originated from the process. The 25 keV implantation shows small craters, which become larger with higher energies. The AFM analysis in table 4.3 shows that this is indeed correct, the energies of 50, 100 and 200 keV result in larger craters (respectively 264, 257 and 249 nm in diameter) than the lower energies of 5 and 25keV (respectively 204 and 204 nm in diameter). This could be explained by the damage done by the argon at higher energies. For these energies, the argon penetrates the entire layer of a-Si. Before, this layer could have had a small percentage of crystallinity but these high energy argon atoms completely amorphize this layer. During the anneal, the combination of argon diffusion in the material and the completely amorphous silicon might result in larger grains of polycrystalline silicon.
However, table 4.3 also shows that the mean pore diameter has an optimum for an energy of 50 keV and decreases slightly for higher energies. Unexpectedly, even though the mean pore diameter decreases slightly for energies beyond 50 keV, the average roughness increases.

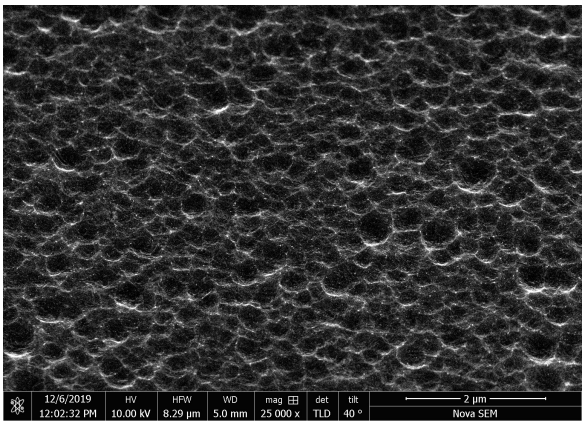
This might be caused by the damage done to the monocrystalline silicon surface by the high energy argon implantation.
It is also noteworthy that even though the SEM images show that no craters originate from the 5 keV implantation, the AFM analysis software still measures a mean pore diameter of 200 nm, which is clearly not the case. For small textures, the software links multiple of the small textures together during the mean pore size analysis. Thus, the calculated mean pore size is overestimated. An example of this problem is shown in appendix B.



(a) Argon 5 keV implantation. (b) Argon 25 keV implantation.



(c) Argon 50 keV implantation. (d) Argon 100 keV implantation.



(e) Argon 200 keV implantation.

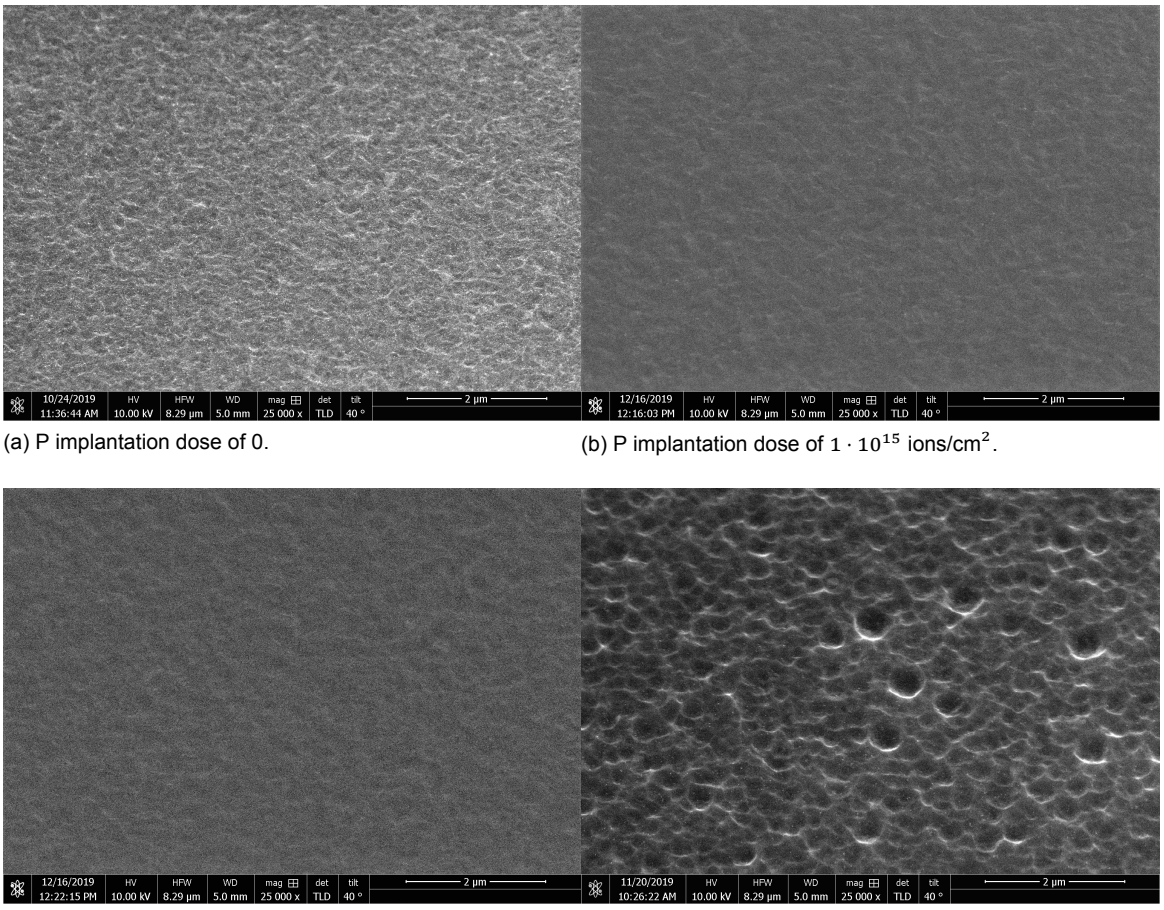
Figure 4.11: SEM images of different argon implantation energies using a 1 µm layer of a-Si in the sacrificial layer process.

Layer thickness (µm)	Implantation	Mean pore diameter (nm)	Average roughness (nm)
1	Ar 5 keV	203.5 ± 4.4	5.6
1	Ar 25 keV	203.5 ± 4.8	5.6
1	Ar 50 keV	264.0 ± 8.0	8.6
1	Ar 100 keV	257.0 ± 7.6	10.1
1	Ar 200 keV	248.9 ± 6.2	12.9

Table 4.3: AFM analysis of argon implantation energy series.

Implantation dose

The effect of the implantation dose was also examined. This was tested using an a-Si layer of 1 µm with three different implantation doses: $1 \cdot 10^{15}$, $5 \cdot 10^{15}$ and $1 \cdot 10^{16}$ ions/cm^2. For reference, the process was also done without implantation, so with a dose of 0. Phosphorus was implanted at an energy of 5 keV. The results are shown in figure 4.12. These figures show that no useful craters are created at lower implantation doses. AFM analysis, shown in table 4.4, was used to confirm this. These results clearly show that the crater size increases with the implanted phosphorus dose to a maximum average diameter of 277 nm at the highest dose. This sample also has the largest average roughness. Thus, it is likely that the polycrystalline silicon grain size is very dependent on the implanted dopant concentration. This could be caused by the increased diffusion coefficient shown by Wada et al.[55]
Also important to note is that the mean pore diameter for the implantation doses of 0, $1 \cdot 10^{15}$, and $5 \cdot 10^{15}$ shown in table 4.4 are again likely to be overestimated, as is explained in appendix B.



(a) P implantation dose of 0.

(b) P implantation dose of $1 \cdot 10^{15}$ ions/cm^2.

(c) P implantation dose of $5 \cdot 10^{15}$ ions/cm^2.

(d) P implantation dose of $1 \cdot 10^{16}$ ions/cm^2.

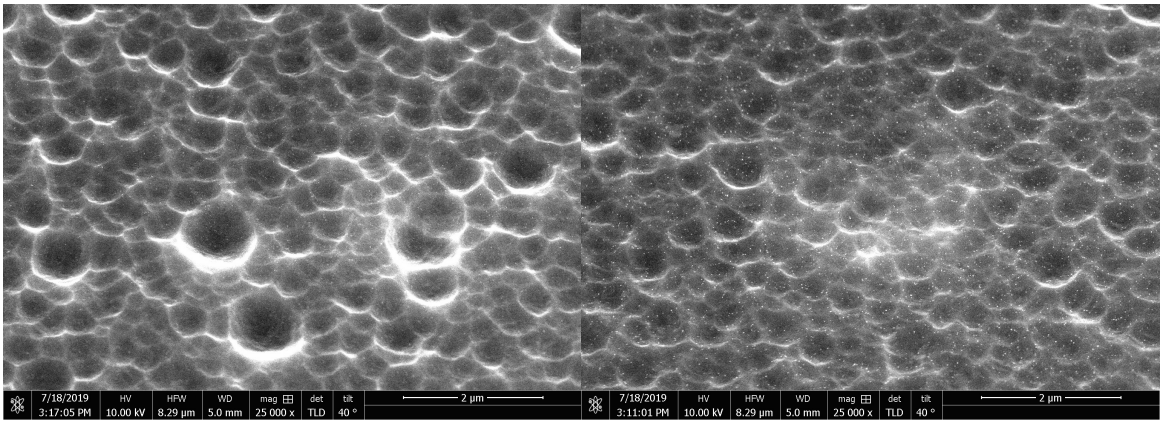
Figure 4.12: SEM images of different phosphorus implantation doses used in the sacrificial layer process.

Layer thickness (µm)	Implantation	Mean pore diameter (nm)	Average roughness (nm)
1	0 ions/cm^2	193.1± 3.6	5.3
1	$1 \cdot 10^{15}$ ions/cm^2	216.3 ± 5.4	6.7
1	$5 \cdot 10^{15}$ ions/cm^2	228.7 ± 6.3	5.7
1	$1 \cdot 10^{16}$ ions/cm^2	276.6 ± 8.0	15.9

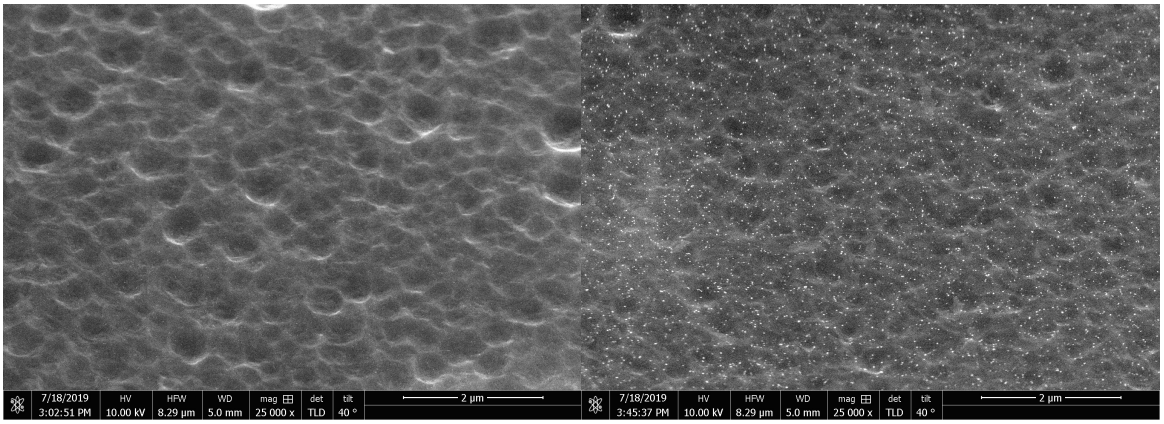
Table 4.4: AFM analysis of phosphorus implantation dose series at an energy of 5 kev.

Anneal time and temperature

Differences in anneal time and temperature can have significant effect on the grain size of the polycrystalline silicon that is created.[55][5][7] Therefore, effects of changes in these parameters were examined. For this purpose, two relatively high temperature anneals were tested in this thesis, 950 °C and 1050 °C. For the anneal time, a short anneal time of 5 minutes and a long anneal time of 60 minutes was used. The other parameters were kept the same: 1 µm of a-Si, 5keV $1 \cdot 10^{16}$ ions/cm^2 P implantation. These samples were investigated using SEM and AFM. The SEM images will be shown first, in figure 4.13. These images show that 950 °C samples show the largest craters. Looking at these images, the 5 minute anneal seems to create the largest craters. The short anneal for 1050 °C shows smaller craters compared to the 950 °C samples, while the 1050 °C long anneal samples show even smaller craters. The results of the AFM measurements are shown in table 4.5. These measurements show that indeed the 950 °C samples show the largest craters, with diameters of 411 and 431 nm for respectively the short and long anneal time. The longer anneal time shows a larger mean pore diameter but since the error of the two measurements incorporate the value of the other measurement, this conclusion cannot be drawn with full certainty. The 1050 °C short time sample shows smaller craters, with an averare diameter of 294 nm, compared to the 950 °samples. Also, the crater size at 1050 °C decreases for longer anneal time, to a diameter of 196 nm. This could be caused by almost full crystallization of the a-Si layer. If the crystallinity fraction of the silicon becomes too large, there are too few grain boundaries for the etchant to go through. This prohibits the creation of craters in the a-Si. It is also important to note that the created craters during this test were much larger compared to the craters that originated from the other tests: average crater diameter of 431 ±40 compared to 277 ±8 nm. The cause of this difference will be thoroughly discussed in the recommendations section.



(a) 5 minutes anneal at 950 °C. (b) 60 minutes anneal at 950 °C.



(c) 5 minutes anneal at 1050 °C. (d) 60 minutes anneal at 1050 °C.

Figure 4.13: SEM images of different anneal times and temperatures for the sacrificial layer method using phosphorus implantation.

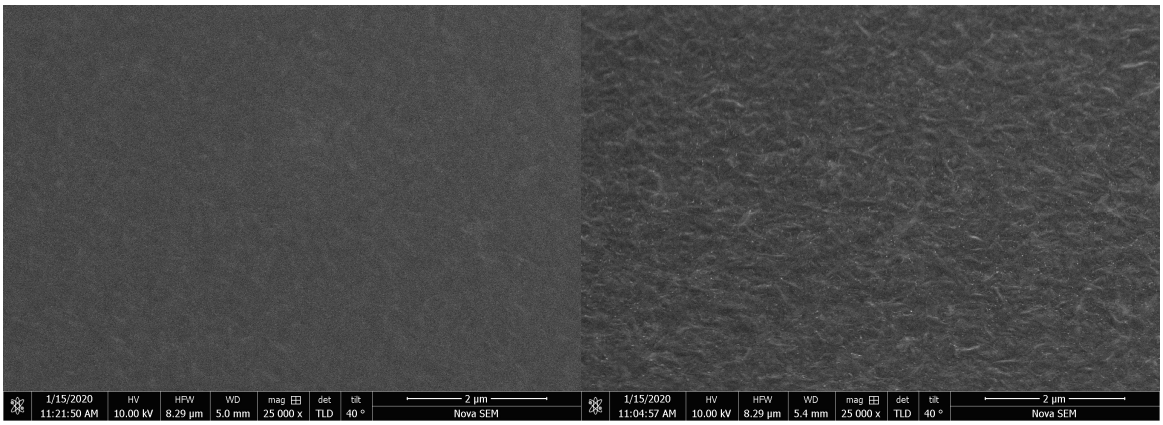
Anneal temperature (°C)	Anneal time (min)	Mean pore diameter (nm)	Mean roughness (nm)
950	5	411 ± 44	69.3
950	60	431 ± 40	67.2
1050	5	294 ± 22	26.9
1050	60	196 ± 12	15.4

Table 4.5: AFM analysis of different anneal times and temperatures for the sacrificial layer method using 1 µm of a-Si and 5 keV phosphorus implantation.

Implanted ion

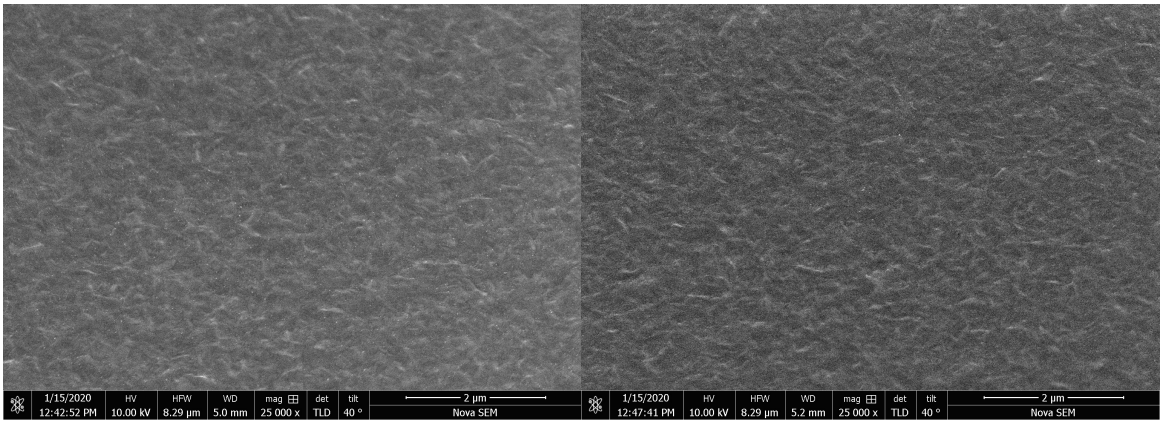
Up until now, only phosphorus and argon were used for ion implantation. As was mentioned in section 3.2.3, there are five available ions for implantation: Boron (B), Phosphorus (P), Argon (Ar), Arsenic (As), and Boron Difluoride (BF_2). These ions were tested in the sacrificial layer method. For this test, the a-Si thicknesses of 1 and 2 µm were used since these resulted in the largest crater sizes. The anneal conditions were the same during this test, a temperature of 950 °C for 60 minutes. For boron, implantation energies of 5 and 50 keV were used. This was done since higher energies could lead to unwanted doping in the crystalline silicon, which has a negative effect on the eventual solar cell performance. For arsenic and boron difluoride, energies of 200 and 250 keV were used. These relatively high energies were used since these ions are heavier and therefore need higher energies to penetrate into the a-Si layer. For argon, the thickness of 2 µm and the energy of 250 keV was not performed in earlier measurements. Therefore, argon implantation was performed at 100, 200 and 250

keV for the two thicknesses. The results for the boron implantations are shown in figure 4.14. This shows that the boron implantation results in practically no craters. Therefore, these samples were not examined using the AFM.



(a) Boron 5 keV implantation in 1 µm of a-Si.

(b) Boron 50 keV implantation in 1 µm of a-Si.

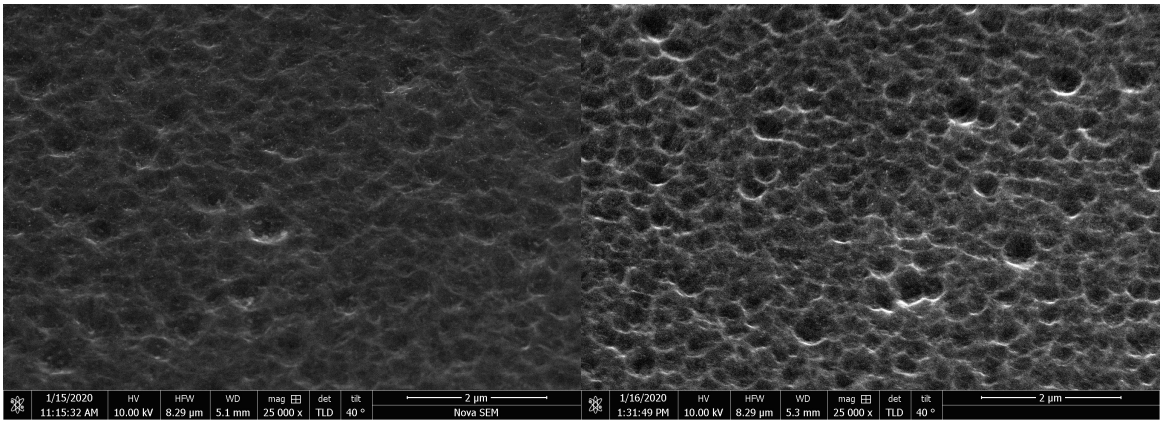


(c) Boron 5 keV implantation in 2 µm of a-Si.

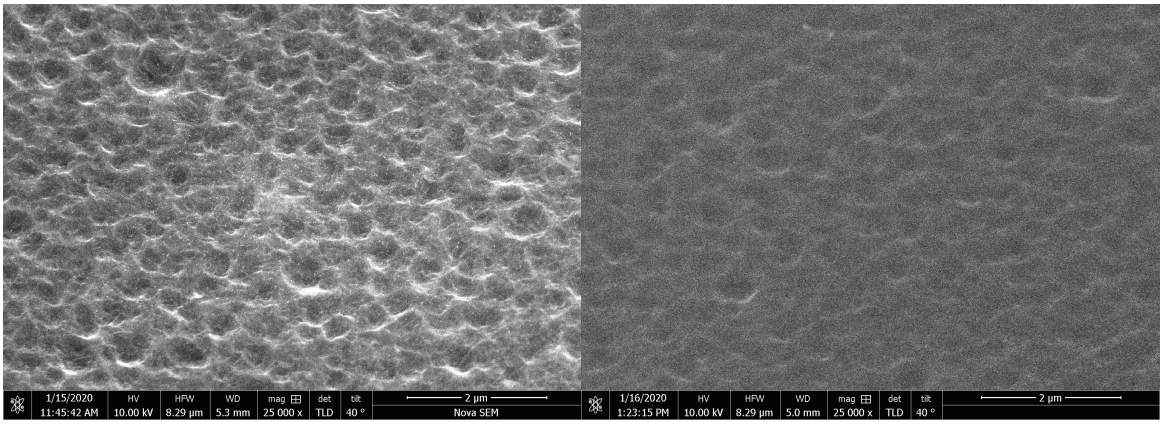
(d) Boron 50 keV implantation in 2 µm of a-Si.

Figure 4.14: SEM images of different boron implantation energies for 1 and 2 µm a-Si in the sacrificial layer process.

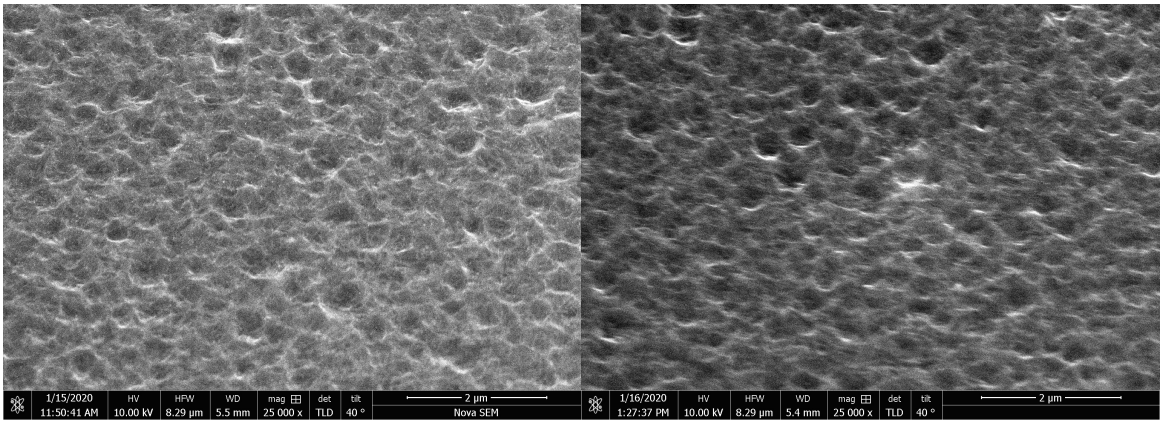
The results of the argon implantation is shown in figure 4.15. These images show that craters originate from all used argon implantations. However, the differences are quite small and therefore difficult to distinguish with the naked eye. Therefore, the AFM analysis is used to draw conclusions from these implantations, shown in table 4.6. For the 1 µm samples, the mean pore diameter remains fairly constant when the implantation energy increases from 100 to 200 keV at around 252 nm. However, the 250 keV sample shows a clear increase to 313 nm. The 2 µm samples show a small increase in mean crater diameter from 276 to 288 for an energy increase from 100 to 200 keV. However, the largest energy of 250 keV shows a significant increase up to 320 nm average diameter. Since the error of the two largest mean diameters, for 250 keV in 1 µm and in 2 µm, incorporates the other value, the best sample cannot be chosen with full certainty.



(a) Argon 100 keV implantation in 1 µm of a-Si. (b) Argon 100 keV implantation in 2 µm of a-Si.



(c) Argon 200 keV implantation in 1 µm of a-Si. (d) Argon 200 keV implantation in 2 µm of a-Si.



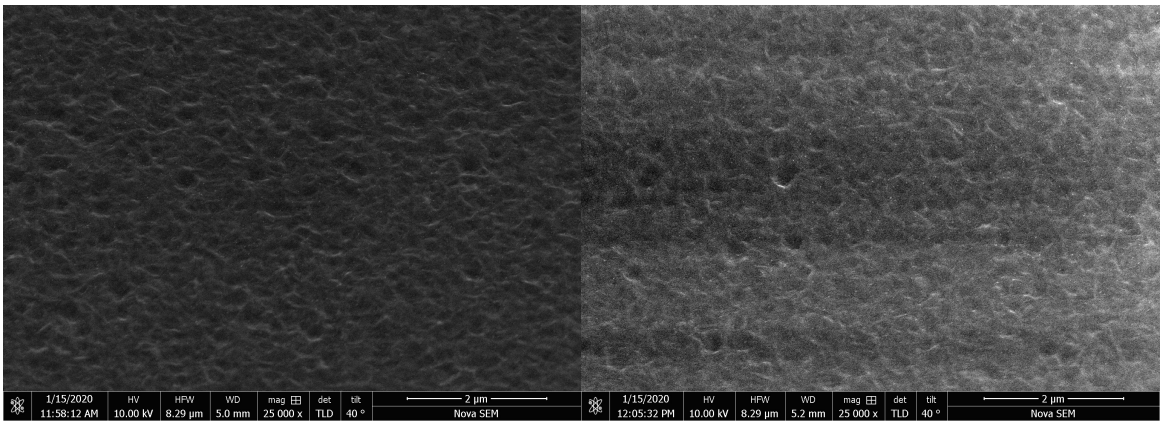
(e) Argon 250 keV implantation in 1 µm of a-Si. (f) Argon 250 keV implantation in 2 µm of a-Si.

Figure 4.15: SEM images of different argon implantation energies using a 1 µm layer of a-Si in the sacrificial layer process.

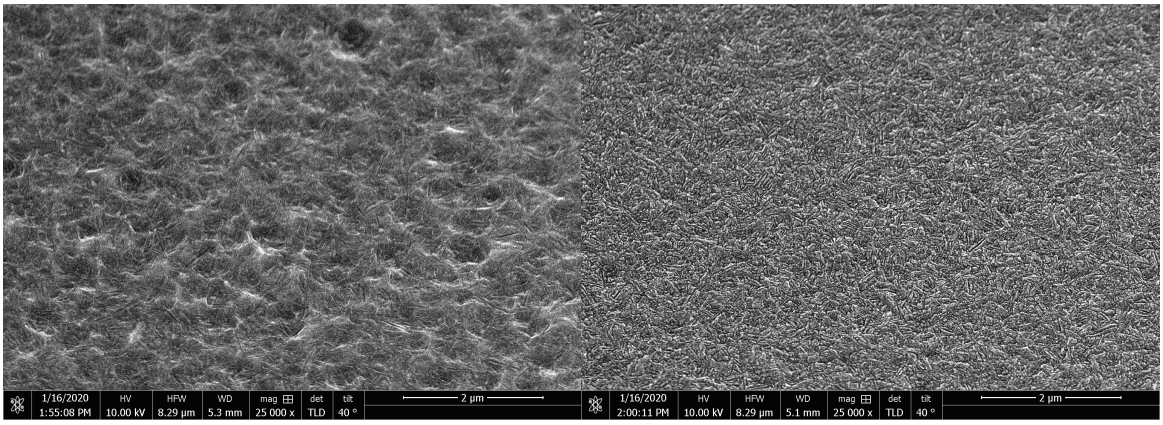
Layer thickness (µm)	Implantation	Mean pore diameter (nm)	Average roughness (nm)
1	Ar 100 keV	253.0 ± 8.5	14.8
1	Ar 200 keV	251.1 ± 6.7	16.2
1	Ar 250 keV	313.0 ± 12.0	15
2	Ar 100 keV	276.2 ± 12.7	14.9
2	Ar 200 keV	288.4 ± 10.9	14.5
2	Ar 250 keV	320.3 ± 14.3	15.2

Table 4.6: AFM analysis of argon implantation energy series.

The results of the boron difluoride implantation is shown in figure 4.16. The 1 µm samples show craters that are similar in size, but smaller than the craters that were created using argon. For the 2 µm saples, the 200 keV sample shows craters that are similar to the argon samples, but more shallow. While the 250 keV sample does not show craters at all. AFM imaging was not performed on these samples since they showed less promise in terms of average crater size compared to the argon implanted samples.



(a) BF_2 200 keV implantation in 1 µm of a-Si. (b) BF_2 250 keV implantation in 1 µm of a-Si.

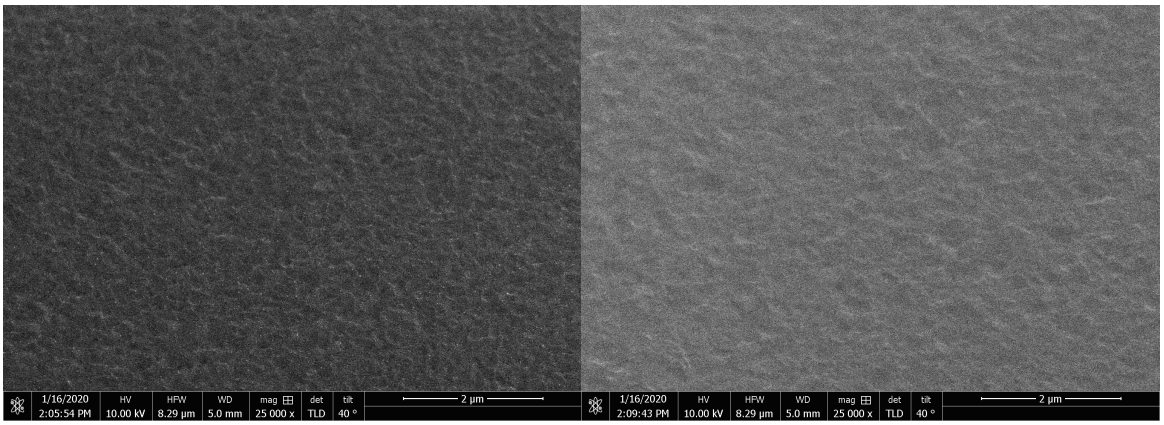


(c) BF_2 200 keV implantation in 2 µm of a-Si. (d) BF_2 250 keV implantation in 2 µm of a-Si.

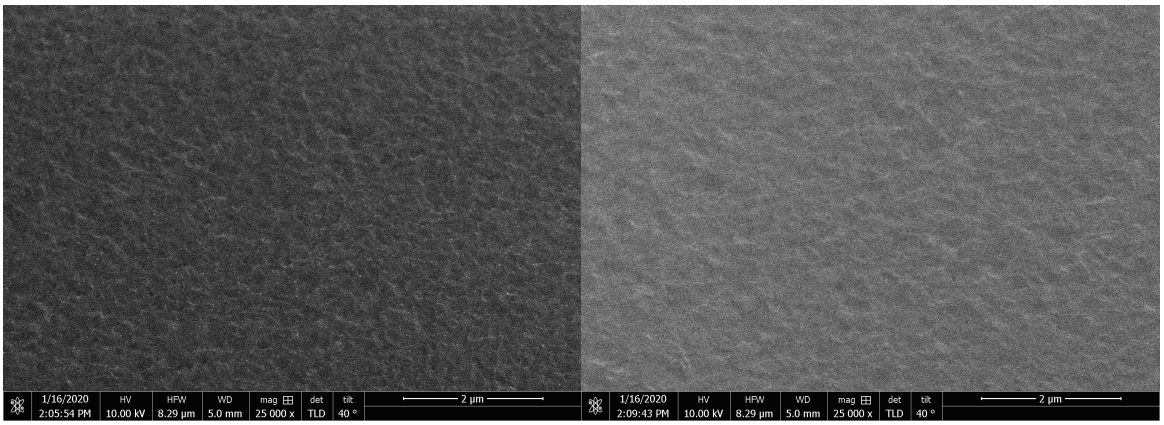
Figure 4.16: SEM images of different boron difluoride implantation energies for 1 and 2 µm a-Si in the sacrificial layer process.

Finally, the results of the arsenic implantation samples are shown in figure 4.17. These images show no sign of the formation of craters on the surface. This could be caused by the weight of the arsenic ions. These are the heaviest particles used for implantation and therefore have a smaller implantation depth. Thus, these a-Si layers might be too thick for the ions to reach the crystalline silicon surface during the anneal. Therefore, the polycrystalline grain size near the surface is small, which ruins the formation of craters on the crystalline

silicon surface. Since these surfaces show no sign of craters, they were not examined using AFM.



(a) As 200 keV implantation in 1 µm of a-Si. (b) As 250 keV implantation in 1 µm of a-Si.

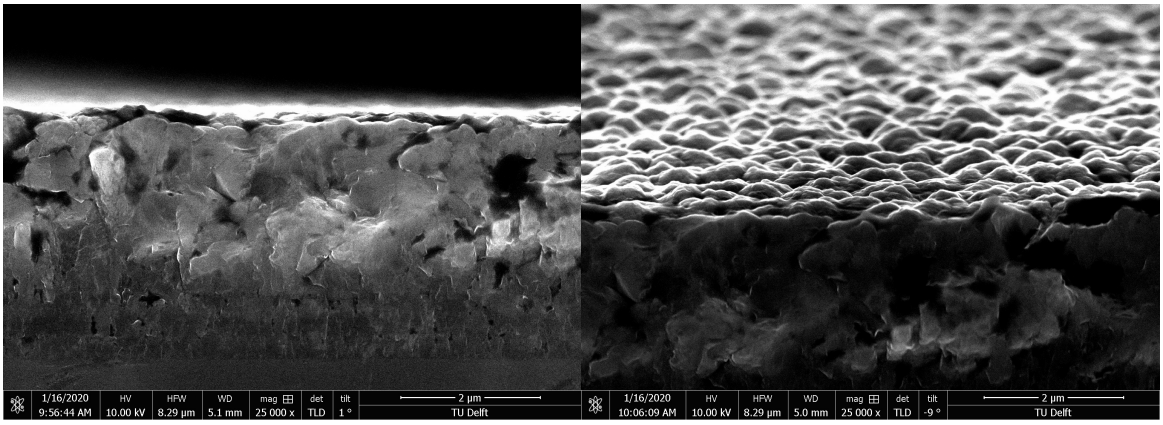


(c) As 200 keV implantation in 2 µm of a-Si. (d) As 250 keV implantation in 2 µm of a-Si.

Figure 4.17: SEM images of different arsenic implantation energies for 1 and 2 µm a-Si in the sacrificial layer process.

4.2.2. Nanocrystalline silicon test

The nano-crystalline silicon crack test was also performed on the texture created with the sacrificial layer method. Since the argon samples showed the most potential, the texture created using 1 µm of a-Si with 250 keV argon implantation. The results were examined using SEM and the result is shown in figure 4.18. These images show that the nc-Si layer obtained does not show obvious cracks created by the surface. Figure 4.18b shows that the top of the nc-Si layer copies the texture of the crystalline silicon, but reversed. Therefore, the craters result in blunt hills on top of the nc-Si layer.



(a) Side view of nc-Si on texture. (b) Top view of nc-Si on texture.

Figure 4.18: SEM images of 3 µm of nc-Si on texture created using sacrificial layer method using an a-Si layer of 1 µm and 250 keV Ar implantation.

4.3. Optical performance

The crystalline silicon is the bottom layer of the eventual triple junction solar cell. As the bottom cell, this layer should ensure that part of the light that is reflected light, is scattered into wide angles. This increases the optical path length through the top two absorbers of the top two solar cells, which increases absorption and thus efficiency. The wafer texture is copied by subsequent layers. Therefore, it is profitable if the texture of this layer promotes light incoupling and therefore has low reflectance. Both the reflectance and light scattering were measured and will be shown in this section.

4.3.1. Reflectance

The reflectance was measured for a wavelength range between 300 and 1200 nm using the lambda 1050. This was done for both the photolithography and the sacrificial layer samples. As mentioned, a low reflectance is desired. For the photolithography samples, two effects were examined. First, the reflectance of the hexagonal figures that were created using the two different masks was compared. Second, the effect of over-etching was examined using the 3 µm period, which will be used for the creation of SHJ's. For the sacrificial layer samples, the effect of the creation of the craters on the reflectance was inspected. Afterwards, the reflectance of both texturing types is compared.

Photolithography

The reflectance of the created textures using the two different masks is shown in figure 4.19. For recollection, mask 1 creates a hexagonal texture with a period of 2 µm, while mask 2 creates a hexagonal texture with a period of 3 µm. This graph shows that the reflectance of the textures are very similar between 300 and 450 nm. After this, the reflectance of the larger period texture becomes lower. This remains until a wavelength of 1150 nm, after which the texture created by mask 1 has a lower reflectance. The lower reflectance of the hexagonal texture created using mask 2 can be explained. Since both mask have the same hole diameter, the etch distance for mask 2 is larger than for mask 1. Therefore, the semi-spherical walls of the hexagonal texture are larger for the texture with the larger period, which promotes light incoupling and therefore decreases the reflectance.

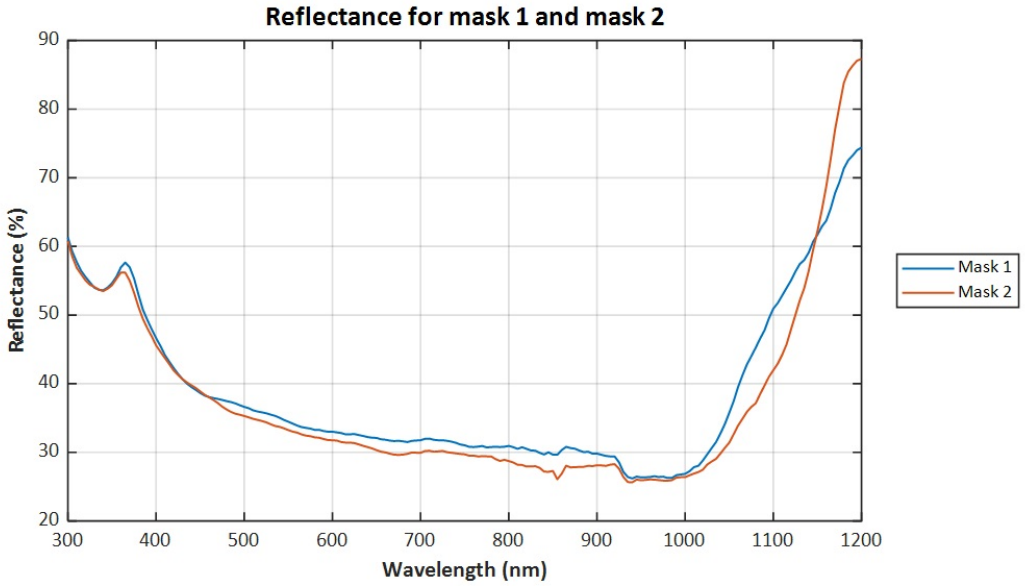


Figure 4.19: Reflectance of hexagonal textures with two different periods created using photolithography. Note that the scale is from 20 to 90%.

The effect of etch time on the reflectance created hexagonal texture is shown in figure 4.20. The minimum etch time to create the hexagonal texture for this period was 12 minutes, as was shown in section 4.1.1. Therefore, the 10 minute etch time sample is a bit under-etched and all etch times beyond that are over-etched. The figure shows that the reflectance decreases with longer etch times. This was expected since over-etching causes the texture to flatten. As was explained in section 4.1.2, when the sample is etched too long, the edges of the texture are more exposed to the etchant compared to the bottom of the texture since the etching reactants are expelled from the surface more easily. Therefore, the sides are more vulnerable to being etched. The consequence of this effect is that over-etching causes the surface to flatten, which decreases incoupling and therefore increases reflectance.

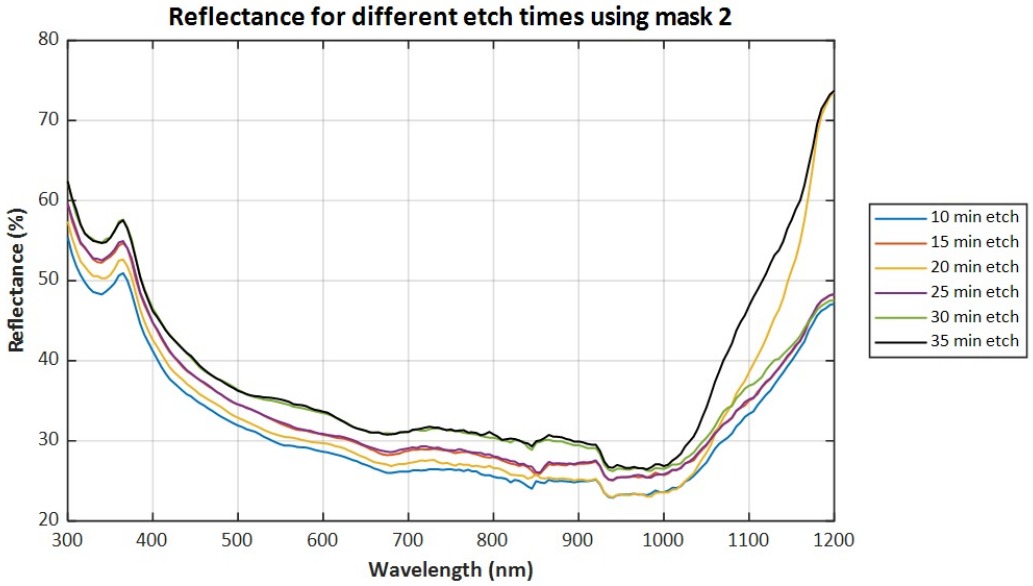
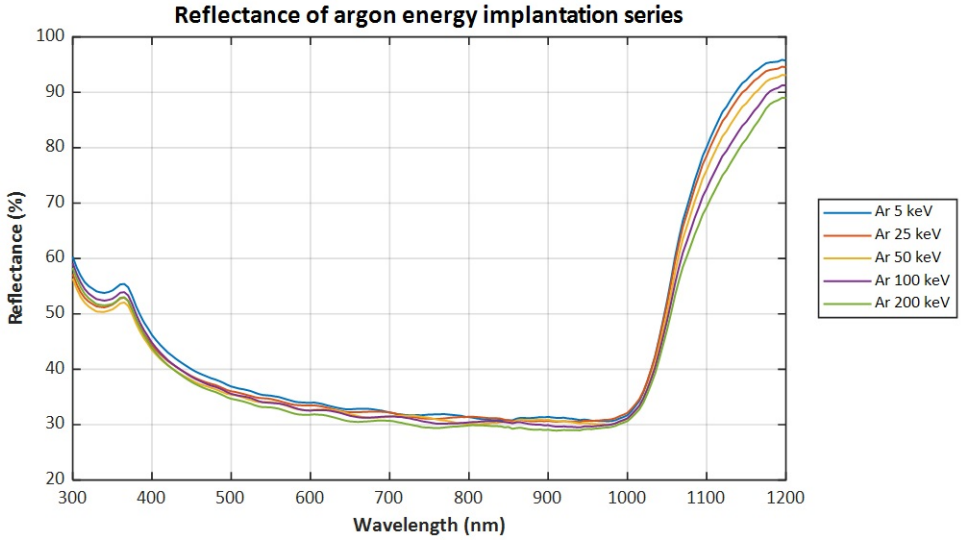


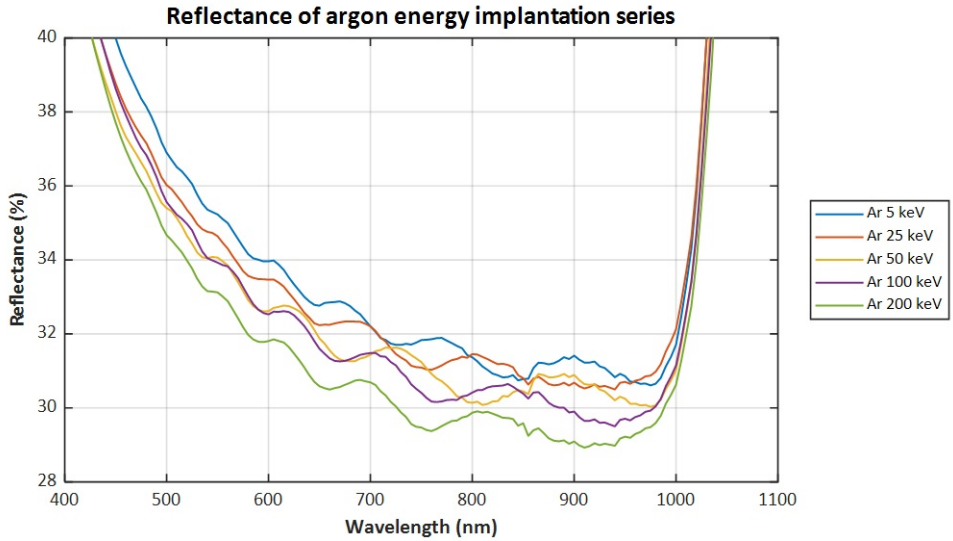
Figure 4.20: Reflectance for different etch times of hexagonal textures with a period of 3 µm created using photolithography. Note that the scale is from 20 to 80%.

Sacrificial layer

The effect of the creation of craters in the crystalline silicon surface on the reflectance is shown in this section. For this purpose, the reflectance of the argon energy series was used since these samples showed a gradual change in the surface. At 5 keV, no craters were created. At 25 keV, small craters arose. At higher energies, the craters had an approximately constant size while the surface roughness steadily increased. These samples are a great example for the effect of the creation of craters and an increase of roughness on the reflectance. Other experiment series, such as the dose series and the layer thickness series, show the same trends in the reflectance measurements. Therefore, it was chosen to show only the argon series. The reflectance measurements of these samples is shown in figure 4.21. Since the measurements are very close in the region between 400 and 1050 nm, a zoomed in version is also added. This graph shows that the reflectance decreases over the entire wavelength range when the craters are created on the crystalline silicon surface. Also, as the roughness of the samples increases, the reflectance decreases. This is as expected since the creation of these craters and an increase in roughness both promote incoupling of light.



(a) Full graph.



(b) Zoomed in graph.

Figure 4.21: Reflectance of textures created with the sacrificial layer method using different implantation energies for argon. Note that the scale is from 20 to 100% for (a) and 28 to 40 % for (b).

Optical Comparison of Photolithography and Sacrificial Layer Method

This section is dedicated to the comparison of the reflectance of the samples textured using the different techniques. The samples that are compared are the photolithography and sacrificial layer method samples that were used during the crystalline silicon tests: the 3 µm period hexagonal texture sample that was etched for 12 minutes and sacrificial layer sample using 250 keV argon implantation in 1 µm of a-Si. The reflectance of these samples was also compared to the reflectance of the large craters that were obtained during the anneal temperature and time tests. For reference, a flat/untextured wafer was also measured. The result is shown in figure 4.22. This measurement shows that for small wavelengths, the reflectance of the argon implanted sacrificial layer samples is the lowest, followed by respectively the photolithography samples and the anneal test samples. Between 400 and 600 nm, the reflectance of the three different samples is really close, after which the anneal test sample has the best reflectance up until 800 nm. Between 800 and 1050 nm, the photolithography sample have the lowest reflectance, followed by respectively the anneal test sample and the argon sacrificial layer sample. The figure also demonstrates that the reflectance decreases compared to flat for all textures. The average reflectance over this wavelength range was also calculated. For photolithography, the mean reflectance is 37.7% compared to 38.2% for the anneal sacrificial layer sample, 41.5% for the argon implanted sacrificial layer sample and 45.8 % for the untextured wafer. This indicates that the hexagonal texture made with photolithography results in the best incoupling of light. This is respectively followed by the large craters created during the anneal sacrificial layer test sample and the smaller craters of the argon implanted sacrificial layer sample.

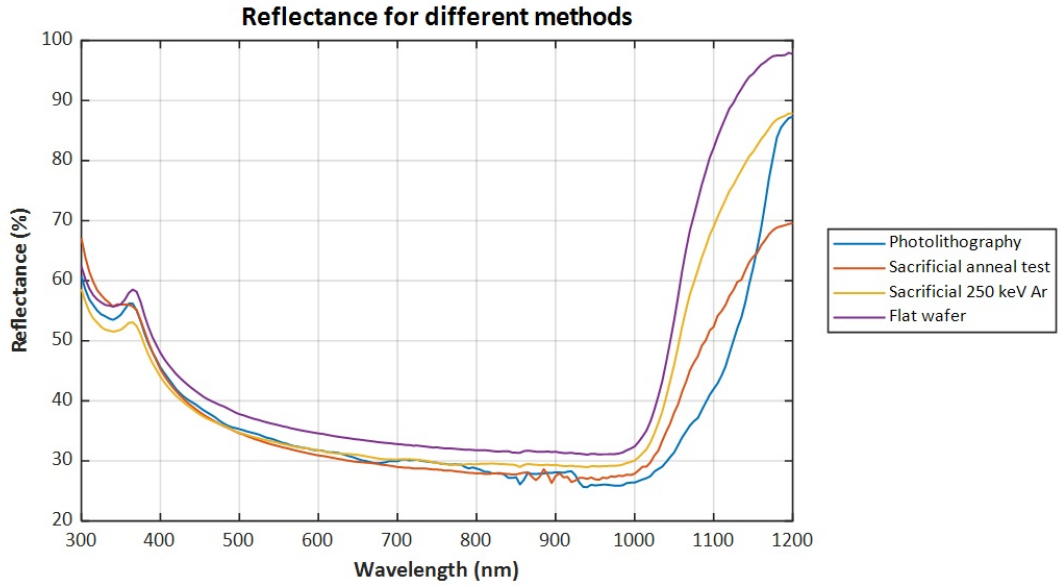
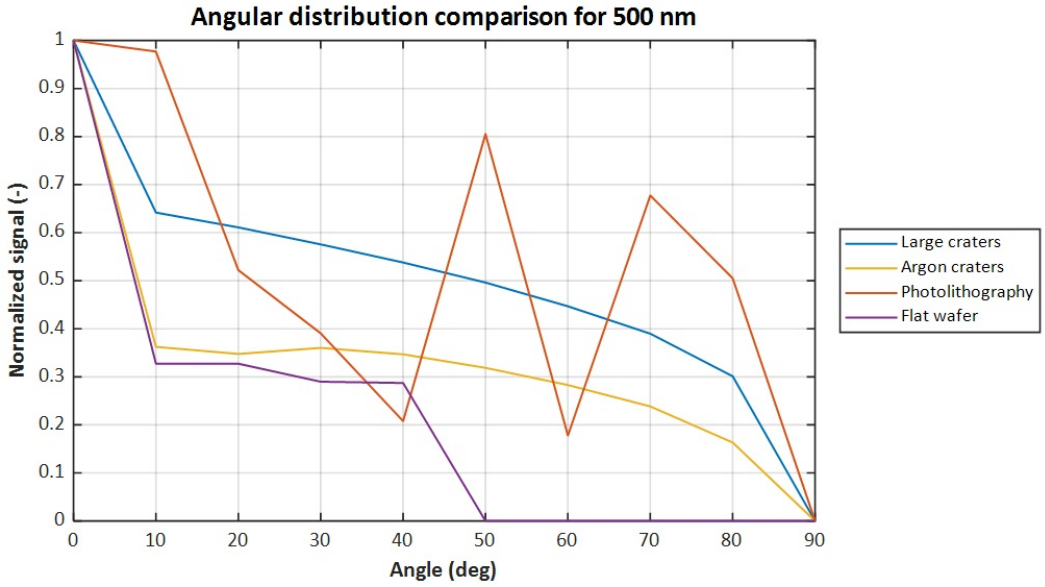


Figure 4.22: Reflectance of textures created with the sacrificial layer method compared to hexagonal textures created using photolithography.Note that the scale is from 20 to 100%.

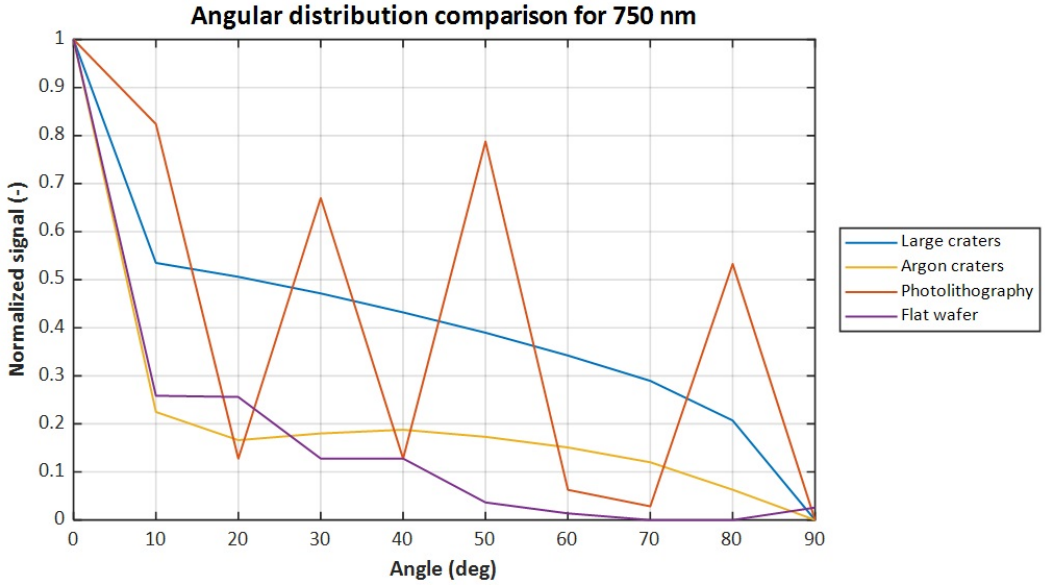
4.3.2. Light scattering

As mentioned before, the textures are created on the bottom layer of the eventual triple junction solar cell. Therefore, light that is reflected by this layer should be scattered into wide angles to increase the pathway of the light through the absorbers of the two solar cells that are created on top. The light scattering was examined by measuring the angular distribution of the reflected light using the ARTA on the lambda 950. The angular distribution of reflectance can be used to understand the light scattering effect of the different samples. The angular distribution of reflectance was measured for three different samples: the 3 µm period hexagonal texture sample that was etched for 12 minutes, the sacrificial layer sample using 250 keV argon implantation in 1 µm of a-Si, and the large crater samples that were obtained during the anneal temperature and time tests. For reference, a flat, polished wafer was also

measured. The results are shown in figure 4.23 for two different wavelengths: 500 nm and 750 nm. These figures show that the reflectance of the hexagonal texture from photolithography is very dependent on the measured angle. Also, if the two images are compared, it shows that the angular dependence varies for different wavelengths. The random textures created with the sacrificial layer method do not show the same results. The results for the large craters show light scattering into wider angles compared to the flat surface, which happens for both the 500 and 750 nm light. This light scattering is at approximately the same level as the photolithography samples, but more gradual over different angles. The smaller craters from argon implantation show the same gradual scattering of light as the large craters, but at a lower level. This indicates that both the hexagonal texture and large craters from the sacrificial layer method are suitable for light scattering.



(a) Angular distribution of reflectance comparison for 500 nm light.



(b) Angular distribution of reflectance comparison for 750 nm light.

Figure 4.23: Angular distribution of reflectance comparison for 500 and 750 nm light.

4.4. Silicon heterojunction solar cells

The created textures were used to produce SHJ's. This process was done as described in section 3.3.4. For these SHJ's, the hexagonal texture with a period of 3 µm was used and argon implantation at 250 keV in 1 µm of a-Si was used for the sacrificial layer texture. The deposition rate of the different layers are dependent on the surface texture on which the layer is deposited. The deposition rate on a flat surface is different than the deposition rate on a textured surface. Since the textures created in this research were not used in SHJ's before, multiple deposition times were used during the production of these cells. The charge carrier lifetimes and IV-curves of these cells were measured and will be shown in this section.

4.4.1. Charge carrier lifetime

Minority charge carrier lifetime measurements give an indication of the quality of the layers in the created SHJ. A low charge carrier lifetime can for example indicate a large defect density, bad adhesion between the layers, or badly optimized layer thicknesses. The results of these measurements for the SHJ's using the sacrificial layer texture and the hexagonal texture are shown respectively in tables 4.7 and 4.8. The deposition time of all layers was varied. Wafer number 1 corresponds to the longest deposition times while wafer number 5 corresponds to the shortest deposition times. The exact times will be shown in appendix C. These measurements were carried out before the TCO was applied to the cell. These results show that the minority charge carrier lifetimes are very low for the sacrificial layer textured samples, around 2.4 µs. The lifetime of the hexagonal texture SHJ's is better, between 48.6 and 141 µs. However, these values are still very low for a solar cell. For these SHJ's it is aimed to have a lifetime of between 2000 and 4000 µs. The most logical explanation for this is that deposition rate of a-Si is smaller than anticipated. This results in layers that are too thin to carry out their function in the SHJ. If the passivation layers become too thin, the dangling bonds are not entirely passivated. This is detrimental to the lifetime of the minority charge carriers.

Deposition time (min)	1	2	3	4	5
Minority charge carrier lifetime (µs)	2.39	2.41	2.41	2.40	2.37

Table 4.7: Lifetime measurement of SHJ using sacrificial layer texture created with argon implantation.

Deposition time (min)	1	2	3	4	5
Minority charge carrier lifetime (µs)	76.71	55.14	64.461	141.03	48.63

Table 4.8: Lifetime measurement of SHJ using hexagonal texture created with photolithography.

4.4.2. IV-curve

The IV-curves of these solar cells were measured to find important PV parameters of the SHJ's. These parameters characterize the performance of these cells. The parameters that will be shown in this section are the efficiency, the short circuit current density, the open circuit voltage and the fill factor. The created SHJ's were 4 by 4 mm. The IV curves were measured for the SHJ's with the longest deposition time. The IV-curve data for 10 cells was collected for each texturing method, of which the average of the best three cells is shown in table 4.9. The results show that the efficiency and the fill factor of the SHJ's using the sacrificial layer texture are very low, at just 0.1% and 0.22 respectively. The cells using the hexagonal texture perform better, with an efficiency of 10.0 % and a fill factor of 0.57. Even though this is much better than the sacrificial layer texture cells, it is still lower than was anticipated. This is likely to have the same cause as the low minority carrier lifetime, a low deposition rate which caused even the thickest deposited a-Si layers to be too thin. This results in bad passivation, which decreases the minority carrier lifetime, which indicates that less of the created electron-hole pairs are collected at the contacts. This decreases the performance of the solar cell.

Texturing type	Efficiency(%)	FF(-)	V_{oc}(V)	J_{sc}(A/m^2)
Sacrificial layer	0.1	0.20	0.29	19.5
Hexagonal	10.0	0.57	0.57	309.1

Table 4.9: Parameters found from the IV-curve measurements.

4.4.3. Reflectance

As was mentioned before, the texture of the crystalline silicon wafer is copied by subsequent layers. Therefore, it is interesting to measure the reflectance of the SHJ and to compare it to the reflectance of just the texture. To show the effect of the TCO on the reflectance, the measurement was done with and without TCO. The results of these measurements are shown in figure 4.24. This figure shows that the reflectance of the SHJ with the hexagonal texture is lower at all wavelengths. The average reflectance over this range is 29.5% for the SHJ using the hexagonal texture compared to 32.7% for the sacrificial layer texture. The average reflectance of the SHJ compared to the texture in crystalline silicon dropped from 37.7% to 29.5 % for the hexagonal texture and from 41.5% to 32.7 % for the craters originated from the sacrificial layer texture. Figure 4.24 also shows that adding the TCO to the SHJ decreased the reflectance even further. More specifically, to an average reflectance of 13.4 % for the hexagonal texture and 14.4% for the sacrificial layer texture.

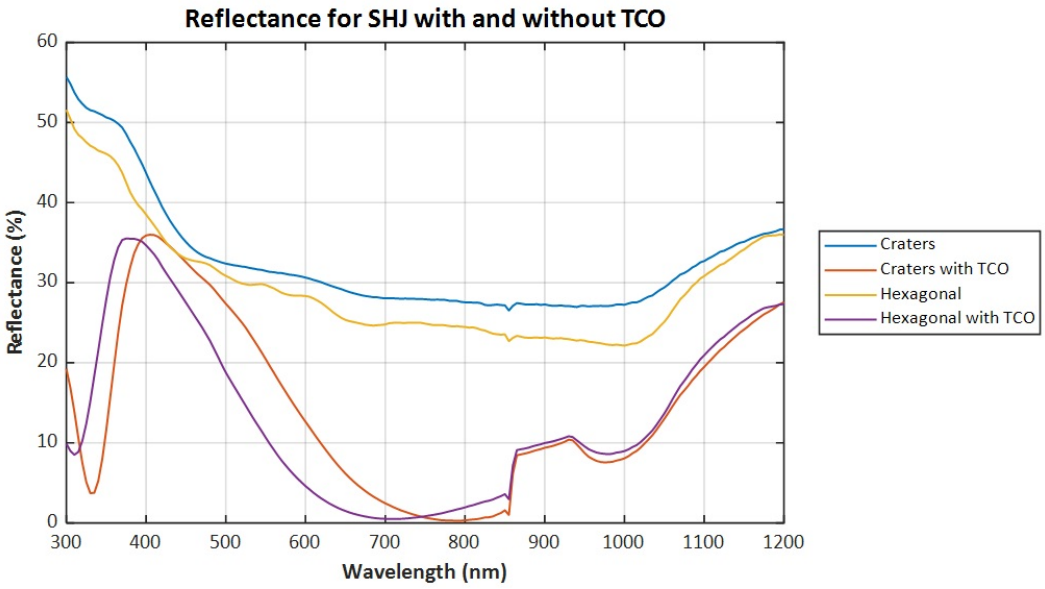


Figure 4.24: Reflectance of SHJ's using textures created with the sacrificial layer method compared to hexagonal textures created using photolithography.Note that the scale is from 0 to 60%.

5

Conclusions and Recommendations

This thesis was focused on the development of novel approaches for texturing crystalline silicon for multi-junction solar cell applications. More specifically, two new texturing methods were examined. The first was an approach to create a hexagonal texture using photolithography. The second made use of a sacrificial layer of polycrystalline silicon to create a random texture of craters. The most important findings of this research will be summarized in this chapter. This chapter will follow the order of the subgoals that were described in section 1.6. These subgoals were used to reach the main goal: to develop two new types of crystalline silicon texturization, eventually aimed to be used in a triple junction solar cell from monocrystalline silicon and two thin film silicon alloy layers.

5.1. Conclusions

The first subgoal of this research was to develop a process that results in a hexagonal texture on crystalline silicon. This process was described in section 3.1.4. During the design of this process, it was discovered that the etch rate of this poly-Si etch on crystalline silicon was unknown. Thus, the minimum etch time to create the hexagonal texture was found experimentally. This was done for two masks that were already available. The first mask (mask 1) resulted in a hole diameter of 1 µm and a hole period of 2 µm. The second mask (mask 2) also resulted in a hole diameter of 1 µm but resulted in a hole period of 3 µm. For mask 1, an mimimum etch time of 16 minutes was found. For mask 2, it was found that the etch rate was too low to result in the hexagonal texture. This was most likely caused by the accumulation of etching reactants in the holes of the silicon dioxide mask, which decreases the etch rate. Therefore, this etch process was altered to include water rinsing of the wafers to remove these etching reactants in between etch baths. This resulted in a hexagonal texture after a total etch time of 12 minutes.

The second subgoal was to design a photolithography mask that creates a hexagonal texture without generating cracks in a deposited layer of nc-Si:H. To do this, two thicknesses of nc-Si were deposited on the hexagonal textures created using both masks that were already available, which was shown in section 4.1.2. The used thicknesses were 3 and 5 µm. The SEM images showed that for the mask with the smaller period, cracks did develop in the nc-Si layers. These cracks did not appear for the hexagonal texture created using the mask with the larger period. Therefore, it was decided to use this period (3 µm) for the new mask design. The hole diameter of the new mask was decided to be 1 µm. This was done in order to consider the optimum height difference and the fact that there might be a difference in horizontal and vertical etch rate.

The third subgoal was to investigate the effect of different parameters on crater size of the random texture created with the sacrificial layer method. This crater size should be aimed to be around 3 to 3.5 µm on average. The parameters that were investigated in this research

are: the amorphous silicon layer thickness, the anneal temperature, the anneal time, the implanted ion and the ion implantation energy. During the examination of one parameter, the others were mostly kept constant.

The investigation of the effect of the a-Si layer thickness showed that the crater size increased on average when the layer thickness increased from 0 to 0.5 µm and from 0.5 to 1 µm. It also showed that for larger thicknesses, 2 and 4 µm, the average crater size went down again. This could be caused by the dopant concentration in the a-Si layer. If the layer is too thick, the phosphorus concentration near the crystalline silicon surface is too low. The poly-silicon grain size is dependent on the implanted impurity concentration. For larger a-Si thicknesses, the dopant concentration near the crystalline silicon surface might be lower compared to the concentration for thinner layers. This could result in smaller polycrystalline silicon grains, which results in smaller craters. The largest average crater diameter was found to be 277 nm.

For the ion implantation energy tests, phosphorus and argon were used. Phosphorus implantation was done at two energies, 5 and 50 keV, for two a-Si thicknesses, 0.5 and 2 µm. A higher implantation energy resulted in a decrease in the mean crater size for the 0.5 µm a-Si layer. This could be caused by phosphorus ions that penetrate into the crystalline silicon at higher energies, which decreased the dopant density in the a-Si. This results in smaller craters. The 2 µm a-Si layer showed opposite results. Here, the average crater size increased with higher implantation energy. This could also be related to the implantation depth. For small implantation energies, the phosphorus ions do not reach the bottom of the a-Si layer during the anneal. Therefore, for the silicon atoms in the a-Si that are close to the crystalline silicon surface, there are no phosphorus atoms to facilitate diffusion which leads to smaller grains in the resulting polycrystalline silicon. At higher implantation energies, these phosphorus atoms are more likely to be present, which could increase the grain size of the polycrystalline silicon close to the surface of the crystalline silicon. The argon energy series was performed for 5, 25, 50, 100 and 200 keV implantation energy using 1 µm layers of a-Si. The results showed that the higher energies of 50, 100 and 200 keV resulted in larger craters than the smaller energies. Of these higher energies, the 50 keV implantation resulted in the largest craters, with an average of 264 nm. Unexpectedly, even though the mean pore diameter decreased slightly for energies beyond 50 keV, the average roughness increased, which is an indication for lower optical reflectance.

The effect of the implantation dose was tested using an a-Si layer of 1 µm with four different phosphorus implantation doses: 0, $1 \cdot 10^{15}$, $5 \cdot 10^{15}$ and $1 \cdot 10^{16}$ ions/cm^2. The results showed that the crater size increases with the implanted phosphorus dose to a maximum average diameter of 277 nm at the highest dose.

For the anneal temperature and time tests, two relatively high temperature anneals of 950 °C and 1050 °C were used for two anneal times of 5 and 60 minutes. It was found that the 950 °C samples resulted in the largest craters. At this temperature, the longer anneal time showed a larger mean pore diameter but since the error of the two measurements incorporated the value of the other measurement, this conclusion could not be drawn with full certainty. The small craters at high temperature could be caused by almost full crystallization of the a-Si layer, which prohibits the creation of craters in the crystalline silicon. It is also important to note that the craters produced during this test were much larger compared to the craters that originated from the other tests: average crater diameter of 431 ±40 compared to 277 ±8 nm. The cause of this difference will be thoroughly discussed in the recommendations section.

Four different ions were used for implantation to investigate the effect of the different ions on the size of the produced craters: Boron (B), Argon (Ar), Arsenic (As), and Boron Difluoride (BF_2). Phosphorus was not used in this test since this ion was already investigated during the other tests. Two different thicknesses of a-Si were applied, 1 µm and 2 µm. For boron, implantation energies of 5 and 50 keV were used. No craters were produced when boron implantation was used. For the other ions, three energies were used: 100, 200 and 250 keV. Of these ions, argon resulted in the largest craters for the highest energy. The average crater diameter was 313 nm for the 1 µm a-Si sample and 320 nm for the 2 µm a-Si sample.

The nano-crystalline silicon crack test was performed on wafers with a sacrificial layer tex-

ture that was created using 1 µm of a-Si and 250 keV argon implantation. The results did not show obvious cracks created by the surface.

The fourth subgoal was to compare the resulting textures in terms of optical performance. This was done in terms of total reflectance and the angular distribution of the reflectance, which indicates light scattering. The reflectance of the photolithography samples showed that the mask with the period of 3 micron resulted in lower reflectance than the mask with a period of 2 micron. This is caused by the fact that both masks have the same hole diameter, which results in larger semi-spherical walls for the larger period since the etch distance is larger. This promotes light incoupling. It was also found that over-etching causes the reflectance to increase. For the sacrificial layer method it was found that the creation of craters causes a decrease in the reflectance over the entire wavelength. The comparison of the reflectance for the different methods showed that the mean reflectance was lowest for the photolithography samples, at 37.7%. The mean reflectance for the largest craters originated from the sacrificial layer method (mean diameter of 431 nm) was 0.5% lower at 38.2%. The mean reflectance of the smaller craters from argon implantation (mean diameter of 320 nm) was 41.5 %.
The angular distribution of reflectance measurements indicated that both the photolithography and the large craters from the sacrificial layer texture are suitable for light scattering. The photolithography samples showed a large angular dependence of the reflectance, which also changed for different wavelengths. The sacrificial layer large craters show light scattering into wider angles compared to a flat surface. This light scattering is at approximately the same level as the photolithography samples, but more gradual over different angles. The smaller craters from argon implantation show the same gradual scattering of light as the large craters, but at a lower level.

The fifth and final subgoal was to use these new texturing methods in the production of Silicon Hetero Junction (SHJ) solar cells and to compare the performances of these solar cells. For these SHJ's, the hexagonal texture with a period of 3 µm was used and argon implantation at 250 keV was used for the sacrificial layer texture. Unfortunately, the minority charge carrier lifetime measurements showed that the lifetimes of the cells were very low. This is most likely caused by a low deposition rate of a-Si on the textures, which results in bad passivation of the dangling bonds at the surface.
The IV-curve measurements showed that the performance of cells using both textures was lower than anticipated. The hexagonal texture SHJ resulted in an efficiency of 10.0%, while the sacrificial layer texture only converted 0.1 %. This can again be allocated to a bad passivation of dangling bonds resulting from a low deposition rate of a-Si.
Optically, the hexagonal texture resulted in a lower average reflectance in the SHJ's of 13.4%, compared to 14.4% for the sacrificial layer texture.

The goal of this research was to develop two new types of crystalline silicon texturization, eventually aimed to be used in a triple junction solar cell from monocrystalline silicon and two thin film silicon alloy layers. This was achieved for both the hexagonal texture method using photolithography and for the sacrificial layer texture. The photolithography method resulted in a texture that could grow a crack-free layer of nanocrystalline silicon while maintaining good light scattering characteristics. For the sacrificial layer method, the optimal crater size of around 3-3.5 µm was not reached. However, insight was gained on the effect of the different parameters on the resulting texture and it did prove to grow a crack-free nanocrystalline silicon layer. Also, the optical characteristics of this texture show great promise.

5.2. Recommendations

The research conducted during this thesis proved to have great promise for implementation in multi-junction solar cells that use crystalline silicon. Unfortunately, due to a limited amount of time, a number of interesting research options were not examined. This section is therefore allocated to these interesting options.

Firstly, during section 3.1.3, the mask design was discussed. It was mentioned that an aspect ratio of 0.25 is desired in hexagonal textured back reflectors.[33] In other words, the height difference in the hexagonal texture should be a quarter of the texture period. The height of the final texture is dependent on the horizontal and vertical etch rate of the used poly-silicon etch, as well as the hole diameter of the mask. During the mask design process, it was decided to use a small hole diameter. This was done to make sure that it was possible to reach the desired aspect ratio since the difference between the horizontal and vertical etch rate was not known. If, for example, the horizontal etch rate is larger than the vertical etch rate, the texture becomes too shallow. This can be avoided by using a smaller hole diameter. If the hexagonal texture turns out to be too steep, this can be resolved by over-etching of the texture, which flattens it. However, the aspect ratio of the created hexagonal texture was not measured since this texture proved to be too steep to accurately image using AFM. Other measurement techniques could be used to measure this aspect ratio which can be used to find the (over-)etching time that creates this optimal aspect ratio. It would also be interesting to check if this aspect ratio is indeed optimal for this purpose, since the study by Manea et al. [33] involved textured back reflectors.

Secondly, during the anneal temperature and time series for the sacrificial layer texturing method, large craters were originated from using phosphorus implantation at 5 kev in a 1 µm layer of a-Si in combination with a 60 minute anneal at 950 °C. These craters had an average diameter of around 430 nm. Unfortunately, these results could not be reproduced. Therefore, it would be interesting to do a more extensive anneal temperature and time research. A mistake could have been made during these tests, which resulted in a faulty conclusion with respect to the optimal anneal time and temperature.

Thirdly, the production of the SHJ's did not go as smoothly as was anticipated. This resulted in a deposition time for the different layers that was presumably too short, which expressed itself in short minority charge carrier lifetimes. This induced problems for the PV performance of these cells. Therefore, the layer thicknesses of these cells should be further optimized before a definitive conclusion can be made about which texture is best for these cells.

Finally, it would be very interesting to see the performance of these textures in the proposed triple junction solar cell and to compare these textures to other crystalline silicon textures that were investigated in research by T. de Vrijer. These textures include smaller pyramids created using the standard texturing method and periods that were made smooth using an isotropic etch.

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Appendix A: AFM Measured Characteristics

The AFM can be used to measure different characteristics of textured surfaces. These characteristics include but are not limited to: average crater size, surface roughness, kurtosis, maximum peak height, mean slope, skewness, maximum valley depth, maximum height difference, and density of summits. It was mentioned in section 4.2 that only the average crater size and surface roughness were shown in this research since other parameters show the same trends. An example for this is given in table A.1, where the argon implantation energy is varied. The a-Si layer thickness, implantation dose, anneal temperature and anneal time were kept constant at respectively 1 µm, 10^{16} ions/cm^2, 950 °C and 60 minutes. The maximum height difference and the mean slope show approximately the same trend as the roughness. For larger energies, the craters are created which causes the average roughness to increase. The same effect is demonstrated in the maximum height difference and the mean slope. The creation of the craters causes a larger average height difference and also a larger mean slope.

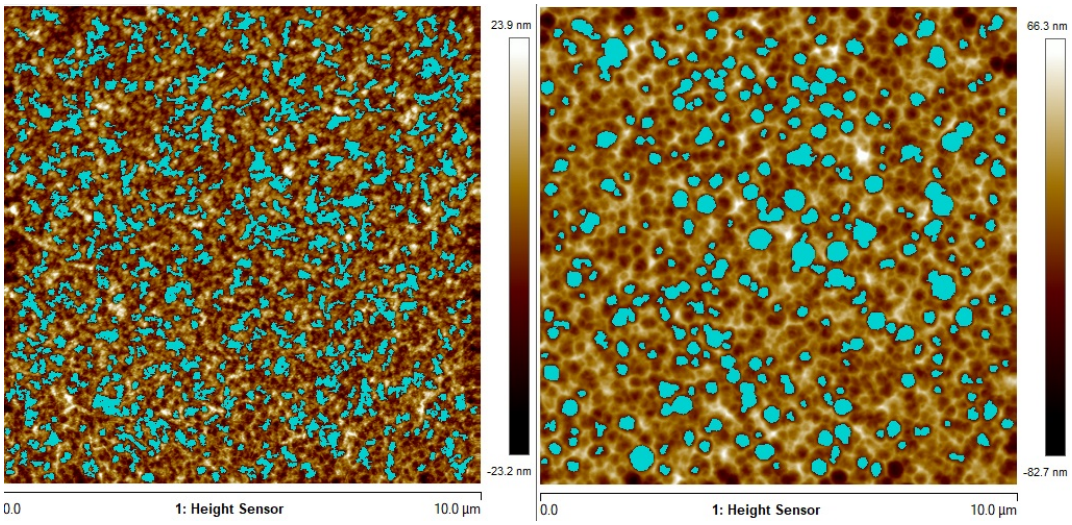
Implantation	Mean pore diameter (nm)	Roughness (nm)	Max height difference(nm)	mean slope (°)
Ar 5 keV	203.5 ± 4.4	5.6	57.5	9.6
Ar 25 keV	203.5 ± 4.8	5.6	61.0	11.4
Ar 50 keV	264.0 ± 8.0	8.6	117	15.2
Ar 100 keV	257.0 ± 7.6	10.1	112	16.5
Ar 200 keV	248.9 ± 6.2	12.9	124	18.3

Table A.1: AFM analysis of argon implantation energy series.

B

Appendix B: AFM Overestimating Crater Size

As mentioned in section 4.2.1, the mean crater diameter is overestimated for samples that have no or very small craters (smaller than 200 nm average diameter). The origin of this overestimation is that for small craters, the software links multiple of the small textures together during the mean pore size analysis. An example of this problem is shown in figure B.1. The image on the left gives an average crater size of 193 nm, compared to a crater size of 277 nm on the right. The crater size of 193 nm for the left image is most likely an overestimation.



(a) No craters (b) Craters

Figure B.1: AFM analysis images of a sample without craters compared to a sample with craters.

C

Appendix C: Deposition times of SHJ layers

The deposition time of the layers in the SHJ was varied since the deposition rate of these layers is dependent on the monocrystalline silicon texture. The deposition times in seconds for each layer is shown in table C.1.

Wafer number	1	2	3	4	5
n-a-Si	102	91	81	70	60
i-a-Si:H	56	50	44	38	33
n-type wafer					
i-a-Si:H	101	91	80	70	60
H_2 Plasma treatment	120	108	95	83	71
nc-Si Seed	120	108	95	83	71
p-SiO_x:H	228	205	181	158	134

Table C.1: Deposition times for the production of the SHJ solar cells. All values are in seconds.