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A 15nW per Sensor Interference-Immune Readout IC for Capacitive Touch Sensors

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Abstract— This paper presents a readout IC that uses an asynchronous capacitance-to-digital-converter (CDC) to digitize the capacitance of a touch sensor. A power-efficient tracking algorithm ensures that the CDC consumes negligible power consumption in the absence of touch events. To facilitate its use in wake-on-touch applications, the CDC can be periodically triggered by a co-integrated ultra-low power relaxation oscillator. At a 38 Hz scan-rate, the readout IC consumes 15 nW per touch sensor, which is the lowest reported to date.

Keywords—Stand-alone touch sensor; Self-capacitance sensor; Asynchronous tracking logic; CDC; Ultra-low power oscillator.

I. INTRODUCTION

In battery-powered devices such as smart meters, wearables and mobile devices, sleep modes are often used to extend battery life [1-3]. In such modes, most of the device's electronic systems will be disabled, with the exception of a watchdog circuit that wakes up the full system when necessary [1-3]. Since its power dissipation will then define an upper limit on battery life, a typical watchdog circuit will consist of an event-detecting sensor, together with an ultra-low-power timer and readout circuit.

Due to their low cost, low power and robustness, capacitive touch sensors are often used to realize user interface functions such as buttons, sliders, and wheels [4]. Since capacitive sensors do not consume static power, the power consumption of a capacitive sensing system will be limited by that of the readout circuitry, typically a capacitance-to-digital-converter (CDC), [5-19]. For use in watchdog circuits, ultra-low-power readout circuits are required, which must also be robust to external interference in order to limit the occurrence of power-wasting detection errors [5].

Energy-efficient CDCs based on sigma-delta modulation [6-12], period modulation [13], and slope integration [14,15] have been reported. Although they can achieve high resolution, this is not required in watchdog circuits, and their power consumption is also too high. Much lower power with moderate resolution can be achieved by CDCs based on the successive approximation algorithm (SAR) [16-19]. State-of-the art designs only require a few nW to perform an 8-bit conversion [16-18]. However, touch sensors typically have a large baseline capacitance compared to the capacitance changes induced by touch events. A conventional CDC will then use most of its dynamic range, and thus most of its power consumption, to digitize this baseline capacitance. To address a similar problem, an LSB-first SAR algorithm was proposed in [20], whose activity, and hence power dissipation, is dependent on the

change in its analog input between successive readout cycles. When signal activity is low, only 3.7 μ W was required to perform a 10b conversion. However, compared to the conventional SAR algorithm, the required logic is significantly more complex.

This paper presents a stand-alone readout IC [21] that consists of an asynchronous tracking CDC, whose power consumption depends on touch activity, and which is periodically triggered by a nano-power timer. The CDC employs a differential architecture, which confers considerable robustness to common mode interference and human finger noise, i.e. external interference coupled into the sensor by a touch event. At a 38 Hz scan-rate, the readout IC consumes only 15 nW per sensor pad, which is about 46 \times better than the state of the art [2].

In the following, Section II describes the operating principle of the proposed readout IC. Section III and Section IV discuss its circuit implementation, detailed design, measurement results, and comparison with the state of the art. Finally, conclusions are drawn.

II. OPERATING PRINCIPLE

A. Touch Sensing System

As described in [4], capacitive touch sensors can be divided into two types: a) mutual capacitance sensors and b) self-capacitance sensors. A mutual capacitance sensor typically consists of an array of conductive rows and columns separated by a dielectric. A dielectric overlay provides mechanical protection. When touched, part of the array's projected electric field will be diverted to ground, which, in turn, decreases the mutual capacitance between the nearest row and column intersection. In self-capacitance sensors, the capacitance between individual electrodes and ground is detected (Fig. 1). In this case, a touch event will increase the sensor's capacitance to ground. The readout IC senses the total capacitive load of a finger on a row or column, which is typically much larger than their mutual capacitance. In addition, self-capacitance sensors typically cost less than mutual-capacitance sensors, mainly because they can be fabricated from a single metal layer, and only one connection per sensor is required. As a result, self-capacitance sensors are often the preferred choice due to their lower cost, higher touch signal, and thus simpler read-out circuitry.

A block diagram of the proposed touch sensing system is shown in Fig. 1. It consists of a readout IC and a PCB-based

touch sensor. The latter consists of a conductive pad that is shielded electrically by a surrounding ground plane, and mechanically by a dielectric overlay (typically glass, or plastic). When touched, the capacitance of the sensor pad to ground will increase slightly. It can be modeled as a relatively large fixed (or baseline) capacitance (C_p), together with a small variable capacitance (C_{touch}) that represents the touch signal.

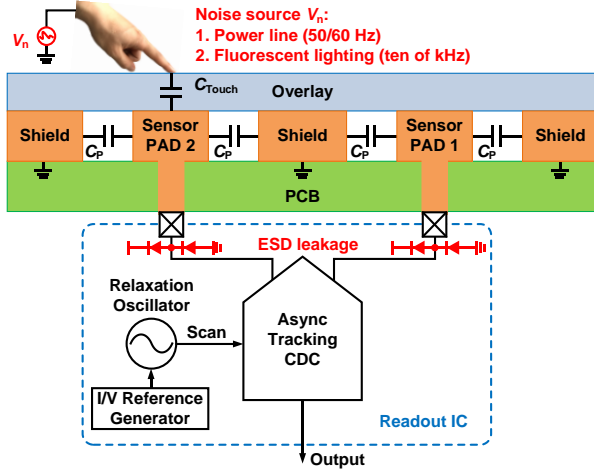


Fig. 1. Schematic diagram of the stand-alone touch readout IC connected to two sensor pads on a PCB.

The readout IC consists of a CDC and an ultra-low-power relaxation oscillator that periodically triggers the CDC. Since the sensor pad is exposed to the environment, it will pick up external interference from the mains and from fluorescent lighting, which may contaminate the touch signal. To minimize detection errors, the readout IC should be designed to be robust to such interference.

B. Tracking Algorithm

As shown in Fig. 2a, where the sensor is readout by a conventional SAR CDC, the full SAR algorithm will be executed during every conversion cycle; even when the sensor's capacitance has not changed e.g. during cycles #2 and #4 [16-19]. The corresponding SAR cycles are thus unnecessary and waste energy.

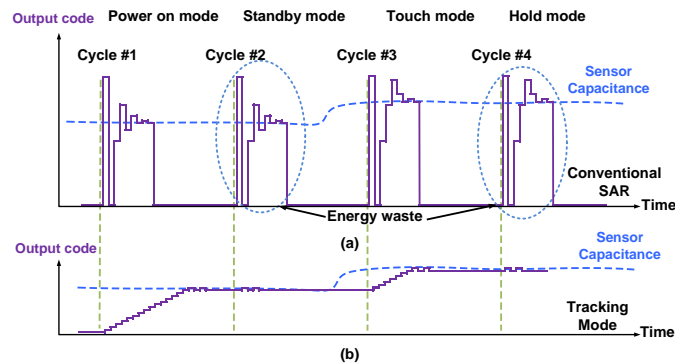


Fig. 2. SAR algorithm (a) and tracking algorithm (b).

A more efficient algorithm is shown in Fig. 2b, in which the CDC uses the stored digital output of the previous conversion

cycle as a starting point and only updates its digital output if the capacitance changes. In effect, the CDC just tracks changes in sensor capacitance. Conversion time refers to the time interval between the beginning and end of a conversion. Like the LSB-first algorithm, the result is higher energy efficiency compared with conventional SAR CDCs [20]. Moreover, the proposed tracking technique can be simply implemented with power-efficient asynchronous control logic.

C. Interference immunity

The proposed tracking CDC is designed to operate in a differential manner, by digitizing the difference in capacitance between two neighboring touch sensing pads. Environmental interference that couples to both inputs of the CDC will then appear as a common mode voltage, and be rejected. Due to the mismatch between the two sense-pad capacitances, a small fraction of this interference will still appear as a differential voltage, but in practice this residual interference is quite negligible. In applications where it is not feasible to sense neighboring pads, a dummy pad can be realized to facilitate pseudo-differential operation.

Another source of error is human finger noise, which is caused by capacitively-coupled interference from the mains (50/60 Hz) and fluorescent lighting (tens of kHz) pick-up [5]. This interference appears only at the touched pad, and so will not be rejected by the CDC's differential architecture. As will be explained next, however, the effect of such interference is mitigated by the fact that the CDC is only sensitive to changes in V_n that occur over a short period of time.

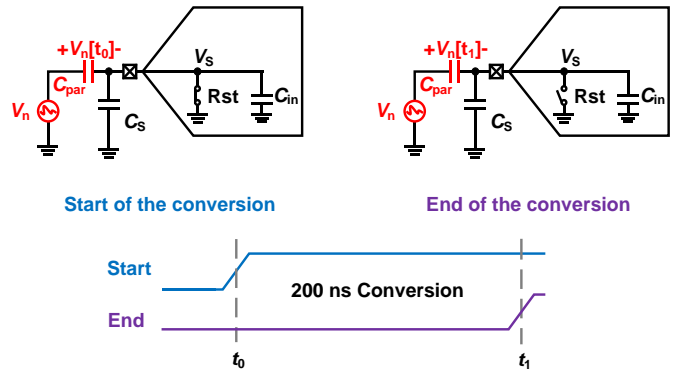


Fig. 3. Input CDS function of the CDC.

As shown in Fig. 3, human finger noise can be modeled as an interference source V_n that is coupled to the touched pad by a parasitic capacitance C_{par} . During the reset phase, while V_s is grounded, C_{par} is charged to V_n and stored at time t_0 . Thus, V_s sees only the change in V_n during conversion time. At the end of the conversion, t_1 , V_s is given by

$$V_s[t_1] = (V_n[t_1] - V_n[t_0]) \cdot \alpha, \quad (1)$$

where α is the ratio of C_{par} to the total capacitance present on the pad, which is due to the sensor, the C-DAC and any parasitic capacitances. Equation (1) corresponds to a correlated-double sampling (CDS) transfer function, which suppresses interference at low-frequencies ($< 1/T_{conv}$). Thanks to the short conversion time of the CDC (~ 200 ns for touch events), human

finger noise will be significantly reduced. Moreover, the residual interference will be further attenuated by a factor of α .

III. CIRCUIT IMPLEMENTATION

A. Asynchronous Tracking CDC

Fig. 4 shows the schematic and timing diagram of the proposed asynchronous tracking CDC. It consists of a differential capacitive DAC (CDAC), an asynchronous logic unit, a coarse fine binary counter, and a dynamic comparator. The CDC digitizes the difference in capacitance ΔC between two external capacitors C_{s1} and C_{s2} . At the start of each conversion, their voltages, V_{s1} and V_{s2} , respectively, are first reset to zero and then pulled up towards V_{dd} by fixed base-line-compensating capacitors C_z ($= 9.2$ pF). This is necessary because the lower limit of the comparator's common-mode input range is defined by the threshold voltage of an NMOS device. The pull-up function implemented by the capacitors C_z ensures that $V_{s1,2}$ are always within the comparator's common-mode range even with large sensor capacitances (up to 50 pF). The asynchronous logic unit and the binary counter then force $V_{s1} = V_{s2}$ by ramping the two CDACs up and down, respectively, starting from their mid-code. The final counter code Data is then proportional to ΔC . During the next conversion, the counter is loaded with the previous code and is either incremented or decremented to force $V_{s1} = V_{s2}$ again. The CDC's activity is thus proportional to the change in ΔC between read-out cycles.

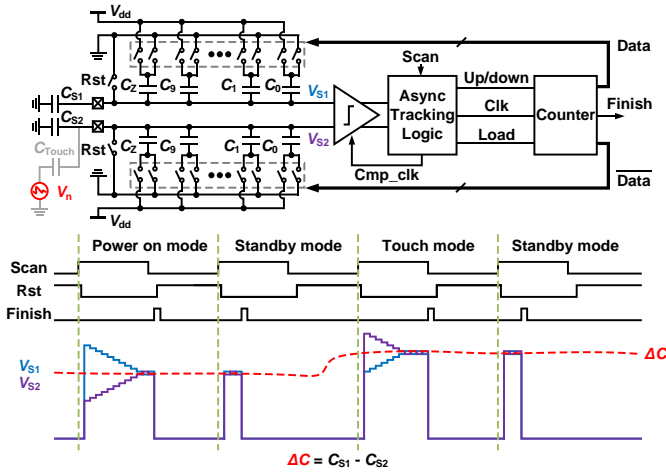


Fig. 4. Asynchronous Tracking CDC and simplified timing diagram.

An analysis of the power consumption of CDACs used in data converters concludes that for minimum power consumption, a CDAC should be implemented with unary weighted capacitors and uses a thermometer code to ramp its output voltage up/down towards the value of the input voltage [22]. However, a unary implementation will require a large number of switches and logic gates. Although the logic can be implemented with dynamic circuitry, its leakage current will be a dominant source of power consumption, especially at the low scan-rates required for touch sensing. For this reason, a binary-weighted CDAC will be used in this design.

As discussed before, significant energy will be wasted if the full SAR algorithm is always executed, especially during the

mid-code transitions of a binary CDAC. But even with the proposed tracking algorithm, small changes in sensor capacitance may still cause mid-code transitions, leading to increased power consumption. To reduce this, the CDAC is implemented as a combination of a 4-bit coarse CDAC and a 6-bit fine CDAC whose range is equivalent to two coarse LSBs. Each time the coarse CDAC toggles, the fine CDAC is reset to its mid-code thus ensuring that the coarse CDAC only toggles when ΔC changes by more than one coarse LSB. For such fine-only conversions, this technique reduces the maximum CDAC switching losses by $\sim 16\times$.

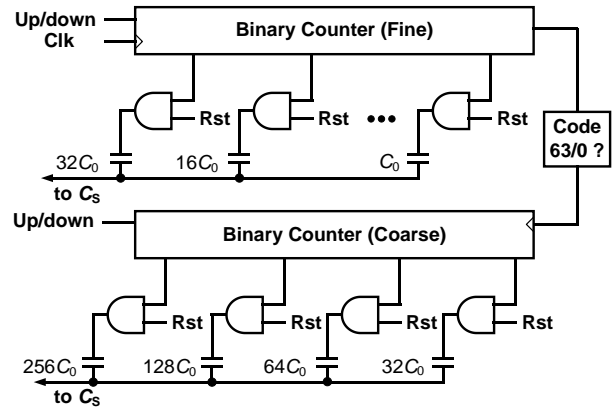


Fig. 5. Coarse fine binary counter.

The two CDACs are driven by 6b and 4b binary counters, respectively. To save power, the fine counter is reset to its mid-code every time the coarse counter toggles. As shown in Fig. 5, this is implemented by setting the fine counter's MSB bit to 1 and its other bits to 0, whenever the coarse counter transitions to the states 63 or 0. As discussed before, the range of the fine CDAC is equal to two LSBs of the coarse CDAC, so the output of the CDC can be decoded simply by adding the state of the fine counter to half the state of the coarse counter.

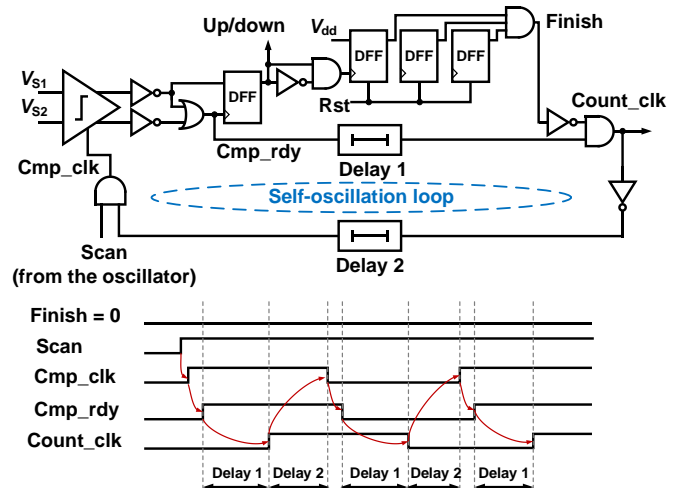


Fig. 6. Asynchronous logic unit.

The CDC employs asynchronous logic based on a self-oscillating loop formed by the delay (~ 30 ns) between the

comparator's clock signal and its ready signal. As shown in Fig. 6, the self-oscillation loop starts and, while the *Finish* signal is low, provides a clock signal for the comparator and the counter. To minimize false decisions, the *Finish* signal stops the conversion only after the comparator's output changes sign 3 times. Two delay blocks, *Delay 1* and *Delay 2*, implemented as inverter chains, are inserted into the oscillation loop to prevent errors due to incomplete settling. *Delay 1* is designed to provide a delay of ~ 3 ns, as required for the logic that generates the *Finish* signal. *Delay 2*, on the other hand, provides the ~ 12 ns delay required to ensure CDAC settling.

In order to make the CDC's operation fully dynamic, a low-noise single-phase comparator has been implemented. The schematics and timing of the comparator are shown in Fig. 7 [23]. When the clock signal is low, *Di* nodes are pre-charged to V_{dd} , while *Xi* nodes and outputs of the comparator are reset to ground. After the rising edge of clock, *Di* node voltages drop at a rate that depends on the input voltages. At $t = t_0$, *Gm1* amplifies the differential inputs. The outputs of *Gm1* (*Di+* and *Di-*), are connected to *Gm2* pair and amplified even further. The *Gm2* outputs (*Xi* nodes) will then drive the core latch. Thus, the differential input will be amplified by two gain stages before it drives the core latch, which reduces the total input referred noise and offset of the core latch.

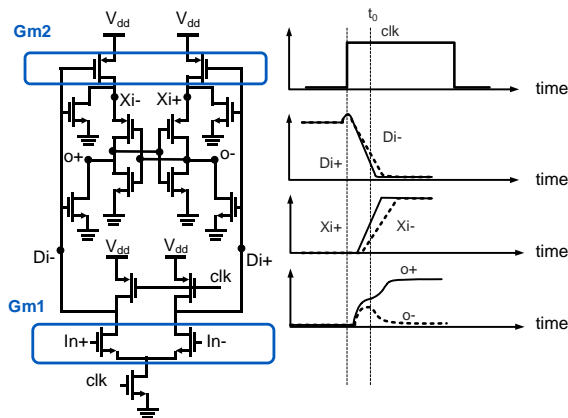


Fig. 7. Dynamic comparator.

The comparator is designed to ensure that the CDC is quantization-noise limited. This reduces spurious activity due to thermal noise, and thus reduces the CDC's average power consumption. The CDAC elements were sized for matching, and as such their thermal noise contribution is negligible. According to simulations, the total input-referred noise of the comparator is about $200 \mu\text{Vrms}$, which is $\sim 6\times$ smaller than the input signal swing (~ 1.2 mV) corresponding to a one LSB step. Its simulated offset is less than 12 mV, which results in a 10 LSB offset error at the output of the CDC. Being a static error, however, this does not generate false touch events. Over temperature, the worst-case variation of the offset was simulated to be only 1 mV, i.e. less than an LSB.

Since the CDC is designed for low power rather than speed, input leakage currents, e.g. due to ESD devices, may discharge the CDAC leading to decision errors. However, simulations show that the CDC's conversion time T_{conv} (~ 90 ns to $\sim 1 \mu\text{s}$ for fine-only conversions) is short enough to prevent such errors.

B. Oscillator

In order to trigger the capacitance to digital converter, a timer is required to provide the clock signal. For wake-up timer applications, the frequency stability specifications are very relaxed. However, if the frequency is too high, it will unnecessarily increase the scan-rate of the CDC and thus its dynamic power consumption, while if it is too low touch events may be missed. A frequency stability of 5% over temperature (25°C to 85°C), which results in an acceptable 5% variation in power consumption, is a proper choice.

The schematic of the proposed relaxation oscillator is shown in Fig. 8. A current source (I_{ref}) charges an integration capacitor (C_{int}), causing a voltage ramp-up rate of $I_{\text{ref}}/C_{\text{int}}$ on C_{int} . A continuous-time comparator periodically resets the integration capacitor when its voltage V_{int} exceeds V_{ref} . The oscillator's schematic and the corresponding waveforms are shown in Fig. 9.

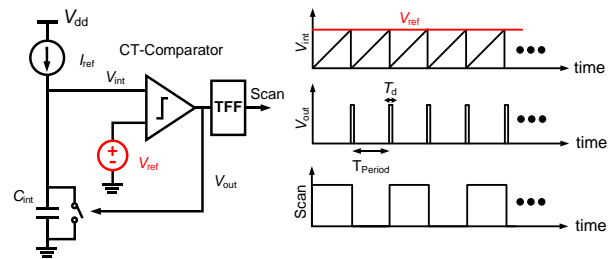


Fig. 8. Low-power oscillator and its timing diagram.

The period of the relaxation oscillator (T_{Period}) can be expressed as

$$T_{\text{period}} \approx \frac{V_{\text{ref}}}{I_{\text{ref}}} C_{\text{int}}, \quad T_{\text{period}} \gg T_d, \quad (2)$$

where T_d is the comparator delay. Its output V_{Out} is a short pulse with a low duty cycle T_d/T_{period} , which may be too short to reliably trigger the CDC. To increase the duty cycle, the output of the comparator is used to drive a T flip-flop (TFF). The resulting scan clock will then have a robust 50% duty cycle.

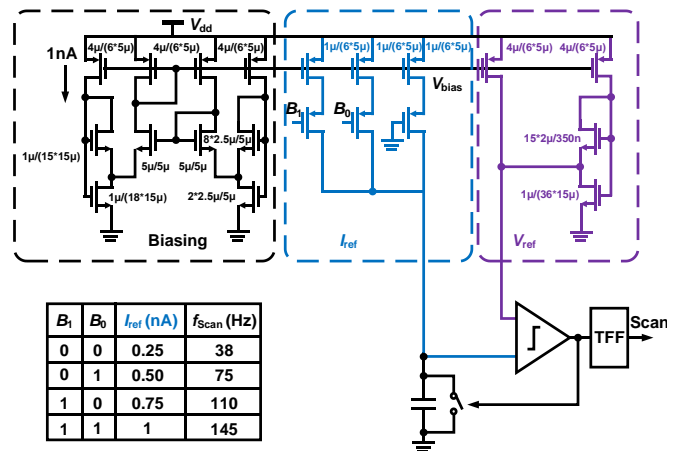


Fig. 9. The schematic of the references generation circuits for the oscillator.

For stand-alone operation, references (V_{ref} and I_{ref}) should be implemented on-chip. However, on-chip current and voltage references are often quite temperature dependent when biased at nano-Ampere levels. According to (2), the oscillator's output frequency is determined by the ratio between I_{ref} and V_{ref} . If these two references have similar temperature dependencies, then the oscillation frequency will be temperature independent. This suggests a low-complexity ratio-metric method of building the circuit references.

In this design, both the charging current and the threshold voltage are derived from a constant inversion current source shown in Fig. 9. The biasing block is similar to a constant Gm circuit, with the usual resistor being replaced by self-cascoded nMOS transistors [24]. To compensate for process spread, the biasing circuit can be trimmed by adjusting the charging current with the help of a 2-bit current DAC controlled by B1 and B0. Monte-Carlo simulation shows that the spread in the oscillator's output frequency due to process variation and mismatch is only about 10 Hz (1σ).

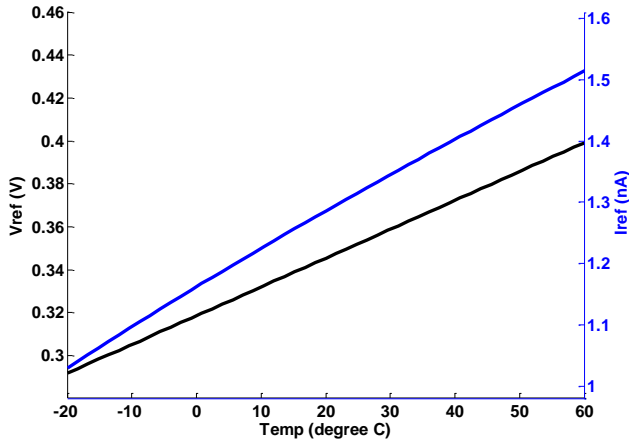


Fig. 10. Simulated temperature dependencies of the voltage and current reference generators.

Fig. 10 shows the results of simulating the behavior of the reference generators over temperature. The temperature coefficients of the voltage reference and current reference are $1.35\text{mV}/^\circ\text{C}$ and $6\text{pA}/^\circ\text{C}$, respectively. The resulting oscillation frequency then has a temperature stability of $\pm 2\%$ from 25°C to 85°C . To achieve a low operating current and low leakage, all transistors in the reference circuit are implemented with high-threshold devices.

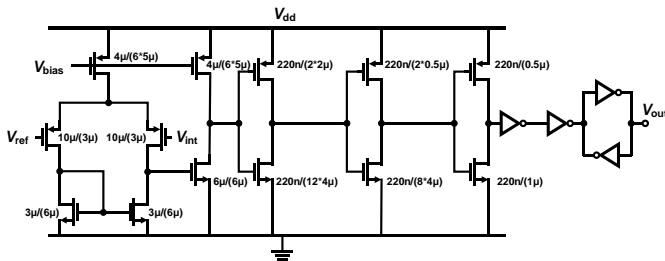


Fig. 11. Continuous time comparator.

The proposed relaxation oscillator uses a low-power continuous-time comparator to periodically reset the integration capacitor when its voltage exceeds a certain threshold. As shown in Fig. 11, this consists of a preamp followed by a chain of inverters. The preamp consists of a two-stage operational amplifier that is biased by the current reference circuit, consuming 2 nA of static current. PMOS transistors are used as the input pair to allow the comparator work under a low input common mode voltage (Fig. 11). The amplifier then is followed by an inverter chain to provide enough comparator delay T_d . The first three inverters are sized to have low short-circuit currents when driven by signals with long rise/fall time. A regenerative back-to-back inverter latch at the end of the chain provides a reset signal with steep edges. Simulation shows the supply sensitivity of the oscillator is only 3.7 Hz/V .

IV. MEASUREMENT RESULTS AND COMPARISON

The readout IC is implemented in a standard TSMC $0.18\ \mu\text{m}$ CMOS process, and occupies an active area of $0.1\ \text{mm}^2$ (Fig. 12). The CDC and Oscillator occupy 80% and 20% of the total area, respectively. For good matching, the unit capacitors of the 6-bit fine CDAC are realized with fringe capacitors ($\sim 11\text{fF/LSB}$), while the 4-bit coarse CDAC is realized with MIM capacitors ($\sim 320\ \text{fF/LSB}$), to save area. The CDC has a $\pm 10.8\ \text{pF}$ differential input range when connected to $9.2\ \text{pF}$ baseline capacitors.

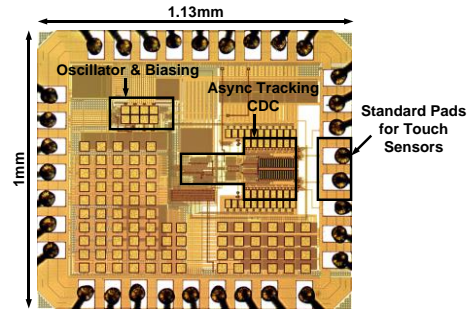


Fig. 12. Die micrograph of the readout IC.

The measurement setup for characterizing the proposed readout IC is shown in Fig. 13. A Keithley 2400 source-meter is used as the supply voltage and also for current measurements. The FPGA is only used to program the IC's trim registers, and to define the various scan rates used to evaluate CDC performance. Measurements with the CDC connected to the touch sensor were made with the help of the on-chip clock. A climate chamber was used to characterize the frequency variation of the oscillator and the power consumption of the readout IC over temperature. The PCB touch panel is fabricated in an FR4 2-layer PCB technology, with a sensor diameter of 10 mm and 0.7 mm spacing to the ground plane (Fig. 13). The sensors are connected to the readout IC using standard pads.

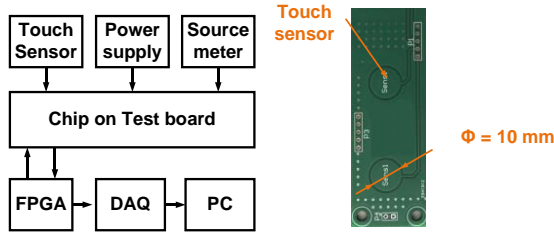
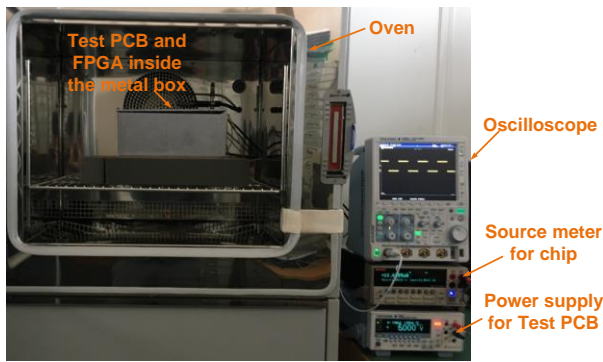


Fig. 13. Measurement setup.

Fig. 14 shows the readout IC's response to an actual touch when sampled at a 38 Hz scan-rate. For this measurement, the two buttons have baseline capacitances of ~ 9 pF and ~ 11 pF, respectively, where the 2 pF difference in capacitance is due to PCB parasitics (one button is closer to the chip than the other). The typical range of button capacitance is from about 5 pF to 15 pF. Together, the CDC and the relaxation oscillator then consume 30 nW (CDC: 13.8 nW; Oscillator: 16.2 nW) from a 1.35 V supply.

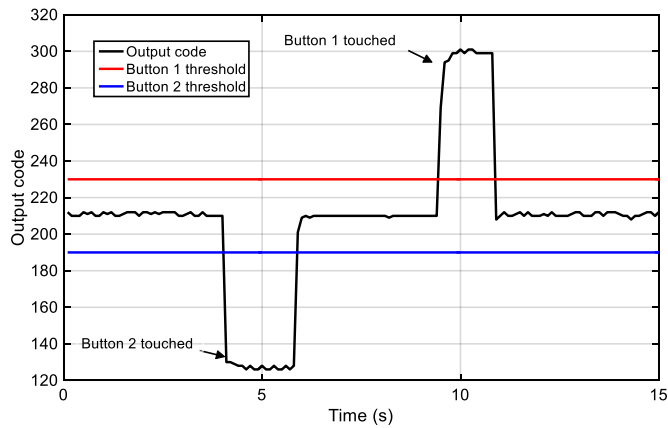


Fig. 14. Transient response of the read-out IC.

Fig. 15 shows the CDC's measured current consumption at different scan rates when the sensor's capacitance changes by a given amount ΔC per readout cycle. This is emulated by using an external voltage source to drive its ground node, thus preloading it with a well-defined differential charge. As shown in Fig. 15, the CDC's current consumption is roughly proportional to the amount of ΔC per readout cycle. This is measured when the CDC is supplied at 1V.

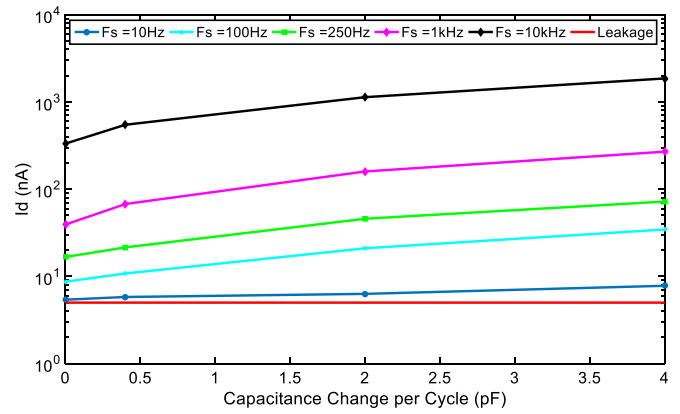


Fig. 15. Measured current consumption of the proposed tracking CDC.

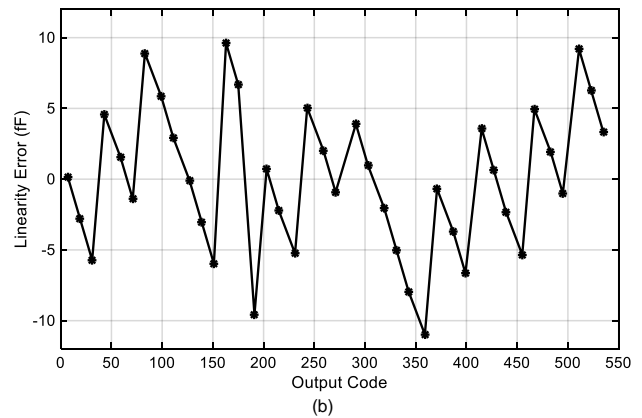
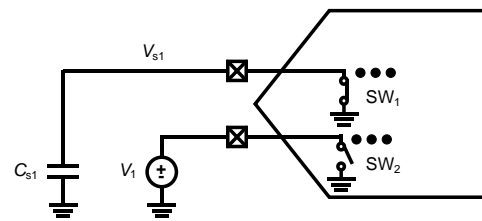


Fig. 16. The CDC's linearity measurement test bench (a) and the results (b).

The test bench used to measure sensor linearity is shown in Fig. 16a. The CDC is configured to operate in single input mode, i.e. while one input is connected to an external capacitor, the other input is biased with an external reference voltage (V_1). In order to avoid short circuits, the on-chip switch, SW_2 , is programmed to be always open. During each conversion, the tracking algorithm adjusts the CDAC such that $V_{s1} = V_1$. Therefore, sweeping V_1 can emulate capacitance changes. Since only one CDAC is active in this mode, each LSB corresponds to a $2\times$ unit capacitance change. As the CDC employs a coarse-fine charge redistribution scheme, calibration is required to find the conversion step and the ratio of the coarse and fine capacitor banks. Fig. 16b shows the nonlinearity of the proposed CDC, which is less than 0.1% over the full (10.8 pF) range.

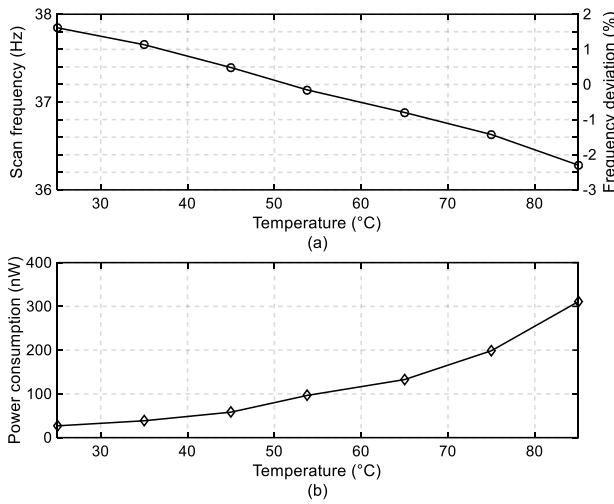


Fig. 17. Temperature sensitivity of the proposed readout IC, a) frequency deviation, b) power consumption over temperature.

The proposed oscillator achieves a temperature sensitivity of 0.7%/°C as shown in Fig. 17a. Moreover, the power consumption of the read-out IC versus temperature is shown in Fig. 17b. At low temperature the power consumption is mostly dominated by the dynamic power consumption of the system. At higher temperatures, however, the leakage current of the chip increases exponentially, dominating the total power consumption.

Table I. Comparison with state-of-the-art CDCs

	This work				[13]	[14]	[16]	[17]	[18]	[15]	[19]
Technique	Asynchronous Tracking				PM	ID ¹	SAR	SAR	SAR	DS	SAR+VCO
Support Self-capacitance	Yes				No	Yes	No	No	No	Yes	No
Differential	Yes				No	No	No	Yes	Yes	No	No
Technology (nm)	0.18				160	40	180	180	180	180	40
F_s (kHz)	10 ²				4.8	52.6	0.25	62.5	200	156.25	1000
Cap-range (pF)	±10.8 ²				8	11.3	75.3	12.66	6	30.7	5
Resolution (fF _{rms})	11.46 ²				1.4	12.3	6	1.1	5.2	8.7	1.1
Cap-change (LSB/Cycle)	0	10	50	100	--	--	--	--	--	--	--
Power (μW)	0.33 ³	0.55 ³	1.14 ³	1.86 ³	14	1.84	0.16	7.25	9.4	0.11	75
FoM ⁵ (fJ/c-s)	61	100	208	342	1870	141	181	35 ⁴	45	5300	55

1. Iterative delay-chain discharge.
2. Measured at a scan rate, F_s , of 10 kHz and a baseline capacitance of 9.2pF.
3. Excluding the on-chip oscillator.
4. Excluding the high frequency clock generator used for power gating amplifier, and SAR logic.
5. FoM = Power/($F_s \cdot 2^{\text{ENOB}}$), ENOB = $(20 \log((\text{Cap-range}/2\sqrt{2})/(\text{LSB}/\sqrt{12}) - 1.76)) / 6.02$

Table II. Comparison with state-of-the-art stand-alone touch sensors

Product	Year	Scan-rate	Power/Button (uW)
MSP430FR2633 [1]	2015	8 Hz	0.690
EFM32 [2]	2016	10 Hz	1.561
PSOC4 [3]	2016	8 Hz	3.961
This work	2017	38 Hz	0.015

The CDC's immunity to interference was characterized by coupling a voltage source to one of its inputs via a 1 pF capacitor and measuring the resulting rms error (2^{15} samples).

Fig. 18 shows that low frequency interference, e.g. 50/60 Hz, is indeed strongly attenuated. At higher frequencies, this attenuation becomes amplitude-dependent, since large signals increase T_{conv} , and thus reduce the cut-off frequency of the CDC's CDS function.

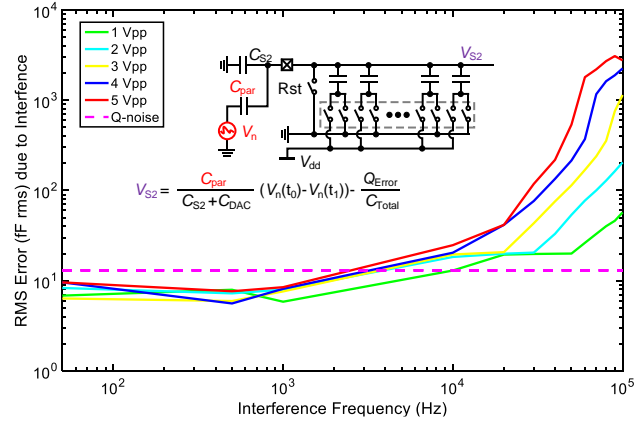


Fig. 18. CDS transfer function for interference and the measured rms error. ($C_{\text{par}} = 1\text{pF}$).

At a scan rate of 10 kHz, the CDC draws 333 nA from a 1 V supply. It achieves a quantization-noise limited resolution of 11.46 fF_{rms} (39.7 fF LSB), and a FoM_{Walden} of 61 fJ/c-s. In Table I and II, the performance of the tracking CDC is summarized and compared with the state-of-the-art and to commercial products. Compared to prior CDCs [6-9], it achieves competitive energy-efficiency, while offering self-capacitance sensing capability with excellent interference immunity.

Compared to state-of-the-art stand-alone readout systems for touch sensors, it consumes 15 nW per button, which is 46× better than the state of the art [2]. These characteristics make the presented readout IC a promising candidate for self-capacitance touch sensors with a limited power budget.

V. CONCLUSION

This paper presents an ultra-low power stand-alone readout IC for self-capacitance touch sensors. Low-power operation is achieved by utilizing the charge redistribution technique. An asynchronous tracking algorithm is proposed to realize data-dependent power consumption. This is especially efficient in wake-on-touch applications where the touch sensor spends most of its time in idle mode. Employing a differential architecture together with an intrinsic correlated-double sampling function heavily attenuates the effect of environmental interference and human finger noise. Including the on-chip relaxation oscillator, the readout IC achieves competitive energy-efficiency, while offering self-capacitance sensing capability with excellent interference immunity. The readout IC consumes only 15 nW per button from a 1.35 V supply (coin cell).

REFERENCES

- [1] Texas Instrument, "MSP430FR2633", Datasheet, Available online: <http://www.ti.com/lit/ds/symlink/msp430fr2633.pdf>.
- [2] Silicon Lab, "EFM32", Application Note, Available online: <https://www.silabs.com/documents/public/application-notes/an0028-efm32-lesense-capacitive-sense.pdf>.
- [3] Cypress Semiconductor, "PSoC4", Tech Note, Available online: <http://www.cypress.com/file/231251/download>.
- [4] H. Klein et al., "Advanced Capacitive Sensing for Mobile Devices", in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers: Advances in Analog Circuit Design 2018*, Springer 2018.
- [5] J.-H. Yang, et al., "A Highly Noise-Immune Touch Controller Using Filtered-Delta-Integration and a Charge-Interpolation Technique for 10.1-inch Capacitive Touch-Screen" *2013 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 390-391, Feb 2013.
- [6] Z. Tan, R. Daamen, A. Humbert, Y. V. Ponomarev, Y. Chae and M. A. P. Pertijs, "A 1.2-V 8.3-nJ CMOS Humidity Sensor for RFID Applications," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2469-2477, Oct. 2013.
- [7] Hui Jiang, Samira Amani, Johan G. Vogel, Saleh Heidary Shalmany, and Stoyan Nihtianov, "A 117dB In-band CMRR 98.5dB SNR CDC for Sub-nm Displacement Sensing with an Electrically Floating Target," in *2018 Symposium on VLSI Circuits*, HL, 2018.
- [8] Sujin Park, Geon-Hwi Lee, and SeongHwan Cho, "A 2.69uW Dual Quantization-based Capacitance-to-Digital Converter for Pressure, Humidity, and Acceleration Sensing in 0.18um CMOS," in *2018 Symposium on VLSI Circuits*, HL, 2018.
- [9] Sechang Oh, Wanyeong Jung, Kaiyuan Yang, D. Blaauw and D. Sylvester, "15.4b incremental sigma-delta capacitance-to-digital converter with zoom-in 9b asynchronous SAR," *2014 Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, HI, 2014, pp. 1-2.
- [10] S. Xia, K. Makinwa and S. Nihtianov, "A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time," *2012 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012.
- [11] R. Yang, M. A. P. Pertijs and S. Nihtianov, "A Precision Capacitance-to-Digital Converter With 16.7-bit ENOB and 7.5-ppm/°C Thermal Drift," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 3018-3031, Nov. 2017.
- [12] B. Yousefzadeh, W. Wu, B. Buter, K. Makinwa and M. Pertijs, "A compact sensor readout circuit with combined temperature, capacitance and voltage sensing functionality," in *2017 Symposium on VLSI Circuits*, Kyoto, 2017.
- [13] Y. He, Z. Chang, L. Pakula, S. H. Shalmany and M. Pertijs, "27.7 A 0.05mm² 1V capacitance-to-digital converter based on period modulation," *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015.
- [14] W. Jung, S. Jeong, S. Oh, D. Sylvester and D. Blaauw, "27.6 A 0.7pF-to-10nF fully digital capacitance-to-digital converter using iterative delay-chain discharge," *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015.
- [15] S. Oh et al., "A Dual-Slope Capacitance-to-Digital Converter Integrated in an Implantable Pressure-Sensing System," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1581-1591, July 2015.
- [16] H. Ha, D. Sylvester, D. Blaauw and J. Sim, "12.6 A 160nW 63.9fJ/conversion-step capacitance-to-digital converter for ultra-low-power wireless sensor nodes," *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, CA, 2014.
- [17] H. Omran, et al., "A 35fJ/Step Differential Successive Approximation Capacitive Sensor Readout Circuit with Quasi-Dynamic Operation," *VLSI Circuits Dig. Tech. Papers*, pp. 24-25, 2016.
- [18] H. Jiang, Z. Wang, C. Zhang, H. Jiang, and Z. Wang, "A combined low power SAR capacitance-to-digital analog-to-digital converter for multisenor system," *Analog Integrated Circuits and Signal Processing*, vol. 75, issue. 2, pp. 311-322, May 2013.
- [19] A. Sanyal and N. Sun, "An Energy-Efficient Hybrid SAR-VCO ΔΣ Capacitance-to-Digital Converter in 40-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1966-1976, July 2017.
- [20] F. M. Yaul and A. P. Chandrakasan, "A 10 bit SAR ADC With Data-Dependent Energy Reduction Using LSB-First Successive Approximation," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2825-2834, Dec. 2014.
- [21] S. Hussaini, H. Jiang, P. Walsh, D. MacSweeney and K. A. A. Makinwa, "A 15nW Per Button Noise-Immune Readout IC for Capacitive Touch Sensor," *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, Dresden, 2018, pp. 190-193.
- [22] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn, "Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog Converters Used in Successive Approximation ADCs," in *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 58, no. 8, pp. 1736-1748, Aug. 2011.
- [23] Masaya Miyahara, Yusuke Asada, Daehwa Paik, and Akira Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *2008 IEEE Asian Solid-State Circuits Conference*, 2008.
- [24] E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," in *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 52, no. 2, pp. 61-65, Feb. 2005.



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