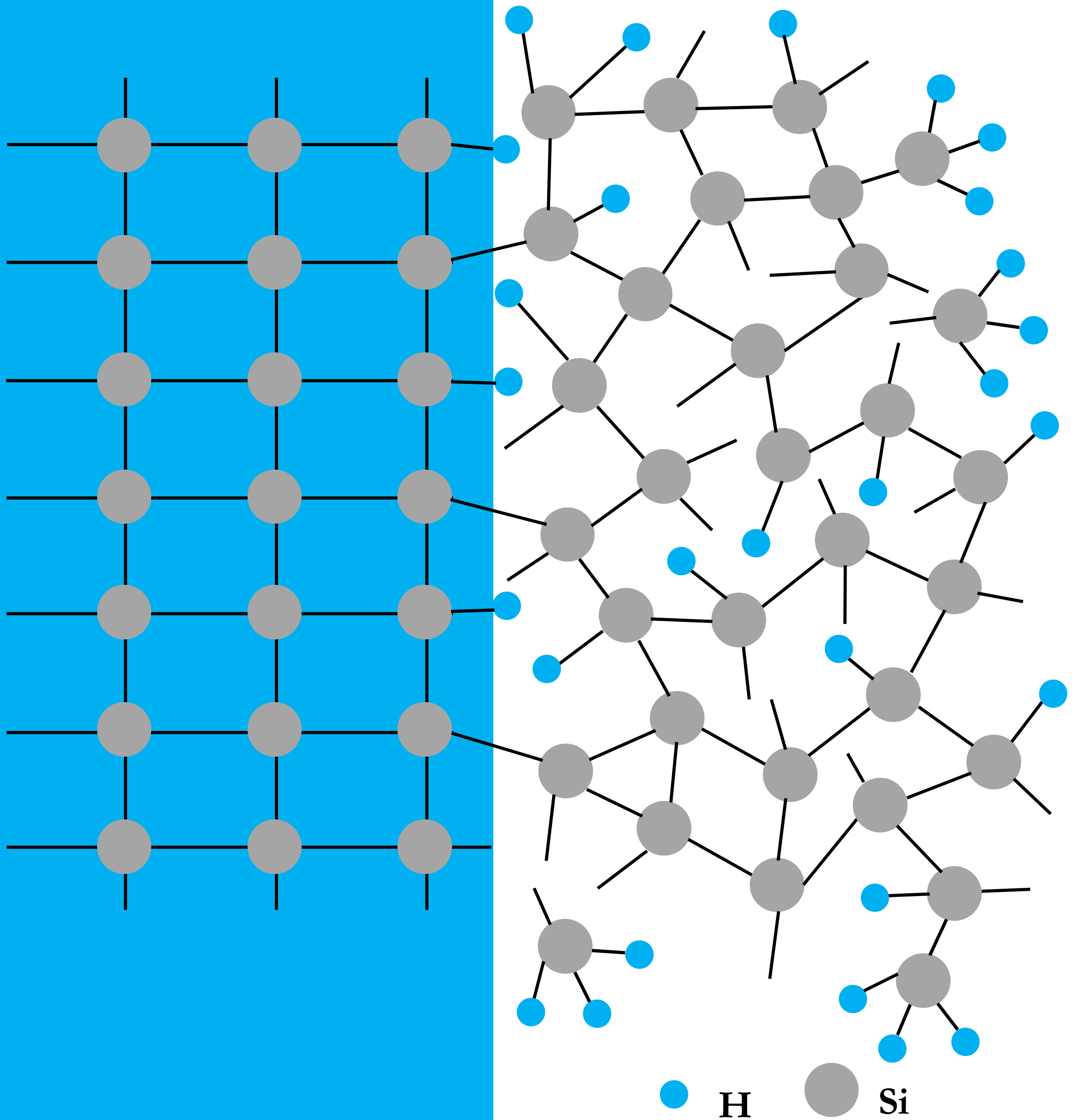
Contact Stack Evaluation for SHJ Solar Cells and Process Development of IBC-SHJ Solar Cells

Yifeng Zhao



EKL Else Kooi Laboratory
TU Delft Delft University of Technology
PVMD Delft University of Technology

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by

Yifeng Zhao

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PVMD Group, Sustainable Energy Technology, EEMCS Faculty

Delft University of Technology

Graduate

Yifeng Zhao

MSc Sustainable Energy Technology

Faculty of Electrical Engineering, Mathematics of Computer Science (EEMCS)

zhyf993@gmail.com

Supervisor:

Dr. Olindo Isabella, PVMD/ESE

Dr. Paul Procel Moya, PVMD/ESE

Dr. Guangtao Yang, PVMD/ESE

MSc Thesis Committee:

Prof. dr. Miro Zeman, PVMD/ESE

Dr. Olindo Isabella, PVMD/ESE

Dr. Paul Procel Moya, PVMD/ESE

Dr. Guangtao Yang, PVMD/ESE

Dr. Gregory Pandraud, EKL

Delft University of Technology

Department of Electrical Sustainable Energy

Photovoltaic Materials and Devices

ABSTRACT

Nowadays, silicon heterojunction (SHJ) solar cell is one of the most promising photovoltaic technologies thanks to the outstanding passivation quality from the a-Si:H layers. Together with the interdigitated-back-contacted (IBC) architecture, it enables the highest efficient, 26.7%, single junction c-Si solar cell. However, the mass production of such high efficient solar cells is limited, due to the complexity of the solar cell processes and the involved expensive TCO layer(s).

The objective of this thesis is to develop high efficiency, simple processed IBC-SHJ solar cells. To accomplish this goal, a comprehensive study 'from layer to device' is conducted: firstly, the focus is on the contact stacks deposited via PECVD, which includes intrinsic and doped hydrogenated amorphous silicon (a-Si:H) and nanocrystalline silicon oxide (nc-SiO_x:H) thin-film layers; Then the optimized passivation contact stacks are used in the front back contacted (FBC) solar cells, with which the factors that limit the fill factor (FF) and open-circuit voltage (V_{OC}) are identified; Lastly, a simplified process is developed to fabricate tunneling IBC-SHJ solar cells.

The influences of PECVD deposition parameters on passivation quality and carrier selectivity of the passivation and contact layer stacks were intensively studied. With the optimized 6 nm thick intrinsic a-Si:H layer an effective lifetime over 3 ms and implied-V_{OC} (iV_{OC}) beyond 720 mV are achieved on double side textured c-Si. Enhanced passivation qualities with iV_{OC} of 729 mV is obtained by adding the field effect passivation from the optimized n-type a-Si:H and nc-SiO_x:H layers on top of the excellent chemical passivation induced by the optimized 10 nm thick intrinsic a-Si:H layer. On the other hand, with the optimized intrinsic a-Si:H passivation layer, the deposition of p-type a-Si:H or nc-SiO_x:H does not deteriorate the overall passivation quality. Besides that the optimized p-type nc-SiO_x:H layer exhibits excellent activation energy of 51.4 meV, which closes to the optimal value for a high efficient hole selectivity, and a dark conductivity of 0.174 S/cm, which is high enough to facilitate the hole transport.

Research on FBC-SHJ solar cells reveals that thicker p-type nc-SiO_x:H layer is essential to ensure a smaller/no drop from SunsVoc to V_{OC}, which is related to minority carrier collection. Besides, such a thick doped nc-SiO_x:H layers can effectively shield the device precursor from the influence of ITO's field effect and keep the overall passivation quality after ITO sputtering. Accordingly, the best FBC device shows promising results in terms of SunsVoc with 727 mV and 734 mV, pFF of 0.862 and 0.841, measured before and after metallization, respectively. By implementing 3 nm n-type nc-Si:H instead of directly n-type nc-SiO_x:H in contact with ITO, FF improves from 0.56 to 0.73. The best manufactured FBC-SHJ solar cell (7.84 cm^2) exhibits V_{OC} of 710 mV, EQE short-circuit current density ($J_{SC,EQE}$) of 39.4 mA/cm^2, FF of 0.73 and efficiency of 20.4%.

For IBC-SHJ solar cells manufacture, the lift-off patterning approach is proved to be not suitable for processing double side textured cells, mainly due to the fact that the doped nc-SiO_x thin film alloys is not HF resistant. However, by applying this non-HF resistant property of the doped nc-SiOx alloys, a novel wet-chemical approach for processing tunneling IBC-SHJ solar cell is developed. This patterning approach allows to simplify the process. And the tunneling structure avoids the patterning step of the p-type nc-SiO_x:H layer. The first preliminary IBC device demonstrated with this approach exhibits V_{OC} of 659 mV, J_{SC} of 41.30 mA/cm^2, FF of 0.67, and efficiency of 18.2%. Further optimization on the thickness of the intrinsic a-Si:H layers induces an excellent V_{OC} of 719 mV with an average V_{OC} of 715 mV over 7 cells, J_{SC} over 41 mA/cm^2. However, the low FF (<0.60) is limiting the cells performance, which is mainly attribute to the low conductivity of the n-type nc-SiO_x:H layers.

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NOMENCLATURE

Nomenclature	*Meaning*	*Unit*
α	Absorption Coefficient	[-]
A	Absorbance	[-]
ARC	Antireflection Coating	[-]
a-Si:H	Hydrogenated Amorphous Silicon	[-]
BSF	Back Surface Field	[-]
CRN	Continuous Random Network	[-]
c-Si	Crystalline Silicon	[-]
CZ	Czochralski	[-]
DHs	Dihydrides	[-]
D_p	Diffusion Coefficient of Holes	[cm^2/s]
ΔE_C	Band Offset	[eV]
ΔE_V	Band Offset	[eV]
E_{act}	Activation Energy	[eV]
E_C	The Lowest Energy of Conduction Band	[eV]
E_F	Fermi Level	[eV]
E_G	Bandgap	[eV]
E_{mob}	Mobility Gap	[eV]
E_{ph}	Energy of Photon	[eV]
E_V	The Highest Energy of Valence Band	[eV]
FBC	Front-back-contacted	[-]
EQE	External Quantum Efficiency	[-]
FF	Fill Factor	[-]
FSF	Front Surface Field	[-]
FTIR	Fourier-transform Infrared Spectroscopy	[-]
FZ	Float Zone	[-]
G	Carrier Generation Rate	[cm^{-3}/s]

Nomenclature	*Meaning*	*Unit*
h	Planck Constant	[Js]
HDSP	Hydrogen Diluted Silane Plasma	[-]
HSM	High Stretching Mode	[-]
I	Transmitted Intensity	[mW/cm^2]
I_o	Total Incident Intensity	[mW/cm^2]
I_{ph}	Photocurrent	[A]
IBC	Interdigitated-back-contacted	[-]
IQE	Internal Quantum Efficiency	[-]
iV_{oc}	Implied Open-circuit Voltage	[mV]
J_o	Saturation Current Density	[mA/cm^2]
J_{sc}	Short-circuit Density	[mA/cm^2]
J_{ph}	Photogenerated Current Density	[mA/cm^2]
K_B	Boltzmann Constant	[J/K]
L_n	Diffusion Length of Electrons	[µm]
L_p	Diffusion Length of Holes	[µm]
LSM	Low Stretching Mode	[-]
MHs	Monohydrides	[-]
MCD	Minority Carrier Density	[cm^{-3}]
$\hat{n}$	Unit Outward Vector Normal to Surface	[-]
n_i	Intrinsic Carrier Concentration	[cm^{-3}]
nc-SiO_x:H	Hydrogenated Nanocrystalline Silicon Oxide	[-]
N_a	Concentration of Acceptor	[cm^{-3}]
N_d	Concentration of Donors	[cm^{-3}]
N_H	Hydrogen Density	[cm^{-3}]
N_{Si}	Silicon Density	[cm^{-3}]
N_C	Effective Density of States at Conduction Band	[cm^{-3}]
N_V	Effective Density of States at Valence Band	[cm^{-3}]
NIR	Near-infrared	[-]

Nomenclature	*Meaning*	*Unit*
PCD	Photoconductance Decay	[-]
PECVD	Plasma-enhanced Chemical Vapor Deposition	[-]
PSP	Pure Silane Plasma	[-]
q	Elementary Charge	[C]
QSSPC	Quasi-steady-state-photoconductance	[-]
R	Microstructure Factor	[-]
rf	Radio Frequency	[MHz]
r_p	Parallel Complex Amplitude Reflection Coefficient	[-]
r_s	Vertical Complex Amplitude Reflection Coefficient	[-]
s	Surface Recombination Velocity	[cm/s]
SE	Spectroscopic Ellipsometry	[-]
SHJ	Silicon Heterojunction	[-]
$Si\text{-}H_x$	Hydrogen Silicon Bond Configurations	[-]
SiH_4	Silane	[-]
SMs	Stretching Modes	[-]
SRH	Shockley-Read-Hall	[-]
t	Optical Thickness	[μm]
T	Transmittance	[-]
TAT	Trap-assisted-tunneling	[-]
TEM	Transmission Electron Microscopy	[-]
TCO	Transparent Conducting Oxide	[-]
TJ	Tunneling Junction	[-]
v	Frequency	[s^{-1}]
V_B	Self-bias Voltage	[V]
V_{bi}	Built-in Voltage	[V]
V_{oc}	Open-circuit Voltage	[mV]
VIS	Visible Light	[-]
W	Thickness of The Substrate	[μm]
η	Photoconversion Efficiency	[-]

Nomenclature	*Meaning*	*Unit*
τ_{aug}	Auger Lifetime	[μs]
τ_b	Bulk Lifetime	[μs]
τ_{eff}	Effective Lifetime	[μs]
τ_{rad}	Radiation Lifetime	[μs]
τ_s	Surface Lifetime	[μs]
τ_{SRH}	Shockley-Read-Hall Lifetime	[μs]
μc-Si	Microcrystalline Silicon	[-]
δn_S	Excess Minority Electrons	[cm^{-3}]
δp_S	Excess Minority Holes	[cm^{-3}]
ψ	Amplitude Ratio	[-]
ϕ	Work Function	[V]
$\Psi_{ph,\lambda}$	Spectral Photon Flow	[s^{-1}]
Δ	Phase Difference	[-]
ω	Wavenumber	[cm^{-1}]
σ_d	Dark Conductivity	[S/cm]
μ_n	Mobility of Electrons	[cm^2/Vs]
μ_p	Mobility of Holes	[cm^2/Vs]
χ	Electron Affinity	[V]

1

INTRODUCTION

'If we are serious about moving toward energy independence in a cost-effective way, we should invest in solar energy. If we are serious about cutting air and water pollution and reducing greenhouse gas emissions, we should invest in solar energy.'

-Bernie Sanders

1.1 Solar Energy: The Technology on The Upbeat

Global warming, the most important challenge that humankind is facing in 21st century [1], is promoting the ongoing global sustainable transition of energy system. Decarbonization of the current energy system requires abundant of renewable technologies to be implemented simultaneously. Among all those technologies, the booming of solar photovoltaic (PV) deployment in 2016 is reported to expand more than 50% of solar PV capacity in 2015, which also strongly boosts renewable energy accounts for over two third of the new power capacity installed in 2016 [2]. More than 31,000 solar panels are installed per hour in 2016 [3]. Solar PV is now becoming the world's fastest growing energy technology [2, Fig. 1.1] and solar related renewable energy is providing the most jobs in renewable energy field [3, Fig. 1.2]. Until 2017, the cumulative installed capacity of solar PV reached over 400 GW_p [4]. Therefore, efficient light conversion and low production cost of solar PV modules are imperative and critical to continuing the prosperity of this technology for the present and the future.

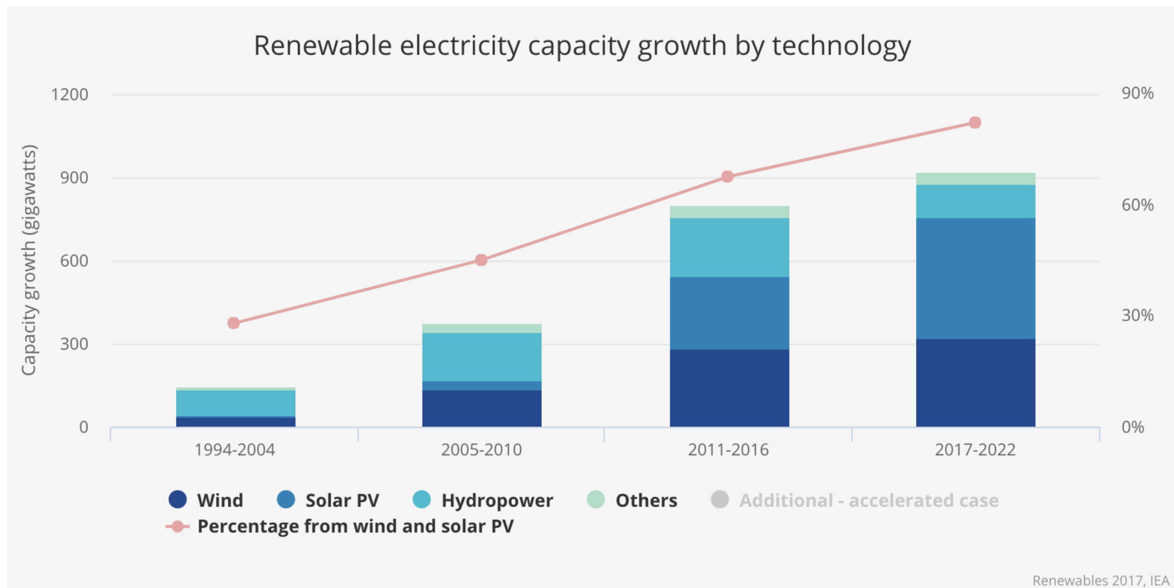


Figure 1.1 The renewable electricity capacity growth by technology from 1994 to 2022. A significant increment of solar PV is presented. Adapted from [2].

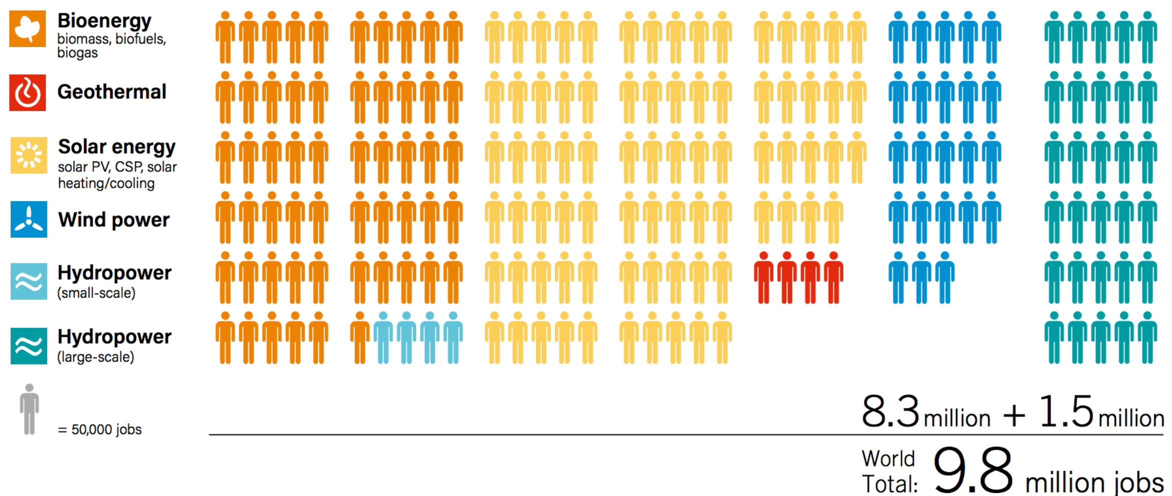


Figure 1.2 The jobs in renewable energy in 2016. Adapted from [3]. Solar energy including solar PV, thermal concentrated solar power (CSP) system, solar heating/cooling provides most jobs among all the renewable technologies.

1.2 The Working Principle of a Solar Cell

The thriving solar PV market is a technologically diverse market. Among all different technologies, the basic working principle of a solar cell is based on photovoltaic effect, i.e. the potential is generated over the junction that are formed by two different materials when receiving the electromagnetic radiation. Light, the energy from sun to earth, is assumed to be consisted with a lot of photons contain certain energy ($E = h\upsilon$, where h is Planck constant, υ is the frequency of

light) by Albert Einstein. The bandgap of a semiconductor that is used as the absorber of light is presented below. The light with energy (E_{ph}) larger than the bandgap (E_G) will excite the electron (e^-) form valence band (VB) to conduction band (CB), while leaving a positively charged hole (h^+) in VB. Both VB and CB are allowed energy states for conduction of charge carriers.

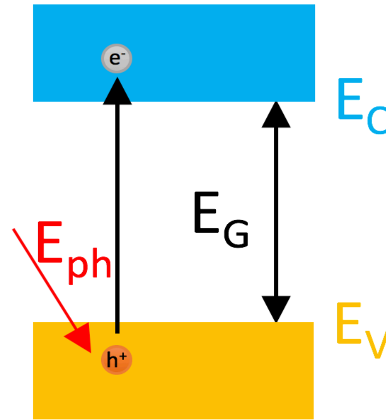


Figure 1.3 The generation of electron-hole pair when an incident light with energy larger than the bandgap of the material. E_C and E_V are the conduction band edge and valence band edge, respectively. Photon with energy less than the E_G is transmitted (not absorbed) through the material.

After the generation of electron-hole pairs, electrons and holes are selectively collected with kind of 'semipermeable membranes' (ideal situation) and flow out to the external circuit and been utilized as the form of electricity. Since a closed loop is formed, the electrons that pass through the external circuit will recombine with holes at the hole contact.

After understanding the working principle of a solar cell, a specified solar cell technology which is so called silicon heterojunction solar cell is introduce in the next section. This is also the technology studied in this thesis.

1.3 Silicon Heterojunction Solar Cell

1.3.1 Introduction of Development Status

It is well-known that Silicon Heterojunction (SHJ) solar cell is one of the most efficient photovoltaic technologies nowadays concurrently with advantages of lower manufacture cost compared to that of the conventional crystalline silicon solar cells [5]. The reported world record photoconversion efficiency (η) for standard (front-back-contacted) SHJ (FBC-SHJ) solar cell is 25.1%, which was principally based on the improvement of effective minority carrier lifetime (τ_{eff}) of the solar cell [6]. However, some disadvantages are related to this kind of structure. For instance, lesser incident light can be absorbed due to the optical shading caused by the metal contact grids

at the front side. As a result, the short circuit current density (J_{sc}) and then further the photoconversion efficiency (η) of the solar cell still have room for improvements. Therefore, compared to the standard SHJ solar cell, the interdigitated back-contacted silicon heterojunction (IBC-SHJ) solar cell, which removes the front metal contact grids to the backside of the solar cell offering better overall cell performance. The certified record photoconversion efficiency for this type of solar cell is recently reached 26.6%, which is manufactured by Japanese Kaneka Corporation [7]. During the 33rd European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC 2017), the record is refreshed to over 26.7% by Kaneka. This efficiency is quite close to the calculated theoretical maximum efficiency (29.43%) for the crystalline silicon (c-Si) solar cell [8]. According to the promising results developed on IBC-SHJ solar cell, the intensely research interests are reflected by massive published literatures related to this topic [9]–[15]. The developments of monocrystalline silicon solar cells in past 20 years is presented in [16, Fig. 1.4].

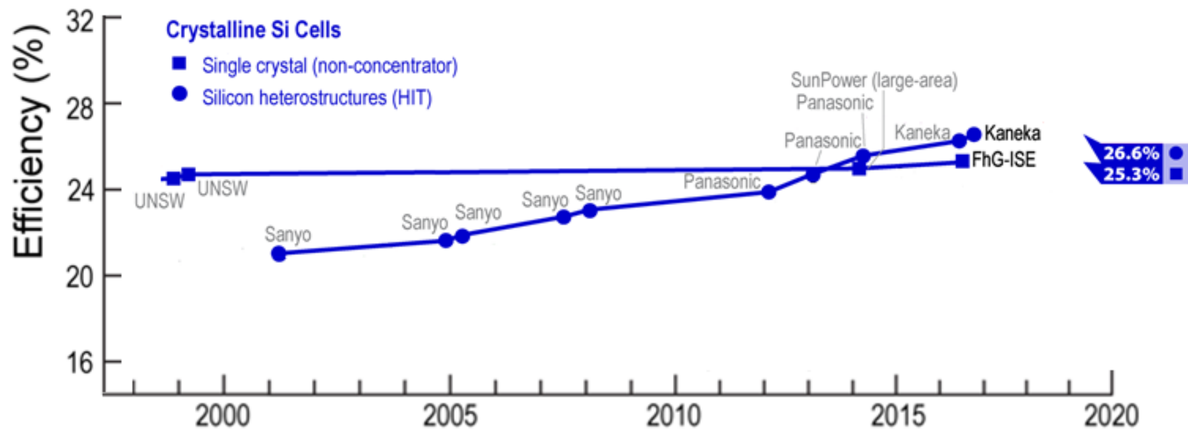


Figure 1.4 The record efficiency developments of monocrystalline silicon solar cells in past two decades. Adapted from [16].

1.3.2 Comparison of Silicon Heterojunction and Homojunction Solar Cells

The basic structure of a FBC-SHJ solar cell within this thesis is presented in Fig. 1.5. The double side textured (DST) float-zone (FZ) <100> n-type (phosphorus doped) c-Si wafer is used as the effective absorber. Then hydrogenated intrinsic amorphous silicon (i-a-Si:H) layers passivate both sides of the c-Si substrate. On top of intrinsic layers, the 'semipermeable membranes' mentioned previously are deposited, i.e. either n-type or p-type (boron doped) silicon layers. In this project, for the same type of doping, different materials are tested and optimized, namely, hydrogenated amorphous silicon (a-Si:H) and hydrogenated nano-crystalline silicon oxide (nc-SiO_X:H). At the front side, transparent conductive oxide (TCO) is necessary according to low lateral conductivity of doped materials, besides, it also acts as the anti-reflection coating (ARC) at front. Rear TCO layer can be also applied but not for lateral conductivity. Rear TCO is used as a contact and optical

layer which is mainly for improving the near infrared region (NIR) response [17], also prevent spiking/diffusion of metal contacts [18]. The metals contacts are eventually formed for connecting the solar cell to the external circuit.

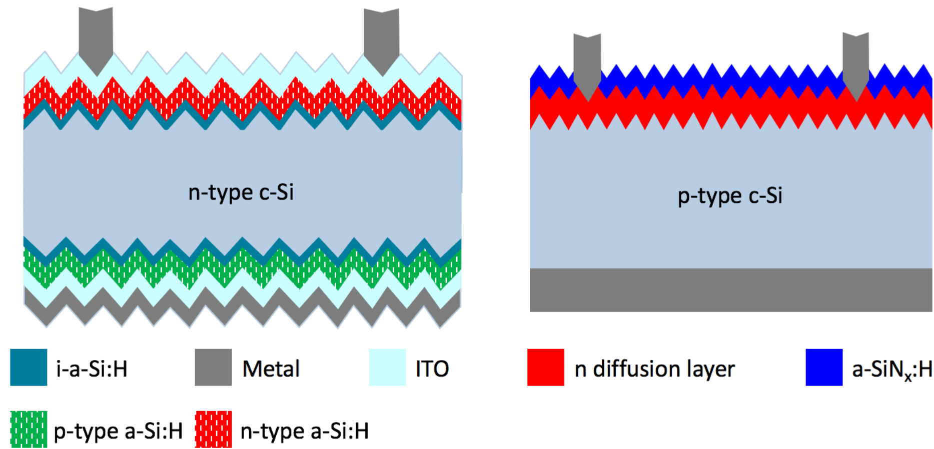


Figure 1.5 The schematic representation of a FBC-SHJ solar cell (left) and a conventional homojunction solar cell (right). Structures are not scaled according to the practical case.

After being aware of the typical structure of a FBC-SHJ solar cell, the electronic band diagram of n-type SHJ solar cell under dark and thermal equilibrium is illustrated below in [19, Fig. 1.6]. As mentioned previously, the a-Si:H can not only provide passivation to c-Si surface, but also forms the band bending or band offsets (ΔE_V or ΔE_C) such as a-Si:H (p^+)/a-Si:H (i)/c-Si and a-Si:H (n^+)/a-Si:H (i)/c-Si by applying different bandgap materials to realize carrier selective transport [20]. Different from FBC-SHJ solar cells, the junction of conventional homojunction solar cells are diffusion based junctions. This is also the origin of 'heterojunction' and 'homojunction'. Normally a Gaussian like distribution of in-diffused dopants in p/n junction of a conventional solar cell, while an abrupt interface distribution profile in a-Si:H (or nc-SiOx:H)/c-Si interface of SHJ solar cell.

In conventional solar cells, high phosphorus doping with high surface concentration is required for semiconductor metal interface to reduce recombination and contact resistivity. However, this also induces electronic losses such as Auger recombination and bandgap narrowing [18]. In SHJ solar cell, the formed energy barrier or band bending effectively minimizes injection of minority carriers into the oppositely doped layer, i.e. effective collection of charge carriers then higher V_{OC} of the final device.

Figure 1.6 The electronic band diagram of n-type SHJ solar cell under dark and thermal equilibrium. Adapted from [19]. Different carrier transport mechanisms are shown, namely, a). trap-assisted tunneling (TAT), b). direct tunneling and c). thermionic emission.

Besides, since higher bandgap materials are used at illuminated side (e.g. a-Si:H: $E_G \approx 1.7$ eV, c-Si: $E_G \approx 1.12$ eV), lesser parasitic absorption is observed in SHJ solar cell. This enables better light management for obtaining higher J_{SC} of the final device.

Moreover, instead of p-type c-Si substrate, n-type c-Si wafer is often used as the absorber in SHJ solar cells, which suffers lesser light induced degradation and is cheaper to be produced with high quality due to its higher tolerance to the impurities [21]. The p-type c-Si substrate is also studied for the SHJ solar cell, however, due to the band structure and asymmetry in interface defect capture cross sections for p-type SHJ solar cell [19], it does not show better performance or even comparable to the n-type SHJ solar cells.

In terms of manufacture process, SHJ solar cells are made under low temperature process (below 200 °C) compared to high temperature homojunction solar cells (up to around 1000 °C). In other words, fabricating SHJ solar cells have a lower thermal budget compared to homojunction solar cells [20]. Meanwhile, low temperature reduces the risk of wafer blowing [20]. The industrialized manufacture time of a SHJ solar cell is also reported to be shorter than homojunction one [20].

1.3.3 Interdigitated Back-Contacted Silicon Heterojunction Solar Cell

IBC-SHJ as a promising candidate for high efficiency solar cell is also studied in this thesis. As suggested by its name, the junctions that selectively collect holes and electrons are all moved to the rear side of the solar cell and interdigitated arranged. The schematic representation of a lift-offed IBC-SHJ solar cell and a tunneling IBC-SHJ solar cell manufactured in this thesis are shown in Fig. 1.7.

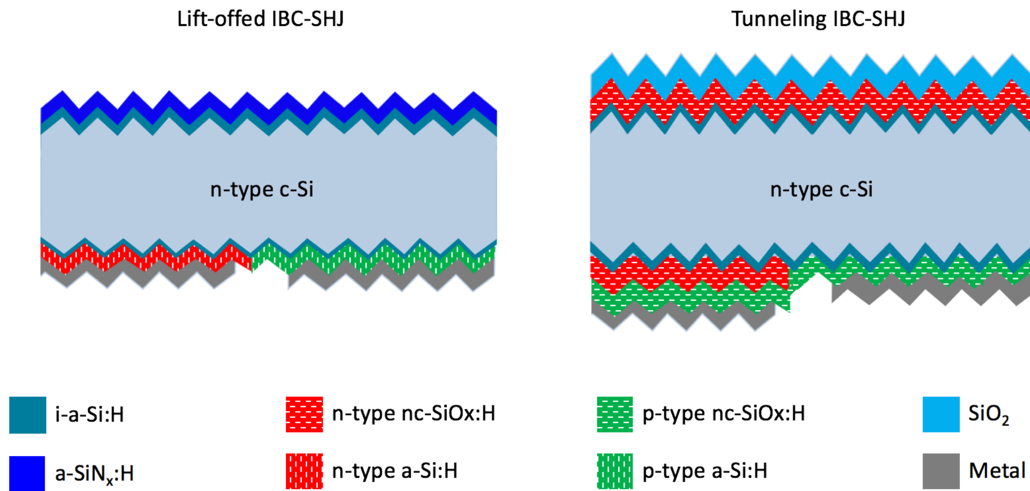


Figure 1.7 Schematic representation of typical structures of a double side textured lift-offed IBC-SHJ and a double side textured tunneling IBC-SHJ solar cells. Structures are not scaled according to the practical case.

As shown in Fig. 1.7, the lift-offed IBC-SHJ uses p-type a-Si:H as emitter and n-type a-Si:H as back surface field (BSF), while a tunneling IBC-SHJ uses n-type nc-SiO_x:H and p-type nc-SiO_x:H layer stack as BSF (electron collecting region), and p-type nc-SiO_x:H as emitter. The working principle of the electron collecting (interband tunneling) passivating contact in tunneling IBC-SHJ is explained in Chapter 6.

The passivation of full rear area is critical for the final V_{OC}, while the FF of this device is mainly dependent on the interface quality of i-a-Si:H/p-type contact [22] and the metal coverage [23]. Although two structures shown in Fig. 1.7 have connected BSF and emitter, low lateral conductance of doped silicon layers leads to expected negligible shunt happens (confirmed within the thesis).

Since no metal contacts are covered at front side (no need for collecting charge carriers at front side), it provides more freedom to optimize the structure of front side to improve the J_{SC}. Based on different manufacture process of IBC-SHJ solar cells, the a-SiNx:H can be applied as ARC but it should be the first step since it is deposited under relatively high temperature (400°C) for high quality layer. If ARC is deposited after rear side junctions are formed, low temperature (150 °C) SiO_2 can be utilized as ARC as well. For some IBC-SHJ solar cells, the front surface field (FSF) that is either highly phosphorus doped n^+-type layer (ion-implanted) or n-type doped silicon layer can be applied to the front side to prevent diffusion of minority holes from the c-Si substrate to the front side to recombine. If no FSF or lowly-doped FSF is used, excellent passivation is required [24] for achieving high V_{OC}.

In general, rear emitter FBC-SHJ solar cell is manufactured to examine the passivation and FF, which should have similar effects when those layers are applied on the IBC-SHJ solar cell. It is also reported the FF is worse in IBC-SHJ than FBC-SHJ solar cells [25].

1.3 Research Goals

It is widely accepted that the high open circuit voltage (V_{oc}) is crucial for the obtained high efficiency SHJ solar cells [26]–[28]. The main reason for the attained high V_{oc} is due to the implementation of i-a-Si:H between the crystalline silicon (c-Si) substrate and the doped silicon layers. With the well optimized i-a-Si:H layers, the recombination can be effectively suppressed at the interfaces of c-Si and doped silicon layers [26].

Aside from the i-a-Si:H layer, optimized doped contact stacks are necessary for providing better band bending between c-Si/i-a-Si:H which enable possibilities for higher V_{oc} of final device [29]. It is also critical for forming low resistive interface between TCO and doped silicon layers [29], which influences the fill factor (FF) of final device.

Therefore, the first main scientific research goal of this thesis is proposed:

- How to optimize deposition parameters of i-a-Si:H in terms of good passivation and uniformity? How to optimize deposition parameters of doped silicon layers according to good conductivity and passivation quality?

Once all the optimized layers are ready, the manufacture of FBC-SHJ and IBC-SHJ is conducted. For FBC-SHJ, the main research goal is:

- Integrate the optimized contact stacks to FBC-SHJ solar cells to identify the limiting factors of FF and V_{OC}.

After successful manufacture of FBC-SHJ solar cell as a proof of concept, the corresponded structure and contact stacks are transferred to IBC-SHJ solar cell. Therefore, the last main research goal is:

- Optimize the manufacture process of IBC-SHJ solar cells with layers from well-performed FBC-SHJ solar cell and achieve a high efficiency.

1.4 Outline

In this thesis, study is done mainly based on the research goals proposed above. The thesis comprises seven chapters in total.

In the first chapter, general introduction of thriving solar energy technology market, working principle of a solar cell is given. Besides, silicon heterojunction solar cell (FBC-SHJ and IBC-SHJ) is introduced and compared with conventional homojunction solar cells. The second chapter

introduces the material properties of passivation contacts that are optimized and applied for SHJ solar cells. Besides, the mechanism of passivation and recombination are explained. The tools and techniques that are used to manufacture and characterize the SHJ solar cells are introduced and explained in the third chapter. In the third chapter, the investigations of hydrogenated intrinsic amorphous silicon layer and doped silicon layers' optimizations are explained and conducted. After obtaining optimized layers, the manufacture of FBC-SHJ solar cell is conducted. The limiting factors of FF and V_{OC} of cells with this structure are investigated and analyzed. In the sixth chapter, the manufacture of both flat-rear and textured-rear lift-offed IBC-SHJ solar cells are conducted and analyzed. Inspired from the limiting factors of the standard process, the tunneling IBC-SHJ solar cells are successfully manufactured. Lastly, the main results are summarized, the conclusions are drawn and the outlooks are given for further research on this topic.

2

FUNDAMENTALS

This chapter firstly reviews the literature that is concerned about explanation of the material properties of passivating contacts that are used in this thesis. After being aware of the material properties, a more comprehensive understanding of passivation and recombination based on material properties can be acquired.

2.1 Hydrogenated Amorphous Silicon

Unhydrogenated a-Si was developed around 1950s to 1960s due to strong research interest in the amorphous semiconductors. However, serious high defect density of a-Si was proven to be problematic for semiconductor industry, for instance, difficulty for doping and unacceptable photoconductivity [30]. Then the a-Si:H was firstly developed by Chittick, Alexander and Sterling in UK in the late 1960s [31]. There is no substantial change of the current method to deposit the a-Si:H from that of late 1960s, which is introduced in next chapter about PECVD. Afterwards, it was firstly utilized in photovoltaic devices by Carlson and Wronski in 1976 and an initial efficiency around 2% is achieved [30]. Thanks to the promising start, fast evolution of the efficiency was achieved and reached around 13% until 1989 [30]. Later, Japanese Sanyo company made a great progress on the development of a-Si:H in the market. Until now, due to state-of-art concept such as high efficiency SHJ solar cells, the research on a-Si:H is still attracting and promising.

2.1.1 Atomic Structure

Crystalline silicon (c-Si) is tetrahedrally bonded to other four neighbor atoms, there is a long-range periodic order of this tetrahedral structure in c-Si [32, Fig. 2.1]. That is, the lattice structure and orientation are same for all directions, which results a well-ordered lattice or less defects in the bulk. However, as suggested from the name, the disorder of the atomic structure (continuous random network) of a-Si:H is the main difference between a-Si:H and c-Si. Although fourfold coordination structure of a-Si:H can be found in short-range order [32, Fig. 2.1], the slightly distortion of Si-Si bond length and angle happens compared to that of c-Si. Those bonds with

deviated bond angles and lengths are called as weak or strained bonds [33]. In general, weak bond has higher energy than the normal Si-Si bond, which is more unstable and easier to break and form defects. As for the long-range order, some of the silicon atoms are not full fourfold coordinated, therefore, those unbonded valence electrons exist as dangling bonds.

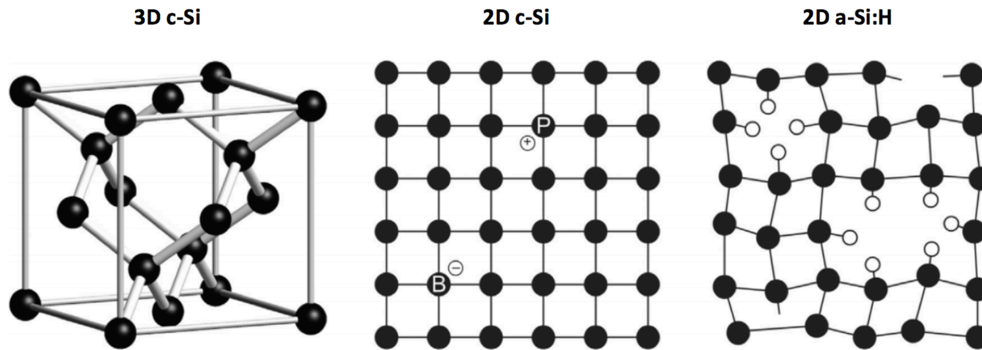


Figure 2.1 Representation of the crystallographic unit cell of c-Si, substitutional phosphorus and boron doping of c-Si, the a-Si:H with hydrogen saturated dangling bonds and unsaturated dangling bonds. Adapted from [32].

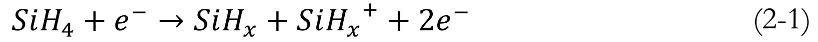
In a-Si:H, the dangling bonds are not homogeneous distributed, but normally grouped as monovacancy, divacacy, trivacancy, 2 monovacancies, 6-ring void, platelet and even nanosized voids [34]. Those dangling bonds act as the recombination centers in both the a-Si:H bulk and interface of a-Si:H/c-Si, leading to high rate of Shockley-Read-Hall (SRH) recombination [35]. SRH recombination is the impurity atom or lattice defect induced recombination, which forms trapping state within the band gap. Generally, SRH recombination is the dominant mechanism for semiconductors at most operating conditions [21]. If the bulk is too defective, then the tunneling recombination which is defect-assisted will be more significant [36]. But for the case of SHJ solar cell, the a-Si:H/c-Si interface defect density affects more negatively about the passivation quality.

Generally, Fourier Transform Infrared Spectroscopy (FTIR) is used for determining the microstructure of the hydrides in a-Si:H amorphous structure. According to the reported results [37], if monohydrides (MHs or Si-H: 2000 cm^{-1} [38]) (corresponded to low stretching mode) are the majority contents in the amorphous layer, the defect density is shown to be low and an abrupt a-Si:H/c-Si interface can be detected by transmission electron microscopy (TEM), that is, less dangling bonds and better passivation is obtained. In contrast, if the dihydrides (DHs or Si-H_2: 2090 cm^{-1} [38]) (corresponded to high stretching mode) are the main components, higher microvoids and defect density are formed, which results poor passivation results.

2.1.2 Growth and Passivation Mechanisms of i-a-Si:H

For deposition of a-Si:H, radio-frequency plasma enhanced chemical vapor deposition (rf-PECVD) is extensively used. The working principle of rf-PECVD in the next chapter. For simplification,

precursor gas SiH_4 with a certain dilution with H_2 is applied for i-a-Si:H. During its deposition, the main reactions can be generally expressed as:



$$SiH_4 + e^- \rightarrow SiH_x + {SiH_x}^+ + 2e^- \qquad (2\text{-}1)$$

$$H_2 + e^- \rightarrow H + H^+ + 2e^- \qquad (2\text{-}2)$$

Although different reactions could happen spontaneously when the SiH_4 molecules are collide with energized electrons (more detailed explanation in [20]), radical SiH_3 is the most abundant species among all products if low power (< 10 W/cm^2) and low pressure (< 10 Pa) are applied and it is also the main film precursor of low defect density a-Si:H deposition [20]. The standard view of the interaction between SiH_3 and hydrogenated c-Si surface are illustrated below in [20, Fig. 2.2].

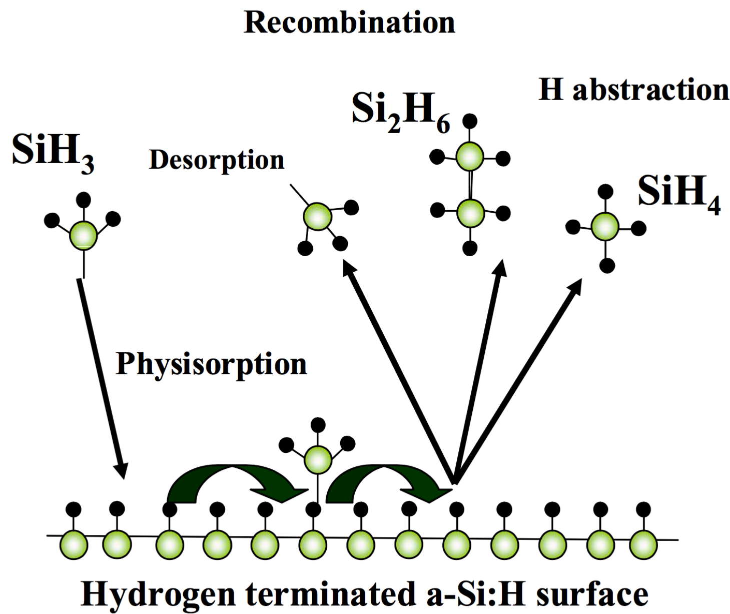


Figure 2.2 The standard view of the interaction between SiH_3 and hydrogenated c-Si surface. Adapted from [20].

The general growth of a-Si:H can be summarized as [39]: firstly, the diffusion of SiH_3 radicals to the hydrogenated c-Si surface; then, physisorption of SiH3 rather than chemical bonding and diffuse on the growing film; lastly, chemical bonding with Si dangling bonds.

The dangling bonds then existed on the surface of c-Si can be effectively passivated by depositing a-Si:H layer to form Si-Si bonds. Since not every dangling bond can be passivated in this way, the hydrogenated deposition provides an alternative, which enables termination of dangling bonds by atomic hydrogen. Therefore, sufficient atomic hydrogen is critical and efficient to saturate the dangling bonds on the surface of c-Si.

For the layer itself, if no hydrogen dilution during the deposition, the formed a-Si has defect density up to 10^{21} cm^{-3}. Sufficient hydrogen dilution can decrease the defect density down to 10^{15}

- 10^{16} cm^{-3}, in other words, every one million Si atoms there is at most one dangling bond [21]. Therefore, part of the project aims on generating more active atomic hydrogen during the growth of a-Si:H to provide excellent passivation.

2.1.3 Energy States

Schrödinger equation that is used for explaining the electronic properties of c-Si is not feasible for a-Si:H according to no long-range periodic order existed in a-Si:H. However, the density of electronic states (DOS) N_E that describes the number of allowed states per unit volume and energy is still valid for a-Si:H.

As shown in [33, Fig. 2.3], both c-Si and a-Si:H have the conduction band E_C and valence band E_V which represent the allowed energy states. Differently, for c-Si, between the E_C and E_V, there

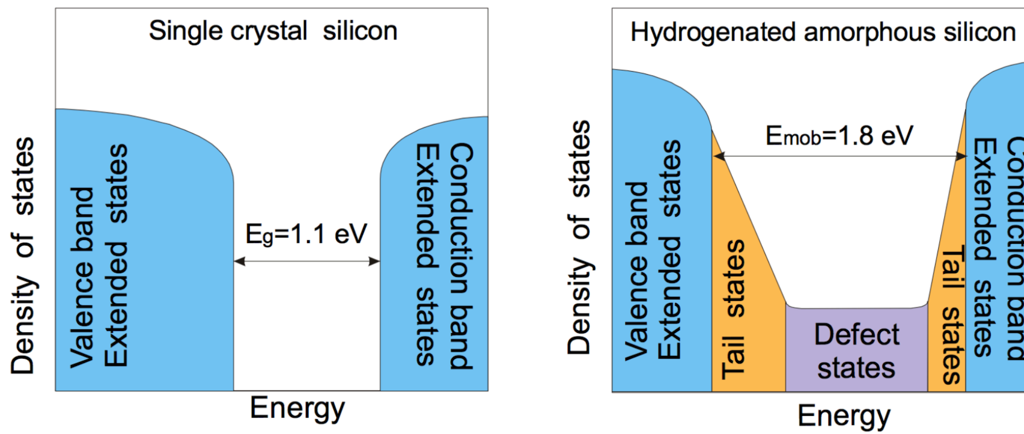


Figure 2.3 The schematic illustration of distribution of allowed energy states in c-Si and a-Si:H. Adapted from [33].

is so called band gap E_G that has no allowed states inside, while as for a-Si:H, there is no well-defined E_G because both E_C and E_V show the continuous distribution of DOS extend to the band gap region. Those regions are called as band tail states. In the atomic level, those band tail states reflect the energy states of the previously mentioned weak bonds in the a-Si:H. The wider the tail states, the more degree of disorder in the a-Si:H material.

As illustrated in Fig. 2.3, there are allowed defect states in the band gap region, which can also explain the aforementioned dominant SRH recombination in a-Si:H material. Besides, since the defect and tail states are within the structure, so they are defined as localized states. In contrast, there are non-localized states in which the charge carriers are free carriers, those states are called as extended states. According to different mobility of charger carriers in localized and extended states, i.e. the mobility of charge carrier is much higher in extended states, the band gap of a-Si:H can be defined based on the carriers' mobility and called as mobility gap E_{mob}. The value of the E_{mob} is based on the energy difference between two mobility edges which are close to the interface

of the localized states and the extended states. As shown in [33, Fig. 2.3], the E_{mob} of a-Si:H is 1.8 eV, which is higher than the band gap of c-Si. The tail states together with the defect states both are the trapping centers, which are detrimental to the lifetime of charge carriers [33]. Within this thesis, the E_{mob} of a-Si:H is presented as E_G.

2.1.4 Optical and Electrical Properties

Due to different atomic structure of a-Si:H from c-Si, which is an indirect bandgap material, a-Si:H is a direct bandgap material. In general, the bandgap of a-Si:H varies from 1.6 eV to 1.8 eV based on the amount of hydrogen integrated into the amorphous network. Therefore, the absorption coefficient of a-Si:H in the visible part of the spectrum (390 nm to 700nm or 3.18 eV to 1.77 eV) is around 70 times higher than that of the c-Si [33]. The optical properties of a-Si:H can be varied if it is alloyed with elements such as carbon and germanium [33].

The electrical properties are close related to the previously introduced atomic structure and energy states of a-Si:H. The values of mobility for holes and electrons in a-Si:H is around one hundred times smaller than that of c-Si. For c-Si at 300 K, the holes and electrons mobility are around 460 $cm^2V^{-1}S^{-1}$ and 1360 $cm^2V^{-1}S^{-1}$, respectively [33]. As for a-Si:H, those values drop to only 1 $cm^2V^{-1}S^{-1}$ and 10 $cm^2V^{-1}S^{-1}$ for holes and electrons, respectively [33]. Reasons behind the phenomenon are exactly due to the existence of dangling bonds [40] , floating bonds which are silicon with five bonds [41]. Despite of these abnormal silicon bonds, it is also reported that a-Si:H material has the natural of structural hole-trapping defects, which leads low mobility of holes in a-Si:H [42]. Consequently, low dark conductivity for a-Si:H less than 10^{-10} $\Omega^{-1}cm^{-1}$ can be measured [33]. Different doping regimes of a-Si:H with phosphorus and boron can influence their conductivities. As reported in [43], n-type a-Si:H has a higher dark conductivity measured compared to p-type a-Si:H. It is also known that alloying of oxygen into a-Si:H leads to decreased conductivity [44].

2.2 Hydrogenated Nanocrystalline Silicon

Hydrogenated nanocrystalline silicon (nc-Si:H), also known as hydrogenated microcrystalline silicon (mc-Si:H), can be deposited by PECVD as well. With comparison to a-Si:H, more hydrogen dilution is compulsory for nano-crystal growth [45].

2.2.1 Atomic structure

As illustrated below in [33, Fig. 2.4], nc-Si:H has the paracrystalline (lacking long-range ordering) structure. Within this structure, small nanocrystals are embedded in the amorphous (a-Si:H) main structure. Therefore, similar to that of a-Si:H, defective dangling bonds within the bulk of the material, potentially act as recombination centers for SRH recombination, can be partially passivated by hydrogen that are supplied during the growth of the film.

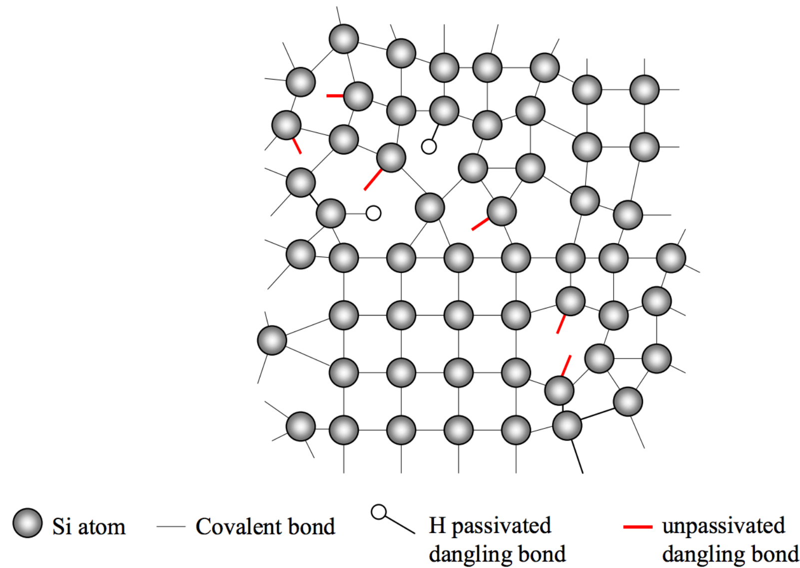


Figure 2.4 Schematic illustration of microcrystalline silicon. Adapted from [33].

2.2.2 Growth Mechanism

There are different growth mechanisms for nc-Si:H [46][47]. Within this thesis, the growth rate of nc-Si:H layer is observed to much slower than that of a-Si:H. This can be explained by the so-called etching model for nc-Si:H growth [46]. Since sufficient hydrogen is applied in the plasma, the weak Si-Si bonds (energetic unfavorable configurations) are etched by energetic hydrogen atoms in the growth regime, meanwhile, the layer is formed similar as that is described in section 2.1.2 for a-Si:H. Another mechanism is chemical annealing model [47], where hydrogen atoms are crucial for chemically transfer the amorphous Si structure to well-ordered crystalline structure. Either in etching model or chemical annealing model, enough hydrogen supplied is of great importance for nc-Si growth.

As illustrated in [48, Fig. 2.5], the beginning of nc-Si:H growth is fully amorphous, which is called as incubation layer [49]. The thickness of the incubation layer is highly substrate dependent [50] and it is in the order of few nanometers [51]. After a certain thickness, the deposited layer start to be more crystallized and gradually saturate with relatively high crystalline fraction. During the growing process, the voids fraction increases initially till the nucleation stage and gradually decreases with crystal growth [52]. As reported in [53], seed layer or CO_2 plasma can be applied for reducing the thickness of incubation layer.

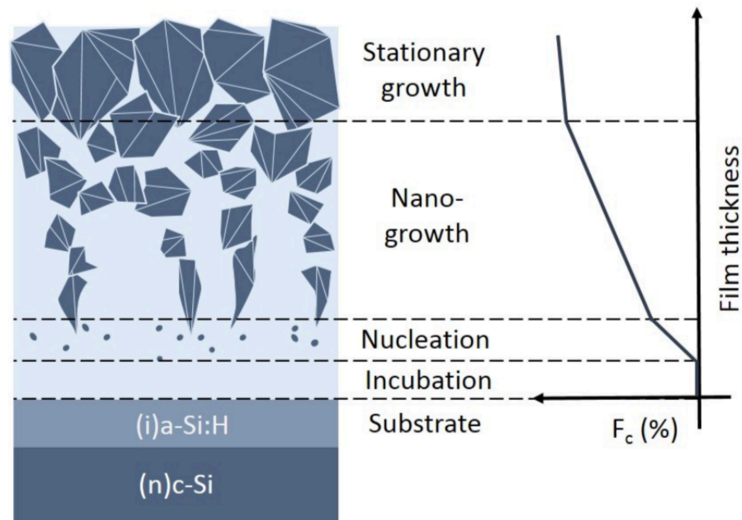


Figure 2.5 The schematic illustration of nc-Si:H growth on an amorphous substrate. F_C represents the crystalline fraction of the film. Adapted from [48].

2.2.3 Optical and Electrical Properties

As shown in [48, Fig. 2.6], although nano-crystals are existed in nc-Si:H, depends on the crystalline fraction, the absorption coefficient of nc-Si:H differs from that of c-Si. Compared to a-Si:H, the using of nc-SiO_x:H provides more favorable absorption coefficient. The formed nc-SiO_x:H has increased bandgap (over 2 eV [21]) and better refractive index matching [53], which are benefit for solar cell light management (lower parasitic absorption and lower reflection [53]). Besides, since nanocrystals are existed, which enable high doping efficiency, i.e. good conductivity. The structure of nc-SiO_x:H is similar to that of nc-Si:H but nano-crystals are embedded in a-SiO_x:H matrix rather than a-Si:H [54].

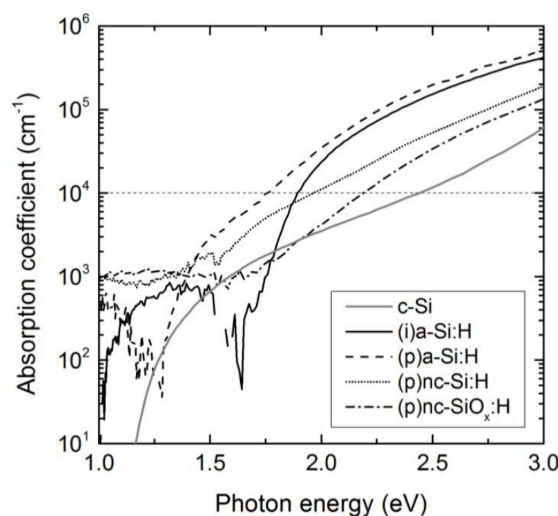


Figure 2.6 Absorption coefficient as a function of photon energy for different materials. Adapted from [48]. Photon energy from 3.0 to 1.0 eV is corresponded to wavelength from 413 to 1240 nm.

Therefore, it is more interesting to alloy oxygen into nc-Si:H film to tune its optical properties. As reported in [55] and shown in [55, Fig. 2.7], a favorable reduced refractive index is observed if a higher content of oxygen is alloyed into the film. However, the conductivity also decreases, in other words, the crystalline fraction decreases. This applies for both doping types of nc-SiO_x:H. Besides, alloying of oxygen into n type layer enables a more flexible tuning of optical and electrical properties due to increased optical performance without significant drop of conductivity compared to p-type nc-SiO_x:H [55]. As reported in both [54] and [55], the n-type nc-SiO_x:H has better dark conductivity compared to p-type nc-SiO_x:H.

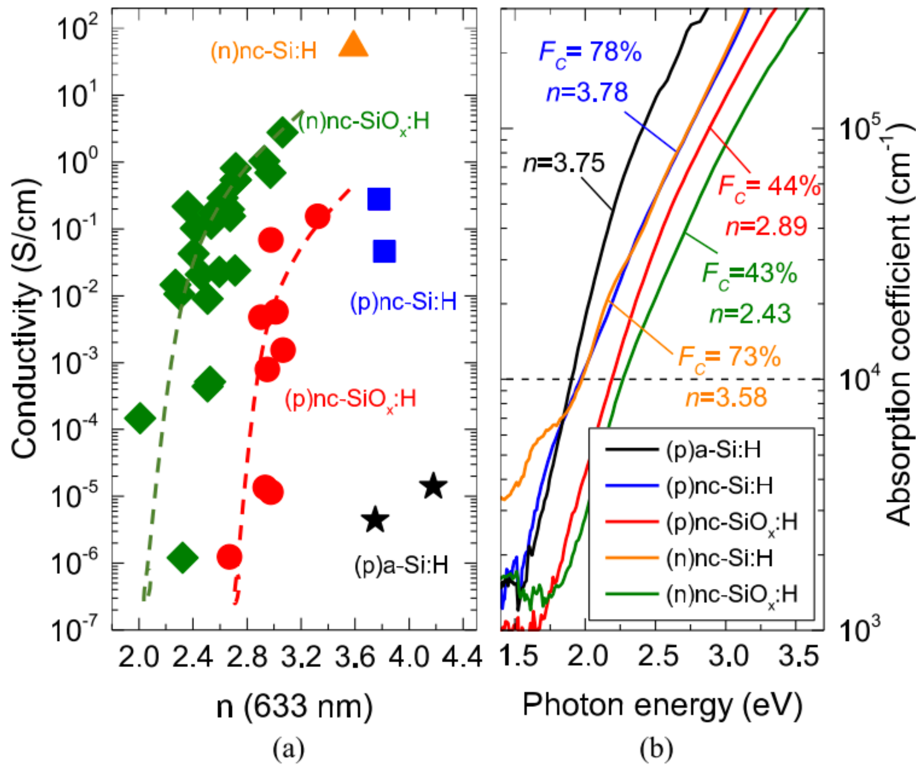


Figure 2.7 Conductivity as a function of refractive index (n) and absorption coefficient as a function of photon energy for different materials. F_C represents the crystalline fraction of the film. Adapted from [55].

2.3 Recombination and Passivation

In a real solar cell, photogenerated electrons cannot be totally collected as introduced in section 1.2. Those electrons that are excited from valence band to conduction band are not stable, thus they will eventually stabilize in empty states that have lower energy in valence band. In other words, holes (the empty states in valence band) is annihilated with electrons when they back to valence band. This process is called as recombination. As a result, this process suppresses the collection of charge carriers thus the performance of a solar cell. For crystalline silicon based solar cells,

based on where the recombination happens, recombination is divided into two main branches: Bulk Recombination and Surface Recombination. In this section, the recombination mechanisms and passivation are firstly introduced.

2.3.1 Recombination Mechanisms

The basic recombination mechanisms consist of radiative recombination, Auger recombination and Shockley-Read-Hall (SRH) Recombination. The schematic illustrations of all three types of recombination mechanisms are shown in Fig. 2.8.

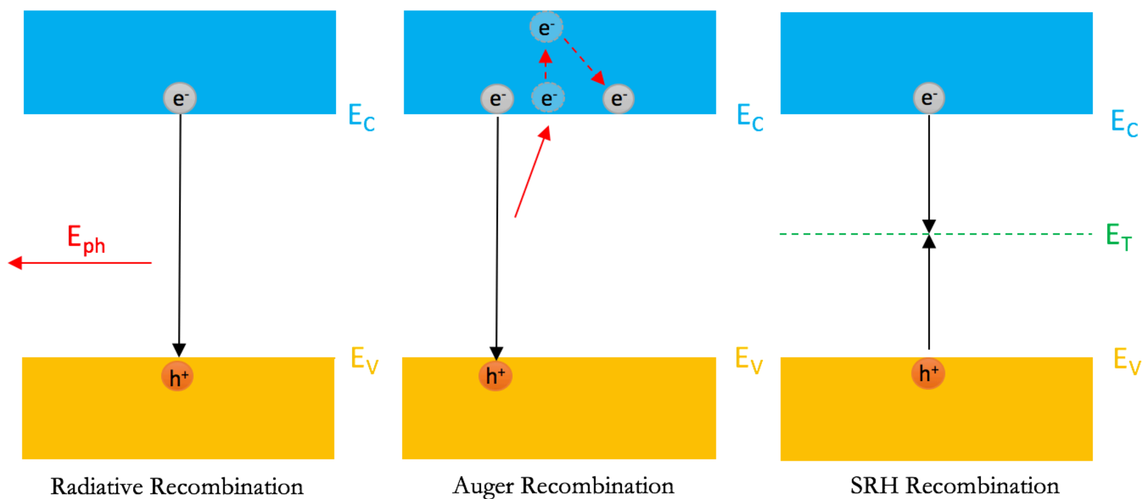


Figure 2.8 Schematic representations of three recombination mechanisms: radiative recombination, Auger recombination and SRH recombination.

In direct bandgap materials, the radiative recombination usually dominates. During the process, one electron directly falls back to valence band and recombine with a hole, meanwhile, the energy is released in a form of a photon. The photon has energy close to the bandgap of the material, so most probably it can leave the material without being absorbed again. Since c-Si is an indirect bandgap material, it is not the dominant recombination mechanism for c-Si based solar cells.

In indirect bandgap material, Auger recombination, a process involved with three carriers, is more important. When an electron recombines with a hole, energy is transferred to another electron (third particle) in conduction band. Due to excitation, the third particle comes to a higher energy level in conduction band but eventually back to the conduction band edge after thermalization. This is an electron-electron-hole (eeh) process, similar principle applies to the electron-hole-hole (ehh) process, where excited hole comes to deeper inside the valence band. In the case of solar cell, Auger recombination is more dominant when doping concentration or injection level is very high. However, under the case of CSP, Auger recombination could be also important for direct bandgap materials.

Different from above mentioned two intrinsic recombination mechanisms, the SRH recombination is an extrinsic process where recombination happens through defects. The defects are previously introduced based on the atomic structure of both c-Si and a-Si:H, i.e., the dangling bonds or doping impurities. SRH recombination is a two-step process: an electron is trapped in the defect state (E_T) exists within the forbidden gap; then before the emission of the electron back to conduction band, the hole moves to the trap state and recombine with the electron. A more detailed description of different types of SRH recombination can be found in [21]. Since the trap states can exist in different positions (either midgap or close to edge of CB or VB), the recombination rate is states level dependent. For instance, if the trap state is too close to conduction band, the trapped electron is very likely to be re-emitter back to conduction band before the hole move to the trap, eventually, the recombination rate decreases. Therefore, the midgap trap states make the most effective SRH recombination.

2.3.2 Surface Recombination

Since the excellent bulk quality of FZ process produced c-Si, the bulk recombination of c-Si can be neglected. To elaborate, assume a n-type substrate, because more trap states at the surface (disrupted lattice) than bulk material, thus less concentration of excess minority carriers holes at the surface (δp_S) than that in the bulk (δp_B). Then a gradient of excess minority carrier holes occurs near the surface, minority carrier holes diffuse from the bulk to the surface mostly recombine in this region. This process can be mathematically described as:

$$-D_p[\hat{n} \cdot \frac{d(\delta p)}{dx}]\bigg|_s = s\delta p_S \qquad (2\text{-}3)$$

where D_p is the diffusion coefficient of holes, $\hat{n}$ is the unit outward vector normal to the surface, s is the surface recombination velocity with a unit of cm/s. If δp_S is smaller, which means the surface recombination is severer and higher value of s. If the concentration gradient part $d(\delta p)/dx$ is zero, then s is zero.

2.3.3 Effective Lifetime

The lifetime of minority carriers electrons or holes is defined as the average time before electrons or holes recombine with the corresponding majority carriers. In general, the effective lifetime (τ_{eff}) is commonly used to give a predication of V_{oc} of solar cells. Since it is closely related to both bulk and surface recombination, τ_{eff} can be expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \qquad (2\text{-}4)$$

where τ_b and τ_s are the lifetime of bulk and surface, respectively. And τ_b can be expanded as:

$$\tau_b = \tau_{aug} + \tau_{rad} + \tau_{SRH} \tag{2-5}$$

In equation (2-5), τ_{aug} indicates the recombination lifetime of Auger recombination, τ_{rad} refers to that of radiative recombination and τ_{SRH} reflects the SRH recombination.

For the used FZ c-Si, τ_b is very high, then the equation (2-4) becomes:

$$\tau_{eff} \approx \tau_s \tag{2-6}$$

Therefore, the effective lifetime can directly reflect the passivation of the interface. Considering a symmetrical surface passivation of a-Si:H, then the relationship between s and τ_s can be expressed as [56]:

$$\tau_{eff} \approx \tau_s = \frac{W}{2s} + \frac{1}{D_p}(\frac{W}{\pi})^2 \tag{2-7}$$

where W is the thickness of the substrate. It is obvious from equation (2-7) that lower surface recombination velocity leads higher obtained effective lifetime. The sufficient τ_{eff} of the passivated structure is crucial to judge whether it is in the level of device quality. The effective lifetime can be directly measured by photoconductance decay (PCD) method, which will be introduced in next chapter.

2.3.4 Reverse Biased Saturation Current Density

The saturation current density (J_o) of a p-n junction that is also recombination dependent is defined as [56]:

$$J_o = qn_i{}^2(\frac{D_p}{L_pN_d} + \frac{D_n}{L_nN_a}) \tag{2-8}$$

where n_i is the intrinsic carrier concentration, q is the elementary charge, L_p, L_n are the diffusion length of holes and electrons, respectively. In the p-n junction, N_d and N_a are the corresponding minority carrier concentration. J_o describes the undesired minority carriers induced reversed current flow from electrical neutral region to the depletion region [56]. The V_{oc} of a device is also related to the J_o and can be expressed as [21]:

$$V_{oc} = \frac{K_BT}{q}ln(\frac{J_{ph}}{J_o} + 1) \tag{2-9}$$

here, K_B is Boltzmann constant, T is the temperature with the unit of Kelvin, J_{ph} is the photogenerated current. Therefore, minimum J_o is required for high-efficiency solar cell

manufacture. A well-designed p-n junction and insignificant recombination can reduce J_o to only several fA/cm^2.

2.3.5 Passivation Mechanisms

With the view to improve the passivation quality of a solar cell, the recombination either at surface or bulk of the materials should be suppressed. In general, passivation mechanisms can be grouped as two parts: chemical passivation and field-effect passivation.

As introduced in section 2.1.2, applying PECVD deposited i-a-Si:H layer on both surfaces of the c-Si substrate is expected to passivate most dangling bonds in assistance with atomic hydrogen. In this way, the dangling bonds form chemical bonding with Si and H atoms. The representation of chemical passivation of c-Si surface by i-a-Si:H layer is given in Fig. 2.9. In other cases, Si-O bonds can be also formed by thermal way [57] or wet-chemical way. The chemical passivation applied in this thesis is critical to reach high V_{OC} of the final solar cell.

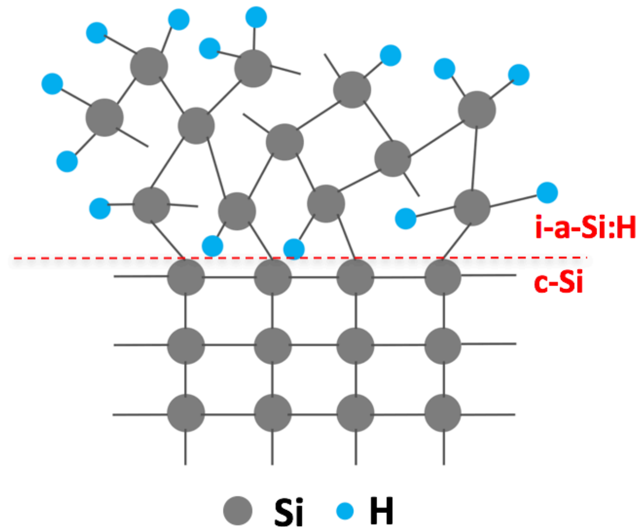


Figure 2.9 Schematic representation of chemical passivation of c-Si surface by i-a-Si:H. The red dashed line indicates the interface between c-Si and i-a-Si:H.

In addition, doped layers that can induce band bending (electric field shielding) of c-Si surface leading to reduction of one type of charge carriers, which eventually reduce the probability of recombination. This is so-called field-effect passivation. As shown in [19, Fig. 1.6], for the p-type contacts, electrons diffuse from the absorber bulk to the surface of the c-Si/p-type side are expelled away to prevent recombination. Same applied to n-type contact, where holes are repelled but electrons are collected. Materials with fixed charges like SiO_2 (positively charged) and Al_2O_3 are used for supplying the field effect. However, since they are not conductive, extra steps are needed for making contacts but sacrifice the field-effect passivation partially. Aside from this, the electric field can be also applied by doping: for homojunction, ion implantation to create the

doping profile on the edge the c-Si substrate; or for the heterojunction, well-optimized doped layers are applied. Therefore, the application of passivation contacts (doped a-Si:H or nc-SiO_x:H in this thesis) in SHJ based solar cells are necessary.

Within this thesis, the combination of chemical passivation and field-effect passivation is applied for reducing the c-Si/i-a-Si:H interface recombination and efficient selective collection of charge carriers.

3

INSTRUMENTATION OF SHJ SOLAR CELL MANUFACTURE AND CHARACTERIZATION METHODS

In this chapter, the tools and techniques that are used to manufacture and characterize the SHJ solar cells are introduced.

3.1 Manufacture Tools

During the manufacture process of SHJ solar cells, the main thin-film layer depositions are realized with Radio Frequency Plasma-Enhanced Chemical Vapor Deposition (rf-PECVD), which is for not only the intrinsic and doped amorphous silicon (a-Si:H) layers but also the doped nano-crystalline silicon oxide (nc-SiO_x:H) layers. This setup forms basic silicon heterojunction structure with passivating contacts. Afterwards, the transparent conductive oxide (TCO) deposition is achieved by Magnetron Sputtering for more efficient lateral carrier transport from passivation contacts to the collecting electrodes. Different metallization methods are applied including aluminum (Al) evaporation, Al sputtering, silver (Ag) evaporation, silver paste screen printing and copper (Cu) electroplating. Moreover, for the case of IBC-SHJ, the photolithography technique is utilized to precisely form the interdigitated back contacts.

3.1.1 Radio Frequency Plasma-Enhanced Chemical Vapor Deposition

For both passivation optimization and manufacture of solar cell device purposes, the deposition of the thin a-Si:H layers or nc-Si:H layers on both sides of the c-Si substrate is realized by using the rf-PECVD so-called AMOR or AMIGO (Elettorava, S.p.A.) in Else Kooi Lab (EKL) at Delft University of Technology. The schematic representation of a typical rf-PECVD chamber is illustrated in [58, Fig. 3.1]. Besides, the top-views of those PECVD tools are shown in Fig. 3.2, where individual deposition chambers are built to prevent cross-contamination.

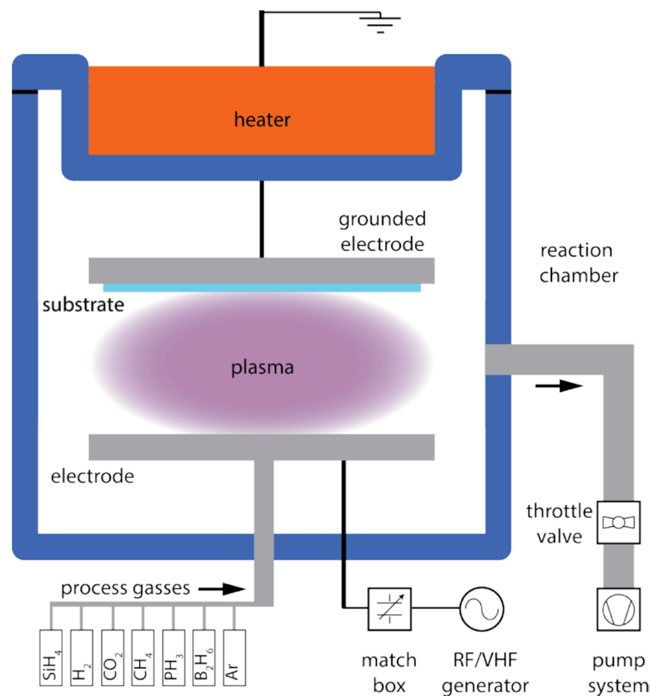


Figure 3.1 The schematic illustration of PECVD and its system compositions. Adapted from [58].

For the deposition of thin-film silicon layers, the sample (either glass or c-Si wafer) is firstly loaded into the PECVD through Loadlock Chamber (LLC). Then, the sample is transferred to specified DPC with the position shown in Fig. 3.2 and heated up to a setting temperature (in this thesis, relatively low temperature around 180°C is set). According to different deposition purposes, various precursor gases mixtures are supplied into the DPC via the bottom showerhead electrode (12×12 cm^2). For i-a-Si:H deposition, hydrogen diluted silane (SiH_4 and H_2) is applied, while dopant gases like diborane (B_2H_6) and phosphine (PH_3) are additionally supplied for depositing p-type and n-type Si thin-film layers. Oxygen and carbon are alloyed via adding carbon dioxide (CO_2) and methane (CH_4) in the chamber, respectively. After the stabilization of gas mixture to the set pressure through the pump, the precursor gases are electrical discharged by switch on the rf-generator and ignited (in the form of plasma) once the power is applied.

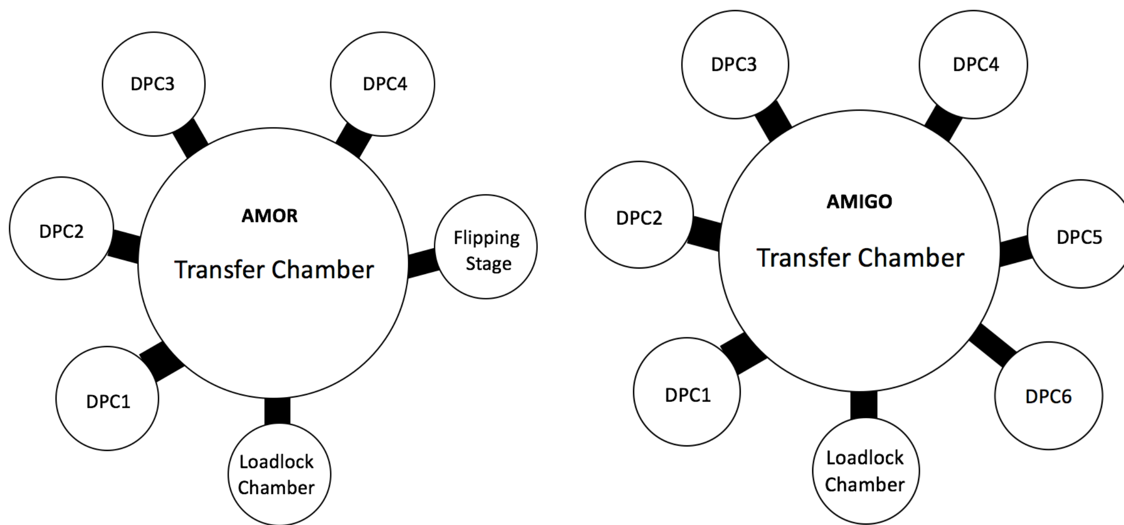


Figure 3.2 The schematic top-view of PECVD in PVMD group. AMOR (left) with four deposition chambers and AMIGO (right) with six deposition chambers. All chambers are connected to pumps to make high vacuum transfer and deposition.

The principle behind the plasma ignition is the acceleration and energization of electrons between two capacitatively coupled parallel electrodes. Those electrons with sufficient energy can dissociate the precursor gases through collisions and form reactive radicals and ions. Finally, the positive ions and radicals are attached to the surface of growing film owing to the formed plasma sheath [59].

In general, the variable deposition parameters such as pressure, power, substrate temperature, hydrogen dilution ratio and the gas flow rate can influence the quality of the deposited layers and they are highly equipment dependent [28], [37], [60]–[63]. All those parameters together can be systematical optimized for excellent properties of obtained layers.

For manufacture of FBC-SHJ solar cell in this thesis project, the DPC1 (p-type deposition) and DPC2 (n-type deposition) of both AMOR and AMIGO are used. AMOR is more specified to make amorphous silicon layers while AMIGO is used for nano-crystal silicon layers. For the thin intrinsic passivation layer (i-a-Si:H), DPC3 of both PECVD tools are optimized and applied.

3.1.2 Radio-Frequency Magnetron Sputtering

Unlike previously introduced PECVD, which involves chemical reactions in the process, radio-frequency magnetron sputtering is a physical vapor deposition (PVD) method for depositing TCO layer and metals. In this PVD method, argon (Ar), which is an inert gas, is used as highly energetic particles to bombard the target (cathode) when RF power is applied, then the target atoms can be released and diffuse to the surface of substrate or vacuum chamber (anode), subsiding eventually on the substrate after random walk. During the sputtering, the discharged electrons from emitter (target), which collide with the remaining Argon atoms to create extra ions and free electrons to

sustain the plasma. The schematic configuration of a rf-magnetron sputtering system is represented in [58, Fig. 3.3].

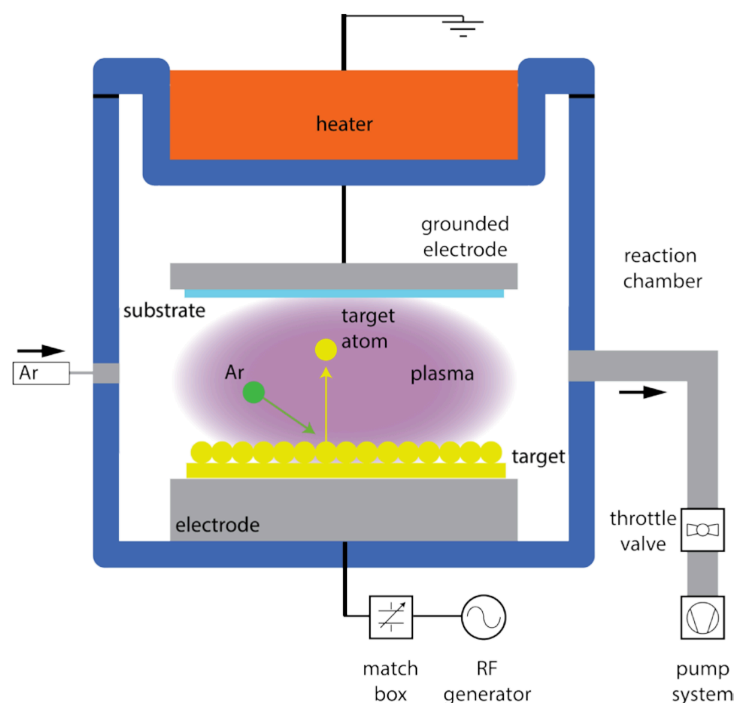


Figure 3.3 The schematic representation of a typical rf-magnetron sputtering system and its system components. Adapted from [58].

Within this thesis, two sputtering tools are used, the one (ZORRO) made by Polyteknik is used for only indium tin oxide (ITO) deposition, another one made by Kurt J. Lesker Company is used for Al sputtering for metallization. Targets that consist of certain compositions are needed for different purposes: a target with 90 wt. % In_2O and 90 wt. % SnO_2 for ITO deposition, while around 99.998% Al for Al sputtering. As reported in [64], damage is induced to the passivation after ITO deposition, a two-step deposition is applied in this thesis, which consists a low power pre-deposition forming a protective layer and then a high power main-deposition. This two-step deposition strategy aims to provide ITO with optimized contact properties and optical properties without significant damage introduction.

3.1.3 Metal Evaporation, Screen Printing and Electroplating

After preceding steps, a precursor is finally ready to be metallized. Since metal contact is one major efficiency limiting factor [29], within this thesis, diverse metallization technologies are tested: metal evaporation, screen printing and electroplating.

The working principle metal evaporation is by heating up the metallic source materials to reach above their melting points, then the metal material is evaporated and directly targeted to the

substrate in a high vacuum chamber (10^{-3} to 10^{-6} Pa to easily control the deposited thickness and the oxidation level of evaporated metals [65]). Ultimately, they condensed back to the solid state on the substrates with lower temperature. In PVMD group, Provac PRO500S is in service for metal evaporation with two different methods: electron beam evaporation and resistive (thermal) evaporation. The schematic illustration is shown below in [66, Fig. 3.4].

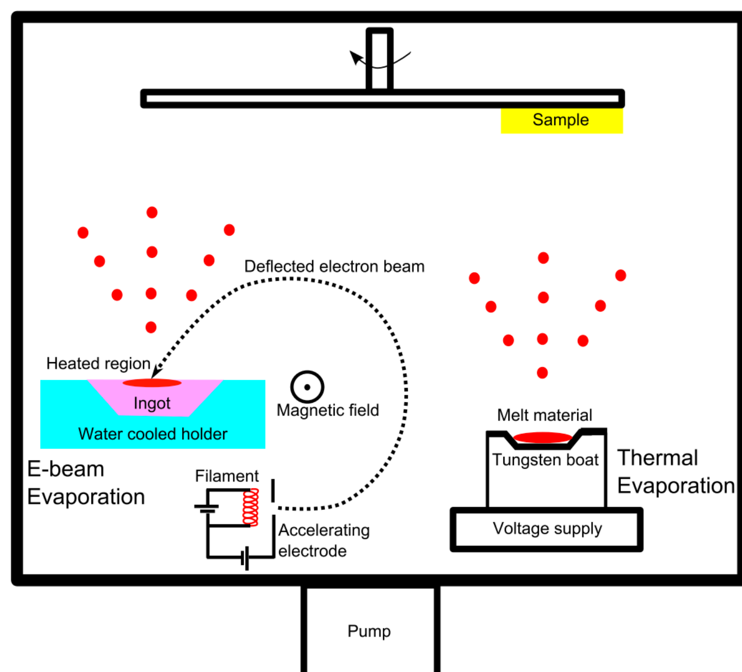


Figure 3.4 The schematic view of metal evaporation system in PVMD group. The electron beam evaporation and resistive (thermal) evaporation on the left and right side, respectively. A stage for four substrates rotates during the metal evaporation. Adapted from [66].

According to different melting points of metallic sources, the electron beam evaporation is used for metals with relatively high melting points such as chromium (Cr) (1856.85°C), where a water-cooled crucible loaded with metallic sources is bombarded and heated by intensive electron beam (emitted from a tungsten filament and directed by a strong magnetic field). While for metals with relatively low melting points like Ag (961.78°C), resistive (thermal) evaporation that apply high current to the open tungsten boat to heat up the source materials is applied. Although Al has low melting point as 660.32°C, the electron beam evaporation is applied to prevent the alloying of Al with tungsten boat.

Another more industrialized technology, screen printing (shown in [67, Fig. 3.5]), is also extensively used in this project. The working principle of screen printing is suggested by its name, where a liquid (viscous) metallic paste is swept by the squeegee on the surface of the screen and 'printed' to the substrate once meets the opening of the screen. The screen is made with an interwoven thin-wire mesh which gives openings as designed for grid patterning. The schematic

representation of the screen printing process is shown below. After forming the grid patterning on the substrate, for the case of SHJ solar cells, the contact formation is necessary to be done under 170°C for 60 min in the air. In this project, the low-temperature silver polymer based paste (produced from DuPont™) is used and it fulfills the contact formation under low temperature. A more detailed introduction about screen printing can be found in somewhere else [67].

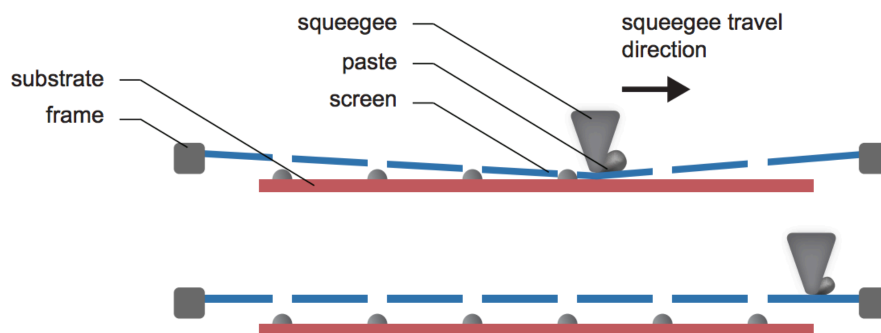


Figure 3.5 The schematic illustrations of screen printing process: during screen process (top picture), end of the process (bottom picture). Adapted from [67].

Asides from previous two metallization methods, the electroplating, in this project, copper (Cu) plating is also tested. The schematic working principle of copper plating is presented in [67, Fig. 3.6].

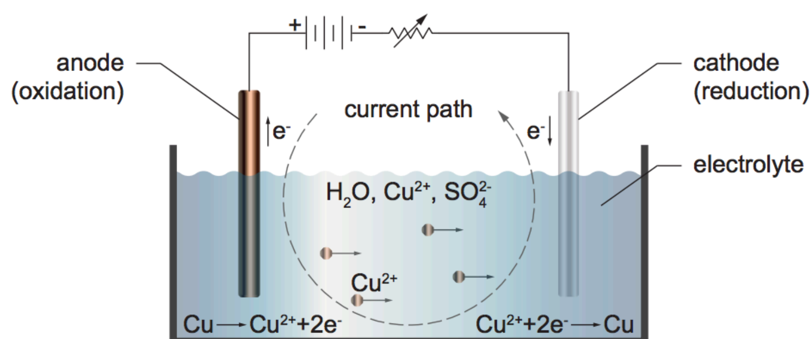


Figure 3.6 The schematic view of working principle of copper plating. The substrate (cathode) and a copper anode are immersed in copper sulphate ($CuSO_4$), where an external DC source connected to both electrodes drives the reaction. Adapted from [67].

As shown in Fig. 3.6, the Cu electroplating is based on the reduction-oxidation reaction, which functions as an electrolytic cell with two electrodes that are immersed in electrolyte. The substrate is the cathode, where the reduction reaction happens (Cu deposition). With depleting of Cu ions in the solution, extra Cu ions is supplied by the sacrifice anode that is made by the copper in this case. Cu plating is thought to be quite promising due to its cheaper price than silver meanwhile maintains an excellent conductivity (5.8×10^7 Sm^{-1}). However, it is reported that Cu can diffuse

easily and fast into Si [68] and induces defects which act as recombination centers into the silicon, degrading the overall performances of the cell eventually. In this project, the titanium (Ti) is used as a high conductivity seed layer between the copper and Si layer to form diffusion barrier of Cu and proceed the Cu plating. In this project, Cu plating is done in a MECO plating unit.

3.1.4 Photolithography

In order to have precise junction formation for the IBC-SHJ solar cells, photolithography is used due to its very narrow typical feature size (<1 μm) compared to other patterning technologies [15]. Photolithography enable UV light to transfer the geometric pattern from a photomask to the light sensitive photoresist (PR), then the exposed (positive PR) or unexposed (negative PR) is etched away by a specific etchant (developer) to form the desired pattern on the surface of substrate. Then, on the one hand, PR that left on the surface can be further used as etching barrier for wet-chemical etching or dry-etching to form the final pattern of the substrate; or on the other hand, for the metallization in SHJ-IBC solar cells, PR can be used for metal liftoff, which will be explained in Chapter 6. Since PR is an organic material, it is in general removed by acetone after the designed pattern is formed. However, if PR is exposed to plasma process such as dry-etching, another plasma tool is needed for removing the PR since it is hardened. The schematic illustration of photolithography process with positive resist is shown below in [67, Fig. 3.7].

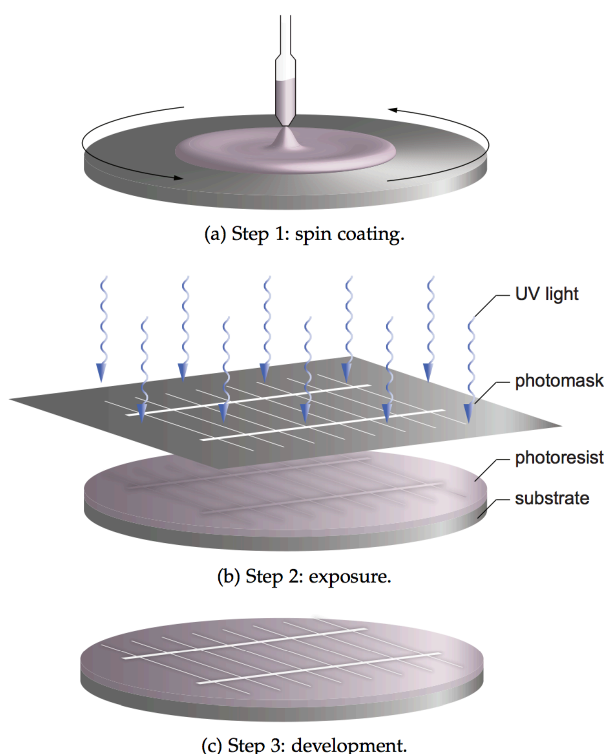


Figure 3.7 The schematic representation of working principle of photolithography with positive photoresist. Adapted from [67].

Since this process is light sensitive, the whole steps are finished in polymer lab of EKL, which is lightened with yellow light (570 - 590 nm). Either EVG 120 Coater-Developer (automatic coating) or Brewer Science Manual Spinner (manual coating) is applied for coating, then EVG 420 Contact Aligner is used for photomask alignment and UV light exposure. Lastly, the patterning of PR is formed by using developer.

3.2 Characterization Techniques

For practical cell manufacture, understanding of the deposited thin-film layers and the performance of the manufactured solar cells, several characterization techniques are usually used and they are introduced in this section.

3.2.1 Spectroscopic Ellipsometry

Precise thickness control of the deposited thin-film layers is extremely important for final device performance [64], [69], [70]. Spectroscopic Ellipsometry (SE) (J.A. Woollam Co., M-2000DI) is an optical measurement technique that measures and characterize the varied polarized light due to reflection or transmission caused by samples [71]. Then, the obtained date is fitted by a well-defined optical model, the deposited layer thickness, optical constants and other physical parameters can be obtained. Generally, it can provide highly accurate thickness data with sensitivity around 0.1 Å [71].The schematic representation of SE measurement setup is shown in [72, Fig. 3.8].

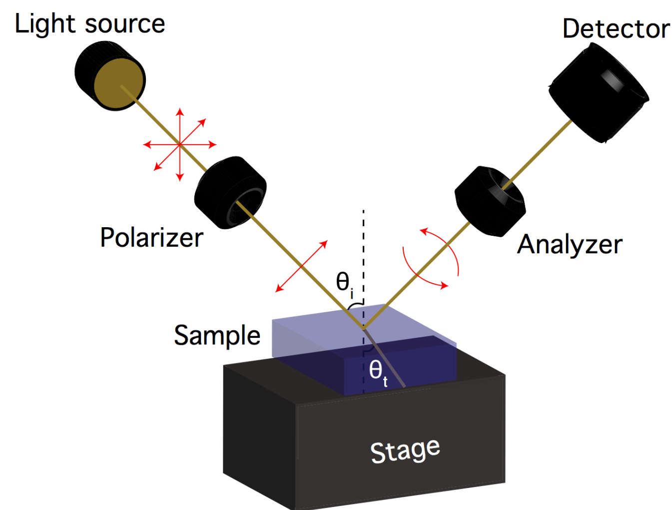


Figure 3.8 Schematic representation of SE measurement setup. Adapted from [72].

The process of characterization the samples by this ex-situ measurement are illustrated in [71, Fig. 3.9]. As shown below, there are two important measured parameters, namely, amplitude ratio (ψ) and phase difference (Δ) between p- and s- polarized light waves. Based on Fresnel equation, the complex amplitude reflection coefficients r_p and r_s are determined, which are described by angle

of incidence, transmittance and the complex refractive index. Then measured ψ and Δ are related to r_p and r_s [71]:

$$\tan(\psi)e^{i\Delta} = \frac{r_p}{r_s} \tag{3-1}$$

With assistance of the well-defined optical model, optical constants and layer thickness are obtained to further analyze the other physical characteristics. For a-Si:H layers deposited for this project, the Cody-Lorentz model is mainly used [73]. While for doped nc-SiO_x:H layers, EMA (effective medium approximation) with Bruggeman model is applied.

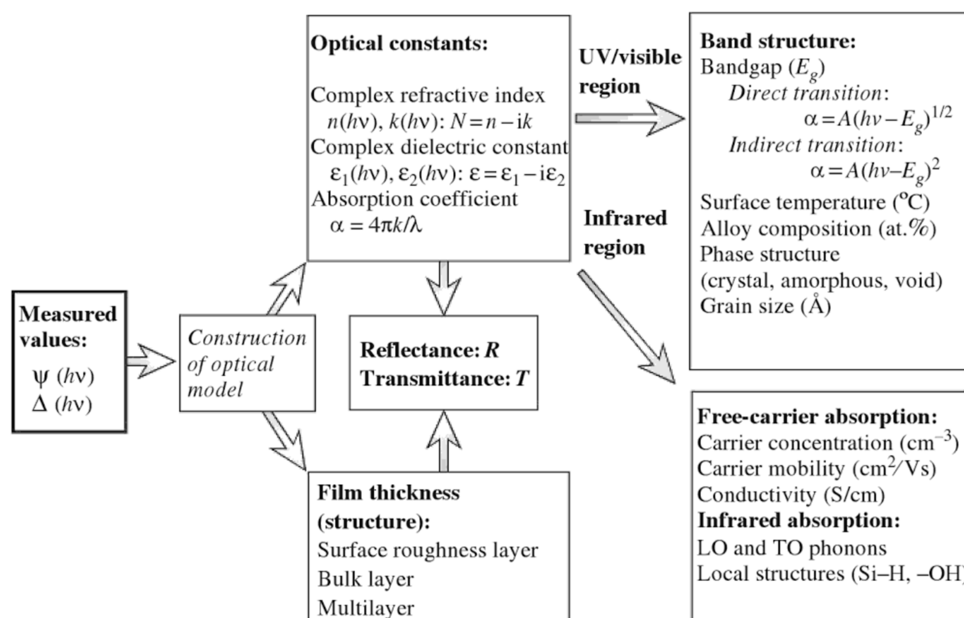


Figure 3.9 The flowchart of physical properties characterization from SE. Adapted from [71].

In this project, SE is mainly used for thickness measurement, which is related to deposition rate checking and uniformity optimization. However, one of the limitations to the measured samples is that the roughness of the surface should be as small as possible. Therefore, randomly textured wafers that are mostly used in this thesis cannot be measured by SE. The thickness measurements of the deposited layers on the substrates with flat surfaces are proceeded, namely, corning glass, glass wafer and n-type polished FZ <111> c-Si wafer. Lastly, the deposition rate on flat surface is assumed to be 1.7 times faster compared to that of textured.

3.2.2 Photoconductance Lifetime Tester

One important method that gives a hint on the quality of the deposited layers and solar cell precursors is the photoconductance lifetime tester (Sinton WCT-120). In general, the test sample and a photodiode (built-in) are placed on a stage with constant temperature. The lamp on top of

the sample flashes the light to the sample for a set short period of time (1s or 1/64s). This flash of light induces changes of photoconductance of the sample, which is induced by recombination of excess generated carriers. Meanwhile, the photoconductance changes are sensed by a coil that is inductively coupled to the RF bridge. Eventually, with analysis of those changes, the data such as lifetime (τ_{eff}), implied open-circuit voltage (iV_{oc}) and revers-biased saturation current (J_o) can be obtained [74]. The schematic representation of Sinton WCT-120 is shown in [72, Fig. 3.10].

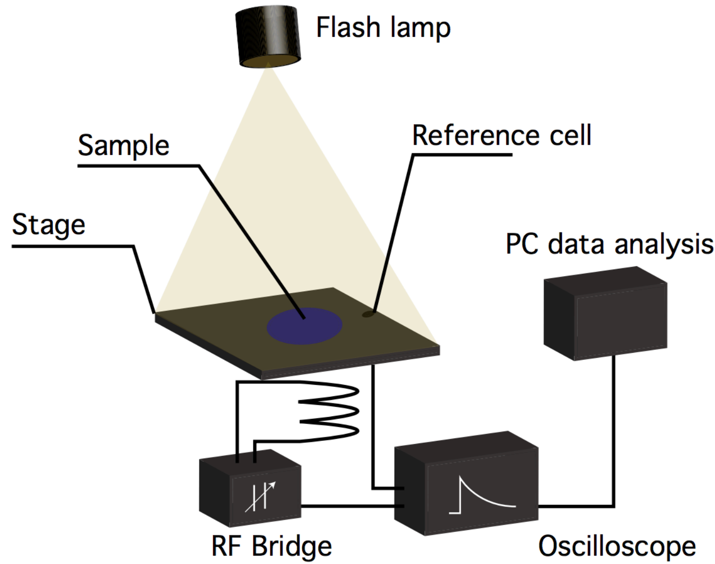


Figure 3.10 Schematic representation of Sinton WCT-120. Adapted from [72].

For a n-type substrate, the measured photoconductance is related to the excess minority carrier density:

$$\sigma_L = q\Delta p(\mu_n + \mu_p)W \tag{3-2}$$

where Δp is the excess carrier density, μ_n and μ_p are mobility for electrons and holes, respectively. Then from change of photoconductance, Δp is acquired. In general, there are two modes for analysis, one is quasi-steady-state-photoconductance (QSSPC) mode, another one is transient photoconductance decay (Transient PCD) mode. For sample with a τ_{eff} < 100 µs, the quasi-steady-state mode is recommended, while for τ_{eff} > 200 µs, the transient PCD is used which has a shorter light-pulse time. Based on continuity equation, the mathematical expression of τ_{eff} acquired from these two modes can be rearranged as:

$$\tau_{eff} = \frac{\Delta p}{G - \frac{\partial \Delta p}{\partial t}} \tag{3-3}$$

where, G is the carrier generation rate and it is calculated from the photodiode. For QSSPC mode, $\partial\Delta p/\partial t$ is neglected because $G \gg \partial\Delta p/\partial t$ and for transient PCD mode, G is almost zero.

The τ_{eff} is shown as a function of minority carrier density (MCD), an example of lifetime curve is shown below. Typically, the τ_{eff} is read at a (MCD) of 10^{15} cm^{-3} because the recombination at a-Si:H (i)/c-Si interface rather than the bulk recombination is more interested to be investigated. Reasons for this MCD are [66]: a). At this level of MCD, the recombination velocity is less influenced by the Auger recombination and radiative recombination, which gives more hint on the defects; b). It has a similar value compared to the injection level under one-sun condition. Aside from the MCD of 10^{15} cm^{-3}, the entire lifetime curve it is generally thought to provide some hints on the dominant recombination. At low injection level (MCD < 10^{15} cm^{-3}), the Shcokley-Read Hall (SRH) recombination is more dominant; while at high injection level (MCD > 10^{15} cm^{-3}), auger recombination is more pronounced [75]. This can be also observed from the simulated effective lifetime curve shown below [48, Fig. 3.11].

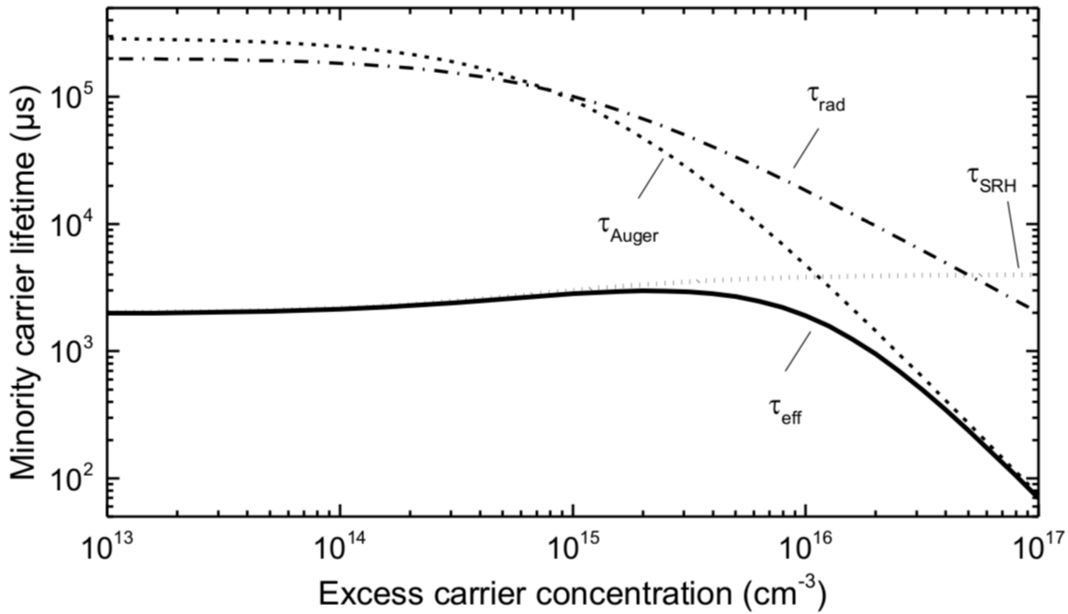


Figure 3.11 An example of simulated recombination lifetime as a function of excess minority carrier density (Δn). Adapted from [48].

Implied V_{oc} is different from the previously mentioned device V_{oc}, but the former is often the upper limit of the latter. The implied V_{oc} only describes the current structure and is calculated based on minority carrier density:

$$iV_{oc} = \frac{K_B T}{q} \ln\left(\frac{\Delta p(N_D + \Delta p)}{n_i^2}\right) \quad (3\text{-}4)$$

where N_D is the concentrations of donors. Then the iV_{oc} is represented as a function of light intensity.

In this thesis, lifetime measurement is extensively used firstly for the passivation optimization, which provides most promising passivation layers for fabricating devices; secondly, it is also used to trace the manufacture process induced damages, such as wet-chemical etch and ITO sputtering; lastly, the obtained entire lifetime curve is analyzed for checking the working status doped passivation layers.

3.2.3 Dark Conductivity and Activation Energy Measurement

The tunneling recombination junction formed between emitter (p-type layer) and TCO is reported as one important limiting factor of device final FF [53]. In general, high tunneling probability (better collection) of minority carriers (holes in this case) over this tunneling recombination junction requires highly doped emitter to narrow the space charge region, if we assume the work function (WF) of TCO is fixed. In the case of poorly doped emitter, the distorted 'S'-shaped J-V curve is observed [76]. Activation energy (E_{act}), which is defined as the energy difference between Fermi Level (E_F) and valence band (E_V) for p-type material, reflects the doping efficiency of the material and further influences the tunneling probability (detailed explanation can be found in section 5.2.3). Therefore, measuring E_{act} of our optimized layers are necessary for analyzing the device performances.

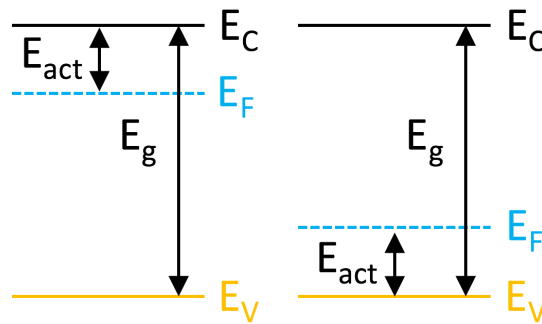


Figure 3.12 The schematic illustration of definition of activation energy of a n-type and p-type materials on the left and right, respectively.

Along with the acquiring of E_{act}, the dark conductivity (σ_d) is firstly measured. The dark conductivity of a semiconductor is expressed as:

$$\sigma_d = q(n\mu_n + p\mu_p) \tag{3-5}$$

where q is the elementary charge; p and n are density of holes and electrons under thermal equilibrium, respectively; μ_p is mobility of holes, while μ_n is electrons' mobility. It is known that the hole and electron density is Fermi Level (E_F) dependent:

For holes:
$$p = N_V \exp\left(\frac{E_V - E_F}{K_B T}\right) \tag{3-6}$$

For electrons:
$$n = N_C \exp\left(\frac{E_F - E_C}{K_B T}\right) \tag{3-7}$$

where N_V and N_C are corresponded to effective density of states at valence band and conduction band, respectively. It is apparent that σ_d is temperature dependent, i.e., for a series of substrate temperature, a series of corresponded σ_d can be measured. The σ_d under a certain temperature is determined by:

$$\sigma_d(T) = \frac{dI}{tlV} \tag{3-8}$$

where d is the distance between electrodes, I and V are the measured current and applied voltage, respectively; t is deposited thickness of the layer, l is the length of electrodes. Then based on the obtained $\sigma_d(T)$ for a range of temperature, the activation energy can be obtained through:

$$\sigma_d(T) = \sigma_o exp\left(-\frac{E_{act}}{K_B T}\right) \tag{3-9}$$

where σ_o is the pre-exponential factor. In order to obtain E_{act}, a curve of $\ln(1/\sigma_d(T))$ over $1/K_B T$ is drawn, then the slope of the fitted straight line indicates the E_{act}. An example is shown below in Fig. 3.13.

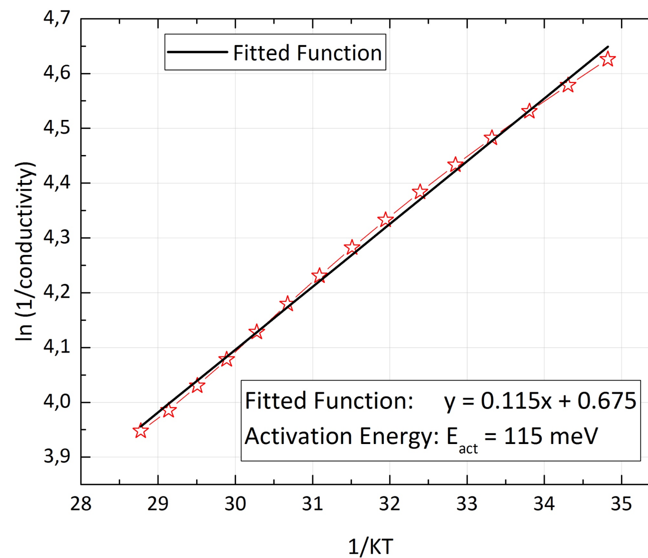


Figure 3.13 An example of activation energy calculation that are based on measured dark conductivity under different substrate temperature.

In this project, samples are prepared by depositing doped layers on the corning glasses, then evaporating Al through a hard mask which enables forming coplanar shaped contacts. Before the measurement, a low temperature annealing under 130°C for 30 minutes is done in air for forming better contacts between doped layers and Al contact.

3.2.4 Current-Voltage Measurement

Improving of the external parameters of a solar cell is always one of the main goals for the researchers. In this project, the manufactured solar cells are tested with a AAA class Wacom WXS-156S-L2 solar simulator. The test is done under standard test conditions (STC), which is characterized by an irradiance of 1000 W/m^2, a AM 1.5 spectrum and solar cell temperature of 25°C. As shown in [72, Fig. 3.14], the AM 1.5 spectrum is simulated by a halogen lamp and a Xe-lamp. Eventually, the current-voltage characteristic (J-V curve) is extracted.

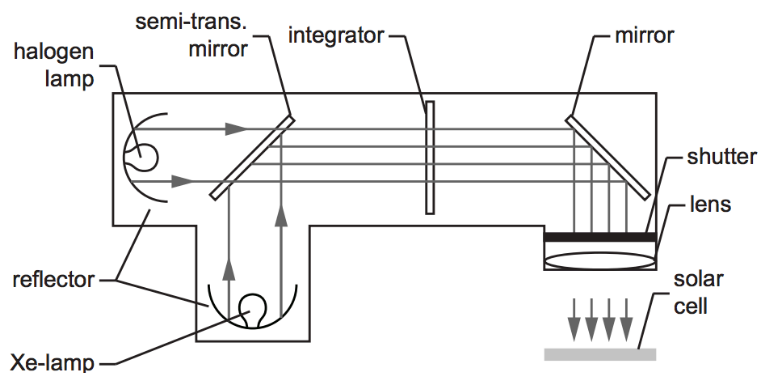


Figure 3.14 The schematic illustration of current-voltage measurement setup. Adapted from [72].

Before the measurement of our own manufactured devices, two reference solar cells are used for calibration. The extracted J-V curve is presented in Fig. 3.15, where the V_{OC} is the open-circuit voltage, J_{SC} is the short-circuit current, MPP stands for maximum power point. Aside from above mentioned parameters, the slope on the J_{SC} side represents the shunt resistance (R_{SH}) of the device, while the slope of the V_{OC} side indicates the series resistance (R_S). Both two resistances can influence the FF. In this project, the R_{SH} is generally high enough to make almost no shunt happens inside the cell, while most cells that are have limited FFs are basically according to high R_S of the devices. The detailed analysis is introduced in Chapter 5.

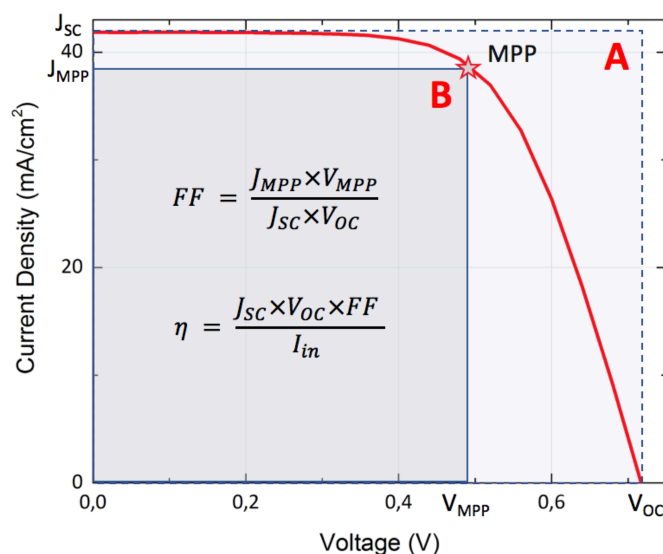


Figure 3.15 An example of measured J-V curve with definition of fill factor and efficiency.

3.2.5 SunsVoc

The J_{SC} measured from Wacom is then used as an input for the SunsVoc measurement. Since only voltage is measured, SunsVoc setup uses a flash lamp with a slow decay to provide a pseudo I-V curve that has no influence from the series resistance. The obtained SunsVoc is a function of illumination level, which gives a hint of the upper limit of Voc that can be measured from Wacom, also is reported to indicate the surface passivation under low illumination condition (< 1 sun) and the contact properties (e.g., a-Si:H(p)/ITO) that are involved in the carrier extraction [77]. Another important parameter is so called pseudo fill factor (pFF), which is normally used to compare with the FF obtained from Wacom. In this way, a clue about the R_S induced FF loss can be implied. The Sinton Suns-Voc-150 ILLUMINATION-VOLTAGE TESTER is used for SunsVoc measurement. In general, SunsVoc of a FBC-SHJ solar cell is measured before (with ITO) and after the metallization.

3.2.6 External Quantum Efficiency

As introduced previously in the working principle of a solar cell, the incident photons must with energy exceeding the band gap of the absorber material, the electron-hole pair can be generated. Then the fraction of photons that incident on the solar cell over the successfully collected electrons and holes is of great interest to us. This fraction is known as external quantum efficiency (EQE), which reflects both optical and electrical losses within the solar cell. Therefore, EQE is defined as:

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\Psi_{ph,\lambda}} \quad (3\text{-}10)$$

where $I_{ph}(\lambda)$ is the photocurrent, $\Psi_{ph,\lambda}$ is the spectral photon flow incident on the solar cell.

In this thesis, a home-built EQE measurement system (spectral response setup) is used. The light emits from a halogen lamp has a spectrum over a wide range of wavelengths, however, since EQE is wavelength dependent, the cell must be illuminated and measured with monochromatic light. Therefore, a monochromator is used to filter the light. Before the light pass through the monochromator, it firstly chopped by an optical chopper, where a chopper is for obtaining periodic signal for a lock-in amplifier. The input signal for the lock-in amplifier is current converted voltage, then signals out from the amplifier is used as final EQE results.

Since $\Psi_{ph,\lambda}$ is not directly measurable, a calibrated photodiode with known EQE is utilized for determining the $\Psi_{ph,\lambda}$ based on:

$$\Psi_{ph,\lambda} = \frac{I_{ph}^{ref}(\lambda)}{qEQE^{ref}(\lambda)} \quad (3\text{-}11)$$

where $EQE^{ref}(\lambda)$ is known, $I_{ph}^{ref}(\lambda)$ is easy measureable, then the $\Psi_{ph,\lambda}$ is determined, which finally can be input for the EQE measurement of the actual sample. After obtaining the $EQE(\lambda)$ for sample, the J_{SC} is determined through:

$$J_{SC} = -q\int_{\lambda_1}^{\lambda_2} EQE(\lambda)\phi_{ph,\lambda}^{AM1.5}\, d\lambda \quad (3\text{-}12)$$

where $\phi_{ph,\lambda}^{AM1.5}$ is the spectral photon flux and it equals to:

$$\phi_{ph,\lambda}^{AM1.5} = \frac{P_{ph,\lambda}^{AM\,1.5}\lambda}{hc} \quad (3\text{-}13)$$

where h is Planck constant, c is the speed of light in vacuum, $P_{ph,\lambda}^{AM\ 1.5}$ is the power density. For SHJ solar cells manufactured in this project, the interesting wavelength range to be investigated is between 300 nm to 1200 nm. This is due to spectral power density of wavelength below 300 nm of AM 1.5 is almost negligible, while 1200 nm is limited by the bandgap of the c-Si absorber.

Since EQE measured also includes the reflectance losses, the total reflectance of the cell is measured for obtaining the Internal Quantum Efficiency (IQE). IQE indicates the ratio of charge carriers that are finally collected to photons that are absorbed by the cell, i.e., the ability to utilize the absorbed photons. This benefits the analysis of front layer stack induced parasitic absorption. IQE is then determined by:

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)} \tag{3-14}$$

where $R(\lambda)$ is the reflectance for wavelength λ, so $1 - R(\lambda)$ means the effective absorbance if the rear side of solar cell is opaque. The $R(\lambda)$ within the interested range is measured by Lambda.

4

Optimization of Hydrogenated Intrinsic Amorphous Silicon and Doped Silicon Layers

In this chapter, the optimizations of both intrinsic and doped silicon layers are conducted. The optimization approach is mainly based on understanding the relation between deposition parameters and optimize according to passivation and uniformity for i-a-Si:H, while activation energy and band gap for doped silicon layers. Besides, the passivation qualities of doped silicon layers on top of i-a-Si:H layers are also investigated.

4.1 Optimization of Hydrogenated Intrinsic Amorphous Silicon

As explained in Chapter 2, the high quality i-a-Si:H thin layer is critical for providing not only the excellent chemical passivation on the a-Si:H/c-Si interface, but also the superior bulk quality itself. Therefore, optimization of i-a-Si:H is firstly studied. The structure of this section consists of pre-deposition, deposition, characterization and analysis. Since pre-deposition is the first step of either passivation test or manufacture of solar cells, it is explained in detail and applies for following two chapters as well. An overview of the process is demonstrated in Fig.4.1.

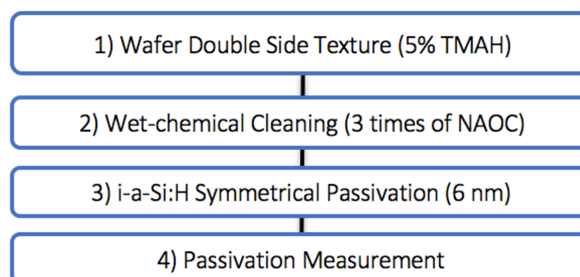


Figure 4.1 The overview of process flow of i-a-Si:H layer optimization.

4.1.1 Pre-deposition

Wafers used for passivation optimization are Topsil n-type double-side polished FZ <100> c-Si wafers with a range of resistivity (3$\pm$2 Ω·cm) and thickness (280$\pm$20 μm).

Wafer texturing

According to a faster etching rate of orientation <100> compared to that of <111>, the surface after etching is exposed as <111> textured random upright-pyramid like crystalline plane. This is so-called anisotropic etching. The sizes of those pyramids are around several microns (0.5 μm to 2.1 μm reported from [78]) . Owing to those random pyramids, the light incident on the surface of those pyramids can partially transmitted into the inner structure and partially reflected to other pyramids' surfaces then being coupled into the wafer again. Thus, less reflection loss and enhanced absorption is achieved. Besides, the light that scattered on the pyramids' facets also prolong the optical path of light in the wafer.

In this thesis, textured is realized by dipping wafers in the hot (75 $\pm$ 2°C) alkaline etching solution 5% tetramethylammonium hydroxide (TMAH, $(CH_3)_4NOH$) for 20 minutes. The texture solution is a mixture of 1L 25% TMAH (SIGMA-ALDRICH), 120 ml ALKA-TEX.8 (ISRA) and 4L deionized water (DI water). ALKA-TEX.8 is used for reducing the texture time and extending the lifetime of the etching bath.

Wet-chemical Wafer Cleaning

Contamination-free and low defect density c-Si substrate is required for better passivation performance. After texture, the defect density increases according to large surface and possibly contamination compared to planar one. Therefore, there are three main purposes for the wafer cleaning: a). Remove the impurities or any other contaminants such as organics and metals left from the texturing process; b). Smooth the texturing process induced nano-roughness which is the structure irregularities; The nano-roughness, which is an extended layer with several Å of length, contributes to stretched and dangling bonds; c). Partially passivate or so-called H-termination the dangling bonds at c-Si surface avoid formation of oxidants during the transport to rf-PECVD system.

In this thesis, the wet-chemical oxidation then followed by hydrofluoric dip (HF) are repeated several times for wafer cleaning. The method for cleaning is called as NAOC (Nitric acid oxidation cycle). During the cleaning, the as-textured wafers are firstly immersed into the concentrated HNO_3 (99%) at room temperature for 10 mins to remove organic contaminants. Then rinsed with DI water for around 5 mins. Afterwards, those wafers are put into the 69.5% HNO_3 at temperature of 110 $\pm$ 5 °C for 10 mins to clean metal contaminants. Again, 5 mins of DI water rinsing is applied. Lastly, the formed oxide layer and former existed native oxide are both removed away by Marangoni (0.55% HF) process and the dangling bonds are partially passivated. In total, the

complete NAOC cycle is repeated for three times (suggested from [72], [78]). Besides, the time that wafer is immersed in 0.55% HF solution should be not too short nor too long, which can left with oxidants or increase surface roughness, respectively [66]. Therefore, 5 minutes of HF dip is conducted as the standard procedure.

Lastly, in order to avoid the re-oxidation after the last HF dip in NAOC cleaning, the time interval between wafers out of the Marangoni and load into the vacuum chamber should be as short as possible. In general, the time is kept within 5 minutes.

4.1.2 Deposition of i-a-Si:H

The variable parameters for rf-PECVD are commonly the pressure, power, substrate temperature and hydrogen dilution ratio (H_2/SiH_4). It is essential to understand the influence on the properties of deposited a-Si:H film caused by different parameters. The review of literature is firstly given below.

Review of Deposition Parameters

According to pressure, as previously mentioned, the free mean path of the radicals before collisions are dependent on pressure. When the pressure is high, higher possibility for happening of collisions, thus less influence from so-called ion bombardment effect and feasible for high mobility radicals SiH_3 [60], [61]. In contrast, lower pressure leads to higher self-induced voltage, thus the ion bombardment effect is stronger and more defects are induced [62].

The rf power is closely related to the dissociation of SiH_4 molecules and deposition rate of the a-Si:H. In general, higher deposition rate is induced by higher rf power according higher dissociation of the gas molecules. As reported in [61], for relatively low power (< 11 mW/cm^2 for 130 °C and < 32 mW/cm^2 for 180 °C), the epitaxial growth that leads to worse passivation is prone to happen due to lower ion bombardment. However, the passivation get worse with the increasing of rf power as well, this is mainly due to a). the plasma damage to the c-Si substrate is enhanced; b). higher defect density induced by severer ion bombardment. The optimal power is exactly the phase transition between a-Si:H and μc-Si:H [61]. It is also reported that higher power leads to higher proportion of SiH_2 in plasma [60], which is a radical with high sticking coefficient (around 0.9) and leads to poor passivation quality of deposited films.

Considering the substrate temperature, with assistance of FTIR, lower substrate temperature leads to higher hydrogen content in the structure, however, it is caused by higher fraction of DHs than MHs, which means higher defect density. Therefore, poor passivation is observed under low deposition temperature [28]. However, once substrate temperature it too high, according to the breaking of weak Si-H bonds or so-called hydrogen effusion effect, more dangling bonds appear again [63]. Besides, the epitaxial growth is likely to happen under high temperature with high

hydrogen content, thus enhanced ion bombardment induced from high power is necessary to produce a-Si:H rather than μc-Si:H [61].

Hydrogen dilution ratio DR, which is defined as the ratio of flow rate of H_2 to that of SiH_4, is a critical parameter to influence the passivating performance. Moderate higher hydrogen dilution ratio can break the weak Si-Si bonds and form the Si-Si bonds, which is less defective [79]. However, too High dilution ratio tends to enhance the transition from a-Si:H to μc-Si:H, i.e., the happening of epitaxial growth, which is detrimental to the passivation [37]. Meanwhile, hydrogen plasma etching could happen when the hydrogen content is too high [80]. As reported [37], higher dilution ratio leads to less hydrogen content or narrower bandgap of the deposited layer. This is due to less DHs in the network. In the optimized condition, the MHs are dominant in the structure. Optimal hydrogen dilution ratio is found to be different from different research groups, this means it is highly dependent on the equipment and process [37]. In addition, the a-Si:H grows under hydrogen diluted silane is more stable than that of undiluted silane [81].

All these parameters together can be systematically optimized to get excellent passivation of i-a-Si:H/c-Si interface.

Deposition Parameters

Based on the principle of single variable, different combinations of parameters are designed to investigate pressure, power, substrate temperature and hydrogen dilution ratio induced influences. Depositions in this section are conducted in AMOR. The deposition rates on textured wafers are based on thickness measurement on glasses depositions. All samples are aimed to be symmetrically passivated by 6 nm i-a-Si:H. The main parameters with the corresponding variation are listed in Table 4.1.

Table 4.1 The variations of main parameters of rf-PECVD.

Parameters	Variations	Units
Substrate Temperature	140 to 200	°C
Dilution Ratio	0 to 5	-
Power	1.8 to 6.7	W
Pressure	0.7 to 3.7	mbar

4.1.3 Analysis of Passivation Results

As reported in [82], the passivation quality varies obviously with the thickness of deposited a-Si:H layer when it is thinner than 10 nm. However, since the non-uniformity of the deposited layers in

the study of substrate temperature and dilution ratio, the difference of passivation quality is attributed not only from the deposition conditions but also the thickness of the deposited layers. According to the insufficient accuracy, the study of substrate temperature and dilution ratio can only give a general trend. After this, the uniformity optimization is conducted (next section). Then based on uniformity optimization, the pressure and power induced influences are studied.

Effect of Substrate Temperature and Dilution Ratio

The deposition parameters are listed in Table 4.2. Although two variables are shown in the table, for each substrate temperature, a complete range of dilution ratio experiments are conducted.

Table 4.2 Process parameters for deposition during investigation of temperature effect.

Layers	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	Dilution Ratio (-)	Flow rate (sccm)	Frequency (MHz)
i-a-Si:H	140-200	0.7	2.7	0-3	40	13.56

The measured τ_{eff} and iV_{oc} as a function of temperature are plotted below in Fig. 4.2. When dilution ratio equals to 3 and under 140°C, the plasma is hardly to be ignited. Same problem occurs when the dilution ratio goes up than 3. Possible reasons behind this could be the impropriate initial conditions such as power and pressure. Therefore, this point is not presented.

As shown in Fig. 4.2, except from the case of dilution ratio equals to 0, all other dilution ratio series show an optimized temperature at 180°C, or highest lifetime obtained. To elaborate, the τ_{eff} increases from below 200 μs to over 600 μs (dilution ratio equals to 0.5 and 1) or even beyond 1200 μs (dilution ratio equals to 3) till temperature up to 180 °C. Further, the τ_{eff} decreases when temperature is up to 200 °C, especially a sharp decrement (over 1000 μs) is observed for dilution ratio equals to 3. The trends of measured iV_{OC} are well corresponded to that of τ_{eff}, which means it is safe to conclude the measured iV_{OC} can be used to reflect the chemical passivation quality.

For the case of zero dilution ratio, the increase of τ_{eff} in 200 °C compared to that of 180 °C might be cause by: a). non-uniformity induced thicker layer than other samples; b). the experimental error caused by wafer difference (not from the same wafer) and cleaning (not cleaned at the same batch).

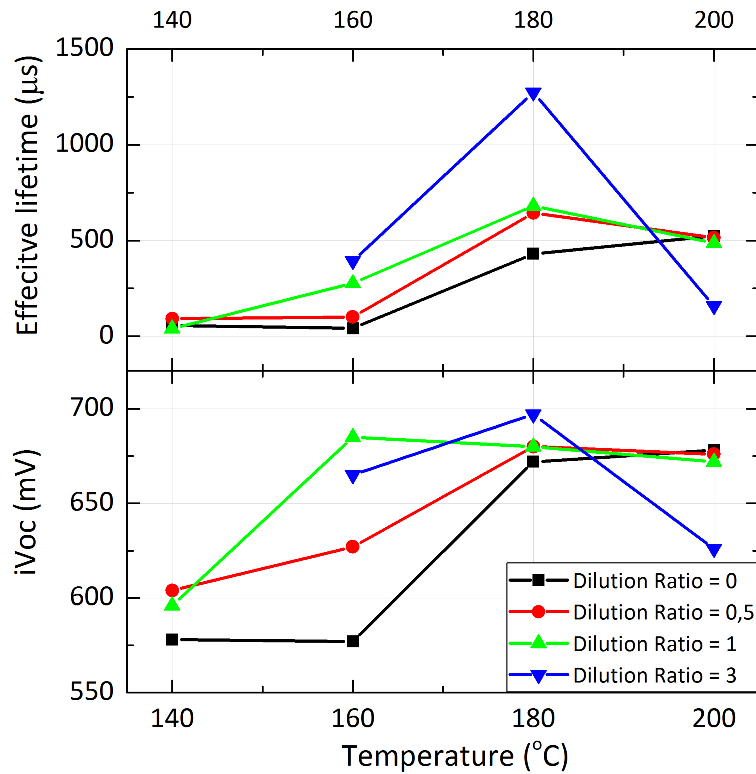


Figure 4.2 The effective lifetime and implied open-circuit voltage as functions of increasing temperature under different dilution ratio series.

In conclusion, the optimized temperature is chosen as 180 °C and the dilution ratio is chosen as 3 for the following optimization of deposition power and pressure.

Effect of Deposition Pressure

In this section, the effect of deposition pressure is studied. The deposition conditions are presented below in Table 4.3. Three power series are used to investigate the pressure induced influence. The τ_{eff} and iV_{oc} dependence on the increasing pressure under different power series is shown below in Fig. 4.3.

Table 4.3 Process parameters for deposition during investigation of deposition pressure.

Layers	Dilution Ratio (-)	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	Flow rate (sccm)	Frequency (MHz)
i-a-Si:H	3	180	0.9-2.3	2.0-2.7	40	13.56

As illustrated in Fig. 4.3, three power series can be divided into two groups. For cases with deposition power of 2.0 W and 2.3 W, optimized passivation quality occurs when the pressure reaches 0.9 mbar. Further, when pressure is increased to 1.1 mbar, the τ_{eff} drops for both 2.0 W

(from 3135 μs to 2631 μs) and 2.3 W (from 3250 μs to 2601 μs). Further drop of lifetime when pressure exceed 1.4 mbar can be found in the case of 2.0 W. According to the second power group (implied power equals to 2.7 W), a higher value of optimized pressure (1.4 mbar) is obtained.

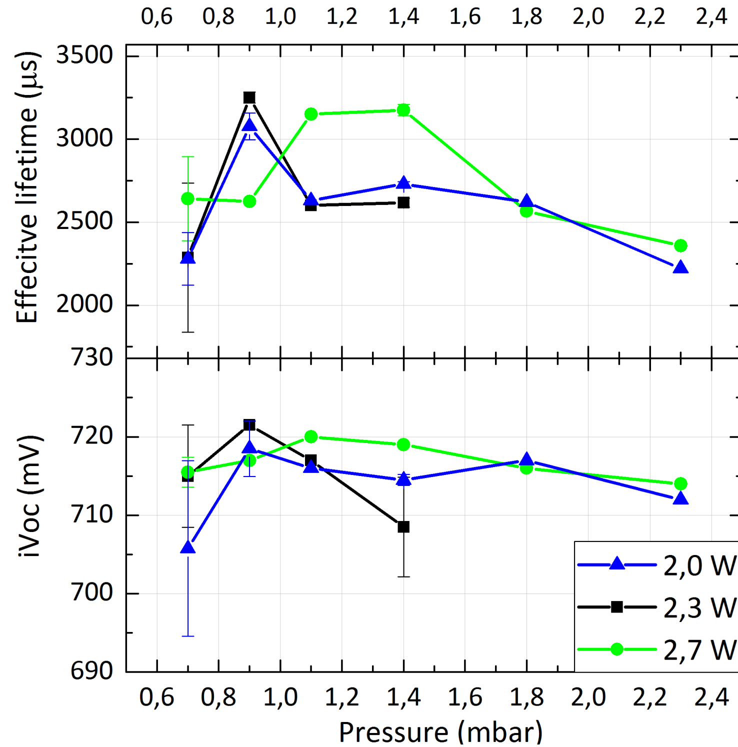


Figure 4.3 The effective lifetime and implied open-circuit voltage as functions of increasing pressure under different power series.

To sum up, at those optimized conditions based on τ_{eff}, namely, 2.0 W and 2.3 W under 0.9 mbar, 2.7 W under 1.4 mbar, the corresponded values of iV_{oc} are 721 mV, 722 mV and 719 mV, respectively; and the values of J_o are 5 fA/cm^2, 5.5 fA/cm^2 and 6 fA/cm^2, respectively.

Effect of Deposition Power

Lastly, the optimization of deposition power is studied. The deposition conditions are presented below in Table 4.4. Three power series are used to investigate the pressure induced influence.

Table 4.4 Process parameters for deposition during investigation of deposition power.

Layers	Dilution Ratio (-)	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	Flow rate (sccm)	Frequency (MHz)
i-a-Si:H	3	180	0.9-1.4	2.0-5.7	40	13.56

The measured τ_{eff}, iV_{oc} and J_o dependence on the increasing power under different pressure series is shown below in Fig. 4.4.

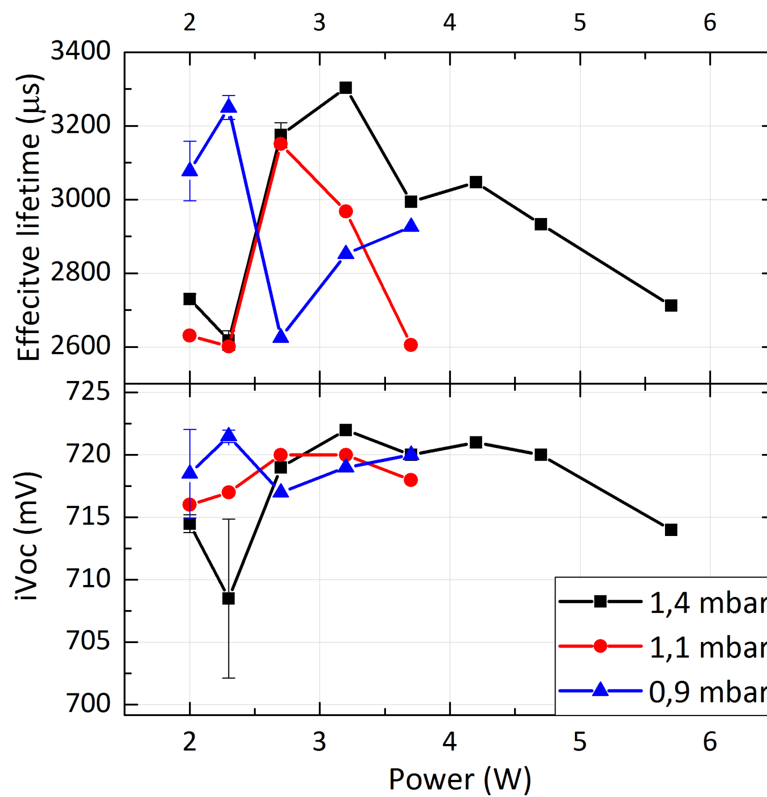


Figure 4.4 The effective lifetime and implied open-circuit voltage as functions of increasing power under different pressure series.

It is revealed in Fig 4.4 that the optimized deposition power under different deposition pressure is different. Those optimized conditions based on τ_{eff} are, namely, 0.9 mbar under 2.3 W, 1.1 mbar under 2.7 W, 1.4 mbar under 3.2 W, the corresponded values of iV_{oc} are 722 mV, 720 mV and 722 mV, respectively; and the corresponded values of J_o is 5.5 fA/cm^2 for all cases.

Above mentioned three optimized power and pressure sets are drawn below in Fig. 4.5. It indicates the systematical change of deposition power and pressure can provide the optimized passivation quality, that is, higher power is corresponded to a higher value of optimized pressure.

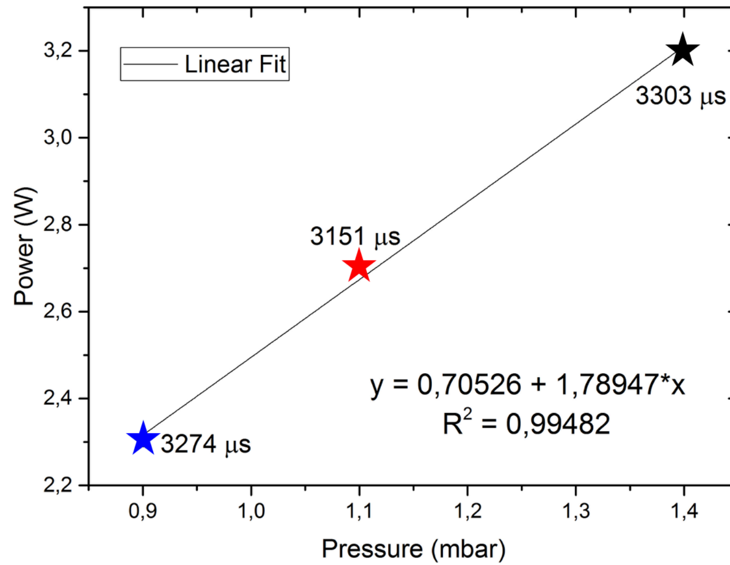


Figure 4.5 Fitting curve of three sets of optimized pressure and power.

In conclusion, for a total flow of 40 sccm, the optimized depositions substrate temperature is 180 °C with a dilution ratio of 3. Three sets of the pressure and power values can obtain similar excellent passivation results, namely, 0.9 mbar under 2.3 W, 1.1 mbar under 2.7 W, 1.4 mbar under 3.2 W.

4.1.4 Analysis of Uniformity Results

According to [82] and non-uniformity of depositions in previous substrate temperature and dilution ratio section, the non-uniform distributed layers' thickness set up obstacles for investigation of the passivation quality. Besides, uniform distributed layers build the fundamentals for analyzing the performance of manufactured solar cells on the same wafer. Therefore, uniformity test is indispensable to be studied. There are two important parameters that are used to judge the 'good' or 'bad' uniformity. One of the parameter is the standard deviation (STDEV), which describes how spread out numbers are and can be mathematically expresses as:

$$STDEV = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \overline{x})^2} \tag{4-1}$$

where N is the number of samples, x_i is value of each sample, $\overline{x}$ is the mean value of the samples. Another parameter is called as non-uniformity, which is defined as [83]:

$$Non-uniformity = \frac{(h_{max} - h_{min})}{2h_{avg}} \times 100\% \tag{4-2}$$

where h_{max} and h_{min} are the maximum and minimum measured thickness, respectively; h_{avg} is the average thickness of the total measured thickness. Normally, if the value of non-uniformity is below 10%, the uniformity of this layer is acceptable. Based on previously passivation optimization, the deposition pressure and power are investigated under 180 °C with a dilution ratio of 3.

Effect of Deposition Pressure

The investigation of deposition pressure is conducted, the results are shown below in Fig 4.6.

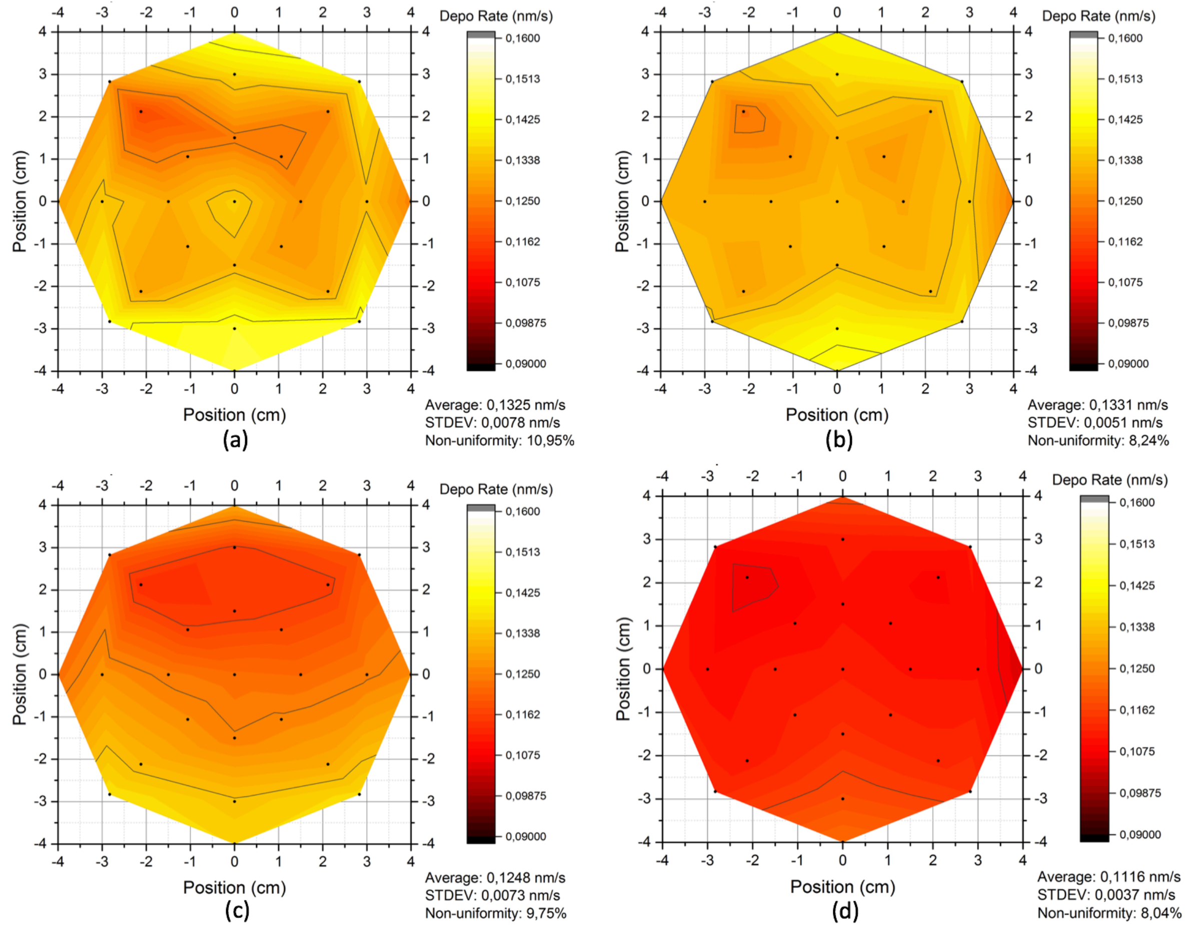


Figure 4.6 Comparison of uniformities under 180 °C, fixed deposition power 2.0 W with a dilution ratio of 3 (in total 40 sccm) but different deposition pressure: a). 0.8 mbar; b) 0.9 mbar; c). 1.1 mbar; d). 1.4 mbar. Theses samples use Corning glasses as substrates.

The measured thicknesses are transferred to deposition rates and two-dimensional (2D) color filled contour plots are given for more straight view on the uniformity of the layer. Black dots represent the measured points (in total 25 points for each sample). It is revealed in Fig. 4.6 that the values of STDEV and non-uniformity are conforming each other. In terms of non-uniformity, deposition pressure above 0.8 mbar is acceptable for obtaining uniform layer.

Effect of Deposition Power

From above obtained results, 1.4 mbar is chosen for optimizing the deposition power. The samples are shown below in Fig. 4.7.

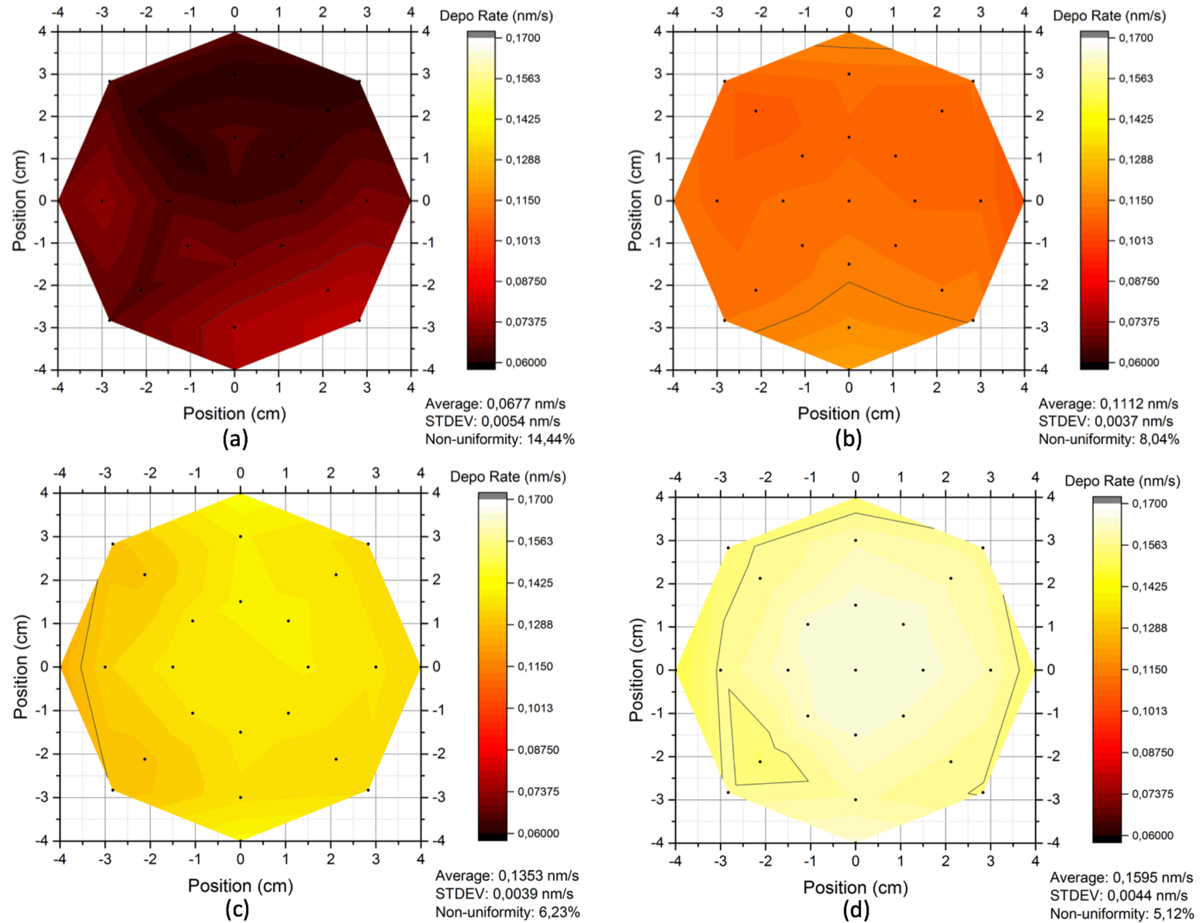


Figure 4.7 Comparison of uniformities under 180 °C, fixed deposition pressure 0.7 mbar with a dilution ratio of 3 (in total 40 sccm) but different deposition power: a). 1.8 W; b) 2.0 W; c). 2.3 W; d). 2.7 W. Theses samples use n-type polished FZ <111> c-Si wafers as substrates.

As shown in Fig. 4.7, except the case of 1.8 W, uniformity gets better with higher deposition power (non-uniformity < 10 %). Higher power is also tested (not shown), still keeping high uniformity.

The reason behind the non-uniformity is speculated to be so-called 'edge effect', where the asymmetry design of electrodes inducing higher potential at the edges of electrodes are stronger than that of the middle. Stronger depletion of SiH_4 at edges leads to faster deposition at the edges. This phenomenon can be found in Fig. 4.5, the edges are thicker than the centers in general. However, increasing of pressure is preferable for formation of radical SiH_3 [60], which has low sticking coefficient (mentioned in section 2.1.2), thus more uniform layer can be obtained. With increasing of power, the dissociation of SiH_4 at edges become gradually saturated while the middle

parts still the increases with the power. Therefore, the smaller difference of depletion of SiH_4 between edges and middle can be found.

4.1.3 Summary

After the optimization of deposition parameters of i-a-Si:H in terms of both passivation and uniformity, the final chosen parameters for manufacture of solar cells are listed below in the Table 4.5. The higher power is chosen due to its slightly better passivation quality over other two optimized conditions. With 6 nm i-a-Si:H symmetrical passivation, an effective lifetime over 3.3 ms, iVoc beyond 722 mV and low J_0 (5.5 fA/cm^2) can be obtained. The excellent passivation quality is also confirmed by depositing 10 nm i-a-Si:H symmetrically on n-type FZ <111> c-Si wafer, which shows a lifetime over 13 ms and iVoc beyond 730 mV.

Table 4.5 Deposition parameters of optimized hydrogenated intrinsic amorphous silicon layer.

Layers	Dilution Ratio (-)	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	Flow rate (sccm)	Frequency (MHz)
i-a-Si:H	3	180	1.4	3.2	40	13.56

4.2 Optimization of Doped Silicon Layers

After optimization of i-a-Si:H, the main passivating contacts to achieve carrier selective collection and form lossless contact in SHJ solar cell are needed. Those passivating contacts are manipulated by adding certain amount of impurity atoms to change their electrical conductivities. In this thesis, the doped silicon layers are divided into two main groups, namely, doped hydrogenated amorphous silicon and doped hydrogenated nanocrystalline silicon oxide. Firstly, carrier selectivity collection is introduced. Afterwards, the optimization of those doped layers is conducted.

4.2.1 Carrier Selectivity Collection

The carrier selectivity collection refers to the collection of certain types of charge carriers at c-Si/i-a-Si:H interface. According to definition proposed in [84], good selectivity indicates large difference in the carrier concentrations. Fermi level is a good indicator that represents the relative amount of charge carriers. Under thermal equilibrium, ideal selectivity is achieved when Fermi level is above conduction band edge for electrons or below valence band edge for holes. Meanwhile, change of the carrier concentration influences the band bending at c-Si/i-a-Si:H interface. Under thermal equilibrium, the band bending is numerically represented by the built-in voltage (V_{bi}). The related energy band diagram of a n-type SHJ solar cell is analyzed below.

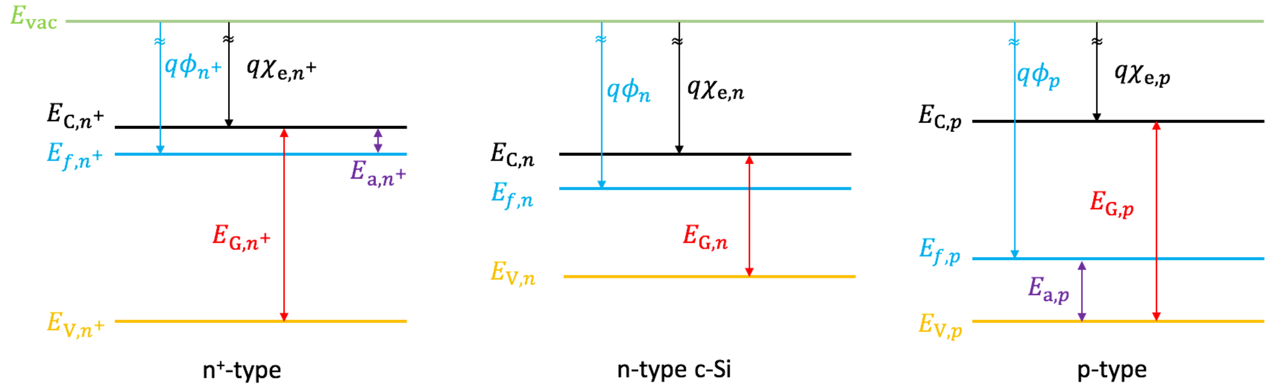


Figure 4.8 Energy band diagrams of an n⁺-type layer, n-type c-Si and p-type layer. Both p- and n⁺-type layers have larger bandgap than n-type c-Si.

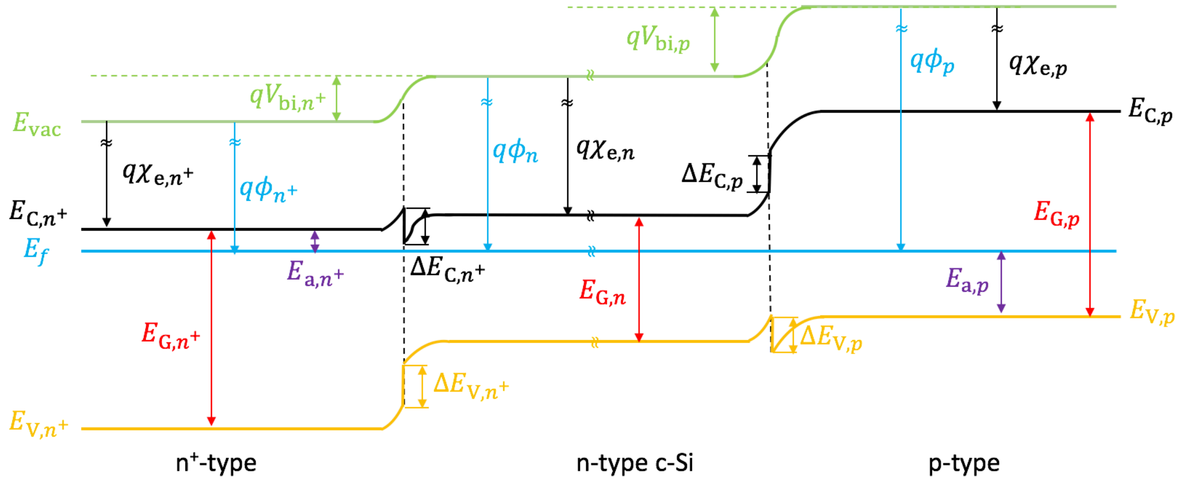


Figure 4.9 The energy band diagram of an n-type SHJ solar cell with large bandgap n⁺- and p-type passivating contacts under dark and thermal equilibrium. The lengths of the layers are not scaled to the practical case.

For heterojunction, as shown in Fig. 4.9, assume the bulk is a n-type c-Si substrate, then the built-in voltage is defined as the work function difference of adjacent layers individually. For p-type layer:

$$V_{bi,p} = \phi_p - \phi_n \tag{4-3}$$

while for n-type layer:

$$V_{bi,n^+} = \phi_n - \phi_{n^+} \tag{4-4}$$

where ϕ_n is the work function of n-type c-Si substrate, ϕ_p and ϕ_{n^+} are the work functions for p-type and n-type layers, respectively and they are expressed as:

$$\phi_p = \chi_{e,p} + E_{G,p} - E_{a,p} \tag{4-5}$$

$$\phi_{n^+} = \chi_{e,n^+} + E_{a,n^+} \tag{4-6}$$

where χ_e is the electron affinity. Then the V_{bi} can be expressed as:

$$V_{bi,p} = \chi_{e,p} - \phi_n + E_{G,p} - E_{a,p} \tag{4-7}$$

$$V_{bi,n^+} = \phi_n - \chi_{e,n^+} - E_{a,n^+} \tag{4-8}$$

where ϕ_n is fixed for c-Si, $\chi_{e,p}$ and χ_{e,n^+} are also almost constant for thin-film silicon layers [85]. Therefore, for maximizing built-in voltage thus the selectivity, p-type layers with larger bandgap and lower activation energy are preferred; for n-type layer, only lower activation energy is required. To quantitatively demonstrate the activation energy, the dark J-V measurement is applied, which measures the dark conductivity at the meantime. Besides, the value of bandgap is extracted from Spectroscopic Ellipsometry. For doped a-Si:H layers, the optimization of passivation quality is firstly conducted, then followed by conductivity measurement. As for optimization of doped nc-SiO_x:H layers, optimization of conductivity is of the priority, then the passivation quality is checked.

4.2.2 Doped Hydrogenated Amorphous Silicon

Before conducting the optimization doped a-Si:H layers, it is essential to understand the doping mechanisms.

Doping Mechanism

As introduced in Fig. 2.1, the substutional doping of impurity in c-Si, for example, phosphorus, leads to tetrahedral coordination, while the extra valence electron from P atom induces the doping. According to research from John Robertson [86], in amorphous silicon, the 8-N rule is satisfied, where N is the impurities' valence electron number. For $N > 4$, such as P atom ($N = 5$), threefold coordination of P atom in the amorphous network is suggested. While for $N < 4$, for instance B atom ($N = 3$), it will form the same number of covalent bonds as its valence electrons, thus, B atom will be also threefold coordinated.

Taking P atom doping as an example, three possible configurations are shown below. The P atom in Fig. 4.10.a is incorporated as the 8-N rule. However, this is electrically inactive, i.e. no doping effect is induced from this state. The higher doping efficiency requires higher fraction of fourfold coordination. For c-Si, the doping efficiency is almost unity, while for a-Si:H it is two to three magnitudes lower than that of c-Si. Although the coordination in Fig. 4.10.c fulfill the fourfold coordination, it is very unstable. Therefore, the active doping is mainly contributed from the defect-compensated donor state (Fig. 4.10.b), which forms a dangling bond simultaneously. Similar applies to B atom doping, where defect-compensated acceptor state play the major role for p-type

doing. This explains the reported results from [87], [88], where the higher doping is companied by higher defect density.

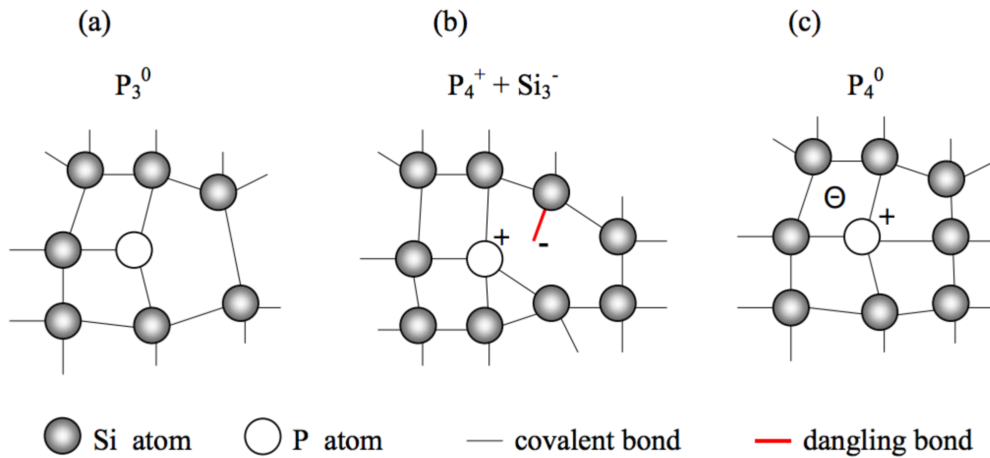


Figure 4.10 Three possible configurations of P atom doping in a-Si:H. a). non-doping state; b). defect-compensated donor state; c). neutral donor state. The express P_Z^q represents the coordination of P atom, where Z is the coordination number while q is the charge state (0 = 'neutral'). Adapted from [33].

With the view to conduct the optimization of doped a-Si:H layers, the tradeoff between the passivation and electrical conductivity is expected. The samples are prepared exactly same as that in previous section before conducting rf-PECVD depositions. Besides, the i-a-Si:H layer (10 nm) that is optimized in previous section is applied for optimization of doped layers. The process overview is given below in Fig. 4.11. The optimization of doped a-Si:H is conducted in AMOR.

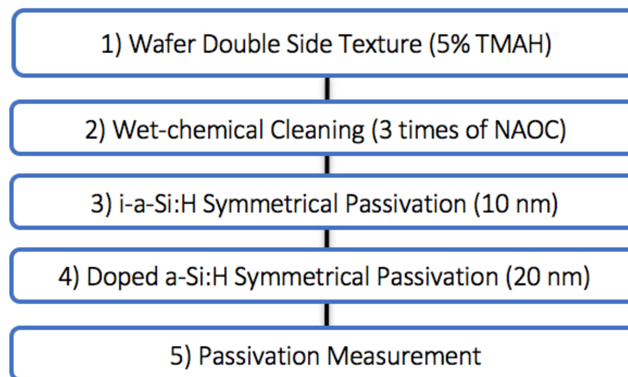


Figure 4.11 The process flowchart of doped a-Si:H passivation optimization.

n-type a-Si:H

The typical deposition parameters of n-type a-Si:H from PVMD group are given in Table 4.6.

Table 4.6 Deposition parameters of i/n symmetrical passivation optimization.

Layers	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	SiH_4 (sccm)	PH_3 (sccm)	H_2 (sccm)	Frequency (MHz)
i-a-Si:H	180	1.4	3.2	10	0	30	13.56
n-type a-Si:H	180	0.6	2.6	40	11	0	13.56

For better demonstration of passivation quality change after n-type a-Si:H layer deposition, the comparison between i-a-Si:H and i/n a-Si:H is illustrated below.

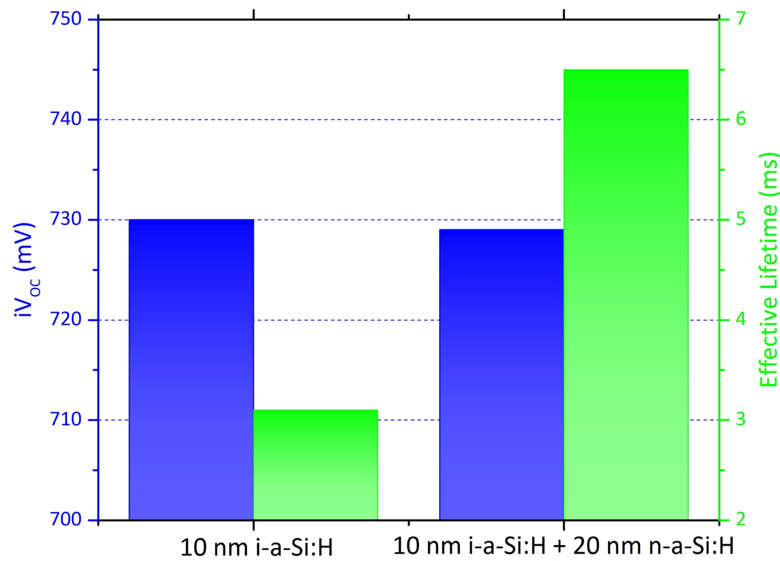


Figure 4.12 The comparison of passivation quality between i-a-Si:H and i/n a-Si:H.

As demonstrated in Fig. 4.12, the passivation quality in terms of lifetime double from 3.1 ms to 6.5 ms after n layer deposition. Meanwhile, the values of iV_{OC} are kept around 730 mV. The excellent passivation quality of n-a-Si:H layer is sufficient to be applied into solar cell manufacture.

p-type a-Si:H

Since the present deposition parameters for p-type a-Si:H gives very poor passivation quality [89], the initial combination of the deposition parameters for p-type a-Si:H is based on that of the optimized i-a-Si:H layer. The deposition parameters of p-type a-Si:H are given below in Table 4.7. Here a lower power is chosen for reducing the ion bombardment induced damage to the i-a-Si:H passivation beneath.

Table 4.7 Deposition parameters of i/p symmetrical passivation optimization.

Layers	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	SiH_4 (sccm)	B_2H_6 (sccm)	H_2 (sccm)	Frequency (MHz)
i-a-Si:H	180	1.4	3.2	10	0	30	13.56
p-type a-Si:H	180	0.7-1.1	2.3	6.7-26.7	8-20	0-26.6	13.56

To simplify, here dilution ratio is used for distinguishing of different combinations of deposition parameters and it is defined as:

$$Dilution\ Ratio = \frac{SiH_4 + H_2}{B_2H_6} \times 100\% \tag{4-9}$$

where different gases represent the corresponding gas flow. This dilution ratio is different from the hydrogen dilution ratio described in optimization of i-a-Si:H. According to limited time, the experiments are mainly designed for different dilution ratios from 0.5 to 5. Afterwards, the optimized dilution ratio varies the pressure from 0.7 to 1.1 mbar is tested. The gas combination of each dilution ratio is demonstrated in Table 4.8. The passivation results of varying dilution ratios are presented below.

Table 4.8 Gas combinations for different dilution ratios.

Dilution Ratio	SiH_4 (sccm)	B_2H_6 (sccm)	H_2 (sccm)
0.5	26.7	13.3	30
1	20	20	0
3 (solid point)	20	10	10
3 (hollow point)	10	10	20
4	8	8	24
5	6.7	6.7	26.6

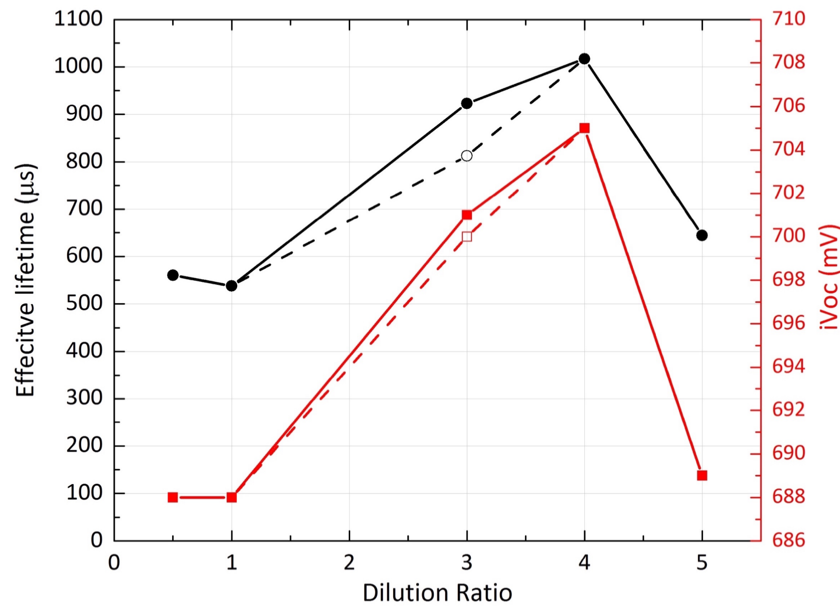


Figure 4.13 The passivation quality of i/p-a-Si:H of varying dilution ratios, where the thicknesses for i-a-Si:H and p-a-Si:H are 10 nm and 20 nm, respectively.

According to passivation quality, the obtained results basically conform with previous introduced doping mechanism, where higher doping concentration of B_2H_6 is supposed to introduce more defects thus inferior passivation quality. For dilution ratio series, the optimized passivation quality of p-a-Si:H is achieved when DR equals to 4, the effective lifetime reaches 1017 µs with iV_{OC} of 705 mV and J_0 of 7.1 fA/cm^2.

Besides, under DR equals to 4, the pressure is slightly changed from 0.7 mbar to 1.1 mbar. The results demonstrated in Table 4.9 indicate the optimized pressure is still 0.9 mbar.

Table 4.9 Passivation quality of p-a-Si:H with varying pressure.

$P_{deposition}$ (mbar)	τ_{eff} (µs)	iV_{OC} (mV)	J_O (fA/cm^2)
0.7	788	697	12.5
0.9	1017	705	7.1
1.1	671	695	8.5

In contrary to the case of n-a-Si:H, which enhances the passivation quality of i-a-Si:H layer, even the ‘optimized’ p-a-Si:H layer induces a large degradation of passivation. Compare to the passivation quality obtained in [48], the optimization of p-a-Si:H is still needed to be further investigated.

The conductivity of doped a-Si:H layers are measured and exhibited in section 4.3.

4.2.3 Doped Hydrogenated Nanocrystalline Silicon Oxide

Optimizing doped nc-SiO_x:H layers with the aim to reduce their activation energies are conducted previously in the group. The measured physical properties of the doped nc-SiO_x:H layers are listed below, where X_C represents the crystalline fraction.

Table 4.10 The physical properties of optimized doped nc-SiO_x:H layers.

Layers	E_{act} (meV)	E_G (eV)	X_C (%)	Thickness (nm)
p-nc-SiO_x:H	99.0	2.27	60.7	57
n-nc-SiO_x:H	40.6	2.70	68.9	115

The deposition parameters of both n- and p-type nc-SiO_x:H are demonstrated below in Table 4.11.

Table 4.11 The deposition parameters of doped nc-SiO_x:H.

Layers	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	SiH_4 (sccm)	B_2H_6 (200ppm in H_2) (sccm)	PH_3 (sccm)	CO_2 (sccm)	H_2 (sccm)
p-nc-SiO_x:H	180	2.2	11	0.8	10	-	1.4	170
n-nc-SiO_x:H	180	1.5	11	1	-	1.2	1.6	100

Further optimization of the layers takes mainly two aspects into account:

- Since CO_2 plasma treatment is reported to be effective for reducing the thickness of incubation layer [90], i.e. higher crystalline fraction over a fixed thickness of nc-SiO_x:H layer. The CO_2 plasma treatment is applied on the surface of i-a-Si:H layers before the depositions of nc-SiO_x:H layer.
- Besides, the i-a-Si:H layer is deposited under relatively low power (3.2 W), while the doped nc-SiO_x:H requires a high power (11 W). The potential damage induced by this high power to i-a-Si:H layer beneath is considered. This is conducted by using grading deposition, in which the oxide layer is deposited with initially 3 W, then 6 W and eventually 11 W for different corresponding time rather than 11 W directly.

Effect of Carbon Dioxide Plasma Pretreatment on Passivation

The deposition conditions are listed below. The CO_2 plasma treatment is selectively applied for 10 seconds. The deposition parameters are summarized in Table 4.12.

Table 4.12 The deposition parameters for investigating effect of CO_2 plasma treatment.

Layers/ Process	with/ w/o CO_2 PT	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	SiH_4 (sccm)	B_2H_6 (200ppm in H_2) (sccm)	PH_3 (sccm)	CO_2 (sccm)	H_2 (sccm)
CO_2 PT	-	180	2	4	0	0	-	100	0
p-type-a	w/o	180	2.2	11	0.8	10	-	1.4	170
p-type-b	w	180	2.2	11	0.8	10	-	1.4	170
n-type-a	w/o	180	1.5	11	1	-	1.2	1.6	100
n-type-b	w	180	1.5	11	1	-	1.2	1.6	100

The passivation results are demonstrated in Fig. 4.14. For p-type nc-SiO_x:H layer, although an increment of iV_{OC} of 4 mV is observed after CO_2 plasma treatment, the effective lifetime drops around 300 μs at the meantime. As for n-type nc-SiO_x:H layer, both iV_{OC} and effective lifetime are decreased when CO_2 plasma treatment is applied. The lifetime drop is more than 35% compared to the sample without CO_2 plasma treatment.

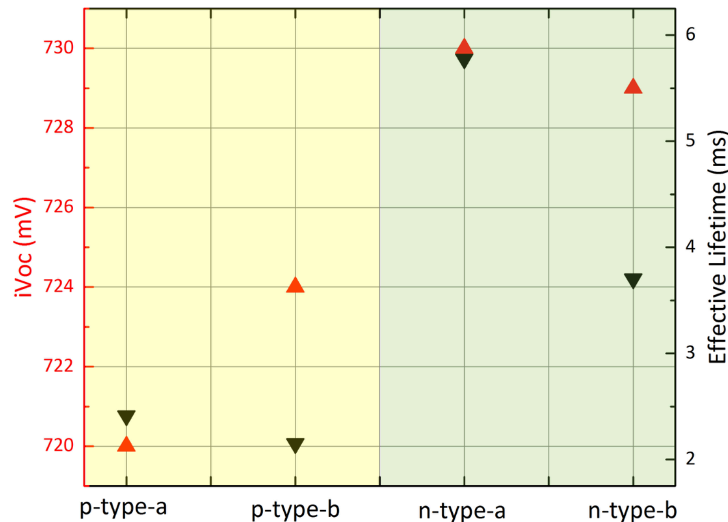


Figure 4.14 The investigation results of CO_2 plasma treatment on passivation qualities.

Therefore, in terms of passivation, there is nearly no improvement can be observed. However, since CO_2 plasma treatment can have persistent memory effect in the deposition chamber, which

requires frequent cleaning for other depositions. Eventually, the effect of CO_2 plasma treatment on crystal growth during deposition of doped nc-SiO_x:H layer is not further investigated.

Effect of High Power Deposition

The deposition conditions are listed in the Table 4.13. For p-type layers, the CO_2 plasma treatment is applied.

Table 4.13 The deposition parameters for investigating effect of high power deposition.

Layers	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	SiH_4 (sccm)	B_2H_6 (200ppm in H_2) (sccm)	PH_3 (sccm)	CO_2 (sccm)	H_2 (sccm)
p-type-A	180	2.2	11	0.8	10	-	1.4	170
p-type-B	180	2.2	3+6+11	0.8	10	-	1.4	170
n-type-A	180	1.5	11	1	-	1.2	1.6	100
n-type-B	180	1.5	3+6+11	1	-	1.2	1.6	100

The measured passivation qualities are illustrated below in Fig. 4.15.

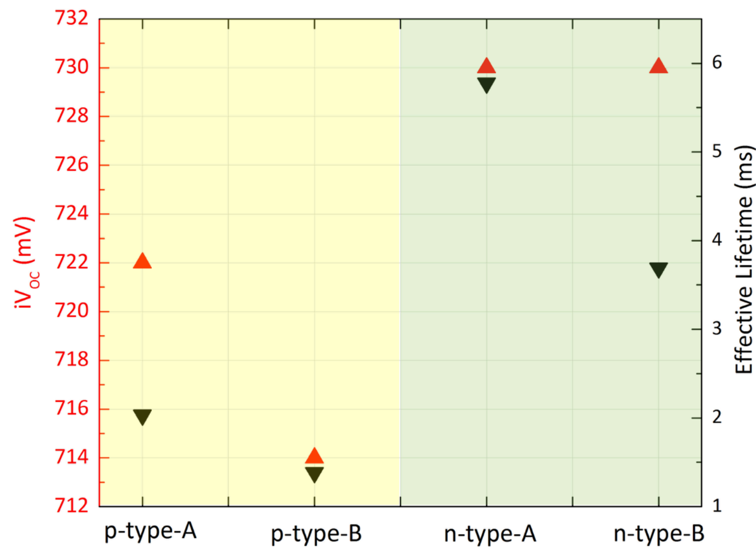


Figure 4.15 The investigation results of high power deposition on passivation qualities.

As demonstrated Fig. 4.15, no expected damage is observed by direct high power deposition to the i-a-Si:H layer. In contrast, the effective lifetime degrades for grading deposition in both types. The values of iV_{OC} are kept same for n-type layers while 8 mV drop for p-type layers. In addition, grading deposition is speculated to have thicker incubation layer according to low power

deposition at initial stage. Therefore, the direct deposition (without grading deposition) of both types of nc-SiO_x:H layers are chosen.

Summary

In terms of passivation quality, the optimized both n- and p-type nc-SiO_x:H should be directly applied without either grading deposition or CO_2 plasma treatment.

4.2.4 Summary

Within this section, all doped silicon layers are optimized mainly in term of the passivation. the optimized passivation qualities of all doped silicon layers are listed below in Table 4.14. Beneath the doped layers, there are 10 nm of optimized i-a-Si:H layers.

Table 4.14 The passivation qualities of optimized doped silicon layers.

Layers	τ_{eff} (ms)	iV_{OC} (mV)	J_O (fA/cm^2)
n-a-Si:H	6.5	729	4.2
p-a-Si:H	1.0	706	7.1
n-nc-SiO_x:H	6.8	730	3.6
p-nc-SiO_x:H	2.4	720	9.5

4.3 Argon Test

It is reported in [91], post argon plasma treatment on the surface of thin i-a-Si:H layer can better improve the passivation quality compared to post hydrogen plasma treatment. It is explained according to neutralization of the surface stress thus proceeding the transfer from dihydrides (multi-hydrides) to mono-hydrides, which is beneficial for forming more dense, abrupt and better passivated i-a-Si:H/c-Si interface. Based on this research, auxiliary experiments are further conducted for checking argon plasma induced changes of conductivity and activation energy.

The samples are prepared by depositing the doped layers without or with argon (around 20 sccm) on top of the Corning glasses, then with e-beam evaporation, Al (300 nm) is deposited on those layers through the hard mask that is designed for dark conductivity measurement. Afterwards, samples are annealed in air for 30 minutes for forming better contact of Al and deposited layers.

The investigation results of argon plasma during deposition of the doped layers are demonstrated below in Table 4.15. Except p-type a-Si:H layer, it is obvious that argon plasma generally introduces negative influences on the conductivity of doped layers. For the n-type nc-SiO_x:H sample, the activation energy is too high to be measured. Therefore, in terms of conductivity, the

argon plasma is not suggested to be added during deposition of doped silicon layers except p-type a-Si:H layer.

Besides, it is also observed that the conductivity of n-type nc-SiO_x:H layer is even lower compared to that of n-type a-Si:H layer, which is not in agreement with the expected improvement of conductivity for nc-SiO_x:H layer. Although nano-crystals are contained in the nc-SiO_x:H layer, the amount of oxygen alloyed in the layer might be too high to deteriorate the conductivity significantly. Therefore, n-type nc-SiO_x:H still needs further optimization according to better conductivity and lower activation energy, in other words, reduce the oxygen content alloyed in the layer. Especially when its conductivity is compared to that reported in [48].

Table 4.15 The physical properties of optimized doped a-Si:H layers with and without argon.

Layers	with/w/o argon	E_a (meV)	Conductivity (S/cm)	Thickness (nm)
n-a-Si:H	w/o	191.5	8.64E-2	35
	with	193.7	1.71E-2	74
p-a-Si:H	w/o	419.7	3.30E-5	103
	with	357.6	3.64E-4	60
n-nc-SiO_x:H	w/o	114.6	5.99E-3	40
	with	out of range	out of range	27
p-nc-SiO_x:H	w/o	51.4	1.74E-1	29
	with	299.8	3.15E-5	28

As summarized in Table 4.15, it is worth noting the excellent activation energy of p-type nc-SiO_x:H is achieved for only 29 nm on glass. However, the measured activation energy and conductivity could be different from the case of real solar cells. This is according to layers applied to solar cells might have different thicknesses compared to that in the table. Besides, especially for doped nc-SiO_x:H layer, the substrate sensitive growth can lead to different crystalline fractions on glass and i-a-Si:H layer (solar cell case). Generally, a lower crystalline fraction (less conductive) of deposited nc-SiO_x:H layer on top of i-a-Si:H layer is expected according to [48].

4.4 Summary

Within this chapter, the optimizations of both intrinsic and doped silicon layers are conducted. For i-a-Si:H layer, the optimization is processed mainly based on passivation quality and

uniformity. For doped silicon layers, the conductivity of layers, which is related to the field effect passivation of c-Si/i-a-Si:H interface, is considered together with the chemical passivation quality. Eventually, the argon plasma induced influence on conductivity and activation energy of doped layers are investigated. Except the increased conductivity is observed for p-type a-Si:H layer, other doped layers suffer from the argon plasma treatment, especially for doped nc-SiO_x:H layers. The measured conductivity also gives a hint that further optimization of n-type nc-SiO_x:H is necessary for finding a balance between the oxygen content alloyed in the layer and the transparence if it is applied to FBC-SHJ solar cells. Till now, the layers are ready to be applied for manufacture of FBC-SHJ solar cells.

5

FBC-SHJ SOLAR CELL

In this chapter, the optimized silicon layers are applied to manufacture the FBC-SHJ solar cells. An overview of manufacture process is firstly introduced. Afterwards, the performances of manufactured solar cells are measured and analyzed. Due to their relatively simple process, FBC-SHJ solar cells are the elemental demonstrator of passivation and junction quality. Therefore, the investigation of FBC-SHJ solar cells gives hints on the evaluation of IBC-SHJ solar cells performance.

5.1 Production Process

The schematic demonstration of FBC-SHJ solar cell manufacture process is shown in Fig. 5.1.

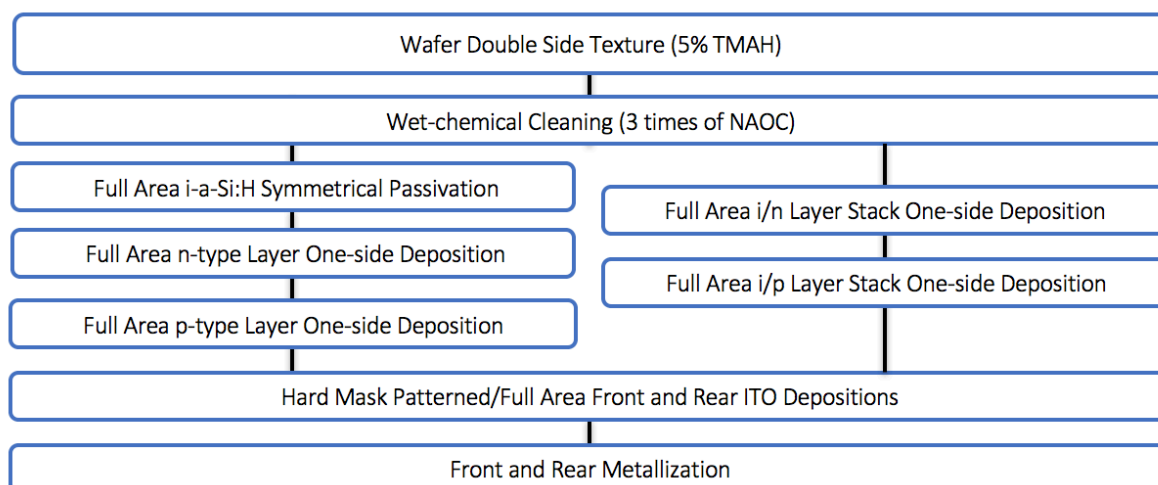
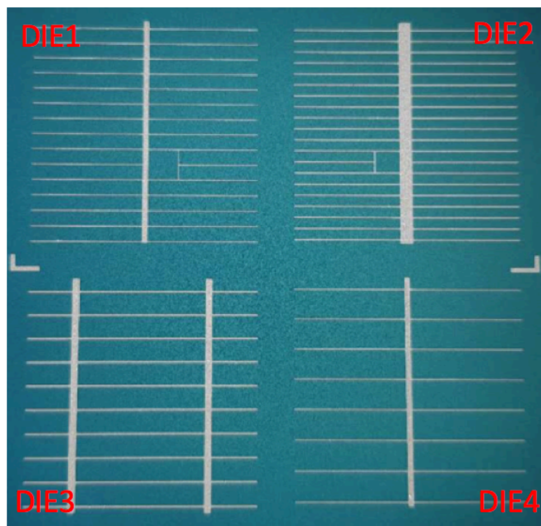


Figure 5.1 Schematic process flowchart of FBC-SHJ solar cell manufacture. Different deposition sequences are applied.

SIEGERT WAFER n-type double-side polished FZ <100> c-Si wafers with a range of resistivity (1-5 Ω·cm) and thickness (280±20 μm) are used as substrates. Wafers are firstly textured on both sides and cleaned as same as the pre-deposition steps of passivation optimization. Initially (left sequence in Fig. 5.1), those wafers are then loaded into AMOR (with flipping stage) for symmetrical i-a-Si:H layer passivation, afterwards, doped a-Si:H and nc-SiO_x:H layers are deposited

in AMOR and AMIGO, respectively. Initially, experiments were performed on AMOR which is designed for SHJ solar cells including an internal flipping stage. However, due to the AMOR maintenance, experiments were carried out under AMIGO premises (without flipping stage). In this case, another deposition sequence is tested and applied in AMIGO as right-hand process in Fig. 5.1. (i.e. one-side i/n layer stack is firstly deposited then i/p layer stack on the other side with vacuum break). Before each deposition, pre-conditioning of the deposition chambers is done by hydrogen plasma treatment for 30 minutes and coating of the deposited layer for 15 minutes. After forming the passivation contacts on both sides of the substrate, the ITO is deposited by rf-sputtering tool either full area or patterned by hard mask. Eventually, metallization is conducted by different methods with different materials. The front metallization follows the scheme depicted in Fig. 5.2 for 2.8 cm × 2.8 cm device with different metal coverage.

After ITO sputtering severe lifetime drop is reported as consequence of passivation quality degradation [64]. Such an effect has been also observed previously in PVMD group [78]. Therefore, the passivation quality of the solar cell precursor is measured before and after the ITO in terms of lifetime. The objective of these measurements is twofold: i). to check the passivation quality of the precursor, and ii). to evaluate the possible passivation degradation induced by ITO deposition. Besides, to evaluate carriers collection from c-Si to the metal finger, the SunsVoc of the precursor before and after metallization are measured. For finished solar cells, the illuminated J-V characteristics and EQE are measured to evaluate the final performance of the solar cell.



DIE	Metal Coverage
1	5%
2	12%
3	11.5%
4	3%

Figure 5.2 The front metal grid patterning of the FBC-SHJ solar cells.

5.2 Investigation of Manufacture Sequences

As shown in Fig.5.1, the influence induced by different manufacture sequences are investigated. The potential influence of breaking vacuum in Amigo for flipping the wafer is the oxidization of the c-Si surface, which deteriorates the passivation quality of the c-Si/i-a-Si:H interface afterwards

(proved within the thesis). Since the i-a-Si:H layers for the left and right sequences are individually deposited by AMOR and AMIGO, respectively, the passivation quality of i-a-Si:H layers from both PECVD tools are firstly examined. Within this first investigation, the order of the deposition sequences can be also evaluated.

By adjusting the optimized recipe of i-a-Si:H from AMOR based on power density (power per electrode area and electrode distance), the recipe was adapted for AMIGO as Table 5.1 summarizes. The symmetrical passivation test is carried out by depositing 11 nm intrinsic layers from both PECVD tools with same pre-deposition steps as introduced previously. Lifetime results demonstrate similar passivation qualities of i-a-Si:H from both PECVD tools (see Table 5.1).

Table 5.1 Deposition parameters and passivation qualities of 11 nm optimized hydrogenated intrinsic amorphous silicon layer in both AMOR and AMIGO.

Layers	Dilution Ratio (-)	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	Flow rate (sccm)	τ_{eff} (μs)	iV_{OC} (mV)
AMOR i-a-Si:H	3	180	1.4	3.2	40	3.17	730
AMIGO i-a-Si:H	3	180	1.4	3	40	3.15	730

Later, further investigation on the solar cells are conducted. The test structure under study is shown in Fig. 5.3.

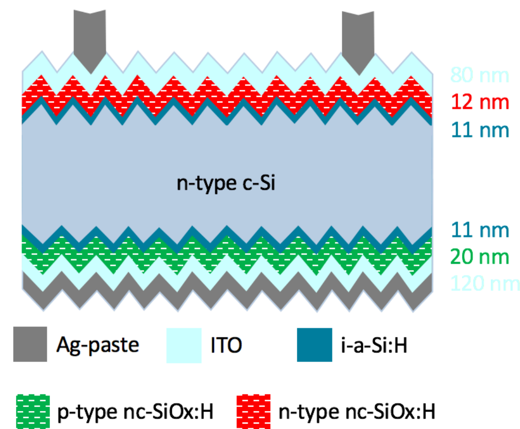


Figure 5.3 The illustration of solar cell structure for the investigation different deposition sequences.

As Fig. 5.3 depicts, a solar cell with rear junction is developed. Accordingly, to collect generated electrons avoiding low lateral conductivity of doped nc-SiO_x:H layers, a front 80 nm ITO layer is applied. The rear side is also covered by 120 nm ITO, but in this case, lateral transport is not necessary for full area metallization. However the purpose of the rear side ITO is to act as back reflector reducing the parasitic absorption in metal interfaces [17]. Besides, front ITO also is used

as ARC (minimum reflection at 600 nm [19]), which enhances the light in-coupling of the front surface. Additionally, ITO layers protect the inner layers from eventual metal diffusion. The metallization was based on Ag screen-printing and Ag thermal evaporation according to front (see Fig. 5.2) or rear side scheme (full metallization). The external parameters from illuminated J-V measurement are summarized on Table 5.2.

Table 5.2 The external parameters of solar cells with different deposition sequences.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
AMOR	4	38.42	694	0.50	13.27	700	0.80
AMIGO	4	38.51	699	0.51	13.61	711	0.81

There is no significant influence on external parameters following aforementioned deposition sequences. Therefore, both sequences deploy similar passivation and junction quality, thus demonstrating that from both plasma tools similar SHJ solar cells can be attained.

In addition, since this test structure is a typical structure among this chapter, the external parameters presented in the Table 5.2 reflect the most challenging limiting factor for achieving high-efficiency solar cell as FF. The ΔFF is defined as the difference between pFF measured from SunsVoc and FF measured from illuminated J-V measurement. A larger ΔFF indicates the cell suffers more from the highly resistive transport of charge carriers, which is generally expressed as a higher value of R_S. Therefore, the main purpose for the following series of experiments is to investigate the source of FF losses. Besides, other external parameters are investigated along with the FF.

5.3 FF Evaluation

In order to understand which parameters of solar cell influence on FF, a general explanation of transport of carriers in SHJ is firstly presented.

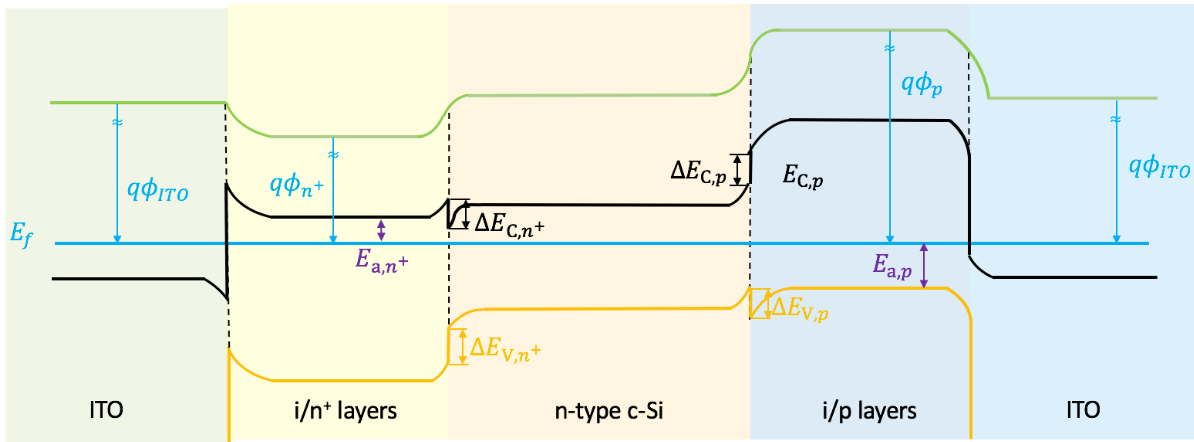


Figure 5.4 The energy band diagram of a typical SHJ precursor till ITO contact.

Fig. 5.4 depicts a sketch of band diagram of SHJ solar cells. In this case, for the sake of simplicity, the i-a-Si:H layers that are applied on both sides of c-Si substrate of the real solar cell are assumed has same band gap as the doped layers. At each heterointerface (c-Si/a-Si:H and doped layer/ITO), a band offset and energy barriers are built as consequence of different electronic structure of each material. Transport mechanisms of carriers crossing through heterointerfaces are thermionic emission and tunneling. In general, the ITO is assumed as a degenerated n-type semiconductor [92].

For hole collection at the c-Si/i-a-Si:H interface physics follow trap-assisted-tunneling (TAT), direct tunneling or thermionic emission. Accordingly, the efficient collection depends on c-Si induced band bending, energy barrier size and ITO conductivity [93]. In particular, for the p-layer/ITO interfaces, the holes have to tunnel through the so-called band to band tunneling. FF is mainly affected by the doping in doped layers, the work function mismatch (ΔWF $= \phi_{ITO} - \phi_p$), and bandgap (in case of p-contact) [93]. It is reported that WF of TCO is not decisive for hole collection if high doping (very small E_{act}) is achieved for p-layer [94]. Similarly, the better WF match the lesser restriction on the doping and thickness of the p-layer [95]. Thus, tailoring of this energy barrier is possible by engineering either p-layer or the ITO.

Similarly, for electron collection at c-Si/i-a-Si:H contact is TAT or direct tunneling. Since ITO is n-type like, therefore, direct tunneling in the conduction band occurs at n-type/ITO contact. However, if n-type layer is not well doped in terms of activation energy, the Schottky barrier can also formed on n-type/ITO contact, which hinders the collection of electrons to the electrode. The transport mechanisms for this interface can be direct tunneling, TAT and thermionic emissions.

Therefore, for forming low-resistive contacts between doped nc-SiO_x:H and ITO, typically, the last few nanometers of doped layers are deposited without CO_2, which is expected to enhance the

doping efficiency, thus lower E_{act}. If the layer thickness is described as '*x* + *y*', it means the layer consists of *x* nm of nc-SiO_x:H and *y* nm of nc-Si:H.

The investigation of improving FF starts from i-a-Si:H analysis, then focusing on doped silicon layers aiming on low activation energy. Afterward, different designs of solar cell structures are also tested including hybrid solar cells with polysilicon contacts.

Within the thesis, Al e-beam evaporation is already proved to be detrimental to the nc-SiO_x:H passivation layer (> 30 mV reduction), while no degradation in case of Ag screen printing and Ag thermal evaporation. Therefore, following experiments only use Ag screen printing and/or Ag thermal evaporation for metallization.

5.3.1 The Effect of i-a-Si:H Thickness

The thickness of i-a-Si:H buffer layer induced influence is tested with different thickness. The front emitter design as demonstrate below are tested. The p layer consists of 3 nm of nc-SiO_x:H and 10 nm nc-Si:H layers, while n layer consists only the nc-SiO_x:H.

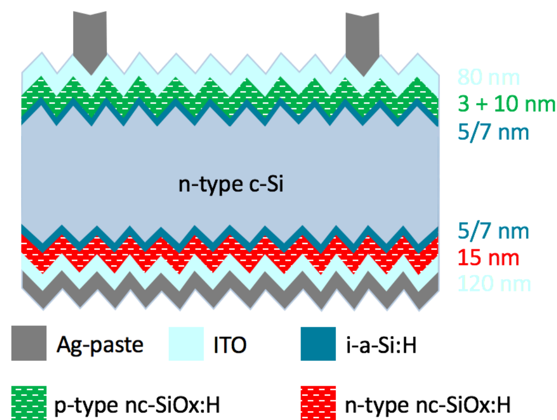
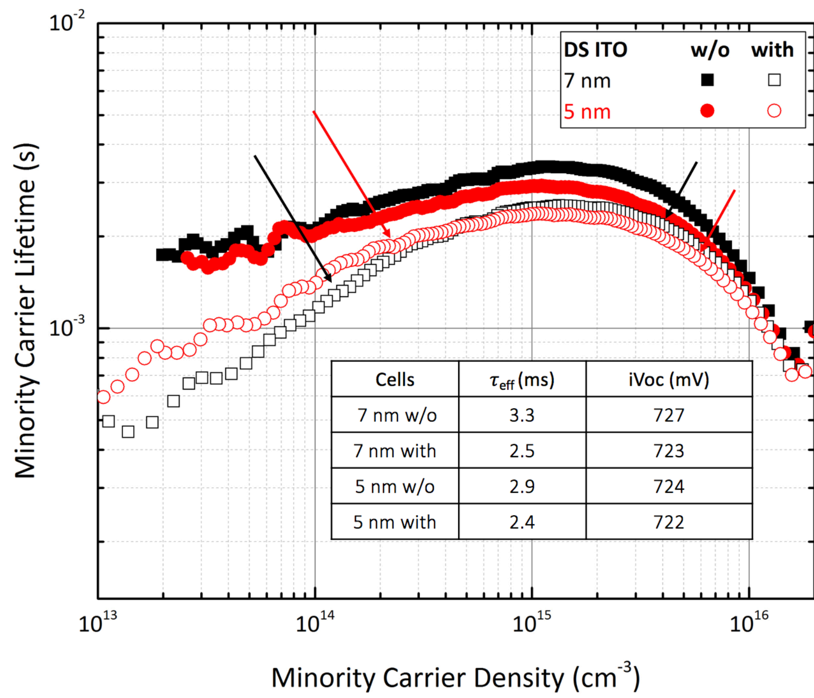


Figure 5.5 The test structure with varying i-a-Si:H layer thickness.

The precursor lifetime with excess minority carrier density before and after ITO sputtering are plotted in Fig. 5.6. No post annealing is conducted.

As expected, the thicker intrinsic layer provides overall better passivation quality. However, since thin doped layers on both sides, the ITO deposition induced damages can be observed on both precursors (the effect of the doped layer's thickness will be explained in next section). Both the chemical passivation (observed at high injection: > 5×10^{15} cm^{-3}) and field effect passivation (observed at low injection: 10^{14} cm^{-3}) are weakened but still exhibits excellent passivation qualities with iV_{OC} over 720 mV. The lower drop of passivation quality is observed for precursor with 5 nm i-a-Si:H.

After metallization (Ag screen printing for both front and rear sides). The external parameters measured cells (DIE 1) are demonstrated in Fig. 5.7.



Cells	τ_{eff} (ms)	iVoc (mV)
7 nm w/o	3.3	727
7 nm with	2.5	723
5 nm w/o	2.9	724
5 nm with	2.4	722

Figure 5.6 The minority carrier lifetime measurements of different i-a-Si:H thickness. The minority carrier lifetime is extracted at minority carrier density at 10^{15} cm^{-3}.

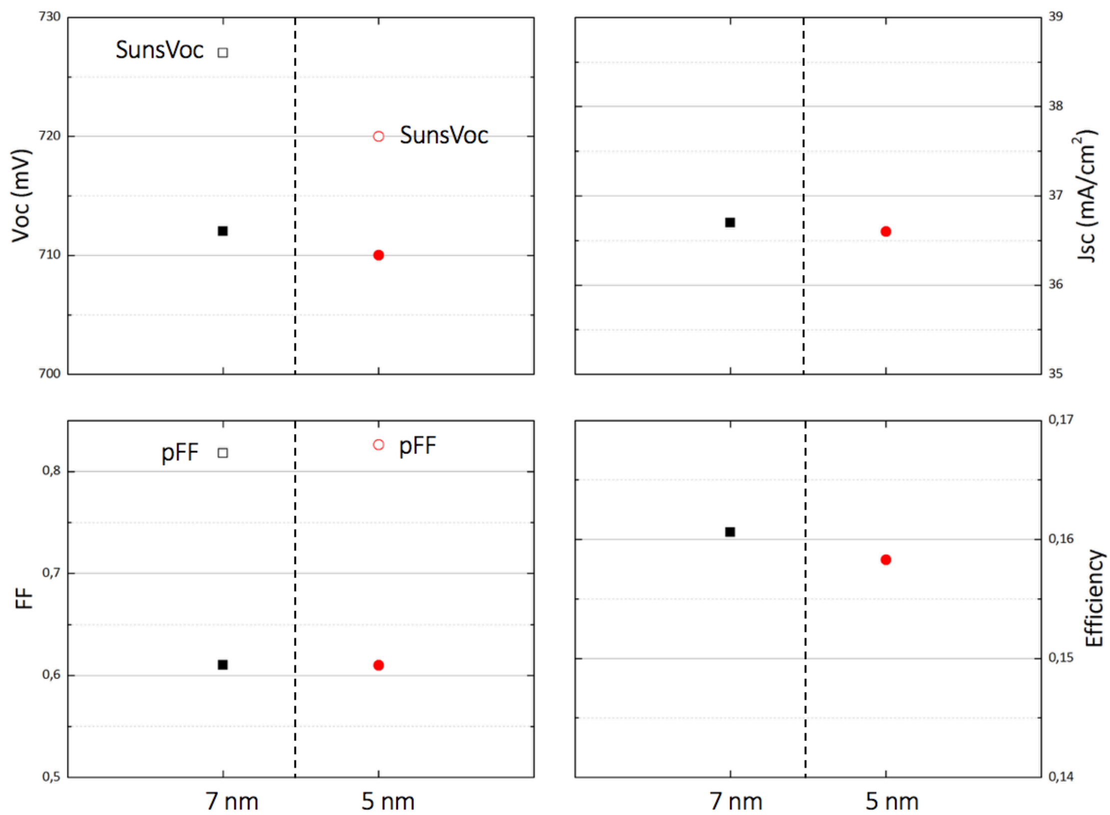


Figure 5.7 The external parameters for investigation of different i-a-Si:H thicknesses.

The V_{OC} of both cells are around 710 mV, while larger drop from SunsVoc is observed for the cell with 7 nm i-a-Si:H layer. This indicates a worse collection of minority charge carriers (detailed explanation can be found in the next section). Besides, slightly higher J_{SC} are obtained for thick i layer cell. Again, the significant loss of FF from pFF over 20% abs. is observed for both cells. The FF of both cell is same. Overall, since no obvious difference of external parameters between those two cells, the influence induced by the i-a-Si:H layer thicknesses within the test range is not obvious. However, further experiments should be designed for more sets of solar cells with different thickness of i-a-Si:H layers.

Therefore, the improvement of FF by thinning the i layer from 7 nm to 5 nm is negligible. Instead, in terms of better passivation quality, 7 nm i-a-Si:H layer is more favorable.

5.3.2 The Effect of Doped Layer Thickness

The thickness of doped nc-SiO_x:H layer can significantly influence the crystalline fraction of the layer, which is favorable for both forming good band bending at c-Si/i-a-Si:H interface and low-resistive doped nc-SiO_x:H/ITO contacts. Therefore, a decent FF is expected to be obtained if thicker layers are used. The investigation of influence induced by doped nc-SiO_x:H thickness is conducted and the solar cell structure is demonstrated in Fig. 5.8.

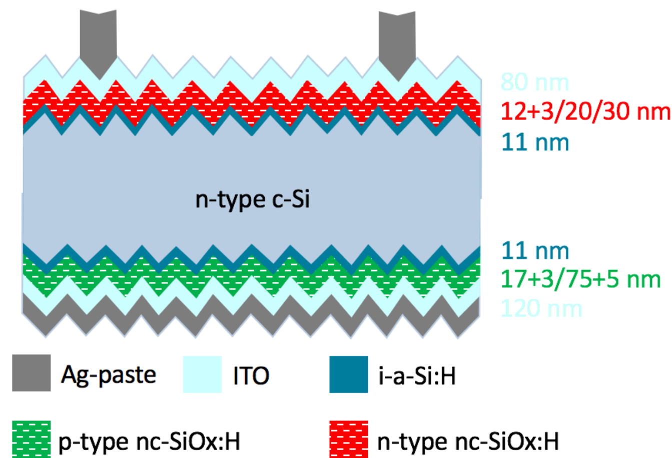


Figure 5.8 The solar cell structure with varying n- and p-type nc-SiO_x:H layer thickness.

5.3.2.1 n-type nc-SiO_x:H

The n-type nc-SiO_x:H thickness is set as 15 nm (12 + 3 nm), 20 nm and 30 nm while keeping the p-type nc-SiO_x:H layer as 20 nm (17 + 3 nm) and other layers as demonstrated in the figure Fig. 5.8. The precursor lifetime with excess minority carrier density before and after ITO sputtering are plotted in Fig. 5.9. No post annealing is conducted.

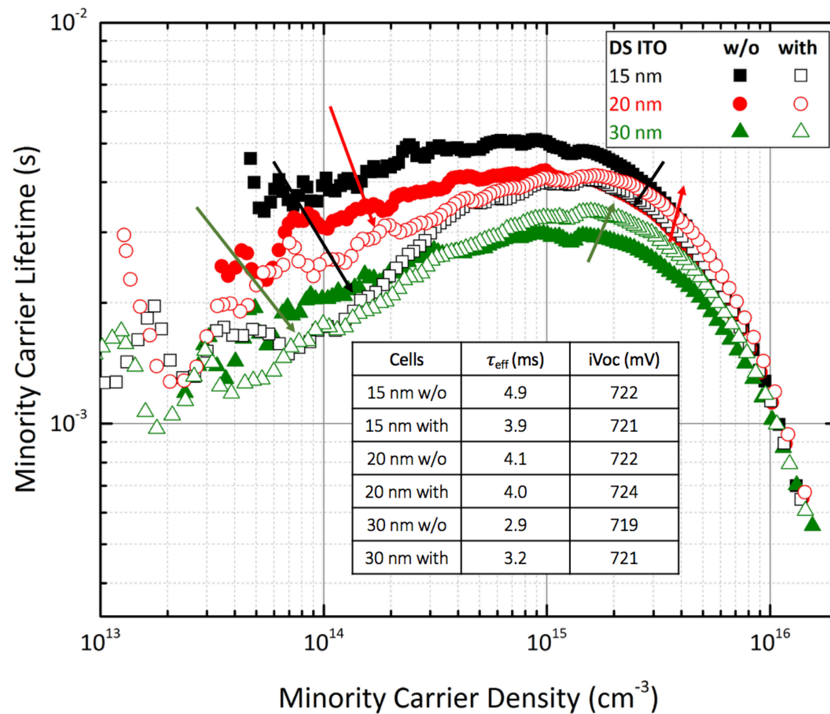


Figure 5.9 The minority carrier lifetime measurements of different n-type nc-SiO_x:H thickness. The minority carrier lifetime is extracted at minority carrier density of 10^{15} cm^{-3}.

As shown in Fig. 5.9, before the ITO deposition, the thinner the n layer the better the passivation of the precursor is presented. This is ascribed to deposition time (low deposition rate: 1 nm/min) that during the deposition degrades passivating effects of i-a-Si:H. In contrast, the expected damage form ITO deposition is less apparent for the thicker n layer precursor. The precursor with thinnest (15 nm) n layer presents degradations of both effective lifetime and iV_{OC}, while for precursors with 20 nm and 30 nm n layer, 2 mV improvement of iV_{OC} is measured. Although all three samples exhibit degradations at low injection level, the thicker n layer seems to shield more effectively the field effect from deposited ITO keeping the electron selectivity at c-Si/i-a-Si:H interface.

After metallization (Ag screen printing for front side and Ag thermal evaporation for rear side), the values of measured external parameters are demonstrated in Fig. 5.10. The 'DIE 3' of each wafer is used for comparison.

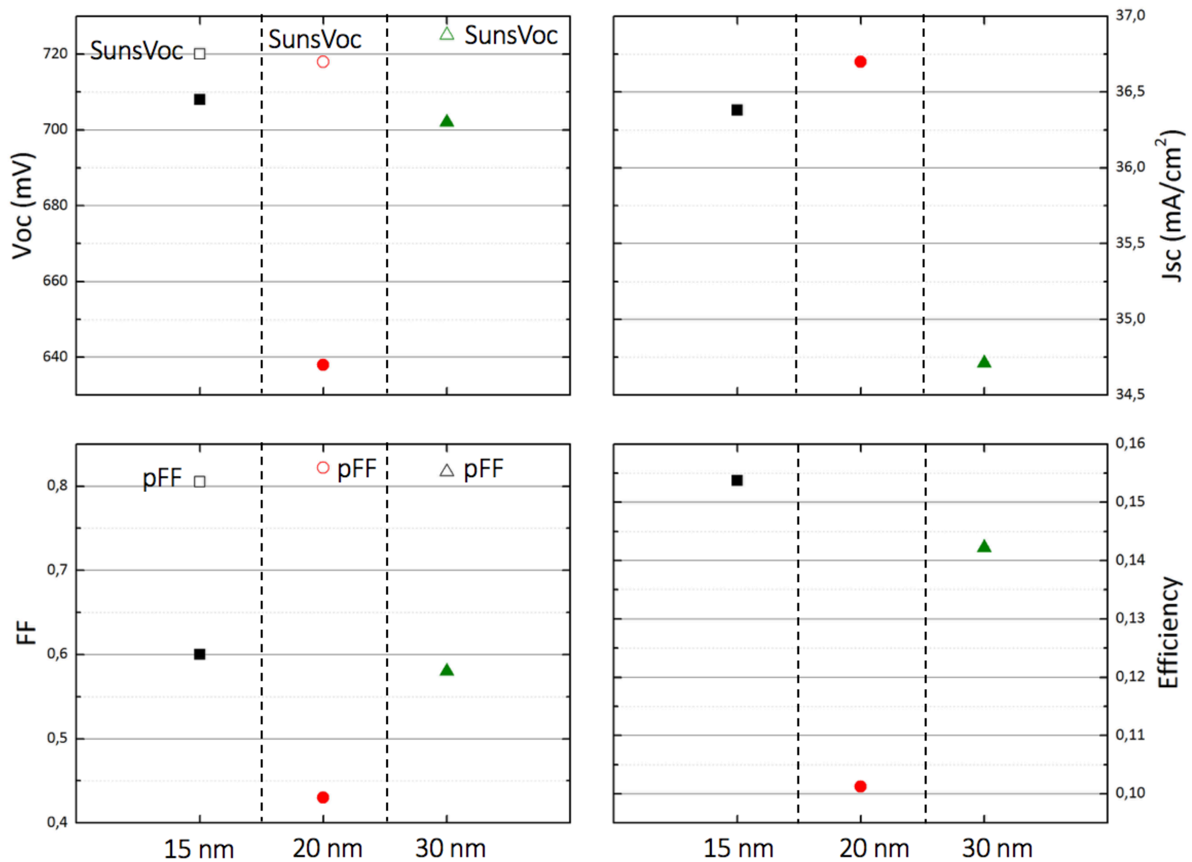


Figure 5.10 The external parameters for investigation of different n layer thicknesses.

It is essential to mention that the V_{OC} on 20 nm n layer sample is an experimental error during illuminated J-V measurement, since other cells on the same wafer exhibit V_{OC} around 703 mV. Therefore, further analysis is only based on cells with 15 nm and 30 nm n layer. Although the SunsVoc of both cells are over 720 mV, they suffer from large reductions from SunsVoc to device V_{OC} (12 mV and 23 mV). This gives a hint that the drop of SunsVoc in this case is not related to the n layer but the p layer, which will be investigated in next section. Besides, it is confirmed the thicker n layer on the front side, the more severe parasitic absorption can occur. By comparing the cells with 15 nm and 30 nm n layer, more than 1.5 mA/cm^2 current loss is presented. As for FF, although the 15 nm layer cell gives the highest FF of 0.60, it is similar to the cell with 35 nm n layer. This slight increment might according to the 3 nm highly doped n-type nc-Si:H is formed. Overall, the cell with thinnest n layer exhibits the highest efficiency (15.37%).

To sum up, thicker n layer can effectively reduce the ITO sputtering induced damage on passivation quality. Within the test range, the n-type nc-SiO_x:H layer thickness for the test structure is not the main reason for drop of SunsVoc to V_{OC}, the FF is not significantly influenced by the thickness either. Besides, increased parasitic absorption of thicker front n layer is exhibited. Lastly,

in terms of passivation, cell with 15 nm n-type nc-SiO_x:H is sufficient for achieving similar SunsVoc as cell with 35 nm n-type nc-SiO_x:H.

5.3.2.2 p-type nc-SiO_x:H

The thickness of p-type nc-SiO_X:H is expected to play an important role of minority carrier collection. Therefore, the p-type nc-SiO_x:H thickness is set as 20 nm (17 +3 nm) and 80 nm (75 + 5 nm) while keeping the n-type nc-SiO_x:H layer as 20 nm and other layers as demonstrated in the Fig. 5.7. The precursor lifetime with excess minority carrier density before and after ITO sputtering are plotted in Fig. 5.11. No post annealing is conducted.

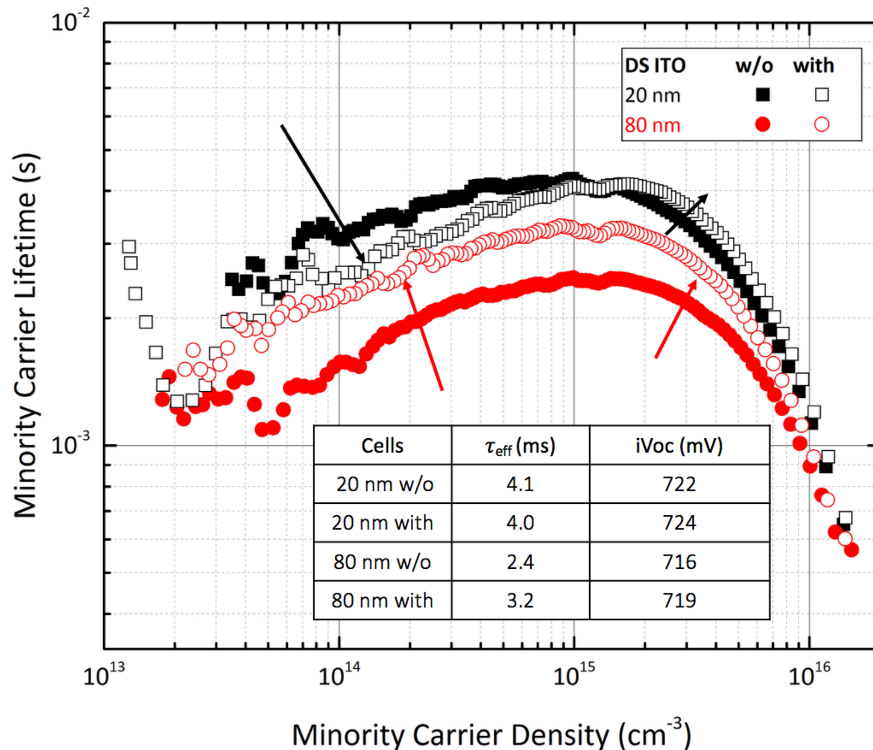


Figure 5.11 The minority carrier lifetime measurements of different p-type nc-SiO_x:H thickness. The minority carrier lifetime is extracted at minority carrier density of 10^{15} cm^{-3}.

As demonstrated Fig. 5.11, before ITO deposition, the precursor with thinner p layer has overall better passivation quality compared to thick p layer precursor. This can be explained by more than four times longer deposition time of p layer that increases the effusion (rupture of Si-H bonds) of hydrogen atom at c-Si/i-a-Si:H interface on the n layer side (since n layer is already deposited), thus lesser dangling bonds at the interface can be passivated. Besides, same as the low deposition rate of n-type nc-SiO_x:H layer, the passivation quality of i-a-Si:H layer can be possibly damaged.

After ITO deposition, although the precursor with thinner p layer shows increased chemical passivation (higher iV_{OC}), the reduced field effect passivation (low injection level) is observed. While both chemical passivation and field effect passivation is increased for thick p layer precursor,

since ITO acts as a capping layer and moderate temperature (120 °C) deposition temperature provides extra annealing, which enables the hydrogen atoms to passivate again the interfaces. Besides, the field effect provided by thick p layer is more resistant to ITO induced field effect. Thus, no degradation of the field effect passivation is observed.

After metallization (Ag screen printing for front side and Ag thermal evaporation for rear side), the values of measured external parameters are demonstrated below (DIE 2).

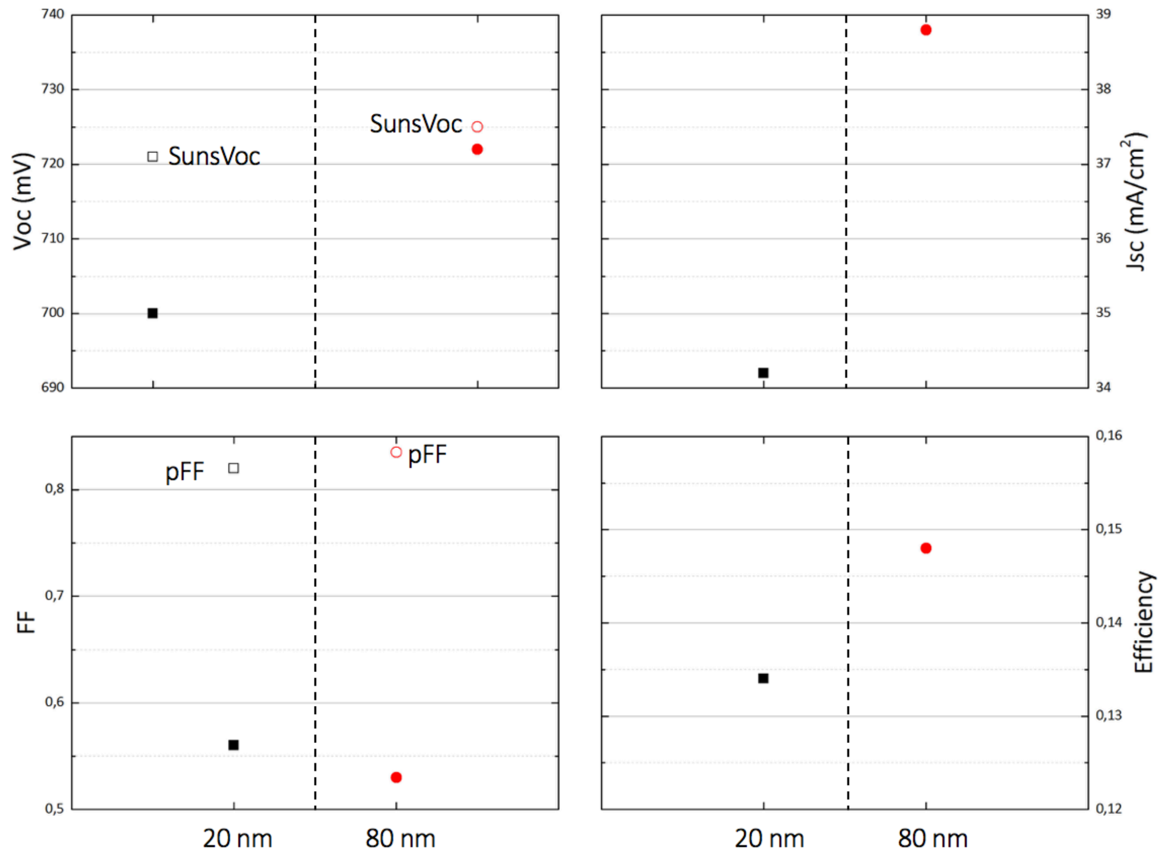


Figure 5.12 The external parameters for investigation of different p layer thicknesses.

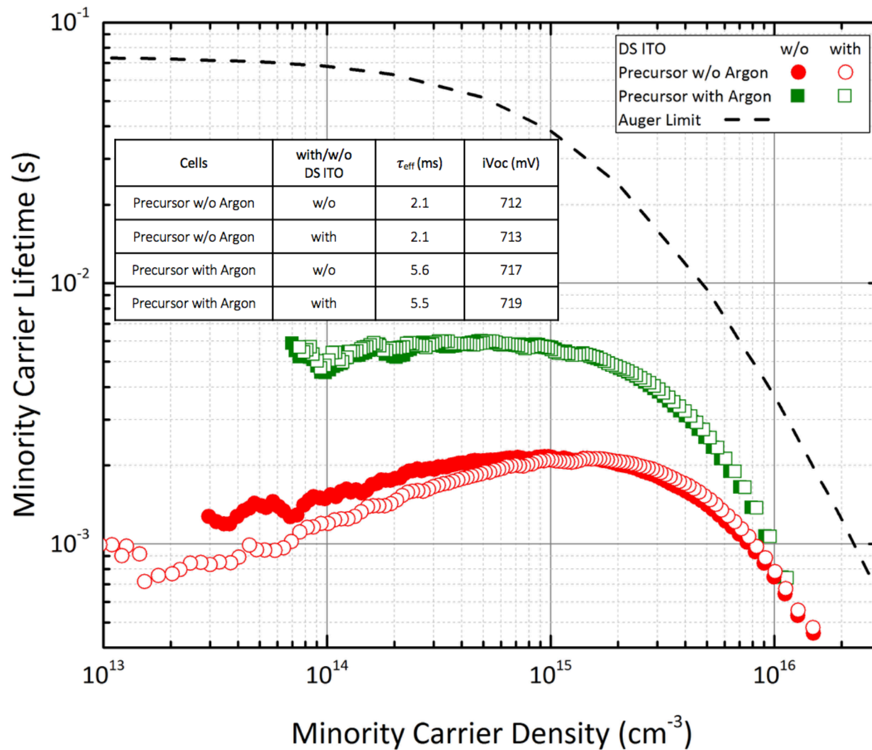
As shown in Fig. 5.12, although similar values of SunsVoc are measured for both cells, the cell with thick p layer reaches V_{OC} of 722 mV, which is 22 mV higher than the cell with thin p layer. Therefore, the much lower difference between the SunsVoc and V_{OC} for thick p layer cell (only 3 mV) compared to thin p layer cell (around 20 mV) indicates the better minority carrier collection. This is ascribed to higher doping efficiency or higher crystalline fraction that is achieved for thick p layer. With this observation, the always existed large drop from SunsVoc to V_{OC} for investigation of n layer thickness can be explained, which also applies to investigation of i-a-Si:H layer. The significant increase of J_{SC} for thick p layer cell can be attributed to either enhanced internal reflection of light or inaccurate shading during the measurement. Although cell with thinner p layer has 3% abs. higher FF, generally, low FF (below 60%) is observed for both cells. Since p/ITO

contact is formed with highly doped p-type nc-Si:H/ITO, which indicates the resistive collection of majority carriers limits the FF, i.e., the n-type nc-SiO_x:H layer or n-type nc-SiO_x:H/ITO contact.

To sum up, the thicker p layer can effectively shield the filed effect and damage induced by ITO sputtering. The cell with thicker p layer exhibit smaller difference between SunsVoc and V_{OC}, which is attributed to better minority carrier collection. Besides, the cell with thinner p layer has higher measured FF. But FF is still not significantly influenced by thickness of p layer, which suggests the low FF originates from n-type nc-SiO_x:H layer or n-type nc-SiO_x:H/ITO contact.

5.3.2.3 Combination of both thick n- and p-type nc-SiO_x:H layers

As suspected resistive transport of electrons at n-type nc-SiO_x:H layer side (including ITO contact), thick n layer (80 nm: 70+10 nm) is applied for increasing the conductivity. In combination with the advantages of thick p-type nc-SiO_x:H (80 nm: 75 +5 nm) layer, the cell is expected to have excellent charge carrier selective transport. The structure of the cell is same as demonstrated in Fig. 5.4 except the thickness of n- and p-type nc-SiO_x:H layers and i-a-Si:H (11 nm). The precursor lifetime with excess minority carrier density before and after ITO sputtering are plotted below.



Cells	with/w/o DS ITO	τ_{eff} (ms)	iVoc (mV)
Precursor w/o Argon	w/o	2.1	712
Precursor w/o Argon	with	2.1	713
Precursor with Argon	w/o	5.6	717
Precursor with Argon	with	5.5	719

Figure 5.13 The minority carrier lifetime measurements of precursor with thick n and p layers. The minority carrier lifetime is extracted at minority carrier density of 10^{15} cm^{-3}. No post annealing.

As shown in Fig. 5.13, the precursor with Argon means during the growth of n-type nc-SiO_x:H layer, an argon flow of around 20 sccm is added for first half of the deposition. For both precursors, the thick layers on both sides provide sufficient protection from the ITO induced field effect and

damage, increased iV_{OC} is measured. It is worth noting that the precursor with argon exhibits excellent passivation qualities for both before and after ITO deposition. Different from lifetime curve of precursor without argon, the precursor with argon demonstrates relatively flat lifetime curve at injection level below 10^{15} cm^{-3}, which indicates the enhanced field effect passivation. Besides, improvement of high injection level clearly states improved chemical passivation with argon plasma. However, compared to the calculated Auger limit based on [96], which reflects the effective lifetime upper limit based on only intrinsic recombination, more efforts are needed on further improving the passivation quality.

The results of SunsVoc measurements of PVMD precursor (with argon) and cell are demonstrated below together with that of Kaneka 26.6% HJ-IBC cell in Table 5.3.

Table 5.3 The SunsVoc measurement of PVMD precursor and Kaneka 26.6% HJ-IBC cell.

Sample	SunsVoc (mV)	pFF (-)	Wafer Thickness (μm)
PVMD precursor	727	0.862	280 (before manufacture)
PVMD cell (metallized)	734	0.841	280 (before manufacture)
Kaneka 26.6% HJ-IBC [7]	740	0.858	200 (after manufacture)

As compared Table 5.3, the PVMD precursor shows an excellent pFF of 0.862 which indicates the outstanding junction formation at both sides of c-Si/i-a-Si:H interface. After metallization, the PVMD cell exhibits 7 mV increment of SunsVoc, reaching 734 mV for 280 μm thick wafer, which is expected to have around 740 mV if 200 μm thick wafer is used. Therefore, this is also a remarkable step in terms of passivation. The improved passivation quality after metallization is attributed to the one hour curing under 170 °C during Ag screen printing.

Since the precursor is very promising, it is made as front emitter cell. This is because the full area metal coverage at rear side helps the collection of electrons from suspected 'bad' n-type layers, so only '1-D' current flow from absorber to the metal electrode. While thick enough p-type nc-SiO_x:H layer at front side is expected to have low-resistive transport, which is less strict on the front ITO properties (conductivity and thickness) even though the hole collection is '2-D' like (lateral transport is needed). The precursor without argon is made as rear emitter cell. Different emitter designs are introduced in the following section. The best results (same cell design) of illuminated J-V measurements are listed below in Table 5.4.

Table 5.4 The external parameters of the cells with both thick n- and p-type layers (DIE 2).

Sample	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)
cell with argon (font emitter)	31.48	727	0.57	13.08
cell w/o argon (rear emitter)	33.31	716	0.54	12.77

As demonstrated Table 5.4, the argon plasma induced improvement of V_{OC} is more than 10 mV. This can be explained by the effect of post argon plasma treatment to the i-a-Si:H layer as reported in [91], since no improved passivation quality is observed from symmetrical passivation tests which use argon plasma during the layer growth. The best V_{OC} obtained for cell with argon reaches 729 mV. Higher J_{SC} for rear emitter cell is mainly according to larger bandgap of the n-type layer compared to p-type layer. Besides, referring to Table 4.15, the argon plasma deteriorates the conductivity of n-type nc-SiO_x:H layer, which explains no observation of expected high FF from thick layers. Since low FF is also observed for cell without argon plasma, therefore, the FF problem can potentially come from either the n-type nc-SiO_x:H layer and its contact with ITO or the p-type nc-SiOx:H/ITO contact.

To sum up, it is confirmed that thick layers on both sides can effectively shield the effect from ITO, meanwhile, sample with additional argon plasma during growth of n layer can significantly improve the passivation quality. However, the FF problem still exists. To identify the origin of the FF problem, further experiments are necessary.

5.3.3 The investigation of Doped Layer Combination

With the view to check either the FF problem comes from n- or p-type layer, cells with different emitter designs, i.e. front emitter and rear emitter, along with different combination of doped layers are conducted to identify the origin of the FF problem. Firstly, the characteristics of different emitter designs are introduced as follows (assume n-type c-Si substrate):

- Front emitter: collection of holes in front metal grid includes lateral transport within the emitter and front TCO, which requires the good electrical properties of both the emitter and the TCO; however, front layer stack determines the how severe is the parasitic absorption. For ITO, there is tradeoff of transparency and conductivity. Thus, to enable effective collection of holes, the optimization of ITO should be carefully conducted. Same applies to the emitter. The advantage of this design is that it allows the effective collection of the low mobility holes due to stronger field effect at front side.
- Rear emitter: the collection of holes becomes more '1-D' like according to full metal coverage at rear side. Besides, as reported in [97], a large fraction of lateral transport at

front side for electrons collection occurs at low-resistive n-type c-Si substrate rather than in TCO. Therefore, transparency of the front TCO is more dominant compared to its electrical conductivity. Within the thesis, high quality FZ wafer used to ensure the sufficient minority carrier collection.

Based on studies from previous sections, the n-type nc-SiO_x:H layer and its contact with ITO are suspected to be the main reasons for the loss of FF. Meanwhile, since excellent conductivity p-type nc-SiO_x:H is measured, the front emitter design is firstly applied.

Two front emitter cells are manufactured. The structure is similar to that shown in Fig. 5.5, the thickness of i-a-Si:H layer is fixed at 5 nm on both sides. One (Cell A) of them has the p layer consists of 3 + 10 nm, n layer consists only the nc-SiO_x:H; while the other cell (Cell B) has extra 2 nm p- and n-type a-Si:H on top of corresponding doped nc-SiO_x:H layers. The measured best results from SunsVoc and illuminated J-V setup in term of FF are listed below.

Table 5.5 The results of front emitter cells for investigating the FF.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Cell A	2	34.52	709	0.65	15.91	727	0.814
Cell B	2	33.23	703	0.72	16.82	722	0.804

As summarized in Table 5.5, the additional 2 nm doped a-Si:H layers on both sides leads to an increase of FF for 7% abs. This indicates at least one of doped layers forming poor contact with ITO. The large drop of SunsVoc to V_{OC} indicates the doping of this p layer combination is insufficient (no strong band bending from 3 nm p-type nc-SiO_x:H). Although this is promising, according to the measured poor TCO conductivity (not optimized) from four-point-probe (4PP) sheet resistance measurement and limited time, no further investigation based on this method is conducted.

Instead, three rear emitter cells which enable less strict requirements on front ITO are manufactured. In order to reduce the front parasitic absorption, the first cell (Cell C) is manufactured with front layer stack with only 7 nm n-type nc-SiO_x:H and 7 nm i-a-Si:H, while for forming sufficient minority carrier collection (based on above Cell A), p layer stack is slightly thicker and consists of 7 + 15 nm. Besides, with consideration of too thin (resistive) the n layer is formed on the front sides, another cell (Cell D) is designed consisting n-type layer stack with 12 + 3 nm (based on Fig. 5.10) which is for better contact formation, while having rear side of p-type layer with 12 + 3 nm. The last cell (Cell E), which has same rear design as Cell C but replacing the front side n/ITO contact by the p/ITO contact, the structure is

demonstrated in Fig. 6.15 (left), this is so-called tunneling FBC-SHJ solar cell. The best cells' results in terms of FF are demonstrated below in Table 5.6.

Table 5.6 The results of rear emitter cells for investigating the FF.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Cell C	2	36.4	707	0.55	14.13	712	0.83
Cell D	2	35.8	710	0.73	18.56	717	0.81
Cell E	2	30.0	694	0.73	15.13	706	0.81

By comparing Cell C and Cell E, an improved of FF of 18% abs. is measured by replacing only the front n/ITO contact to p/ITO contact. This clearly states the n/ITO contact and/or n layer itself are/is limiting the FF.

By comparing Cell C and Cell D, although Cell D has even thinner rear p layer stack, the same 18% abs. of FF increment can be observed. This is mainly due to better contact formation at front n contact, because thicker n-type nc-SiO_x:H layer and additional nc-Si:H layer are applied. Besides, it is worth noting that a 3% abs. FF difference can be observed for the same measured cell (probably due to insufficient thickness of metal grid), i.e. 3% abs. FF improvement can be obtained if the probe is measuring the middle of busbar. Therefore, the arm of the probe can result in small area shading during the measurement, which eventually underestimates the J_{SC}. In fact, same J_{SC} is obtained for Cell C and Cell D if there is no shading during measurement (36.8 mA/cm^2). Thus, there is nearly no excess parasitic absorption for front n layer stack with 12 + 3 nm compared to only 7 nm nc-SiO_x:H. Lastly, the difference between SunsVoc to V_{OC} for Cell C is 2 mV smaller than Cell D, this indicates it is possible to reduce the gap if thicker rear p layer is applied for Cell D.

To sum up, n-type nc-SiO_x:H layer itself and n-type nc-SiO_x:H/ITO contact are the main limiting factors for FF reaching 73%. Instead, the combination of 12 + 3 nm n layer stack plays a critical role for not only the improvement of the FF, but also transparent enough for obtaining nice current. By optimizing the rear p layer thickness and the combination of nc-SiO_x:H and nc-Si:H, the higher V_{OC} for Cell D is achievable without reducing the FF.

Further, the EQE measurement of the Cell D is conducted. The EQE results in combination of reflectance measurement and illuminated J-V measurement are plotted in Fig. 5.14. Besides, another cell (Cell F) from the same wafer of Cell D which has a better efficiency is presented in Table 5.7.

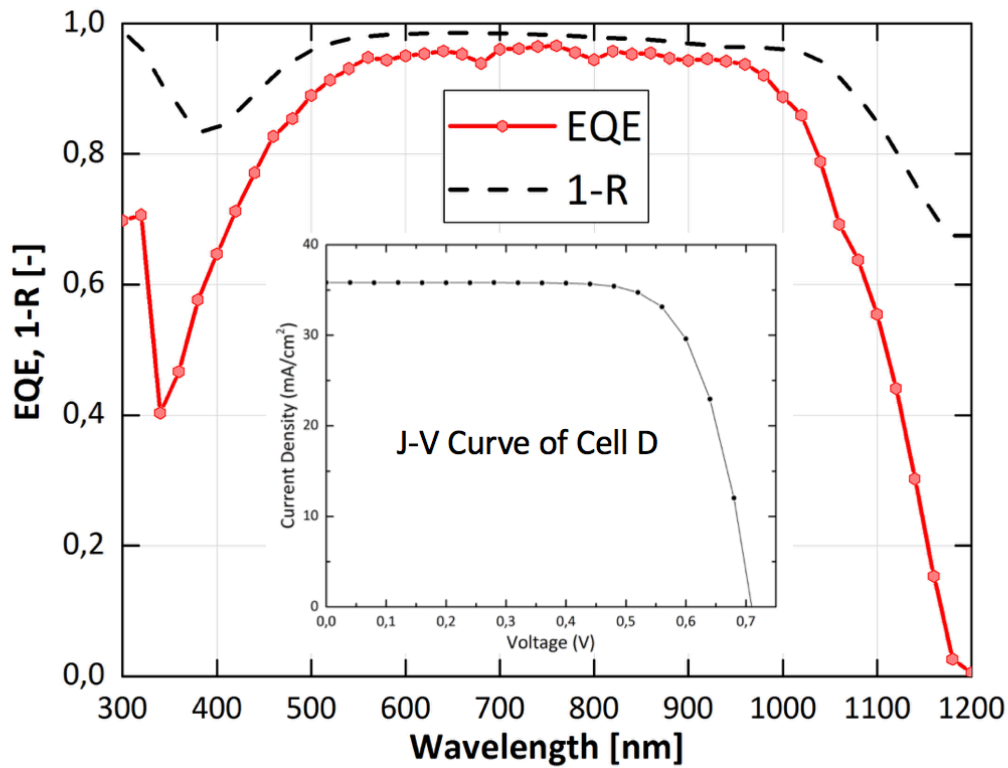


Figure 5.14 The EQE and J-V curve of Cell D. The measured $J_{SC,EQE}$ equals to 39.4 mA/cm^2.

Table 5.7 The external parameters of best manufactured FBC-SHJ solar cells.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	$J_{SC,EQE}$ (mA/cm^2)	η_{EQE} (%)
Cell D	2	35.8	710	0.73	18.56	39.4	20.42
Cell F	1	38.4	711	0.685	18.70	39.4	19.19

After achieving FF of 73%, the potential limitation for the non-optimized n-type nc-SiO_x:H layer and its contact on FF is further investigated by implementing the hybrid cell design with doped polysilicon contacts.

5.3.4 The Investigation of Hybrid Cell Design

The design of the hybrid cell is demonstrated below in Fig 5.15. In order to check the potential limitation of n layer stack on FF, the wet-chemical ultra-thin tunneling oxide (around 1.5 nm [98]) and n-type polysilicon are applied as BSF. The front p layer stack is same as that of Cell D. The Ag thermal evaporation is used for metallization of both sides.

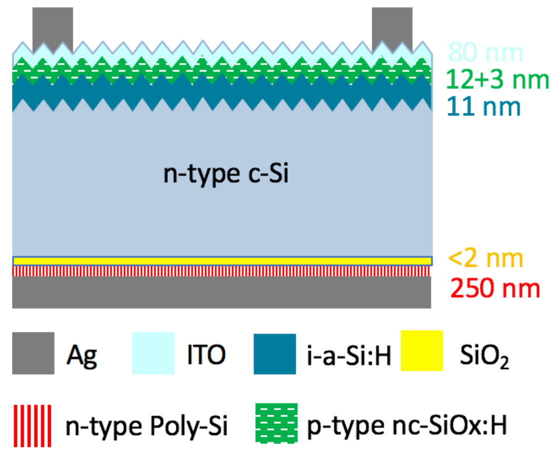


Figure 5.15 The hybrid solar cell structure for checking potential limitation of n-type nc-SiO_x:H layer stack and its contact.

The best measured external parameters are demonstrated below in Table 5.8, a further 3% abs. FF improvement is observed. Therefore, if the optimized n-type nc-SiO_x:H layer stack and its contact are applied for the same structure of Cell D, FF improvement should be expected. Besides, in the Hybrid structure, thinner ITO (less conductive) that is in contact with p-type layer stack, which probably forms a more resistive tunneling recombination junction. While in the case of Cell D, since the emitter is at the rear side, there are lesser restrictions on the ITO and the p layer stack.

Table 5.8 The measured external parameters of the hybrid solar cell with n-type polysilicon.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	$J_{SC,EQE}$ (mA/cm^2)	η_{EQE} (%)
Hybrid n-poly-Si	2	34.1	688	0.76	17.83	38.4	20.08

Another hybrid structure which uses p-type polysilicon and n-type nc-SiO_x:H layer stack is also tested. Since the quality of p-type polysilicon is not good, in combination with non-optimized n-type nc-SiO_x:H layer stack, the FF can only reach 71%. Therefore, the p-type nc-SiOx:H layer stack used in Cell D is better than p-type polysilicon in terms of passivation and minority carrier collection.

In parallel, the 12 nm n-type a-Si:H is also applied to replace the 20 nm n-type nc-SiO_x:H layer. The test structures are same as that of Fig 5.8, where rear p-type layer stack is 17 + 3 nm. The best results from both structures are demonstrate below in Table 5.9. The 'reference' sample is cell with 25 nm n-type nc-SiO_x:H layer.

Table 5.9 The measured external parameters of the hybrid solar cell with n-type a-Si:H.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Hybrid n-a-Si:H	2	33.5	702	0.63	14.82	720	0.822
Reference	2	34.2	700	0.56	13.41	721	0.820

As listed Table 5.9, the hybrid cell has 7% abs. FF improvement over the reference cell. This again points out the n-type nc-SiO_x:H is not optimized, since same ITO layer are applied for both cells. Higher J_{SC} for the reference cell is due to more transparent nc-SiO_x:H layer at the front side even if its thickness is almost doubled compared to n-a-Si:H.

To sum up, results of both hybrid solar cells suggest that the FF can be improved by replacing n-type nc-SiO_x:H by either n-type polysilicon or a-Si:H layer, i.e. the n-type nc-SiO_x:H layer needs further optimization in terms of conductivity.

5.4 FBC-SHJ Solar Cells with Doped a-Si:H layers

In parallel with previous investigations of FF improvement, the FBC-SHJ solar cells with doped a-Si:H layers are manufactured as well. The solar cell structures are demonstrated in Fig. 5.16.

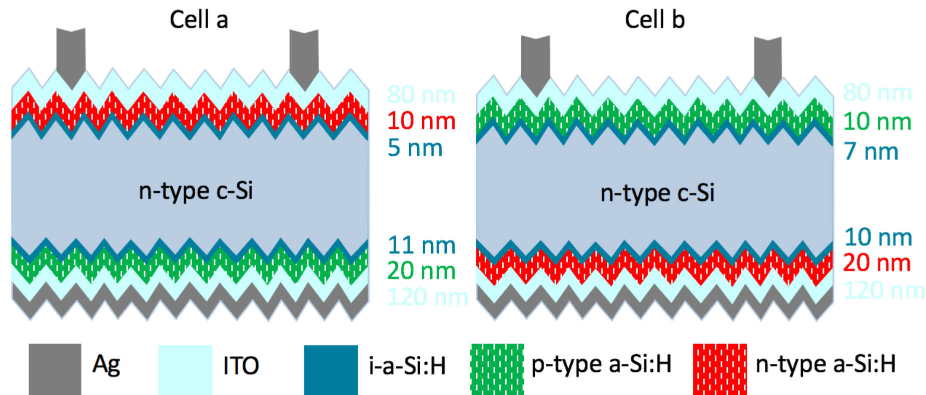


Figure 5.16 The structures of FBC-SHJ solar cells with doped a-Si:H layers.

Table 5.10 The external parameters of a-Si:H FBC-SHJ solar cells.

Sample	DIE	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Cell a	2	33.6	696	0.67	15.68	709	0.800
Cell b	2	32.2	680	0.69	15.11	694	0.792

All cells have Ag screen printing for front side and Ag thermal evaporation for rear side. The measured external parameters are listed above in Table 5.10. Better V_{OC} obtained for Cell a is mainly according to thicker i-a-Si:H layer beneath the p-a-Si:H layer, but still much lower compared to passivation quality of nc-SiO_x:H layers. Since p-a-Si:H layer is mainly optimized in terms of passivation quality, the obtained FF for both cells are limited by its low conductivity. It also explains the large ΔV_{OC} of both cells (around 14 mV). According to limited time, no deep investigation is conducted further. Further optimization of both p type and n type layers and their contact with ITO are expected to significantly improve the FF. Lastly, by comparing the FF of hybrid cell with n-type a-Si:H (63%) and Cell a (67%), optimization of p-type nc-SiO_x:H/ITO contact is also necessary for eventually reaching high FF.

5.5 Summary

By applying the optimized passivation contact stacks into FBC-SHJ solar cells, the V_{OC} and FF limiting factors are investigated. An efficiency of 20.42% is reached for FBC-SHJ solar cell. Further optimization of n-type nc-SiO_x:H layer and ITO are apparent for continuous improving the FF. Besides, thicker p-type layer stack can be applied on the rear side for enhancing the device V_{OC}, but a tradeoff between FF and V_{OC} is expected. Since p-type nc-SiO_x:H layer is already optimized in terms of passivation and conductivity, more attentions should be paid to optimization of ITO, or its contact with ITO. The better conductivity and transparency are required for achieving better FF and J_{SC}, respectively. The evaluation of n-type nc-SiO_x:H/ITO interface and p-type nc-SiO_x:H are also important for further optimizing the lossless contacts.

6

MANUFACTURE OF IBC-SHJ SOLAR CELL

The Manufacture process of IBC-SHJ solar cell is the main topic of this chapter. The brief introduction of common technologies to pattern IBC-SHJ solar cells are firstly given in section 6.1. Afterward, two different approaches for patterning the thin-film silicon layers for IBC-SHJ solar cell manufacture process are introduced and explained. In section 6.2, the problems that occurred during the manufacture of IBC-SHJ solar cells with the previously developed lift-off approach are listed. In section 6.3, a very time-effective way for fabricating tunneling IBC-SHJ solar cells is proposed and realized.

6.1 Patterning Technologies for IBC-SHJ Solar Cells

As demonstrated in Fig. 1.7, all contacts are patterned on the rear side of the c-Si substrate and it is extremely critical for precisely patterning of those contacts to ensure excellent carrier collection. The main technologies used for patterning of IBC-SHJ solar cells are introduced as follows:

- **Photolithography**: The most precise (small feature size: < 1 μm) contact formation among all three technologies [15]. It is normally combined with wet-chemical etching or dry-etching as mentioned in [10] to form desired pattern of BSF and emitter. However, photolithography is expensive, etching process is risky and time-inefficient.
- **Shadow Masking**: The cheapest and easiest way to apply the desired pattern (openings) on the mask to the samples. However, it suffers from the thickness control of deposited layer closing the edge of the mask [99] and very large feature size (< 100 μm). Besides, alignment of hard mask is also challenging [15].
- **Inkjet Printing**: Inkjet printing is developed with the demand for massive production. Varies microstructuring applications with this technology can be found in [100]. Inkjet printing is a cheaper way for forming desired pattern compared to photolithography, but wet-chemical process is still needed. One example can be found in [14], where the technology is used for patterning ITO/metal electrodes. Nevertheless, this technology suffers from large feature size (< 50 μm) [15].

Besides these technologies, laser based patterning [22], [101], [102] is also emerging. Since photolithography tools are currently available in EKL and they can realize the precise patterning of rear contacts, photolithography technology is chosen for this thesis.

6.2 Manufacture Process of Lift-offed IBC-SHJ Solar Cell

The manufacture processes of Lift-offed IBC-SHJ solar cells with flat and textured rear side are separately introduced, the limiting factors of the process are pointed out and analyzed.

6.2.1 *Flat-rear IBC-SHJ Solar Cell*

6.2.1.1 Manufacture Process on Flat-rear IBC-SHJ Solar Cell

The first working lift-offed IBC-SHJ solar cell in PVMD group is manufactured by the previous master student Jiali Zhou [89]. This approach used Jiali's thesis used as the reference method for manufacture of IBC-SHJ solar cells in this thesis. The schematic demonstration of the process is presented below in Fig. 6.1.

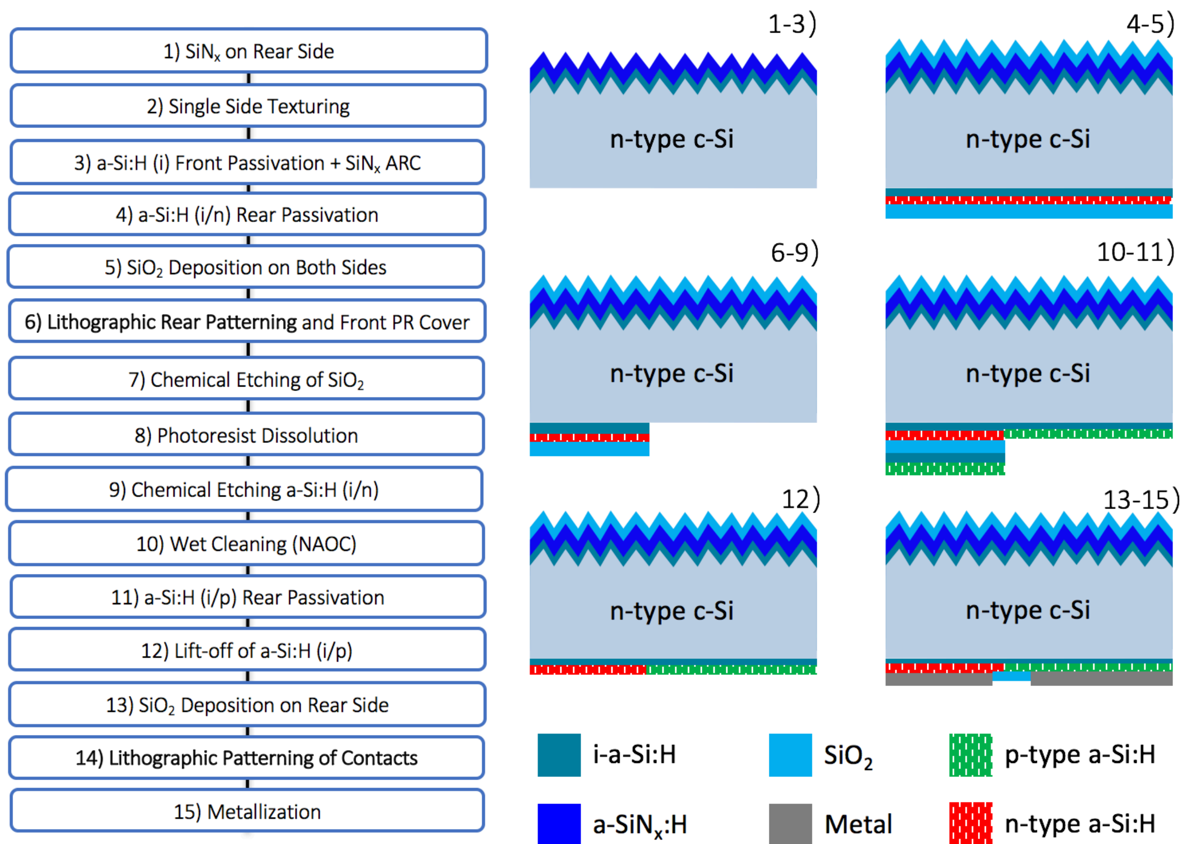


Figure 6.1 Schematic flowchart of flat-rear lift-offed IBC-SHJ solar cell manufacture with doped a-Si:H layers. Structures are not scaled according to the practical case.

As demonstrated in Fig. 6.1, the case of doped a-Si:H layers used as the passivating contacts is taken as an example. The double-side polished FZ <100> n-type c-Si substrate is firstly covered

with SiN_x (400 °C) on one side firstly by PECVD. Afterward, the wafer is dipped into TMAH solution for single side texture, because SiNx layer can be used as a protective layer against TMAH solution. Then it is followed by 3 times of NAOC standard cleaning procedure and load into PECVD in Kavli for i-a-Si:H (250 °C) for front side passivation and SiN_x (400 °C) for passivation (providing atomic hydrogen) and ARC. After the front side depositions (till step 3) in Fig. 6.1), the wafer is cleaned again with 3 times of NAOC standard cleaning procedure and loaded into either Amor or Amigo for rear side i/n-a-Si:H (180 °C). Later, the wafer is transferred back to PECVD in Kavli for SiO_2 (150 °C) depositions on both sides of the wafer (around 2 μm) (step 5) in Fig. 6.1). The SiO_2 layer deposited on the front surface is used as a protective layer for SiN_x during the following chemical etching processes. The SiO_2 layer on the rear side is mainly prepared for liftoff process and protection of BSF during polyetch.

Afterward, at step 6), the first photolithography patterning is applied to open the emitter area (positive resist). Meanwhile, the front side is covered with photoresist, which gives more flexibility of the following etching of SiO_2 on the emitter area by 0.55 % HF solution. With the observance of hydrophobic on the emitter area (a-Si:H is hydrophobic) at step 7), the wafer is ready to be dipped into polyetch etching for few seconds to remove i/n a-Si:H on the emitter area. Before the polyetch dipping, the photoresist left on both rear and front side should be removed by acetone. Until finishing step 9), the emitter area is ready to be deposited with i/p a-Si:H silicon layers. It is worth noting that pin holes formed on SiO_2 during polyetch dipping are critical for successful liftoff [89] and sufficient oxide left on the BSF area is also essential for successful liftoff. Subsequently, full area i/p a-Si:H layer stack is deposited. It is followed by liftoff process, which removes the i/p a-Si:H on the BSF by etching the SiO_2 beneath.

Eventually, the second photolithography patterning is applied for metallization. Before this step, SiO_2 is again deposited around 200 nm on the rear side to kind of passivate the emitter and BSF that are not been covered by metal electrodes.

To sum up, this method requires two times of photolithography steps for opening the emitter area and metallization. The critical steps for successful manufacture of a working device are chemical etching of i/n a-Si:H on the emitter area and liftoff for removing i/p a-Si:H on BSF. In other words, the thickness of SiO_2 on both sides are required to be thick enough to ensure the realization of previous two critical steps.

6.2.1.2 The Limiting Factors of the Lift-off Process

This section mainly describes the challenges found during the first trial of the above-mentioned lift-off process.

Passivation Quality

Since the surface passivation of a-Si:H layers within this thesis are optimized only on textured surfaces, the passivation of the optimized i-a-Si:H is firstly tested on flat surface. However, with expected 9 nm i-a-Si:H symmetrically deposited on flat c-Si substrate, the lifetime only reaches 566 μs with an iV_{OC} of 670 mV. This inferior passivation quality is not used for the SHJ-IBC cells manufacture process. The reasons for such low passivation quality could be: 1). Thinner layer deposited on the <100> flat surface than that on the pyramid facets of the textured Si. This is examined by measuring with SE, which indicates only less than 5 nm i-a-Si:H layer is deposited on the <100> flat surface. The lower deposition rate on the <100> flat surface than that on the textured surface is mainly attributed to the high hydrogen dilution ratio induced lower landing rate of the ion particles and/or higher etching rate of the landed ion particles on the flat surface; 2). The deposition parameters are not optimized for <100> surface, especially when, comparing to the passivation quality of 6 nm i-a-Si:H layer passivated textured surface, which gives over 3300 μs with an iV_{OC} of 722 mV.

The solution for this low deposition rate is to use the so-called 'double i layer' strategy. In this strategy, the first 3 nm of a-Si:H layer is deposited with pure silane (w/o H_2 dilution) is used as a seed layer, then on top of which, the optimized i-a-Si:H is applied. The pure silane layer is for growing as a seed layer, further hydrogen can penetrate to the c-Si/i-a-Si:H interface during the hydrogen diluted deposition and post-annealing in H_2 rich atmosphere. In total 9 nm i-a-Si:H layer is deposited with this strategy, lifetime and iV_{OC} improves to 927 μs and 695 mV, respectively. The deposition conditions of two different methods are listed in the Table 6.1.

Table 6.1 Comparison of deposition parameters of i-a-Si:H layer on <100> c-Si surface.

Layers	H_2 Dilution Ratio (-)	$T_{substrate}$ (°C)	$P_{deposition}$ (mbar)	Power (W)	SiH_4 (sccm)	H2 (sccm)
'Optimized' i-a-Si:H	3	180	1.4	3.2	10	30
'Double i Layer'	0	180	0.7	2.7	40	0
	3	180	1.4	3.2	10	30

The passivation quality from 'double i layer' deposition is still far below the achieved passivation on textured surfaces. According to limited time, the optimization on the <100> c-Si surface is not investigated further.

Additionally, till step 4) in Fig. 6.1, the structure with font side i-a-Si:H (5 nm)/SiNx (300 nm) passivation stack (from Kavli) and rear side 'double i layer' (9nm)/n-a-Si:H (15 nm) stack presents a lifetime of only 1046 μs and iV_{OC} of 694 mV. These low values again prove that passivation quality is a limiting factor of manufacture high efficient cell with the lift-off process.

Photoresist Leftover

During step 7), the 2 μm SiO_2 is etched by 0.55 % HF for around 13 minutes. Till the emitter area becomes hydrophobic, the sample is checked under the optical microscope. However, small strips can be found on the emitter area (left, in Fig. 6.2), which is supposed to be completely cleaned. With the following acetone dip, the small strips are removed. Therefore, the small strips left on the emitter area as shown in Fig. 6.2 is photoresist.

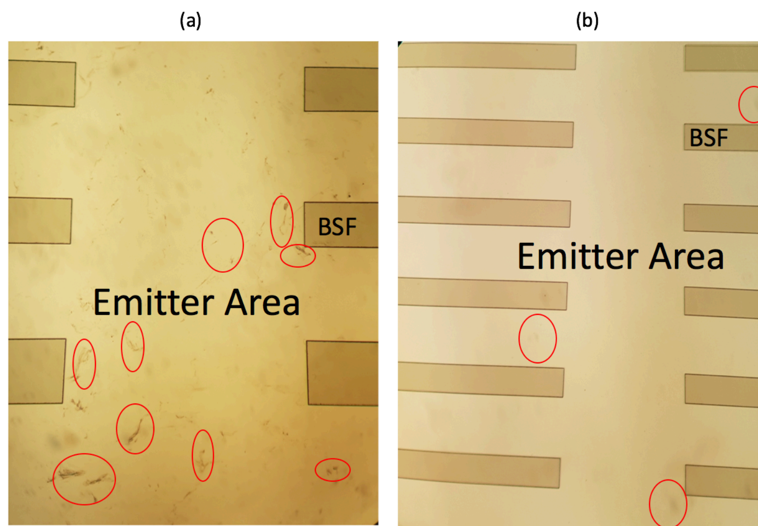


Figure 6.2 The indication of photoresist remaining under the observation of optical microscope: a). After etching in HF, with 10 minutes baking after development (left); b). After 17 minutes baking under 105°C in air (right), still some leftover can be found on the right bottom corner.

Since the development in step 6) is carefully checked and no photoresist is left on the opened emitter area. Therefore, the existence of photoresist leftovers is due to the etching process. The speculated reason for this phenomenon is drawn below. As illustrated below, the insufficient baking of photoresist leads to its falling off from the edge if there is no SiO_2 left beneath. However, as shown in Fig. 6.2, a longer time of baking photoresist is tried, which basically solves the problem, but still some photoresist can be found on emitter area. The schematic illustration of HF etching step is shown in Fig. 6.3.

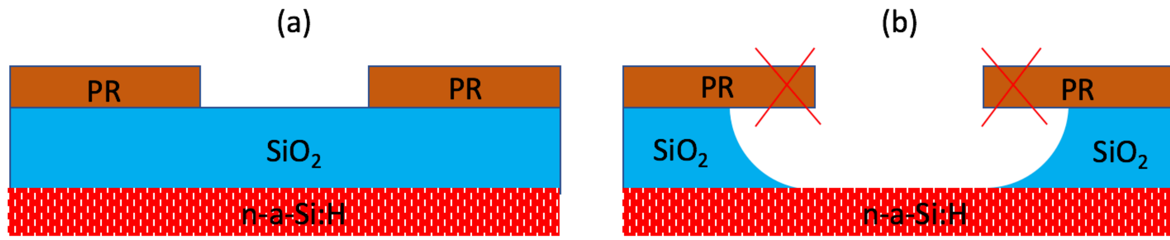


Figure 6.3 Schematic representation of a). Before HF dipping; b). After HF etching (isotropic). The red crosses indicate the possible falling of the photoresists.

As shown in Fig. 6.3.b, the isotropic etching of SiO_2 in HF leads to loss of supporting SiO_2 structure beneath the edge of photoresist. If photoresist is well-baked, the photoresist should be hard enough to keep it complete. Besides, thicker SiO_2 needs longer time of etching, in other words, a larger notch can be expected. Therefore, two possible situations can happen: firstly, the time when photoresist was falling off is before the complete etching of oxide on the emitter area, which sets obstacles for the HF etching and following polyetch dipping; if the time is after completely etching of oxide on top of the emitter area, with following acetone cleaning, there is no further influence. The problem will be less pounced if a thinner oxide layer is used. Therefore, there is a tradeoff on the thickness of the SiO_2.

Insufficient Light Management

As reported in [103], the significant improvement on the light trapping can be found on double side textured wafer compared to the only front side textured wafer. The schematic path of ray is illustrated in Fig. 6.4. The light incident into the absorber is randomized by the rear textured side, meanwhile, the optical path of light is prolonged. Therefore, insufficient light trapping for the rear-flat wafer is also one limiting factor for achieving high efficiency solar cells.

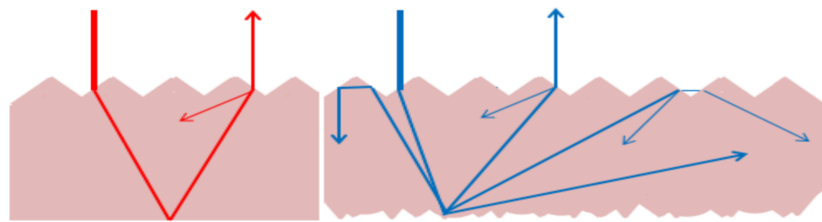


Figure 6.4 The comparison of rays in flat-rear and textured-rear (Lambertian) structure. Adapted from [104].

6.2.1.3 Results and Analysis

The results of the manufactured best flat-rear IBC-SHJ solar cells are presented below in Table 6.2 with comparison to the reference IBC-SHJ solar cell from Jiali [89].

Table 6.2 The results of manufactured flat-rear IBC-SHJ and reference IBC-SHJ solar cells.

Solar cell	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Flat-rear IBC-SHJ	37.38	524	0.47	9.2	559	0.84
Reference IBC-SHJ [89]	38.50	576	0.70	15.6	-	-

For the flat-rear IBC-SHJ solar cell, the FF is very poor compared to the reference cell and 'S-shaped' J-V curve was observed. The low FF suffers from both low R_{sh} and high R_S. The very large difference between pFF and FF also indicates the cell suffers from significant R_S. Besides, a drop of 35 mV from SunsVoc to the final device V_{OC} is observed. Both inferior FF and V_{OC} are speculated mainly as results of the final metallization process. During the Al e-beam evaporation, the temperature of the cell surface will increase because of continuous attachment of high temperature Al vapor. Once the cell is overheated (the evaporation process is too long), it can reach temperature probably higher than 180 °C (intolerant for low-temperature deposited layers), because 'burned' traces of photoresist is observed (black parts in Fig. 6.5). As reported in [105], when temperature goes up to 250 °C, the burning of photoresist can happen and deteriorate the etching process of the photoresist. Therefore, the burned photoresist can potentially lead to imperfect isolation of metal grids of BSF and emitter due to the incomplete liftoff process, which eventually results in the observed shunting issue. Besides, since no photoresist should be in the emitter and BSF region, the illustrated 'burned' photoresist within the emitter and BSF region are due to thermal expansion of the PR from the 'gap'. As a result, lesser metal coverage of emitter and BSF negatively influence the collection of carriers.

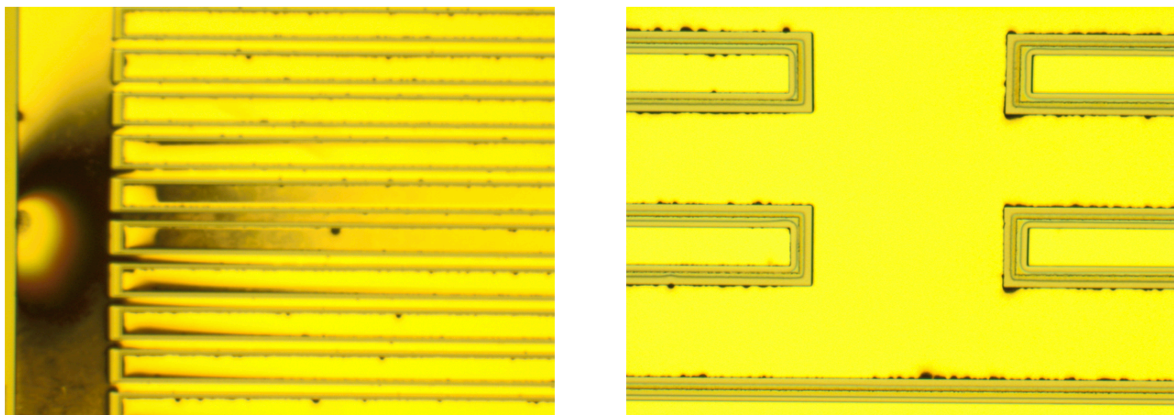


Figure 6.5 The optical microscope images of 'burned' photoresist after metallization.

To sum up, the problems originated from high temperature during Al e-beam evaporation are suspected to be the main reasons for poor performance of the manufactured cell. With this

manufacture process, it is able to make working rear-flat IBC-SHJ solar cells, but further optimizations are needed for making high-efficiency IBC-SHJ solar cells. According to limited time and above mentioned limiting factors, no further investigation on the flat-rear IBC-SHJ solar cell is conducted. Instead, the textured-rear IBC-SHJ solar cells are manufactured.

6.2.2 Textured-rear IBC-SHJ Solar Cell

6.2.2.1 Manufacture Process of Textured-rear IBC-SHJ Solar Cell

Suffers from the worse performance on flat-rear IBC-SHJ cell, the manufacture process on the flat-rear solar cell is adjusted to the textured-rear surface. In order to check potential shunting problem when the BSF and emitter are directly connected, wafers are prepared as two groups. The first group is similar to previously mentioned flat-rear IBC-SHJ solar cell, which has no gap (no isolation) between the emitter and BSF. Another group, SiN_x is used as the initial gap between emitter and BSF. The schematic representations of both groups are illustrated below in Fig. 6.6.

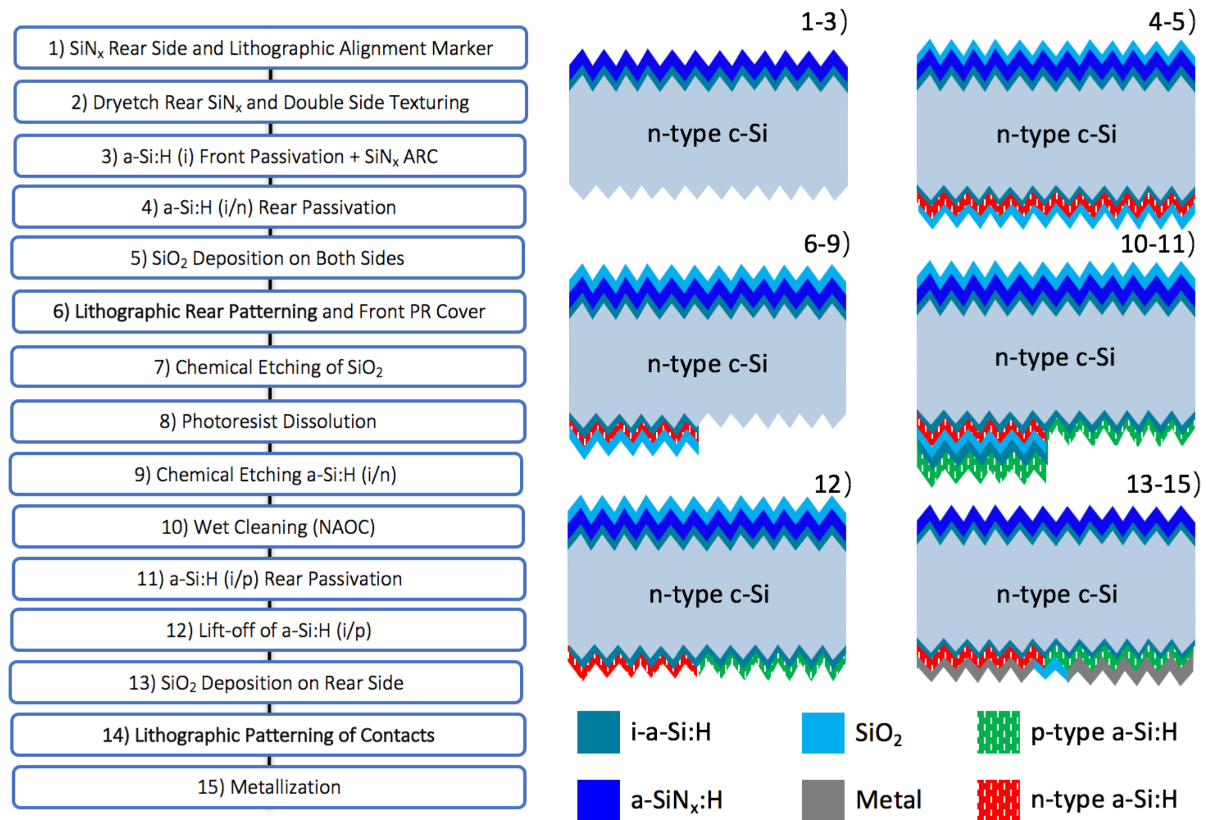


Figure 6.6 Schematic flowchart of textured-rear lift-offed IBC-SHJ solar cell (no gap) manufacture with doped a-Si:H layers. Structures are not scaled according to the practical case.

As presented in Fig. 6.6 and Fig. 6.7, the basic difference in terms of two manufacture process is at the initial step. The cell without gap need to have alignment marker prepared on the rear side first, since after double-side texturing, the textured surface is not visible for alignment. As for the

cell with gap, the first lithography step is done for patterning the gap between BSF and emitter, meanwhile, the alignment marker is patterned. Afterward, the similar process as flat-rear IBC-SHJ solar cell is expected to be done on the cases of textured-rear IBC-SHJ solar cell.

Aside from using doped a-Si:H layers as passivating contacts, the optimized doped nc-SiO_x:H layers are applied to these two manufacture processes as well. For nc-SiO_x:H, both deposition sequences are tested (either i/n or i/p is tested at step 4)).

Consequently, there is no cell successfully manufactured based on those flowcharts. The limiting factors of those processes are listed below.

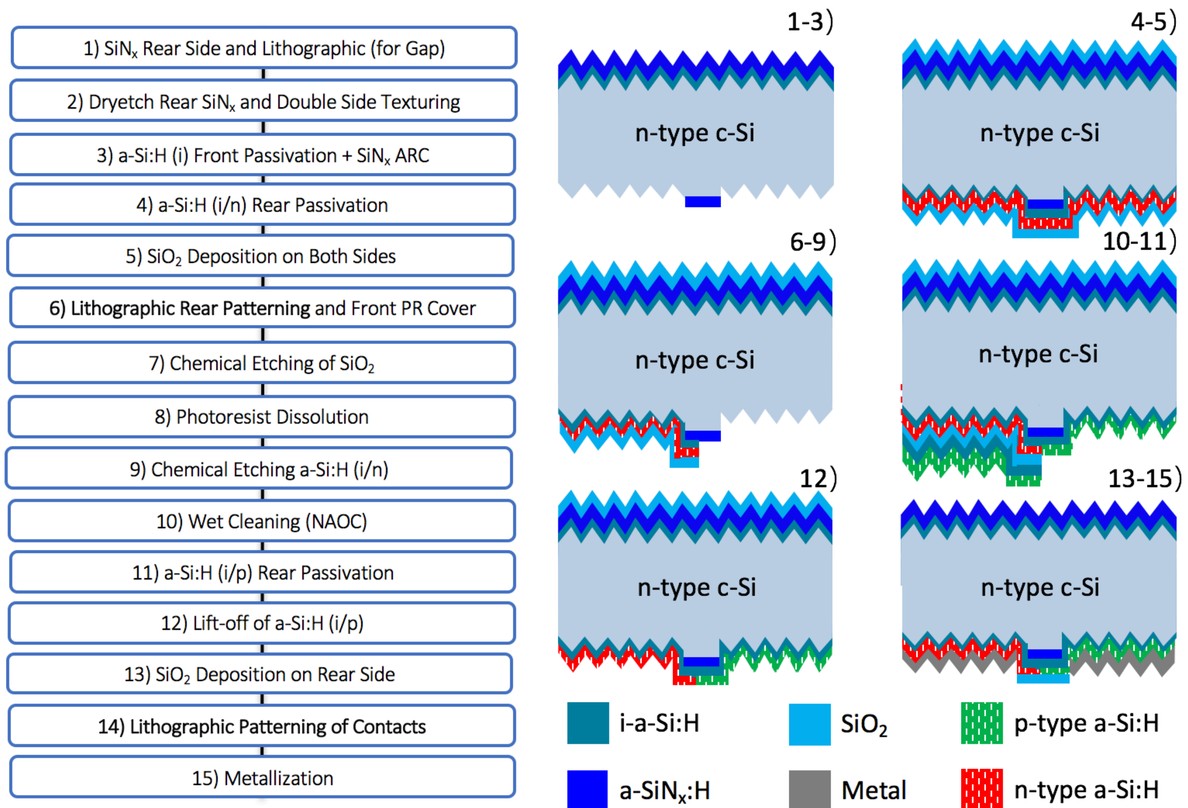


Figure 6.7 Schematic flowchart of textured-rear lift-offed IBC-SHJ solar cell (with gap) manufacture with doped a-Si:H layers. Structures are not scaled according to the practical case.

6.2.2.2 The Limiting Factors of the Manufacture Processes

This section mainly describes the problems found during the manufacture of IBC-SHJ solar cells on double side textured wafers.

Passivation Quality

The passivation quality is tested based on structure till step 4). The font side i-a-Si:H (5 nm)/SiNx (300 nm) passivation stack is deposited in Kavli (not optimized), the rear side is covered by full area i-a-Si:H with either n-type a-Si:H or nc-SiO_x:H. For the case of i/n a-Si:H (6.5 nm/15 nm) on

the rear side, the lifetime only reaches 1848 μs with an iV_{OC} of 704 mV, which indicates although optimized layers are applied on the textured rear side, the front i-a-Si:H/c-Si interface is still not optimized. Similar inferior passivation quality is also found on p-type nc-SiO_x:H applied. Therefore, solving the front side passivation problem is the key to improve the passivation quality of the final device.

Since SiN_x is deposited under high temperature (400 °C), which already sets a precondition: the SiN_x must be deposited firstly. The deposited SiN_x is mainly used as ARC, which gives the possibility to replace it with low-temperature SiO_2 (150 °C). With this low temperature ARC, the optimized i-a-Si:H layer can be passivated on the front c-Si surface. This approach will be applied and introduced in section 6.3 for fabricating tunneling IBC-SHJ solar cells.

Photoresist Leftover

At step 9), the photoresist leftover after HF dip is again found on the textured surface, which is observed to be more serious than that of the flat surface. The Fig. 6.8 is demonstrated below, where n-a-Si:H layer is used. It is hard to distinguish if oxide is totally removed when wafer is cleaned with acetone. The possible influences are same as the that of the flat surface.

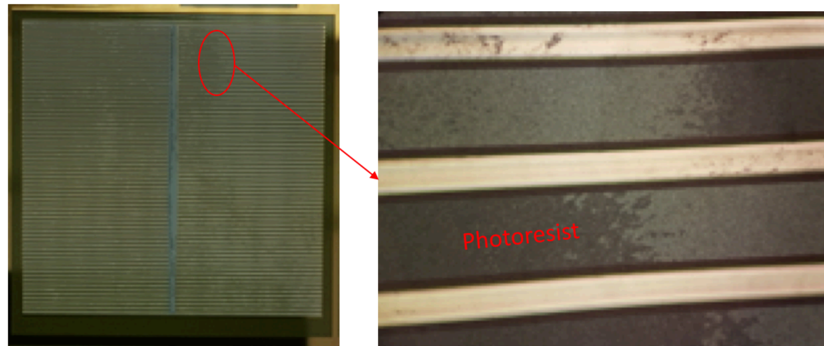


Figure 6.8 The indication of photoresist leftover after HF dipping. The right figure is obtained under the optical microscope. After acetone dipping, the surface is well-cleaned.

Polyetch Etching

Etching i/n a-Si:H (6.5 nm/15 nm) layer stack at step 9), 8 seconds is tested to be sufficient for etching the layer stack (with 3 seconds over etch). Therefore, the requirement on the SiO_2 thickness is not strict. This is also good for solving the photoresist leftover problem. However, in the case of etching i-a-Si:H/p-nc-SiO_x:H (11 nm/15 nm) (first deposited) layer stack, it takes more than 30 seconds to be completely etched away. This requires thicker SiO_2 on both front side and rear BSF side, thus the photoresist leftover problem is more severe.

Limited Cleaning Cycle

At step 10), only one NAOC standard cleaning is applied. More times of NAOC cleaning requires longer time of HF dipping. This is risky for removing the SiO_2 for liftoff process and SiO_2 and SiN_x at front side. Applying too thick oxide worsens photoresist leftover and is time-inefficient.

Etching of n-type nc-SiO_x:H

This is specially observed from the sample with firstly n-type nc-SiO_x:H layer deposition sequence. At step 12), liftoff of i-a-Si:H/p-type nc-SiO_x:H is conducted in 0.55% HF solution (picture is shown below). The reaction (small bulbs) was considered as liftoff process. However, after finishing fabricating this cell, the illuminated J-V curve indicates no junction was formed. With careful analysis, it turns out that n-type nc-SiO_x:H can be etched by 0.55% HF, while p-type nc-SiO_x:H is not etched (or very slow etching rate). As can be observed from the Fig. 6.9, there is no bulb on emitter busbar (p-type nc-SiO_x:H), while reaction happens only at the BSF busbar.

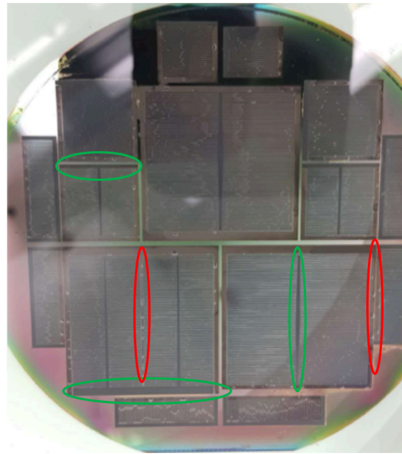


Figure 6.9 The indication for n-type nc-SiO_x:H (red circle) layer being etched by 0.55% HF solution while p-type nc-SiO_x:H (green circle) is not etched.

The schematic explanation is illustrated below. For addressing the rear side processing, the front side of the wafer is not presented. As shown in Fig. 6.10, after the full are i-a-Si:H/p-type nc-SiO_x:H deposition on the rear side (shown in (a)), most (explained in next section) of the i-a-Si:H/p-type nc-SiO_x:H on BSF region can be firstly liftoff by etching of the SiO_2 beneath (shown in (b)). However, since there is no etching selectivity on the n-type nc-SiO_x:H layer, 0.55% HF keeps etching the n-type beneath, while p-type nc-SiO_x:H on the emitter side remains unreacted. Therefore, when the reaction stops (no visible bulbs), there is nearly no n-type layer left for forming BSF as illustrated in (c). Thus, the final device cannot work.

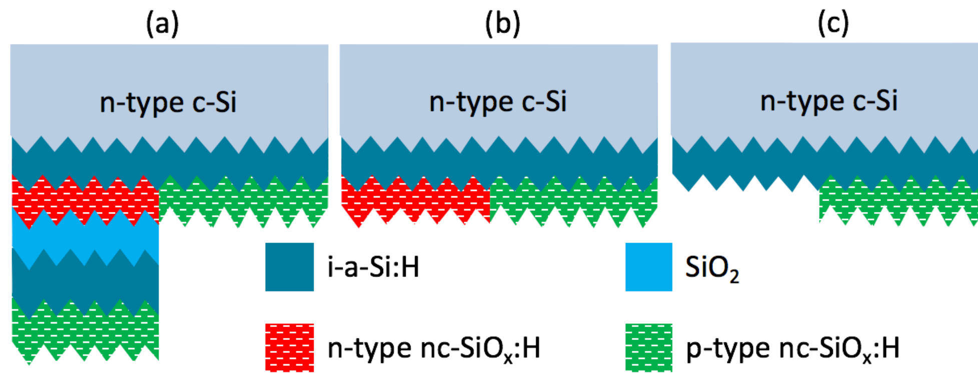


Figure 6.10 The schematic representation of etching n-type nc-SiO_x:H during liftoff process.

This observation can be also well-explained by conductivities that are measured in Chapter 4. The high conductivity of p-type nc-SiO_x:H indicates less amount of oxygen is alloyed, while relatively low conductivity n-type nc-SiO_x:H is the opposite. Thus, 0.55% HF can etch more oxygen alloyed n-type nc-SiO_x:H but not the p-type nc-SiO_x:H. It is worth noting that this observation provides possibilities for manufacture of tunneling IBC-SHJ solar cell by the wet-chemical approach.

Liftoff on Textured Surface

Since a-Si:H layers are not constrained by previously mentioned etching issues, liftoff of the i/p a-Si:H layer stack was conducted. As shown in Fig. 6.11, the brown color indicates the i-a-Si:H/n-a-Si:H/SiO_2/i-a-Si:H/p-a-Si:H layer stack, which is supposed to liftoff the i/p-a-Si:H by etching the SiO_2 beneath. Nevertheless, some parts cannot be liftoff.

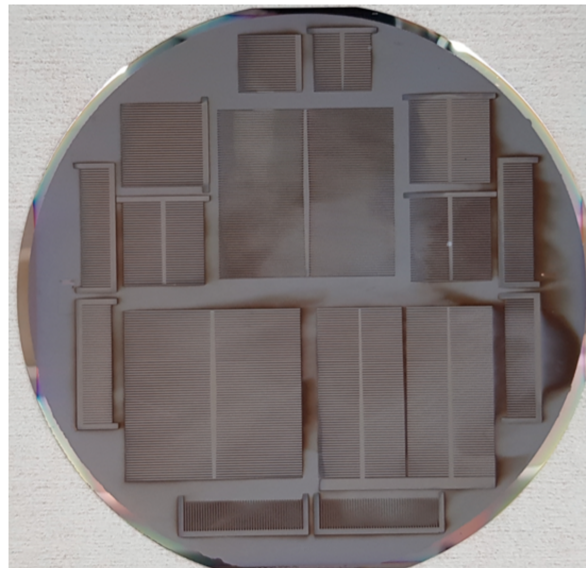


Figure 6.11 The incomplete liftoff process on the textured surface.

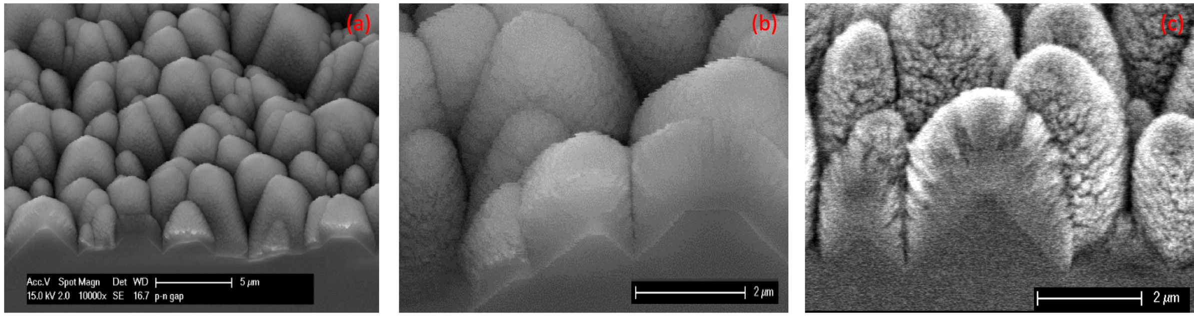


Figure 6.12 The SEM images of deposited SiO_2 on top of the SiN_x passivated textured silicon surface [106]. (a). The as-deposited sample, 5 µm resolution; (b). the sample after 30 seconds 0.55% HF etching, 2 µm resolution; c). the sample after 90 seconds 0.55% HF etching, 2 µm resolution.

This can be explained by the SEM images shown in Fig. 6.12. The SEM sample is prepared by firstly depositing around 2 µm SiO_2 on one side of the double side textured wafer, then the sample is cut into small pieces and etched with different time in 0.55% HF. This HF etching simulates the effect of polyetch for opening emitter area. Although the as-deposited SiO_2 layer is expected to have a conformal growth over pyramids, as shown in (a), valleys between pyramids are non-conformal growth according to too deep intervals between pyramids. This indicates a large thickness different of deposited SiO_2 on the textured surface. Figure (b) provides a closer look of the sample after 0.55% HF etching for 30 seconds, the valley of SiO_2 is almost in contact with the c-Si surface. Besides, it also confirms the oxide growth is individually on each pyramid. As shown in (c), after 90 seconds etching, the c-Si surface already opened at several intervals. This gives a hint that when polyetch is conducted at step 7), there is no or insufficient oxide left for liftoff at some valleys of pyramids. Therefore, the not liftoff i-a-Si:H/p-a-Si:H layer stack forms recombination centers for electrons collection.

6.2.2.3 Summary and Outlook on The Lift-off Approach

Lastly, the summary is given based on the practical problems occurred during the manufacture process. Afterward, novel manufacture process is designed aims at solving those limiting factors.

Summary

During the manufacture of double side textured lift-offed IBC-SHJ solar cells, the manufacture process developed on flat-surface is not feasible to be directly applied. Based on different passivating contacts, different limiting factors constrain the successful manufacture.

For a-Si:H layers, the main limiting factors are inferior passivation quality compared to symmetrical passivation test and unsuccessful liftoff process on the textured surface.

For nc-SiO_x:H layers, passivation quality also suffers from the not optimized front i-a-Si:H/c-Si interface. Aside from the textured surface, the n-type nc-SiO_x:H is not resistant to 0.55% HF solution; thus, no liftoff can be realized.

Outlook

With the view to make successful manufacture of the textured-rear IBC-SHJ solar cell, the current process flow can be adjusted based on different layers.

For a-Si:H layers, the main change is on step 12), instead of using liftoff process to remove the i/p a-Si:H on BSF, dry-etch (ALACTEL GIR 300 F-ETCHER) can be applied.

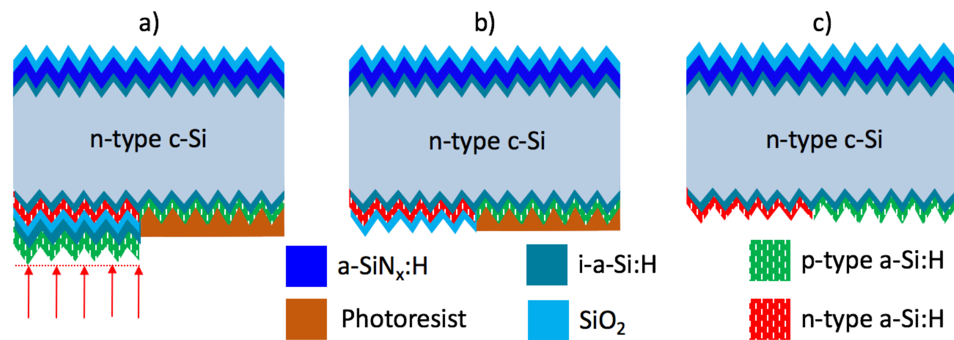


Figure 6.13 Dryetch of i/p a-Si:H layer stack. a). Negative PR cover the emitter, plasma etches the i/p a-Si:H layer stack; b). remove the SiO_2 with 0.55% HF; c). photoresist removal.

As shown Fig. 6.13, after i/p a-Si:H layer stack deposition, an extra photolithography step is needed. Use the same mask for the emitter, negative photoresist rather than positive photoresist is coated. Therefore, the emitter is protected. With known etch rate of the a-Si:H layers, the etched thickness can be well-controlled. Over-etch is applied to ensure i/p a-Si:H is totally removed. Besides, since BSF is protected by SiO_2, plasma-induced passivation damage is proved to be negligible. Afterward, the 0.55% HF can selectively etch SiO_2 till it reaches n-type a-Si:H layer. Subsequently, the photoresist can be removed by NMP (1-Methyl-2-pyrrolidon) and HNO_3 cleaning.

For nc-SiO_x:H layers, at step 7) in Fig. 6.7, 0.55% HF etches not only the SiO_2, but also the n-type nc-SiO_x:H. Afterward, just a few seconds dipping in polyetch to ensure complete removal of i-a-Si:H and incubation layer of n-type nc-SiO_x:H. Other steps are similar to that of adjusted a-Si:H dry-etch approach. However, according to limited time, these two proposals are not investigated in the thesis.

Instead, based on those experience, a novel manufacture process for making tunneling IBC-SHJ solar cell is successfully developed.

6.3 Manufacture of Tunneling IBC-SHJ solar cell

6.3.1 Introduction of Interband Tunneling Junction

Different from lift-offed IBC-SHJ solar cell, the electron collecting of tunneling IBC-SHJ is realized by n/p layer stack, or so-called interband tunneling junction (TJ or tunneling recombination junction) (shown in [14, Fig. 6.14]) . Basically, electrons from c-Si bulk is firstly collected at n-type passivating contact, then collected electrons have to tunnel through the potential barrier to recombine with the holes from p-type passivation contact. If the potential barrier is too large (wide space charge region), the resulting insufficient tunneling leads to resistive transport of electrons.

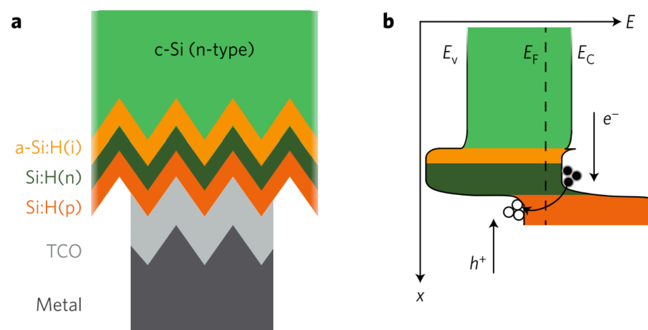


Figure 6.14 Schematic illustration of interband tunneling passivating contact (collecting electrons). Adapted from [14]. a. the contact stack which includes tunneling junction; b. the corresponding band diagram.

As described in [14], forming efficient interband tunnel junction and manipulating working device with this structure, basically, three requirements are needed:

- Good selectivity on c-Si surface by field-effect passivation. In this case, the n-type layer should provide sufficient field-effect passivation to achieve selectively collection of electrons, and meanwhile, strong enough to screen the field-effect from p-type layer above.
- Lossless carrier collection at tunneling junction. This requires highly doped adjacent n-type and p-type layers, which narrow the space charge region, thus enhances the probability for tunneling recombination;
- Low lateral conductivity of p-type layer. Since p-type layer is full area, shunting needs to be avoided between BSF and emitter.

In order to meet first two requirements, high doping efficiency for both n-type and p-type layers are required. Since low activation energies are measured from doped-nc-SiOx:H layers, they are expected to be good candidates. Within this project, 30 nm n-type-nc-SiO_x:H is deposited, which is expected to provide sufficient and undisturbed field-effect passivation.

Besides, since the nano-crystal growth of nc-SiO_x:H is substrate sensitive [50], the p-type nc-SiO_x:H that deposited on top of n-type nc-SiO_x:H is expected to continue the crystal growth of n-type layer [14], thus effectively narrow the space charge region and eventually enhance the tunneling probability. Meanwhile, the p-type nc-SiO_x:H on top of i-a-Si:H should have a relatively thick amorphous phase incubation layer, which indicates low lateral conductivity thus enables good electrical isolation between emitter and BSF.

Before fabricating the tunneling IBC-SHJ solar cell, the tunneling FBC-SHJ solar cell is manufactured as a proof of working concept. The results of both types are analyzed in section 6.3.3. The structures of both tunneling FBC and IBC cells are demonstrated below in Fig. 6.15.

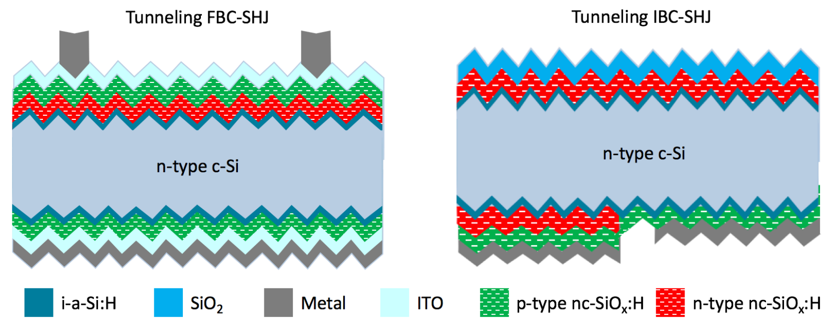


Figure 6.15 Schematic representation of tunneling FBC-SHJ and IBC-SHJ solar cells.

6.3.2 Manufacture Process of Tunneling IBC-SHJ solar cell

As identified etching of n-type nc-SiO_x:H in HF solution in section 6.2.2.2, the wet-chemical etch approach for fabricating tunneling IBC-SHJ solar cell is developed and represented in Fig. 6.16.

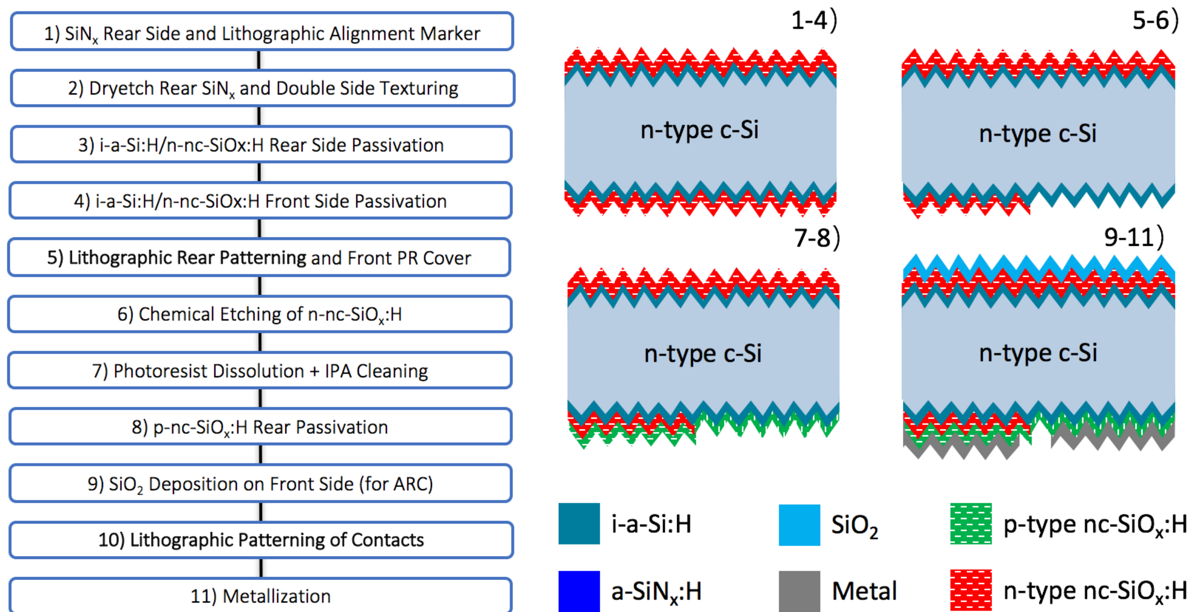


Figure 6.16 Schematic flowchart of tunneling IBC-SHJ solar cell manufacture with doped nc-SiO_x:H layers. Structures are not scaled according to the practical case.

Firstly, the wafer is covered by SiN_x (Novellus, PECVD) on rear side and photolithography is applied to prepare alignment marker for future photolithography steps. After developing, the SiN_x that is unprotected by photoresist is removed by dry-etching (DRYTEK TRIODE 384T). Since dry-etching harden the photoresist, another plasma treatment (Tepla Stripper) is used for removing photoresist. Then, NAOC cleaning (without HF dipping) and double side texturing are conducted. This texturing process is tested (passivation test) to be efficient on removing most of the defect-rich c-Si surface induced by dry-etching.

Afterward, 3 times NAOC cleaning are performed before loading sample into PECVD deposition chamber (AMIGO). The i/n layers are deposited on both sides, thus ensure optimized interface passivation. Later, the emitter area is opened by photolithography and n-type nc-SiO_x:H is etched by diluted 2.4 vol.% BHF solution. This BHF etching cannot totally etch the n-type nc-SiO_x:H, the less oxygen alloyed a-SiO_x:H incubation layer is left after the etching. Since the remaining n-type layer in emitter area can act as recombination center for collected holes, it is essential to be completely removed. A mixture solution of 0.55 vol.% HF and 31 wt.% H_2O_2 with a volume ratio of 1:6 is made for etching this n-type incubation layer. After all the etching steps, the wafer is cleaned by acetone and IPA separately for two times, the DI water rinse is applied in between each cleaning. Then full area p-type nc-SiO_x:H is deposited on the rear side forming interband tunnel junction and emitter. Low-temperature SiO_2 (150 °C) is applied at the front surface as extra passivation layer and ARC. Eventually, the metallization step is conducted with assistance of the last photolithography step (metal lift-off).

6.3.3 The Improvements and Limiting Factors of the Manufacture Process

In terms of improvements, the manufacture process of tunneling IBC-SHJ solar cell is compared with that of lift-offed IBC-SHJ solar cell. Besides, since the process is newly developed, the challenging factor for further improvement is pointed out.

Improved Passivation Quality

The passivation quality is significantly improved since the optimized c-Si/i-a-Si:H interface passivation on both sides. Till step 4), the n-nc-SiO_x:H (5nm)/i-a-Si:H (7nm)/n-c-Si/i-a-Si:H (7nm)/n-nc-SiO_x:H (30nm) shows the effective lifetime over 5.3 ms and iV_{OC} beyond 713 mV. As for the final device, SunsVoc over 730 mV and V_{OC} around 720 mV are achieved.

Besides, at step 6), the chemical etching eventually ends at i-a-Si:H layer, which means it will keep the c-Si rear surface being passivated by i-a-Si:H layer. Therefore, the NAOC cleaning before p-type layer deposition is not strictly needed.

Easier-controlled ARC Thickness

In lift-offed IBC-SHJ solar cell manufacture process, the uncertainties during etching processes introduce the challenge of controlling the ARC thickness, which is important for the light management. Since there is no etching of SiO_2 as ARC at front surface in the tunneling IBC-SHJ solar cell process, the thickness of ARC is easily controlled and optimized. The good light management results in the measured J_{SC} over 40 mA/cm^2 on average.

Successful Sliver Liftoff on Textured Surface

In general, Al is used for liftoff according to its good adhesion to silicon layers. Ag, which has poor adhesion on flat silicon surface, is tested not suitable for liftoff process. However, it is proved that Ag thermal evaporation induces negligible damage on passivation quality if nc-SiO_x:H layers are used. Therefore, Ag liftoff is tested on textured silicon surface and it is proved to be feasible (shown in Fig. 6.17).

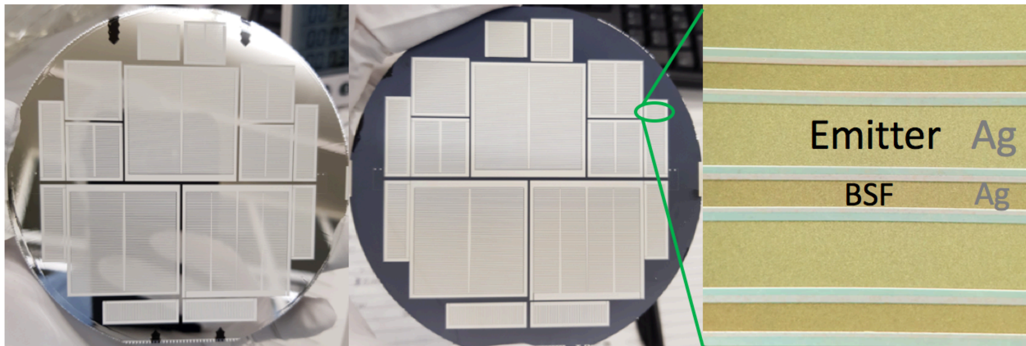


Figure 6.17 Demonstration of silver liftoff on the textured surface. The perfect isolation of metal contacts between BSF and emitter can be observed under optical microscope.

Decisive Wet-chemical Etching

Step 6) is the most challenging step in the whole process. The combined etching by diluted BHF and mixture solution (H_2O_2 and HF) must completely remove the n-type layers on the emitter region. Since diluted BHF has a good selectivity over Si, it will not etch the i-a-Si:H layer. Therefore, expected hydrophobic on the emitter region after sufficient BHF dipping is expected (i-a-Si:H is hydrophobic). In fact, no expected full-area hydrophobic happens since still thin oxide layer is left and cannot be etched by diluted BHF. It is necessary to mention the non-uniform etching is observed according to random nucleation growth of nc-SiO_x:H layer. The irremovable part is speculated to be related to the n-type nc-SiO_x:H incubation layer as illustrated in Fig. 2.5. Those several nanometers incubation layer is thought to be less-oxygen alloyed because it is resistant to diluted BHF etching. Therefore, the mixed H_2O_2 and HF solution that is used for etching silicon layer, is applied for completely etching the incubation layer. Thus, precisely etching of n-type layers without etching too much i-a-Si:H layer is important for keeping the passivation.

Time-effective

The manufacture process of lift-offed SHJ-IBC solar cells includes 28 steps in total, while with this novel manufacture process for tunneling IBC-SHJ solar cell, only 18 steps are needed. Several time-consuming steps in the lift-off process are not included in the new process. Thus, the manufacture time is reduced from 8 working days to maximum 3 working days (3 wafers in one run). Eventually, the manufacture efficiency is significantly improved.

6.3.4 Results and Analysis

First Run

Eventually, the successfully manufactured tunneling IBC-SHJ solar cells are measured by illuminated J-V measurement and the best result is shown below. Meanwhile, the tunneling FBC-SHJ solar cell, which is manufactured as a proof of concept, is also presented in Table 6.3 (the best in terms of FF).

Table 6.3 The external parameters of manufactured tunneling FBC-SHJ, IBC-SHJ and reference IBC-SHJ solar cells.

Sample	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Tunneling FBC-SHJ	30.0	694	0.73	15.20	706	0.80
Tunneling IBC-SHJ	41.3	659	0.67	18.24	670	0.77
Reference IBC-SHJ [89]	38.5	576	0.70	15.52	-	-

The tunneling FBC-SHJ solar cell has the electron collector at front with structure of ITO (80 nm)/p-nc-Si:H (15 nm)/ p-nc-SiO_x:H (7 nm)/n-nc-SiO_x:H (30 nm)/i-a-Si:H (7nm), while the emitter at rear side with i-a-Si:H (7nm)/ p-nc-SiO_x:H (7 nm)/ p-nc-SiO_x:H (15 nm)/ITO (120 nm). Firstly, according to insufficient doping qualities of the n-type layer, thick layer (30 nm) is applied. Besides, the exact same p-type layers are applied at both front and rear sides to simulate the rear side of tunneling IBC-SHJ solar cell. Although the cell suffers from severe parasitic absorption due to too thick front layer stack, the values of FF and V_{OC} prove the interband tunneling junction is able to function normally.

As for tunneling IBC-SHJ solar cell, the excellent J_{SC} is obtained according to good light management on front side and well-collection of majority carriers (electrons). However, the low V_{OC} is mainly attributed to the chemical etching process in step 6). It is found that the V_{OC} values measured on different cells, manufactured in the same wafer, are not uniformly distributed (ranges from 637 mV to 681 mV), which confirms the non-uniform etching in step 6). The drop from

SunsVoc to device V_{OC} is mainly attributed to the inefficient minority carrier collection as concluded in chapter 5. The moderate FF mainly suffers from high R_S, which mainly originates from non-optimized n-type nc-SiO_x:H, non-ideal p-nc-Si:H/Ag contact and thin Ag thickness (1.3 μm). As a starting point, the efficiency of 18.2% is achieved.

Further Exploration

After the promising kick-off, two more runs of the tunneling IBC-SHJ solar cells are conducted. In the second series of experiments, the thickness of rear side i-a-Si:H passivation layer is varied from 7 nm to 11 nm while remaining all other layers and processes unchanged. The objective is to ensure sufficient thickness of i-a-Si:H layer can be left after the chemical etching of n-type layers and eventually better V_{OC} of the solar cells. Firstly, the passivation qualities with varying thickness of rear i-a-Si:H layers till step 4) are demonstrated below.

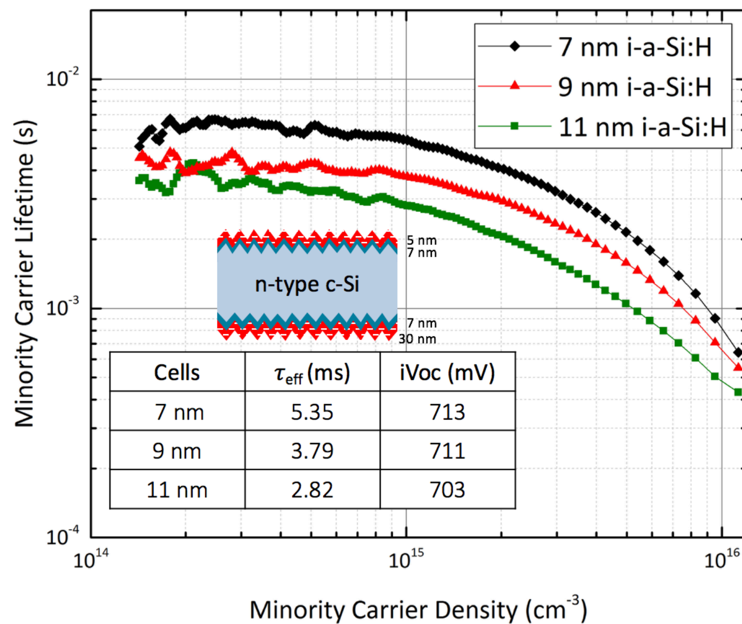


Figure 6.18 The minority carrier lifetime measurements of tunneling IBC-SHJ solar cells till step 4). The schematic structure of the measured sample is demonstrated. The minority carrier lifetime is extracted at minority carrier density of 10^{15} cm^{-3}.

As shown Fig. 6.18, the thicker intrinsic layer the more inferior passivation quality can be observed. This suggests again the insufficient field effect passivation from n-type nc-SiO_x:H layer.

Afterward, according to incomplete etching of n-type layer before depositing p-type layer (step 6), shown in Fig. 6.19, all cells suffer from extremely low FF (see Fig. 6.20). The etching time of 2 minutes diluted BHF and 2 minutes mixed H_2O_2 and HF solution that is kept same as the first run. Therefore, the etching step needs to be carefully processed.

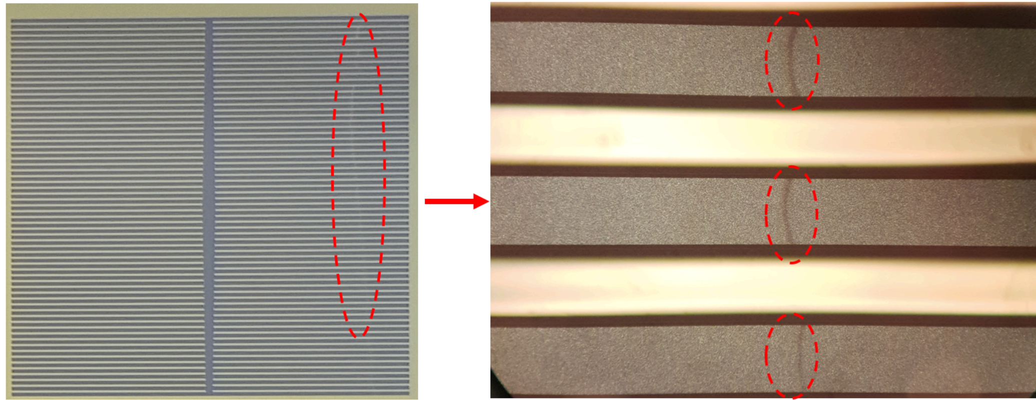


Figure 6.19 Images shown the incomplete etching of n-type layer before p-type nc-SiO_x:H deposition. The yellow strip within the red dashed circle indicates existing of n-type layer.

The parameters of tunneling IBC-SHJ solar cell (2nd run) obtained from illuminated J-V measurement are demonstrated below in Fig. 6.20.

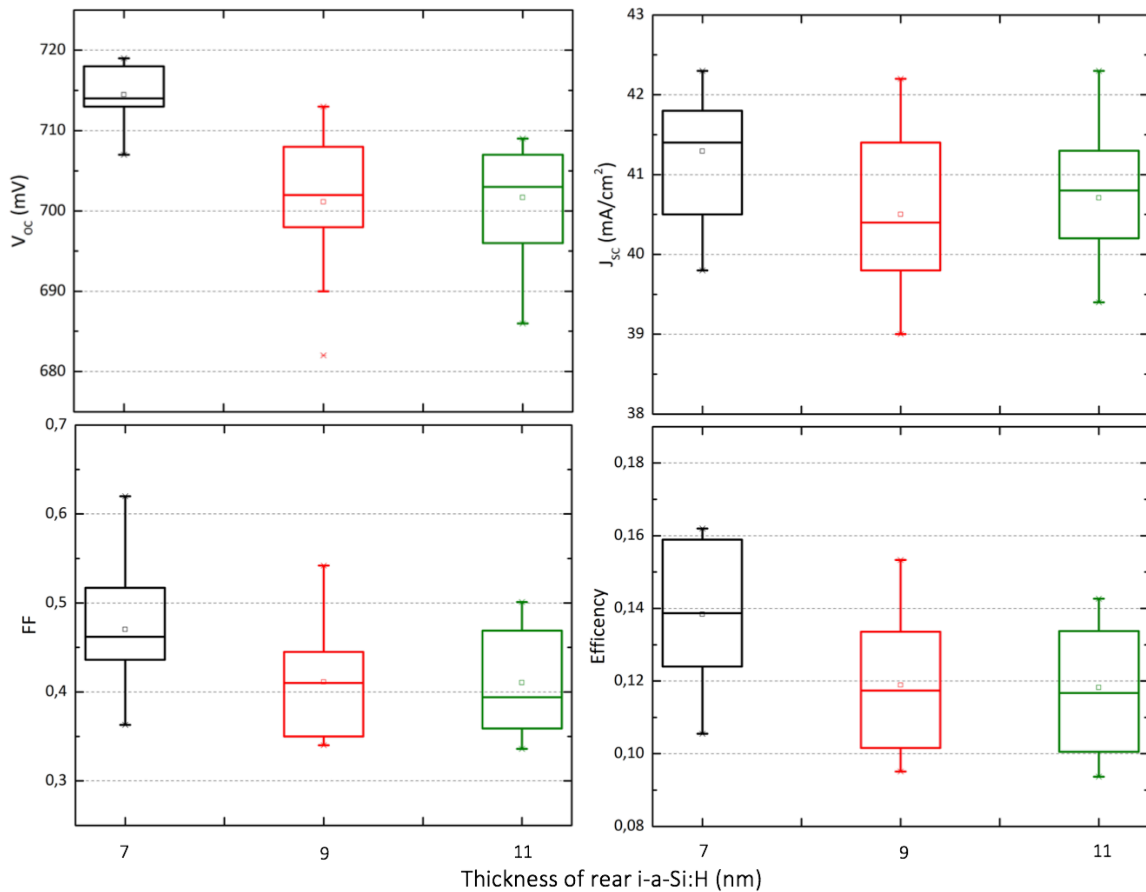


Figure 6.20 The box plots of measured tunneling IBC-SHJ cells parameters (2nd run) with different rear i-a-Si:H layer thickness.

As demonstrated in Fig. 6.20, the device V_{OC} reaches an average around 715 mV for the sample with only 7 nm rear i-a-Si:H, while similar V_{OC} (around 700 mV) can be found on both 9 nm and 11 nm i-a-Si:H layer cases. The similar trend of V_{OC} is found on J_{SC}, where the thinnest rear i-a-Si:H layer exhibits the highest average J_{SC} (over 41mA/cm^2). As explained previously, all cells suffer from the incomplete etching thus low FF and low efficiency. The best cell in terms of efficiency in this run is 16.29% with an area of 1 cm^2. The results are present in Table 6.4.

Table 6.4 The external parameters of manufactured best tunneling IBC-SHJ solar cells in 2nd run.

Sample	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (-)	η (%)	SunsVoc (mV)	pFF (-)
Tunneling IBC-SHJ 2nd	41.77	709	0.55	16.29	730	0.81

Although cells obtained have favorable V_{OC} and J_{SC}, the low FF limits them for achieving high efficiency. Therefore, further optimizations on the layer properties and processes still need to be proceeded.

6.3.5 Summary on Tunneling IBC-SHJ Solar Cells

The novel manufacture process of tunneling IBC-SHJ solar cell is successfully developed and an efficiency of 18.2% is achieved. Within two series of experiments, the highest V_{OC} of 719mV with J_{SC} of 41.65 mA/cm^2 are realized concurrently. Among all manufactured cells, the low FF limits the solar cell efficiency. The low FF compared to the reference tunneling FBC-SHJ is suspected mainly due to the incomplete etching of n-type layer on emitter region, which acts as the recombination center and eventually deteriorates the collection of charge carriers. Besides, the lowly-conductivity n-type nc-SiO_x:H layer, non-ideal p-nc-Si:H/Ag contact and thin Ag thickness (1.3 μm).

7

CONCLUSIONS AND OUTLOOKS

With the final goal to successfully manufacture high efficiency IBC-SHJ solar cells, a comprehensive study 'from layer to device' is conducted. During the study, three main topics are investigated: optimization of the contact layer stack, identification of the FF and V_{OC} limiting factors in FBC-SHJ solar cells, and lastly, the manufacture of high efficiency IBC-SHJ solar cells. Based on the understanding of the whole process and acquired practical experience, outlooks are given for both short-term achievable efficiency improvements and long-term high efficiency SHJ solar cells.

7.1 Conclusions

7.1.1 Optimization of the contact layer stack

The optimized contact layer stack includes the i-a-Si:H, which is critical for providing excellent chemical passivation on c-Si surface, and doped silicon passivation contacts that realize the selectivity collection and transport of charge carriers. For i-a-Si:H, the optimization approach is mainly based on understanding the relation between deposition parameters and optimizing according to measured passivation quality and uniformity. As for doped silicon passivation contacts, namely, doped a-Si:H and nc-SiO_x:H layers, in addition to the passivation quality, the activation energy and band gap (for p-type layer) optimization is also critical for achieving lossless transport and collection of charge carries. Within the project, the symmetrical 6 nm i-a-Si:H passivation structure can reach effective lifetime over 3.3 ms, iVoc beyond 722 mV and J_0 below 5.5 fA/cm^2. The excellent underlying i-a-Si:H passivation layer enables the implementation of optimized doped passivation contacts without significant degradation. It is worth noting that optimized p-type nc-SiO_x:H layer exhibits favorable activation energy (51.4 meV) and dark conductivity (0.714 S/cm) for only 29 nm deposited on glass. Additional argon plasma during depositing of the doped layers generally destroys their conductivity except p-type a-Si:H.

7.1.2 Identification of the FF and V_{OC} limiting factors in FBC-SHJ solar cells

The optimized contact layer stacks are integrated into the manufacture of FBC-SHJ solar cells. Since the FBC-SHJ solar cells are manufactured for using as proof of concept for further process of high efficiency IBC-SHJ solar cells, the FF and V_{OC} are the most important parameters to be investigated.

In terms of V_{OC}, it is found that the thicker p layer stack is essential for ensuring smaller drop from SunsVoc to V_{OC} thanks to enhanced minority carrier collection. Besides, thick doped nc-SiO_x:H layers can effectively shield the field effect from ITO and simultaneously keep the chemical passivation quality. Lastly, sample with thick n- and p-layer with additional argon plasma during growth of n layer can significantly improve the passivation quality. Under this conditions, before metallization, outstanding values of SunsVoc and pFF were achieved as 727 mV and 0.862 respectively. After metallization, the same sample exhibited SunsVoc of 734 mV and pFF of 0.841.

As for transport contribution to the FF, in Chapter 4 it was reported a relatively low conductive n-type nc-SiO_x:H layer, this effect together with the low ΔVoc reveal that low FF values are related to majority carrier collection and nor to p-contact stack. Moreover, n-contact/ITO interface becomes crucial as demonstrating by tunnel contact in which such an interface is not present as described in Chapter 6. Another tested approach for this n-type nc-SiO_x:H layer consists on covering with few-nanometers nc-Si:H layer deposited for forming contact with ITO is important for improving the FF.

From the highest achieved FF (73%), the doped layers' thickness of 12 +3 nm on both sides are sufficient thick to keep good SunsVoc and relatively efficient charge carrier collection. Thus, the best manufactured FBC-SHJ solar cell with this FF reaches an efficiency of 20.42% using $J_{SC,EQE}$. Additionally, the hybrid cell with p-type nc-SiO_x:H and n-type polysilicon layers are manufactured, which revealed that FF degradation originates from n-type nc-SiOx:H and its contact with ITO, since 76% FF is achieved on the front junction hybrid cell with an efficiency of 20.08%.

7.1.3 Manufacture of IBC-SHJ solar cells

After successful manufacture of FBC-SHJ solar cells, the corresponded structures are transferred to IBC-SHJ solar cells.

The manufacture process developed in PVMD group for flat-rear IBC-SHJ solar cells is found to be limited by mostly the poor passivation quality and insufficient light management. According to overheated metallization, the manufactured flat-rear IBC-SHJ solar cell suffers from low passivation quality and low FF. In order to acquire excellent passivation quality that is obtained on FBC-SHJ solar cells, integration of optimized layers into rear-textured IBC-SHJ solar cell structure is critical. However, the 'liftoff' process that is critical for successful manufacture of flat-rear IBC-

SHJ solar cell is not applicable to the textured surface. Therefore, no successful textured-rear IBC-SHJ solar cell is manufactured. However, it is found that the 0.55% HF that is used for processing the liftoff process etches the n-type nc-SiO_x:H layer, which brings about the novel manufacture process of tunneling IBC-SHJ solar cells. Based on successfully manufactured tunneling FBC-SHJ solar cell (73% FF) as the proof of concept, the tunneling IBC-SHJ solar cell is manufactured with an efficiency of 18.2% (67% FF), which renew the IBC-SHJ solar cell record in PVMD group. Further trials prove that average device V_{OC} of 715 mV (highest 719 mV) and J_{SC} over 41 mA/cm^2 can be achieved concurrently, but limited FF (below 60%) constrains the final efficiency below 17%. This mainly attributes to incomplete etching of n-type layer for forming the rear patterning.

7.2 Outlooks

7.2.1 Layer Optimization

Optimization of n-type nc-SiO_x:H

As concluded above, the lowly-conductive n-type nc-SiO_x:H layer hinders the forming of lossless contact. Aside from this, its observed etching behavior in HF solution indicates the amount of oxygen alloyed into the layer is possibly too high. According to [48], although the low power density (150 mW/cm^2) and high pressure (around 12 mbar) deposition tends to obtain layer with higher crystalline fraction, this generally corresponds to the high refractive index and smaller bandgap. With moderate modification of deposition power density (slightly higher) and/or deposition pressure (slightly lower), they are expected to not only keep sufficient crystalline fraction but also reduce the refractive index and increase the bandgap. Besides, for fixed power density and pressure, the lesser the flow of CO_2, which is the source of oxygen, the higher the crystalline fraction but increased refractive index are expected. Besides, PH_3 and SiH_4 are reported have less impact on the crystalline fraction and they also need to be optimized both optically and electrically.

Therefore, systematic optimization of the n-type nc-SiO_x:H is needed. But in terms of FF improvement, improving the conductivity is of the top priority. Nevertheless, it can be expected that if n-type nc-SiO_x:H is only optimized in terms of conductivity, there will be two major impacts: firstly, the reduced transparency if as front layer for FBC-SHJ solar cells; secondly, it might not be able to be etched HF or BHF, then the wet-chemical approach for manufacture of tunneling IBC-SHJ can probably be not compatible.

Post Argon plasma treatment or hydrogen plasma treatment for i-a-Si:H

Within the thesis, the as-deposited i-a-Si:H already exhibits excellent passivation quality on c-Si surface, but further potential improvement can be expected if post hydrogen plasma treatment [102], [103] or post argon plasma treatment [91] is applied. The best precursor manufactured in

terms of passivation in this project involves the agron plasma, which is suspected related to post argon plasma treatment to i-a-Si:H layer. As for post hydrogen plasma treatment, it can not only provides enhance the surface passivation, but also fasten the nucleation [109], [110]. Therefore, it is also expected for fater nucleantion of doped nc-SiO_x:H layers, which ehhances the conductivity and lower the activation energy whitin a thin thickness.

Optimization of ITO

It is known that the resistivity ρ of TCO is expressed as: $\rho = R_{sheet}t = 1/(qN\mu)$, where R_{sheet} is sheet resistance, t is thickness, N is charge carrier density and μ is carrier mobility. To reduce the resistivity, in one hand, N should be increased. However, the more the free carrier concentration, the lesser transparent the TCO. The increased free carrier concentration leads to severer free carrier absorption in NIR spectrum and poor matching of refractive index in both NIR and VIS spectrum [111]. Therefore, higher temperature around 200 °C [112] should be the way to improve μ to optimize TCO (especially ITO) in terms of both transparency and conductivity. In this thesis, the temperature for ITO sputtering is only 110 °C. In addition, 10 nm low power (20 W) 'protective' ITO layer is in contact with passivating contacts, which is suspected to have low conductivity in that region. Besides, a general FF increment of 2% to 3% abs. is measured during annealing of the manufactured solar cells, which is possibly due to crystallization of the sputtered ITO and eventually enhanced conductivity. Therefore, higher temperature and direct high power sputtering of ITO is expected to improve the conductivity. However, the potential damage to the underneath passivation contacts is also needed to be investigated.

7.2.2 Process Optimization

Precise etching for n-type nc-SiO_x:H

For manufacture of tunneling IBC-SHJ solar cells, the etching of n-type nc-SiO_x:H is decisive for ensuring no recombination centers formed in the emitter region. An optimized etching method with high reproducibility should be found. This includes the thickness of rear i-a-Si:H layer, the concentration of etching solution (diluted BHF and mixture solution of H_2O_2 and HF) and the etching time.

Low-temperature SiO_2 or SiN_x as protective layer

During manufacture of tunneling IBC-SHJ solar cells, the thin n-type nc-SiO_x:H on front surface, which act as FSF, can be potentially etched by TMAH contained developer when conducting rear side patterning. Therefore, capping the SiO_2 directly after step 4) (Fig. 6.16) can protect front side from being etched. Since further manufacture process nearly not etch the SiO_2, the thickness optimized for ARC is not influenced. Same applies to low-temperature SiN_x, if it is used for ARC.

Double ARC

For IBC-SHJ solar cells, if the low-temperature ARC such as SiO_2 or SiN_x is applied, it provides more freedom to process optimization. In this project, the low-temperature SiO_2 is already applied, which enables the using of the optimized silicon layers and reaches excellent device V_{OC} and J_{SC}. Similarly, low-temperature SiN_x can be applied together with SiO_2 forming double ARC, reducing the reflection in a wider spectrum [113]. Since SiN_x have a higher refractive index (around 2) compared to SiO_2 (around 1.5) [114], the SiN_x is used as the inner ARC, while SiO_2 is the outer ARC. The suggested thickness from [113] are 80 nm and 140 nm for SiN_x and SiO_2, respectively.

For FBC-SHJ solar cells, the combination of ITO and SiO_2 can be applied, however, an extra photolithography step is needed to open the area for metal contacts because SiO_2 is insulating.

Increase thickness for metal

For manufactured tunneling IBC-SHJ soar cells, cells with different size (from 1 cm^2 to 9 cm^2) exhibit variation of FF, i.e. smaller cells generally have higher FF compared to larger cells. This is attributed to the thin (1.2 μm) Ag grids, while its influence is lesser apparent on smaller cells. Thick metal grids are required for larger cell because they can effective reduce the contributed series resistance, which enhances the FF. However, the thickness of metal is usually limited by photolithography based liftoff process, since at least twice thick photoresist is needed for successful liftoff of the metal grids. With hard masking, it is easy to deposit desired thick metal grids.

Hard mask for IBC-SHJ solar cell patterning

For both lift-offed IBC-SHJ and tunneling IBC-SHJ solar cells, the using of hard mask for forming patterning at rear side can avoid the wet-chemical etching and simplifies the manufacture process in a large degree. However, the large feature size of hard masking requires the precise alignment of mask. Otherwise, inaccurate patterning of BSF and emitter can lead to severe shunting or recombination problem, thus deteriorating the performance of the solar cell.

Implementation of patterned TCO in IBC-SHJ solar cell

Implementation of ITO patterning into the IBC-SHJ solar cell manufacture process by either photolithography or hard masking can enhance the collection of the charge carriers, prevent metal diffusion into the passivating contacts and improve light management. This includes the optimization of etching ITO and photoresist removal if photolithography is applied.

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