A 440-μW, 109.8-dB DR, 106.5-dB SNDR Discrete-Time Zoom ADC With a 20-kHz BW

Eland, Efraim; Karmakar, Shoubhik; Gonen, Burak; van Veldhoven, Robert; Makinwa, Kofi A.A.

DOI
10.1109/JSSC.2020.3044896

Publication date
2021

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A 440-μW, 109.8-dB DR, 106.5-dB SNDR Discrete-Time Zoom ADC With a 20-kHz BW

Efraïm Eland, *Graduate Student Member, IEEE*, Shoubhik Karmakar, *Graduate Student Member, IEEE*, Burak Gönen, *Member, IEEE*, Robert van Veldhoven, *Senior Member, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article describes a discrete-time zoom analog-to-digital converter (ADC) intended for audio applications. It uses a coarse 5-bit SAR ADC in tandem with a fine third-order delta–sigma modulator ($\Delta\Sigma$M) to efficiently obtain a high dynamic range. To minimize its over-sampling ratio (OSR) and, thus, its digital power consumption, the modulator employs a 2-bit quantizer and a loop filter notch. In addition, an extra feed-forward path minimizes the leakage of the SAR ADC's quantization noise into the audio band. The prototype ADC occupies 0.27 mm^2 in a 0.16-μm technology. It achieves 109.8-dB DR, 106.5-dB SNDR, and 107.5-dB SNR in a 20-kHz bandwidth while dissipating 440 μW. It also achieves state-of-the-art energy efficiency, as demonstrated by a Schreier FoM of 186.4 dB and an SNDR FoM of 183.6 dB.**

***Index Terms*— A/D conversion, asynchronous SAR analog-to-digital converter (ADC), audio ADC, delta–sigma ADC, discrete-time (DT) delta–sigma, dynamic zoom ADC, inverter-based operational transconductance amplifier (OTA), low-power circuits, multi-bit quantizer.**

I. Introduction

AUDIO applications often require analog-to-digital converters (ADCs) with high dynamic range (DR), high energy efficiency, and low area [1]–[3]. By combining a low-power successive-approximation register (SAR) ADC with a high-resolution delta–sigma modulator ($\Delta\Sigma$M), zoom ADCs can meet all these requirements [4], [5]. The SAR ADC determines the coarse references of the fine $\Delta\Sigma$M, drastically reducing loop filter swing and enabling energy-efficient design. The overall digital output is then obtained by simply summing the outputs of both converters.

Recently proposed $\Delta\Sigma$Ms with finite impulse response (FIR) DACs and negative-R-assisted integrators are also capable of satisfying the requirements of audio applications [2], [3], [6], [7]. An FIR DAC essentially filters out the fed back quantization noise and, thereby, also relaxes loop filter swing. However, it introduces an extra delay in the feedback path, which requires an additional compensation path to maintain stability [2], [7]. This delay also limits the extent to which the loop filter's input swing can be reduced. Similarly, the swing at the virtual ground of an active integrator can be reduced by connecting it to a negative resistance [3], [6]. This effectively increases the integrator's gain and linearity. However, since the negative resistance is realized by an active circuit, it also produces noise and consumes power. Furthermore, foreground calibration is required to ensure good matching between the negative resistance and the integrator's equivalent input resistance. In comparison, zoom ADCs seem to present a good tradeoff between design complexity, energy efficiency, and resolution.

However, zoom ADCs also have drawbacks. In order to absorb SAR ADC non-idealities, their fine $\Delta\Sigma$Ms are usually designed to provide at least ±1 LSB of over-ranging [4], [5], [8], [9]. In the case of a 1-bit $\Delta\Sigma$M, this means that the modulator's DAC must span at least three SAR LSBs, leading to a significant loss of SQNR. Another issue is the leakage of the SAR ADC's quantization noise, to which zoom ADCs, like other MASH ADCs, are susceptible. This is because summing the outputs of the SAR ADC and the $\Delta\Sigma$M tacitly assumes that the signal transfer function (STF) of the latter is exactly unity, which will usually not be the case, especially at high frequencies [4]. These issues can be mitigated by increasing the modulator's over-sampling ratio (OSR) or by using a digital noise cancellation filter. However, both approaches inevitably increase power consumption [3], [5]. Previous zoom ADCs also suffered from limited robustness to out-of-band interferers.

This article, an extended version of [10], describes a discrete-time (DT) zoom ADC architecture that mitigates SQNR loss and quantization noise leakage, without compromising energy efficiency. Although a continuous-time (CT) loop filter enables the use of low-power ADC drivers and confers inherent anti-aliasing, a DT loop filter is more robust to component mismatch and, thus, does not require calibration. By employing a $\Delta\Sigma$M with a 2-bit quantizer, which fully exploits the existing DAC levels, its SQNR can be improved by $\sim$9.5 dB. An analog feed-forward path ensures a unity STF, which significantly reduces quantization noise leakage. Taken together, these techniques enable a significant (40%) reduction in OSR, while also increasing the ADC's

Manuscript received August 23, 2020; revised November 3, 2020; accepted December 3, 2020. Date of publication January 5, 2021; date of current version March 26, 2021. This article was approved by Associate Editor Brian Ginsburg. *(Corresponding author: Efraïm Eland.)*

Efraïm Eland, Shoubhik Karmakar, and Kofi A. A. Makinwa are with the Faculty of Electrical Engineering, Mathematics, and Computer Science, Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: e.n.eland@tudelft.nl).

Burak Gönen is with Ethernovia, 3702 AA Zeist, The Netherlands.

Robert van Veldhoven is with AMS IP, NXP Semiconductors, 5656 AE Eindhoven, The Netherlands.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2020.3044896.

Digital Object Identifier 10.1109/JSSC.2020.3044896

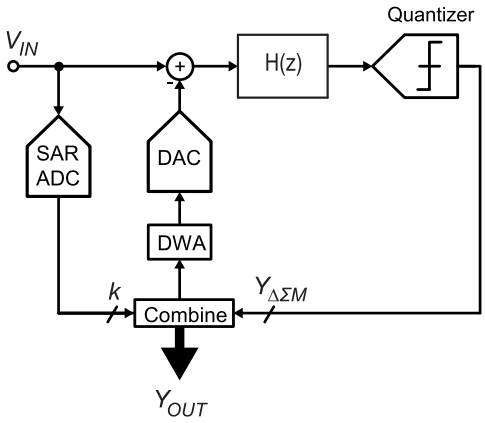


Fig. 1. Simplified block diagram of a zoom ADC employing an asynchronous SAR ADC, a ΔΣM with a conventional 1-bit quantizer, a DAC, and a DWA algorithm.

robustness to out-of-band interferers. They also confer state-of-the-art energy efficiency, resulting in a Schreier DR FoM of 186.4 dB and an SNDR FoM of 183.6 dB. In a 20-kHz bandwidth (BW), the proposed ADC achieves 109.8-dB DR, 107.5-dB signal-to-noise ratio, (SNR) and 106.5-dB signal-to-noise-and-distortion ratio (SNDR) while only consuming 440 μW.

This article is organized as follows. Section II briefly introduces the zoom ADC's working principle and its limitations. Section III describes the methods used to improve its performance and efficiency. Section IV explains some key circuit-level details. Measurement results are presented in Section V, followed by a conclusion.

II. Dynamic Zoom ADC

Fig. 1 shows a simplified block diagram of a zoom ADC. It employs a coarse N-bit asynchronous SAR ADC, operating at a sampling frequency f_S, which provides an N-bit output code k. The fine ΔΣM, also operating at f_S, then uses this output to set its references as

$$V_{ref+} = (k + M + 1) \cdot V_{LSB,C} \quad (1)$$

$$V_{ref-} = (k\text{-}M) \cdot V_{LSB,C} \quad (2)$$

where $V_{LSB,C}$ is the quantization step of the N-bit DAC and M is the over-ranging factor needed to accommodate SAR ADC non-idealities and quantization noise and to ensure that the modulator remains in its stable operating region. The SAR ADC is a mid-tread quantizer, and so the nominal input level is $(k + 0.5)V_{LSB,C}$. If the fine references V_{REF+} and V_{REF-} are updated at the sampling rate, the situation for $M = 1$ (minimum over-ranging) is shown in Fig. 2(a). However, the DAC of a 1-bit ΔΣM will then span 3-$V_{LSB,C}$. This "zooming-out" effectively increases the modulator's quantization error by 3×, reducing the SQNR by ∼9.5 dB compared with the case with no over-ranging. Although this can be restored by increasing the OSR, it comes at the expense of power consumption.

A. 2-Bit Quantizer

As shown in Fig. 2(b), although the 1-bit ΔΣM has a 3.$V_{LSB,C}$ range, it does not use the two intermediate

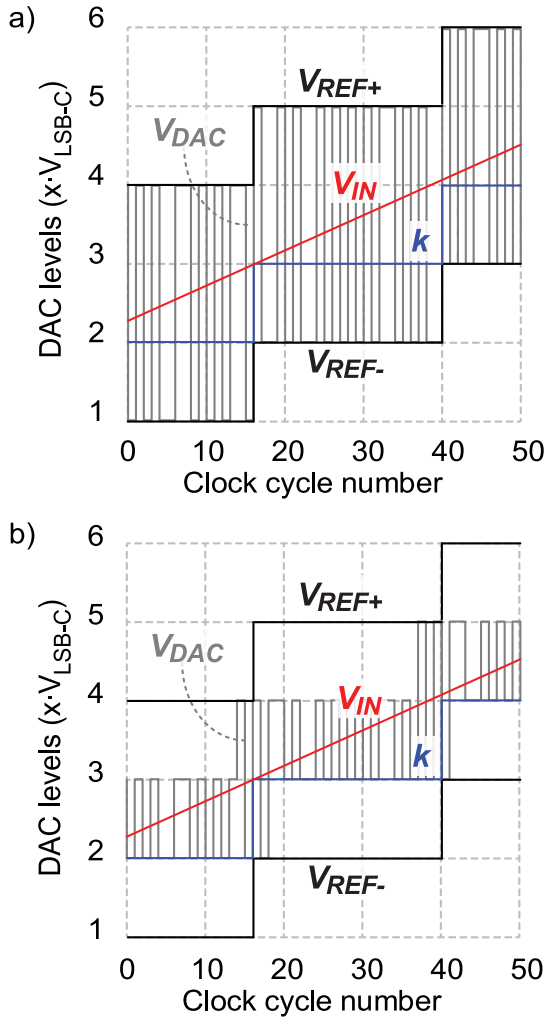


Fig. 2. SAR output (k) and ΔΣM DAC swings with $M = 1$ for (a) 1- and (b) 2-bit quantizers.

DAC levels. These levels can be accessed by using a 2-bit quantizer. It should be noted that the DAC itself remains unchanged, as does the data weighted averaging (DWA) scheme required to obtain high linearity. The resulting increase in SQNR enables a corresponding decrease in OSR, which, in turn, leads to reduced analog and digital power consumption, more than making up for the increased power consumption of the 2-bit quantizer.

B. Loop Filter Order, Coarse Resolution, and OSR

As in previous work [5], [9], the zoom ADC's target SQNR is set to about 120 dB to ensure that it achieves a thermal-noise limited DR of 110 dB. Similarly, it uses an energy-efficient feed-forward loop filter. Fig. 3 shows the SQNR across OSR for different loop filter orders (L) and coarse ADC resolutions (N). To keep the OSR and, therefore, the digital power consumption low, a third-order loop filter is preferred over a second-order filter. A 5-bit SAR ADC was chosen as a good tradeoff between digital complexity and OSR [5]. A third-order loop filter with optimally placed NTF zeros (see Fig. 4) then achieves an SQNR of ∼118 dB over the audio band. The sampling frequency is 3.5 MHz (OSR = 87.5), which is 30%

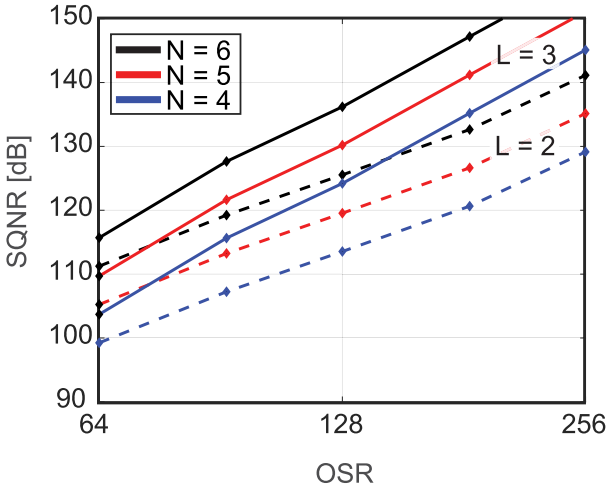


Fig. 3. SQNR across OSR for different loop filter orders (L) and coarse resolution (N) while employing a 2-bit quantizer.

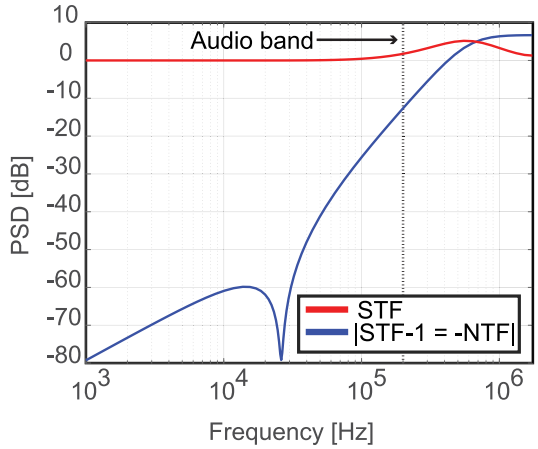


Fig. 4. STF and NTF of the $\Delta\Sigma$M loop filter, for an OSR of 87.5 in a 20-kHz BW, without the use of fuzz reduction techniques.

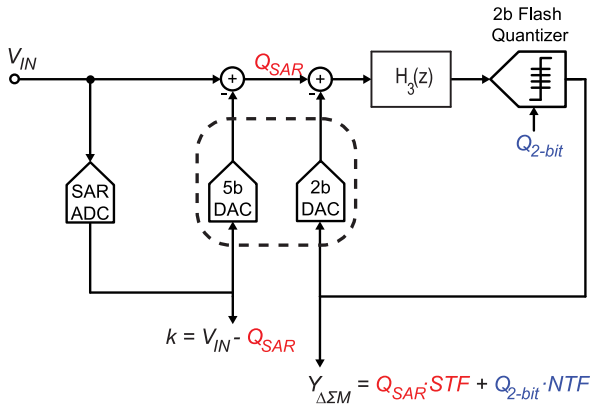


Fig. 5. Intuitive block diagram of the coarse-fine operation of the N-bit DAC.

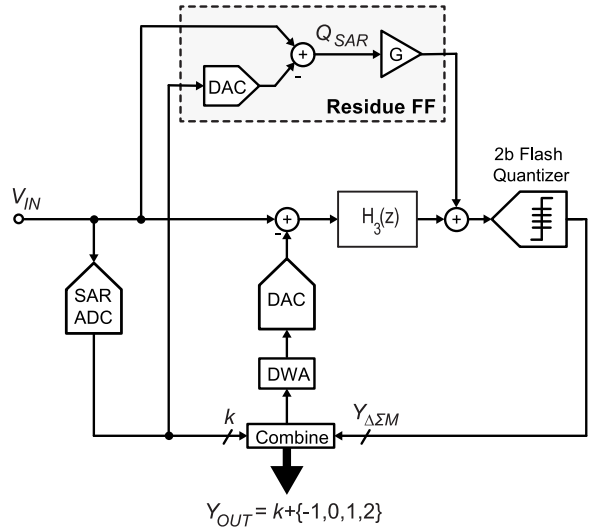


Fig. 6. Simplified block diagram of a zoom ADC employing an asynchronous SAR ADC, $\Delta\Sigma$M with a 2-bit flash quantizer, DAC, DWA algorithm, and residue feedforward.

lower than that of a previous zoom ADC with comparable specs [5]. Even at this low OSR, the 1st order mismatch shaping provided by DWA is still enough to support the target SQNR. Simulations show that an SQNR of 116dB can be achieved even in the presence of a 1% mismatch in the unit DAC elements.

C. Residue Feed-Forward "Fuzz" Cancellation

As shown in Fig. 5, a zoom ADC can be modeled as a 0-N MASH ADC by splitting its DAC into two halves, one driven by the SAR ADC and the other driven by the $\Delta\Sigma$M. The overall digital output $Y_{\mathrm{OUT}} = k + Y_{\Delta\Sigma M}$, can then be expressed as [4]

$$Y_{\mathrm{out}} = \mathrm{V_{IN}}(z) + Q_{\mathrm{SAR}}(z)\cdot(\mathrm{STF}-1) + Q_{2-\mathrm{bit}}(z)\cdot\mathrm{NTF} \qquad (3)$$

where Q_{SAR} and $Q_{2-\mathrm{bit}}$ represent the quantization noise of the SAR and the 2-bit quantizer, respectively. As expected, $Q_{2-\mathrm{bit}}$ is shaped by the NTF. However, the cancellation of Q_{SAR} is limited by STF-1, which is equal to -NTF for a feed-forward loop filter. As shown in Fig. 4, the cancellation of Q_{SAR} degrades rapidly outside the audio band. In fact, at 20 kHz, Q_{SAR} will only be suppressed by about 60 dB. Since the quantization "noise" of a 5-bit ADC is quite tonal, the result is increased distortion at high frequencies, referred to as "fuzz" in the literature [4].

SAR ADC quantization noise leakage can be mitigated by increasing OSR, at the expense of higher power consumption, especially in a switched-capacitor implementation. Alternatively, a digital noise cancellation filter can be used to process k before combining it with $Y_{\Delta\Sigma M}$ [4], but this will again be at the expense of higher digital power consumption.

In this work, we propose a low-power "fuzz" cancellation technique. It is based on the observation that, from (3), Q_{SAR} leakage can be prevented by ensuring that the modulator has a unity STF. One way of doing this is by implementing an input feed-forward path [11]. As shown in Fig. 5, the modulator's input is actually the residue of the SAR ADC. Thus, this should be extracted and added to the input of the modulator's quantizer. Rather than extracting the small residue at the input of the SAR ADC's comparator, which would require complex circuitry, a simpler approach is to generate a replica. This can be done by subtracting the output of a replica of the SAR DAC from the input signal, as shown in Fig. 6. Since the quantizer of the modulator has a fixed gain *(Kq)*, that relates

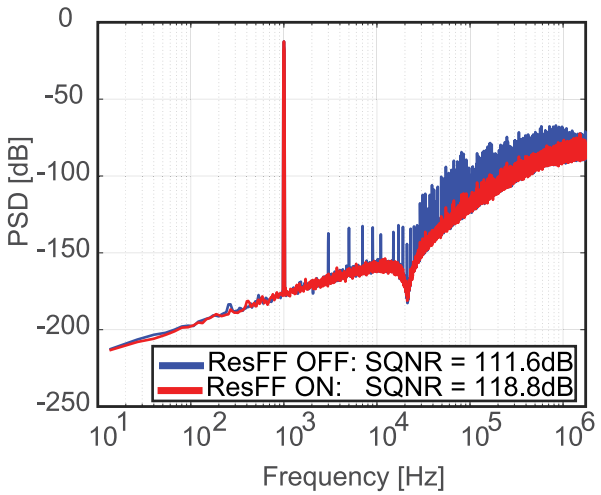


Fig. 7. Zoom ADC output spectrum for a −1.5-dB FS input at 1 kHz with residue feedforward turned "on" and "off" with $G = 1/Kq$.

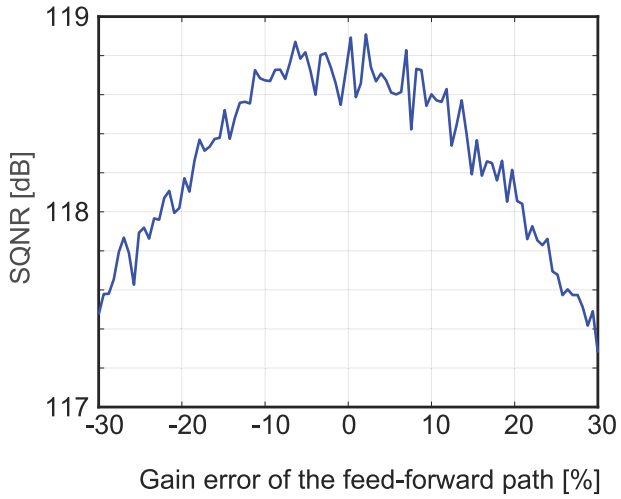


Fig. 8. Peak SQNR across variations in residue feedforward gain G compared with the optimal value $1/K_q$.

its input swing to the output swing of its 2-bit DAC, the output of the residue feed-forward path should be scaled by a factor $G = 1/Kq$ for optimal fuzz suppression.

D. Out-of-Band Interferers

The high slew rates of out-of-band interferers may exceed the fine reference values predicted by the SAR ADC and overload the modulator [3], [5]. Although this problem can be solved by using a simple first-order LPF to limit the amplitude of such interferers, i.e., as an anti-overload filter, it does add to system complexity. The proposed residue feed-forward path eliminates STF peaking and, thus, naturally increases the modulator's resistance to such interferers. The proposed 2-bit quantizer also helps because it reduces the swing in the loop filter. As a result, the overload-free BW of the proposed zoom ADC is about 2× higher than that of previous designs.

Fig. 7 shows the simulated effect of the proposed residue feed-forward technique for a −0.5-dB FS input signal at 1 kHz. A significant reduction in the "fuzz" can be seen, resulting in an overall SQNR of ∼118 dB, an improvement of ∼7 dB. Fig. 8 shows the effect of variations in G on the overall SQNR. For a 20% variation, it can be seen that the SQNR degradation is <1 dB, indicating that the proposed technique is robust to variations (PVT).

III. Circuit Implementation

A simplified schematic of the proposed zoom ADC is shown in Fig. 9(a). It consists of a 5-bit asynchronous SAR, a DT third-order CIFF loop filter with local feedback, a 2-bit quantizer, and a residue feed-forward stage.

A. Loop Filter

The loop filter consists of three switched-capacitor integrators. The input sampling capacitor ($C_S = 13.6$ pF), which also serves as the feedback DAC, is sized for thermal noise and consists of 31 unit elements ($C_0 = 438$ fF). The sampling capacitors of the second and third stages are significantly smaller, and their size is limited by matching requirements. The integration capacitors of all three stages are sized to ensure that the output swing of their operational transconductance amplifiers (OTAs) remains within their linear ranges.

The NTF zeros are implemented by configuring two integrators as a resonator. Since the required local feedback factor ($\beta_{\text{localFB}} = 0.07$) is quite small, the local feedback was implemented between the first and second integrators to enable the use of a reasonably sized capacitor ($C_{\text{notch}} = 64$ fF), ensuring better matching between C_{notch} and the other loop filter capacitors.

B. Differential Sampling and Chopping

The input is sampled using a fully differential sampling network. The sampling switches S_i $[1, \ldots, 31]$ are bootstrapped to maintain high linearity [12], and thick-oxide switches are used in the bootstrapping circuitry, thereby reducing complexity.

While the input is being tracked during phase-φ_1, OTA_1 is configured in unity feedback and is disconnected from the loop filter. At the end of φ_1, the input gets sampled onto C_S, whereas OTA_1, having had enough time to settle, is chopped [13], as illustrated in Fig. 9(b). Chopping OTA_1 while it is disconnected from the loop filter prevents chopping artifacts from coupling to the input signal. Since the chopper switches are connected to the input pairs of OTA_1, they are quite large (31× minimum size) to minimize their impact on OTA settling time and noise. The noise contributed by the output chopper switches is significantly lower, and so these are minimum-size devices.

The SAR ADC is clocked using φ_1, at the rising edge, after which it samples the input and enters the conversion phase. Within a few nanoseconds, it provides the 5-bit output k [4], [5] and resumes tracking, thereafter, until the next cycle. The digital backend uses k along with the 2-bit $\Delta\Sigma$M quantizer output to pre-calculate the 5-bit output of the zoom ADC. At the onset of φ_2, this 5-bit value is thermometer encoded, processed by a DWA algorithm [14], and, finally, passed on to the 31 unit elements of the capacitive DAC.

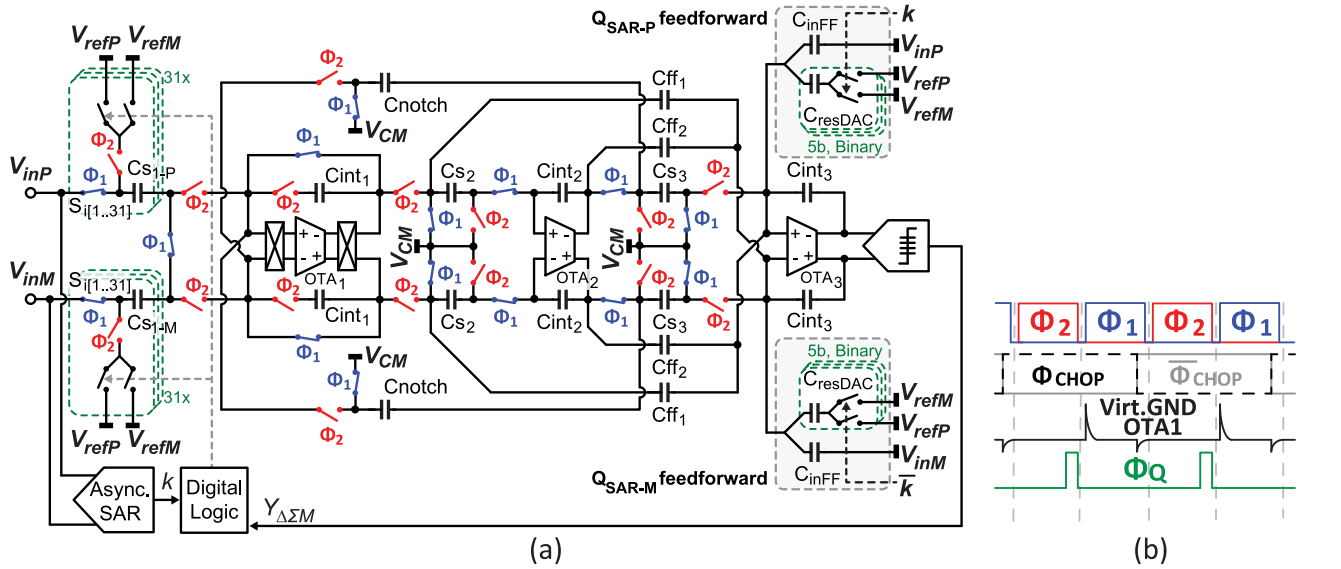


Fig. 9. Simplified circuit diagram of (a) proposed DT zoom ADC, with the corresponding timing diagram and simplified visualization of the virtual ground of OTA1 due to (b) switching activities.

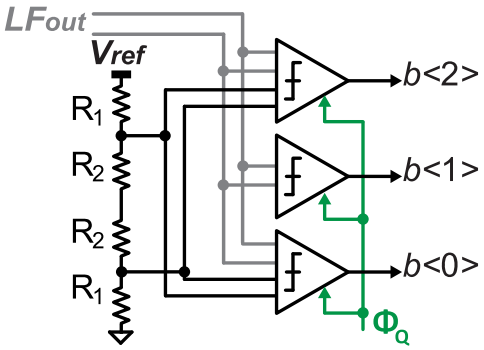


Fig. 10. Simplified schematic of the 2-bit flash quantizer.

C. Multibit Quantizer

Fig. 10 shows the schematic of the 2-bit flash quantizer comprising of a resistive reference ladder along with three comparators. To relax the specifications of the individual comparator offset, noise, and kickback, thus ensuring a low-power quantizer, a relatively large V_{REF} for the references is required. This translates into a low quantizer gain.

The top and bottom comparators make use of dual-difference comparators [15], [16] since they compare a differential input with a differential reference voltage. To minimize kickback on the reference ladder, the top and bottom comparators use a CT pre-amplifier, as shown in Fig. 11(a). This enables the use of large resistors (R_u = 72 kΩ, R1 = 10·R_u, and R2 = 3·R_u), limiting overall current in the ladder to $\sim$1 μA.

The middle comparator, as shown in Fig. 11(b), is a conventional design that employs a simple dynamic pre-amplifier to minimize kickback and maintain low power [16].

D. Residue Feed-Forward Path

To implement the residue feed-forward path, a replica of Q_{SAR} is generated by subtracting V_{IN} and V_{DAC}.

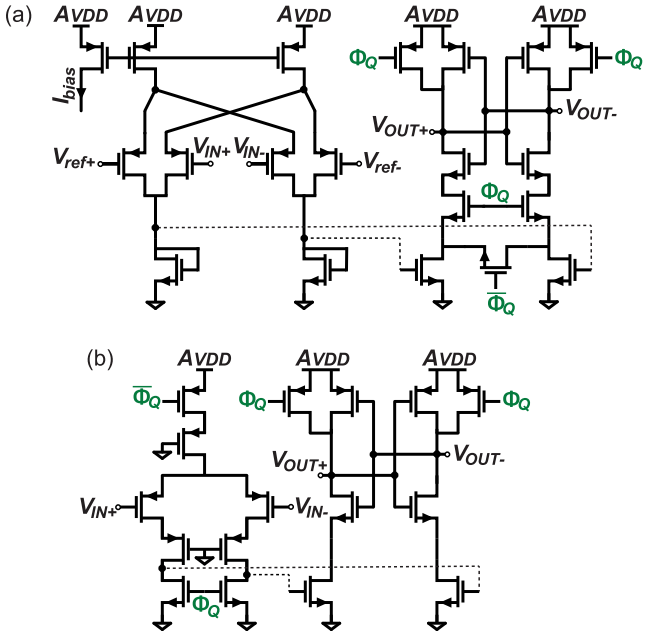


Fig. 11. Schematic circuit of the top and bottom comparators with (a) CT pre-amplifier and (b) middle comparator with dynamic per-amplifier.

To simultaneously generate Q_{SAR} and add it to the loop filter with a gain G, a summation is created at the virtual ground of OTA3 by using a feed-forward capacitor from the input to the virtual ground of OTA3 and by using a binary cap-DAC that is driven by k. Combined with the integration capacitor of OTA3, the residue feedforward gain G is established as follows:

$$G = \frac{C_{\text{inFF}}}{C_{\text{int3}}} = \frac{C_{\text{resDAC}}}{C_{\text{int3}}}. \tag{4}$$

To ensure that the input feedforward capacitor and the DAC capacitors are well matched, they are both realized from unit capacitors (C_0 = 6 fF).

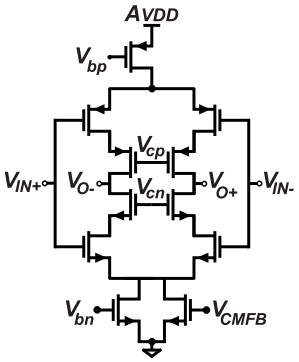


Fig. 12. Schematic of the differential current-starved OTA.

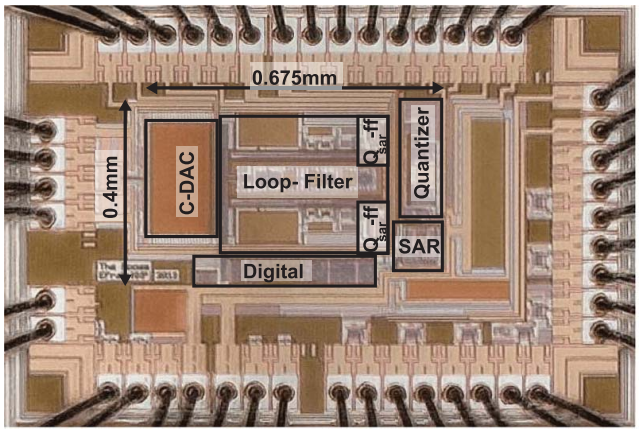


Fig. 13. Die micrograph of the prototype DT zoom ADC.

E. Current-Reuse OTAs

The combination of a coarse SAR ADC and a fine 2-bit $\Delta\Sigma$M results in a very low internal swing. This enables the use of energy-efficient current-reuse OTAs [4], as shown in Fig. 12. The OTA employs head and tail current source for its excellent rejection of supply variations and uses cascode transistors to achieve 60-dB dc gain. A constant g_m-biasing ensures that the NMOS and PMOS input pair remains in the saturation region over PVT. The common-mode feedback is implemented with a conventional switched-capacitor circuit [17], [18]. OTA_1 consumes 48 μA, while OTA_2 and OTA_3 are 8$\times$ scaled versions of OTA_1 and consume 6 μA each.

F. 5-Bit Asynchronous SAR

The 5-bit asynchronous SAR ADC is similar to the one used in [4] and [5]. It employs 1.8-fF unit sampling capacitors with a total capacitance of 55 fF. The digital 5-bit binary output, after being latched, is sent to both the digital of the $\Delta\Sigma$M and the residue feedforward DAC.

IV. Measurement Results

The prototype zoom ADC occupies an active area of 0.27 mm^2 in standard 160-nm CMOS technology, as shown in Fig. 13. It consumes 440 μW from a 1.8-V supply, of which the analog, DAC, and digital logic consume 46%, 19%, and 35%, respectively, as shown in Fig. 14. Low-noise reference buffers supply the 1.8-V references of the $\Delta\Sigma$M and SAR DAC.

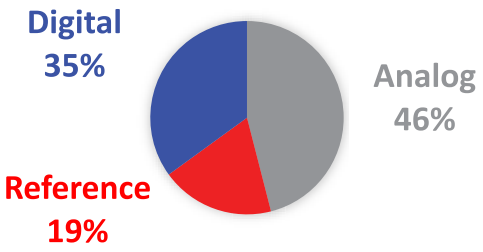


Fig. 14. Power breakdown.

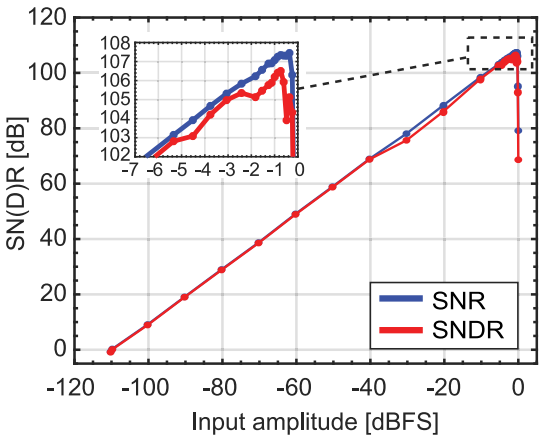


Fig. 15. SNR and SNDR across input amplitude for a 1-kHz sine-wave input.

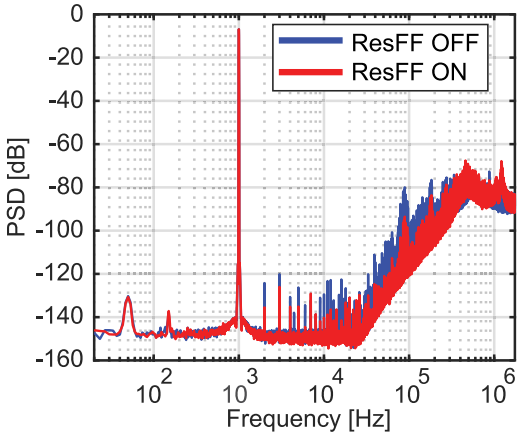


Fig. 16. Output spectrum with residue feedforward turned "off" and "on" for a −0.5-dB FS input signal at 1 kHz.

For a 1-kHz sine-wave signal, the measured SNR and SNDR across input amplitude are shown in Fig. 15, where 0-dB FS corresponds to 3.6 $V_{PP,diff}$. The peak SNR and SNDR are 107.5 and 106.5 dB, respectively. Around −30-dB FS, the SAR ADC starts to toggle between more than two levels, which increases the residual fuzz, causing the modulator's SNDR to drop slightly.

Fig. 16 shows the PSD for a −0.5-dB FS input signal at 1 kHz with the residue feedforward circuit turned "off" and "on." The peak THD and SNDR improve by 7.4 and 2.9 dB, respectively. The remaining fuzz is mainly due to the mismatch between the outputs of the main and residue DACs. Fig. 17 shows the PSD for a −0.5-dB FS input signal at 1 kHz

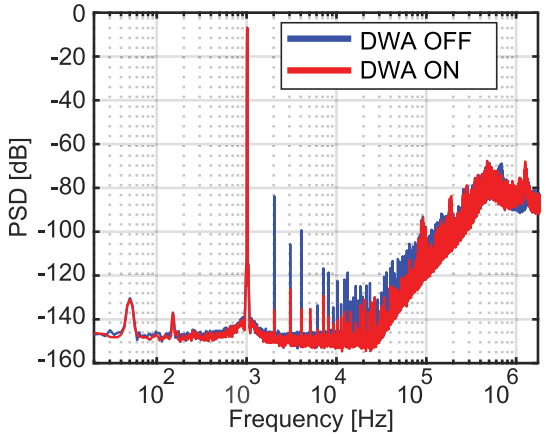


Fig. 17. Output spectrum with DWA turned "off" and "on" for a −0.5-dB FS input signal at 1 kHz.

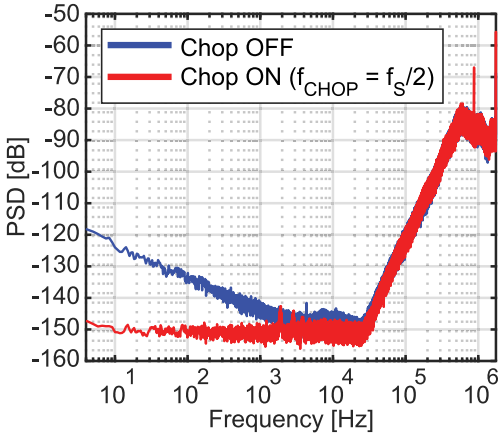


Fig. 18. Power spectral density with inputs shorted and chopping turned "off" and "on" at $fs/2$.

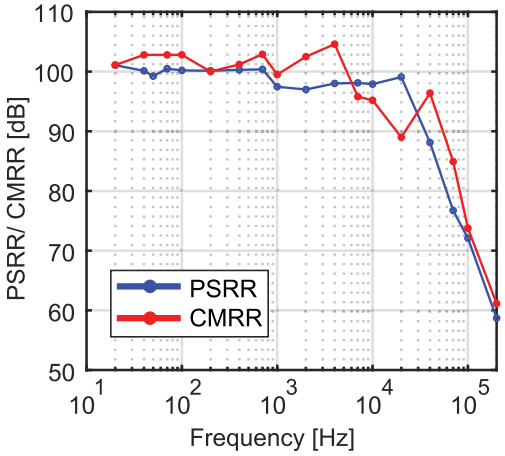


Fig. 19. PSRR and CMRR across input frequency.

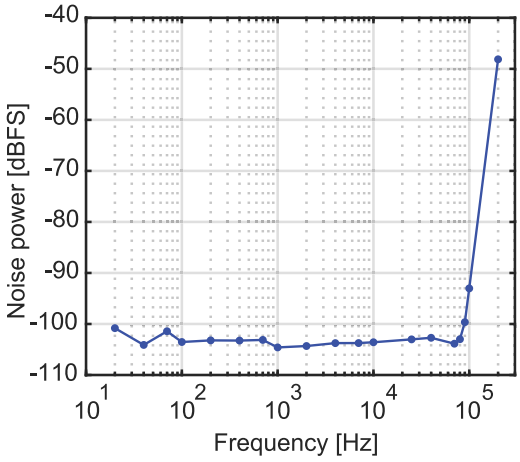


Fig. 20. Total integrated noise in a 20-kHz BW for different input frequencies with a −1.5-dB input amplitude.

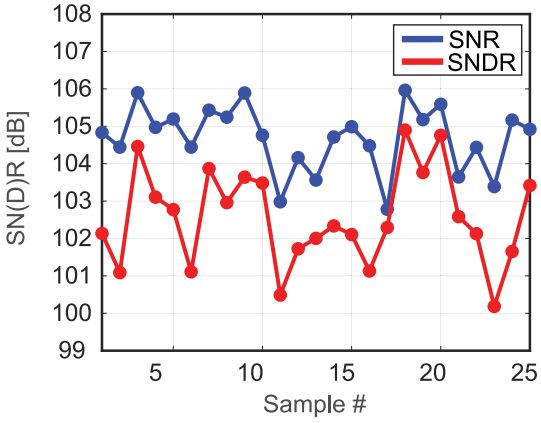


Fig. 21. SNR and SNDR across different samples for a −1.5-dB FS input amplitude at 1 kHz with a 3.5-MHz f_S.

with DWA turned "on" and "off." Even at this low OSR, it can be seen that the use of DWA improves the SNDR by nearly 30 dB.

The output spectrum with shorted inputs is shown in Fig. 18. Without chopping, the $1/f$-noise corner is around 10 kHz, and chopping the first-stage OTA at $f_{\text{chop}} = f_s/2$ reduces this to less than 10 Hz without affecting the modulator's noise floor.

Fig. 19 shows the power-supply rejection ratio (PSRR) for a 100-mV test signal on top of the 1.8-V supply voltage across frequency. The ADC reaches a PSRR of 99.2 dB at 50 Hz and stays above 97 dB over the entire audio band. Fig. 19 also shows the common-mode rejection ratio (CMRR) for full-swing common-mode inputs across frequency. Over the entire audio band, the CMRR remains above 89 dB.

As discussed in Section II, fast-changing out-of-band interferers can cause the $\Delta\Sigma$M to overload due to the limited tracking capability of the SAR ADC. As shown in Fig. 20, the ADC's noise floor remains stable in the presence of −1.5-dB FS interferers at frequencies <80 kHz. Compared with a previous zoom ADC [5], this represents a 2× improvement in interferer robustness and is mainly due to the use of a 2-bit $\Delta\Sigma$M.

Fig. 21 shows the SNR and SNDR for −1.5-dB FS input signals at 1 kHz for 25 different samples. It can be seen that the variation in their peak SNR and SNDR is around 3–4 dB, which demonstrates the robustness of a switched-capacitor zoom ADC to process variation.

Table I summarizes the performance of the zoom ADC and compares its performance to that of other state-of-the-art audio ADCs and previous zoom ADCs. Compared with a recent zoom ADC [5], its energy efficiency (FoM$_S$) is nearly 3 dB better even though its OSR is 30% lower. Compared with a

TABLE I
TABLE OF COMPARISON

	This work	*ISSCC'20* [3]	*JSSC'20* [5]	*JSSC'18* [6]	*JSSC'18* [4]	*JSSC'17* [9]	*ISSCC'16* [2]	*JSSC'16* [19]	*JSSC'16* [20]
Architecture	**DT Zoom**	CT 3-Level	CT Zoom	CT 3-Level	DT Zoom	DT Zoom	CT FIRDAC	CT M-Bit	DT 1-Bit
Tech (nm)	**160**	65	160	65	160	160	180	160	65
Area (mm^2)	**0.27**	0.28	0.27	0.14	0.25	0.16	1	0.21	0.25
Supply (V)	**1.8**	1.2	1.8	1.2	1.8	1.8	1.8	1.6	1
Power (μW)	**440**	134	618	68	280	1120	280	390	800
f_s (MHz)	**3.5**	8	5.12	6.144	2	11.29	6.144	3	6.4
BW (KHz)	**20**	24	20	24	1	20	24	20	25
SNR_{max} (dB)	**107.5**	101	108.1	94.8	119.1	106	99.3	93.4	100.1
$SNDR_{max}$ (dB)	**106.5**	99.4	106.4	94.1	118.1	103	98.5	91.3	95.2
DR (dB)	**109.8**	103.5	108.5	98.2	120.3	109	103.6	103.1	103
FoM_{SNDR}* (dB)	**183.1**	181.9	181.5	179.5	183.6	175.5	177.8	170.5	170.1
FoM_S ** **(dB)**	**186.4**	186	183.6	183.6	185.8	181.5	182.9	180.2	177.9

*FoM_{SNDR} = SNDR + $10\log_{10}$(BW/Power) **FoM_S = DR + $10\log_{10}$(BW/Power)

recent DT zoom ADC [4], this design achieves similar energy efficiency and area while achieving 20× more BW. Although the FoM_S of the negative-R CT $\Delta\Sigma$M in [3] is nearly the same, this work achieves 7 dB more SNDR and occupies about the same area in an older technology node. To summarize, compared with the other audio ADCs, this design uses one of the lowest sampling frequencies to achieve the highest energy efficiency and the highest DR.

V. CONCLUSION

A DT zoom ADC for audio applications has been presented. A low-power analog feed-forward technique reduces the leakage of the SAR ADC quantization noise and improves the overall SNDR. The combination of a 5-bit asynchronous SAR ADC, a third-order loop filter with a notch, and a 2-bit quantizer results in a thermal noise limited system with high DR (109.8 dB) at low OSR (87.5). Furthermore, the low internal swing of the zoom ADC's loop filter enables the use of energy-efficient current-starved OTAs with high gain and high PSRR. The use of fully differential sampling confers high CMRR, while chopping the first-stage OTA only when it is disconnected from the loop filter results in low offset and 1/f noise without introducing chopping artifacts. These advances lead to an ADC with a state-of-the-art Schreier FoM (186.4 dB) and SNDR FoM (183.1 dB).

REFERENCES

[1] R. van Veldhoven, M. Lammers, L. Van Der Dussen, and K. Mabtoul, "A low-cost 4-channel reconfigurable audio interface for car entertainment systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2020, pp. 168–170.

[2] S. Billa, A. Sukumaran, and S. Pavan, "Analysis and design of continuous-time delta–sigma converters incorporating chopping," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2350–2361, Sep. 2017.

[3] M. Jang, C. Lee, and Y. Chae, "A 134 μW 24 kHz-BW 103.5db-dr ct $\Delta\Sigma$ modulator with chopped negative-R and tri-level fir DAC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2020, pp. 1–3.

[4] S. Karmakar, B. Gönen, F. Sebastiano, R. van Veldhoven, and K. A. A. Makinwa, "A 280 μW dynamic zoom ADC with 120 dB DR and 118 dB SNDR in 1 kHz BW," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3497–3507, Dec. 2018.

[5] B. Gonen, S. Karmakar, R. van Veldhoven, and K. A. A. Makinwa, "A contin uous-time zoom ADC for low-power audio applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1023–1031, Apr. 2020.

[6] M. Jang, C. Lee, and Y. Chae, "Analysis and design of low-power continuous-time delta-sigma modulator using negative-R assisted integrator," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 277–287, Jan. 2019.

[7] A. Sukumaran and S. Pavan, "Low power design techniques for single-bit audio continuous-time delta sigma ADCs using FIR feedback," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2515–2525, Nov. 2014.

[8] Y. Chae, K. Souri, and K. A. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.

[9] B. Gonen, F. Sebastiano, R. Quan, R. van Veldhoven, and K. A. A. Makinwa, "A dynamic zoom ADC with 109-dB DR for audio applications," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1542–1550, Jun. 2017.

[10] E. Eland, S. Karmakar, B. Gönen, R. van Veldhoven, and K. Makinwa, "A 440 μW, 109.8 dB DR, 106.5 dB SNDR discrete-time zoom ADC with a 20 kHz BW," in *Proc. IEEE Symp. VLSI Circuits*, Honolulu, HI, USA, Jun. 2020, pp. 1–2.

[11] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," *IET Electron. Lett.*, vol. 37, no. 12, pp. 737–738, Jun. 2001.

[12] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[13] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

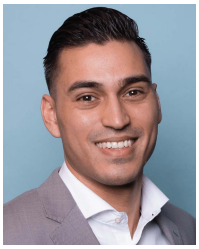
[14] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[15] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Piscataway, NJ, USA: Wiley, 2005.

[16] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2007, pp. 314–605.

[17] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, 1st ed. New York, NY, USA: Wiley, 1996.

[18] O. Choksi and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 12, pp. 906–917, Dec. 2003.
[19] C. De Berti, P. Malcovati, L. Crespi, and A. Baschirotto, "A 106 dB A-weighted DR low-power continuous-time $\Sigma\Delta$ modulator for MEMS microphones," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1607–1618, Jul. 2016.
[20] Y. H. Leow, H. Tang, Z. C. Sun, and L. Siek, "A 1 V 103 dB 3rd-order audio continuous-time $\Delta\Sigma$ ADC with enhanced noise shaping in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2625–2638, Nov. 2016.



Efraïm Eland (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees from the Delft University of Technology, Delft, the Netherlands, in 2017 and 2019, respectively, where he is currently pursuing the Ph.D. degree, with a focus on the design of scalable, energy-efficient, high-speed data converters, in collaboration with NXP Semiconductors, Eindhoven, The Netherlands.

From 2018 to 2019, he was an Intern with NXP Semiconductors.

Shoubhik Karmakar (Graduate Student Member, IEEE) received the B.E. degree in electrical and electronics engineering from the Birla Institute of Technology and Science, Pilani, India, in 2012, and the M.Sc. degree from the Delft University of Technology, Delft, The Netherlands, in 2017, where he is currently pursuing the Ph.D. degree.

His current research interests include energy-efficient data converters and high-performance class-D amplifiers for audio applications.

Burak Gönen (Member, IEEE) received the B.Sc. degree in electronics from Istanbul Technical University, Istanbul, Turkey, in 2012, and the M.Sc. degree (*cum laude*) in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2014, where he is currently pursuing the Ph.D. degree, with a focus on the design of energy- and area-efficient analog-to-digital converters for digital audio and sensor interfaces, in collaboration with NXP Semiconductors, Eindhoven, The Netherlands.

From 2011 to 2012, he was an Intern with Mikroelektronik Ar-Ge Ltd., Istanbul. From 2013 to 2014, he was an Intern with NXP Semiconductors. From 2012 to 2019, he was with Electronic Instrumentation Laboratory, Delft University of Technology. In 2019, he was a Senior Analog IC Design Engineer with Broadcom, Bunnik, The Netherlands. Recently, he joined Ethernovia, Zeist, The Netherlands, as a Senior Member of Technical Staff. His current research interests include high-performance data converters for wireline communications.

Mr. Gönen was awarded the First Prize at the IEEE SSCS Benelux Chapter Student Chip Design Contest in 2017. He was a recipient of the 2018-2019 IEEE SSCS Predoctoral Achievement Award.

Robert van Veldhoven (Senior Member, IEEE) was born in Eindhoven, The Netherlands, in 1972. He received the Ph.D. degree in electrical engineering from the University of Eindhoven, Eindhoven, The Netherlands, in 2010.

In 1996, he joined Philips Research, Eindhoven, and moved to NXP Semiconductors, Eindhoven, in 2006, where he is currently a Data Converter Fellow and an Architect leading a team of 15 engineers working on automotive grade data converters and sensor interfaces. He has (co)authored more than 15 International Solid-State Circuits Conference (ISSCC)/IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) articles. He holds over 25 U.S. patents.

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has resulted in 16 books, over 250 technical articles, and over 30 patents.

Dr. Makinwa is also a member of the Royal Netherlands Academy of Arts and Sciences and the Editorial Board of the PROCEEDINGS OF THE IEEE. He was a co-recipient of 15 best paper awards, including two from the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and three from the International Solid-State Circuits Conference (ISSCC). He is also the Analog Subcommittee Chair of the ISSCC and a Co-Organizer of the Advances in Analog Circuit Design (AACD) Workshop and the Sensor Interfaces Meeting. He has served as a Guest Editor of JSSC. At the 60th anniversary of ISSCC, he was recognized as a Top-Ten Contributor. He has served the IEEE Solid-State Circuits Society as a Distinguished Lecturer and as an elected member of its AdCom.