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A 94.1 dB DR 4.1 nW/Hz Bandwidth/Power Scalable DTDSM for IoT Sensing Applications Based on Swing-Enhanced Floating Inverter Amplifiers

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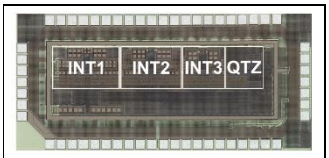
IoT sensing applications operating from batteries or harvested energy require microwatt data converters. To accurately measure small signals, they often need to achieve a high DR (>90dB) and better linearity than the transducers themselves (>14b) with a BW in the kHz range. IoT systems also often consist of multiple sensing modalities with different BW requirements and are often heavily duty-cycled to reduce power consumption. This paper presents a fully dynamic discrete-time delta-sigma modulator (DTDSM) that supports 4x bandwidth/power scaling without any programming overhead except for changing f_s, using a capacitively biased swing-enhanced floating inverter amplifier (SEFIA). The prototype, fabricated in 180nm CMOS, consumes only 4μW at 800Hz BW and achieves >87dB SNDR over 2 octaves of f_s, between 100 kHz and 400 kHz, and a DR of 94.1 dB while operating with an OSR of 125.

Simultaneously achieving fully dynamic operation and high resolution is challenging. Successive approximation register (SAR) ADCs, such as [1], are bandwidth and power scalable. However, they require power-hungry calibration schemes to reach linearity beyond the intrinsic matching of on-chip capacitors. DTDSMs [2], [3] have long been the architecture of choice for high-resolution applications, but their OTAs draw static bias currents, which do not easily scale with f_s on-the-fly without extra programming overhead. Furthermore, they typically require biasing and common-mode feedback (CMFB) circuitry, which takes extra time to settle after waking up when duty-cycled. Continuous-time (CT) DSMs exhibit high power efficiency [4] but suffer from the same drawbacks. In [5], a floating inverter amplifier (FIA) is proposed, which features fully dynamic operation by providing supply current with reservoir capacitors, but it has an ill-defined bias current, which is sensitive to threshold and supply voltage variations. It also has a limited output swing given by $V_{THN}+|V_{THP}|-2V_{DSAT}$, thus restricting their application.

This paper reports a 4x bandwidth/power scalable DTDSM that simultaneously achieves high resolution and ultra-low power (Fig. 1). We propose the capacitively biased SEFIA to address these challenges. The SEFIA has a larger output swing and a robust and f_s-adaptive operating point control compared to the conventional FIA [5] and does not require CMFB in contrast to conventional inverter-based amplifiers [2]. Swing enhancement and f_s-adaptive self-biasing are achieved with only switches and capacitors, thereby preserving the power efficiency and the fully dynamic nature of FIAs and enabling duty-cycled operation with simple clock gating. The 3rd order DSM employs a feedforward topology for its high linearity. Its 1-bit quantizer employs an FIA-based pre-amplifier and a Strong-Arm latch. The third integrator shares its supply reservoir with the pre-amplifier of the quantizer to further reduce power.

Fig. 2 shows a switched-capacitor integrator based on the SEFIA. Reservoir capacitors C_{res1} and C_{res2}, operating in a ping-pong sequence, supply the amplifier. During the sampling/auto-zeroing phase φ1, C_{res1} supplies the SEFIA, while C_{res2} is precharged to V_{DD}, and vice versa during the integration phase φ2. The capacitively biased SEFIA augments the conventional FIA [5] by auto-zero capacitors (C_c's) and dynamic biasing capacitors (C_i's), where C_i's serve as dynamic floating current sources. During φ1, the input transistors are diode-connected, which charges C_i and splits the gate potentials of the PMOS and NMOS. At the end of φ1, the gate voltages are stored on C_c's. When f_s is increased, the stored $|V_{GS}|$'s of the input transistors increase, thus adaptively boosting the OTA's bandwidth during the integration phase, where the amplifier is reconfigured as a class-AB current reuse amplifier. This enables bandwidth/power scaling of the DSM by simply varying f_s. The current efficiency g_m/I_D is also boosted by sizing C_i so that the input pairs operate in weak inversion during the entire integration phase.

On the contrary, the conventional FIA operates in strong inversion at the beginning of φ2 when $V_{DD}>V_{THN}+|V_{THP}|$. In [5], multiple supplies are used to ensure sufficient driving capability and power efficiency. When C_{res1} and C_{res2} discharge, the instantaneous bandwidth of the SEFIA reduces. To avoid any memory effect, a reset phase is introduced at the beginning of φ1 by shorting the differential outputs.



Chip micrograph of the ΔΣ Modulator.

The SEFIA does not require CMFB and the associated settling time after waking up when duty-cycled. During φ1, the output sampling capacitors C_{OUT} are precharged to V_{CM}, which defines the output common-mode level (Fig. 3 top). Supplying the SEFIA using reservoir capacitors forces equal total current through the NMOS and PMOS input pairs, so the output common-mode remains at V_{CM} during φ2, thus obviating CMFB [5]. In addition, since the PMOS and NMOS gates are split by the voltage across C_i at the end of φ1, the SEFIA's output swing is improved by the same amount and no longer limited by $V_{THN}+|V_{THP}|-2V_{DSAT}$. Fig. 3 (bottom) shows the simulated DC gain of a conventional FIA [5] and the proposed SEFIA across output swing. SEFIA expands the output swing by 1.8x, from 0.62V to 1.12V at 6 dB gain compression. When V_{DD} increases from 1.5V to 1.8V, the SEFIA's output swing increases accordingly. By contrast, the conventional FIA's output swing stays constant.

A prototype of the proposed DTDSM is fabricated in a 180nm process and occupies an active area of 0.75mm^2. The input sampling capacitance is 1pF. Fig. 4 shows an output spectrum when the ADC operates at an f_s of 200 kHz from a 1.5V VDD. Fig. 5 (top left) shows the SN(D)R as a function of input amplitude. It achieves 91.9dB(89.3dB) SN(D)R in 800 Hz BW. At this f_s, the DTDSM draws 4μW from supply. The prototype achieves a DR of 94.1 dB, leading to a Schreier FoM of 177.1 dB. Fig.5 also shows the power (bottom left) and SN(D)R (bottom right) as f_s is varied from 100 kHz to 400 kHz, where 14-bit linearity is maintained throughout. The power consumed in SEFIAs is less than half, highlighting its power efficiency. This DTDSM exhibits fully dynamic operation with 4.1 nW/Hz of signal BW and consistent SN(D)R without any extra programming overhead. To demonstrate the robustness of the proposed capacitive biasing scheme, Fig. 5 (top right) shows the SN(D)R as VDD is varied from 1.2V to 1.8V.

Fig. 6 compares the performance of this ADC with other state-of-the-art microwatt-level ADCs with similar bandwidth. It achieves the highest SNDR among power/bandwidth scalable ADCs. Compared to the microwatt DTDSM in [3], our prototype improves the FoM by >10 dB. It also achieves the lowest power consumption among ADCs in [6] with SNDR >80 dB despite being implemented in a 180nm process. In conclusion, the proposed SEFIA presents an attractive OTA design for power/bandwidth scalable, high-resolution, and ultra-low-power switched-capacitor circuits.

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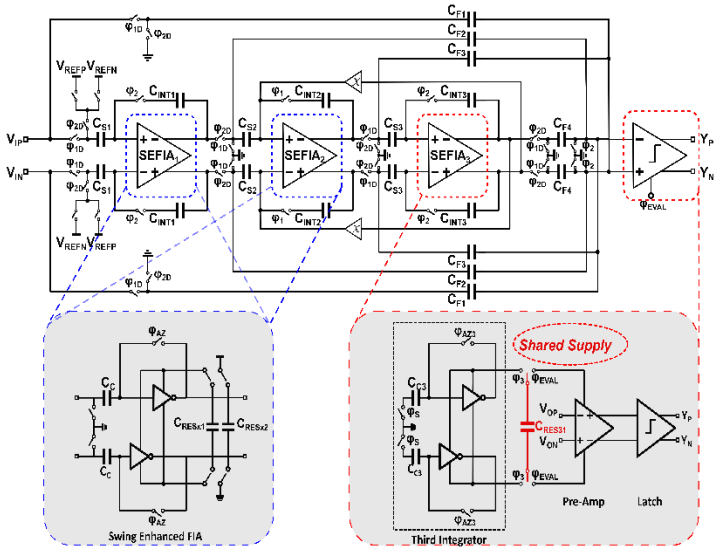

Fig. 1. Circuit schematic of ΔΣ Modulator

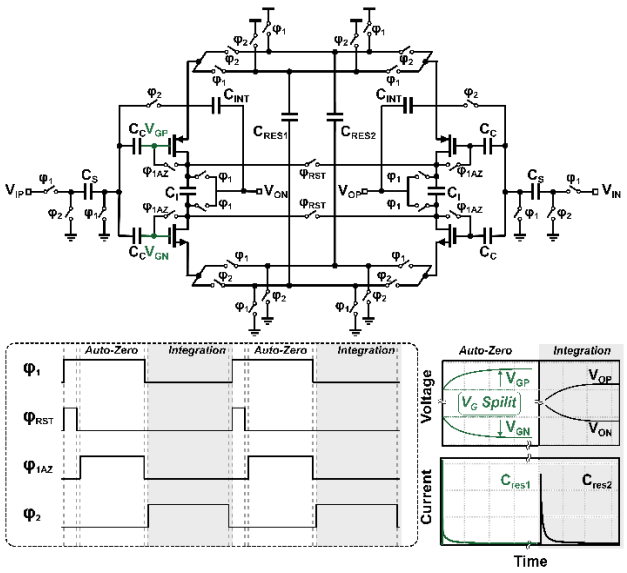

Fig. 2. Simplified circuit diagram of the proposed SEFIA and the corresponding timing diagram.

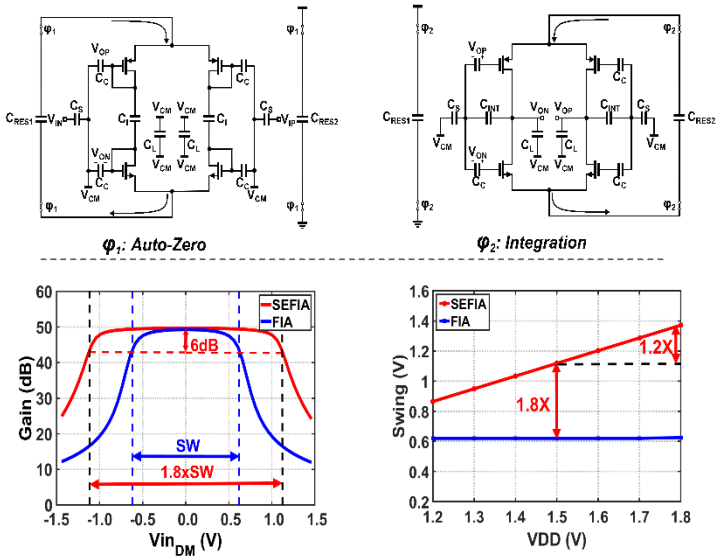

Fig. 3. Operation and output swing comparison of the proposed SEFIA and conventional FIA.

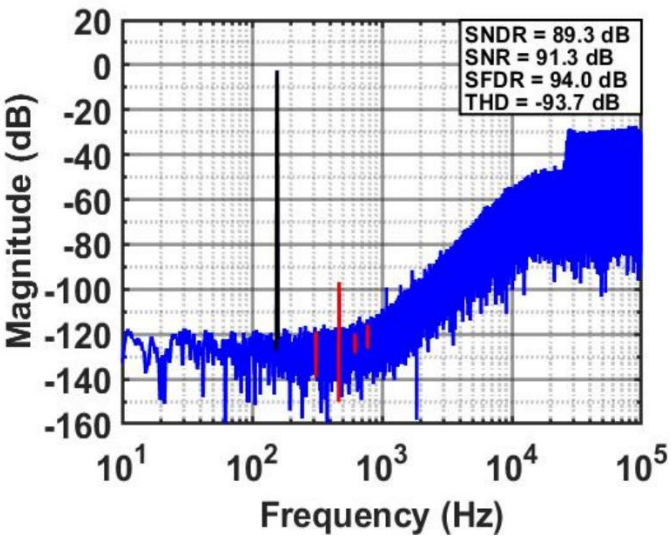

Fig. 4. Measured output spectrum at 200 kHz f_s.

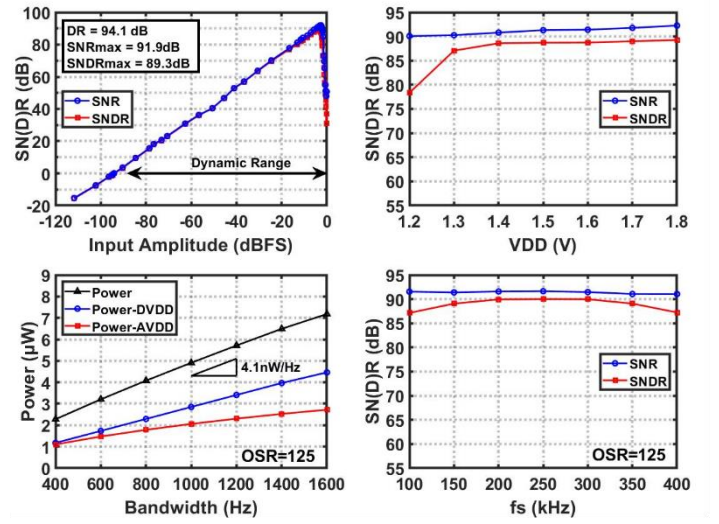

Fig. 5. (Top left) SNDR/SNR vs. input amplitude, (top right) SNDR/SNR vs. VDD, (bottom left) power consumption vs. Bandwidth, and (bottom right) SNDR/SNR vs. f_s when OSR=125.

	This Work	ISSCC'18 Gagnon-Turcotte	ISSCC'18 Yeknami	ISSCC'19 Konijnenburg	ISSCC'20 Jang	ISSCC'18 Chandrakumar
Process (nm)	180	130	65	55	110	65
Architecture	SCSD	SCSD	SCSD	SAR	CTSD	CTSD
BW/Power Scalable	Yes	No	No	Yes	No	No
Area (mm^2)	0.75	-	-	-	0.078	0.053
V_{DD} (V)	1.5	1.2	0.3	0.9	1	1.2
Power (μW)	4	4.4	0.18	0.9	6.5	4.5
f_S (Hz)	200k	500k	256k	32k	128k	400k
OSR	125	25	42.7	107	64	40
BW (Hz)	800	7k	3k	150	10k	5k
DR (dB)	94.1	-	-	-	81	96.5
SNDR (dB)	89.3	60.8	60	78.8	80.4	93.5
FoM_{DR}	177.1	-	-	-	172.9	187
FoM_{SNDR}	172.3	154.4	162.2	161	172.3	184

Fig. 6. Performance summary and comparison.