Waveform Generation for a MIMO Radar

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Master of Science Thesis

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Waveform Generation for a MIMO Radar

by

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Abstract

Multiple-input multiple-output (MIMO) radars achieve improved performance by the simultaneous transmission and reception of waveforms from different locations. Orthogonality of the transmitted waveforms is a requirement for allowing waveform separation at the receiver. In addition, signals with a large BT- product (e.g. coded signals) could be transmitted to achieve high Signal to Noise Ratio (SNR) due to pulse compression. This helps to radiate a larger amount of average power as a result of which range resolution (larger bandwidth) and detection capability improves. These techniques are indeed combined in Space - Time coded active antenna systems, where multiple codes are simultaneously transmitted through the different elements or sub-arrays of an active antenna.

My thesis, "Waveform generation for a MIMO Radar" involves the design and implementation of the Arbitrary Waveform Generation (AWG) Block for a multi-channel transmitter of such a MIMO radar test bed. The 8-channel AWG block is developed on an FPGA platform. Besides the AWG, there are the RF and antenna blocks in the multi-channel transmitter. The synchronization of the multiple transmitters is the essential pre-requisite to develop the system. Similarly the individual channels of the system need to be characterized by measuring the errors within the system. The test-bed will be used as a platform for generating and testing different waveforms (binary codes, multi-phase codes, complementary waveforms, etc.) that can provide the radar with required resolutions in range, space, velocity. This could in turn be used to analyze these signals using their ambiguity function in case of space-time adaptive processing. Finally, the influence of the errors on the ambiguity functions for colored waveform transmission could be studied.

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Chapter 1

Introduction

RADAR (Radio Detection And Ranging) is an electronic system that uses electromagnetic waves to detect the presence of objects. Radars can also be used to measure the range, direction and velocity of the target. Different properties of electromagnetic radiations such as reflection, scattering, constant speed and possibility for beam-forming are exploited in radar implementation. For example, when an electromagnetic wave propagating through a medium encounters another medium with a different refractive index, the wave undergoes reflection or scattering. This reflected energy indicates the presence of a target. Similarly, the constant speed of the electromagnetic waves in a homogenous medium offers the possibility to calculate the distance from the target. With the suitable control over the relative phase and amplitude of the signals beam-forming could be achieved and it gives directional transmission and reception of the electromagnetic waves to calculate the direction of target and finally, by virtue of Doppler shift, the velocity of the target could be determined.

1-1 Motivation

The two major functionalities of RADAR are detection of targets and estimation of target measurements like range, velocity etc. Most of the times, the environment under surveillance is a noisy one. And the two sources of interferences that influence the performance of radars are

1. Clutter: As Skolnik wrote in [1],"Clutter may be defined as any unwanted radar echo." For example, for surveillance radar, the echoes coming from ground, nearby trees, birds etc. are considered as clutter. Also, clutter is application specific i.e. clutter signals in one application could be the wanted signal in another application. Clutters, many a times, have large spatial extent thereby occupying more than a single range bin. On the other, hand most of the times sources of clutter are immobile. Thus, their effect could be removed by filtering the zero doppler data while processing the echo signals.

2. Jamming: Jamming is any un-desired, intentional, high power signal that disrupts the function of the radar. Jamming signals are very wide band signals most of the time. The location of jamming signal is localized and hence directional unlike clutter. But since the signal is wide band, it spreads the entire Doppler band.

1-2 Problem Statement

The purpose of this effort is to design and implement an Arbitrary Waveform Generator (AWG) for a multi-channel transmitter within a space time coded MIMO radar test bed. The test-bed will be used as a platform for generating and testing different waveforms (binary codes, multi-phase codes, complementary waveforms, etc.) that can provide required resolutions in range, space, velocity. The performance of various such waveforms could be analyzed by determining their ambiguity functions in case of space-time adaptive processing. Finally the influence of errors on the ambiguity functions for colored waveform transmission could be studied and therefrom optimum waveforms that can provide high (or specified) resolutions in range, space, velocity (Doppler) could be designed.

1-3 Thesis Outline

The introduction is followed by a description of various radar waveforms in Chapter 2. A detailed review of hardware configuration is presented in Chapter 3. The need for hardware characterization, methods and results are provided in Chapter 4. Chapter 5 concentrates on software architecture and performance testing of the AWG. Conclusions from the completed work and recommendations are focused in Chapter 6.

Chapter 2

Radar Waveforms

2-1 Introduction

This chapter describes the basic functional blocks that make a radar sysem. The chapter discusses various waveforms that have been used in the radar systems. At the end, the critical role in waveform design on radar performance and several strategies adopted in waveform design have been discussed.

2-2 Radar Systems

As described in the previous chapter, RADAR is an electronic system that uses electromagnetic waves to detect the presence of objects. The two main functionalities of the radar system are

1. Detection
2. Estimation

A radar system primarily consists of the following blocks as illustrated in Figure 2-1[1] and Figure 2-2[2].

The important modules that built a radar system, either CW or pulsed radar, are discussed below

2-2-1 Transmitter

The transmitter generates, up-converts and amplifies the waveform which is radiated to the space to detect the presence and position of a target.

[1]Merrill I. Skolnik, "Introduction to Radar Systems", McGraw-Hill Book Company, 1981
[2]Merrill I. Skolnik, "Introduction to Radar Systems", McGraw-Hill Book Company, 1981

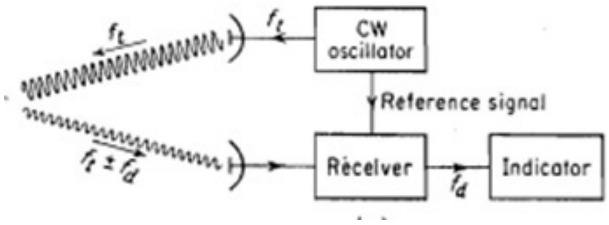


Figure 2-1: Continuous Wave Radar System

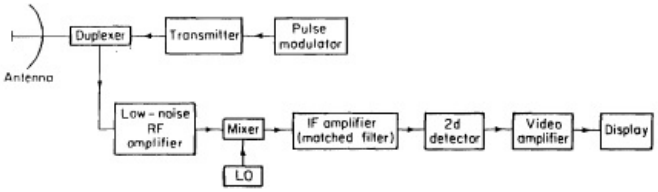


Figure 2-2: Pulsed Radar System

2-2-2 Antenna

Antenna is the transducer that converts the waveform to electromagnetic waves (transmission) and the received the echo signals from the targets to equivalent electrical signals (reception).

2-2-3 Receiver

The receiver is the signal conditioner that amplifies, filters and down-converts the received echo signals from the targets.

2-2-4 Signal processor and display

The received signal is processed to extract the position, direction velocity details of the target and displayed.

2-3 Radar Transmitters

A pulsed radar transmitter can be of the of the following types

2-3-1 Non Coherent transmitter

In a non-coherent transmitter, as the name describes, there is no phase relation maintained between the subsequent transmitted pulses. A typical non coherent transmitter, also called Keyed Oscillator Transmitter (KOT), consists of a high power radio frequency (RF) oscillator like magnetron that produces pulses at its rated frequency. The oscillator is turned on and off using a modulator and each pulse has a random initial phase. The lack of phase relation makes a non-coherent transmitter not suitable for Doppler processing.

2-3-2 Coherent transmitter

A coherent transmitter maintains phase relation among the transmitted pulses. A coherent transmitter, also called Power-Amplifier-Transmitter (PAT), consists of a waveform generator that generates the signals, which is amplified to sufficient level and transmitted. In other words, a coherent transmitter consists of a low power RF oscillator and an RF power amplifier.

In the space time coding based MIMO radar test bed, coherent transmitters are made use of.

2-4 Radar Waveforms

A variety of waveforms have been used for radars till date. Several properties of radar waveforms are discussed in [2], [3], [4]. Radar waveforms are application specific. The performance of radar depends on the properties of the waveform chosen. The following section describes various radar waveforms used in practice. As mentioned in section 2.2, the radars could be classified into the following categories based on the type of the signals transmission schemes employed.

2-4-1 Continuous Wave Radar

An un-modulated or modulated continuous signal is used in continuous wave (CW) radar. Such a system can detect targets using Doppler offset, but range measurements become difficult. Since the radar transmits continuous waves, the need for secondary antenna for reception arises which is considered as another short coming of such a system. An example for CW signal is shown in Figure 2-3. The codes used to generate the following figures are given in Appendix A.

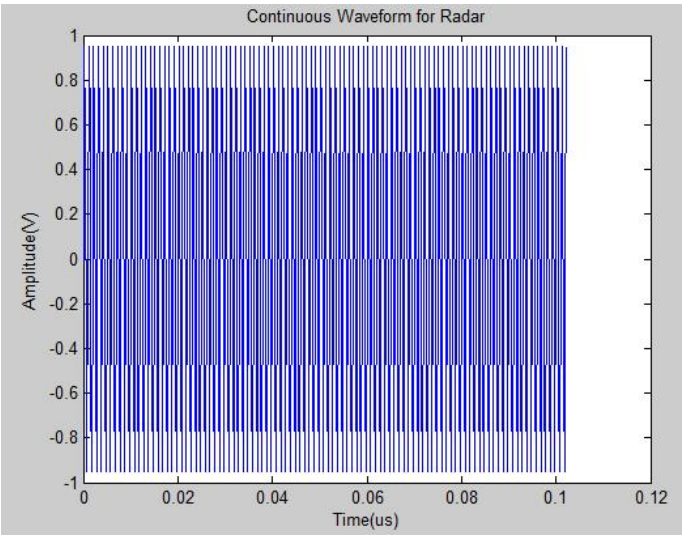


Figure 2-3: Continuous Wave Radar Waveform

2-4-2 Pulsed Radar

Pulsed radar transmits signals at regular time intervals. Unlike the CW radar, pulsed radars could give range measurements. But the selection of pulse width is a compromise between the required resolution of the system and the maximum detectable range. An example for pulsed waveform is given in Figure 2-4. Pulsed radars could be coherent or non-coherent as discussed in Section 2.3.

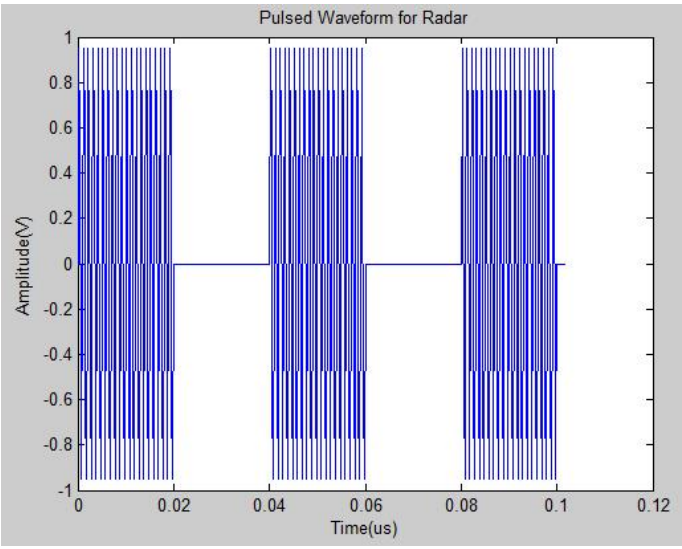


Figure 2-4: Pulsed Waveform for Radar system

Various characteristics of a radar system such as the accuracy, resolution, range, range-Doppler ambiguity etc. are decided by the radar waveforms. Thus the choice of radar waveform decides the performance of the system. For example, the shorter the pulse width of the pulsed radar, the more accurate resolution the system has. But at the same time, short pulse cannot support a good detection range. These issues were solved by the technique of Pulse Compression. Pulse compression shares the idea of transmitting a long pulse with some modulation embedded which spreads the energy over the bandwidth necessary for the required resolution. Pulse compressed waveforms have larger time bandwidth (BT) product compared to uncompressed pulses whose BT=1.The technique of pulse compression in waveforms is employed either in the form of Frequency coding or Phase coding. This gives rise to following waveforms.

2-4-3 Linear Frequency Modulation (LFM)

An LFM signal is a frequency modulated waveform whose carrier frequency varies linearly with time, over a specific period. This is one of the oldest and frequently used waveforms. It finds application in CW and pulsed radars. Since an LFM waveform is a constant amplitude waveform, it makes sure that the amplifier works efficiently. Also, this waveform spreads the energy widely in frequency domain. Mathematically, an LFM signal could be expressed as

$$X(t) = Acos(w_0 + kt^2) \tag{2-1}$$

where, A is the amplitude of the signal,

$w_0 = 2\pi f_0$, where f_0 is the carrier frequency,

k is the rate of frequency increase

Figure 2-5 shows how an LFM signal would look like.

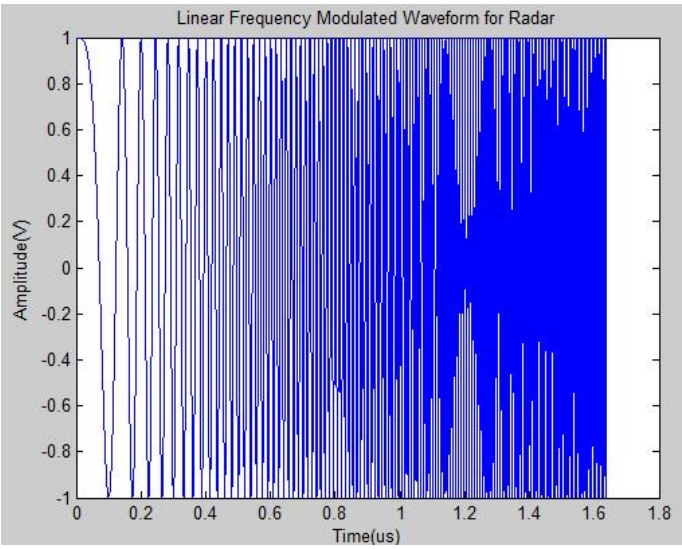


Figure 2-5: Linear Frequency Modulated waveform

Instead of continuous sweep of frequency, the frequency variation with respect to time can be made of N equal steps, giving rise to linear step FM. In this case, the instantaneous frequency f_n of the nth pulse would be

$$f_n = f_0 + n\Delta f, \tag{2-2}$$

f_0 is the carrier frequency and Δf is the frequency step.

2-4-4 Non-linear Frequency Modulation

Here, the carrier frequency of the waveform is varied according to any non-linear law over time. The variation can be symmetrical or asymmetrical over time. Some of the nonlinear frequency modulations can be summed up as quadratic FM with even symmetry about the carrier frequency, quadratic FM with odd symmetry. With the advent of high speed digital hardware another class of signals evolved where the FM is digitally generated as a staircase stepped FM. The non-linear frequency modulation could be expressed as

$$X(t) = Acos(w_0 + kt^2 + k_2(t)) \tag{2-3}$$

where A is the amplitude of the signal $w_0 = 2\pi f_0$, where f_0 is the carrier frequency $k_2(t)$ is any non-linear function of t.

2-4-5 Costas FM

A variation of the discrete FM uses N contiguous pulses with discrete frequency. This type of waveforms is known as Costas FM. This is similar to a frequency hopping system where the FM frequencies are chosen so that resulting waveform has a minimum sidelobe over the delay Doppler plane. Costas FM signals are generated using Welch construction or using some frequency hopping codes. Figure 2-6 represents the time-frequency relation in Costas FM.

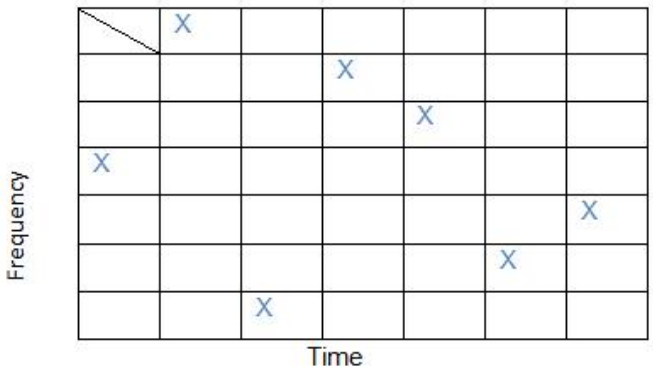


Figure 2-6: Costas FM

As mentioned earlier, another way of implementing pulse compression in waveforms is by means of phase modulation (PM). The pulse is divided into a number of subpulses of equal duration and the phase of each subpulse is varied according to a coded sequence. This can be broadly classified into binary and M phase coding. Following are various popular phase coded waveforms.

2-4-6 Binary phase coding

In this technique, the phase of any subpulse takes any of the two values, either 0 or 180 degrees, according to the sequence. Various types of binary codes with good autocorrelation properties are used in bi-phase coding. Some of the commonly used codes are Barker codes, Maximal length sequences. Figure 2-7 demonstrates the binary phase coded waveform and the code sequence.

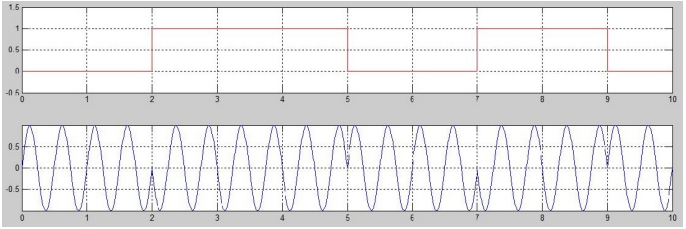


Figure 2-7: Binary Phase coded waveform

2-4-7 Polyphase coding

In poly phase coding or M phase coding, the phase of the subpulse takes any of the M arbitrary values. Frank codes, polyphase Barker sequence, P codes, quadriphase-coded waveform are some of the commonly used sequences in Polyphase coding. The range sidelobes for polyphase coded waveforms are lower than that of binary-coded waveform of same length, but the Doppler performance gets deteriorated.

2-5 Recent trends and considerations while choosing radar waveforms

As mentioned before, the selection of waveform has a great influence on the performance of radar. Two significant challenges encountered in radar design are clutter and jamming. Clutter often comes from a large area; hence spreads across all range bins. Jamming is a strong interfering signal often localized, but with a wide frequency spectrum. This in turn corrupts Doppler processing. This call for the need for a spatial and temporal filtering of signals arises, in other words space-time processing. Phased array antennas combat against the interfering signals with their improved directivity. The multiple antennas in a phased array are fed with phase shifted copies of the transmit waveform. The technique of beam forming, which is achieved by the proper selection of individual phase shift, results in steering the main lobe towards desired direction and nulling out the undesired directions. The technique could be implemented in the receiver also. It also improves the scan rate compared to mechanical scanning. When it comes to a space time coded system, the multiple transmitters transmit orthogonal signals in different directions. The receiver after getting a sum of these reflected orthogonal signals performs the signal processing which is equivalent to the transmit digital beamforming.

Recent research in this field has been around the idea of transmission and reception of multiple signals, as in, Multiple Input Multiple Output (MIMO) radar as studied in[5]. MIMO radars differ from the phased array systems in the fact that each antenna transmits different waveforms while phased array uses weighted copies of a single waveform. Thus, MIMO radar comes with additional degrees of freedom as discussed in [6] and gives the experimental results promising enhanced performance [7]. MIMO radar comes in two configurations, with collocated antenna and widely distributed antenna. In MIMO radar with colocated antennas, transmit and receive antennas are placed close enough that they see the target alike. Several advantages of this system including improvement in parameter identification, flexibility for transmit beampattern design, applicability of adaptive arrays etc. has been discussed in [8]. Also the authors of[8] show that the maximum number of targets identified is Nt times larger than the phase array counterpart, where Nt is the number of transmit antennas. Another configuration being discussed in [9] is widely separated MIMO radar also called Statistical radars, where the antenna arrays are widely separated. As a result, transmit-receive antennas see the target differently. Targets with very high Radar Cross Section (RCS) fluctuations can benefit from this technique. This frequency diversity in radar is similar to the robustness of MIMO wireless communication against channel fading. Thus, targets with high RCS fluctuations could be seen differently from different directions and the scintillation in RCS is exploited to make the system work better.

The diverse waveforms used in MIMO radars can be correlated or uncorrelated. Although most of the works [7], [8], [9] discuss the performance of systems using uncorrelated (orthogonal) waveforms, the signals need not be orthogonal in general. As suggested in [10] the detection properties of a signal is a criterion for waveform selection. The waveforms with maximum SNR at the receiver give better detection results. Another class of waveforms could be optimal estimation waveforms [10] according to information theory used in communication. Selection of waveforms based on information theory has been discussed in [11], [12]. Another approach to select waveforms based on estimation theory has been dealt with in [13], [14]. In [15], [16] the authors suggest the optimization, by optimizing the covariance matrix of waveforms based on Cramer-Rao bound. The discussion on performance of Costas codes on Orthogonal Frequency Division Multiplexing (OFDM) and Goaly complementary codes, as in MIMO communication systems, is dealt in [17]. With the use of uncorrelated waveforms in MIMO radars, the individual transmit-receive pairs are easily separable from the composite received signal. The use of uncorrelated waveforms also gives broad spatial patterns, which is suitable when the direction of target is not known a priori. As shown in [18], with the proper selection of signal cross-correlation matrix the beampattern of the array could be controlled. The limitation in the number of orthogonal signals and their cross correlation property might appear a problem to the waveform diversity in MIMO radar, but methods like the concept of circulating codes as suggested in [19] discusses the possibility of transmitting the time shifted copies of same waveform. And finally as suggested in [20] the waveform diversity could be implemented in various multiple access techniques: For example, intrapulse coding as in Code Division Multiple Access (CDMA), transmitting from a single antenna at a time featuring Time Division Multiple Access (TDMA), using of orthogonal waveforms to making use of Frequency Division Multiple Access (FDMA) and finally use of different polarization.

2-6 Conclusion

This chapter discussed different types of radars and several waveforms used in radar systems. The critical role of waveform selection in radar performance has been described together with recent techniques used to design robust radar waveforms.

Chapter 3

Arbitrary Waveform Generator

3-1 Introduction

The importance of waveform design has been discussed in the previous chapter. This would require robust hardware platforms that can help the realize the waveforms and test for their performance. The objective of this thesis is to develop the transmitter waveform generator for a space-time adaptive radar test-bed.This chapter discusses the considerations and requirements for chosing the hardware platforms, followed by the description of the hardware modules that build up the AWG.

Prior to the selection of suitable hardware platform to realize the system, the initial waveform requirements have been decided and the following Table 3-1 gives the specification of the waveforms to be generated using the system.

Parameter	**Value**
Bandwidth (MHz)	200
Intermediate Frequency (MHz)	300
No. of channels	8

Table 3-1: Waveform Parameters

The AWG should be capable of generating eight synchronous waveforms with bandwidth as high as 200 MHz. Also the waveforms generated should be at an Intermediate Frequency (IF) = 300 MHz. The generation of waveform at IF eases the filter design in the subsequent stages. Given this bandwidth and IF specification, the waveform is a wideband signal spanning from 200MHz to 400MHz. The Nyquist criterion gives the minimum sampling rate aliasing for the system to prevent as follows,

$$F_s >= 2 * F_m, where \tag{3-1}$$

F_s is the minimum sampling rate of the system and F_m is the maximum frequency generated in the system

Thus, a minimum of 800 MHz sampling rate is required to realize the system with specifications given in the Table 3-1.

The memory requirement to store the waveform is considered next. The memory utilization to store the waveform with a given bandwidth and given duration is calculated as follows. The calculation has been made for two situations, for a bandwidth of 200MHz and 100 MHz. The calculation is repeated for two Pulse Repetition Frequencies (PRF), for 1kHz and 10kHz.

The baseband waveform is assumed to have a bandwidth (Δf) of 100MHz, PRF of 1kHz (pulse repetition interval, PRI= 1/PRF) and a duty cycle of 10 percent. As per Nyquist sampling rate, the waveform should be sampled at least at a rate twice the bandwidth. Hence the time duration between the samples (Δt) is given as follows,

$$\Delta t = 1/(2 * \Delta f) \tag{3-2}$$

$$\Delta t = 5ns \tag{3-3}$$

If N is the number of samples, we have

$$(N-1) * \Delta t = PRI \tag{3-4}$$

Thus,

$$(N-1) * \Delta t = 1ms \tag{3-5}$$

or N is approximately equal to 200k samples.

Assuming each sample to be 16bits wide, 400kB of memory are required to store a waveform of 100 MHz bandwidth with a PRF of 1kHz.

In order to store a waveform with 100 pulses, a memory depth of 40MB is needed.

Given below is a Table3-2 with the memory requirement for the hardware platform while operating in the burst mode. Memory requirement for different waveform bandwidth and pulse repetition frequencies have been computed.

Bandwidth (MHz)	**PRF1 = 1kHz**	**PRF1 = 10kHz**
BW1 = 100	40 MB	4 MB
BW1 = 100	80 MB	8 MB

Table 3-2: Memory requirement

The general scheme of the proposed eight channel MIMO radar transmitter for the Space-time test bed could be represented as given in Figure 3-1.

The radar transmitter consists of three blocks namely,

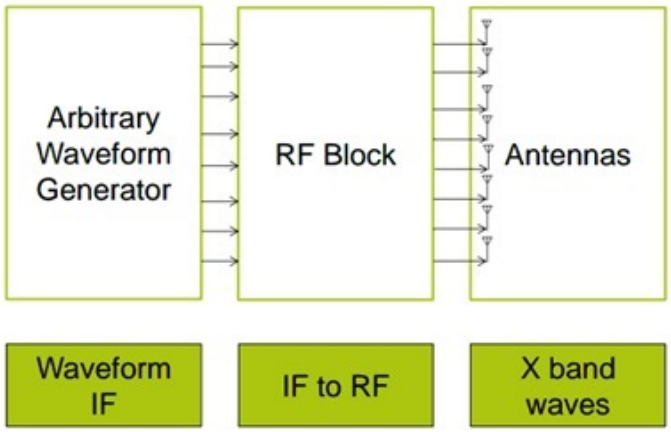


Figure 3-1: Building blocks of MIMO radar transmitter

1. Waveform Generator: This block generates the waveform with required modulation and bandwidth at the designated IF (300 MHz). As per the requirement, 8 waveforms with bandwidth as high as 200 MHz is to be generated. Since the space time coded radar test bed is a coherent system, all the signals shoud be synchronous.

2. RF Block: This block up-converts the IF generated by the preceding block to the final RF (X-band) and amplifies the signals to sufficient power level before transmission. This module consists of eight parallel banks of bandpass filters that filters the IF output of the AWG, upconverts the waveforms to the X band and amplify to the rated power level. Appendix B gives details on the proposed scheme for the RF Module.

3. Antennas: This block converts the X band signal output from the RF module to the final electromagnetic waves. Each of the eight channel outputs of the RF module is fed to respective inputs of the 8 element antenna array. Each element in turn could be a sub array of antennas.

In the first version for the space time coded MIMO radar, the receiver is designed to be a single channel. Thus the system shall be an 8X1 radar system.

The significant role of waveforms in the performance of any radar system has been discussed earlier. This calls for the need for potential hardware platforms to generate and test such signals. The initial waveform design could be carried out with the help of various system design software like Math Works Matlab and Simulink, NI LabVIEW. These platforms offer the possibility to analyze and understand the properties of the waveforms and its impact on performance on the radar system. This also helps to optimize the waveforms to give the required performance. Once the waveform design is completed, suitable hardware platforms are required to generate and test them.

The waveforms generation could be carried out in two ways,

1. Analogue domain: A Voltage Controlled Oscillator (VCO) is a typical example for an analogue domain waveform generator. For example, varying the tuning voltage of a VCO results in frequency swept waveform generator.

2. Digital domain: Several new waveform synthesizers are available in either in Application Specific Integrated Circuit (ASIC) forms and in programmable logic forms. The Direct Digital Synthesis (DDS) is an example for ASIC type digital waveform synthesizer and devices like Field Programmable Gated Array (FPGA) are programmable logic devices capable of generating any arbitrary signals.

In [21] various waveform generation platforms such as DDS, FPGA, Monolithic Microwave Integrated Circuits (MMIC) and Radio Frequency (RF) circuits with their advantages and disadvantages have been discussed. In analogue circuits that use VCOs, the settling time of the device is an important factor that can affect the radar performance. Also, the development and testing of customized waveforms is not possible. The digital counterparts, on the other hand, DDS or FPGAs offer fast switching capabilities together with flexibility in waveform design. With the unprecedented and sustained growth in semiconductor industry, high performance, high speed processors, data convertors and other reconfigurable devices are available. The current available 22nm semiconductor technology promises the availability of such reconfigurable digital platforms that makes the task of developing agile waveforms for MIMO radars easier and opens the possibility to improve the performance of future systems. These digital platforms provide adaptability and make excellent choices for the class of Software Defined Radar. With these possibilities, the digital domain platforms have been identified as the best option to develop the system.

3-2 Digital Waveform Synthesizers

The flexibility to reprogram and generate arbitrary waveforms offered by the digital waveform synthesizers makes excellent choice to develop the Arbitrary Waveform Generator (AWG) for the MIMO radars. As suggested in [22] three main hardware platforms are offered in digital domain waveform synthesis.

3-2-1 Direct Digital Synthesis (DDS)

A DDS is a frequency synthesizer that consists of a phase accumulator, phase to sine converter and a Digital to Analog Converter (DAC). Digitized samples of the time-varying signal are generated followed by a digital-to-analogue conversion. DDS primarily generates periodic waveforms for example sinusoids, triangular and square waveforms DDS also offers linear, non-linear frequency sweep features and digital modulation techniques like Amplitude Shift Keying (ASK), Phase Shift Keying (PSK), Frequency Shift Keying (FSK) etc. When compared with analogue frequency synthesizers, these digital systems offer better phase noise, stability, fine resolution and settling time. DDS is a potential candidate for Frequency Modulated Continuous Wave (FMCW) systems. [23] suggests the implementation of radar systems based on DDS platforms while [24] uses a hybrid of DDS and Phase Locked Loop (PLL) combining the merits of both. One of the disadvantages of DDS is its spurious response. The phase accumulator truncation error, phase-to-sine mapping errors, DAC nonlinearities and quantization are some of the sources of the spurious response. This necessitates in careful frequency planning. Also, the types of waveform that could be generated are limited. Thus it fails to function as an arbitrary waveform generator.

3-2-2 Random Access Memory (RAM) Loop System

A RAM based loop play backs the digital samples of waveform stored in the on-board memory. A typical system consists of an on board memory of sufficient length followed by a DAC. Memory length is a critical factor. Arbitrary waveforms designed using previously mentioned software could be loaded and repeatedly played. This platform does not support any further signal processing prior to transmission if required. As a result, they become unsuitable for a software defined radar platform.

3-2-3 Digital Signal Processor (DSP) and Field Programmable Gated Arrays (FPGA)

With their high power and speed, these general purpose processors prove to be the excellent platform to implement high speed signal processing algorithms. FPGAs and DSPs have dedicated units to optimize the process and enhance the speed of operation. Additionally, the vast amount of resources inside these devices opens room for the implementation of a multi-channel system as in MIMO. With rapid growth in FPGA and data converter technologies, the concept of Software Defined platforms is nearing reality. Most of the manufacturers come up with numerous Intellectual Property (IP) cores and design tools which make algorithm implementation easy.

Another advantage of the above mentioned waveform synthesizers or AWGs in general, is the stability. Unlike the analogue circuits with discrete components with variable tolerances, these digital waveform synthesizers produce stable frequencies. When it comes to a multi-channel system, all the channels need to be identical and these platforms prove to be more suitable for the development of test-beds. Required waveform with sufficient bandwidth at desired Intermediate Frequencies (IF) could be generated using these platforms. This could be followed by an up conversion to the final RF band, amplification and transmission.

3-3 Arbitrary Waveform Generator

From previous discussion on various available options for waveform synthesizers, it is clear that FPGAs offer the best solution. Especially when it comes to the design and implementation of a test-bed, the re-programmability and provision for immense resource in terms of power and memory makes FPGA the best choice. Typical waveform generation process (in digital domain) involves the following processes as

1. *Signal generation*: The signal could be designed and generated using any software like MATLAB or LabVIEW

2. *Storage*: The samples thus generated need to be stored in a memory. Depending on the duration of the signal, the memory could be chosen appropriately. For shorter signals internal memory could be made use of, while longer signals may require on board memory.

3. *Signal Processing*: Depending on the application, some level of signal conditioning might be required. This might include processes like digital up conversion, filtering etc. This could be implemented on FPGA.

4. *Digital to Analogue Conversion*: The high speed digital output lines of the FPGA give the digital value of the signal. A DAC is required to generate the analog equivalent of the signal. The DAC may or may not have a driver amplifier succeeding it.

5. *Filtering*: The output of any sampled system contains harmonics and unwanted components that need to be filtered.

The test bed for this work has been designed for an eight channel transmitter. The waveform generator module should generate eight synchronized waveforms simultaneously. This has been realized using the hardware modules summarized in the table below. Since it was decided to go with an FPGA platform, National Instruments Flexible Reconfigurable Input Output (FlexRIO) boards have been chosen. A FlexRIO board consists of a high power FPGA with an on-board memory and access to high speed digital input/output lines. The NI 7962 FlexRIO family has been chosen as the FPGA platform. This board gives the flexibility to be configured either as an input or output board depending on the adapter module chosen. Thus among the processes listed above, the FlexRIO board is involved in Signal Storage and Signal Processing. In case of the arbitrary waveform generator for space-time radar test bed, the board needs to be configured as an output board. The Active Technologies AT1212 dual channel DAC board has been chosen as the adapter module for the FlexRIO board. This module is involved in the process of Digital to Analogue Conversion. The output of the adapter module is not filtered. The Filtering is currently included as the initial step in the RF Module.

Thus the following configuration as shown in Table D-1 has been chosen to develop an eight channel waveform generator.

Module	**No.of units**
PXIe-1082, 8 Slot 3U PXI Express Chassis	1
NI PXIe-7962R FlexRIO FPGA Module (Virtex-5 SX50T, 512 MB RAM)	4
NI PXIe-PCIe 8361 with MXI-Express for PXI Express	1
NI PXIe-6674T Timing and Synchronization Module with OCXO	1
AT 1212 14 bit, 1.25 GS/s, 2 Channel, DC-Coupled Analog Output Adapter Module	4

Table 3-3: Hardware Configuration

The following sections give details of the modules that make up the AWG. Please refer to the hardware manual document for the datasheets of the modules.

3-3-1 NI PXIe-1082

The NI PXIe-1082 chassis consists of a high-performance 8-slot PXI Express Backplane. It has been designed for a wide range of test and measurement applications. With a data rate

of 1GB/s dedicated to each slot, a total of 4GB/s total system bandwidth could be achieved. The chassis has three PXI Express slots, one PXI Express slot with system timing control, and four PXI Express hybrid slots (that accept both PXI and PXI Express) to plug peripheral modules. A small description on the functionalities of individual slots is given in the following section. Figure 3-2[1] shows the layout of the chassis and description on individual slots as given below.

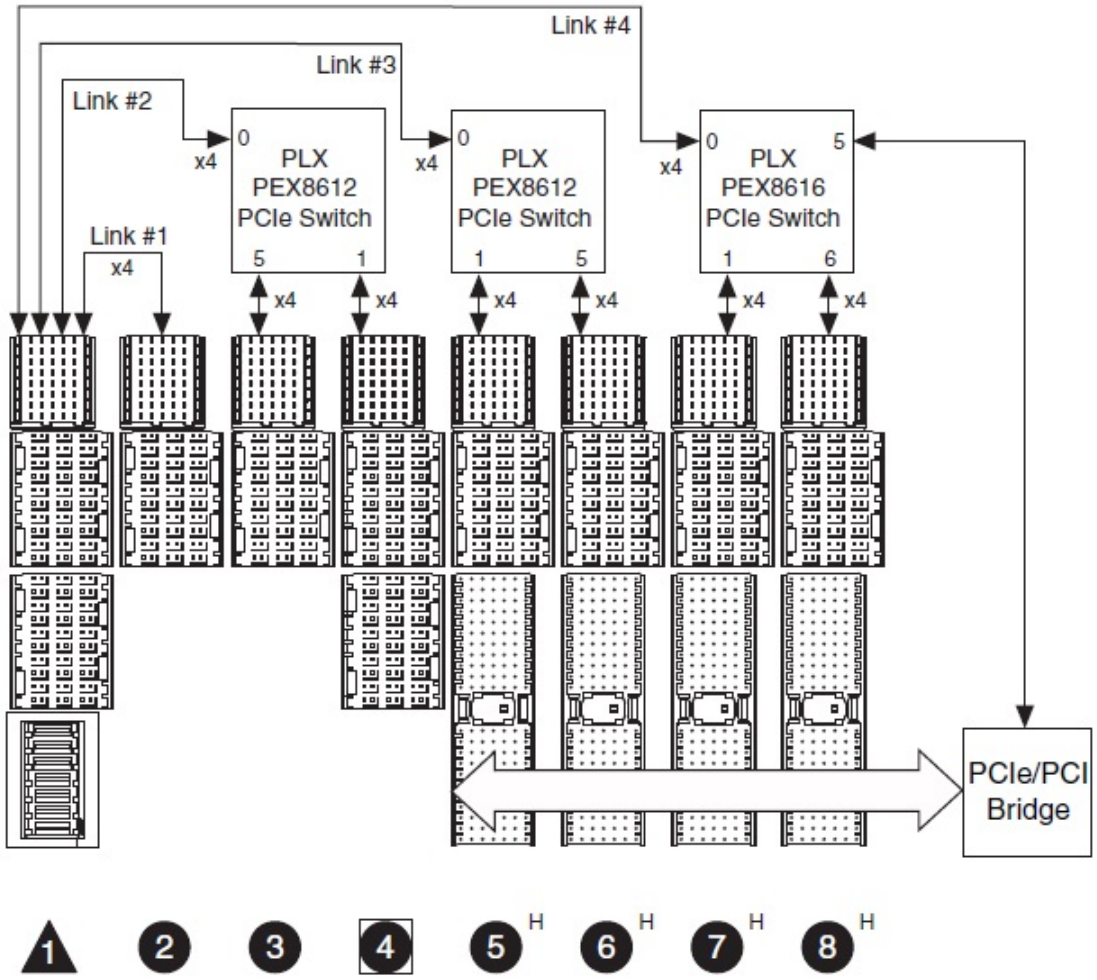


Figure 3-2: Layout of NI PXIe 1082 chassis

Slot1 - System Controller Slot

This is the first slot of the chassis. Through the backplane, the system controller slot maintains connections to the rest of the slots (slots 3 through 8) via PCIe switches. Slot 2 is directly connected to the system controller slot. By default, the system controller will control the power supply.

[1] http://sine.ni.com/ds/app/doc/p/id/ds-336/lang/nl

Slot 2 and Slot 3 - PXI Express (PXIe) Peripheral Slots

Slots 2 and 3 can accept PXIe peripheral modules of the following types.

1. A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot
2. A Compact PCI Express (CPCIe) Type-2 Peripheral with x4 or x1 PCIe link to the system slot

Slot 4 - System Timing Slot

The fourth slot of PXIe 1082 chassis is the system timing slot. This slot can accept the following categories of modules

1. A PXIe System Timing Module with x4 or x1 PCI Express link to the system slot
2. A PXIe Peripheral with x4 or x1 PCI Express link to the system slot
3. A CPCIe Type-2 Peripheral with x4 or x1 PCI Express link to the system slot

The system timing slot has 3 dedicated differential pairs (PXIe DSTAR) connected to each hybrid peripheral slot as shown in the following figure Figure 3-3[2]. This differential pair could be used for high-speed triggering, synchronization and clocking. The system timing slot also provides a single-ended (PXI Star) trigger connected to every slot. The system timing slot also provides the signal PXI CLK10 IN and PXIe SYNC CTRL using which it may provide a 10 MHz reference clock and a timing signal to the backplane of the chassis.

Slot 5-8: Hybrid Peripheral Slots

These four slots in the NI PXIe 1082 chassis could be populated with hybrid peripherals. A hybrid peripheral slot can accept the following peripheral modules

1. A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot
2. A CPCIe Type-2 Peripheral with x4 or x1 PCIe link to the system slot
3. A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2.
4. A CPCI 32-bit peripheral on the backplane 32-bit PCI bus The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus.

[2]http://www.ni.com/pdf/manuals/372752b.pdf

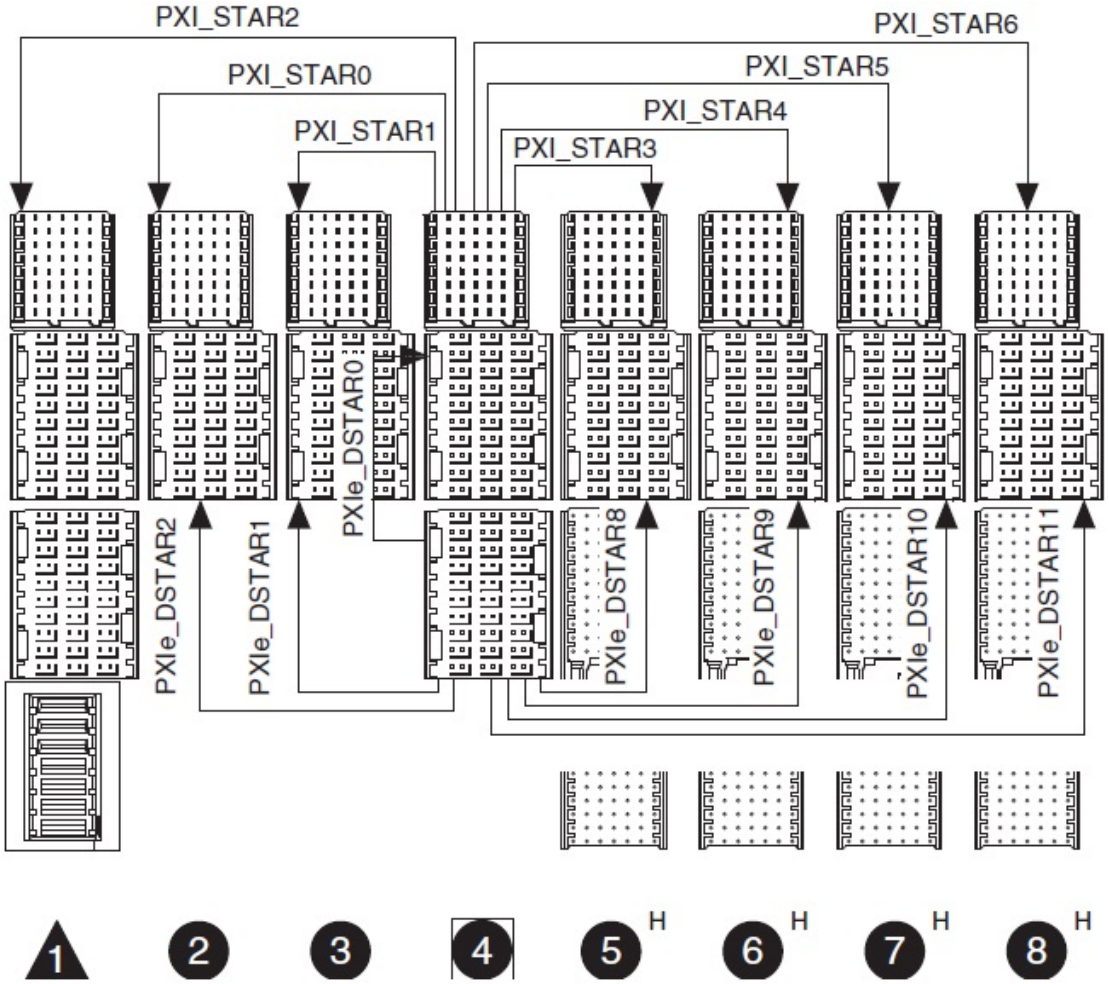


Figure 3-3: Layout of NI PXI DStar A clock to different slots

3-3-2 NI PXIe-7962R

The hybrid peripheral slots of the chassis have been populated with NI PXIe-7962R NI FlexRIO FPGA Module. This PXIe NI FlexRIO FPGA modules feature Xilinx Virtex-5 SX50T FPGAs with 512MB of onboard DRAM (two banks, 256MB each). The Virtex 5 SXT versions of FPGAs are optimized for high-speed digital signal processing (DSP) with around 288 DSP slices for single-cycle multiplication and filtering functions. The DSP slices are embedded modules dedicated to high speed multiplication and filtering. These FPGAs are programmed to store and playback the waveform continuously. Four such NI FlexRIO boards are connected to slots 5 through 8 of NI PXIe chassis 1082. These boards have two time base reference sources onboard - a 40MHz crystal oscillator and a PXIe 100 MHz.

3-3-3 NI PXIe-PCIe8361 with MXI Express for PXIe-PC control of PXI

The PXIe systems could be controlled from PCI Express-equipped desktop or server PC with the MXI-Express, PXIe modules could be used as if they are boards directly installed in the

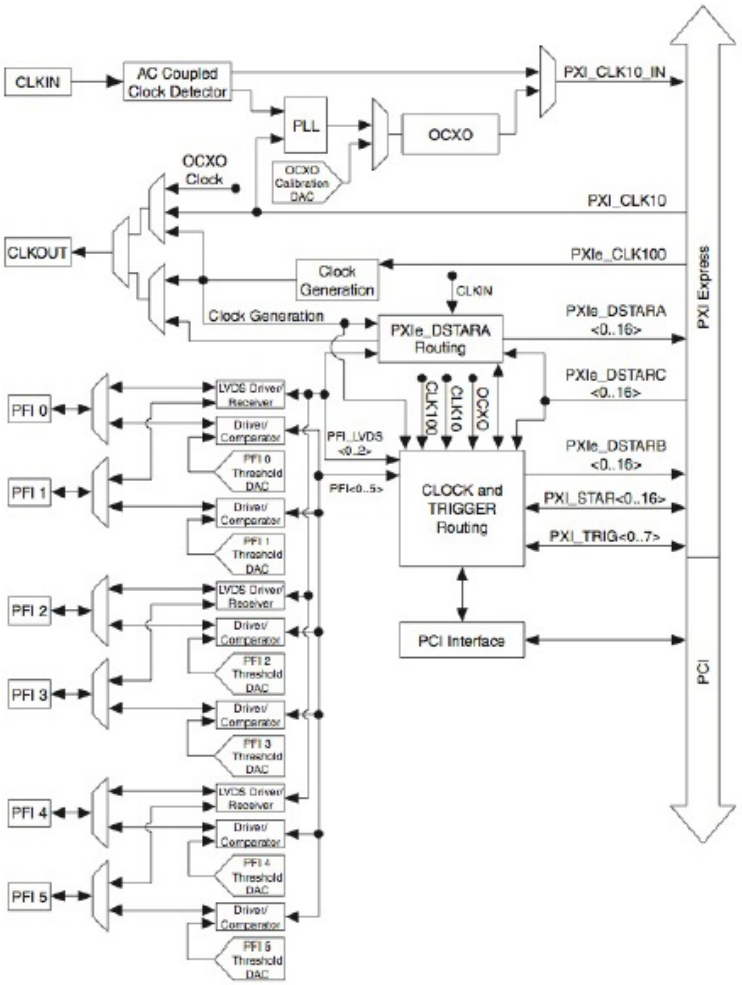


Figure 3-4: Layout of NI PXIe-6674T Timing and Synchronization Unit

computer.

3-3-4 NI PXIe-6674T - Timing and Synchronization Module

This module helps in onboard routing of internal and external clock and trigger signals. This module also facilitates the synchronization of multiple PXIe and PXI chassis. An onboard high-stability 10 MHz OCXO has been provided. Also provides high-resolution DDS clock generation in the range 0.3 Hz to 1 GHz. Thus NI PXIe-6674T generates two types of clock signals - a highly stable 10 MHz clock based on an onboard precision OCXO reference, and a second clock as high as 1 GHz from the DDS clock. Although the references for these two clocks are different, it is possible to lock them to a common source and synchronize them. Figure 3-4[3] depicts the clock and trigger signals generated and routed by the timing and synchronization module.

[3] http://sine.ni.com/ds/app/doc/p/id/ds-261/lang/nl

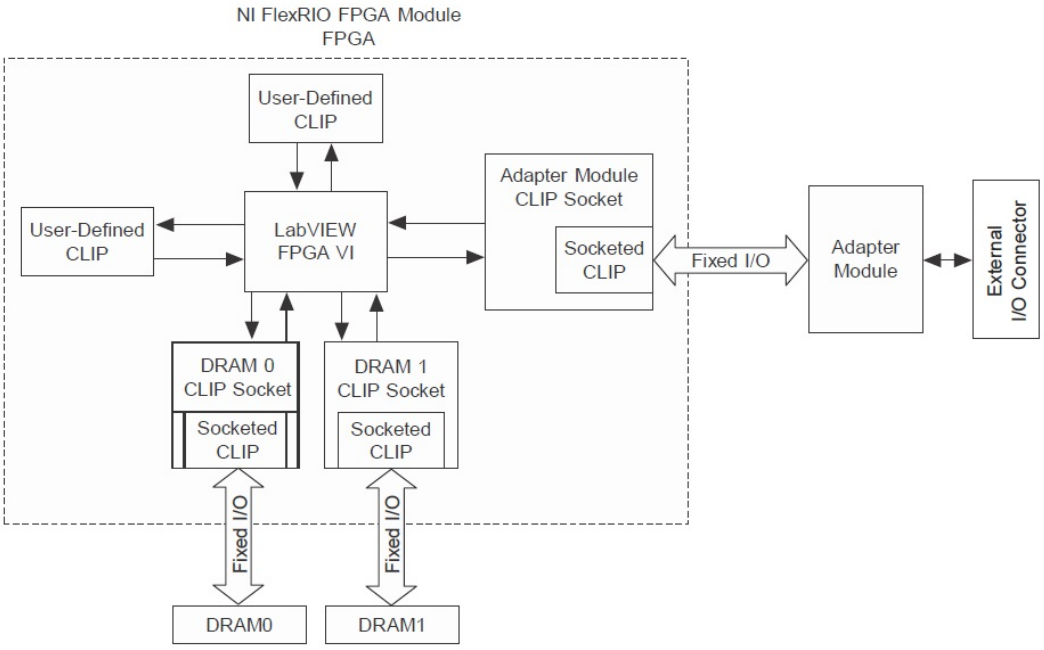


Figure 3-5: Interface between FlexRIO and Adapter Module

3-3-5 AT 1212 14-bit, 1.2 GS/s, 2 Channel, DC-Coupled Analog Output

The NI FlexRIO platforms allow the use of reconfigurable Input Output devices to be plugged into them. The adapter module used in this application is a two channel DAC module provided by Active Technologies. This analog output board has two 14 bit DACs that can run at a maximum of 1.2 GS/s rate and with 480 MHz analogue bandwidth.

3-3-6 Interface between FlexRIO and Adapter module

The FlexRIO module can be used with a wide variety of adapter modules. The interface between the two is taken care of by Component Level Intellectual Property (CLIP). An NI FlexRIO supports two types of CLIP

1. User-defined CLIP: Used to insert HDL IP into an FPGA target, VHDL code could be integrated with an FPGA Labview Virtual Instrument (VI) code.
2. Socketed CLIP: Used to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The schematic showing the communication and data exchange using CLIPs is as shown in Figure 3-5 [4].

[4] http://www.activetechnologies.it/000download/AT1212UserManual.pdf

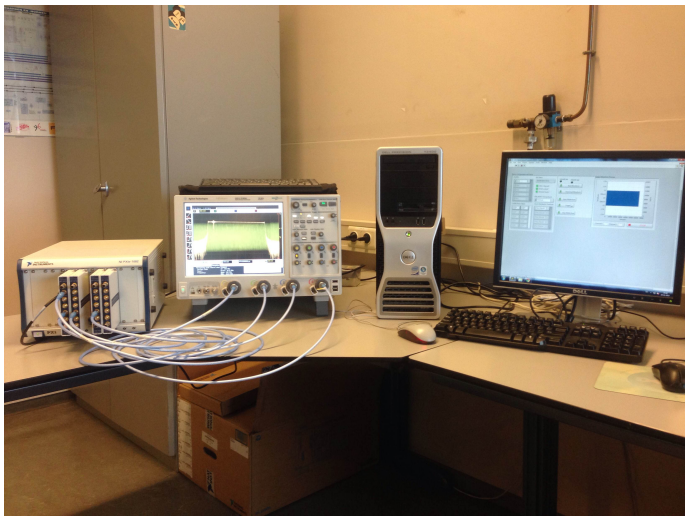


Figure 3-6: AWG test set-up

The fully configured AWG Module is illustrated in Figure 3-6. The Host system generates the waveform, transfers it to the FPGAs via DMA FIFOs. The analogue output of the AWG is tested and captured using the digital storage oscilloscope.

3-4 Configuration with RF hardware

The final experimental set up of the space time radar system with the RF block and antenna could be represented as shown in Figure 3-7[5]. The eight channel AWG is connected to a multi-channel RF block consisting of filters, mixers and amplifiers. Finally the up-converted, amplified signal is fed to the antennas. Receive data (sampled using the Spectrum Analyzer) could be processed with the transmit sequence in the computer.

[5] http://www.activetechnologies.it/02products/at1120overview.htm

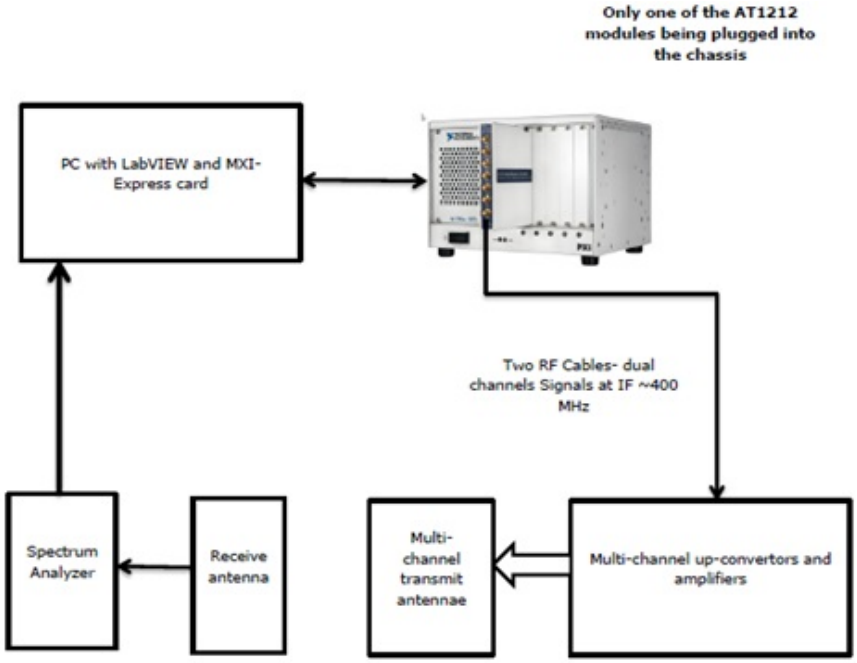


Figure 3-7: Configuration of AWG RF Hardware

3-5 Software Requirement

The National Instruments hardware modules used to set up the waveform generation test-bed could be programmed using the LabVIEW software. The programming of the Virtex 5 FPGA in the FlexRIO board is supported by LabVIEW FPGA module. The AT1212 module requires LabVIEW 2012 and LabVIEW FPGA 2012 versions. Hence the computer has been configured with the following items.

1. Windows 7 OS
2. LabVIEW 2012
3. LabVIEW FPGA 2012
4. NI RIO Drivers
5. NI FlexRIO Adapter Module Support

3-6 Conclusion

This chapter introduced the requirements for the AWG to be designed and implemented. In the subsequent section, study has been made on the available technologies to implement and operate the same. The following section gave details of the hardware modules that have been chosen to realize the waveform generator. The chapter has been concluded with the details of the integrated AWG that could generate waveforms for the space time coded MIMO radar.

Chapter 4

Hardware Characterization

4-1 Introduction

The previous chapter discussed about the different hardware modules that are used to build the 8 channel AWG. Since the two main modules i.e. the FPGA and the adapter module are from different vendors, it was suggested to characterize the complete channel for various performances before using the platform to generate waveforms. This chapter discusses the characterization of the combined hardware. Several parameters of the combination has been measured and analyzed.

The combined modules have been tested for the following parameters. A single channel of AWG is a sampled system consisting of a FlexRIO board with an adapter module with two DACs. The first step is to characterize the channels of the AWG and account for any offsets and errors. Some of the factors contributing to errors and their influence on system performance are discussed below.

4-2 Measurement Scheme

The AWG hardware module characterization has been done using the scheme as shown in Figure 4-1. Several measurements have been done by generating test waveforms in the computer using LabVIEW 2012 and LAbVIEW FPGA 2012. These waveforms are loaded in the FPGA and played back from the AWG. The measurements are done using Agilent Digital Storage Oscilloscope,DSO X 91604A. The AWG specifications for several parameters have been characterized. The following section gives details on the parameters that have been measured, the results and some recommendations to correct these offsets.

4-2-1 DC Offset

In electronic circuits, very often a non-zero output voltage is measured even when the input voltage is zero. This offset is termed as dc offset. The presence of significant level of DC

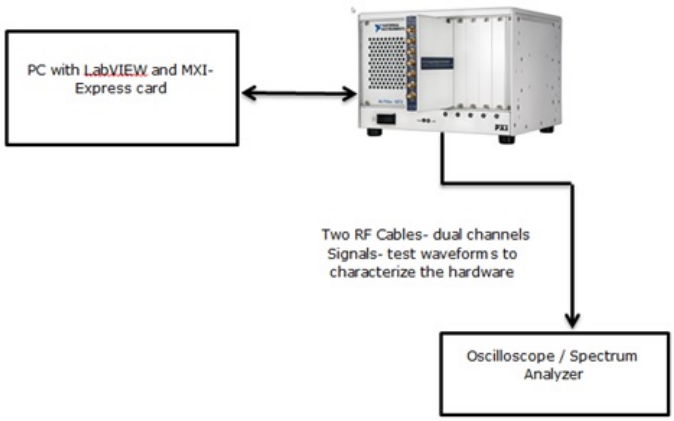


Figure 4-1: Measurment setup for the AWG hardware characterization

offset in a system manifests as saturation of the succeeding circuits and ultimately reducing the dynamic range of the system. Thus it is important to measure the dc offset of individual channels and suppress them in case they exceed the acceptable maximum level. For the eight channel AWG, the variation in dc offset across individual channels may alter the performance of the eight channels, hence the channels would no longer be identical.

Measurement

Each channel has been programmed to output zero voltage. Corresponding output voltage of each channel has been measured and tabulated. Table 4-1 shown below gives the measured values for the eight channels for the AWG.

AO 0+(mv)	**AO 0-(mv)**	**AO 1+(mv)**	**AO 1-(mv)**
-6.7	3.2	1.7	3.4
-1.9	0.0	3.0	4.6
3.3	5.1	-1.6	1.9
2.0	2.6	1.3	3.9

Table 4-1: Measured DC Offset

AO n + corresponds to the positive terminal of the Analog Output channel n of the FlexRIO. AO n- corresponds to the negative terminal of the Analog Output channel n of the FlexRIO.

Methods of compensation

There are often various methods of compensating dc offset like feed-back control, feed-forward control, pre-distortion etc. These values could be used to pre-distort while generating the waveforms. In our system, the maximum observed dc offset is -6.7 mV, which corresponds to less than 0.2 percent of full scale DAC reading.

4-2-2 Time Offset

The time offset among channels of a system refers to the lead or lag of individual channels with respect to each other. It is often desirable to have zero or very minimal offset among the channels. The time offset could be either fixed or variable. When the offset is fixed, it translates to a fixed phase shift among the channels. When the offset is dynamic, also known as Jitter, it translates to the phase noise of the system.

Measurement

Each channel has been programmed to output the square waveform of particular frequency. The rising edge of all the channels have been triggered and compared. The table shown below gives the measured values for the eight channels for the AWG. The measurement gave offset values that were fixed and repeated the same value every time. The maximum value as given in Table 4-2 is around 160 ps. For a waveform of 200 MHz bandwidth (5 ns pulse width), this corresponds to 3.2 percent of pulse width. Hence this delay is within manageable limits.

AO	**RIO0-RIO1(ps)**	**RIO0-RIO2(ps)**	**RIO0-RIO3(ps)**	**RIO2-RIO3(ps)**
AO0-	-21.3	-45.6	-78.4	124
AO0+	-21.5	-46.3	-79.5	125.8
AO1-	-34.8	-65.8	92.3	157.9
AO1+	-37.6	-69.3	89.8	159

Table 4-2: Measured Time Offset

RIO n corresponds to the nth FlexRIO device of the AWG AO n + corresponds to the positive terminal of the Analog Output channel n of the FlexRIO. AO n- corresponds to the negative terminal of the Analog Output channel n of the FlexRIO.

Methods of compensation

It has been observed that the time offset values are fixed; thus, the measured values could be used to compensate while generating the waveforms. The time offset is of great importance since the the AWG to be implemented needs to be a synchronous system.

4-2-3 Spurious Free Dynamic Range (SFDR)

Spurious Free Dynamic Range is defined as the ratio of strength of the fundamental signal to the strongest spurious signal in the output. Hence, SFDR one of the important specifications to analyze the frequency domain performance of a sampled system. Our AWG system gives differential output with a maximum of 4.4 Volts peak-to-peak (2.2 V amplitude) or a single ended output of 2.2 V peak-to-peak (1V amplitude). It has been noticed that while driving the AWG at the rated maximum gave distortions at the output and a noisy spectrum. The

amplitude dependence of the spurious performance has been noticed and studied. Figure 4-2 shows the spectrum of DAC output when generating a 300 MHz sinusoid at DAC full scale rated voltage.

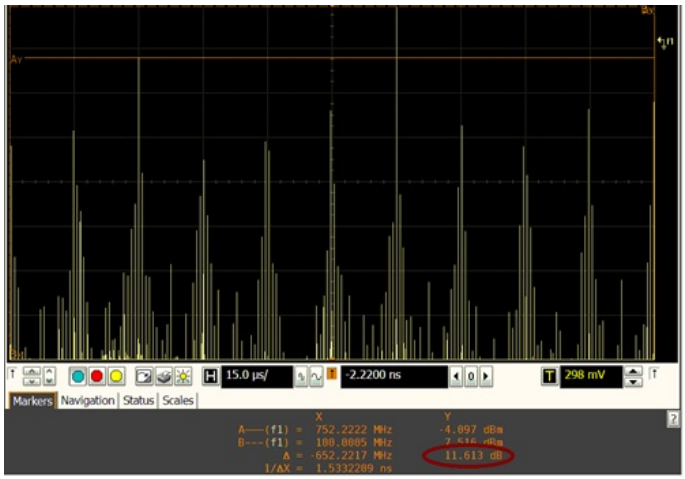


Figure 4-2: DAC full-scale output spectrum

A drastic change is observed when the DAC was operated at half full rate. The spectral purity at this half rate as shown in the following figure proved the amplitude dependence of the DAC board. This reduction in amplitude improved the SFDR of the system by almost 20 dB as shown in Figure 4-3

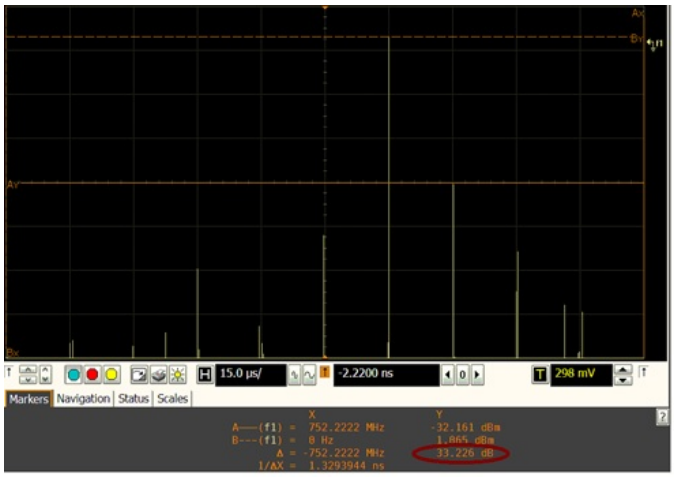


Figure 4-3: DAC half full-scale output spectrum

It has been confirmed that the system gives optimum results when operated at half the maximum value. This dependence on amplitude encouraged to study the SFDR of the system over the first Nyquist zone.

Measurement

The AWG is programmed to generate various tone signals (from 0 to 625 MHz, with 10MHz offset). For the generated frequencies till 310 MHz, the most significant source of spur was identified as the second harmonic frequency. Beyond that, the image frequency folded back to the first Nyquist region acts as the source of spurious. The difference in power level between the signal of interest and the strongest spurious component is measured and the following graph shows the SFDR (red curve) for the generated frequencies in the first Nyquist zone. Figure 4-4 also shows the location of spur (blue curve) for all the generated frequencies.

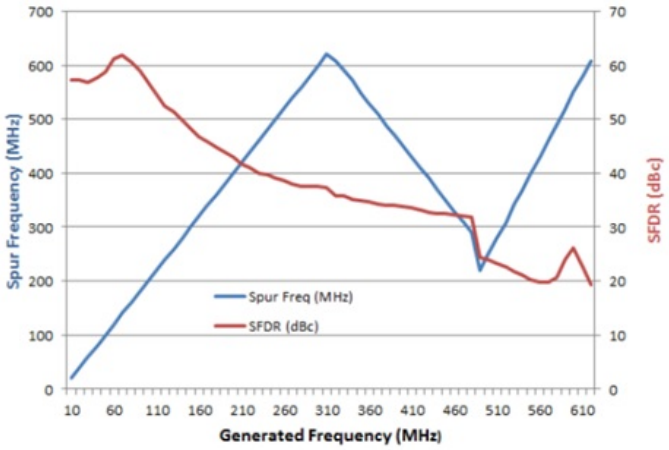


Figure 4-4: DAC SFDR and Spur Frequency in First Nyquist Zone

The SFDR of the system over the whole Nyquist region has been measured. It is evident that the systemŠs spurious performance gets deteriorated as frequency increases. Figure 4-5 shows the results over the frequency range 200 MHz to 400 MHz. It is clear that the worst case SFDR is 34dB.

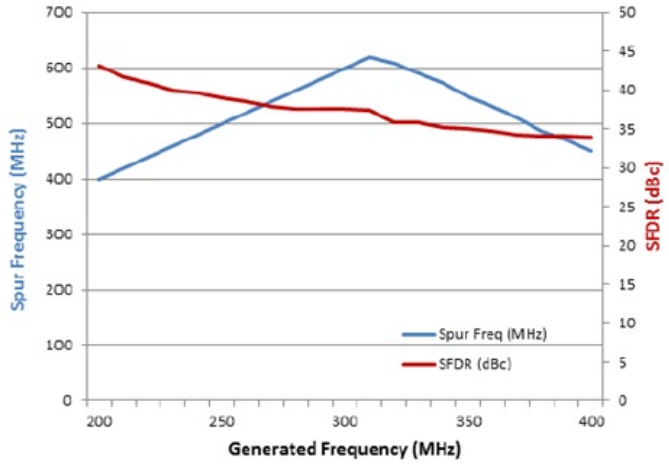


Figure 4-5: DAC SFDR and Spur Frequency in the proposed region of operation

The amplitude dependence and spurious response of our system was compared with an avail-

able commercial product from Tektronix - AWG 5014B. This is a dedicated four channel AWG. The spurious response of both the systems has been compared till 370 MHz. From Figure 4-6 shown below it is clear that till 300 MHz, our system has a performance either on par with or better than the Tektronix system.

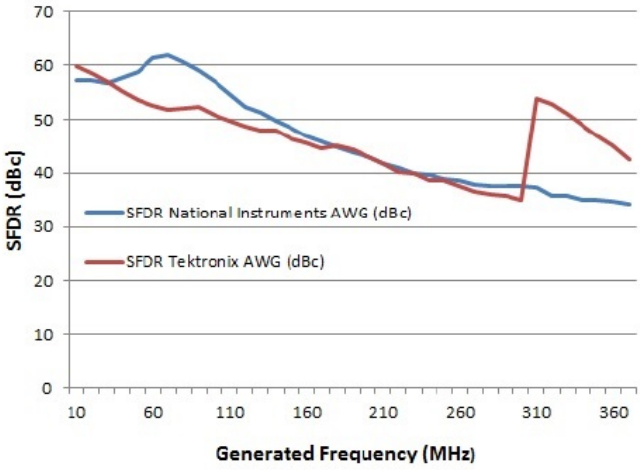


Figure 4-6: DAC SFDR and Spur Frequency in the proposed region of operation

Methods of compensation

The SFDR measurement results could be used to carefully select the Intermediate frequency. The result suggests that lowering the IF would give better spurious performance. But at the same time this would create stringent filtering requirements. Hence a judicious selection of the IF could be made using this information. Also it is to be noted that the output of the DAC contains no filter. Hence this spurious performance results could also be used to design a suitable filter at succeeding stages.

4-2-4 Frequency Response

The output amplitude response of the system over the frequencies to be generated is another important factor to be measured. Since the DAC is a sampled system, the output follows a sinc response. This would in turn result in a non-linear response in frequency. When generating a wideband signal with bandwidth as high as 200MHz, the amplitude response over that bandwidth needs to be reasonably flat. Otherwise it may cause signal distortion. Hence the amplitude response of the system over the first Nyquist band was studied. Figure 4-7 shown below shows the amplitude response of the system. Over the bandwidth of our interest, an amplitude drop of 2 dB is noticed. This non-flat envelope behavior may result in distorted signals. This has to be taken in to account at the receiver also while comparing at the matched filter processing.

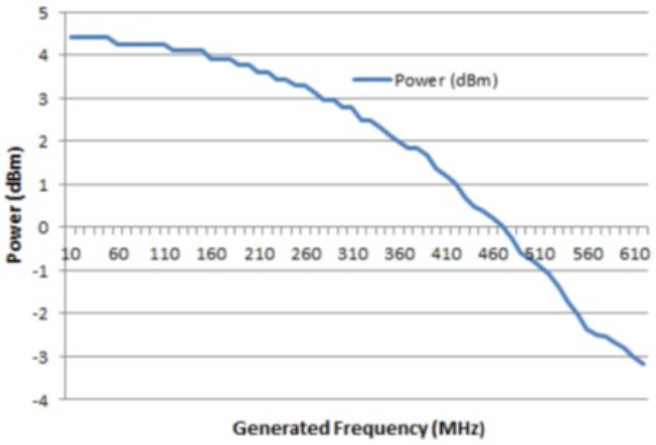


Figure 4-7: Frequency Response over first Nyquist Zone

Measurement

Similar to the SFDR measurement, the frequency response of our system has also been compared with the frequency response of Tektronix AWG. Figure 4-8 shows that our system performs better in the frequency range from 0-370 MHz The rate of fall in amplitude is not as high as seen in the Tektronix AWG.

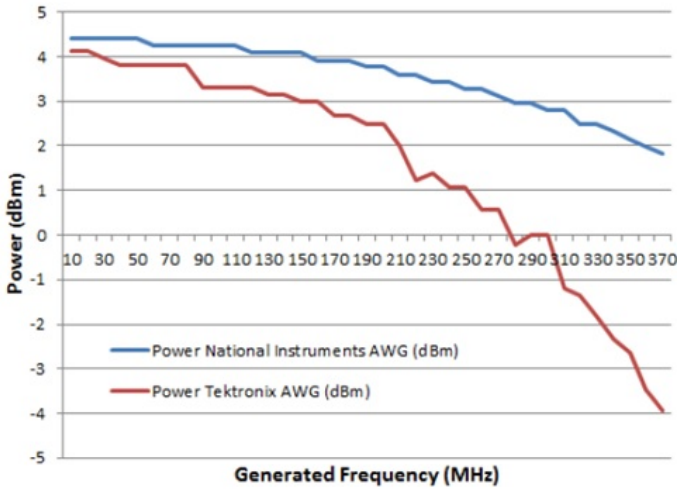


Figure 4-8: Frequency Response of NI AWG compared with Tektronix AWG

Methods of compensation

The frequency response data could be used effectively to either pre-distort the signal while generation so as to cancel the effect of sinc response. It could also be used to design a DAC reconstruction filter at the output that can act as an equalizer and result in a flat frequency response.

4-2-5 Phase Noise

As mentioned earlier, the random and rapid fluctuation in the time offset manifests as the phase noise of the system. The IEEE definition of phase noise is given as

$$L(f) = S(f)/2 \tag{4-1}$$

where S(f) is the single sided spectral density of phase fluctuations. The transmitter has multiple channels and each of the channel is transmitted by an antenna which could be a sub array of elements. In such a situation, the phase noise of the system can cause additional sidelobes in the antenna pattern which is not desirable.

Measurement

The AWG system uses a 10MHz on board crystal is as the reference. Various frequencies have been generated and the phase noise of the system has been measured. The measurement has been done for four frequencies, 150 MHz, 200 MHz, 300 MHz and 400 MHz The phase noise has been measured at an offset of 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. The phase noise plot for 300MHz is shown in Figure 4-9.

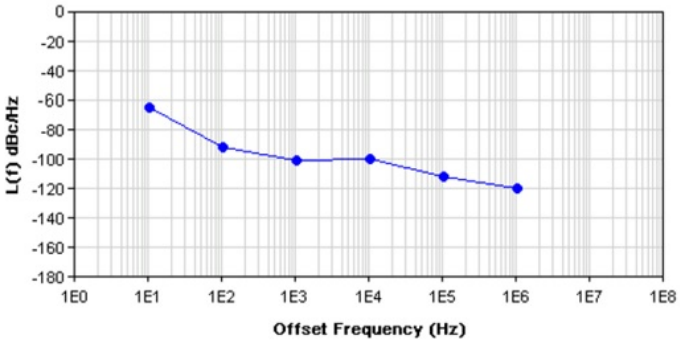


Figure 4-9: Phase Noise of 300MHz

The corresponding jitter values could be translated to the equivalent side lobe level in order to find the impact on the whole system. The following equation gives the relation between the phase noise and random jitter

$$SideLobe(f)(dB) = 20log10(2\pi jitter f) \tag{4-2}$$

where f is the frequency at which phase noise is measured. Table 4-3 gives the value of rms jitter and corresponding side lobe level for various frequencies.

The side lobe level increases with the generated frequency. The worst case side lobe level is calculated as -46 dB. If the performance needs to be improved, a better reference could be provided externally to generate the base clock for the AWG.

Frequency (MHz)	RMS Jitter(ps)	Sidelobe(dB)
150	2.50	-53
200	2.07	-52
300	1.88	-49
400	2.05	-46

Table 4-3: RMS Jitter and side lobe level at different frequencies

4-3 Conclusion

This chapter discussed the various offsets and errors present in the system. The following sections described the techniques used to measure them and the measure values. The impact of the errors or offsets have also been discussed. The measured values have been analysed and recommendation to reduce the effect of the errors have been suggested.

Chapter 5

Software Architecture and AWG Design

5-1 Introduction

The hardware characterization has been discussed in the previous chapter. The next step is to design and implement the arbitrary waveform generator. As per the AWG specifications, waveforms with a bandwidth of 200 MHz and having duration of 1 ms or more should be implemented and generated. This chapter introduces the various design strategies developed to implement the AWG. The methods of testing and the obtained results are also discussed.

5-2 Software Architecture

The top level architecture of the AWG programming is as shown in Figure 5-1. The waveforms designed using Matlab or LabVIEW could be transferred from the host computer. The maximum clock that could be derived in the FlexRIO module is 350 MHz. But the sampling rate of the DAC in the adapter module is 1.25 GHz. In order to match this rate discrepancy, a loop, that runs at 156.25 MHz, writes eight consecutive samples of the waveform simultaneously to the adapter module interface. This loop receives data from the DRAM. But each DRAM bank read/write operation can run at a maximum rate of 100 MHz. This rate discrepency needs to be matched to get a sustained throughput at the DAC. Each DRAM location is 128 bits long. In order to use the DRAM efficiently and to achieve maximum throughput, the data type of the waveform should match the Access size of DRAM. Access size corresponds exactly to the number of bits that are written/read in a given memory write/ memory read operation. The family of hardware that is used to implement the AWG has an access size of 128 bits. Thus a single location can contain a maximum of 9 samples (14*9= 126 bits). This would give a maximum throughput of 900 MSamples/second. But the DAC interface requires data at a higher rate i.e. 1.25 GHz. In order to match the data rates inside the AWG the following design strategies were considered.

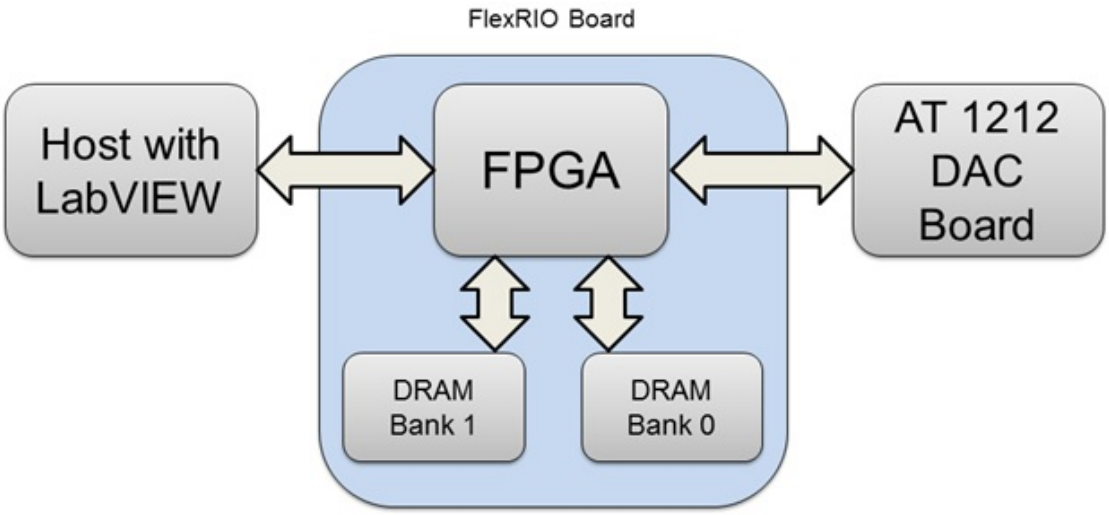


Figure 5-1: Data flow inside the AWG

5-2-1 Single channel Implementation

A FlexRIO board comes with two DRAM banks. The maximum rate at which each of the DRAM banks could be accessed is 100 MHz. If the waveform samples are split to even and odd samples and written into the respective banks, the data could be retrieved at a higher rate i.e. two times faster, which could match the final required data rate. However, this would limit the number of channels in the AWG to four.

5-2-2 Interpolation

Another possibility is to introduce an interpolation function in order to match the two data rates. The data is read from the DRAM at a rate of 100 MHz. Considering eight samples being written to a single DRAM location, the throughput is 800Msamples/sec. This needs to be matched with the rate of 156.25 MHz * 8 samples (1.25 GSamples/sec). A suitable interpolator could be designed inside the FPGA that can solve support continuous output.

5-2-3 Generating the waveform inside the FPGA

Modeling and implementing an algorithm to generate the waveform inside the FPGA could be another option. In this way, the DRAM could be bypassed and signal could be directly generated. This is possible only for a limited set of simple waveforms. When it comes to the generation of sophisticated waveforms, due to the limitations in the supported library functions this option is not feasible.

5-2-4 Representing the data using reduced number of bits

By representing the data using reduced number of bits, the effective throughput of the DRAM read process could be increased. This could match the rate at which samples should be written

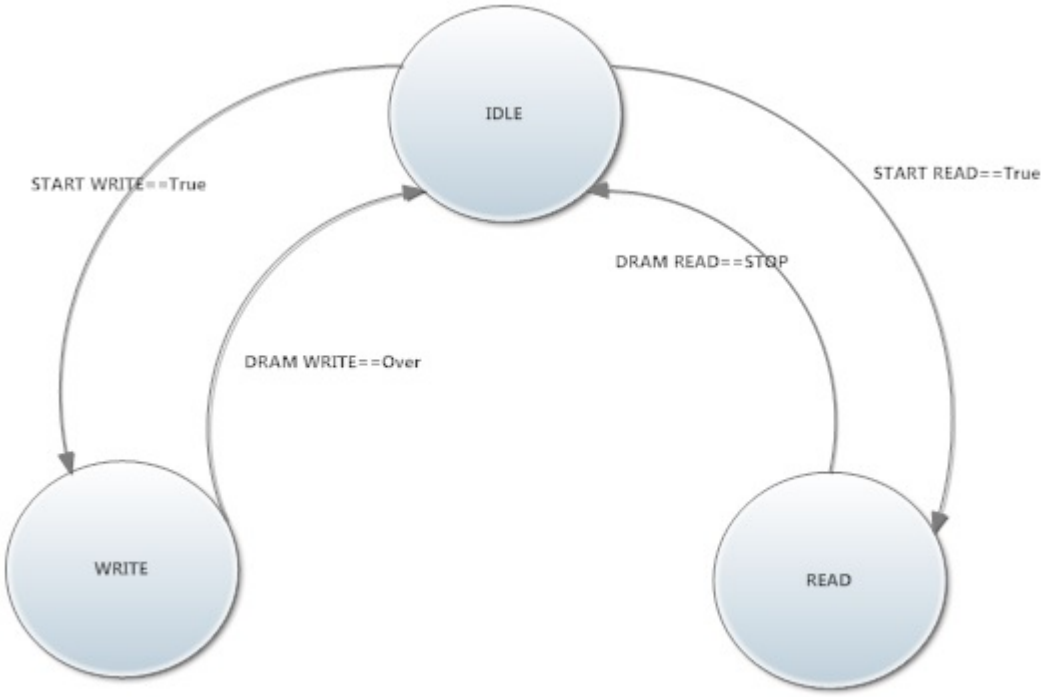


Figure 5-2: Events inside the FPGA

at the DAC interface. Ideally, each sample should be 14 bits. Representing the data using lesser number of bits could increase quantization error and affect the SNR.

5-3 AWG Design

As discussed in the previous section, a number of strategies were considered while designing and implementing the AWG. The following section gives more details on various strategies designed, tested and implemented to realize the AWG. Three designs (Section 5.2.1, 5.2.2 and 5.2.4) were developed and tested. All these designs are event driven based. There are mainly three states in which the FPGA may run as per the occurrences of events,

1. Idle
2. Write
3. Read

When Idle, the FPGA waits for the read or write command issued from the host. Once either the Write or Read command is received, the FPGA moves to the respective processes of writing to the DRAM or reading from the DRAM. Figure 55-2 shows the different events occurring inside the FPGA.

The AWG works on three major steps

5-3-1 Waveform generation and download

The waveforms could be designed and generated in Matlab or LabVIEW and saved as files. These files are read from the host system installed with LAbVIEW. By default, the waveform samples are represented as double values. This is converted to a fixed point data format compatible for DAC representation. These waveform samples are transferred to the FPGAs in the FlexRIO boards via two Direct Memory Access (DMA) FIFOs.

5-3-2 Waveform packing and storing

As mentioned in the previous section, in order to use the DRAM efficiently and to achieve maximum throughput, the data type of the waveform should match the Access size of DRAM. With a waveform sample represented in N bits, it is possible to accommodate 128/N samples in one DRAM location. Hence the first step is to pack the 128/N samples to a single variable. The packed data is written into another FIFO inside the FPGA. This process runs at a rate of 100 MHz. Finally, this data is written to the respective DRAM banks.

5-3-3 Waveform playback

Once the FPGAs receive the signal to read and playback data from the DRAMs, the waveforms samples are read into another FIFO that delivers the data to the DAC interface. In order to achieve a sustained throughput, following designs have been developed.

5-4 Design 1 - Single Channel Design

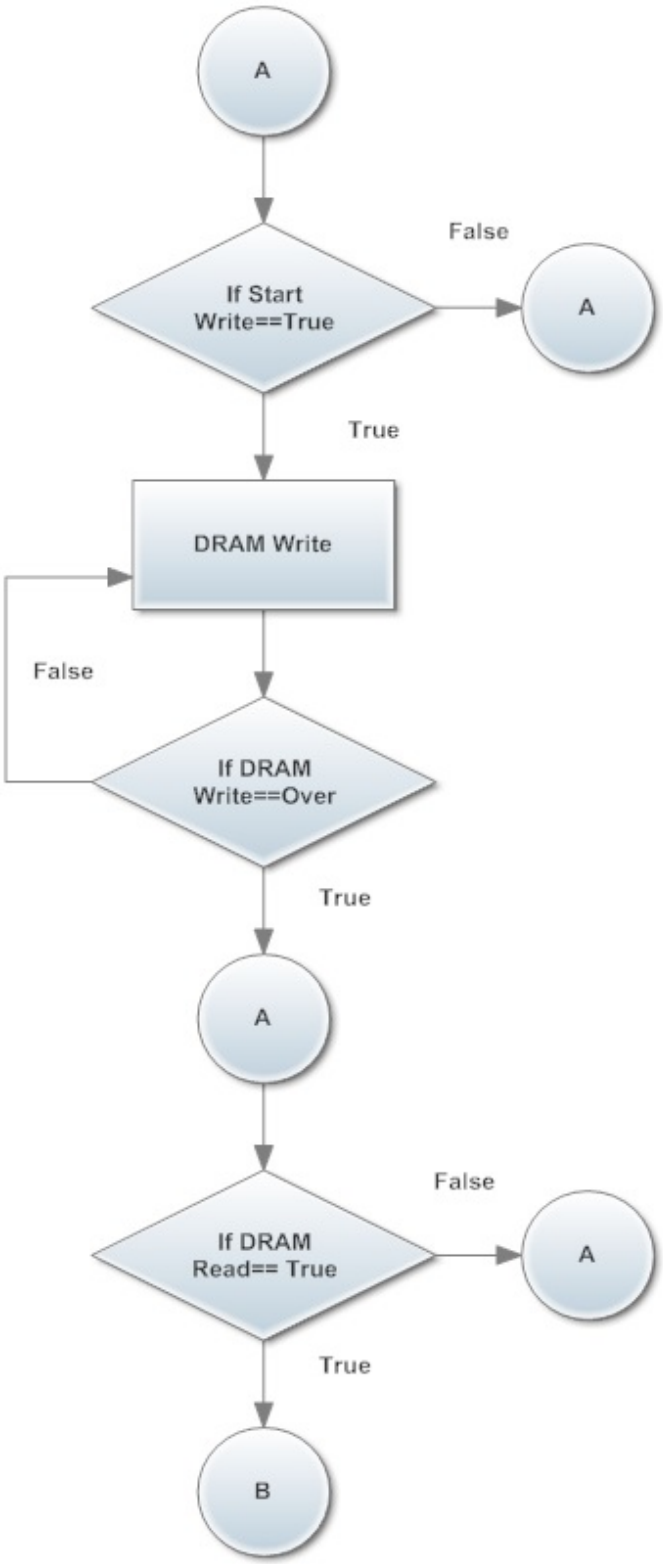
The following flow chart gives the logic used to implement the AWG. As mentioned earlier, the two banks of DRAM in a FlexRIO board were used to store the waveform for a single channel. The waveform is de-interleaved and written to the two DRAM Banks of a FlexRIO board. During playback, the data is interleaved and written to the DAC interface. Figure 5-3 shows the flow chart for this implementation. The flowchart represents the logic implemented in a single FPGA. The same logic is loaded to all the four FlexRIO FPGAs to realize a four channel system.

5-4-1 Testing

The various steps involved in the implementation of AWG including - data packing, data writing to the DRAM and data read from the DRAM needs to be tested. Several strategies were adopted to test validity of the code, for example by providing variables at intermediate stages and reading out their status to the computer, reading random location of the DRAM and compare the data value with the expected value etc. Finally, the data read from the DRAM was fedback to the host. The data is read, interleaved, unpacked and streamed to the Host system. The data stream is plotted in the host and checked for any spikes or glitches. The spectrum of the streamed data is compared with the spectrum of the generated data. Figure 5-4 shows the time and frequency domain representation of the generated waveform and the streamed data. The generated waveform has the following specifications:


Start
Generate signal (14 bit)
De-interleave and write to 2 FIFOs
Transfer data to FPGA
Pack 8 samples and write to another FIFO
DRAM Idle
A

(contd.)


A
If Start
Write==True
False
A
True
DRAM Write
False
If DRAM
Write==Over
True
A
If DRAM
Read== True
False
A
True
B

(contd.)

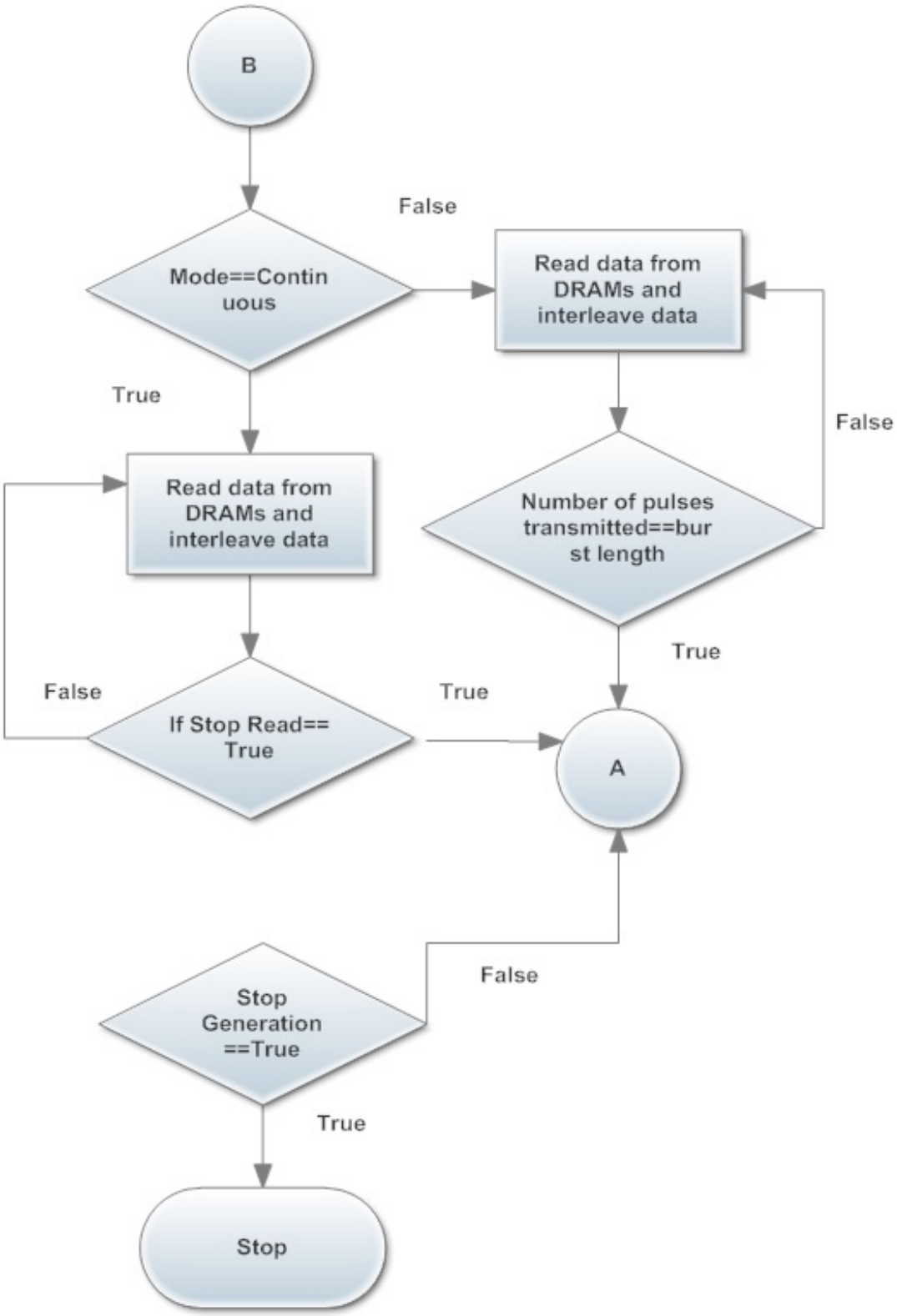


Figure 5-3: Flow Chart for Single Channel Implementation

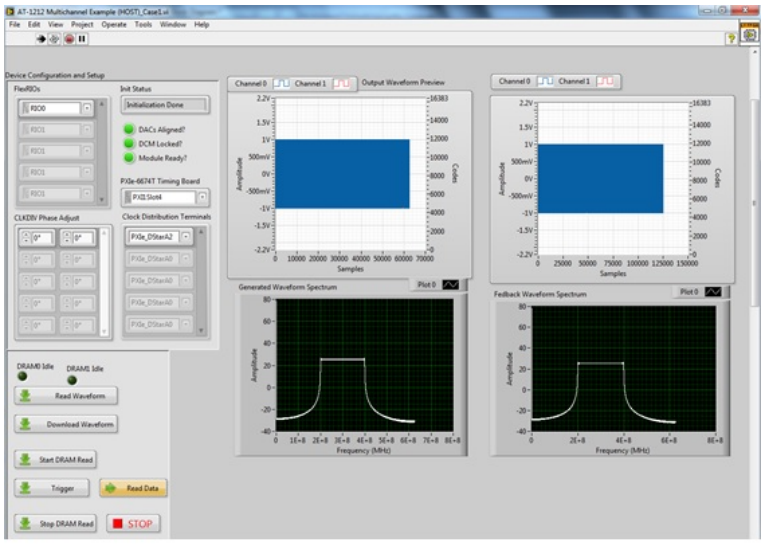


Figure 5-4: Data from the DRAM streamed to the host

- Signal Bandwidth: 200MHz
- IF: 300MHz
- Duration: 100 μs
- Amplitude: $1V_{pp}$ (single ended)

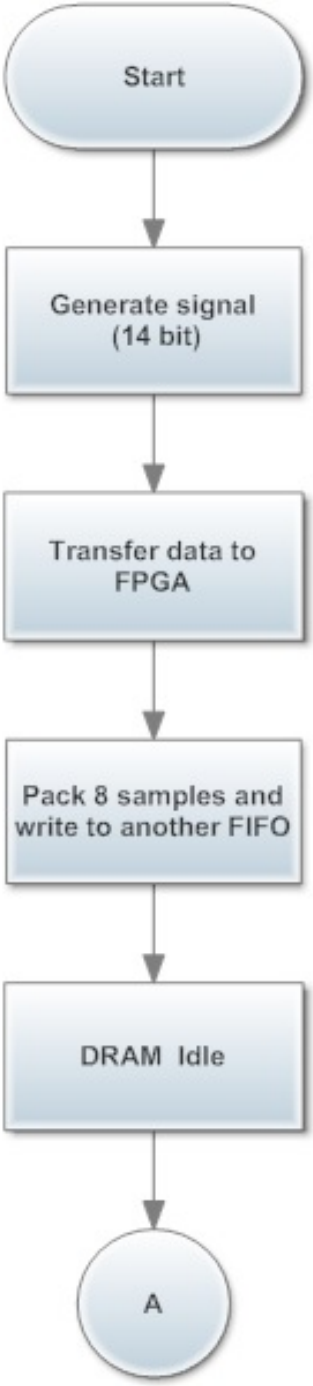
The number of samples in the time domain transmitted waveform is half the number of total samples due to the de-interleaving used to split the waveform into two streams.

5-5 Design 2 - Interpolation

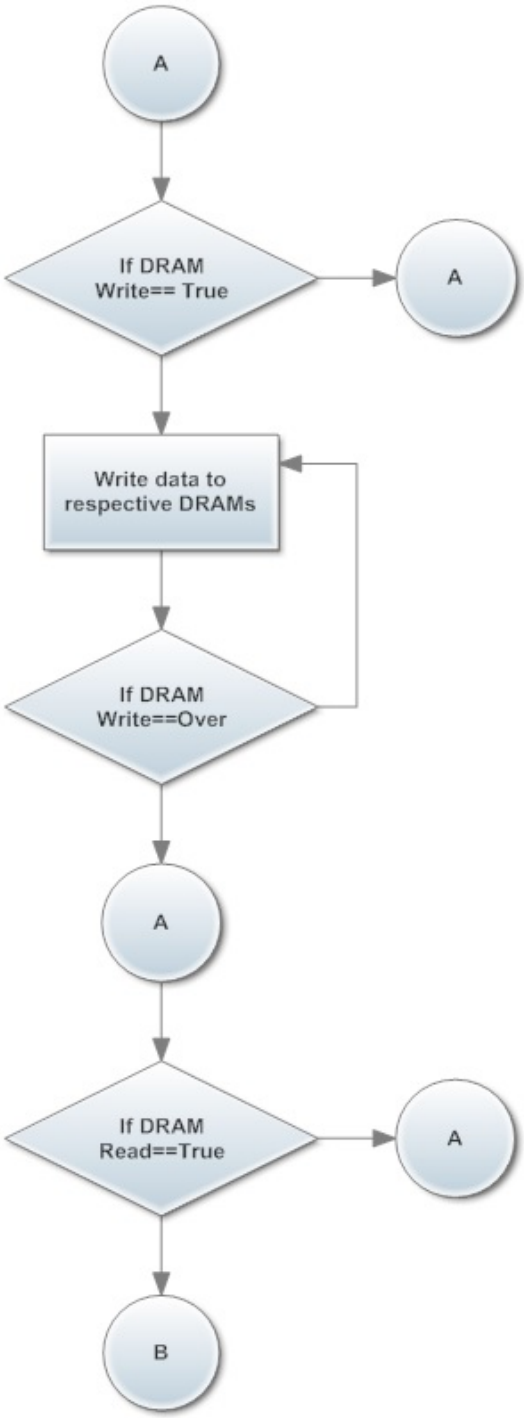
The second design strategy was to implement an interpolation module that could match the different data rates. The data coming from the Host is packed in groups of 8 samples and written to FIFOs. Upon receiving the write command from the host, the data is written to the respective DRAM banks. The DRAM state machine now goes to idle mode. Once, the read command is identified, the data from the DRAM is read to another pair of FIFOs. This data act as the input to the interpolation block. A 1:2 linear interpolator has been implemented. The interpolator module is a simple linear interpolator. For every 8 input samples, the interpolator produced 16 samples. The flowchart for this design is showed in Figure 5-5.

5-5-1 Testing

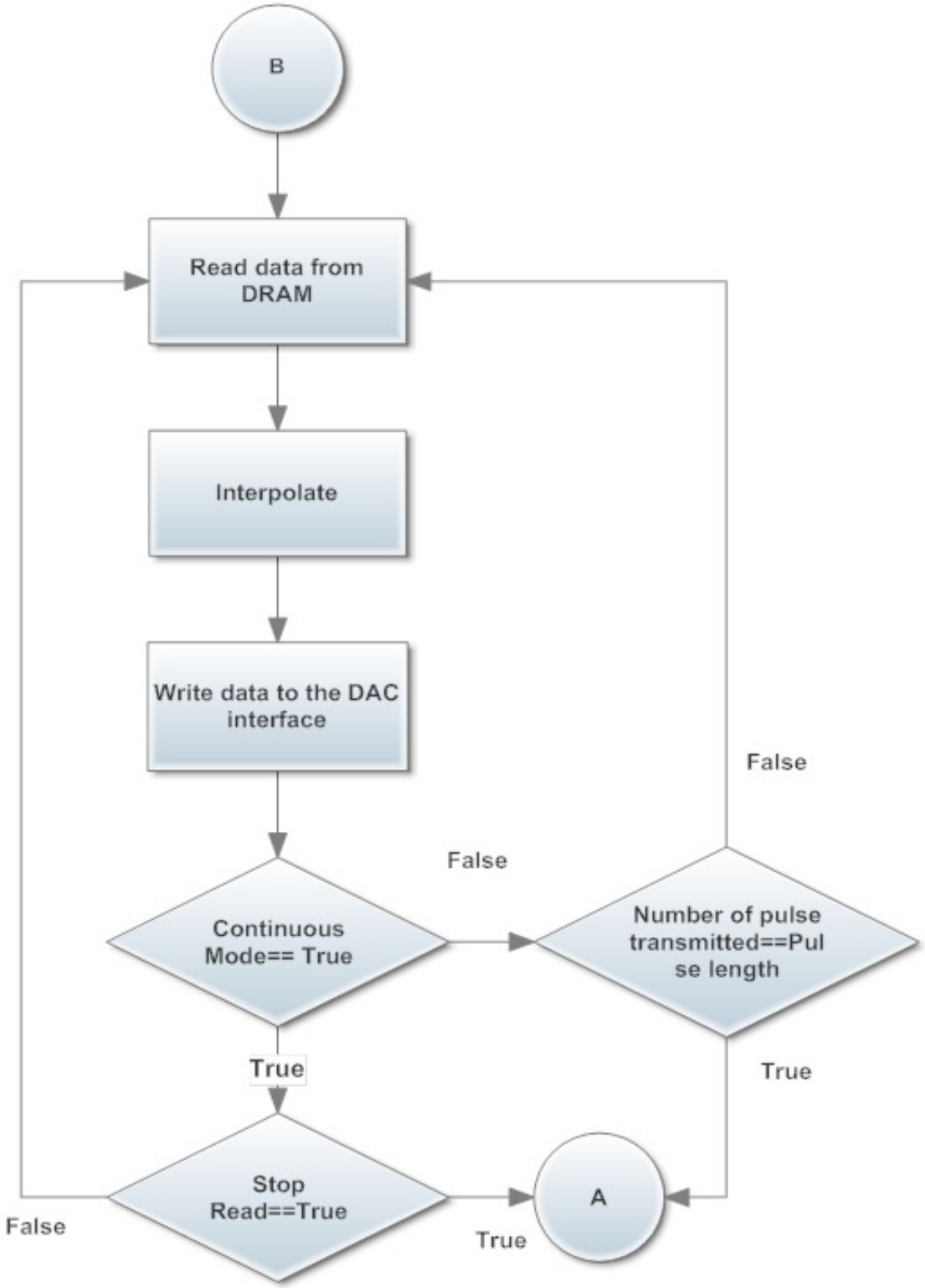
Similar to the single channel design, the data packing, data writing to the DRAM, data read from the DRAM and interpolation has been tested. In this case, the data streaming is performed from two points.


Start
Generate signal (14 bit)
Transfer data to FPGA
Pack 8 samples and write to another FIFO
DRAM Idle
A

(contd.)


A
If DRAM
Write== True
A
Write data to
respective DRAMs
If DRAM
Write==Over
A
If DRAM
Read==True
A
B

(contd.)


B
Read data from DRAM
Interpolate
Write data to the DAC interface
Continuous Mode== True
False
Number of pulse transmitted==Pul se length
False
True
True
Stop Read==True
False
True
A

(contd.)

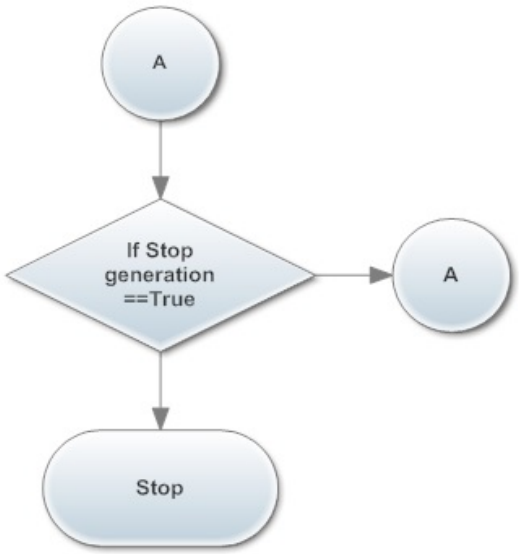


Figure 5-5: Flow Chart for Dual Channel Implementation with Interpolation

- The data from the DRAM is read, unpacked data and streamed to the Host. This would ensure the validity of DRAM write/read process.
- The data after interpolation is unpacked, and streamed to the Host. This would validate the interpolation function.

Following figures show the time and frequency domain comparison of the generated waveform and the streamed data. In Figure 5-6, the waveform and spectrum on the left represents the waveform generated at the Host and the waveform and spectrum on the right represents the feedback waveform. The generated signal after encoding to the DAC format, takes values between 0 and 16,383. Since waveforms were generated at the DAC half full scale level, the sample magnitude varies between 5,000 and 12,000. Figure 5-6 shows the transmitted and streamed data in time and frequency domain. The waveform specifications are as given below:

- Signal Bandwidth: 200MHz
- IF: 200MHz
- Duration: 100 μs
- Amplitude: $1V_{pp}$ (single ended)

Figure 5-7 represents situation when the interpolated data is feedback to the host. It is evident from that the spectrum of the feedback data, that the interpolation causes images and also puts a limit to the maximum frequency that could be generated. Also the number of samples in the generated waveform is 62,500 samples, whereas the feedback data has 125,000 samples (twice the generated samples), because the interpolation factor is 2.

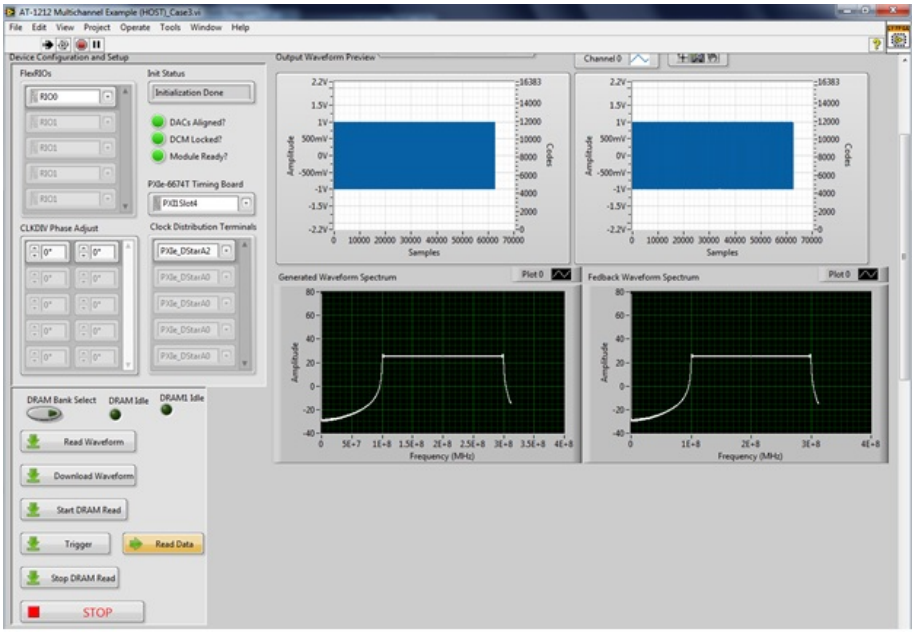


Figure 5-6: Data from the DRAM streamed to the host

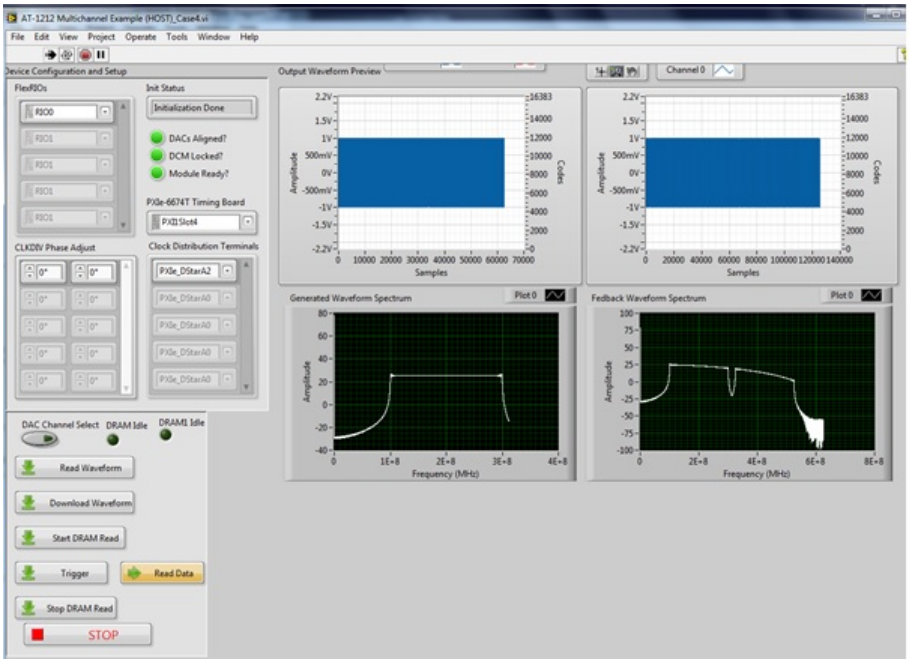


Figure 5-7: Data from the FPGA, after interpolation, streamed to the host

5-6 Design 3 - Waveform generation using lower number of bits

As mentioned in section 5.2.4, this design generates the waveform using lesser number of bits. This would let a single DRAM location contain higher number of samples thereby increasing the throughput of DRAM read operation. Reducing the number of bits would affect the SNR and quantization error. In order to improve the SNR, the waveform samples are scaled to 14 bits before writing to the DAC interface. The flowchart for this design has been illustrated in Figure 5-8.

5-6-1 Testing

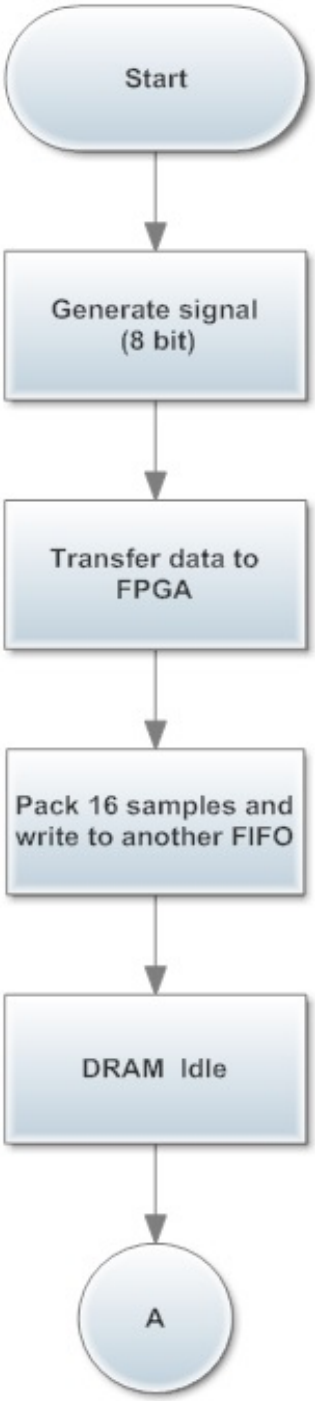
The testing procedures are similar to that of the previous design using interpolation. The data read from the DRAM and the data after scaling to 14 bits are separately tested by streaming the data samples to the host computer. Following figures show generated waveform and the streamed data in time and frequency domain. Since the data is now represented in a lower number of bits, the encoded waveform takes values from 0 to 255. This could be inferred from the right hand side axis, named Codes, of the time domain signal. In frequency domain, this corresponds to around -20 dB, as measured from the spectrum. Figure 5-9 represents the generated data and the DRAM data feedback to the host. The amplitude of the time domain and frequency domain signals for the generated and feedback waveforms remain the same. Figure 5-10 shows the transmitted and scaled data streamed to the host in time and frequency domain. The waveform specifications are as given below:

- Signal Bandwidth: 200MHz
- IF: 300MHz
- Duration: 100 μs
- Amplitude: $1V_{pp}$ (single ended)

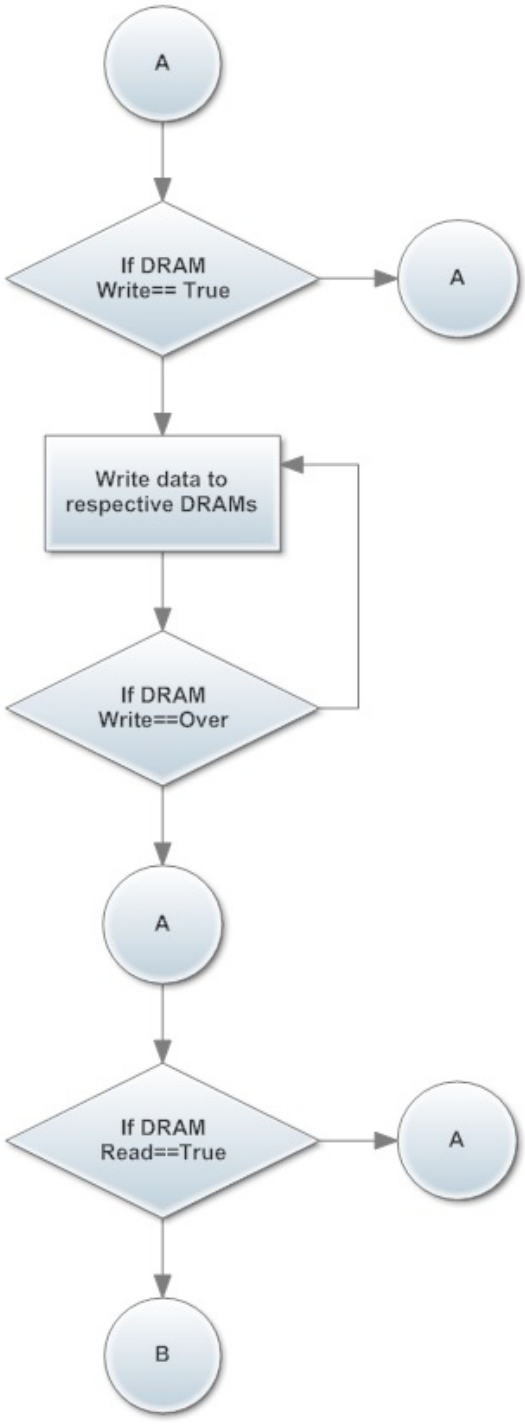
5-7 AWG Output Testing

The preliminary tests were done using the methodologies described in section 5.4.1, section 5.5.1 and section 5.6.1. This ensured the correctness of the implemented logic. However, when the data has been written to the DAC interface inside the FPGA and the AT 1212 DAC board output has been tested, it was observed that

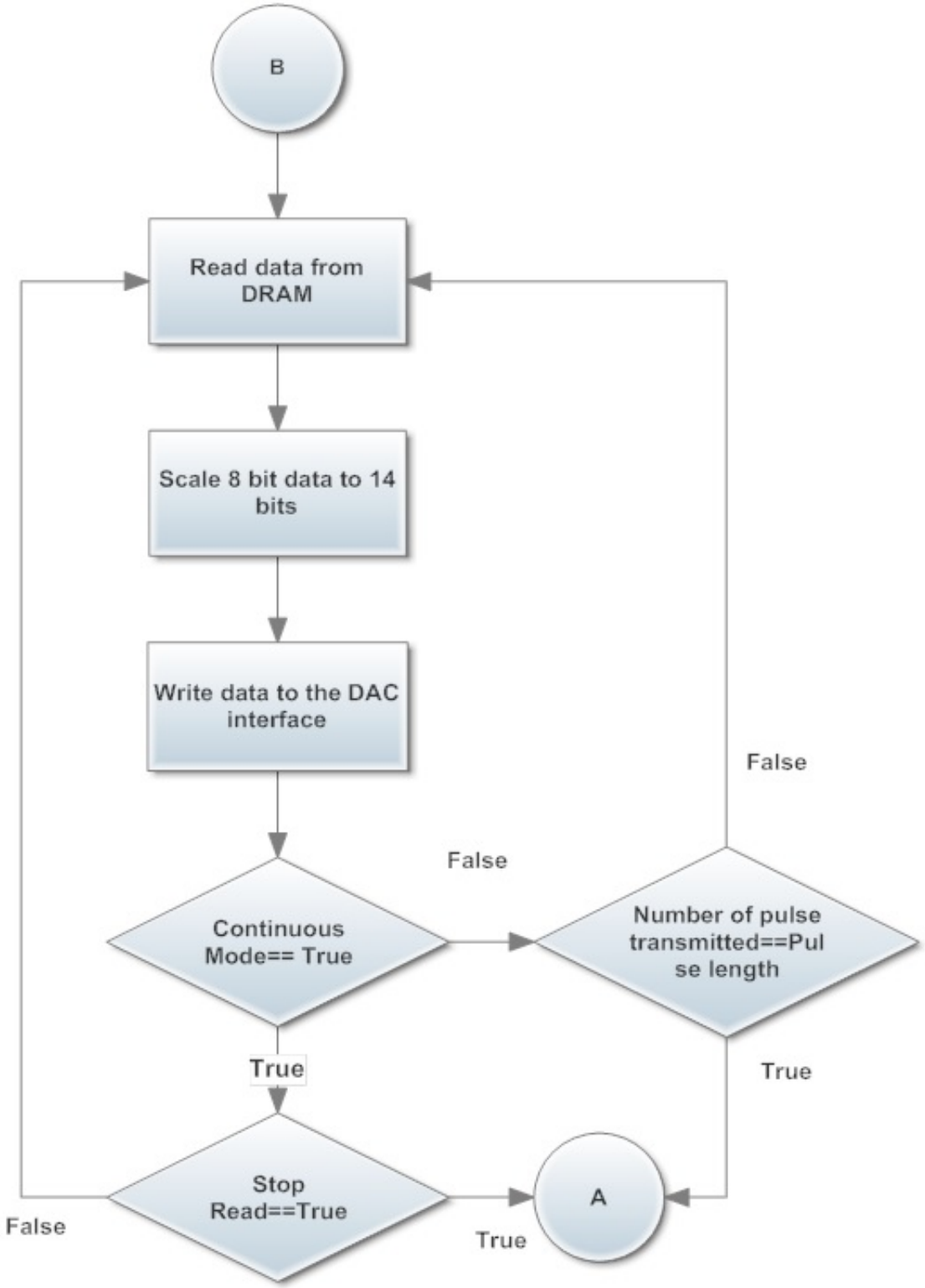
- The analog output waveform had glitches
- The analog outputs from various modules lacked synchronization.
- The same bit file when loaded to the four FlexRIO boards gave inconsistent outputs.


Start
Generate signal (8 bit)
Transfer data to FPGA
Pack 16 samples and write to another FIFO
DRAM Idle
A

(contd.)


A
If DRAM
Write== True
A
Write data to
respective DRAMs
If DRAM
Write==Over
A
If DRAM
Read==True
A
B

(contd.)


B
Read data from DRAM
Scale 8 bit data to 14 bits
Write data to the DAC interface
Continuous Mode== True
False
Number of pulse transmitted==Pul se length
False
True
True
Stop Read==True
False
True
A

(contd.)

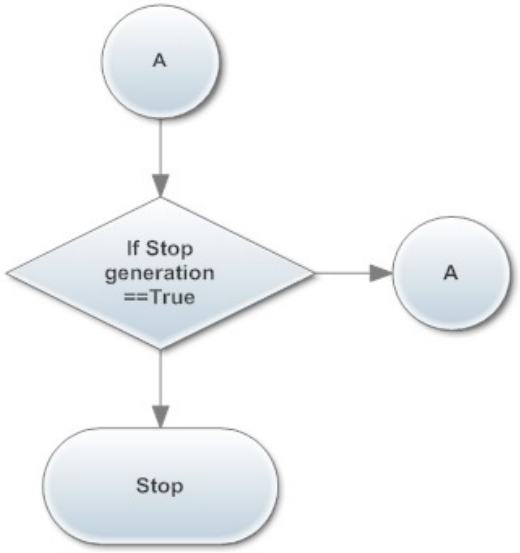


Figure 5-8: Flow Chart for Dual Channel Implementation (8 bit design)

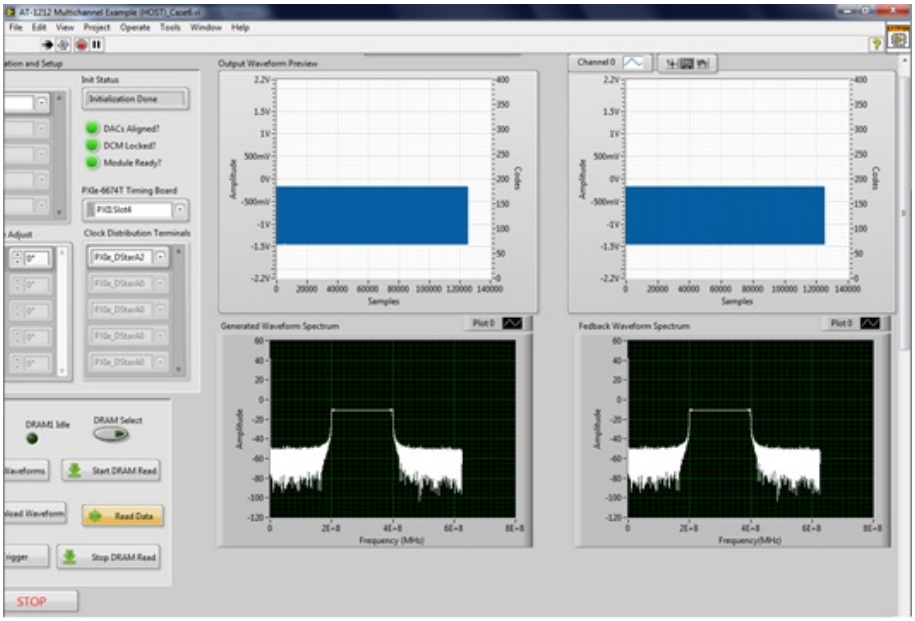


Figure 5-9: Data read from the DRAM streamed to the host

Figure 5-10: Data from the FPGA, after scaling, streamed to the host

Even though the data when streamed to the host proved the implemented logic, the DAC output suffered from the aforementioned problems. It is to be mentioned that the data, when streaming back to host, is accessed at a lower rate. This rate is lower than 156.25 MHz, the rate at which the DAC interface and eventually the DAC reads data from the FPGA. As a result, it could be deducted that the possible reasons for the observation mentioned above could be

- Lack of sustained throughput to the DAC interface at 156.25 MHz
- Insufficient handshaking (communication among different data nodes) between the DRAM and FIFOs resulting in missing samples.

In order to make the design robust, the FPGA code has been optimized by using some additional labview library functions. This has been done to ensure that the throughput is met and handshaking has been taken care of. Even this could not completely solve the problems. Finally, the clock source used by the loop that transfers the data to the DAC interface was re-assigned. Initially, this loop was assigned to run on the DStarA (156.25 MHz) clock. Replacing this clock by the IO Module clock 0 solved the issues there by giving perfect output at the DACs. The IO Module clock 0 is the clock reaching the FlexRIO FPGA board from the DAC module. The socketed clip (please refer to section 3.3.6) following the DAC data interface also uses the IO Module clock 0.

5-8 Results

The following section illustrates the results of the three designs described in section 5.4, section 5.5 and section 5.6.

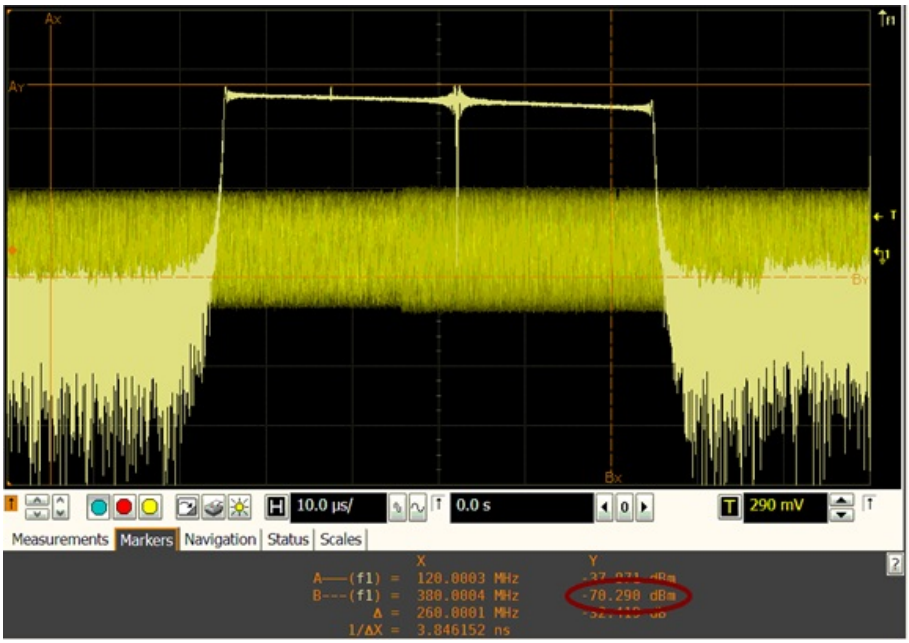


Figure 5-11: Spectrum of Chirp Signal generated using Design 1 implementation of AWG

5-8-1 Design 1

The AWG in the single channel configuration has been programmed to generate a chirp signal. The specifications of the generated waveform are:

- Signal Bandwidth: 200MHz
- IF: 300MHz
- Duration: 100 μs
- Amplitude: $1V_{pp}$ (single ended)

Figure 5-11 shows the spectrum of the generated signal. From the oscilloscope reading, the noise floor level at the DAC output can be measured.

For the Design 1 (single channel configuration of AWG), the noise floor level is -70.290 dBm

5-8-2 Design 2

Since the design 2 implementation of AWG makes use of interpolation, maximum frequency that could be generated by this this design is 312.5 MHz. Hence, the test signal has been shifted to a lower IF. The AWG is programmed to generate the chirp signal with the following specifications:

- Signal Bandwidth: 200MHz
- IF: 200MHz

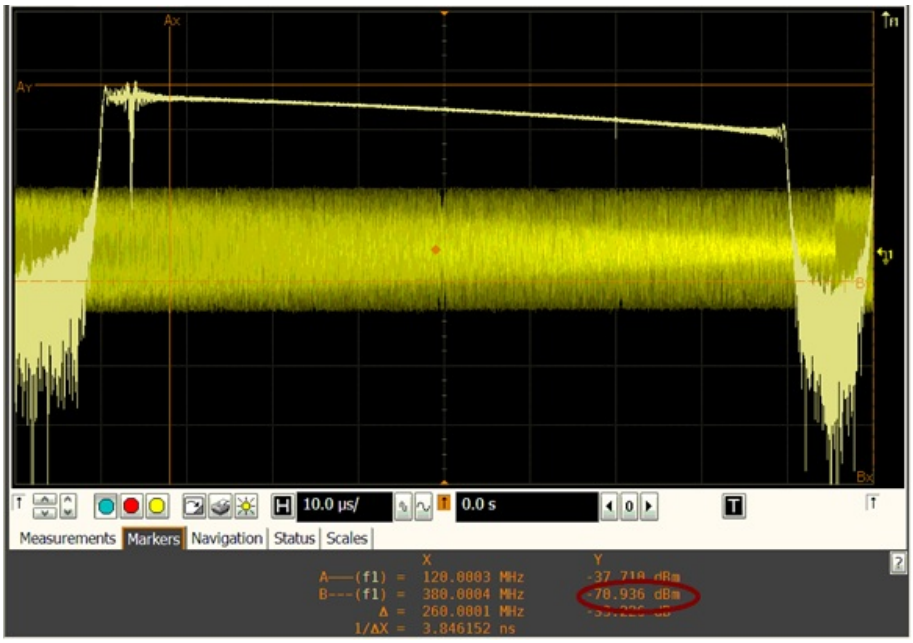


Figure 5-12: Spectrum of Chirp Signal generated using Design 2 implementation of AWG

- Duration: 100 μs
- Amplitude: $1V_{pp}$ (single ended)

Figure 5-12 shows the spectrum of the generated signal. From the oscilloscope reading, the noise floor level at the DAC output can be measured.For the Design 2 (interpolation based implementation of AWG), the noise floor level is -70.936 dBm Interpolation creates images and Figure 5-13 shows the presence of an image signal adjacent to the signal of interest.

5-8-3 Design 3

Finally, the AWG implementation based on Design 3 as described in section 5.6 is tested. The chirp waveform used to test the design had the following specifications.

- Signal Bandwidth: 200MHz
- IF: 300MHz
- Duration: 100 μs
- Amplitude: $1V_{pp}$ (single ended)

Figure 5-14 represents the output of AWG implemented using Design 3. From the oscilloscope reading, the measured noise floor level at the DAC output is -69.968 dBm. Design 3 generates an output that is very much close to the rest of the designs.

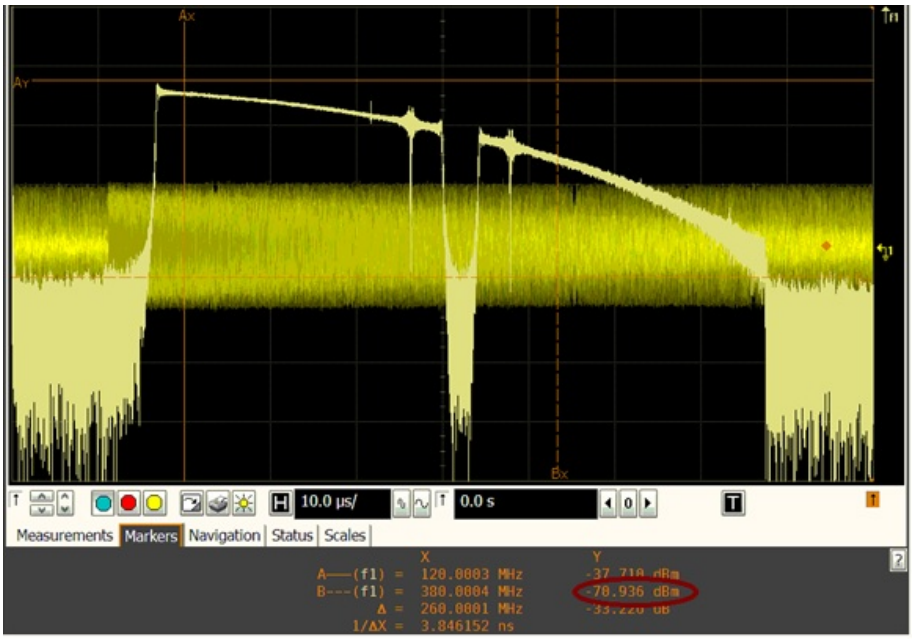


Figure 5-13: Spectrum of Chirp Signal generated using Design 2 implementation of AWG with image signal

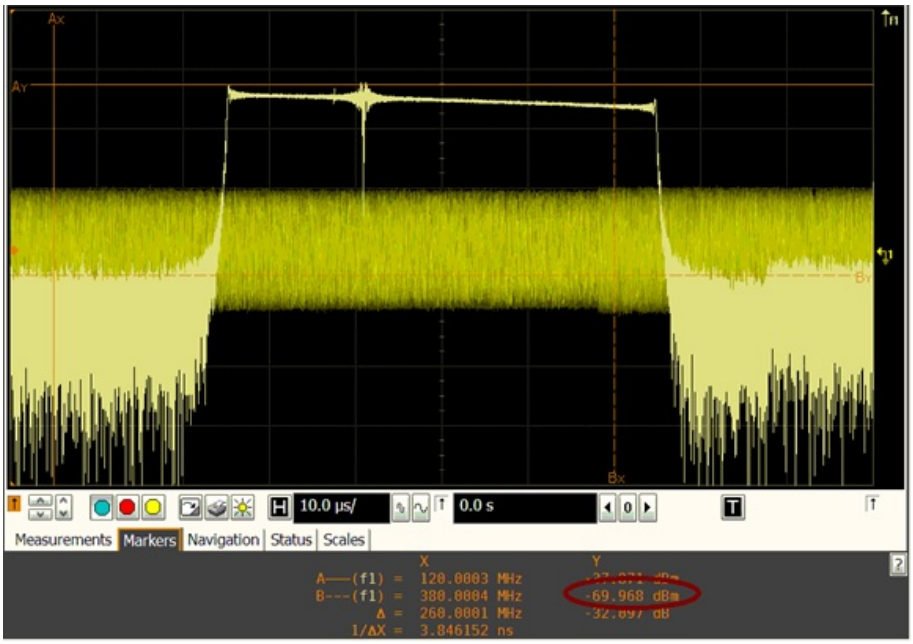


Figure 5-14: Spectrum of Chirp Signal generated using Design 3 implementation of AWG

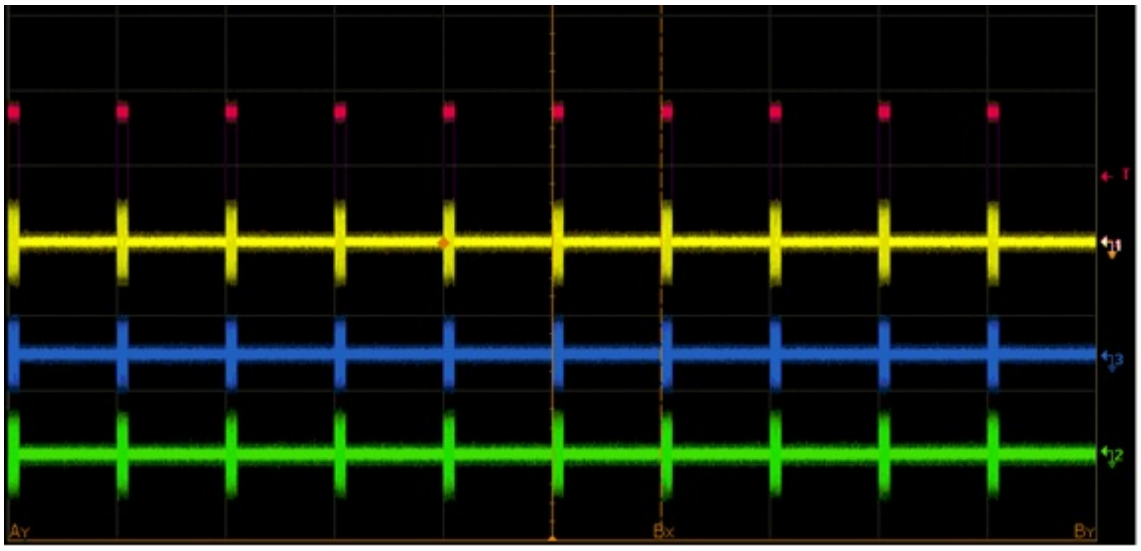


Figure 5-15: Continuous mode output of AWG

5-9 Modes of operation

The AWG has been programmed to operate in two modes as described below

5-9-1 Continuous Mode

In continuous mode, the AWG transmits the waveform continuously until a STOP command is issued from the host computer. Once a Stop command is issued, the AWG goes to idle mode. Figure 5-15 shows the operation of the AWG in a continuous mode. The figure shows the output of three channels on the oscilloscope.

5-9-2 Burst Mode

The Burst mode could be useful in radar doppler processing which requires longer integration time. In burst mode, the AWG transmits a fixed number of pulses and goes to idle mode. The AWG Burst mode has been designed in two versions.

- Design A: Up on receiving the trigger signal to transmit, the AWG once reads the waveform loaded in the DRAM and transmits it. In this design, the AWG generates sequentially the address of the DRAM location to be read. Once the address corresponds to the final location of the DRAM, the DRAM memory access loop terminates. Figure 5-16 shows the output of the AWG working in the burst mode. The waveform consisting of three pulses has been written to the DRAM. Once the trigger is generated, the burst mode transmits three pulses as shown in the following figure.
- Design B: The above design could be made more efficient and scalable when the burst consists of a large number of repetitive waveforms. Instead of writing the waveform N times inside the DRAM, the waveform could be written in the DRAM a single time

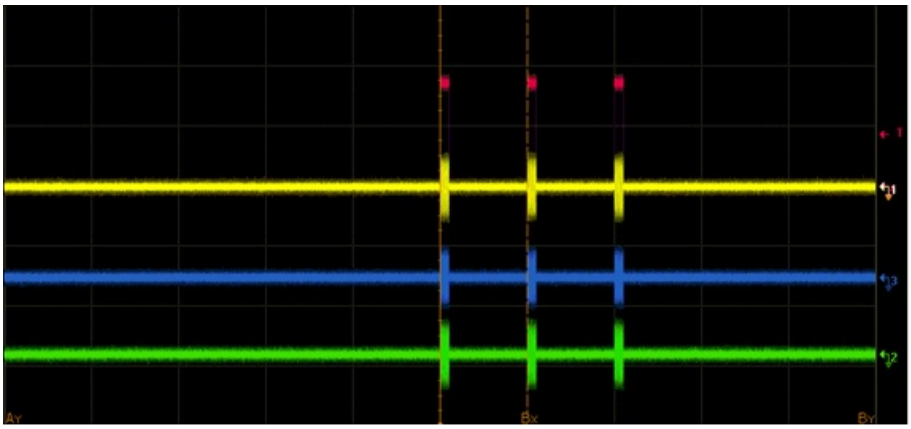


Figure 5-16: Burst mode output of AWG

and looped to transmit the N pulses. Both the designs have been tested and verified for their functionalities.

Thus, the AWG gives the possibility to operate in two different modes producing eight synchronous outputs. The AWG with its eight channels could be programmed to generate eight, different, synchronous signals thereby enabling space coding of the environment under surveillance. Similarly, the each channel of the AWG could be loaded with a set of waveforms that varies over time so that we can code the environment over time also. Thus, the combinations of the above possibilities would realize in an AWG for a space time coded MIMO radar test bed.

5-10 Marker Signal

Usually a pulsed radar system uses a single antenna for transmission and reception. This would require a marker signal to indicate the ON and OFF time of signal transmission to switch the antenna among transmitter and receiver. This marker signal could also be used to inform the exact start and end of a pulse. These exact timing details would be required for the coherent signal processing in the receiver. The AWG generates signals with a specific duty cycle. The DAC interface reads eight consecutive samples simultaneously. The marker signal has been implemented by comparing the value of these eight samples to the fixed point value equivalent of 0 V. The marker signal is turned off when all the samples are equivalent to 0 V. Every FPGA produces its own marker signal. This signal is routed through the DAC board to the SMA connector at the DAC adapter module. It has been observed that there is a fixed delay between the instance of time when the marker signal goes high and the instance of time when actual output becomes valid. The delay has been found to be fixed, 64.795 ns, hence could be taken care of either inside the program or externally by adjusting the phase. The marker signal is directly routed to the DAC board via the FlexRIO digital Input Output header. On the other hand, the waveform samples pass through the socketed clip, undergoes parallel to serialization, reach the DAC. The delay between the marker and the output waveform could be accounted to these intermediate steps. The output waveform of

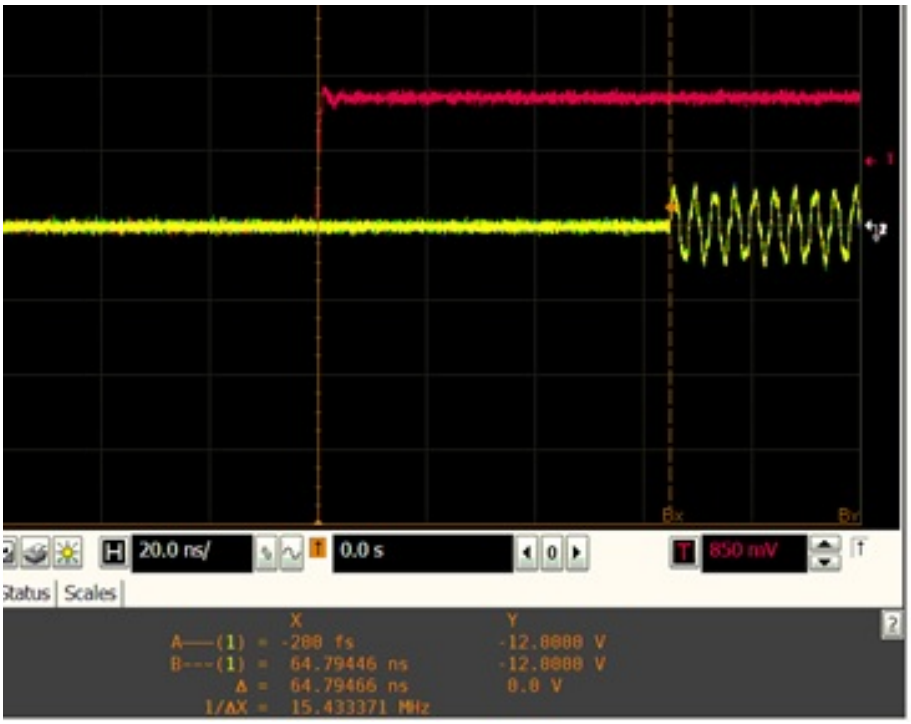


Figure 5-17: Marker signal with output signal of AWG

the AWG with the marker signal is as shown in Figure 5-17. The marker signal switches the value between 0V (OFF period) and 1.8 V (ON period)

It has also been verified that the marker signals from the four FPGAs are synchronous with each other. Figure 5-18 shows the four marker signals.

Figure 5-19 below shows the marker signal along with three synchronized output waveforms of the AWG system

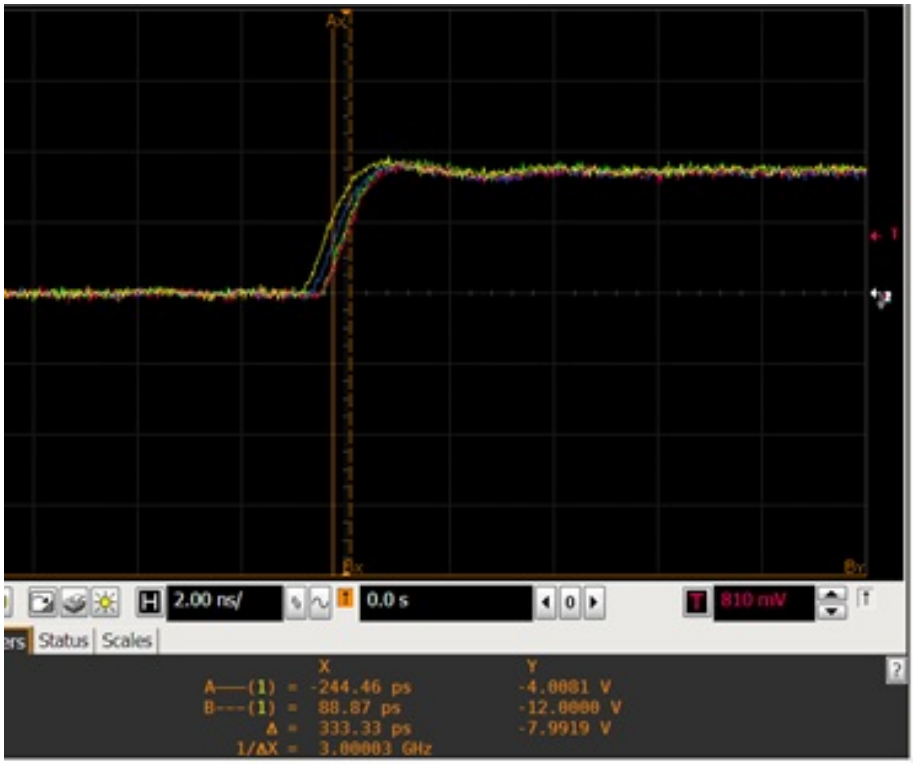


Figure 5-18: Synchronised Marker signals

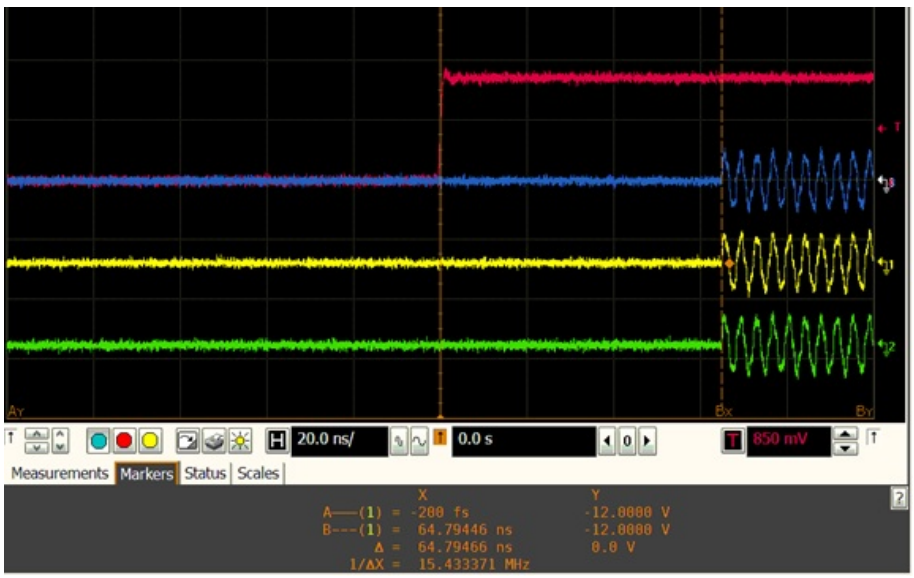


Figure 5-19: Marker signal with output signals of AWG

5-11 Comparison of three designs

The AWG has been implemented in three designs as described in section 5.4, section 5.5 and section 5.6. Each design has its advantages and disadvantages. This section compares the advantages and shortcomings of the three designs.

5-11-1 Design 1

- ✓ Design 1 implementing a single channel has the advantages of good resolution, SNR and better quantization error since the waveform is represented in 14 bits (equal to the number of bits in the DAC).
- ✓ The maximum frequency that could be generated is only limited by the DAC clock rate.
- × The disadvantage of this design is that it can only realize a four channel AWG. This design might not be the best choice when the number of channels required is greater than four.

5-11-2 Design 2

- ✓ Design 2 (that makes use of interpolation) also shares the advantage of good resolution, SNR and better quantization error.
- ✓ Unlike Design 1, Design 2 could be used to realize an eight channel AWG.
- × The maximum frequency that could be generated by the AWG is limited to 312.5 MHz instead of the original 625 MHz
- × Also, the radar being a phase sensitive system, adding new samples in between the generated samples may affect the performance of the system.

Design 2 relies on interpolation to meet the rate requirements for sustained throughput. With a DAC using a sampling frequency of 1.25 GHz, the maximum frequency that could be generated ideally is 625 MHz. With this design, that implements a 1:2 interpolator, the maximum frequency that could be generated is further reduced. The maximum frequency that could be generated by the AWG is limited to 312.5 MHz instead of the original 625 MHz. One of the requirement specifications of the AWG demands the system to generate a waveform with

- Signal Bandwidth: 200MHz
- IF: 300MHz

As a result, the design might not come handy when waveforms with the above specifications need to be generated.

Design	Number of Channels	Frequency generated	SNR
Design 1 (Single Channel)	✗	✓	✓
Design 2 (Interpolation)	✓	✗	✓
Design 3 (Waveform generation using 8 bits)	✓	✓	✓

Figure 5-20: Comparison of three designs used to implement the AWG

5-11-3 Design 3

- ✓ This design also realizes an eight channel AWG system.
- ✓ Since the waveform involves no interpolation, there is no limit to the maximum frequency that could be generated Hence the waveforms with the specification as given by Bandwidth of 200 MHz centered at an IF of 300 MHz could be easily generated.
- × Since the waveform is represented in 8 bits, the quantization error of this design would be a little more than that of Design 1 and Design2 and an increased noise floor level was expected.
- ✓ However, the measured noise floor levels (for same waveforms) when implemented using 14 bits and 8 bits have been observed to be very close.

The advantages and disadvantages are summarized and tabulated in the Figure 5-20. Figure 5-20 shows the criteria while choosing a design for an eight channel AWG that produces waveforms with 200 MHz Bandwidth centered at 300 MHz

Hence from Figure 5-20, Design 3 is the best choice among the three when it comes to the implementation of the AWG with the existing hardware configuration. Although the reduction in number of bits affects the quantization error and SNR of the system, the design still confirms to the requirement specification of

- Number of channels
- Intermediate frequency and signal bandwidth specification

The following section discusses the performance of the third design. The signals generated with this design have been compared with the output of a dedicated signal generator to validate the performance of this implementation.

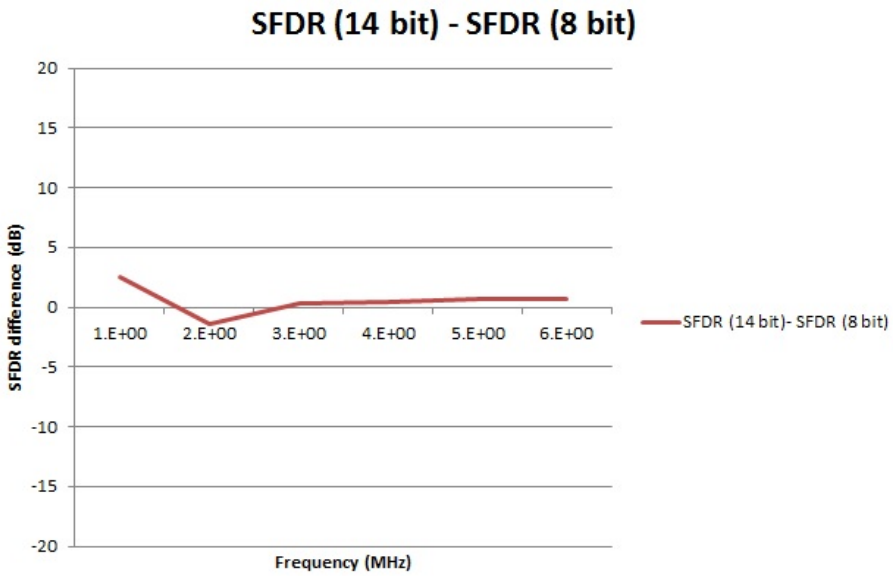


Figure 5-21: SFDR difference for 14 bit and 8 bit implementation

5-12 Performance Evaluation

As mentioned in the section 5.6, this design generates the waveform samples with reduced number of bits. The effect of reducing the number of bits results in quantization error and SNR of the signal. The SFDR and noise level of the system has been evaluated and compared with the 14 bit design and also with the Tektronix waveform generator.

5-12-1 SFDR of 8 bit and 14 bit designs

Several tone signals (100 MHz, 200 Mhz, 300 MHz, 400 MHz, 500MHz and 600 MHz) have been generated using this design. Similarly the same frequencies were generated in 14 bit format also. The waveform in 14 bit format was shorter (4096 samples) and hence stored in the internal memory of FPGA. The SFDR in the first Nyquist zone has been measured and tabulated for these tomes. Figure 5-21 compares the SFDR for 8 bit waveform and 14 bit waveform. Figure 5-21 shows the difference in SFDR between the 14 bit generated waveform and 8 bit generated waveforms. The DAC sampling rate is 1.25 GHz. Hence, it is to be noted that the frequencies generated bear non-integer relationship with the DAC clock. It is evident that the maximum variation is less than 2.5 dB. Also this maximum value occurs at 100 MHz, beyond which the trend shows a decrease in the difference. Since the AWG generates waveforms in the frequency range of 200 MHz -400 MHz, the operation in this region is almost comparable for 14 bit and 8 bit generation. The measurement details are available in Appendix C.

5-12-2 Noise floor level comparison with Tektronix waveform generator

Next, the performance has been compared with the Tektronix waveform generator. Several LFM waveforms spanning different bandwidths were generated and compared. The waveform

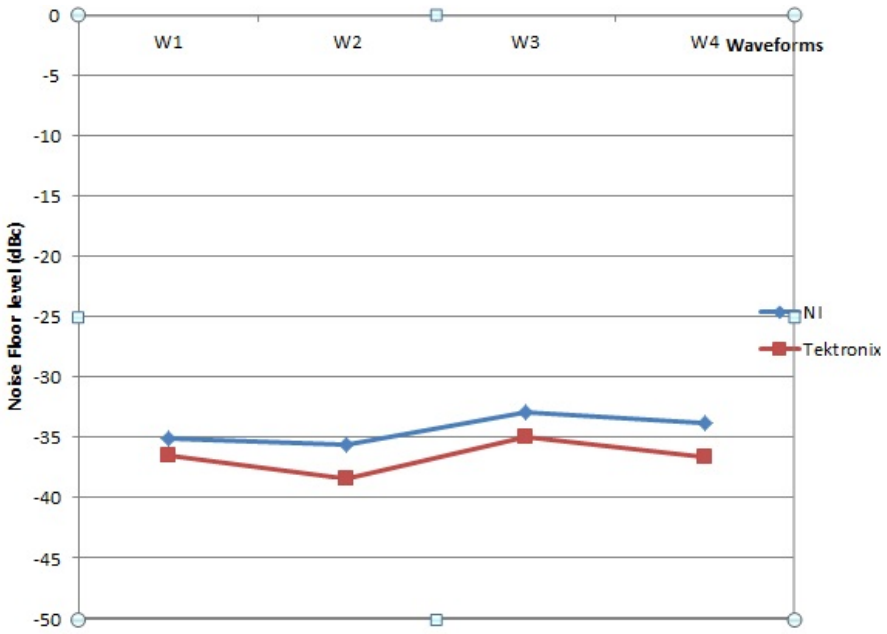


Figure 5-22: Comparing the Noise Floor (for various waveforms) of NI and Tektronix

duration was made 100 μs which is equal to the pulse duration as per the project specification. The following waveforms were generated and analyzed:

- W1: LFM spanning bandwidth 100 MHz to 150 MHz, duration 1000 μs
- W2: LFM spanning bandwidth 200 MHz to 300 MHz, duration 100 μs
- W3: LFM spanning bandwidth 200 MHz to 370 MHz, duration 100 μs
- W4: LFM spanning bandwidth 150 MHz to 350 MHz, duration 1000 μs

From Figure 5-22, it is clear that the difference in the noise floor levels has a maximum value of 2.74 dB. Please refer to Appendix D for more details on the measurements. Thus it could be concluded that that this design generates waveforms with specifications that are almost on par with the dedicated signal generator.

5-12-3 Performance enhancement after filtering

The DAC module in the AWG produces unfiltered output. When integrating with the space time coded radar test bed, the AWG block is followed by the RF Module that up converts and amplifies the AWG output to the final frequency of transmission. The AWG output requires a filtering before it is fed to the mixer for upconversion. Otherwise, mixer being a non-linear device can generate several undesired frequency components. The performance enhancement in the presence of filter has been studied. Figure 5-23 shows the AWG output for the chirp waveform with following specifications:

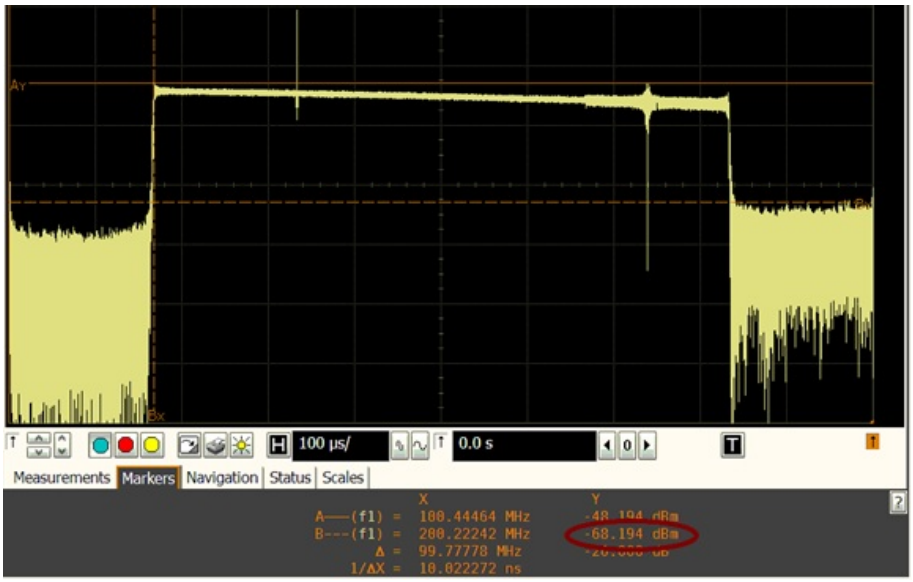


Figure 5-23: Unfiltered output of AWG

Part number	Center Freq. (MHz)	1dB Pass Band (MHz)	I_{ns} L. at F0 (dB) Max	Rejection (dB) Min		VSWR Max
				@MHz	@MHz	
WBLB-T-BP-300-230-L	300	185-415	1.0	60@100	60@500	1.5

Figure 5-24: Filter Specifications

- Signal Bandwidth: 200MHz
- IF: 300MHz
- Duration: 1 ms
- Amplitude: $1V_{pp}$ (single ended)

The noise floor level measured by the oscilloscope is -68.194 dBm. The output of the AWG is now filtered using a band pass filter[1] with the specifications given in Figure 5-24. The filtered spectrum is illustrated in Figure 5-25. The noise floor level of the filtered signal is -77.387 dBm. Thus with the band pass filter following the AWG output, the noise floor level improves by 9.2 dB.

5-13 Waveform Libraries

The AWG design has been designed, implemented and tested. A library containing various sets of waveforms has been created and is made ready to be used with the AWG. The waveforms in the library have the following specification:

[1] http://www.ainfoinc.com

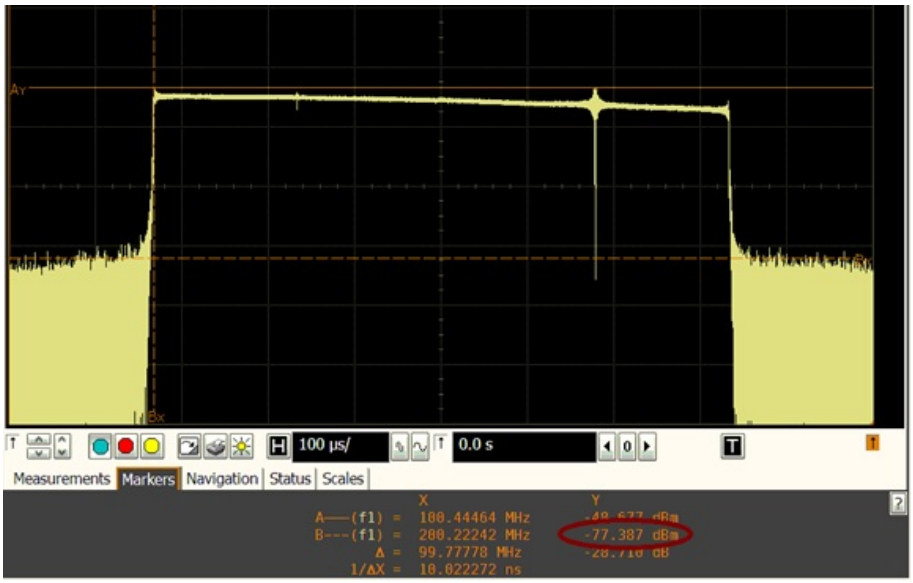


Figure 5-25: AWG output after filtering

- Signal Bandwidth: 200MHz
- IF: 280MHz
- Duration: 1 ms
- Dutycycle: 10%
- Amplitude: $1V_{pp}$ (single ended)

Two sets of waveforms have been included in the library

1. Circulating LFM
2. Cubic Alltop sequence

5-14 Integration with the RF Module and Antenna

The AWG has been successfully integrated with a dual channel RF Module and initial test runs were completed. Currently, the two outputs of the AWG are used to drive the dual channel RF transmitter. The RF module output is transmitted by two antennas. The single channel receiver antenna collects the refelcted signal, which is then downconverted and captured. This integration realised a 2X1 MISO radar system. The transmitted and received signals in different scenarios were captured for further signal processing. Details on the integrated test set up shared in Appendix E.

5-15 Conclusion

The chapter discussed the various strategies adopted in the design and implementation of the AWG. The testing procedures adopted to validate the designs have been described. The technical issues faced and the methods of solving them have been discussed. The results of all the three designs have been shared which was followed by a comparison on their performances. The performance of 8 bit design has been compared and evaluated with respect to the 14 bit design and satisfactory results have been obtained. The 8 bit design has also been compared with the Tektronix signal generator and it was found that the design is comparable to the Tektronix AWG5014B. Different modes of operations of the AWG has been focussed in the later section followed by the details on the marker signals. Finally, it has been shown that the performance of the design has been enhanced in the presence of a band pass filter. Finally, the AWG has been integrated and successfully tested with the dual channel RF module and antennas.

Chapter 6

Conclusions and Recommendations

6-1 Conclusions

In this thesis, an eight channel AWG block for a multi-channel transmitter within a space time coded MIMO radar test bed has been successfully configured, characterized, designed and implemented. A survey of currently available platforms in the market was initially done, at the end of which the existing hardware platform was finalized. The hardware characterization of the whole system was performed for a number of parameters like dc offset, time offset, frequency response, spurious responses and phase noise.

It has been observed and measured that the dc offset in the channels of the AWG is negligible and sums up to less that 0.2 percent of DAC full scale reading. The presence of dc offset can cause saturation of the receiver front end thereby disrupting the performance of the radar. Since this AWG is used within a MIMO radar test bed, the cumulative value of dc offsets from the multiple channels, if at sufficient levels, may cause distortion at the receiver. This could be prevented by several dc offset nulling mechanisms like pre-distortion, feedback control etc. The measured values could be made use of to pre-distort the signal and null the effect of dc offset.

The time delay among all the channels of the AWG has been measured and it has been observed that the delay among the various channels remained constant. The maximum delay among the channels was lesser than 160 ps. For a waveform with 200 MHz bandwidth (with a pulse width of 5 ns), this delay corresponds to 3.2 percent of pulse width. Thus the clock synchronization results in less than 3.2 percent of sample period. The time offset is among channel is critical in the AWG because, this system forms an integral part of multichannel coherent radar. Synchronization among the channels is one of the pre-requisites for such a system.

The DAC output has been studied for the spurious responses after observing the rise in spurious level when the DAC was operated on full scale. This measurement led to the conclusion that the optimal performance of the DAC is achieved when run at half full scale. The main

source of spurious frequency in the first Nyquist zone was the harmonic frequencies. Beyond 312 MHz, sources of the spurious are the image frequencies that get folded back to the first Nyquist zone. These measurements are of importance to the radar test bed since, it determines the dynamic range of the system and hence the performance.

The frequency response study conducted on the AWG hardware system shows the DAC roll off and throws light on the envelope degradation of the signal at high frequencies. The AWG is designed to generate wide band signals (with bandwidth as high as 200 MHz, centered at an IF of 300 MHz). Hence the frequency response data could be made use of to pre-distort the data to combat the DAC roll off and make the envelope flat over the region of operation. However, it has also been measured and concluded that the frequency response of the system is found to be better than that of the standard signal generator inhouse.

The limitations and difficulties that need to be overcome while implementing the AWG that could generate a waveform of the given specification, have been introduced and discussed. The waveforms have bandwidths as high as 200 MHz and the a PRF of 1kHz. These waveforms when generated at a sampling rate of 1.25 GHz contain 1.25 MSamples per channel and require the on-board memory (DRAM) for data storage. This results in the rate discrepancy since the DRAM cannot deliver the data as fast as the DAC interface demands. Three design strategies were proposed, designed, implemented and tested successfully.

The performance of the system was not initially satisfactory because of lack of synchronization and glitches at the output. This has been successfully solved by correcting the clock source of the loop that supplies the data samples to the DAC interface. The code has been improved and optimized to meet the sufficient throughput. This is of prime importance because, as mentioned earlier, synchronous waveforms from the multiple channels is the key to coherent processing in MIMO radar, without which the system could prove to be useless.

The AWG system has been programmed to work in different modes of operation, burst mode and continuous mode. In burst mode, the system transmits a fixed number of pulses and waits for the next trigger (from the host) to start the transmission. For transmitting the same waveform N times inside a burst, a scalable code has been developed instead of loading the DRAM with a waveform N times longer. In continuous mode, the system continues to transmit the waveform until it receives a signal (from the host) to stop transmission.

The marker signals to denote the ON and OFF period of the transmitted pulses has been generated. These signals which mark the exact beginning and end of pulses could be made use of at the receiver signal processing. Since the data access from the DRAM involves pipelining, the DRAM address could not be made use of to generate the signals. Hence a logic circuit was implemented inside the FPGA that compares the current values of the eight samples to the fixed point equivalent of 0 V. The output of this logic circuit is internally routed to the Trigger out SubMiniature version A(SMA) connecter of the AT 1212 DAC board.

It has been observed that the trigger signal leads the analogue output by a fixed time offset of 64.795 ns. This delay could either be account inside the FPGA or externally.

The performance of the three designs have been compared in terms of the following parameters

1. Number of channels
2. Maximum frequency of generation

3. SNR of the system

Considering the specification of the waveform generated, the number of channels required and finally after measuring the performance, it could be concluded that the eight bit waveform design proves to be the ideal choice for the present requirement.

Finally, the AWG has been integrated with a dual channel RF module and initial test runs were conducted. The transmitted and received waveforms for various scenarios have been acquired for further processing.

The work completed in this thesis contributes to the paper describing the X-band MIMO demonstrator, that is being prepared to be submitted at the EuRAD (European Radar) conference 2014.

6-2 Recommendation and Future Work

From the measurements carried out on the AWG hardware, the following recommendations could be deduced which could improve the performance of the system

1. Studies made on the spurious response shows that shifting the IF towards left (i.e) lowering the IF gave better performance. This could lead to more complicated filtering. Hence a suitable lower IF value could be chosen if the application demands a better spurious performance. For example, waveform occupying the frequency band from 200 MHz till 400 MHz could be shifted to 185 MHz to 385 MHz (1 dB pass band of the band pass filter following the DAC). This could improve the SFDR by 2 dB and the signal output level by 0.5 dB

2. Depending on the application specification, the best design could be chosen among the three options. A suggestion to improve Design 2 (design involving interpolation) is to re-design the interpolator. The ideal interpolation factor is 1.5625. Rounding this value to 1.6, an interpolator could be implemented in the FPGA. The interpolation could be applied on sets of 40 samples. With an interpolation factor of 1.6, this would produce 64 samples for every incoming 40 samples. This could also slightly increase the maximum frequency that could be generated by the design. Also, a better interpolation technique other than the linear interpolation could be considered.

3. Similarly, Design 3 (waveform generation using 8 bits) could be re-designed by representing the waveform using more number of bits. Ideally, representing the data in 10 bits should give the theoretical throughput required to maintain a sustained data flow between the FPGA and DAC. As an effort to improve the quantization error, this design could be modified to generate the waveforms using 10 bits, instead of 8.

4. Investigation of the effects of lowering the DAC clock rate from 1.25 GHz till 800 MHz could be conducted. This method of lowering the DAC clock by using an external clock would help to match the throughput rate. However, it would require an external clock source that can provide the synchronised clock for all the modules. It would also have limitations on the maximum frequency that could be generated (according to Nyquist criterion). This would be a limitation on the generation of waveform as per current specifications.

5. The AWG could be syncrhonized with the RF Module so that the the complete radar testbed including the AWG, LO used in the transmitter and receiver are locked to a single reference. This could be accomplished by using an external reference (the same reference used by the LO in the transmitter and receiver) to generate the DSTARA clock inside the Timing and Synchronization Module. This reference clock could be easily fed to the clock reference in connecter in the AWG PXIe Chassis. For the correct functioning of the coherent test-bed, this syncrhonization is of most importance since lack of phase relationship can cause undesired and wrong results.

Appendix A

A-1 Matlab code for waveform generation

```
%Matlab script to develop a continuous wave radar signal
%Author : S. R. Kadathanad
clear all;
close all;
clc;
Fs=5e9;
f=1e9;
t=0:1/Fs:511/Fs;
y=sin(2*pi*f.*t);
plot(t/(1e-6),y);
Title('Continuous Waveform for Radar');
xlabel('Time(us)');
ylabel('Amplitude(V)');

%Matlab script to develop a pulsed wave radar signal

t=0:1/Fs:511/Fs;
for i=1:100
    ynew(i)=y(i);
end
for i=101:200
    ynew(i)=0;
end
for i=201:300
    ynew(i)=y(i);
end
for i=301:400
    ynew(i)=0;
end
for i=401:500
    ynew(i)=y(i);
end
for i=501:511
```

```
34      ynew(i)=0;
35  end
36  figure
37  plot(t(1:511)/(1e-6),ynew);
38  Title('Pulsed Waveform for Radar');
39  xlabel('Time(us)');
40  ylabel('Amplitude(V)');
41
42  %Matlab script to develop a linear frequency modulated waveform for radar
43
44  Fs=10e9;
45  Fcentre=1e9;
46  t=0:1/Fs:2047/Fs;
47  dF1=10e4;
48  Waveform_LFM = chirp(t,Fcentre-dF1/2,1e-9,Fcentre+dF1/2);
49  figure
50  plot(t,Waveform_LFM);
51  Title('Linear Frequency Modulated Waveform for Radar');
52  xlabel('Time(us)');
53  ylabel('Amplitude(V)');
54  close all;
```

Appendix B

B-1 Schematic of the RF Module

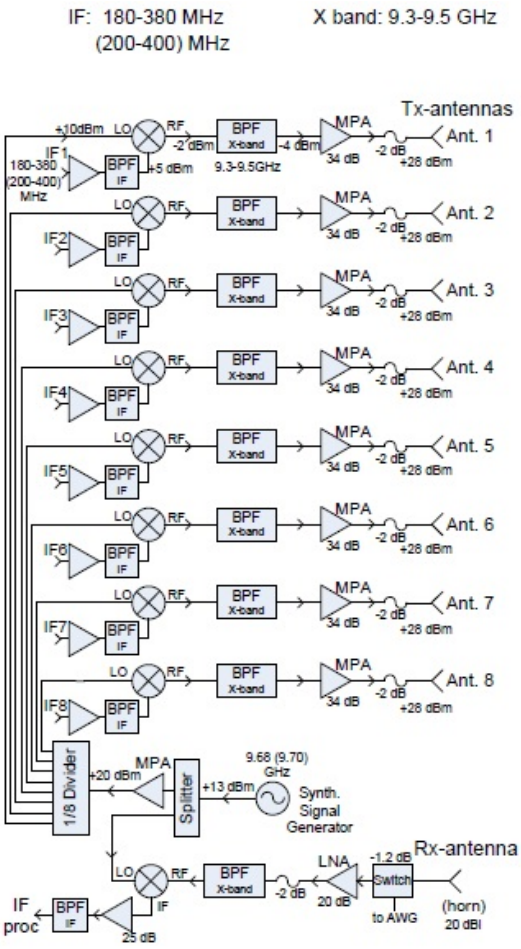


Figure B-1: Schematic of the RF Module for the space time coded MIMO radar

Appendix C

C-1 Spectral Analysis of 8 bit and 14 bit waveforms

This section shares the results of the measurements conducted to compare the SFDR of the 8 bit design with that of 14 bit design. The measurments have been conducted by generating tone frequencies at 100 MHz, 200 MHz, 300 MHz, 400 MHz, 500 MHz and 600 MHz

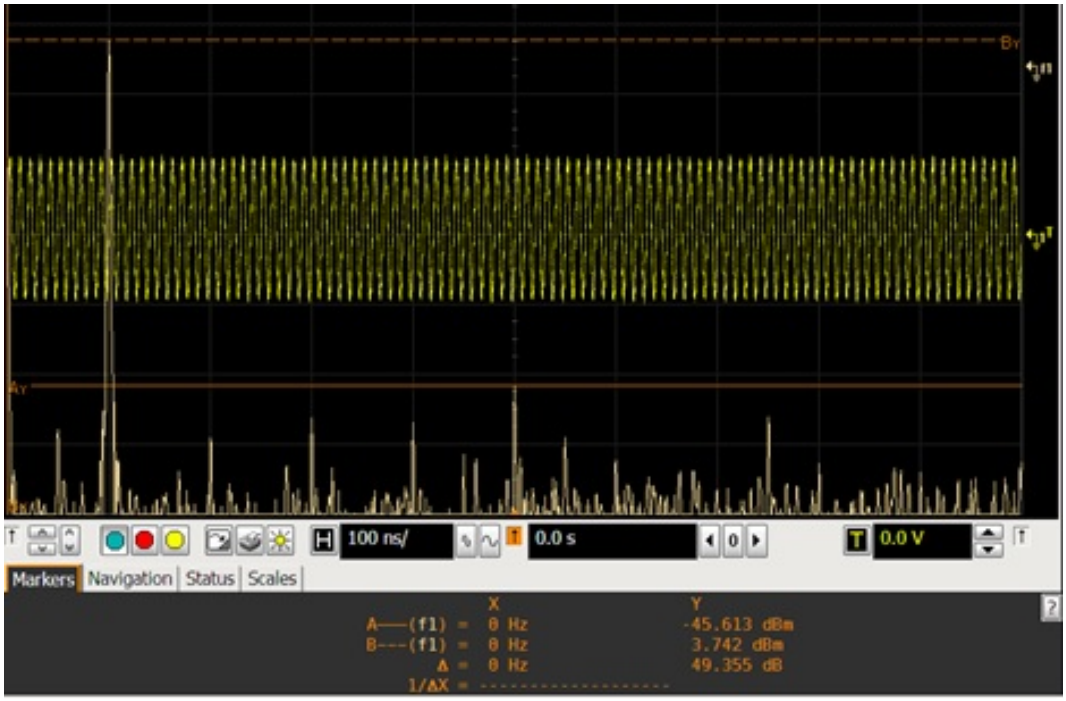


Figure C-1: Frequency:100 MHz, 8 bit design, SFDR: 49.355 dB

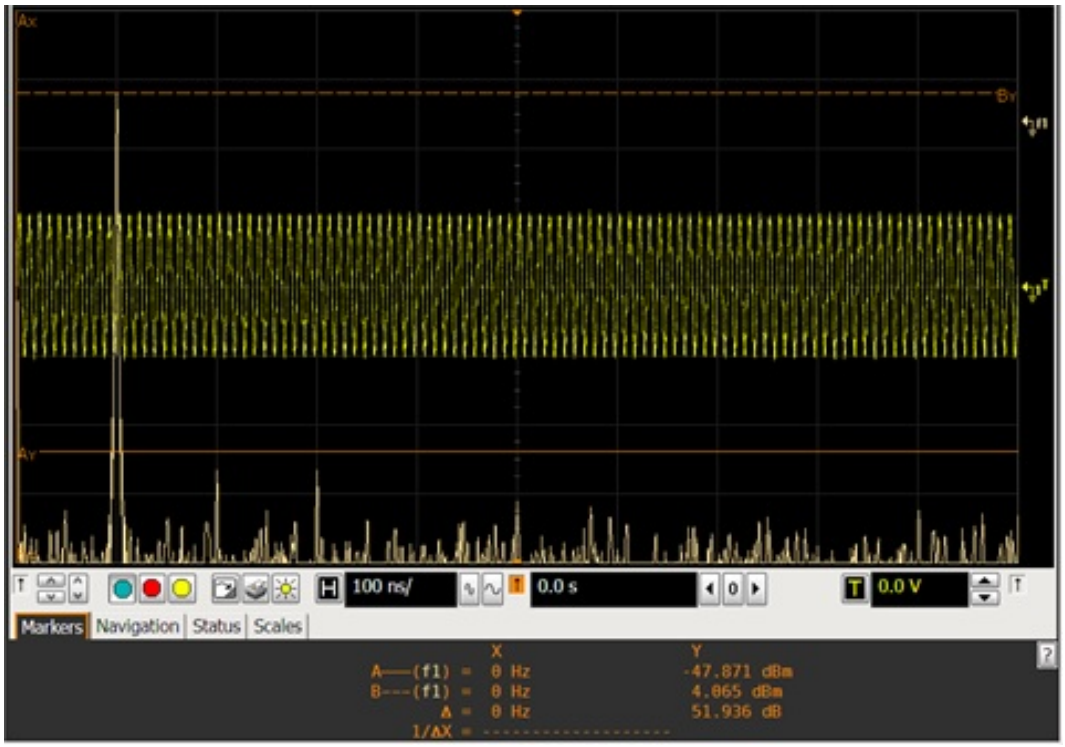


Figure C-2: Frequency:100 MHz, 14 bit design,SFDR: 51.936 dB

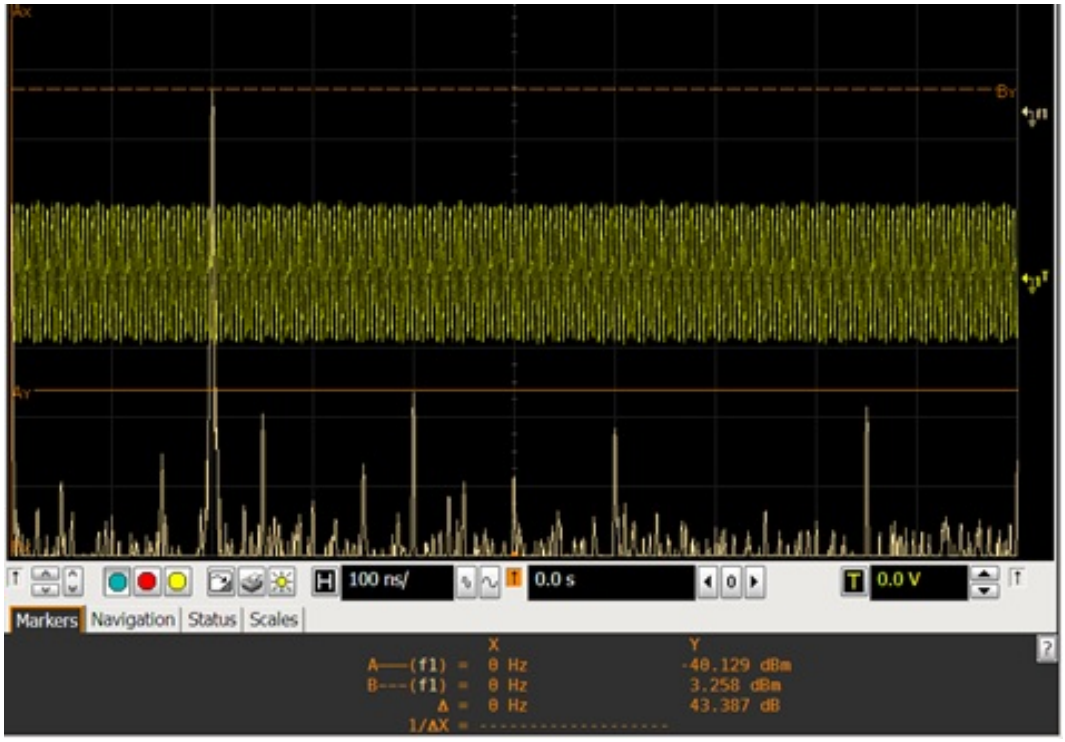


Figure C-3: Frequency:200 MHz, 8 bit design, SFDR: 43.387 dB

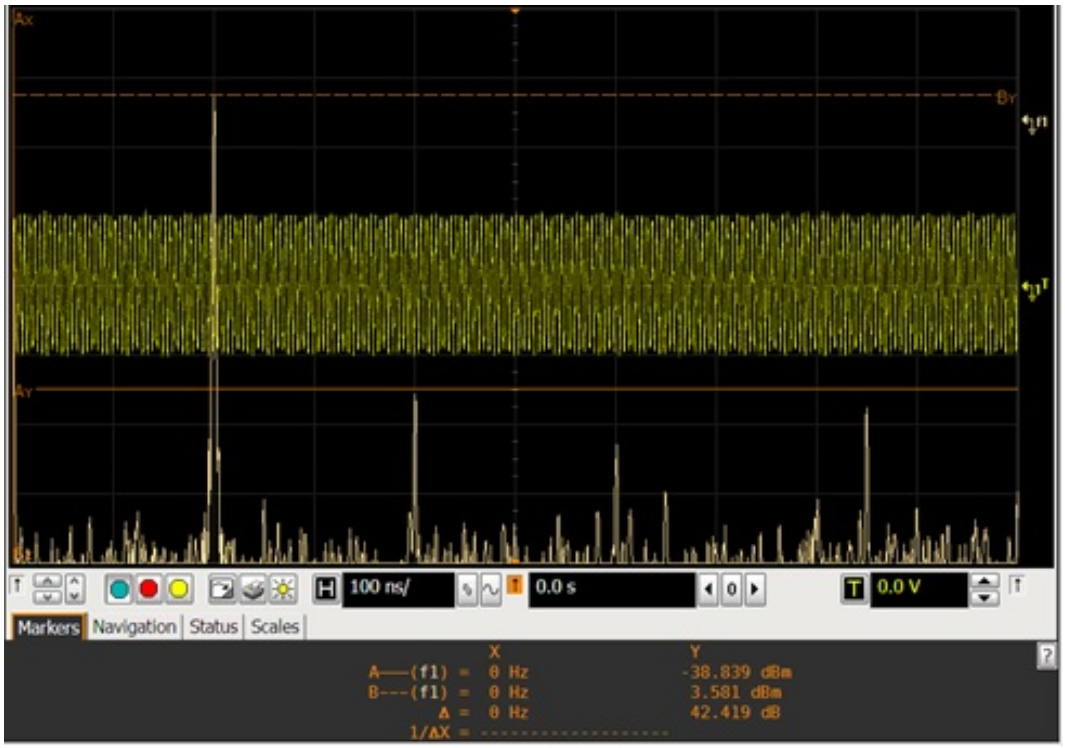


Figure C-4: Frequency:200 MHz, 14 bit design, SFDR: 42.419 dB

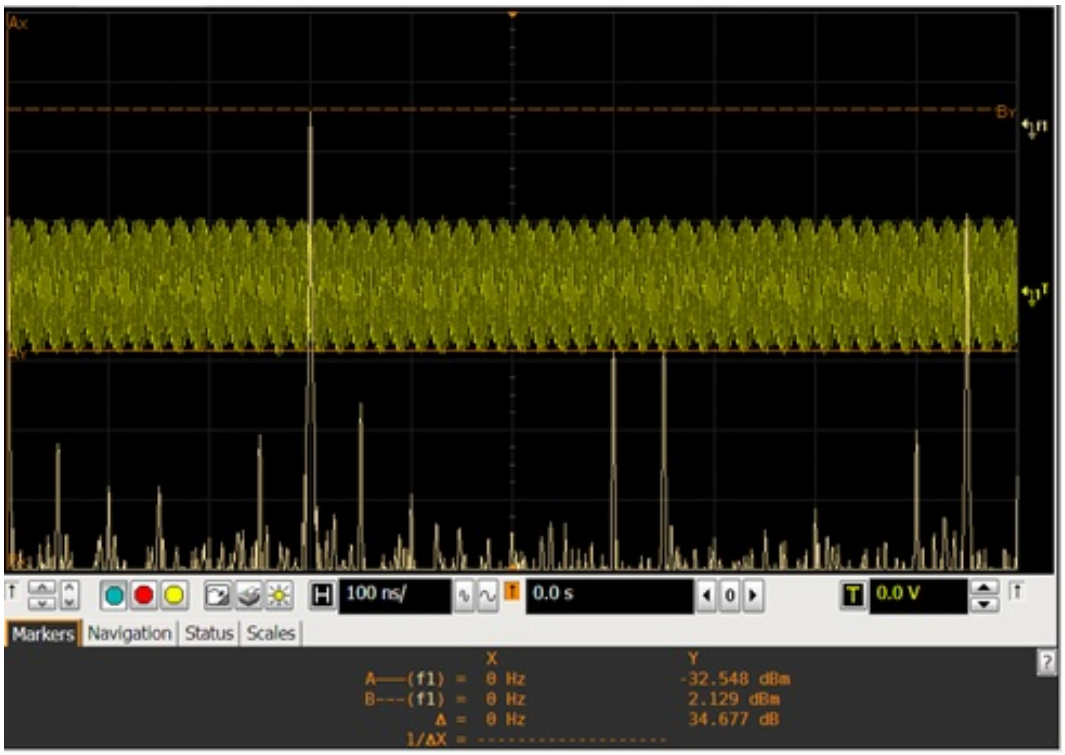


Figure C-5: Frequency:300 MHz, 8 bit design, SFDR: 34.667 dB

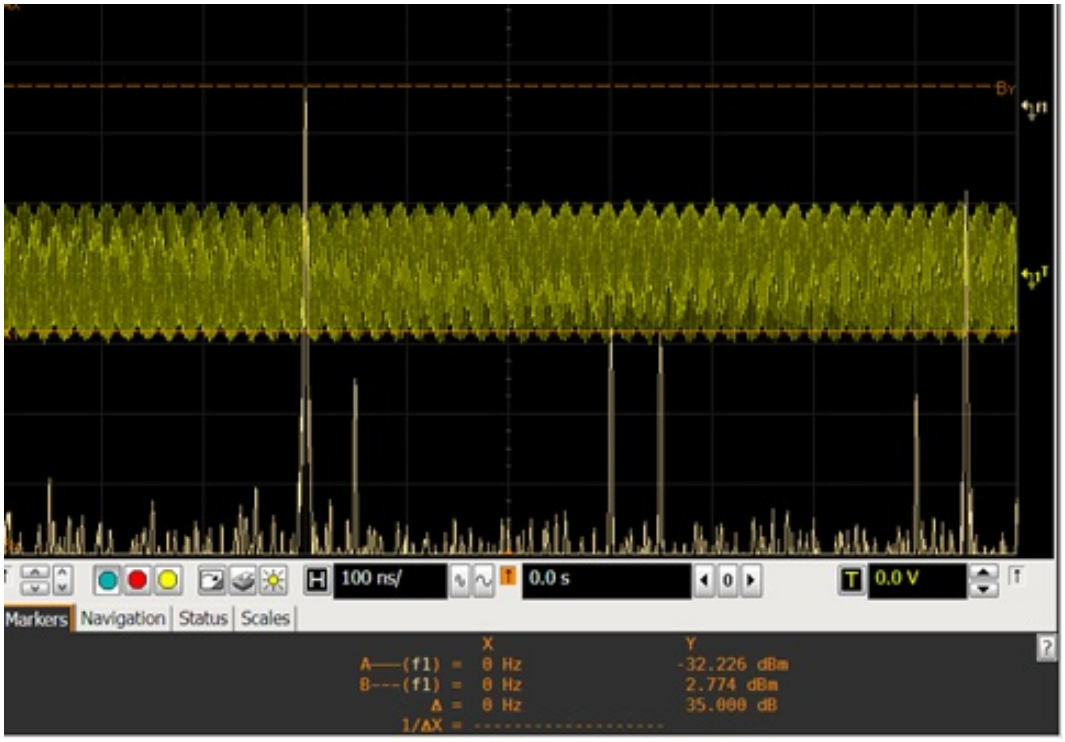


Figure C-6: Frequency:300 MHz, 14 bit design, SFDR: 35.000 dB

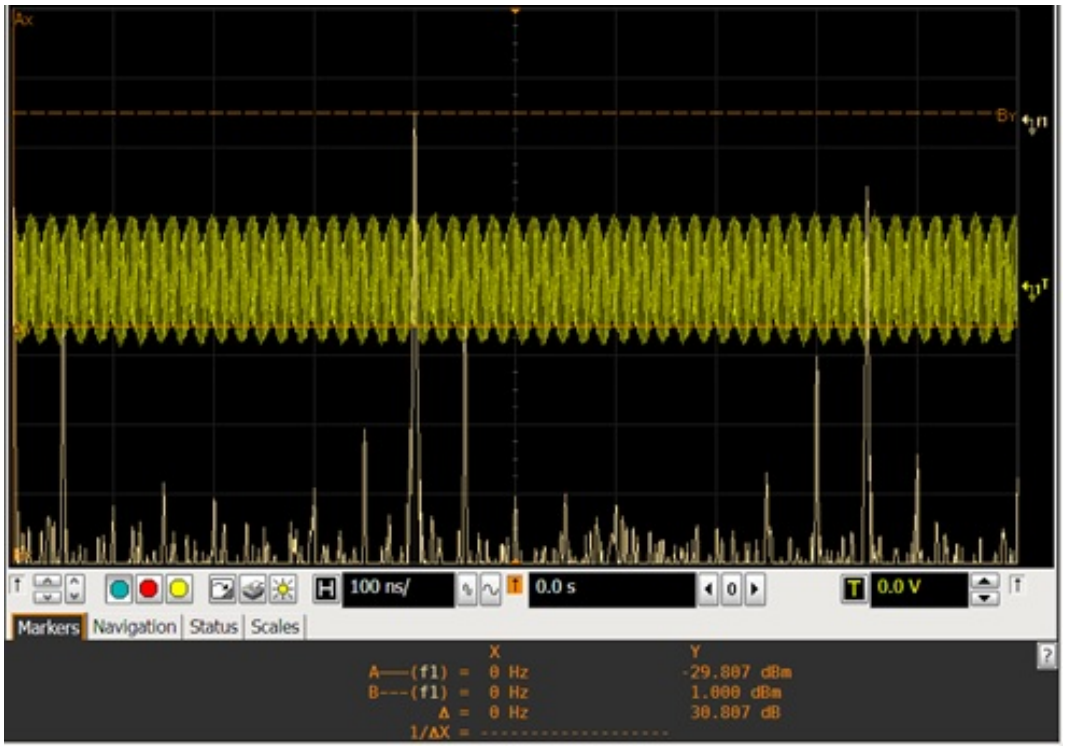


Figure C-7: Frequency:400 MHz, 8 bit design, SFDR: 30.807 dB

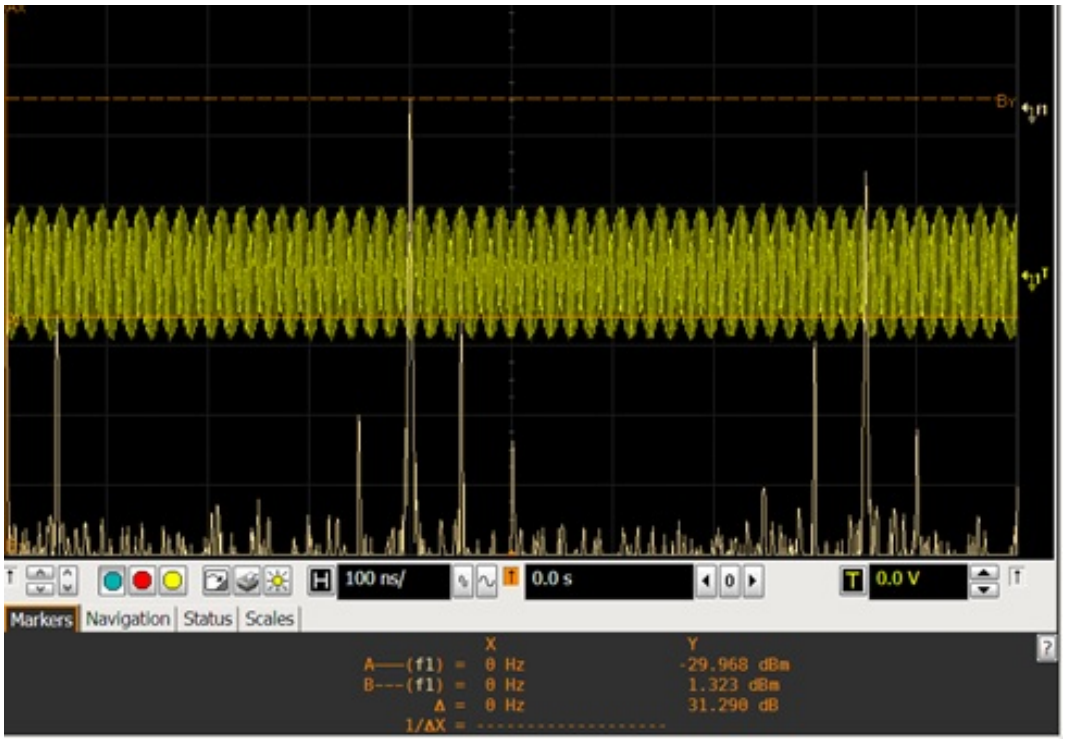


Figure C-8: Frequency:400 MHz, 14 bit design, SFDR: 31.290 dB

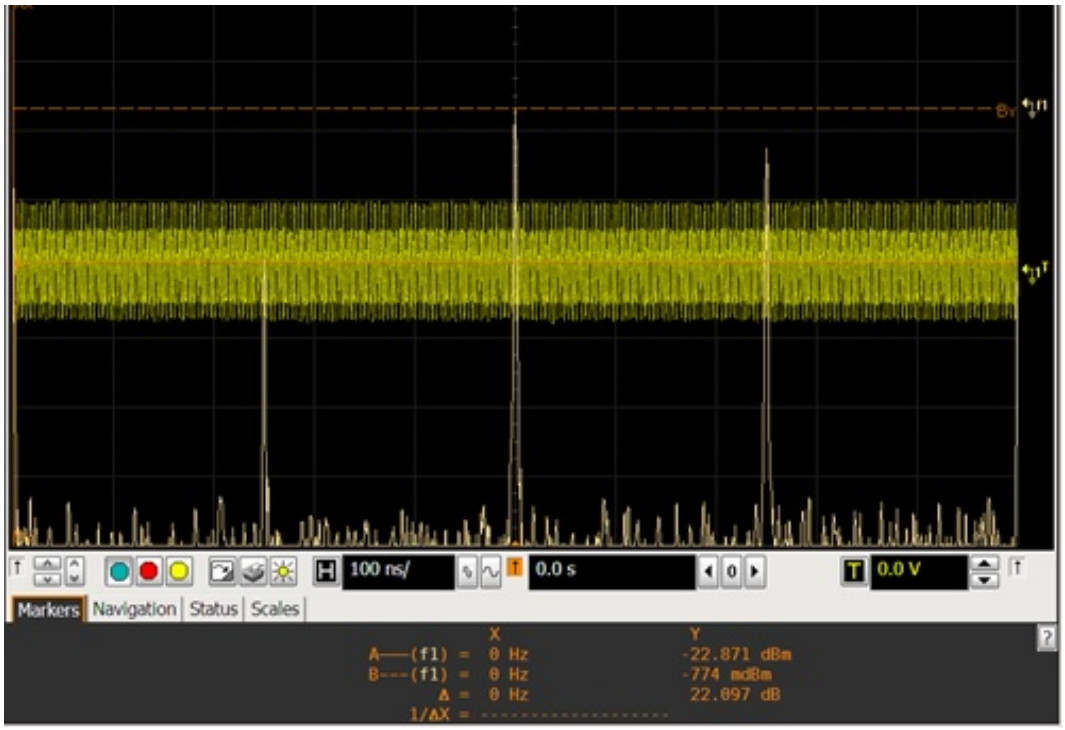


Figure C-9: Frequency:500 MHz, 8 bit design, SFDR: 22.097 dB

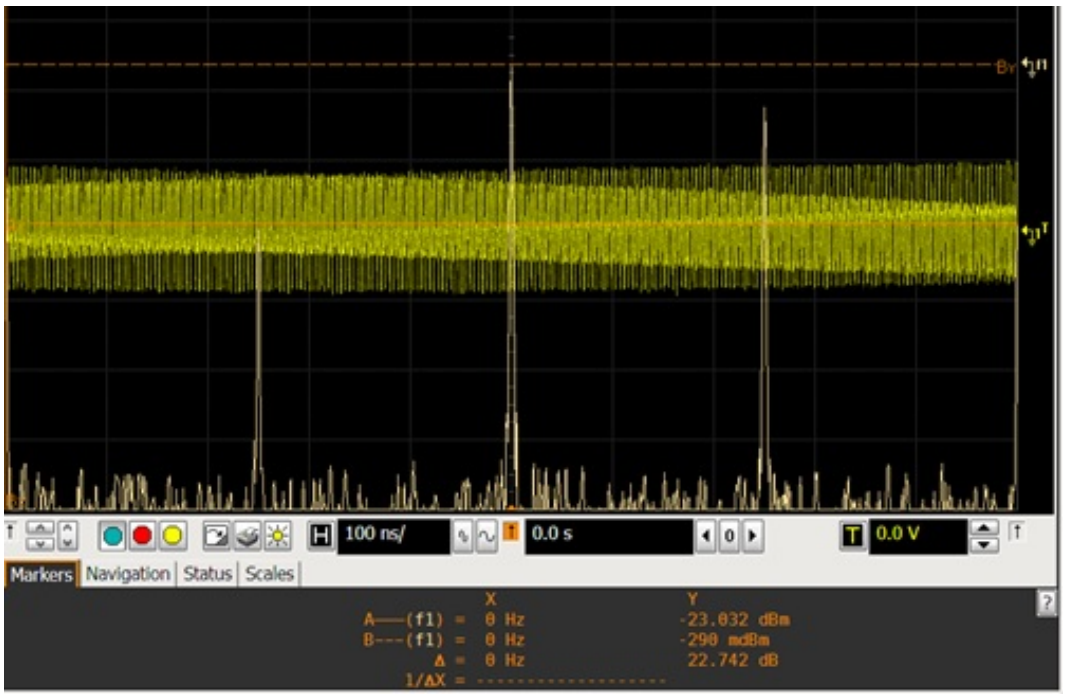


Figure C-10: Frequency:500 MHz, 14 bit design, SFDR: 22.742 dB

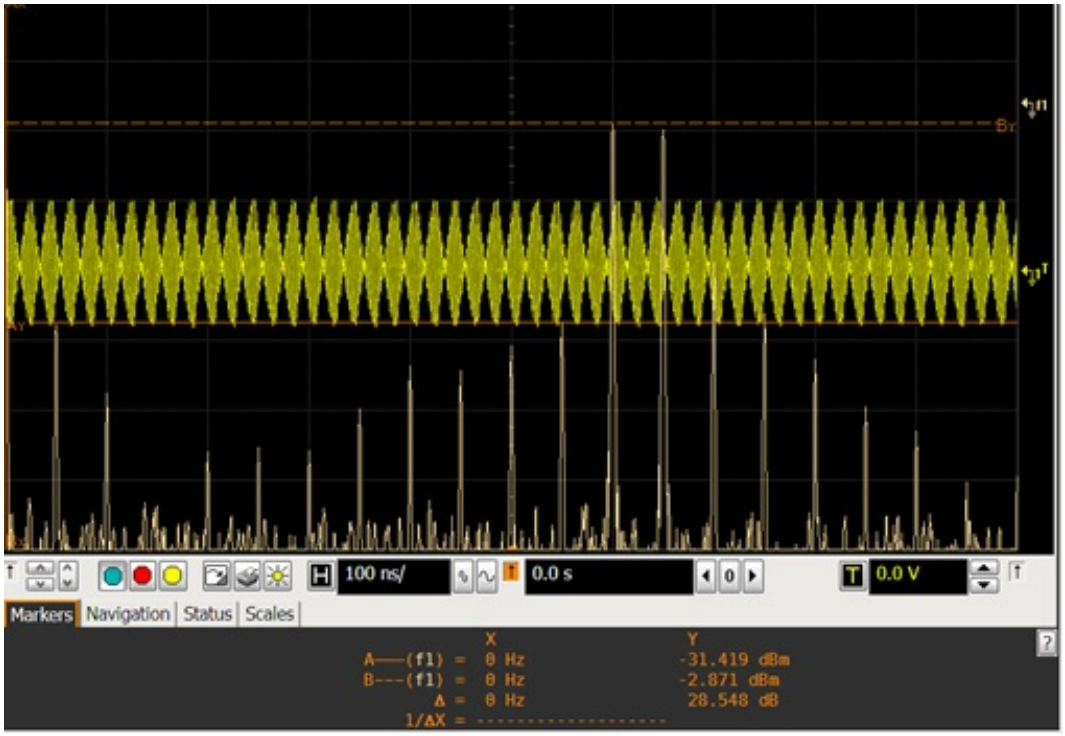


Figure C-11: Frequency:600 MHz, 8 bit design, SFDR: 28.548 dB

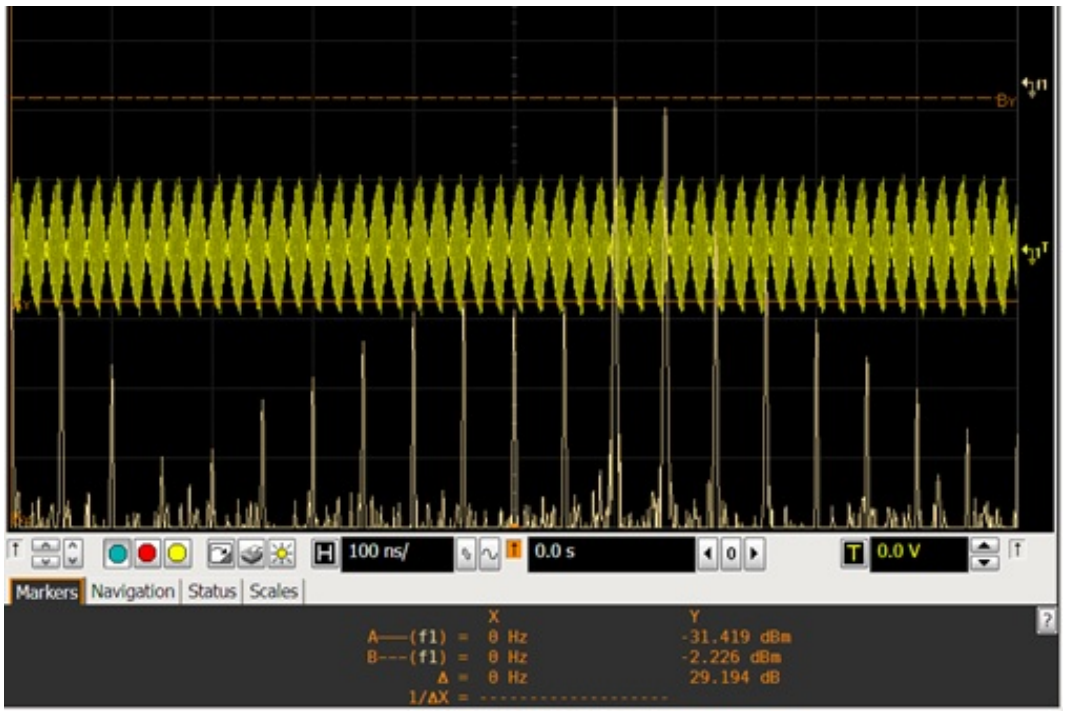


Figure C-12: Frequency:600 MHz, 14 bit design, SFDR: 29.194 dB

Appendix D

D-1 Noise Floor of NI AWG and Tektronix AWG

Waveform	**Signal Bandwidth (MHz)**	**Duration(μs)**	**Amplitude (V_{pp})**
W1	50	1000	1
W2	100	100	1
W3	170	100	1
W4	200	100	1

Table D-1: Waveform Specification

Sl. No.	Waveform	Signal envelope degradation inside bandwidth (dB)		Noise Floor(dB)		Noise Floor difference (NF(Tektronix)-NF(NI))
		Tektronix	NI	Tektronix	NI	
1	Waveform1	Flat	Flat	-36.452	-35.161	-1.291
2	Waveform2	-2.983	-1.290	-38.387	-35.645	-2.742
3	Waveform3	-5.645	-2.419	-35.000	-32.983	-2.017
4	Waveform4	-5.323	-2.258	-36.614	-33.871	-2.743

Figure D-1: Comparison of NI and Tektronix AWG

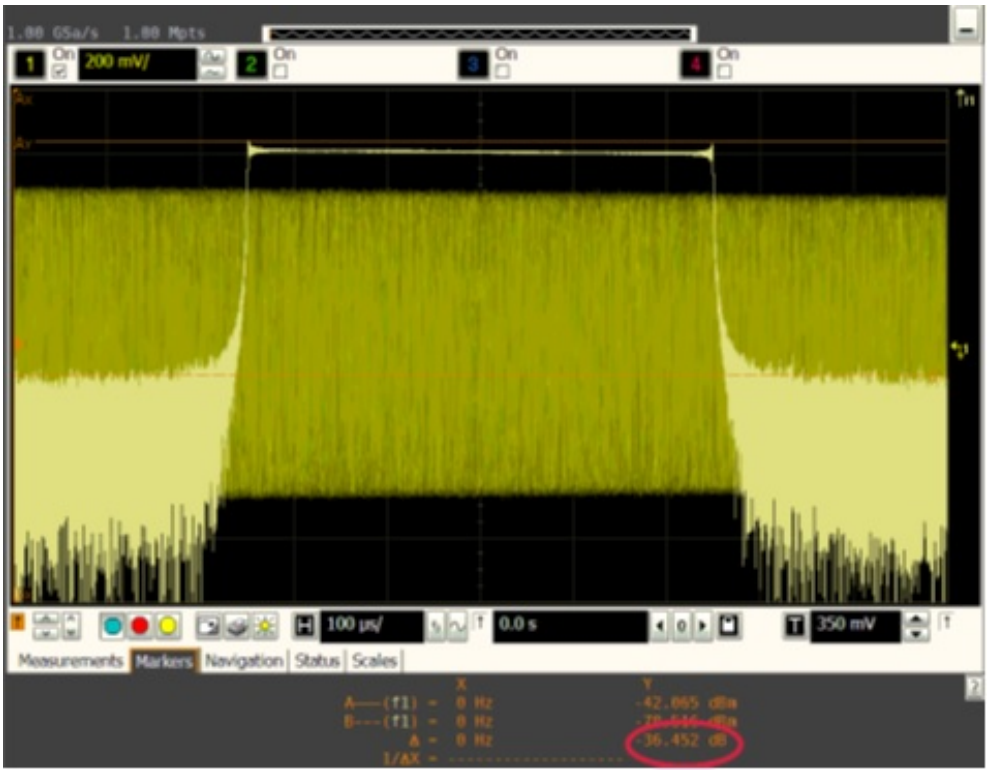


Figure D-2: Waveform 1, Tektronix AWG

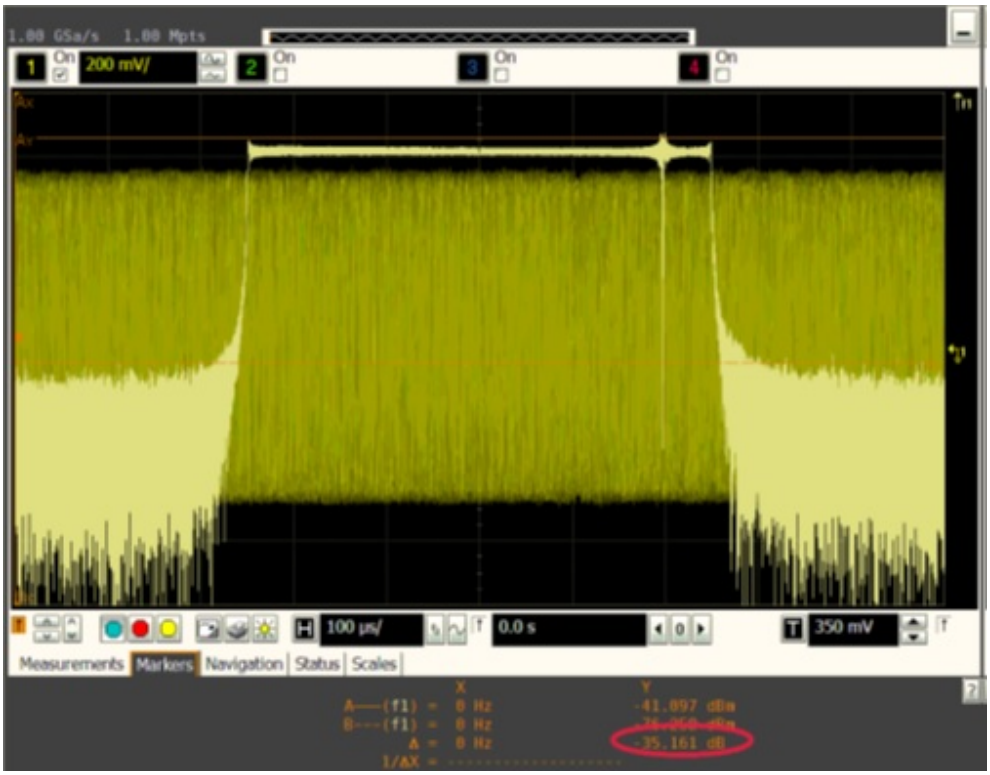


Figure D-3: Waveform 1, NI AWG

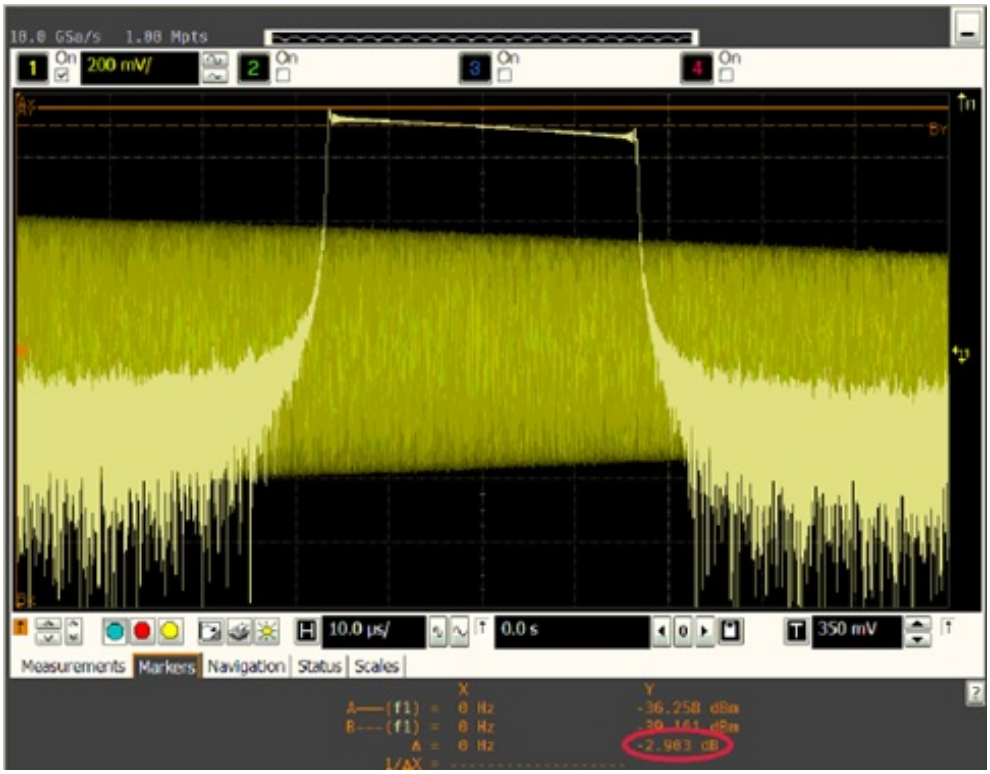


Figure D-4: Waveform 2, Signal envelope degradation, Tektronix AWG

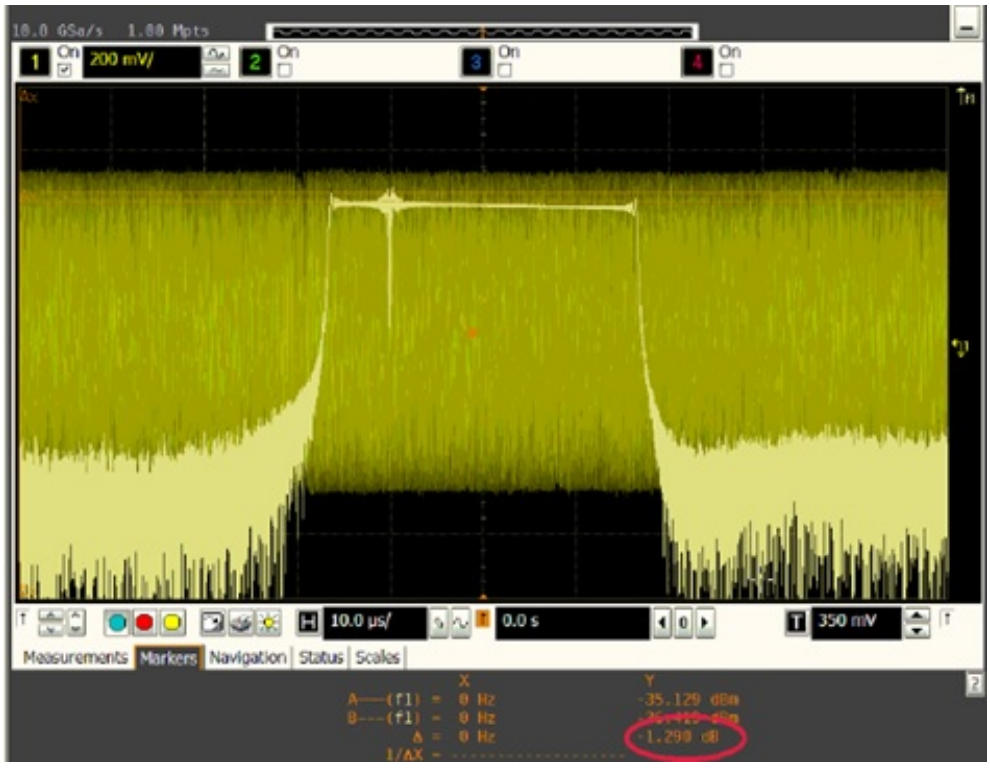


Figure D-5: Waveform 2,Signal envelope degradation, NI AWG

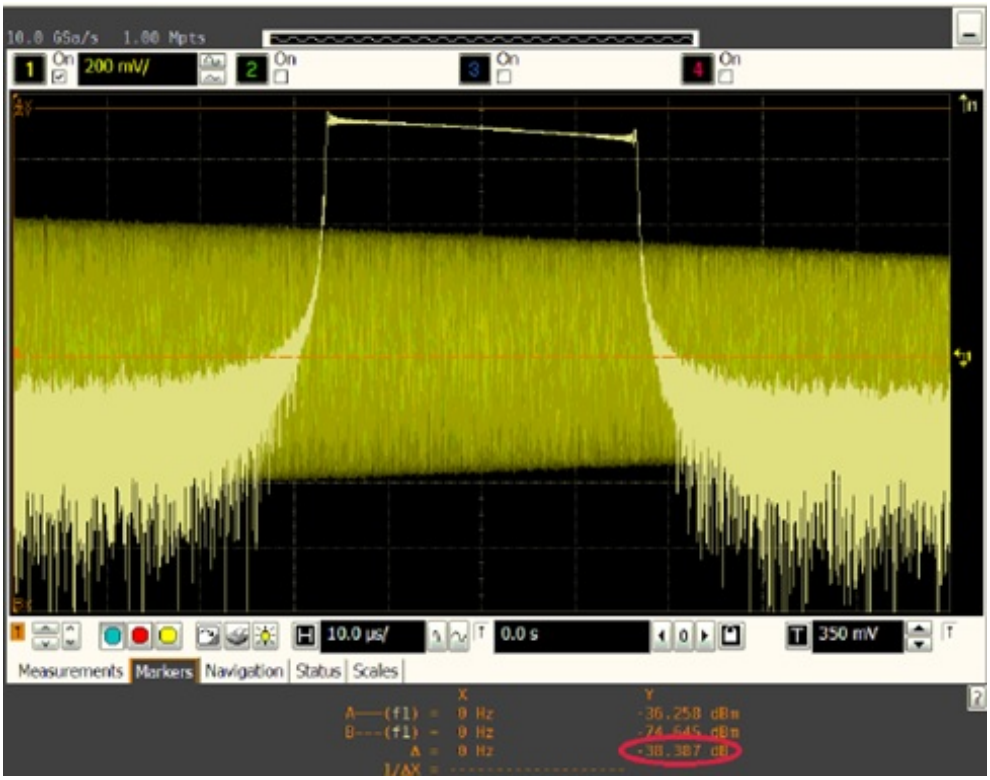


Figure D-6: Waveform 2, Noise Figure, Tektronix AWG

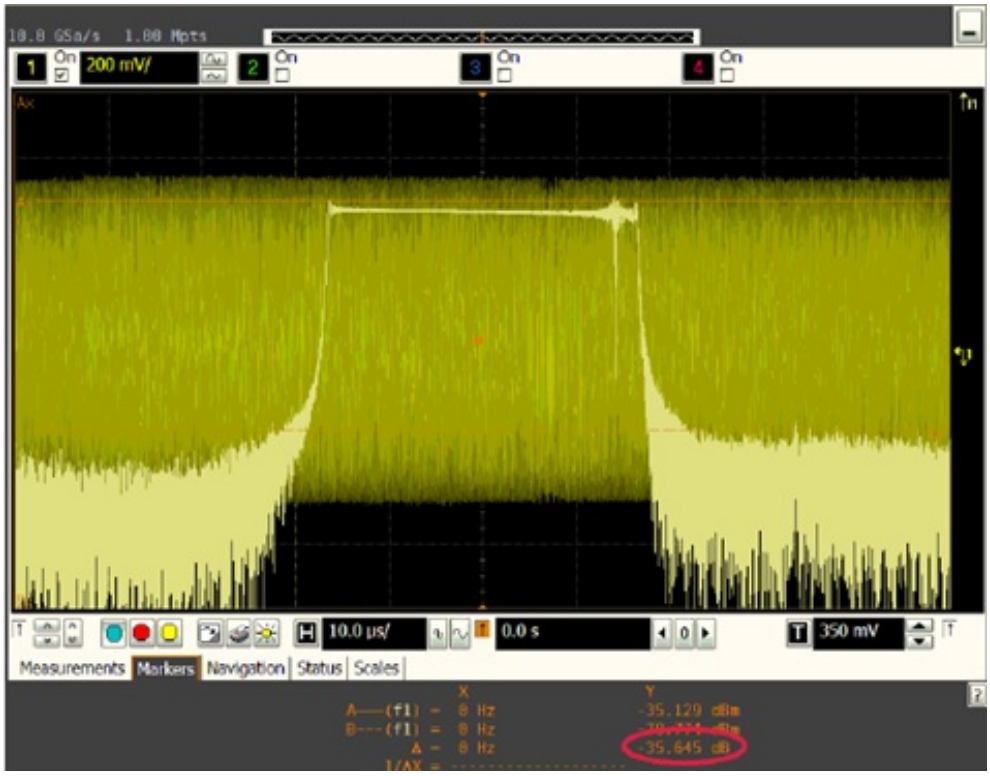


Figure D-7: Waveform 2,Noise Figure, NI AWG

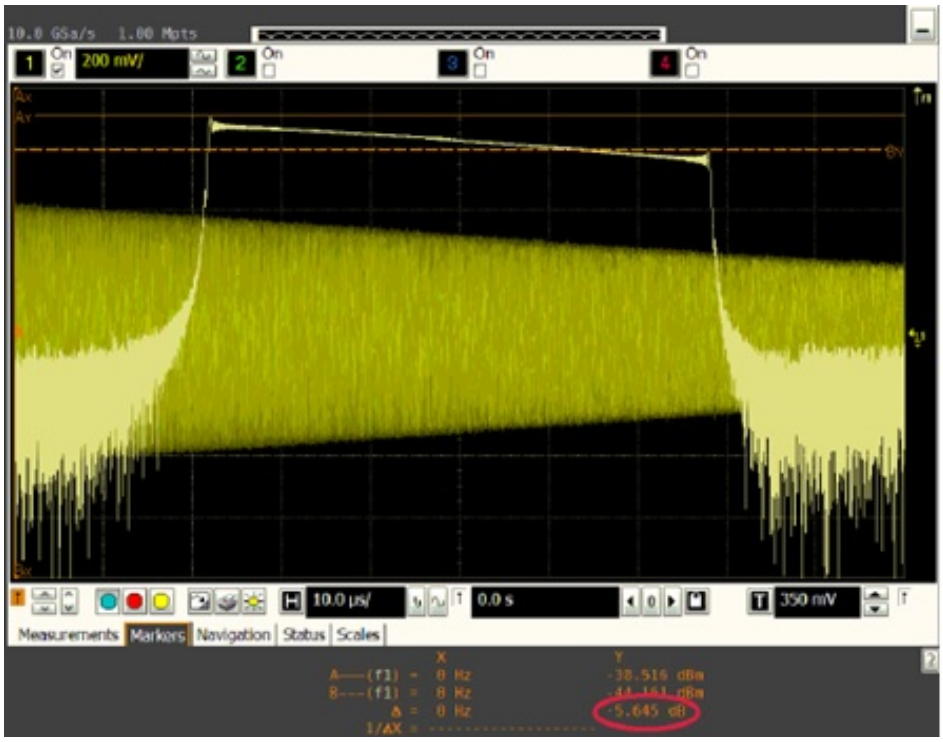


Figure D-8: Waveform 3, Signal envelope degradation, Tektronix AWG

Figure D-9: Waveform 3,Signal envelope degradation, NI AWG

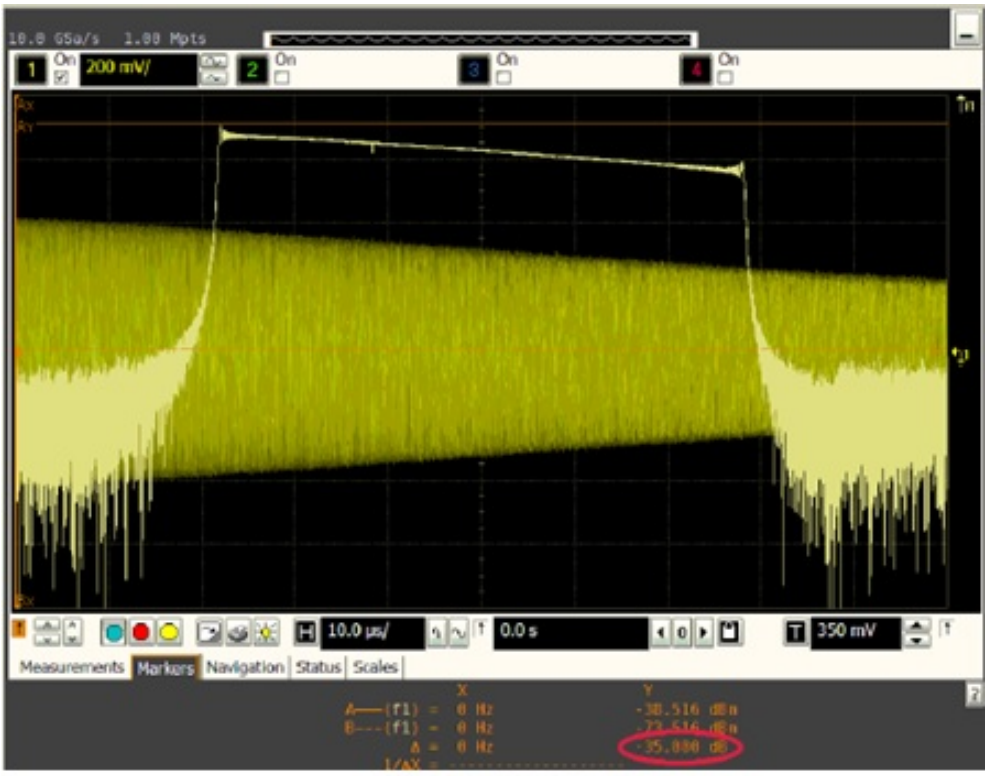


Figure D-10: Waveform 3, Noise Figure, Tektronix AWG

Figure D-11: Waveform 3,Noise Figure, NI AWG

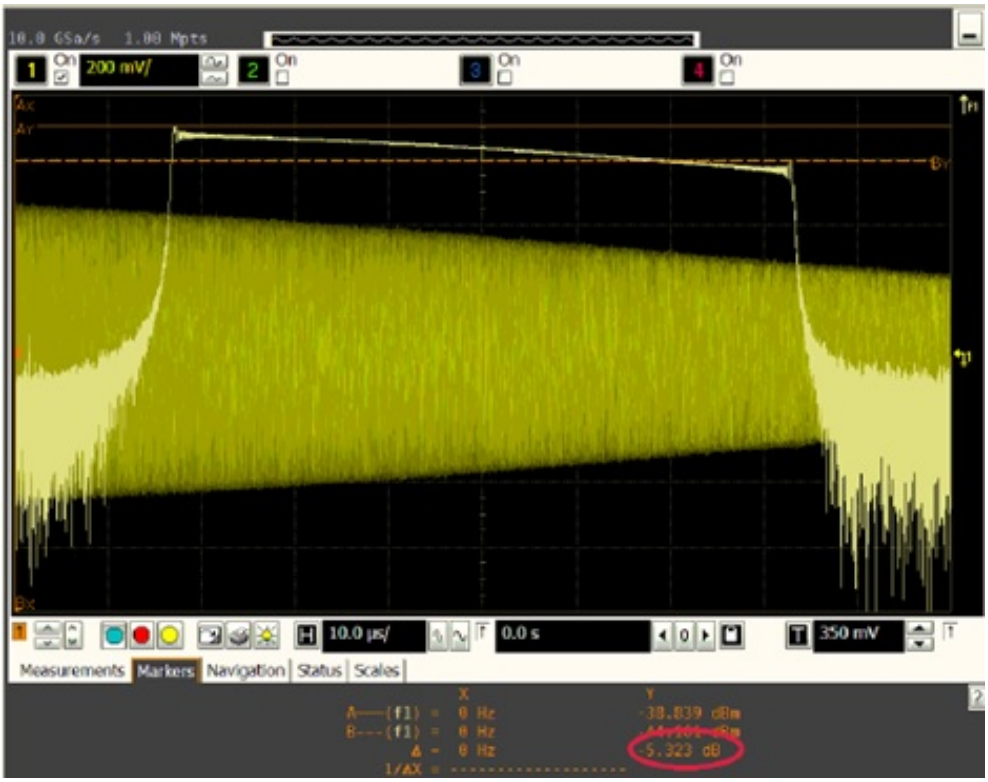


Figure D-12: Waveform 4, Signal envelope Degradation, Tektronix AWG

Figure D-13: Waveform 4,Signal envelope Degradation, NI AWG

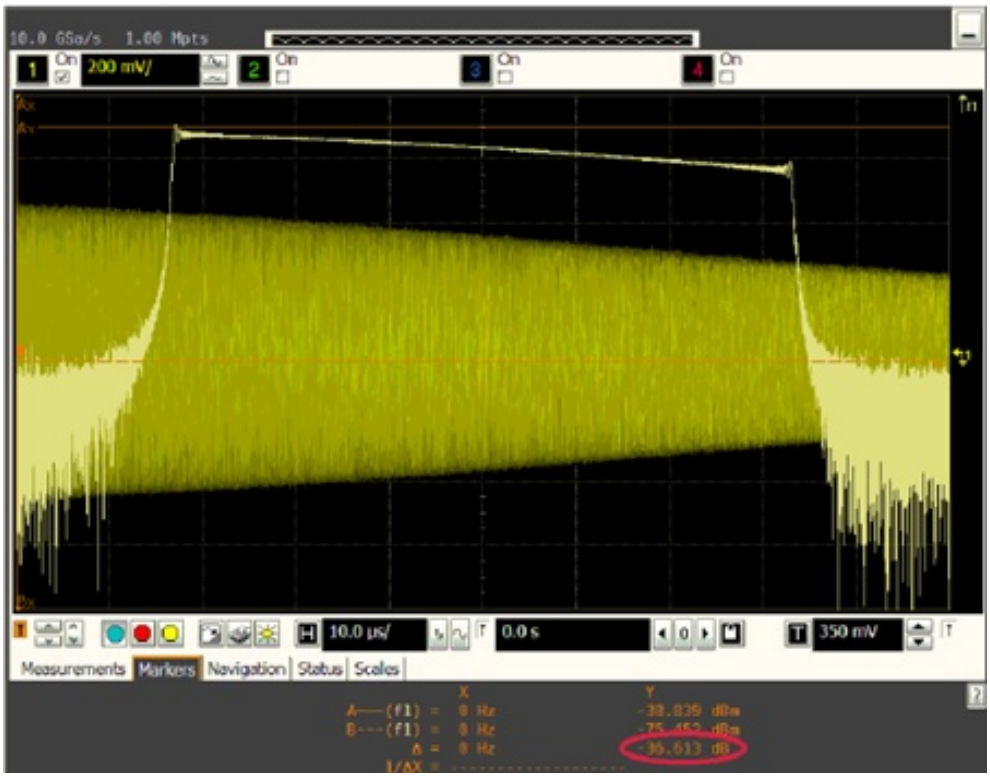


Figure D-14: Waveform 4, Noise Figure, Tektronix AWG

Figure D-15: Waveform 4,Noise Figure, NI AWG

Appendix E

E-1 Integration of AWG with RF Module and Antenna

The AWG has been operated in integration with a dual channel RF Module. The output of the RF Module has been transmitted by two antennas. The output of the receive antenna has been down converted and sampled by the Digital Oscillosope.

Figure E-1: AWG with the data acquisition unit to acquire the transmitted and receive signals

The dual channel RF Module that upcpnverts and amplifies the AWG ouptut and transmits through the horn antennas.

Figure E-2: RF Module and Antenna

The transmit and receive antennas.

Figure E-3: Transmit and Receive antennas

The dihedral reflector that was used as a dominant scatterer while the tests were conducted.

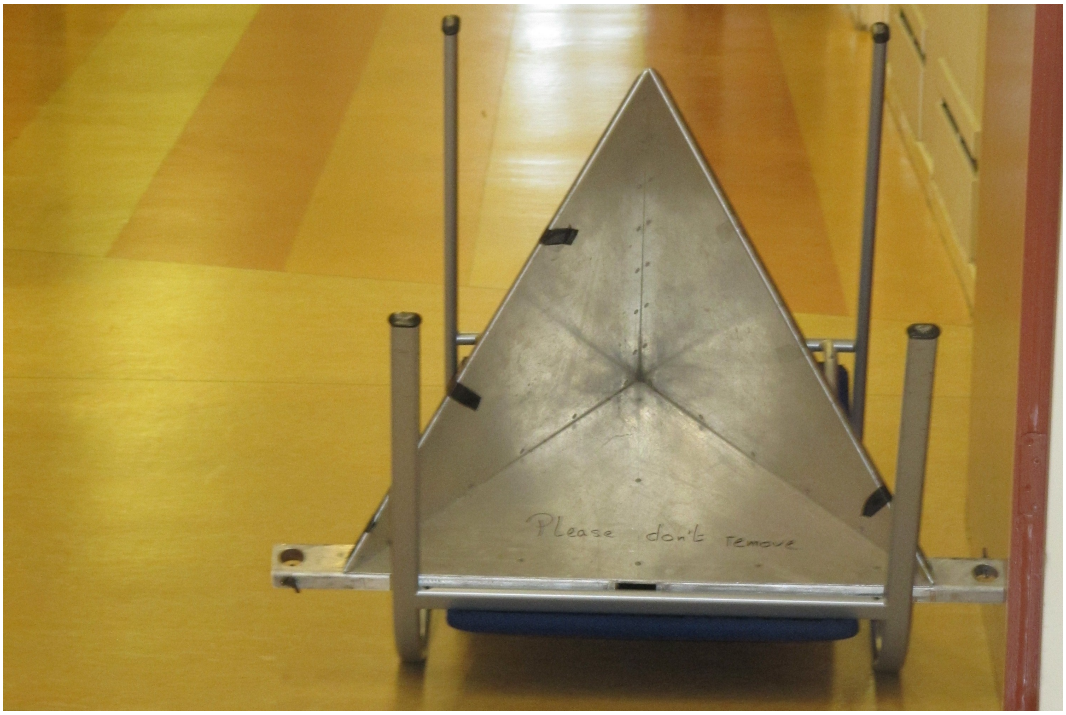


Figure E-4: Dihedral Reflector

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Acronyms

ASK	Amplitude Shift Keying
ASIC	Application Specific Integrated Circuit
AWG	Arbitrary Waveform Generators
CDMA	Code Division Multiple Access
CLIP	Component Level Intellectual Property
CW	Continuous Wave
DSP	Digital Signal Processor
DDS	Direct Digital Synthesis
DMA	Direct Memory Access
DRAM	Dynamic RAM
FPGA	Field Programmable Gated Array
FIFO	First In First Out
FlexRIO	Flexible Reconfigurable Input Output
FDMA	Frequency Division Multiple Access
FMCW	Frequency Modulated Continuous Wave
FSK	Frequency Shift Keying
IP	Intellectual Property
IF	Intermediate Frequency
LFM	Linear Frequency Modulation
LO	Local Oscillator
MMIC	Monolithic Microwave Integrated Circuits
MIMO	Multiple Input Multiple Output
OCXO	Oven-Controlled Crystal Oscillator
OFDM	Orthogonal Frequency Division Multiplexing
PXI	PCI eXtensions for Instrumentation
PCI	Peripheral Component Interconnect
PLL	Phase Locked Loop
PSK	Phase Shift Keying
PRF	Pulse Repetition Frequency
PXIe	PXI Express

RADAR	Radio Detection And Ranging
RCS	Radar Cross Section
RF	Radio Frequency
RAM	Random Access Memory
SNR	Signal to Noise Ratio
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
TDMA	Time Division Multiple Access
VI	Virtual Instrument
VCO	Voltage Controlled Oscillators