Energy Harvesting PMIC Design for an Extended Power-Range

by

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Abstract

This work proposes an energy harvesting DC-DC converter that is able to efficiently process a wide input power range from 25 mW up to 250 mW, to charge a storage device used in Internet-of-Things (IoT) applications. An interleaved boost-converter topology with two inductors is used to divide the high currents over the two branches, in order to reduce the conduction losses in the MOSFET power switches at high input power.

A Maximum Power Point Tracking (MPPT) strategy is employed to find the optimal matching between the harvesting sensor, which in this case is a solar cell, and the input of the converter. The Maximum Power Point (MPP) is found by measuring the output current of the converter, decreasing the duty cycle of the switching power MOSFETs, and again measuring the output current to check if it increases. This process is repeated until the output current no longer increases, which is where the MPP will be. The duty-cycle pulses that control the power switches are generated by comparing a reference voltage representing the duty cycle with two sawtooth waves with a phase difference of 180 degrees generated on-chip.

Usually, for converters that handle large currents, large power switches are required to keep the on-resistance of the switches minimal such that the conduction losses do not dominate. Since the converter also needs to be able to efficiently convert smaller powers, the size of the power switches is made configurable. This is necessary since otherwise the gate-charge losses will become dominant. The total size of the segmented power switches are controlled digitally by a logic unit that calculates the expected input current using 2-bit representations of the measured output current and the two most significant bits of the 5-bit representation for the duty cycle set by the MPPT.

Schematic simulation results show a conversion efficiency of up to 92%. The proposed system is designed and simulated using 180 nm TSMC CMOS technology. The chip covers a total silicon area of 2.20 mm^2, with an active area of 1.12 mm^2.

Preface

I would like to thank the people of Nowi for giving me the opportunity to work alongside them. Everyone has been very kind, and their willingness to discuss things and help out has been very informative and motivating. A special thanks to Weichen, whom I could always contact if I had questions. Our weekly meetings were always a pleasant experience with a laugh.

I would also like to thank Wouter Serdijn, for always keeping the spirits high, encouraging me and showing me new and broader perspectives. Although our update meetings have never taken place in person (due to a global pandemic), they have always been very uplifting and motivating. I have learned a lot about electronics as well as getting to know myself a little bit better.

B.D. Meekes
Delft, August 2022

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1 Introduction

1.1. Internet-of-Things

Developments in computer processing power made it possible to analyze large amounts of data in order to find trends and optimize processes in society and all kinds of industries. The miniaturization of sensor and processing chips enabled data gathering by the Internet-of-Things (IoT) principle, where numerous sensors are connected to the net to share their data. However, for large-scale implementation of these sensors, the bottleneck seems to be the power supply to these sensor nodes. When employing large amounts of sensor nodes, changing batteries for thousands of devices every once in a while is labor-intensive and costly. Besides, the impact on the environment for discarding all these used batteries would be appalling [1, 2]. Connecting the IoT devices to the power grid would limit the spatial employability and mobility, since the device would require a wire and to always be close to a power outlet. These issues need to be resolved.

1.2. Energy Harvesting

A solution to this power-supply problem is energy harvesting (also known as energy scavenging). In energy harvesting, power is extracted from the environment to either prolong the lifetime of a battery or fully power a device. Energy can be extracted from, for example, temperature gradients, vibrations, radio-frequency electromagnetic waves and (sun)light by use of an energy harvesting device (also called a transducer). Since only relatively small amounts of energy are available from the environment, it is important that the energy is harvested as efficiently as possible. Otherwise, little energy would be left over to be consumed by the device. To assure a high efficiency, a DC-DC converter is required to interface between the transducer and a temporary energy storage unit followed by the IoT device.

Energy-Harvesting Power-Management Integrated Circuits (EH PMICs), incorporating a DC-DC converter, have been designed for low-power energy harvesting [3, 4, 5, 6]. Besides their power efficiency, a small area and low bill-of-materials (BOM) are important factors in designing these PMICs. A small area makes it possible to use energy harvesting in small devices, such as GPS tags or tiny sensor nodes. In order for the technology to become economically beneficial relative to single-use batteries, a low BOM is important.

1.3. Harvesting Power

A downside of energy harvesting is that the power supply is highly dependent on environmental conditions. Situations may occur in which ambient energy is only available for a limited amount of time. In those situations it is important that the available energy is maximally absorbed, such that enough energy is harvested to supply the device also when no ambient energy is available. That means a DC-DC Converter with a high efficiency for a relatively high input power is required. When a higher power DC-DC converter is employed in a regular sensor node, more energy will be available to the node. This means the node can send out information more frequently. This will improve the accuracy of the measured data, and will lead to better process optimization. Also, when more energy becomes available, devices consuming more power can be made battery-less and widely deployable. The possibilities will be endless!

1.4. Thesis Objective

In this work, the options of implementing a wide input power range integrated DC-DC Converter occupying little PCB area with a small BOM is explored. A DC-DC converter with Maximum Power Point Tracking is designed to be connected to a solar cell transducer. Solar cells are transducers that are capable of harvesting large amounts of power. Higher powers can also come from mechanical energy sources, but these sources often require a rectifier circuit to convert the energy from alternating current to direct current. Transducers for mechanical energy and their rectifiers will not be included in this work.

This work has been assigned by the company Nowi. Nowi has designed two energy harvesting PMICs that are highly efficient for low power operation. The NH2 chip covers a power range of up to 2 mW and their NH16 chip is able to efficiently convert up to 30 mW. The goal of this project will be to extend this power range to 250 mW, such that it covers a range from 25 mW up to 250 mW. The assumption is made that a rechargeable battery with a voltage of around 4 V is connected to the output of the converter. Also, the converter will be designed to handle an input voltage range from 0.4 V up to 4 V. The thesis objective has been formulated as can be seen below.

> *To design a DC-DC Converter that can harvest a power of up to 250 mW with an efficiency of 85%, without largely increasing the footprint on the PCB to optimally harvest the energy from a solar cell to charge a battery.*

The chip will be designed and simulated in TSMC 180nm CMOS technology.

1.5. Thesis Structure

First some literature research is done on the techniques applied in this project. These techniques are discussed in Chapter 2. The background information forms a framework for the design choices of the system. The design choices are described in Chapters 3, 4 and 5. The design of the converter core is explored in Chapter 3. The design of the Maximum Power Point Tracking with all its subsystems is described in Chapter 4. The considerations made for designing the Segmented Switches are described in Chapter 5. In Chapter 6 the simulation results are presented. The results and performance of the system is discussed in Chapter 7, where some improvements are considered as well. Chapter 8 concludes the work with an overview and the contributions this work made.

2

Background information

2.1. Photovoltaic cell energy harvesting

In solar energy harvesting, the energy from electro-magnetic waves in the form of light is converted into an electrical energy using a photovoltaic cell (PV cell). A PV cell can be fabricated from a piece of silicon. The silicon can have either a monocrystalline structure or a multicrystalline structure. The monocrystalline structure is easier for electrons to pass through resulting in a higher efficiency, however multicrystalline structures are easier and cheaper to fabricate. The current-inducing effect is realized in a P-N junction. A PV cell can either have a single P-N junction as well as multiple, increasing the width of the light spectrum (range of wavelengths) it can absorb energy from.

2.1.1. P-N Junction

A P-N Junction is realized with a positively doped piece of silicon semiconductor material (p-type) placed against a negatively doped piece of silicon semiconductor material (n-type). The p-type material has a lack of electrons compared to regular silicon, or in other words, the material has an excess of holes. The holes are considered charge carriers and are able to move freely through the silicon material. The n-type material is doped with atoms with one extra electron in their outer shell compared to regular silicon. This causes the n-type material to have an excess of electron charge carriers, that are also able to move freely through the silicon material.

At the interface of the p-type and n-type materials, the holes and electrons tend to attract one another causing them to diffuse and combine resulting in a region to arise that is called the depletion region. Since some electrons of the n-type material move to the p-type material to combine with a hole, and vice versa, the material will be depleted from its charge carriers, causing the materials to be charged. The n-type material inside the depletion region will be positively charged, and the p-type material inside the depletion region will be negatively charged. These charged materials cause an electric field to arise. After recombination of the holes and electrons inside the depletion region, there are no more free charge carriers inside the depletion region.

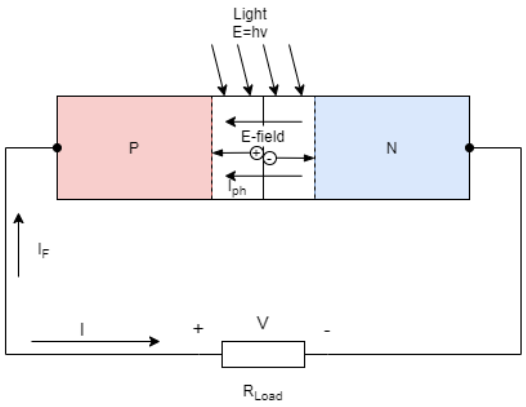


Figure 2.1: Photovoltaic cell under illumination with PN junction and connected load causing a forward biasing voltage

When light hits the PV cell in the form of a photon, the photon might hit an electron-hole pair inside the depletion region causing them to separate. Due to the electric field inside the depletion region, the electron is forced into the n-type material. Now there is an extra electron inside the n-type material that wants to recombine with the extra hole inside the p-type material. When a load is connected to the terminals of these n-type and p-type materials, a current path is formed and the electron will flow through the load to recombine with the hole. When a forward biasing voltage to the junction is generated, the depletion region will become smaller and some electrons will be able to make the jump across, causing a forward biasing current. Figure 2.1 shows a photovoltaic cell under illumination, where photons cause generation of electron-hole pairs inside the depletion region of the P-N junction. A resistive load is connected to the PV cell. The generated electrons and holes are forced to the negative and positive contact, respectively, by the electric field. Through this mechanism, a current is generated that will flow through the resistive load [7].

2.1.2. PV Cell Model

The mechanism described in previous subsection, Subsection 2.1.1, can be modeled as a current source, where the amount of current is determined by the illumination intensity, parallel to a diode (P-N junction) The contacts at the top and bottom of the PV cell introduce resistances, and together with conduction through the bulk and the diffused layer on the top, they can be translated into a series resistance. A small leakage current is unavoidable. Manufacturing defects also contribute to this leakage current. The leakage current can be represented by a shunt resistance. Figure 2.2 shows an equivalent circuit model of the PV cell [8, 9, 10].

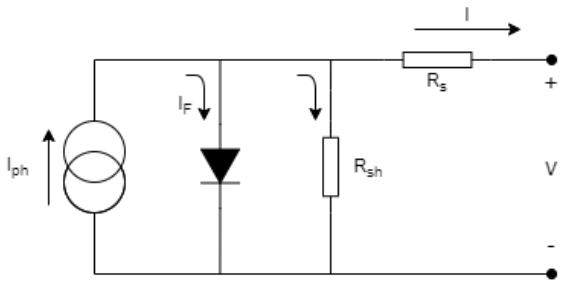


Figure 2.2: Equivalent Circuit Model of Photovoltaic Cell

Under illumination, the current versus voltage curve and power versus voltage curve look like the graphs shown in Figure 2.3. A clear maximum power point can be observed in Figure 2.3b. The voltage increases to a point where the forward bias causes the internal diode to conduct.

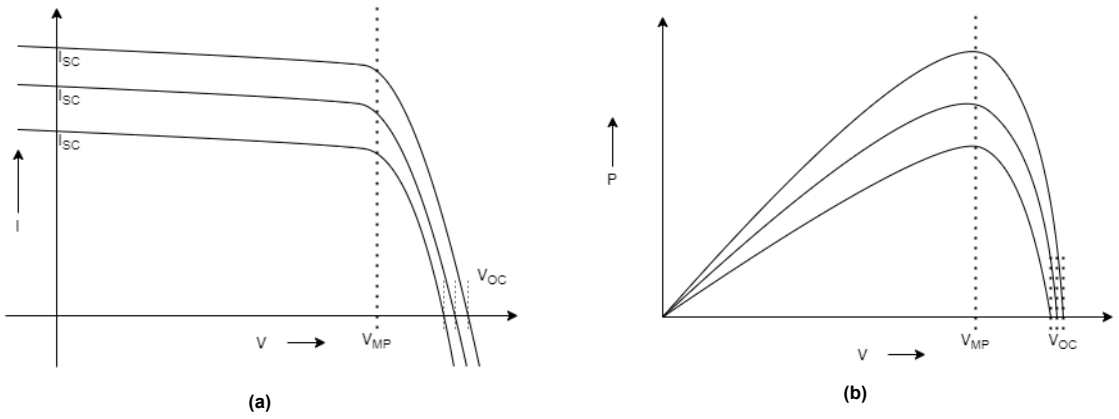


Figure 2.3: Example graphs of a Photovoltaic cell under different intensities of illumination with (a) the current plotted against voltage and (b) power plotted against voltage

Other notable points in Figure 2.3 that can be observed are the open-circuit voltage (V_{OC}) and short-circuit current (I_{SC}). The open-circuit voltage occurs at the point where no net current is flowing out the terminals of the PV cell (e.g. where the load resistance is infinite). This happens when the photocurrent is equal to the forward-biasing current. The open-circuit voltage can be calculated using Equation 2.1 [7], where V_t is the thermal voltage, I_{ph} is the photocurrent and I_S is the saturation current of the diode. When the output of the PV cell is shorted (e.g. when the load resistance is zero), the current that flows is called the short-circuit current and is purely photo-induced.

$$V_{OC} = V_t * \ln(1 + \frac{I_{ph}}{I_S}) \tag{2.1}$$

2.2. Batteries

For energy harvesting IoT applications, a battery is necessary to buffer the energy supply. Since the harvested energy is not a constant flow of energy due to environmental constraints, the battery acts as a temporary storage device. It will be charged when high amounts of energy can be harvested, and it will act as a power supply when no energy can be harvested but the connected load still requires power. One could argue that a supercapacitor can be used for this application, but the voltage across a supercapacitor will drop linearly over time when a constant current is drawn. To the contrary, a rechargeable lithium-ion battery keeps a constant voltage across its state-of-charge curve. Figure 2.4 shows the charge- and discharge curves of a Lithium-ion battery and a supercapacitor.

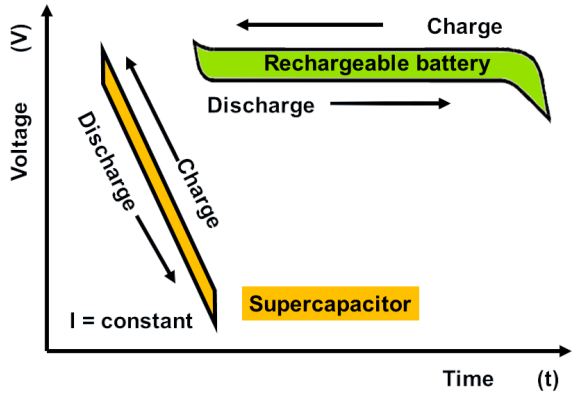


Figure 2.4: Charge- and discharge curves of a rechargeable battery and supercapacitor. From "Wikimedia Commons", by Elcap, 2013 (`https://commons.wikimedia.org/wiki/File:Charge-Discharge-Supercap-vs-Battery.png`), Licensed under CC0 1.0

A downside of the battery is that due to its chemical nature, it can not absorb infinite amounts of current in a short period of time. Especially Lithium-ion (Li-ion) batteries, of which the internal structure results in a high equivalent series resistance. High currents may cause leakages in the battery cell and will shorten its lifetime. A Li-ion battery is a convenient choice for the purpose of energy harvesting, since the technology offers a high power-to-mass density and competitive pricing, as well as remaining at a constant voltage [11]. To be able to handle large current peaks, a capacitor needs to be placed in parallel to the battery.

2.3. DC-DC Converters

The voltage of the battery is usually not the same as the voltage of the harvesting device at its maximum power point. In order to extract maximum power from the harvesting transducer, it can not be directly connected to the battery. A DC-DC converter is required to convert the voltage of the harvesting device at maximum power point to the voltage of the battery to optimally charge it. In the use case of this thesis, only limited area is available for photovoltaic cells since the design is purposed for small, possibly wearable, IoT devices. Therefore, either a single solar cell or a limited amount of solar cells will be used as a harvesting transducer. This means that the input voltage to the DC-DC converter at maximum power point will be lower than the battery voltage. A step-up converter will be required for this purpose. Three types of power converters exist for this application: Switched-Mode Power Converters that make use of an inductor, Switched-Capacitor Power Converters that make use of a capacitor, and hybrids of the two previous types that make use of both inductors as well as capacitors.

2.3.1. Capacitive Converters

Capacitors have the ability to store charge on their plates. Such a charge build-up results in an electric field between the plates, that can be interpreted as a potential difference, viz. a voltage across the capacitor. The voltage across a capacitor can not instantly change, since it requires time for the charge to redistribute. This mechanism is used in a charge pump, which is an implementation of a step-up switched capacitor DC-DC converter [12]. Equation 2.2 gives the current-voltage relation of a capacitor, that shows that the voltage across a capacitor requires time to change.

$$\frac{\delta V(t)}{\delta t} = \frac{I(t)}{C} \tag{2.2}$$

Figure 2.5 shows the two phases of a simple switched capacitor. In the first phase, the capacitor is charged up to the voltage of the input source. In the second phase, the capacitor voltage is stacked on top of the input voltage, resulting in an output voltage of two times the input voltage.

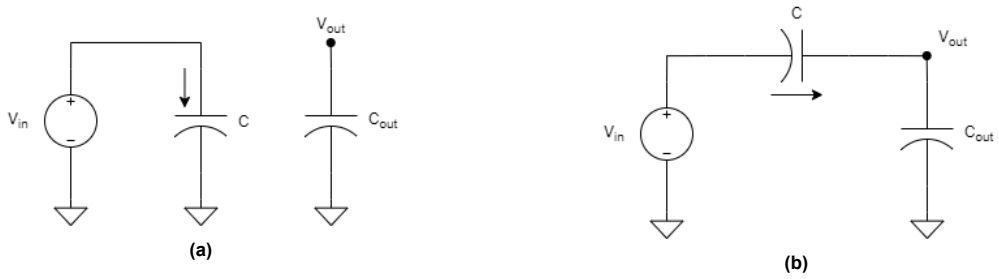


Figure 2.5: (a) Phase 1 and (b) phase 2 of a switched capacitor voltage doubler

The voltage and current as a function of time when charging a capacitor from zero volt to the voltage of a source can be described as in Equation 2.3 and 2.4, respectively. In these equations, R represents the sum of the on-resistances of the switches connecting the capacitor to the voltage source, and the parasitic equivalent series resistance of the capacitor.

$$v_c(t) = V_{in} * (1 - e^{-\frac{t}{RC}}) \tag{2.3}$$

$$i(t) = \frac{V_{in}}{R} * e^{-\frac{t}{RC}} \tag{2.4}$$

When a capacitor starts charging from zero volts, the current is high in the beginning, resulting in a high conduction loss. For that reason, it is beneficial to keep the capacitor close to completely charged when used in a converter such that a high efficiency can be realised. Unfortunately, this limits the amount of charge, and thus the amount of current, that a switched-capacitor power converter can deliver to a load while maintaining a high efficiency. This problem can be reduced by increasing the capacitor size and the switching frequency. However, there are also limits to increasing these parameters. The capacitors can be increased in size as long as the required area is available. Increasing the switching frequency will increase the corresponding switching losses, and at one point the switching losses will overtake the conduction losses. These factors make the switched capacitor converter less suitable for high power conversion.

Another downside of the switched capacitor converter is that the amount of conversion ratios is limited. The number of flying capacitors used and the number of switching phases dictate the available number of conversion ratios. According to Makowski and Maksimovic, the possible conversion ratios for a canonical switched-capacitor converter can be calculated using equation 2.5, where $P[k]$ and $Q[k]$ can be any number in the Fibonacci series for $2 \leq k \leq (N + 2)$ where N is the number of used flying capacitors [12]. Overall, switched capacitor power converters are a good choice for integrated low-power applications.

$$M = \frac{P[k]}{Q[k]} \tag{2.5}$$

The limited amount of conversion ratios reduce the matching capabilities between the converter and the harvesting transducer. Its abilities to extract power from the transducer at different maximum power points will fall short. A big upside of using capacitors over inductors is that capacitors can easily be integrated, reducing overhead cost and PCB area.

2.3.2. Inductive Converters

The inductor has the capability of storing energy in the form of a magnetic field. The voltage-current relation of the inductor (Equation 2.6) shows that when a voltage is applied to an inductor, the current through the inductor will increase linearly. This increasing current will cause an increasing magnetic field. Once there is no longer a voltage applied across the inductor, the magnetic field does not suddenly cease to exist. First, the current induced a magnetic field, now the magnetic field induces the current. Therefore, the current through an inductor is never discontinuous. This mechanism is exploited in inductive converters.

$$\frac{\delta I(t)}{\delta t} = \frac{V(t)}{L} \tag{2.6}$$

In Chapter 3, a more elaborate description on the working principles of inductive switched mode power converters is given. Unlike switched capacitor converters, inductive converters can, in theorie, achieve any conversion ratio. The easily selectable conversion ratio makes the inductive converter very suitable for maximum power point tracking and matching to the harvesting transducer. Unfortunately it can be difficult to integrate inductors, as is discussed in the next section.

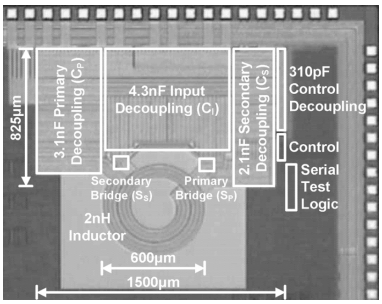
2.4. Inductors

Inductors can be realised using different techniques. The downside of using inductors is that they often are bulky and can be expensive. For that reason, research is done in making inductors smaller and integrateable. The difficulty in integrating inductors lies in the fact that only small traces can be used to form the inductor, as well as that there is only a limited amount of degrees of freedom available for designing an integrated inductor. Due to the relatively narrow traces on silicon, integrated inductors inherently have a high parasitic equivalent series resistance that dissipates energy and reduces the efficiency. At high frequencies, the equivalent series resistance goes up even further due to the skin effect as a result of self-induced eddy currents. The ratio between inductance and equivalent series resistance is called the quality factor, or Q factor. To ensure a high Q factor, inductors often turn out to be bulky and impact the bill-of-materials and required PCB area. Some different implementations of integrated inductors are described in the next section.

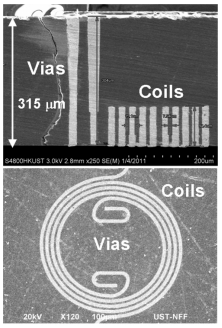
2.4.1. Integrated Inductors

The basic form of integrating an inductor is realised by creating, for example, a spiral using the top metal layers on the chip. This type is also called a Planar Spiral Inductor, as described by Mohan et al. [13] and Yue and Wong [14]. The metal layers have a limited thickness, and the available chip area limits the width of the spiral traces. These factors do not allow for a low resistive path. Also, a limited amount of turns can be made, since such an inductor should not be placed above active circuitry on the silicon because magnetic field lines from the inductor might disturb the active circuitry, and only limited chip area is available. Also, when the inductor is placed above highly-doped low-ohmic substrate material, a current is induced in the substrate by capacitive coupling between the traces and the substrate, as well as eddy currents induced by the magnetic field generated by the inductor [15]. These substrate currents contribute to the conduction losses and thus the reduction of the quality factor of the integrated inductor. Tricks can be used to increase the total inductance by stacking two spiral inductors in the two top metal layers to exploit the mutual inductance. Wibben en Harjani were able to fabricate a 2nH inductor with a series resistance of 500mΩ (Figure 2.6a) [16]. In Wu (2012) [17], a copper spiral was embedded in the bottom layer of the silicon substrate to achieve an inductance of 3.4nH and a series resistance of 350mΩ (Figure 2.6b). Another strategy for improving integrated inductors is implementing a coil inductor with a magnetic core to enhance the inductance (Figure 2.6c) [18].

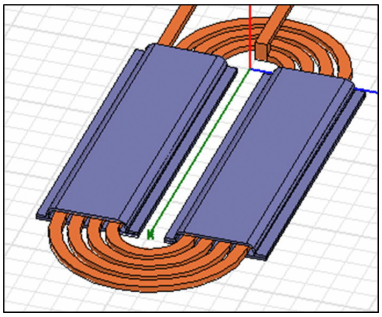
Besides integrating the inductor on the chip, the inductor can also be integrated off-chip but inside the package using bonding wires. The bonding wires are much thicker than on-chip metal traces, reducing the parasitic equivalent series resistance, Wens et al. realized a 18nH bondwire inductor with a series resistance of 1Ω, to implement a boost converter with maximum output power of 150mW and a maximum power efficiency of 63% (Figure 2.6d) [19]. Villar Pique et al. managed to manufacture a bondwire inductor with an inductance of 26.7nH and an equivalent series resistance of 1.08Ω (Figure 2.6e) [20].



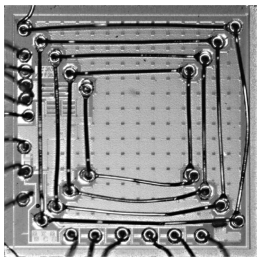
(a) On-chip planar spiral inductor [16]



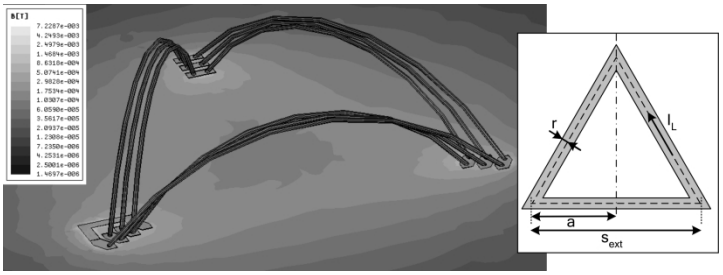
(b) Silicon-embedded coreless inductor [17]



(c) Electroplated magnetic yokes inductor [18]



(d) Bondwire spiral inductor [19]



(e) Bondwire triangular spiral inductor [20]

Figure 2.6: Integrated inductor implementations

2.4.2. External Inductors

The TSMC technology that is available for this project is, unfortunately, not compliant with integrated inductors. Therefore, the options of using external inductors are explored as well.

Thin and Thick film inductors are both planar inductors placed on a ceramic base. The thin film inductor has a thickness of up to 0.1um, while the thick film inductor is about a thousand times thicker. Thin film inductors can be manufactured with high precision, so they can be made small which also results in a high series resistance. Thick film inductors are a little less precise, but have a lower series resistance. Figure 2.7 shows a picture of a film-type inductor from manufacturer MuRata [21]. The high precision of the thin-film inductor make it suitable for the use in impedance matching circuits for high frequency applications.

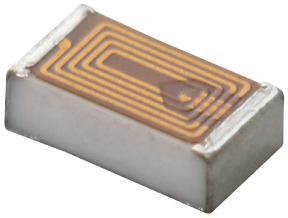


Figure 2.7: Thin film inductor. From ”Murata Manufacturing Co., Ltd.” (https://www.murata.com/products/productdetail?partno=LQP18MN5N6C02%23) [21]

Multiple ceramic layers and coil conductors can be placed on top one another to create a multilayer type inductor. Multilayer inductors make a good balance between inductance, maximum current, size and cost. Figure 2.8 shows an image of multilayer inductor from manufacturer MuRata [22].

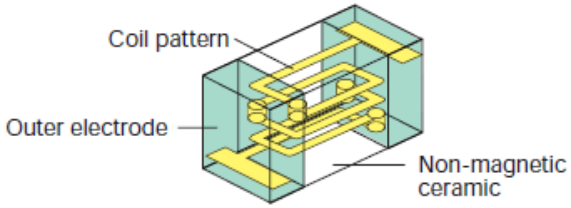


Figure 2.8: Multilayer inductor. From ”Murata Manufacturing Co., Ltd.” (https://article.murata.com/en-eu/article/basic-facts-about-inductors-lesson-2) [22]

Another type of inductor can be created by winding a wire around a ceramic core as in Figure 2.9 to form a coil. The wire can be made with a thickness of choice, making it possible to have a small equivalent series resistance and support large currents. A high Q factor can be realized. These features make the wirewound inductor the best choice for the application of a DC-DC power converter.

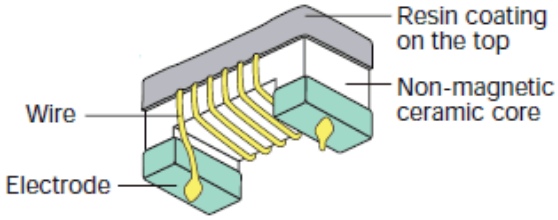


Figure 2.9: Wire wound inductor. From ”Murata Manufacturing Co., Ltd.” (https://article.murata.com/en-eu/article/basic-facts-about-inductors-lesson-2) [22]

2.5. Maximum Power Point Tracking

The available energy in the environment is always changing and thus never constant. For a solar cell, the solar light intensity fluctuates, or maybe a cloud flies over and the light gets blocked. The light intensity translates to a certain voltage at the terminals of the solar cell, with a certain optimal current flowing out. This optimum is called the Maximum Power Point (MPP).

The maximum power point of a PV cell was described in Section 2.1.2. A PV cell at a constant maximum power point can be modeled as a voltage source with a series resistance. The voltage source value is twice the PV cell output voltage. The series resistance determines the current and thus the available power at that power point. The maximum power of this model can be extracted when the load resistance is equal to the series resistance of the model. Different techniques can be used to maximize the energy supply to the load of the converter, which in this case is the charging of a battery.

A first technique is the use of a light sensor to measure the environmental light intensity. This information is then used to configure the converter to maximum power point settings. This technique requires an extra sensor than can not be integrated since it needs to be exposed to light, adding on to the BOM. Also, the sensor is of different size and location than the PV cell, so in case of partial shading, the sensor will not give a representative result. The sensor and PV cell will also age differently, resulting in worsening of accuracy over time. The sensor will also consume power by itself.

Another technique is to measure either the open-circuit voltage or the short-circuit current (or both) and determine a constant parameter that linearly scales the open-circuit voltage and/or the short-circuit current to the maximum power point voltage and current, respectively [23]. The linear relation is only an approximation of the actual MPP values. Therefore, this technique can lack in accuracy when the conditions deviate from standard environmental conditions. Also, when measuring the open-circuit voltage or the short-circuit current, the converter and load will need to be detached for a short period of time to accurately measure. This will reduce the time during which harvesting is enabled, and available energy is possibly missed out on.

The Hill-climbing technique is a more accurate method to reach the maximum power point setting. In this technique, a control parameter of the converter is either increased or decreased in steps. After each step a measurement is done to check if the perturbation led to an increase in power. If so, the next step is done until the maximum power point is reached. This technique is independent of the type of PV cell that is used. Also, aging will not impact the accuracy of the maximum power point tracking. It might occur that the overhead of the Hill-climbing technique overshadows the harvested energy, since the technique requires to keep track of the control parameter as well as the output measurement value. In that case, a more simple MPPT technique is preferred.

3

System Design

3.1. Boost Converter

In Subsection 2.3.2, it was described that the energy-storage capabilities of an inductor can be exploited to boost a voltage to a different voltage in the form of a DC-DC converter. Figure 3.1 shows the two phases of such a switched-mode boost converter. In Phase 1, as seen in Figure 3.1a, the voltage across the inductor is equal to V_{in}. The converter is in Phase 1 for a certain amount of time, referred to as the on-time t_{on}. Figure 3.1b shows Phase 2 of the boost converter. The voltage across the inductor is equal to $V_{out} - V_{in}$, and the inductor is in Phase 2 during the off-phase with a duration of t_{off}. The Volt-Second method can be used to describe the functionality of the boost converter. The volt-second method is based on the steady-state principle, which states that the average voltage across the inductor must be zero in order to be stable, since otherwise the current would increase infinitely.

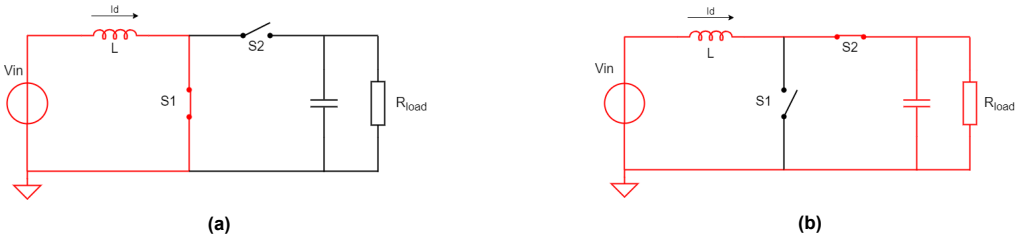


Figure 3.1: (a) Phase 1 and (b) Phase 2 of the boost converter

As per the volt-second method, the average voltage over one cycle must equal zero. A relation between input- and output voltage can then be deduced as in Equation 3.4, where $T = t_{on} + t_{off}$. In steady-state operation every cycle is the same, so the on-time and off-time of the circuit can be translated in terms of a duty cycle D, as seen in Equation 3.5. The duty cycle can be defined as the percentage of time that the circuit is 'on', meaning being switched to Phase 1 as in Figure 3.1a. This means that the duty cycle ranges from 0 to 1, and t_{off} can be defined as $1 - D$ as in Figure 3.1b. The relation in Equation 3.5 is also referred to as the Voltage Conversion Ratio (VCR).

$$\overline{V_L} \cdot T = 0 \tag{3.1}$$

$$V_{in} \cdot t_{on} + (V_{in} - V_{out}) \cdot t_{off} = 0 \tag{3.2}$$

$$V_{in} \cdot t_{on} = (V_{out} - V_{in}) \cdot t_{off} \tag{3.3}$$

$$\frac{V_{out}}{V_{in}} = \frac{T}{t_{off}} \tag{3.4}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{3.5}$$

An input-output relation can also be deduced from the current-voltage relation of the inductor in both states. Using Equation 2.6, the current increase due to the applied voltage during time t_{on} is calculated as in Equation 3.6. The inductor-current ripple due to the applied voltage during Phase 2 can be calculated as in Equation 3.7. For steady-state operation, the calculated current differences in the two phases are equal to each other and the same relation as in Equation 3.5 is found.

$$\Delta I_1 = \frac{V_{in}}{L} t_{on} = \frac{V_{in}}{L} T_s D \tag{3.6}$$

$$\Delta I_2 = \frac{V_{out} - V_{in}}{L} t_{off} = \frac{V_{out} - V_{in}}{L} T_s (1 - D) \tag{3.7}$$

When considering only ideal components, the input power is equal to the output power. Using that equality, an expression for the average input and output current can be deduced using the expression for the Voltage Conversion Ratio as can be seen in Equation 3.10.

$$V_{in} \cdot I_{in} = V_{out} \cdot I_{out} \tag{3.8}$$

$$\frac{I_{in}}{I_{out}} = \frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{3.9}$$

$$\frac{I_{out}}{I_{in}} = 1 - D \tag{3.10}$$

In the case of this project, in which a battery is connected to the output of the converter and a PV cell is connected to the input, the output voltage is set by the battery and the input current is set by the PV cell. Then, the duty cycle can be used to set the voltage conversion ratio to adjust to the optimal input voltage. The average output current is then a function of the average input current and the chosen duty cycle. As can be seen from Equation 3.6 and 3.7, the ripple current is also dependent on the time (t_{on} and t_{off}). When a duty cycle is used to set the VCR, but the ripple current needs to be decreased, the period time can be reduced. The on-time and off-time will then also be shorter. Decreasing the period time is done by increasing the switching frequency and reducing Phases 1 and 2 proportionally. Also, increasing the inductance reduces the ripple current. Since increasing the inductance also increases the required area and price, the inductance can only be increased to some extent.

The intended maximum output power of the converter in this project is 250 mW as described in Chapter 1. This means that at an output voltage of 4 volts the average output current will be 62.5 mA, and at an input voltage of 0.4 volts the average input current will be 625 mA. The average input current is determined by the PV cell and the impedance matching of the PV cell output to the converter input. Figure 3.2 shows a graph of the inductor current at various average current levels.

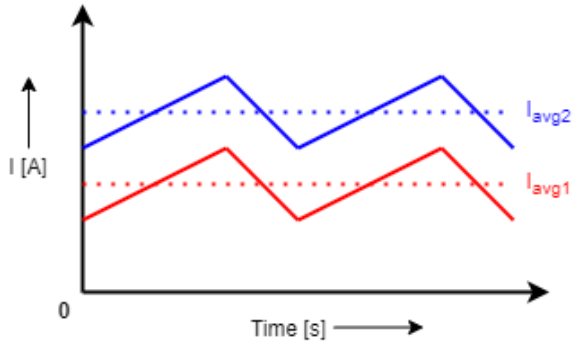


Figure 3.2: Inductor current with two different average levels

The switches seen in Figure 3.1 are implemented using MOSFETs, which are non-ideal components with a finite on-resistance and a parasitic gate capacitance. Also, real-world inductors have an equivalent series resistance. These non-idealities result in losses that decrease the efficiency. The conduction

loss and gate-charge loss are the largest contributors of the total loss and are discussed in Subsections 3.1.1 and 3.1.2, respectively.

3.1.1. Conduction Losses

Conduction losses are caused by currents going through resistive elements in the circuit. These parasitic effects cause dissipation of energy resulting in a reduction of efficiency. Conduction losses are most prominent when the boost converter is operating at high power, and thus conducting high currents. Figure 3.3 shows the circuit of the boost converter with added models of the parasitic resistive elements causing conduction losses during the two phases.

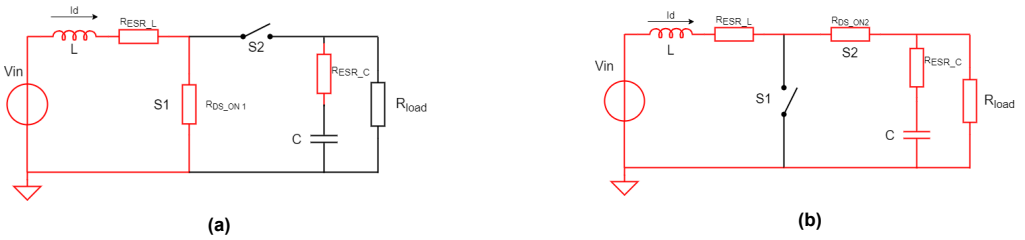


Figure 3.3: (a) Phase 1 and (b) Phase 2 of the boost converter with resistive elements causing conduction loss

The power dissipation caused by the parasitic resistances can be split up in a DC component and an AC component. The DC component shows the dissipation due to the average current level. The AC component demonstrates the power loss due to the ripple current that comes with the operation of the boost converter. The power loss caused by the average DC current can be calculatead using Equation 3.11 for Phase 1 and Equation 3.12 for Phase 2, which are deduced from Joule's law combined with Ohm's law: $P = I^2 \cdot R$.

$$P_{avg1} = I_{avg}^2 \cdot (R_{ESRL} + R_{DS\_ON1}) \cdot D_{on} \tag{3.11}$$

$$P_{avg2} = I_{avg}^2 \cdot (R_{ESRL} + R_{DS\_ON2}) \cdot D_{off} \tag{3.12}$$

In Equations 3.6 and 3.7, the ripple current was calculated. From these, it can be seen that the ripple can be influenced by choosing the inductance and switching frequency. A higher switching frequency will result in a shorter on-time, which in turn will result in a smaller ripple. When determining the power consumption due to the ripple current, the root-mean-square (RMS) of the ripple current must be considered. The RMS represents the value of the DC current that would result in the same power dissipation in a resistive load. The RMS of the ripple current can be calculated using Equation 3.13. For a periodic triangle waveform, Equation 3.13 can be simplified to Equation 3.14.

$$I_{rms} = \sqrt{\frac{1}{T_2 - T_1} \int_{T_1}^{T_2} I^2 \, dt} \tag{3.13}$$

$$I_{rip\_rms} = \frac{I_{rip}}{2\sqrt{3}} \tag{3.14}$$

The power loss caused by the ripple current can be calculated using Equations 3.15 and 3.16, for Phase 1 and Phase 2, respectively.

$$P_{rip1} = (I_{rip})_{rms}^2 \cdot (R_{ESRL} + R_{DS\_ON1}) \cdot D_{on} \tag{3.15}$$

$$P_{rip2} = (I_{rip})_{rms}^2 \cdot (R_{ESRL} + R_{DS\_ON2}) \cdot D_{off} \tag{3.16}$$

Important to note from Equations 3.11, 3.12, 3.15 and 3.16, is that the conduction loss is quadratically dependent on the current, so a linear increase in current will result in a quadratic growth of conduction loss. This is important to keep in mind, since the converter designed in this project requires conversion

of a relatively high current. Equations 3.11, 3.12, 3.15 and 3.16 also show the influence of parasitic series resistances. The current is going through the inductor at all times. Therefore, it is important to choose an inductor with a small ESR. Also the on-resistance of the power switches are of great importance. When a MOSFET is used as a switch, it operates in the linear region. The on-resistance of the MOSFET is then proportional to the length of the gate, and inversely proportional to the width of the gate. This means a wider gate reduces the on-resistance and thus the conduction loss.

The output capacitor also exhibits a parasitic series resistance. The output capacitor absorbs the current peaks in Phase 2, and supplies the output with the average current in Phase 1. Fortunately, the equivalent series resistance of an external capacitor is often much smaller than the inductor equivalent series resistance.

3.1.2. Switching Losses

The physical structure of the integrated MOSFET is accompanied by parasitic capacitances between the gate and the source, the drain and the channel, as seen in Figure 3.4. The capacitances between the gate and source and drain are mainly caused by a slight overlap of the gate and the source and drain contacts.

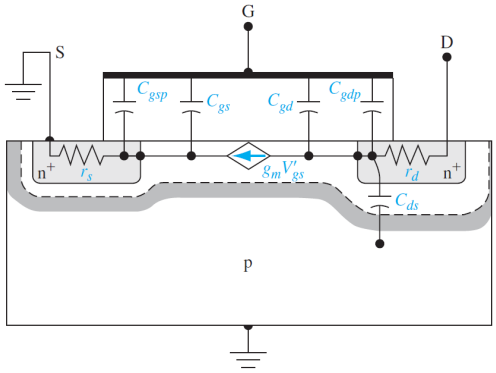


Figure 3.4: Inherent resistances and capacitances in the n-channel MOSFET structure. From ”Semiconductor Physics And Devices”, by Donald A. Neamen, McGraw-Hill, 2011, p. 423 [7]

In order to turn on the switch, these gate capacitances need to be charged first. This requires a small amount of time and a small amount of current. The larger these gate capacitances, the more current and/or time is required to switch the MOSFET.

Since the gate capacitance is mainly formed by the gate overlapping the source and the drain, when increasing the width of the gate, the overlapping area is then also increased by that same width. Therefore, the gate capacitance increases linearly with the width of the MOSFET. This also linearly increases the amount of charge required to charge the capacitance up to a certain voltage, since $Q = C \cdot V$. The gate length is kept constant at a minimum, to keep the on-resistance low.

To determine the power loss due to charging and discharging the gate, first the energy it takes to charge the gate must be determined, as in Equation 3.17. Here, the gate is switched to a voltage of V_g. The value Q represents the amount of charge required to charge the gate. This value for Q can be determined by integrating the current that flows into the gate during the switching-on of the MOSFET. The power loss of the gate due to parasitic capacitances can then be determined by multiplying the energy used per switch by the switching frequency f_s, as in Equation 3.18. Thus, the gate-charge loss is linearly dependent on the switching frequency and the width of the MOSFET.

$$E_{gate} = Q \cdot V_g \tag{3.17}$$

$$P_{gate} = E_{gate} \cdot f_s = Q \cdot V_g \cdot f_s \tag{3.18}$$

3.1.3. Other Losses

Apart from the conduction loss and switching loss, there are also a few other contributors to the overall power loss. For example, when the transition of the switch occurs, it does not happen instantly. The gate voltage starts rising to the high voltage and at a certain point in that process where it approaches the threshold voltage, the switch starts conducting current. At that moment the voltage across the drain and source of the switch is still high. Therefore dissipation will occur at the transition. Figure 3.5 shows an example of an N-type MOSFET falling-edge transition. The power loss during transitions per period can be calculated by integrating the product of the drain-source voltage and the drain current during the transition of both the falling edge and the rising edge, as in Equation 3.19 where t_1 and t_2 are the start and end time of the rising-edge transition and t_3 and t_4 are the start and end time of the falling-edge transition.

$$P_{trans} = \frac{1}{T}\left[\int_{t_1}^{t_2} V_{DS}(t) \cdot I_D(t)\, dt + \int_{t_3}^{t_4} V_{DS}(t) \cdot I_D(t)\, dt\right] \tag{3.19}$$

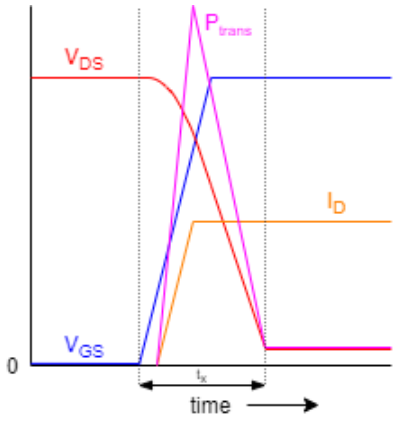


Figure 3.5: Falling-edge transition of N-type MOSFET

The loss during a transition can be minimized by realizing fast switching such that the transition is equally fast. This can be done by designing proper driving circuits that balance the speed versus the power consumption due to extra gate-charge loss. Gate drivers are further discussed in Section 5.1.

To prevent a short-circuit current when the two power switches are accidentally turned on at the same time, a dead time is introduced. This dead time allows the one switch to completely turn off before the other switch is turned on. If this dead time is omitted, a short-circuit current will drain the battery attached to the output of the converter. This will of course cause power loss, but also risk the circuit of being damaged due to possible extreme current peaks. Another risk arises when introducing dead time. The inductor possibly causes a large voltage build-up since it cannot stop conducting current instantaneously. Therefore, a diode is placed parallel to the high-side power switch. When the voltage rises above the forward-voltage during the dead time, the diode will start conducting and prevent high voltage peaks that can possibly break the circuit. When this diode is conducting, power is dissipated. For that reason, the dead time should be chosen properly to allow for non-overlapping switching, but not be too long to cause unnecessary conduction loss in the diode. The conduction loss in the diode, also called dead time-loss, can be calculated using Equation 3.20 where V_D is the diode forward bias voltage.

$$P_{dead} = V_D \cdot I_L \cdot t_{dead} \cdot f_s \tag{3.20}$$

Apart from the fundamental circuit of the boost converter, there is also some control circuitry required to regulate the converter with proper switching etcetera. The power consumed by this overhead circuitry will be at the expense of the overall power efficiency. Therefore, it is important to keep a low power

consumption in mind at all times when designing the overhead circuitry. The circuits that compose this overhead are described in Chapters 4 and 5.

In conclusion, the conduction loss and the gate-charge loss of the power switches are the largest contributors to the total power loss. The conduction loss in the power switch can be reduced by increasing the width of the switch. But by increasing the width the gate-charge loss will increase. Therefore, an optimum can be found for the best width of the power switch for a specific set of input and output voltage and current values.

3.1.4. Continuous- versus Discontinuous Conduction Mode

In Section 3.1, a relation between the output and input voltages of the boost converter was deduced. This expression is however only valid in Continuous Conduction Mode or CCM. The boost converter operates in CCM when the average inductor current is larger than half the current ripple, such that the ripple does not cause the inductor current to go below zero. When the inductor current reaches zero before the end of the period, the boost converter goes into Discontinuous Conduction Mode, or DCM. DCM allows for a lower average current, which is beneficial for low-power boost converters that need to maintain a certain output voltage. Also, DCM requires a much more complicated control since the switching cycle consists of three different states. For this project, the transfer of power through the converter is important. For these reasons, the converter in this project will be operated in CCM. Figure 3.6 shows the inductor current of a boost converter operating at the border of CCM and DCM.

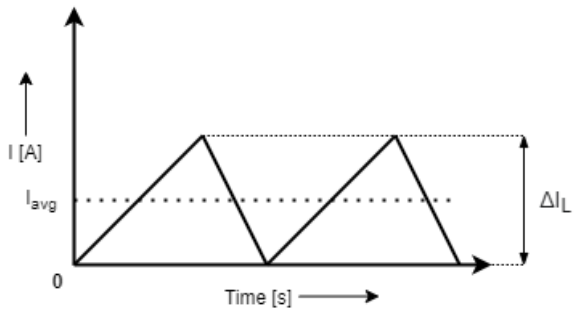


Figure 3.6: Inductor current at the boundary between CCM and DCM

To ensure that the converter operates in CCM, half the ripple current must be smaller than the average inductor current. As seen in Equations 3.6 and 3.7, the ripple current can be minimized by increasing the switching frequency and increasing the inductance. An expression can be deduced for the minimum inductance value for a specific switching frequency and input current, as in Equation 3.24. The expression can be rewritten to find a value for the minimum switching frequency when the inductance and input current are set, as in Equation 3.25. Both expressions are to be a function of output voltage, since the output voltage is set by the connected battery, and a function of average input current, which is limited by the short-circuit current of the PV cell, Here it is assumed that the converter is lossless.

$$I_{in\_avg} \geq \frac{\Delta I_L}{2} \tag{3.21}$$

$$I_{in\_avg} \geq \frac{V_{in}}{2L} \cdot T_s \cdot D \tag{3.22}$$

$$I_{in\_avg} \geq \frac{V_o}{2L} \cdot T_s \cdot D(1-D) \tag{3.23}$$

$$L \geq \frac{T_s V_o D(1-D)}{2I_{in\_avg}} \tag{3.24}$$

$$T_s \leq \frac{2LI_{in\_avg}}{V_o D(1-D)} \tag{3.25}$$

3.2. Interleaved Boost Converter

Since the specifications from Chapter 1 describe a high power with an accompanying high current, the conduction losses due to these high currents will form a dominant part of the total power loss. Therefore, the implementation of an Interleaved Boost Converter is explored. In an interleaved boost converter the average input current is equally divided over two or more branches with separate inductors, to reduce the I^2R losses. In this project, two inductor branches are implemented as in Figure 3.7. Both inductor branches have their own two power switches, configured in a similar manner as in a single inductor boost converter. The switching of an individual branch will be of the same nature as the boost converter. However the switching signals of the two branches will have a 180 degree phase difference. The duty cycle of the switching signals for the two branches need to be equal. The interleaved switching results in a reduction of the ripple current when the input currents are summed together, as well as a reduction in ripple of the output currents of the two branches when summed. Figure 3.8a shows the total input current with a reduced ripple for a duty cycle of 75% and the currents through the individual branches and inductors that have a phase difference of 180 degrees. The frequency of the summed ripple current is double the individual inductor current ripple frequency. When the duty cycle is 50%, the ripple current is even completely cancelled out, as seen in figure 3.8b

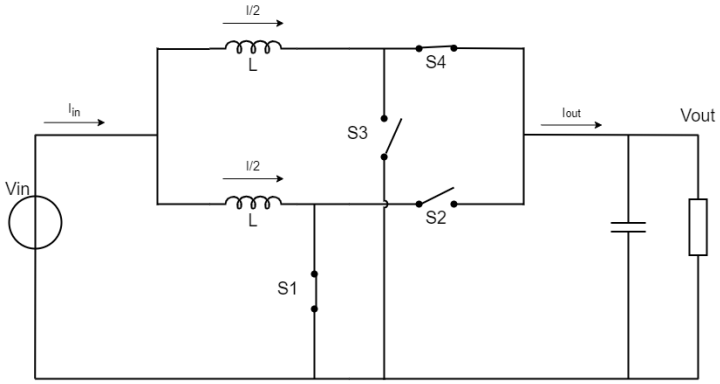


Figure 3.7: Interleaved Boost Converter with two inductor branches

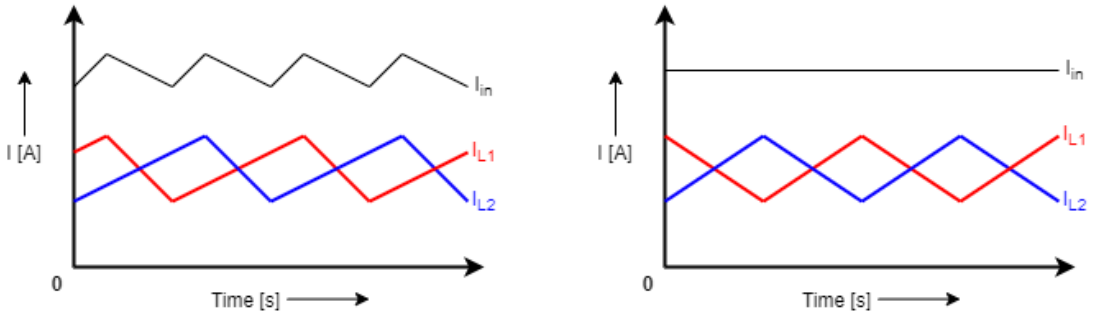


Figure 3.8: Ripple currents through separate branches and total input current for a duty cycle of (a) 75% and (b) 50%

Since the input voltages and output voltages are equal for both branches, the Voltage Conversion Ratio can be calculated in the same way as for the regular boost converter using the volt-second method seen in Equations 3.1 to 3.5, assuming lossless components. The same is valid for the total input and output current, as long as the duty cycle is equal for both branches. The average inductor current per branch, however, is calculated as in Equation 3.26. It can be deduced that $I_{in} = I_{L1} + I_{L2}$, which also follows from Kirchhoff's Current Law.

$$I_{L1\_avg} = I_{L2\_avg} = \frac{I_{in\_avg}}{2} \tag{3.26}$$

The conduction loss in an interleaved boost converter can be calculated using Equations 3.11, 3.12, 3.15 and 3.16. For the interleaved converter, the average current is halved but twice as many switches and inductors are required including their contributions to the conduction loss due to their resistances. From Figure 3.7, Switches 1 and 3 are to be considered low-side switches (Lo), and Switches 2 and 4 are will be regarded as high-side switches (Hi). Equation 3.27 shows the expression for the conduction loss in the Interleaved boost converter due to the power switch on-resistances and inductor equivalent series resistances. The current ripple I_{rip} can be calculated as in Equations 3.6 and 3.7.

$$P_{cond} = 2 \cdot \left[\left(\frac{I_{in\_avg}}{2} \right)^2 + \left(\frac{I_{rip}}{2\sqrt{3}} \right)^2 \right] \cdot [R_{onL} D + R_{onH}(1-D) + R_{ESRL}] \tag{3.27}$$

An expression for the gate-charge loss is given in Equation 3.28, where Q is the charge required to switch a single gate. The factor 4 stems from that there are four power switches present in the circuit.

$$P_{gate} = 4 \cdot Q \cdot V_g \cdot f_s \tag{3.28}$$

Because the average current through the two branches is smaller, the width of the individual power switches can be reduced. The reduced width allows for a faster switching frequency. This faster switching frequency is also beneficial to maintain operation in Continuous Conduction Mode. The CCM must be monitored carefully in the interleaved boost converter, since the average inductor current is halved. This means that there is less headroom available for the ripple current. The expressions for ensuring CCM by choosing either the inductance or switching frequency from Subsection 3.1.4 can be rewritten to be applied to the interleaved boost converter, as is done in Equations 3.29 to 3.33.

$$I_{L\_avg} = \frac{I_{in\_avg}}{2} \geq \frac{\Delta I_L}{2} \tag{3.29}$$

$$I_{in\_avg} \geq \frac{V_{in}}{L} T_s D \tag{3.30}$$

$$I_{in\_avg} \geq \frac{V_o}{L} T_s D(1-D) \tag{3.31}$$

$$L \geq \frac{T_s V_o D(1-D)}{I_{in\_avg}} \tag{3.32}$$

$$T_s \leq \frac{L I_{in\_avg}}{V_o D(1-D)} \tag{3.33}$$

Equation 3.32 and 3.33 can also be rewritten to be only dependent on the target output power at a certain voltage as seen in Equations 3.34 and 3.35. This can be done by using the current input/output relation of the boost converter, which can also be applied to the interleaved boost converter: $I_{out\_avg} = I_{in\_avg}(1-D)$. This calculation that only depends on output parameters is convenient when, for example, a device will be connected to the output that requires a certain fixed power and CCM needs to be ensured for all duty cycles.

$$L \geq \frac{T_s V_o D(1-D)^2}{I_{out\_avg}} \tag{3.34}$$

$$T_s \leq \frac{L I_{out\_avg}}{V_o D(1-D)^2} \tag{3.35}$$

An investigation of commercially available (external) inductors was done. The search properties that were considered as high priority are inductance, ESR, saturation current, geometrical dimensions and price. A selection of suitable inductors is shown in Table 3.1. From the table, inductor Number 6 was selected for inspection because of its high inductance-to-ESR ratio.

Table 3.1: Shortlist of commercially available inductors

#	Name	Brand	Type	Inductance	ESR	Sat. Current	Dims. LxBxH	Price
1	TYA2016101R0M-10	Laird	Wirewound	1 uH	95 $m\Omega$	3300 mA	2x1.6x1.15mm	0.13
2	LPWI201610H1R0T	Littelfuse	Thin Film	1 uH	45 $m\Omega$	3900 mA	2x1.6x1mm	0.54
3	TFM201608ALC-1R0MTCA	TDK	Thin Film	1 uH	66 $m\Omega$	2500 mA	2x1.6x0.8mm	0.43
4	DFE201610E-1R5M=P2	Murata	Wirewound	1.5 uH	91 $m\Omega$	2900 mA	2x1.6x1mm	0.32
5	IHHP0806AZER1R0M01	Vishnay/Dale	Choke	1 uH	58 $m\Omega$	3340 mA	2x1.6x1.2mm	0.36
6	LSEPC2016KKT2R2M	Taiyo Yuden	Wirewound	2.2 uH	90 $m\Omega$	2600 mA	2x1.6x1mm	0.35
7	DFE201612E-4R7M=P2	Murata	Wirewound	4.7 uH	252 $m\Omega$	1800 mA	2x1.6x1.2mm	0.31

For an inductor of 2.2μH, an output voltage of 4V, an average total input current of 625mA (since the input voltage is 0.4V and the input power is 250mW), and a duty cycle of 0.9 (with an input voltage of 0.4V, using Eq. 3.5) the minimum switching frequency is calculated using Equation 3.33 to obtain a value as in Equation 3.36

$$f_s \geq \frac{V_o D(1-D)}{L I_{in\_avg}} = 261.8 \text{ kHz} \tag{3.36}$$

A target switching frequency of 1 MHz was selected for the design. This frequency of 1 MHz allows for some current ripple headroom, to accommodate for different duty cycles and input levels.

3.3. System Overview

Figure 3.9 shows a diagram of the proposed system. The system incorporates the interleaved boost converter topology that is controlled by the maximum power point tracking block. The segmented power switches extend the power range at which the converter can operate efficiently.

In the coming chapters the detailed design and implementation of the Maximum Power Point Tracking circuit and Segmented Power Switches will be described (Chapters 4 and 5, respectively).

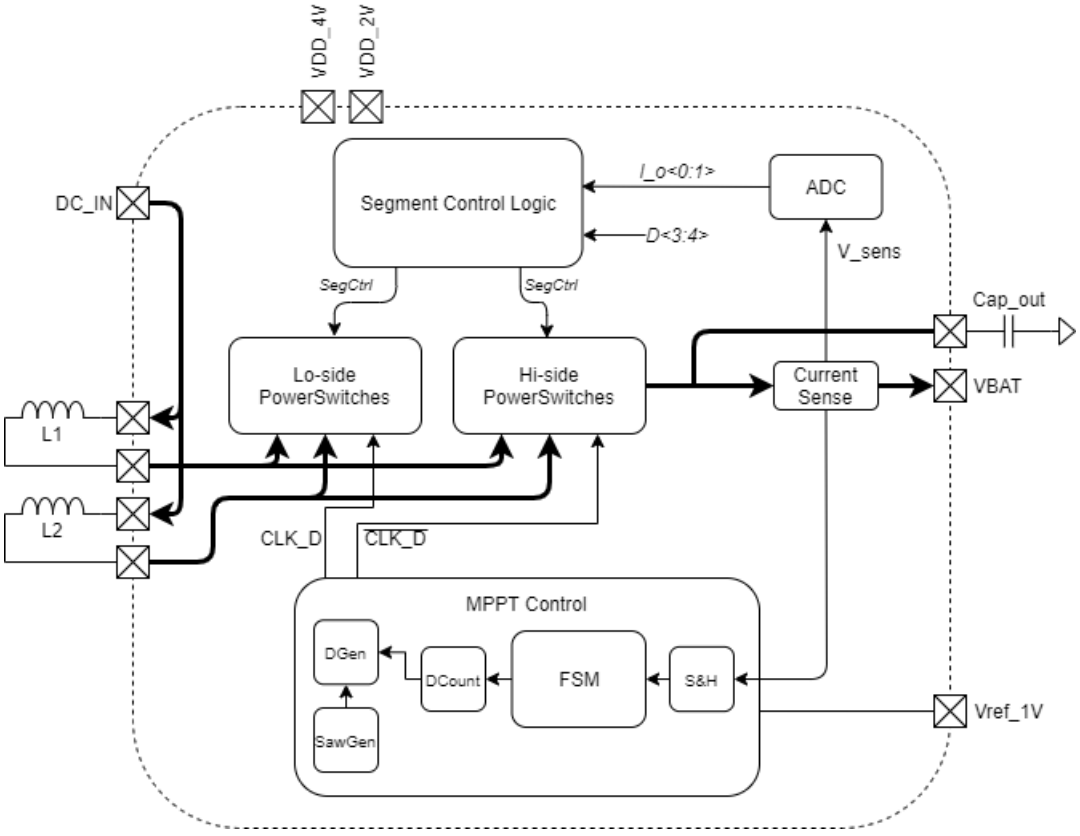


Figure 3.9: System overview

4

Maximum Power Point Tracking Design

Maximum Power Point Tracking is an essential part in energy harvesting to ensure that the maximum amount of energy is extracted from the transducer. As stated before in Chapter 2, the maximum power point of a photovoltaic cell does not occur at a constant voltage and current, as the light intensity may change over time. An algorithm can be employed to find the maximum power point. A battery is connected to the output of the converter. This battery can be interpreted as a voltage source, by which the voltage is fixed. Therefore, the output current can be observed as a representation of the output power [24]. In boost converters and interleaved boost converters, the voltage conversion ratio is set by the duty cycle of the PWM signal controlling the power switches. The duty cycle can be used as a control parameter to find the optimum conversion ratio to maximize the output current, and thus the output power.

Figure 4.1 shows the design overview of the MPPT system with its seven subsystems. These seven subsystems will be described in this chapter.

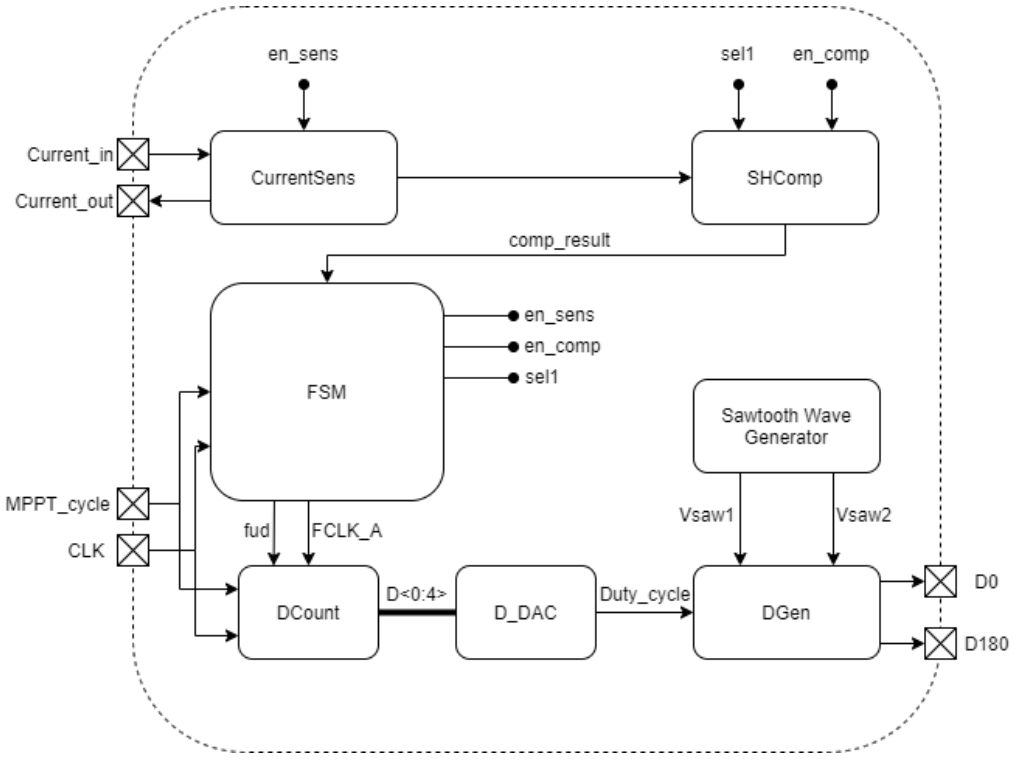


Figure 4.1: Design overview of MPPT system

4.1. Finite-State Machine

A finite-state machine (FSM) controls all the subblocks in the MPPT block. The NH2 FSM block from Nowi is used in this MPPT implementation. Using logic gates all the enable and select signals are generated. A timing diagram of the FSM and its signals is shown in Figure 4.2. The FSM cycle is triggered by the $mppt\_cycle$ bit. Then the Current Sensor is enabled. The output current is measured and converted into a voltage. Thereafter this voltage is loaded onto one of the capacitors of the SHComp block. There is one clock cycle of time available to load the capacitor. The output of the SHComp block is read out by the FSM and it acts accordingly. If the output is higher than the previously measured value, the output to the duty-cycle counter is raised and a new measurement is taken to check whether the current also increases. The FSM keeps checking whether the current has increased. When the current increase stagnates, the 'gear' bit is set, and the cycle of checking the change in current is repeated. If the measured current again has not increased, the maximum power point is reached and the MPPT cycle is completed.

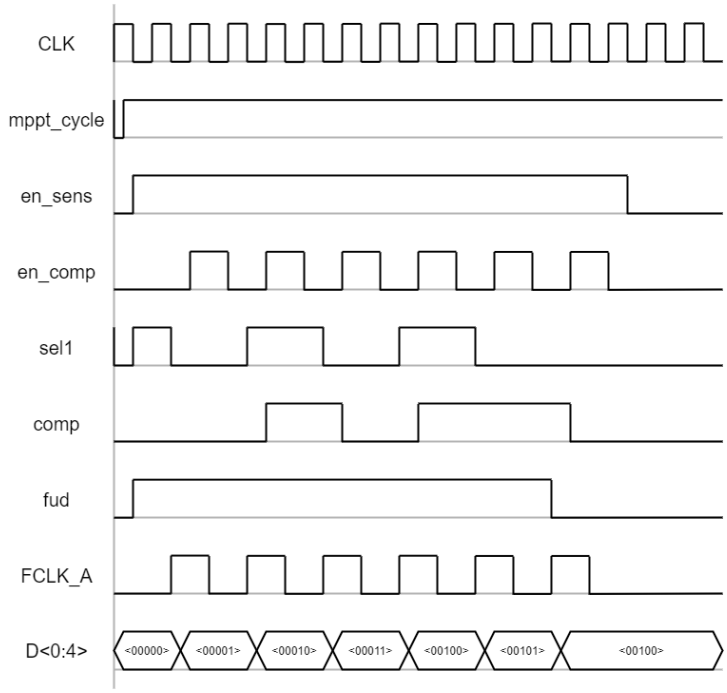


Figure 4.2: MPPT Finite-State Machine timing diagram

The frequency of a MPPT cycle can be related to the physical world. A solar cell is used as the harvesting source. Ideally when the light intensity changes, a new MPPT cycle is started. When a stationary solar cell is used, the light intensity changes when for example a cloud blows over. When a wearable solar cell is used, the light intensity might change when the person moves. It is assumed that the person does not make fast motions, meaning that the angle of the solar cell will not change faster than once per second. So the period of the MPPT cycle is set to 1 second (1 Hz).

The NH2 FSM is designed to operate at a clock frequency of 1 kHz. This results in a period time of 1 millisecond. This means that all the subblocks need to have a response time of less than 1 ms.

4.2. Output Current Measurement

The output current is measured to determine whether the maximum power point is reached. The output current is copied and scaled down using a PMOS current mirror and converted into a voltage using a resistor as shown in Figure 4.3. The amplifier ensures that the drain-source voltages of the measuring PMOS devices are equalized, such that the current scaling is only dependent on the widths of the PMOS devices since the lengths are the same. The current is scaled down to minimize conduction losses from the resistor and current mirror. The current can not be scaled down infinitesimally, since the output of the Current Measurement block needs to be able to drive the input of the Sample-and-Hold block that is connected to the output. This means that the output current of the Current Measurement block needs to charge and discharge the sampling capacitor in the available time. When the MPPT cycle is finished, the measuring block is bypassed through a large PMOS device. The bypass PMOS is sized rather large such that there is little conduction loss and voltage drop across the device for a maximum current of 70 mA. Figure 4.4 shows the simulation result of the Current Sensing block. A step-wise increasing input current is applied to the sensing block. The output voltage as well as its corresponding input current are plotted in the graph. The first and last input current steps are outside the input range designed for.

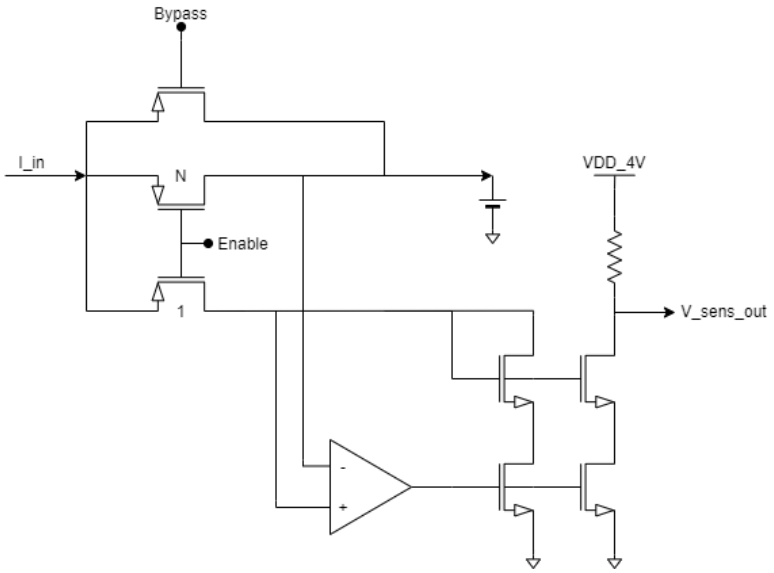


Figure 4.3: Current measurement circuit

Current-Sensor Amplifier

The amplifier in the current-sensing block equalizes the source-drain voltages of the PMOS devices. The drain voltage of the power line is set by the battery it is connected to. Therefore the drain of the scale-down PMOS is controlled by the amplifier. The inputs of the amplifier will always be close to the supply voltage. Therefore, an NMOS input pair is used in a folded cascode topology (Figure 4.5). The amplifier requires a bandwidth of 1 kHz. The design of the amplifier is based on the design of the Nowi NH16 MPPT Analog block.

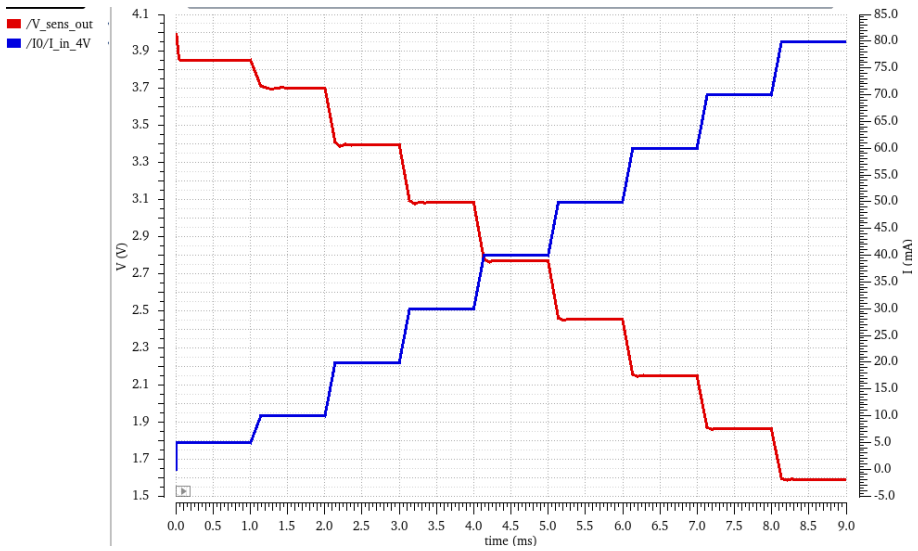


Figure 4.4: Current Sensor Simulation Result; output voltage (red) at step-wise increasing input current (blue)

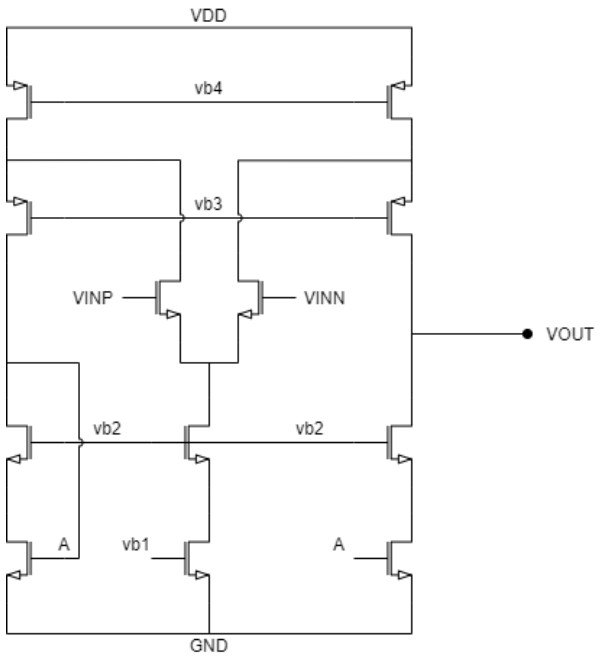


Figure 4.5: NMOS input pair folded cascode amplifier

4.3. Sample-and-Hold Comparison

Once the output current of the converter is translated into a voltage, that voltage value needs to be sampled and stored in order for it to be compared to a subsequent value. This functionality is carried out by the Sample-and-Hold Comparator block shown in Figure 4.6. The FSM selects which capacitor is used to store the measured current on by toggling the *Sel* input. After a voltage is stored, the *Sel* bit is flipped and the next value is stored onto the second capacitor. Then the comparator is activated and the voltages on the capacitor are compared. If the voltage on the second capacitor is greater than the first voltage, the FSM continues. The FSM keeps track of what measurement is stored on which capacitor, and thus how to interpret the comparator output value.

The size of the MOSFETs in the conduction path between Vin and the capacitors determines how much current can flow onto the capacitor and thus how fast the capacitor can be charged. This limits

the maximum clock speed. The output of the Current Sensor block needs to be able to supply this maximum current. A PMOST and NMOST are placed in parallel to implement a transmission gate to accommodate for different voltage levels at the source and drain of the MOSFETs.

The Sample-and-Hold Comparator block is implemented by the Nowi NH2 SHComp block. A selection bit coming from the FSM controls which transmission gate is activated. To prevent charge redistribution from one sampling capacitor onto the other, a non-overlapping clock generator is used. The non-overlapping signals are level shifted from 2 volts to 4 volts to switch the transmission gates.

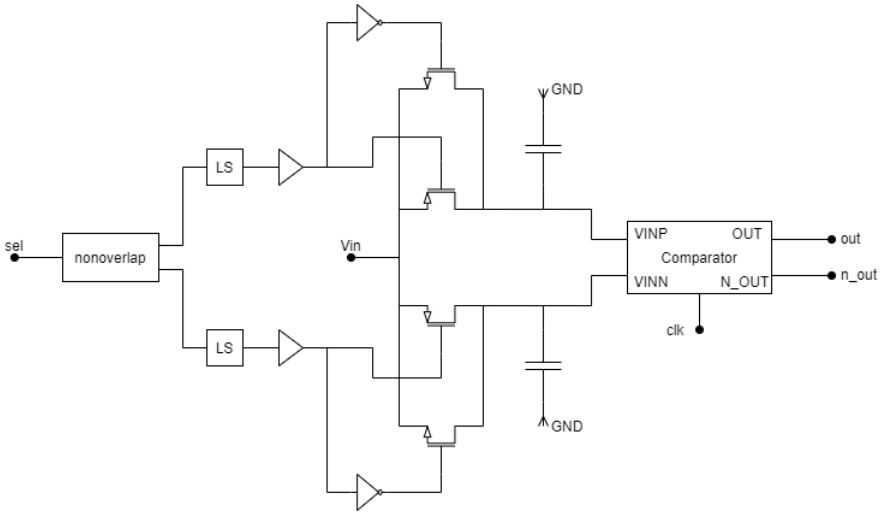


Figure 4.6: Sample-and-hold Capacitors connected to a comparator

4.4. Duty Cycle Counter

The Duty Cycle Counter stores and keeps track of the state of the duty cycle. At the start of every MPPT cycle, the counter is reset to zero. This reset is important since otherwise the MPPT cycle would start from the previous count, which may be already past the Maximum Power Point and the algorithm fails. During the MPPT cycle, the FSM toggles the counter to go up once every clock cycle. Once the maximum power point is crossed, the FSM triggers the counter to count down by one and settle on the count resulting in the maximum power point.

The Counter is implemented using five JK Flip Flops. JK Flip Flops have the functionality to toggle the output when both *J* and *K* inputs are high. The number of JK Flip Flops used determines the number of bits available to binary represent the Duty Cycle, and thus the resolution of the Duty Cycle as well as the number of conversion ratios. Five bits enable 32 different conversion ratios with a resolution of 3.125% of the Full Scale. Reducing the resolution further down will impose strain on the Duty Cycle Generator in its outer operating regions, as will be discussed in more detail in Section 4.6.

The Duty Cycle Counter includes a short-pulse generator, of which its pulse is sent to the clock ports of the Flip Flops. The necessity of this pulse generator is discussed in the next subsection.

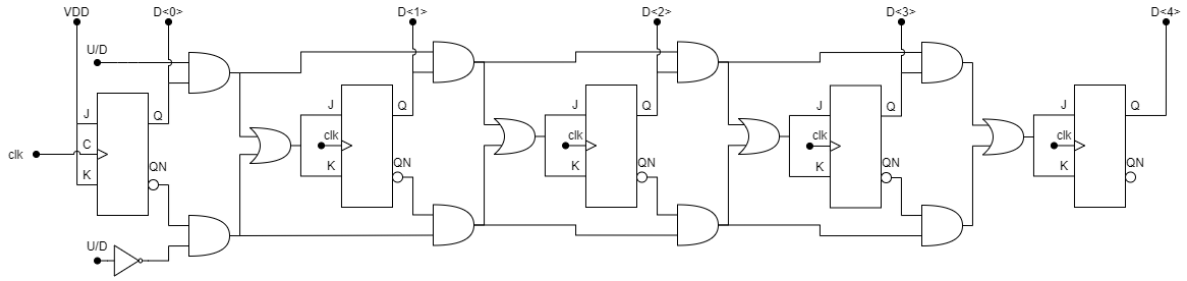


Figure 4.7: 5 Bit Up-/Down Counter using JK Flip Flops

JK Flip Flop

As described in the previous section, the counter is implemented using JK Flip Flops. The big up-side of a JK Flip Flop is that its output toggles when both inputs are high. This functionality makes them suitable for use in a counter, where for every cycle the count needs to go up or down by one. For a regular JK Flip Flop (Figure 4.8), however, the output is not stable when the inputs are high (including the clock). For example, let's assume that the starting condition of a regular JK Flip Flop is $J = K =$*'1'*, $Q =$*'1'* and $Q_n =$*'0'*. Then, when the clock goes high, all the inputs to the bottom NAND-gate are high, resulting in its output going from '1' to '0'. This will also cause the second low-side NAND-gate to switch, resulting in the second high-side NAND-gate to switch as well. Both the outputs of the second NAND-gates go to their opposite input NAND-gate, causing an oscillation when the clock stays high. This phenomenon is called 'racing'.

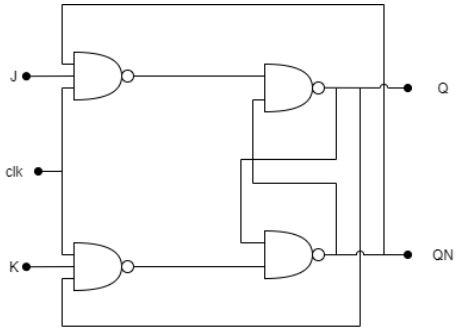


Figure 4.8: Regular JK Flip Flop

A suitable solution to this problem is the Master-Slave topology shown in Figure 4.9. In this topology, when the clock goes high, the outputs of the master part are toggled, but not directly fed back to its inputs. Instead, the outputs are presented to the slave part, waiting for the clock signal to go low again. At that point, the slave processes its inputs to the output, which then also go back to the input of the master. Since the clock is not high again at that moment, the state of both master and slave are stable.

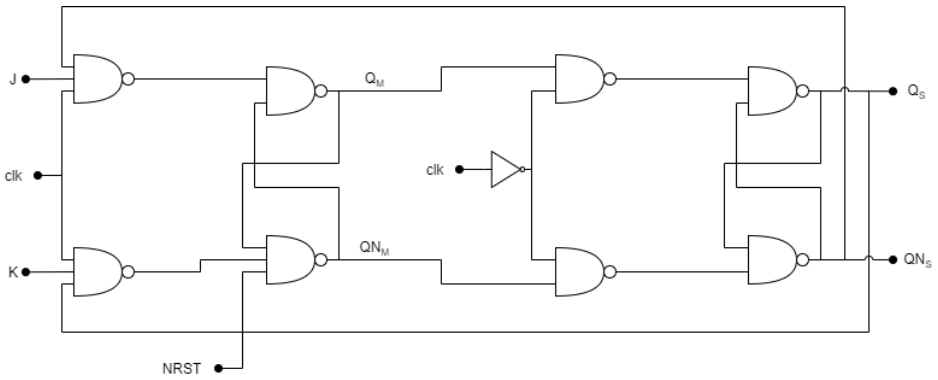


Figure 4.9: Master-Slave JK Flip Flop

A pulse generator was mentioned in Section 4.4. The input of the pulse generator is connected to a clock signal obtained from the FSM. This clock signal has a width of 1 ms. The rising edge will trigger the Master part of the flip flop to transfer the result to its output and present it to the input of the Slave part. The falling edge will trigger the Slave part to compile its result and present the final output result. Figure 4.10 shows a timing diagram of the functioning of the Master-Slave JK Flip Flip controlled by a regular clock signal. If the clock signal from the FSM were to be directly connected to the Master-Slave JK Flip Flop, the result of the toggle would appear at the output after 1 ms. This would be much too slow. In fact, the result should ideally appear at the output immediately. This is where the pulse generator comes in. A pulse is generated at the rising edge of the clock signal coming from the FSM. After a short amount of time, set by an RC-circuit, the pulse goes low. In this manner, the result appearing at the output can be controlled to occur in time and hold its state until the next FSM clock rising edge. Figure 4.11 shows the circuit implementation of the pulse generator.

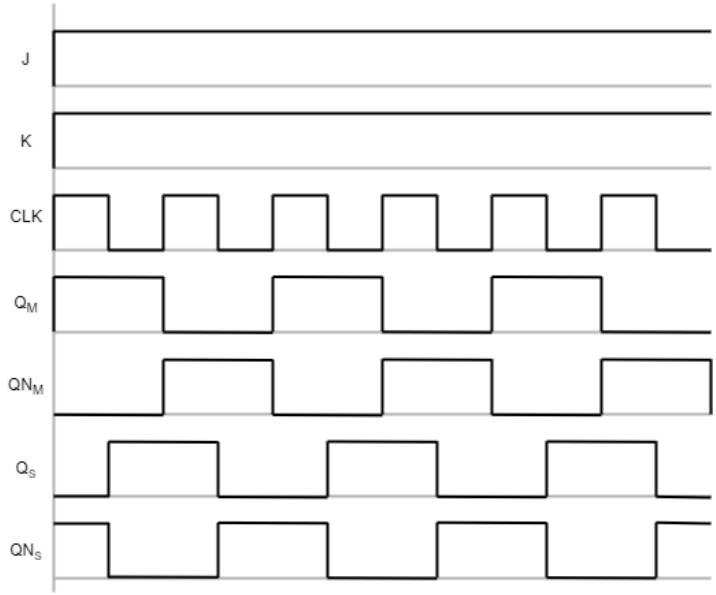


Figure 4.10: Timing diagram of the Master-Slave JK Flip Flop

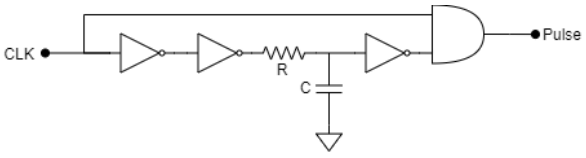


Figure 4.11: Pulse generator to trigger the JKFFs

4.5. Duty-Cycle Digital-to-Analog Converter

As described in the previous section, the duty-cycle counter will output a 5-bit binary code. This code needs to be converted into a voltage that later on can be used to generate a pulse-width modulated signal. A digital-to-analog converter (DAC) is used for this purpose. The output of the DAC will have a voltage range of 0 to 1 volt with a least-significant bit (LSB) of 31.3 mV. The DAC is implemented by a R-2R ladder topology as seen in the circuit diagram of Figure 4.12. The resistor nodes are either connected to ground or to the reference voltage of 1 volt. The switches are controlled by the bits coming from the counter, where the least significant bit controls the leftmost switch and the most significant bit controls the rightmost switch. The upside of the R-2R DAC is that it is easily implementable, the output amplifier always sees the same impedance independent of the input code, and that the output is a voltage, which is required for the following step of the MPPT cycle.

The switches of the DAC are implemented with inverter structures, where the source of the PMOS device is connected to the reference voltage and the source of the NMOS device is connected to ground. The drains of the PMOS and NMOS devices connect to the resistor node. The gates are driven by the counter output. It must be noted that there is an inversion happening at this point. This means that the counter is able to reset to zero and count up, with the effect of starting at the highest duty cycle and going down to the MPP. The MPPT algorithm is required to start at the highest duty cycle to make sure that there is no accidental current being drawn from the battery back into the converter, which would result in unnecessary power consumption. Also, the MPPT would be unreliable since it is not designed for current flowing into the opposite direction. A low duty cycle will also result in a small voltage conversion ratio, meaning that the input voltage will be high. The input voltage may then be higher than the open-circuit voltage of the photovoltaic cell causing the internal diode to conduct and create an internal short, drawing current from the converter and battery.

A buffer is added to the output of the DAC.

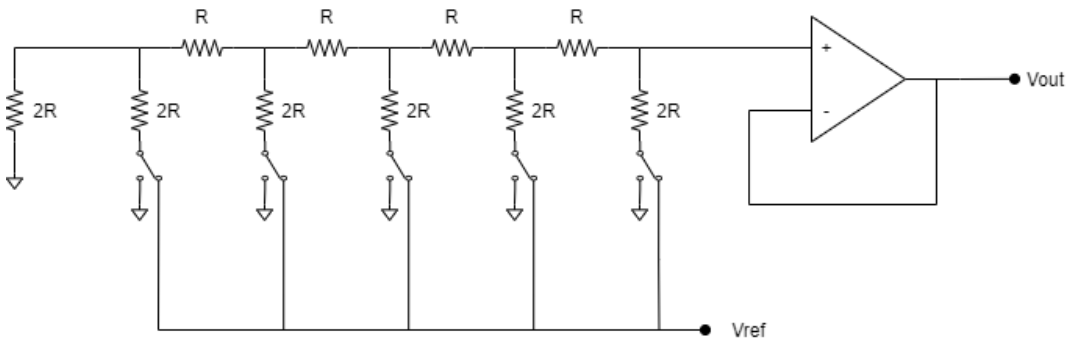


Figure 4.12: R-2R Digital-to-Analog Converter

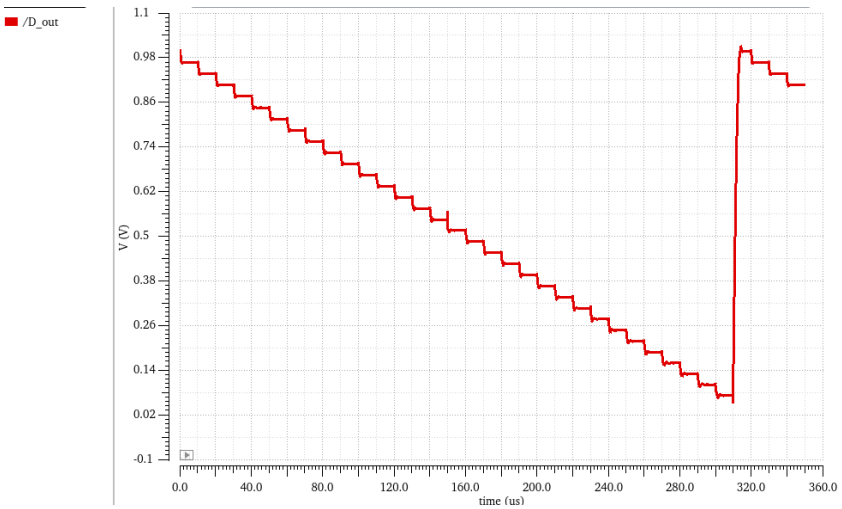


Figure 4.13: The DACs output voltage representing the intended duty cycle, coming from the Counter's 5-bit code

4.6. Duty-Cycle Pulse Generator

The duty-cycle generator uses a pulse-width modulation technique that generates a pulse-wave with a duty cycle according to the information that it is given by the duty-cycle counter.

The generator compares the duty-cycle signal to a saw-tooth wave. A triangular wave could also be used to be compared to. The choice for a saw-tooth wave is further explored in Section 4.7. The output of this comparator is high when the duty-cycle voltage is higher than the saw-tooth. When the saw-tooth crosses the duty-cycle voltage, the comparator output goes low. This way a square wave is generated at the frequency of the saw-tooth wave. Since an interleaved boost converter is realized, two square waves need to be generated with the same duty cycle and frequency, but with a phase shift of 180 degrees. Therefore, two comparators are required. The phase difference of the square wave is realized by feeding two different saw-tooth waves into the different comparators with a phase difference of 180 degrees. Figure 4.14 shows the circuit diagram of such a generator.

The saw-tooth waves have a voltage swing of 1 volt peak-to-peak. The signal V_D will also range from 0 to 1 volt. Since these voltages are somewhat low, and can reach below the threshold voltage of NMOS transistors, the input-pair of the comparator must be PMOS. The generated PWM signals will go via a level shifter to the power switches and will have peak-to-peak voltages of 2 volts and 4 volts after level-shifting. The level shifters ensure fast edges. The propagation delay of the comparators is not of much importance in this circuit, as long as the propagation delay is approximately the same for the rising-edge and the falling-edge. The equal propagation delays on both edges result in a phase shift of the PWM signal, but has no impact on the duty cycle itself.

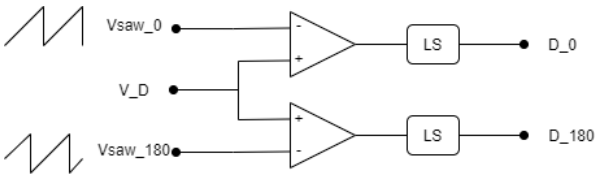


Figure 4.14: Duty Cycle PWM Generator

Figure 4.15 shows a transient simulation result of both PWM output signals. The duty-cycle values are scaled to a range between 0 to 1 and are plotted against the input voltage containing the intended duty-cycle information in the form of a voltage between 0 and 1 volt. The ideal output would look like a linear line where, for example, an input voltage of 250mV corresponds to a duty cycle of 25%, an input voltage of 500mV corresponds to a duty cycle of 50%, an input voltage of 750mV corresponds to a duty cycle of 75%, etcetera. It can be seen from the transient simulation result that at both ends of the duty cycle lines, the result deviates from the linear line. This shows that both the highest duty cycles, larger than 90%, and the lowest duty cycles, smaller than 10%, are difficult to generate accurately. This can be caused by the limited speed of the comparator; there is not enough time available to settle to the intended output value before the next edge arrives. Also, a small offset can be perceived. This offset is caused by non-idealities in the sawtooth waves presented to the inputs of the comparators. The cause of this problem will be further discussed in Subsection 4.7.1.

The outputs of the Duty-cycle Generator are sent to two non-overlapping clock units.

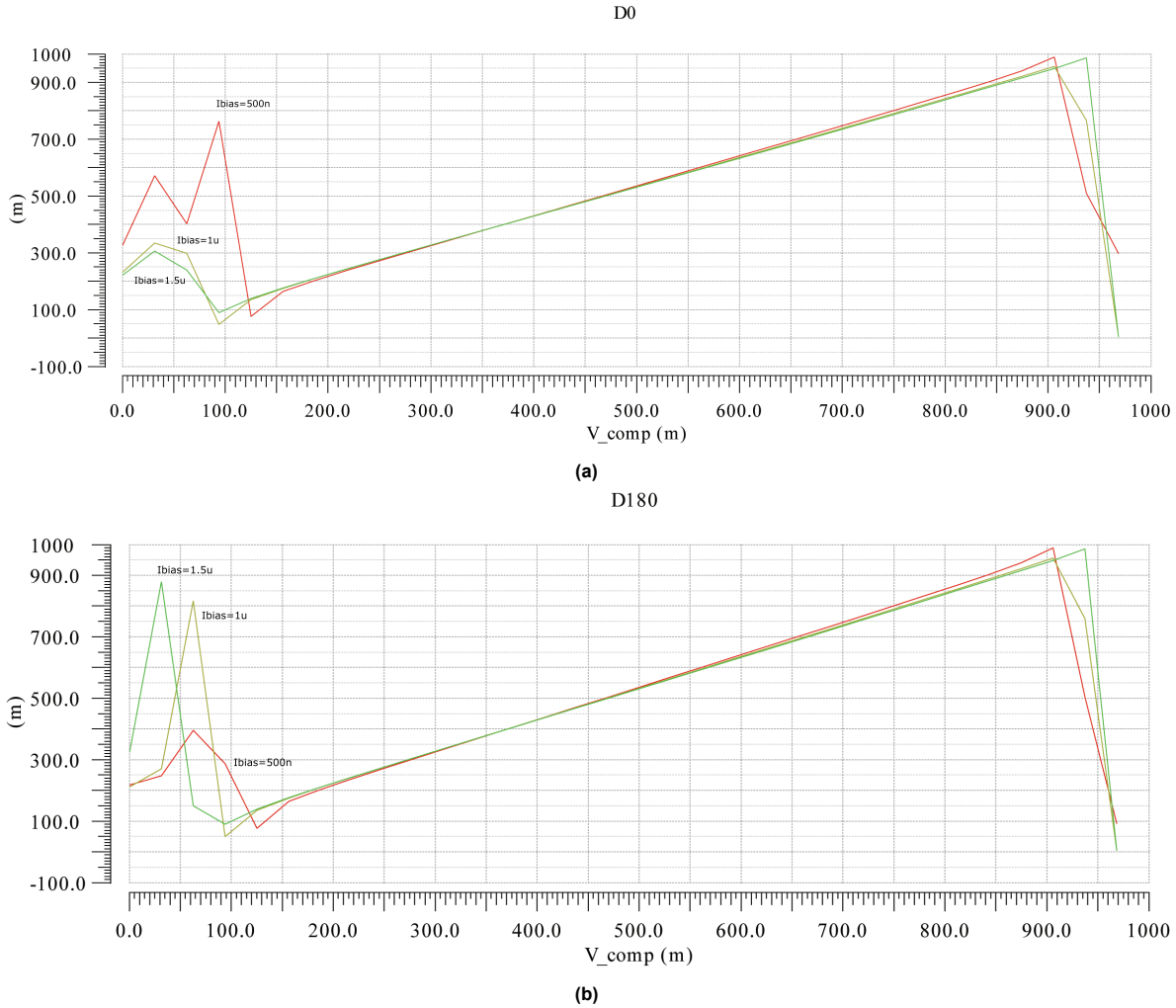


Figure 4.15: Duty-cycle Generator results with (a) Zero phase shifted duty cycle versus input voltage for three biasing currents (500nA (red), 1uA (yellow) and 1.5uA (green)) and (b) 180 degrees shifted duty cycle versus input voltage for three biasing currents (500nA (red), 1uA (yellow) and 1.5uA (green))

4.7. Sawtooth Wave Generator

The sawtooth wave generator produces the sawtooth waves that go into the duty-cycle generator comparators to produce the control signals for the power switches. For the application of an interleaved boost-converter topology, two sawtooth waves with a phase difference of 180 degrees are required. The design of the wave generator is based on the principle of a relaxation oscillator [25, 26, 27].

A current is applied to a capacitor such that the voltage across the capacitor increases. When the capacitor voltage reaches a reference voltage (both voltages are connected to the inputs of a comparator), the comparator flips and sends a signal that the capacitor needs to be discharged. This signal needs to be kept high during the time required to fully discharge the capacitor. Therefore, a delay element is introduced such that a short pulse is generated which controls the switch that discharges the capacitor. This switch also needs to be wide enough to be able to handle the current required for quickly discharging the capacitor.

An extra capacitor is used to generate the second sawtooth wave. This second capacitor will be discharged when the first sawtooth wave crosses half its peak voltage. Ideally, this moment occurs at the halfway point of the first sawtooth wave cycle, and thus reset the second sawtooth wave at a 180 degree phase shift.

The amplitude of the sawtooth wave is determined by the reference voltage to which the capacitor voltage is compared. An external reference voltage of 1 volt is available from an external supply via a dedicated pin. Two large resistors of equal size are used to form a voltage divider to generate another voltage of half the external reference voltage. The first capacitor voltage will be compared to the 1 volt reference voltage, thus setting the peak voltage of the sawtooth wave to 1 volt. The second capacitor is reset when the first capacitor voltage crosses 0.5 volts, giving it a 180 degree phase shift but also a peak voltage of 1 volt since there is equal time to charge the second capacitor. At the chip startup, it might take a small amount of time for the comparators to reach their correct biasing points. It might occur that the main capacitors of the wave generators charge beyond 1 volt before the comparators are fully operational, causing the generator to get stuck and refrain from oscillating. For this reason, an external reset function was added in the form of an OR-gate to trigger a discharge of the wave generators' main capacitors at startup. This reset pin is connected to the $mppt\_cycle$ signal, triggering at the start of every MPPT cycle.

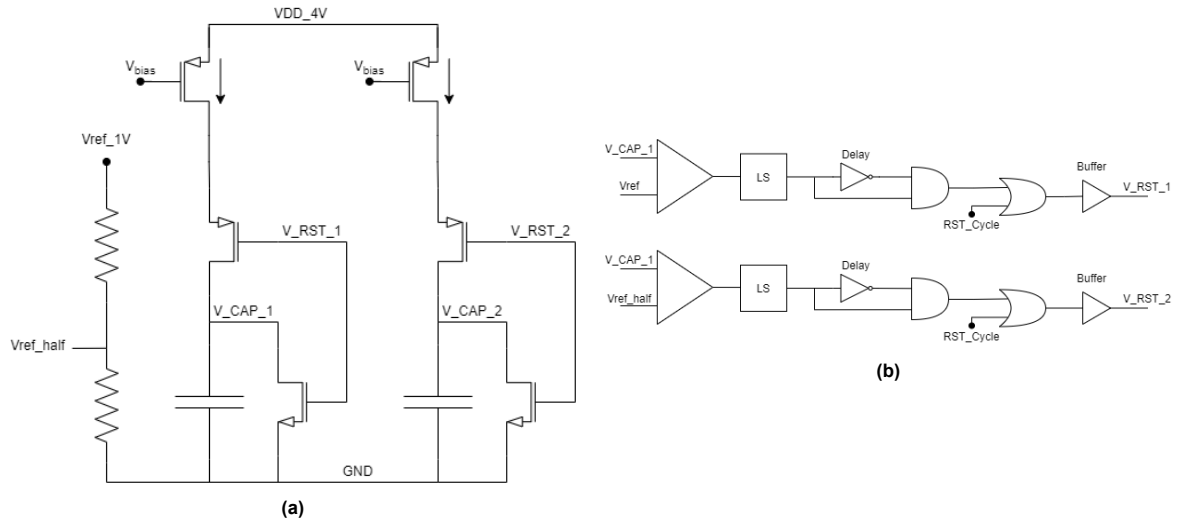


Figure 4.16: Sawtooth Wave Generator with (a) the integrating capacitors and (b) the reset circuit

4.7.1. Sawtooth-Wave Timing and Parasitics

The frequency of the sawtooth wave is controlled by the capacitance of the capacitor and the current that charges the capacitor. In case of a constant current, the time it takes to charge the capacitor from zero volt up to a specific voltage can be easily calculated using the current-voltage relation of a capacitor:

$$\Delta t = \frac{C \cdot \Delta V}{I} \tag{4.1}$$

The converter is designed for a 1MHz switching frequency. That means that the time available for charging the capacitor is $1\mu s$, assuming the reset time is negligible. Also, only little power is available, which means the charging current needs to be minimized. As mentioned before, the peak voltage can be set to 1 volt. Then, a balance between capacitance and charging current can be made by rewriting Equation 4.1 as done in Equation 4.2; the ratio between capacitance and charging current should be $1\mu FA^{-1}$. Several non-idealities have impact on this calculation.

$$\frac{C}{I} = \frac{\Delta t}{\Delta V} \tag{4.2}$$

Realistically, the capacitor discharge time cannot be zero. The aim is to discharge in one permille of the charging time, since at a thousandth, the duty cycle is not much affected, while being still achievable at 1 ns. But of course; the faster the discharging, the better. In order to discharge quickly, the resetting NMOS device needs to be able to accommodate such a short current peak. Increasing the width of the NMOS reset device introduces parasitic capacitances that will contribute to crosstalk between the reset signal and the capacitor voltage, modeled as in Figure 4.17. When the reset pulse is finished and V_{rst} pulls down again from 4 volts to zero, the voltage drop of V_{cap} can be calculated using the following equations, where $C_2 = C_{gd,n} + C_{gd,p}$ and initial conditions of $V_{cap} = 0$ and $V_{rst} = 4$ switching to $V_{rst} = 0$. Rearranging the terms of Equation 4.3e gives an expression for the voltage drop across the main capacitor due to parasitic capacitances as in Equation 4.4.

$$\Delta Q_1 = \Delta Q_2 \tag{4.3a}$$
$$C_1 \cdot \Delta V_1 = C_2 \cdot \Delta V_2 \tag{4.3b}$$
$$\Delta V_1 = V_{cap} = x \tag{4.3c}$$
$$\Delta V_2 = x + V_{rst} \tag{4.3d}$$
$$C_1 \cdot x = C_2 \cdot (x + V_{rst}) \tag{4.3e}$$

$$x = \Delta V_1 = \frac{V_{rst} \cdot C_2}{C_1 - C_2} \tag{4.4}$$

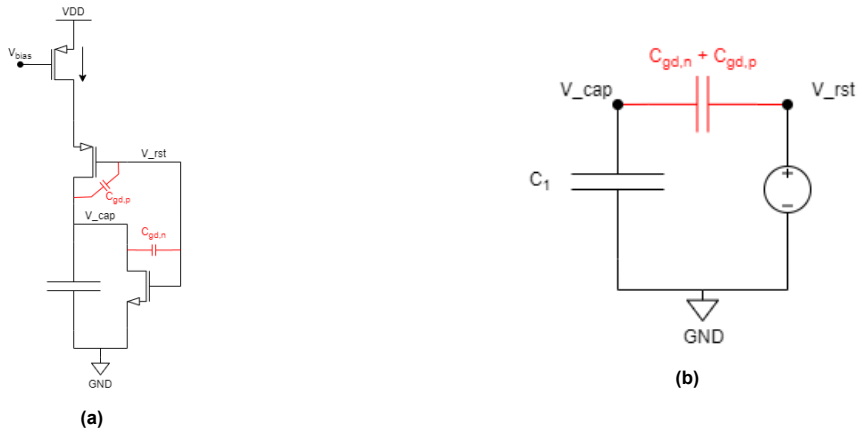


Figure 4.17: (a) Parasitic Gate-Drain capacitances in the relaxation circuit (b) Reset AC Coupling model

From Equation 4.4 it can be deduced that there is a lower limit to the capacitance of capacitor C_1 in relation to the parasitic capacitance C_2. The voltage drop will cause node V_{cap} to go below zero volts. This results in extra required time to charge the capacitor back up to the reference voltage. That extra time will also be added to the subsequent duty cycle, since the Duty Cycle Generator cannot compare

below zero volts. Fortunately, the effect on the duty cycle will be compensated for by the MPPT process. However, the extra time added to the duty-cycle signal will cause a slight misinterpretation of the duty cycle from the perspective of the Switch Segmentation controller, discussed in Chapter 5. The AC-coupling effect will have much less impact when switching node V_{rst} from zero volt to 4 volts due to the charge being drained to ground directly as well as the smaller voltage difference. The effect of AC coupling is shown in Figure 4.18; the parasitic capacitance pushes down the capacitor voltage below zero volts by an amount calculated using Equation 4.4 when the reset node drops from 4 volts to zero volts after discharging the main capacitor.

Another non-ideality is the propagation delay of the comparators from Figure 4.16b. The comparator requires some time to charge all of its nodes to the intended voltages, due to capacitances. The important nodes that require charging time are the output node caused by the load capacitance, the input nodes caused by the gate-capacitance of the input transistors and intermediate nodes caused by both gate-capacitances and drain-source capacitances of transistors used inside the comparator. The comparator transistors are sized with short gate lengths so as to maximize the transconductance and bandwidth. The choice for low-voltage transistors is made since the comparison decision is made around 1 volt and around 0.5 volt, so there is only a small voltage swing. The input pair of the comparator is of the PMOS type to accurately compare at low input voltages. Figure 4.19a shows the topology of the comparator. Also, increasing the biasing current will improve the speed of the comparator since it charges the load capacitance faster, but since the comparator will need to be on continuously as a sawtooth wave is always required for the operation of the converter, and only limited power is available, the biasing current can only be increased to some extent. Since the speed of the comparator is essentially the time it takes for it to charge the load capacitance to its intended output voltage, the output capacitor should be small to realise maximum speed. The outputs of the comparators are connected to the input gates of the levelshifters. Fortunately, the input transistor gate capacitance of the level shifter is small.

The input capacitance of the comparator also takes time to charge to its final value. This parasitic capacitance can be modeled as a capacitor in parallel to the oscillator's main capacitor, only slightly increasing the time required to charge to the reference voltage. Since the output voltage of the 0 degree phase shifted sawtooth wave is connected to both the inputs of the comparators unlike the 180 degree phase shifted sawtooth node, there will be a difference between the total capacitances (including parasitic capacitance) per branch. The difference in total capacitance will result a discrepancy between the slopes of the two sawtooth waves, that will cause inaccuracy in the moment of resetting of the 180 degree shifted sawtooth wave. In order to equalize the parasitic capacitances added to both the main capacitors, a dummy comparator is connected to the main capacitor of the 180 degree phase-shifted wave generator branch. The dummy comparator consists out of two input pairs, as seen in Figure 4.19b, without their second stages since they do not contribute to the input capacitance and would only consume extra power.

A pulse generator is placed after the comparator and level shifter. It generates a pulse that stays high as long as is required to discharge the capacitor. The pulse feeds into a buffer. The buffer is required to drive the discharging NMOS device. In designing the buffer, a consideration is made to minimize the power and delay product in the form of choosing a tapering factor [28]. When using two stages, the tapering factor can be calculated using Equation 4.5, where W_{power} is the width of the transistor to be driven and W_{unit} the width of the unit transistor. The delay of the buffer will add on to the propagation delay of the comparator.

$$f = \sqrt[2]{\frac{W_{power}}{W_{unit}}} \tag{4.5}$$

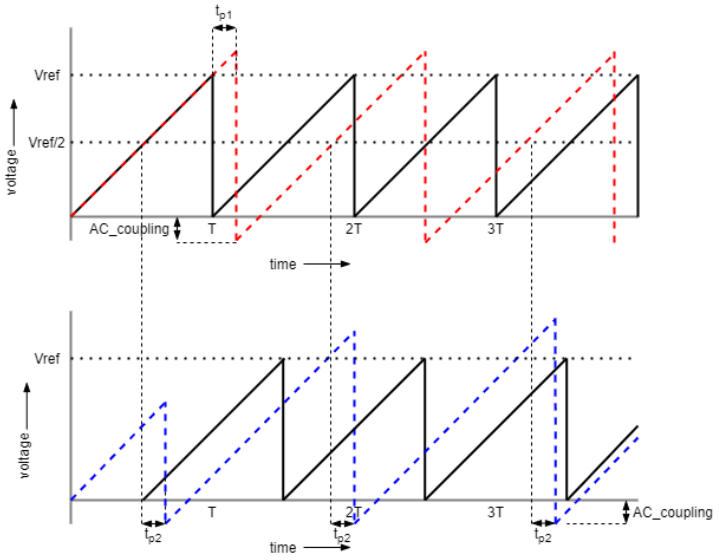


Figure 4.18: Plot of the sawtooth wave generator output with non-idealities, where the upper plot is the zero degree shifted sawtooth wave and the lower plot is the 180 degree shifted sawtooth wave. The black lines show the ideal sawtooth waveforms.

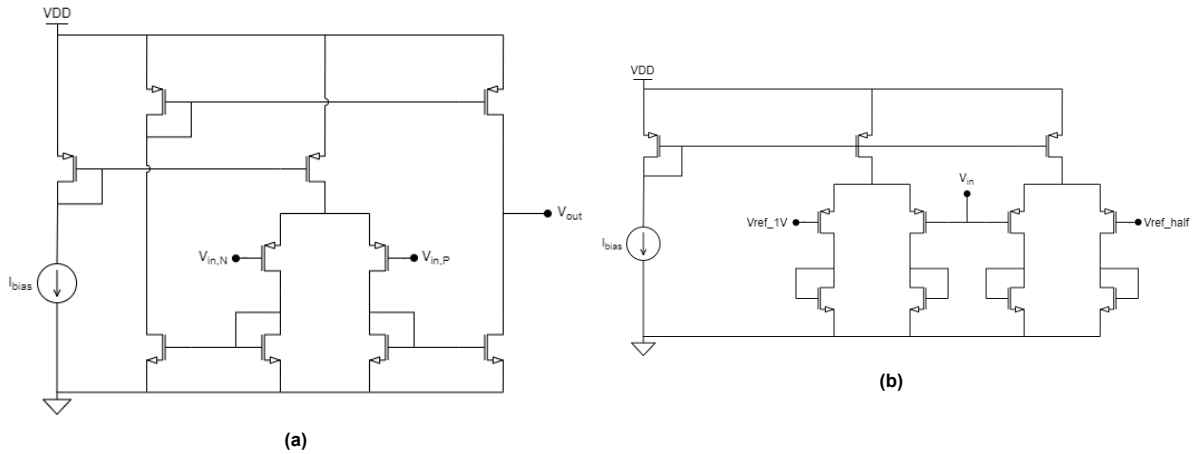


Figure 4.19: (a) Wave Generator Comparator topology (b) Wave Generator dummy comparator

Figure 4.18 shows a plot of the sawtooth wave generator and the effects of AC coupling and comparator propagation delay. Here, the black-line sawtooth waves show the ideal case. The dashed-line waveforms show the non-ideal cases. The simulation result after post-layout extraction is shown in Figure 4.20. As expected, the AC coupling effect causes a voltage drop of around 100 mV below zero volt and the propagation delay causes the peak voltage to cross the 1 volt reference voltage by about 100 mV as well. The graph also shows that the resetting of Sawtooth Wave 2 does not happen at 50% of the Sawtooth-Wave 1 cycle, and thus the phase shift is more than 180 degrees. The first wave triggers both itself as well as the second wave. A possible solution is to make the wave generators cross coupled, meaning that the first wave resets the second wave and the second wave resets the first when either of the waves reaches half the full scale voltage. One of the main capacitors will need to be precharged before starting the oscillator to establish the 180 degree phase difference between the two sawtooth waves. The capacitor needs to be charged to half the full scale voltage.

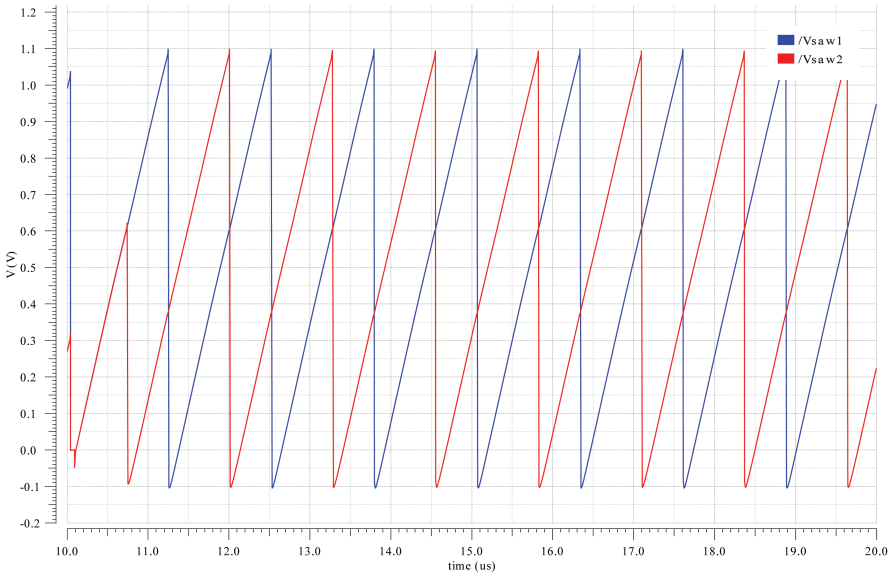


Figure 4.20: Post layout transient simulation result of sawtooth wave generator

The option of implementing a triangular wave generator was also explored. A possible implementation of a triangular wave generator is shown in Figure 4.21. A triangular wave generator requires a comparator to detect the peak voltage, as well as a comparator to detect the zero voltage crossing. This means a propagation delay is inserted both on the high side as well as on the low side. The influence of these propagation delays on the triangular wave can be seen in Figure 4.22, where the black line shows the ideal triangle waveform and the dashed blue line shows the non-ideal triangle waveform. It was found that the switching of the comparator detecting the zero voltage crossing had a large impact on the output wave, due to capacitive coupling. Because of this difficulty to generate a proper triangle wave, as well as the need for double the amount of comparators with accompanying propagation delays, the choice for implementing a sawtooth wave generator was made.

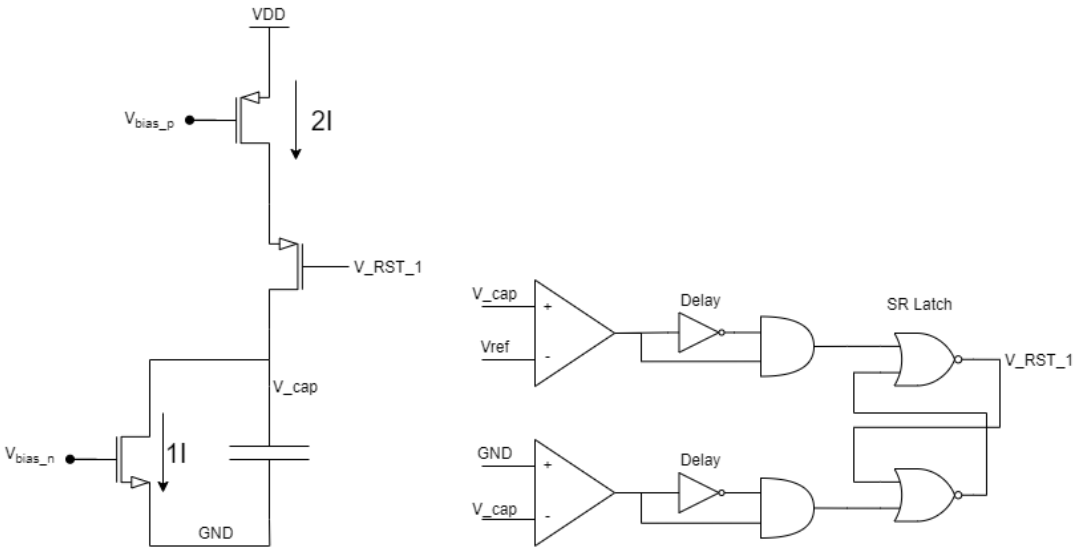


Figure 4.21: Triangular wave generator circuit implementation

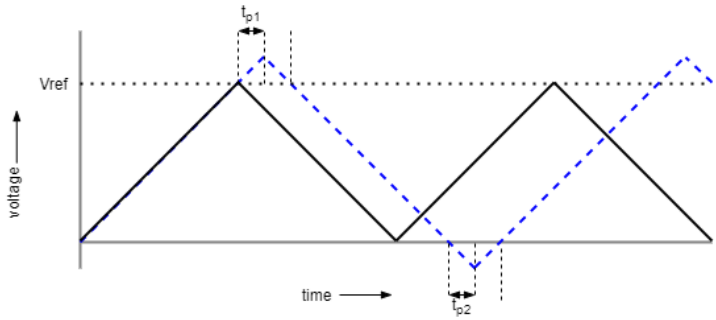


Figure 4.22: Plot of the ideal triangular wave generator output (black line) and a triangular wave with the effects of comparator propagation delays (dashed blue line)

4.7.2. Process and Temperature Variation

As described in Subsection 4.7.1, some key characteristics of the wave generator highly depend on component values and biasing currents. Process variation may cause these component sizes to be slightly inaccurate. Since small component sizes are chosen for power efficiency purposes, process variation caused size fluctuation may be relatively large. These inaccuracies directly influence the waveform at the output of the generator. A Monte-Carlo analysis was done with 200 repetitions to check the consequences of process variations, as seen in Table 4.1. The table shows the minimum and maximum values for phase difference between the two sawtooth waves generated, the sawtooth wave frequencies, the sawtooth's maximum voltage and the sawtooth's minimum voltage, as a result of process variation. Also, the mean values are displayed, as well as the standard deviation from these mean values. In the first row, it can be seen that the phase difference, displayed as a percentage of 360 degrees, is higher than the intended 50%, representing 180 degrees phase difference. The table also shows that process variations mostly impact the frequencies of the sawtooth waves, and that the sawtooth waves' frequencies are lower than the intended 1 MHz. Some options for improvement are discussed in Chapter 7.

Table 4.1: Sawtooth Wave Generator Monte-Carlo analyses results

Name	Min	Max	Mean	Std Dev
Phase difference [%]	58.1%	59.3%	58.7%	0.258%
Freq wave 1 [Hz]	785.3k	958.6k	868.5k	27.17k
Freq wave 2 [Hz]	785.3k	958.6k	868.5k	27.17k
Vmax wave 1 [V]	1.073	1.093	1.085	3.86m
Vmax wave 2 [V]	1.073	1.093	1.085	3.76m
Vmin wave 1 [V]	-118.2m	-95.53m	-106.9m	4.02m
Vmin wave 2 [V]	-116m	-93.85m	-104.9m	3.93m

5

Segmented Switch Design

As stated in Chapter 3, the size of the power switches can be optimized for a specific input power setting. The energy dissipated in the power switches mainly comes from two loss mechanisms; conduction loss and gate-charge loss. The conduction loss of the power switch can be reduced by decreasing the on-resistance of the switch. The on-resistance reduces when the width of the MOSFET is increased. The gate-charge loss originates from the parasitic capacitances of the gate. When switching the MOSFET on, the gate capacitances first need to be charged, as well as being discharged when turning off the switch. These parasitic gate capacitances are proportional to the width of the MOSFETs.

The low-side power switches are implemented using 5V NMOS devices. For the high-side power switch the choice for 5V PMOS devices was made. PMOS devices are worse conductors than NMOS devices, however, an NMOS device would be difficult to switch in the high-side position. Since the high-side device's source is not connected to ground, an NMOS device would require a bootstrapping circuit to be able to switch it on. Bootstrapping adds extra complexity to the circuit and requires extra on-chip capacitor area. The PMOS device will be easy to switch in the high-side position, since it will be turned on when the gate is pulled to ground as the source is connected to the output battery that fixes the voltage to 4 volts.

The power switches are controlled by the PWM signal coming from the Duty Cycle Generator. Before that signal reaches the switches, it first goes through a non-overlapping clock generator circuit. This circuit ensures that the low-side switch and high-side switch are never conducting at the same time, preventing a short circuit from the battery to ground.

5.1. Tapered Buffer

The large power switches will require a driver to switch the devices fast enough. As the switching frequency of the power devices is determined by the frequency of the sawtooth wave generator, the switching frequency will be just below 1 MHz, as can be seen in Table 4.1. The driver will be implemented in the form of a tapered buffer. The buffer supplies the current required to charge or discharge the parasitic gate capacitance of the power switch in order for it to make the transition in the amount of time that is available. The buffer is implemented by cascading inverter stages with an increasing width. Increasing the amount of inverter stages will first reduce the propagation delay, up to a certain amount from which the propagation delay will increase again. Increasing the amount of inverter stages will also increase the power dissipation. The amount of inverter stages that is optimal for propagation delay and power dissipation depends on the gate capacitance of the power switch and the transistor technology that is used, that is to say the gate capacitance of the unit inverter [29]. It should be noted that using an odd number of inverter stages will invert the control signal. Cherkauer (1995) shows that the optimum amount of inverter stages in this application is either 4 or 5 [29]. Therefore, the NMOS power switches will be driven by 4-stage buffers and the PMOS devices will be driven by 5-stage buffers. The tapering factor can be calculated using Equation 5.1, where N is the number of stages, W_{pwr} is the width of the power switch and W_{unit} is the width of the unit transistor.

$$f = \sqrt[N]{\frac{W_{pwr}}{W_{unit}}} \tag{5.1}$$

5.2. Power Switch Width Optimization

A simulation was done to find the optimum width of the NMOS device for conducting the current described in the Thesis Objective of Chapter 1; a total input current of 625mA, an input voltage of 0.4V, an output voltage of 4V and a duty cycle of 90%. A simulation setup was made as shown in Figure 5.1. The optimization was done by executing transient simulations for device widths ranging from $10000\mu m$ to $50000\mu m$. For every width the tapering factor is calculated using Equation 5.1 and the widths of the driver transistors are set accordingly. A pulse switches the buffer and subsequently the power switch. The current that is drawn from the voltage source supplying the buffer is measured. The total gate-charge loss is determined by multiplying this measured current to the voltage of the voltage source supplying the buffer. When the switch is turned on, the voltage drop across the power switch's drain and source terminals is measured to determine the conduction loss. The total conduction loss in the NMOS low-side power switches is calculated by multiplying by two (since there are two NMOS devices in the interleaved boost topology) and multiplying the conduction loss of the single NMOS device by the duty cycle (percentage of time the device is conducting). The current source connected to the drain and source of the power switch mimics the inductor in the boost converter, and the current is set to the input specification per inductor branch of 312.5mA. The conduction loss and gate-charge loss are plotted against the width of the power switch (amount of fingers, where one finger has a $100\mu m$ width), as well as the sum of the two losses. Figure 5.2 shows the results of the optimization simulation with an optimum width of $35000\mu m$.

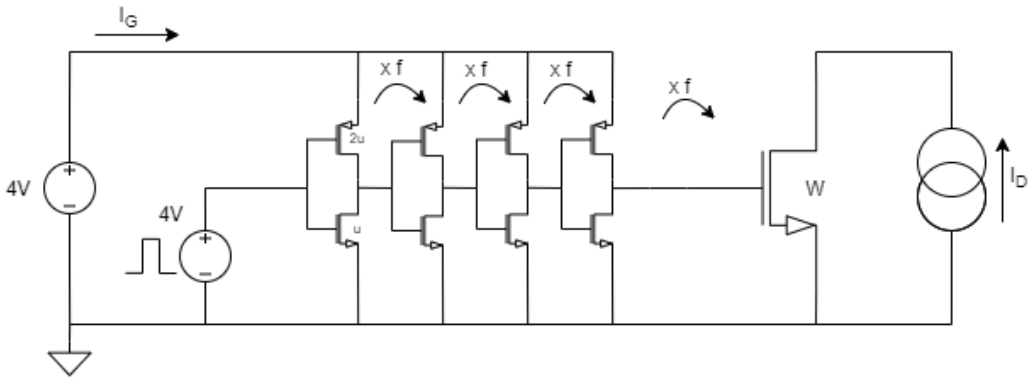


Figure 5.1: Width optimization simulation circuit for NMOS device including driver

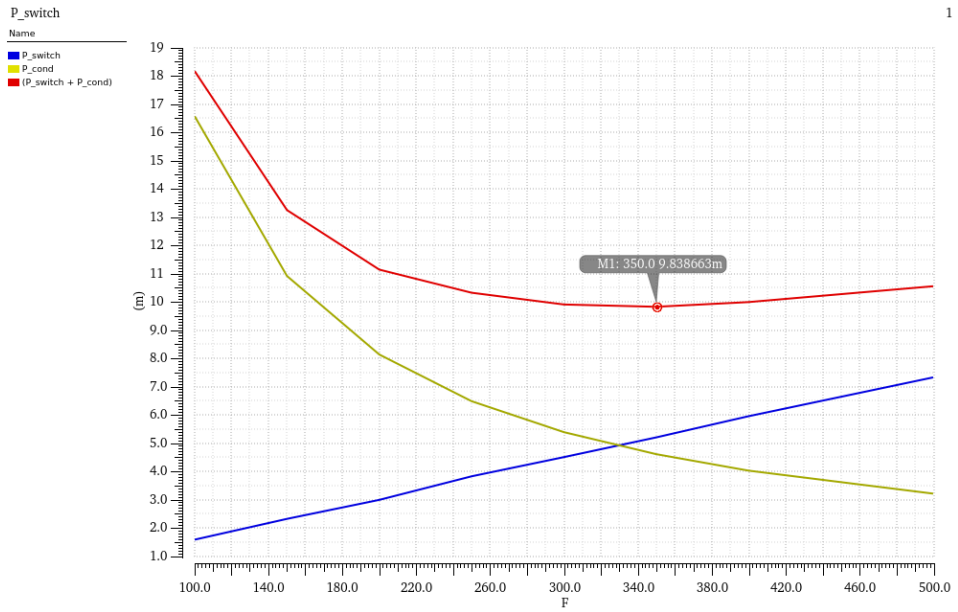


Figure 5.2: Width optimization simulation result for NMOS device including driver

A similar simulation was performed for the PMOS power switch. The test circuit is shown in Figure 5.3. The total conduction loss in the PMOS devices is calculated by multiplying the conduction loss of the single PMOS device by two and multiplying by 1 minus the duty cycle (percentage of time it is conducting). The width of the PMOS power switch ranges from $10000\mu m$ up to $70000\mu m$. The result of the simulation is shown in Figure 5.4, with an optimal width of $40000\mu m$.

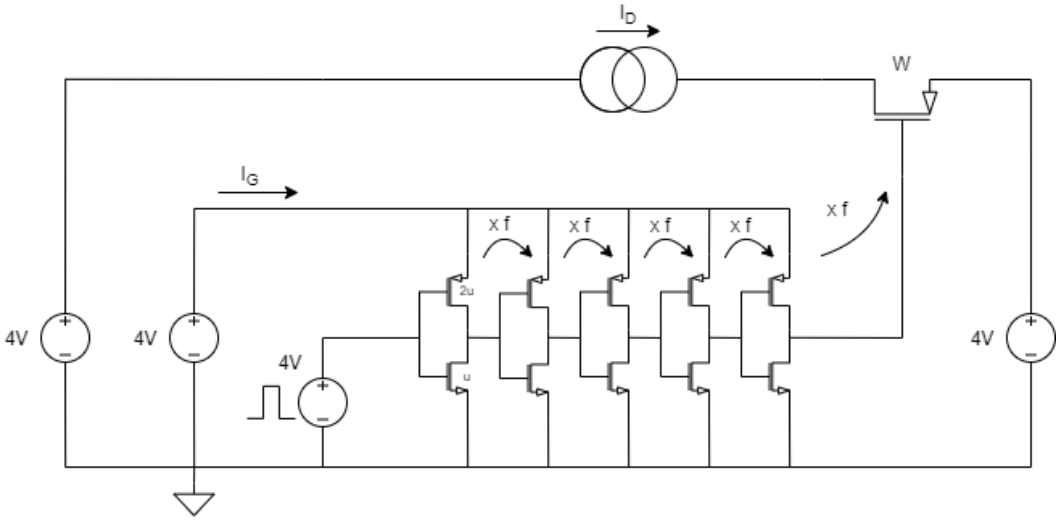


Figure 5.3: Width optimization simulation circuit for PMOS device including driver

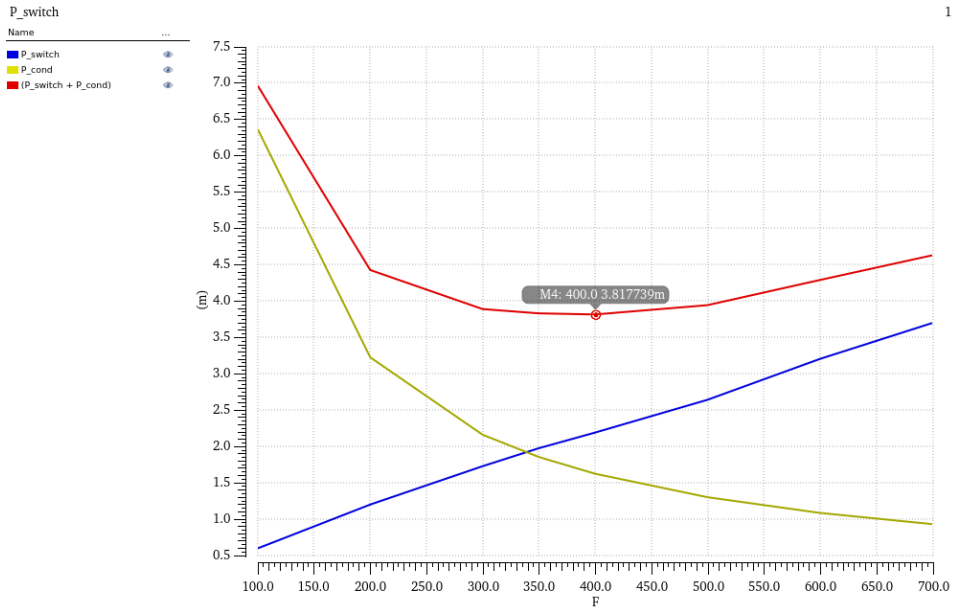


Figure 5.4: Width optimization simulation result for PMOS device including driver

5.3. Switch Segmentation

The situation may occur where only a limited amount of power is available from the harvesting transducer. In that case, only a small current can be delivered. When this is the case, the gate-charge losses from a large gate will become disproportionately large with respect to the input current. For that reason, smaller power switches are preferred when little power is available. The large power switches suggested in Section 5.2 can be split up into multiple smaller switches. That way, the switch width can be made configurable according to the available input current. When a high input current is detected, multiple segments can be added to the conduction path. And when a low input current is detected, only one segment will be conducting, and in that case only that specific switch needs to be switched on and off, thus reducing the total gate-charge loss.

In order to know how much input current is available from the transducer, and thus how wide the power switches should be, its magnitude must be tracked. Since the output current is already measured during the MPPT cycle as described in Section 4.2, and the duty cycle is set during the MPPT, the input current can be determined using the values found for the output current and duty cycle. The relation between input current and output current and duty cycle is known, namely, as described in Chapter 3, more specifically in Equation 3.10. This equation can be rewritten to form an expression for the input current as a function of the output current and the duty cycle, as in Equation 5.2.

$$I_{in} = \frac{I_{out}}{1 - D} \tag{5.2}$$

The output current will range from 0 to 62.5 mA (250 mW max output at 4 volts). To keep the logic circuitry somewhat simple, the output current range is split up into four parts, such that it can be represented by two bits. The output current segments are shown in Table 5.1, including their binary representation. The duty cycle information from the MPPT is then also categorized into four parts by taking the left two bits of the original 5-bit representation. The binary values and what duty cycle range they represent are displayed in Table 5.2. Unfortunately, quite a lot of information is lost when only the two most significant bits of the duty cycle are selected. This will introduce errors in the input current representation. Appendix A shows a table with in the first column all 32 possible duty cycle values (since 5 bits). The table then shows how the duty cycle will be interpreted by the Segment Control block (which will be discussed in Section 5.4) as a 2-bit representation. The input current is calculated for the binary values of the output current and both the 2-bit duty cycle as well as the actual 5-bit duty cycle, using Equation 5.2. The difference between the two outcomes shows the error due to truncation. The table presented in Appendix A gives an indication of the errors that can possibly occur.

Table 5.1: 2-Bit binary representation of output current with their corresponding range

I_{out} **Binary**	I_{out} **min.**	I_{out} **max.**
00	0 mA	15.63 mA
01	15.63 mA	31.25 mA
10	31.25 mA	46.88 mA
11	46.88 mA	62.5 mA

Table 5.2: 2-Bit binary representation of the duty cycle with its corresponding range

D<3:4>	**D min.**	**D max.**
00	0	0.21875
01	0.25	0.46875
10	0.50	0.71875
11	0.75	0.96875

The maximum input current that can be calculated with the two 2-bit variables is 250 mA, as seen in Equation 5.3, assuming the highest value in the range of the output current. The outcomes of the input current calculation will also be represented by a 2-bit binary code. Therefore, the input current outcomes can be interpreted as shown in Table 5.3.

$$I_{in\_max} = \frac{62.5 \times 10^{-3}}{1 - 0.75} = 250 \times 10^{-3} A \tag{5.3}$$

Table 5.3: 2-Bit binary input current calculation outcome, including the range it represents

I_{in} **Binary**	I_{in} **min.**	I_{in} **max.**
00	0 mA	62.5 mA
01	62.5 mA	125 mA
10	125 mA	187.5 mA
11	187.5 mA	250 mA

The combination of all input variables and their corresponding output code results in a truth table, which can be found in Appendix B. The calculation result for the input current can be used to set the amount of power switch segments that are selected to be switched. Since the result of the calculation is a 2-bit binary code, the power switches will consist of 4 segments. The size of the segments is the result of the optimization from Section 5.2 divided by four. Each segment will require its own tapered buffer, such that a specific buffer can also stay off when their segment is not required to be switched. One segment will always need to be switched, otherwise the interleaved boost converter would not function. The three remaining segments are selected by a thermometer code representation of the input current code. The segment sizes are made equal and the segments are selected by thermometer code since if the switch segments were sized according a binary weighting, the segments would require different buffers with different sizes and thus different propagation delays. This would result in different switching behaviour of the segments. Equal size segments also allow them to be easily matched in layout, and allow for equal distribution of currents across the segments. The circuits for the low-side NMOS and high-side PMOS segmented power switches are shown in Figure 5.5. The diode seen in Figure 5.5b is added to prevent charge build-up (and thus high-voltage peaks) at the input of the high-side PMOS power switch during the dead-time as described in Subsection 3.1.3.

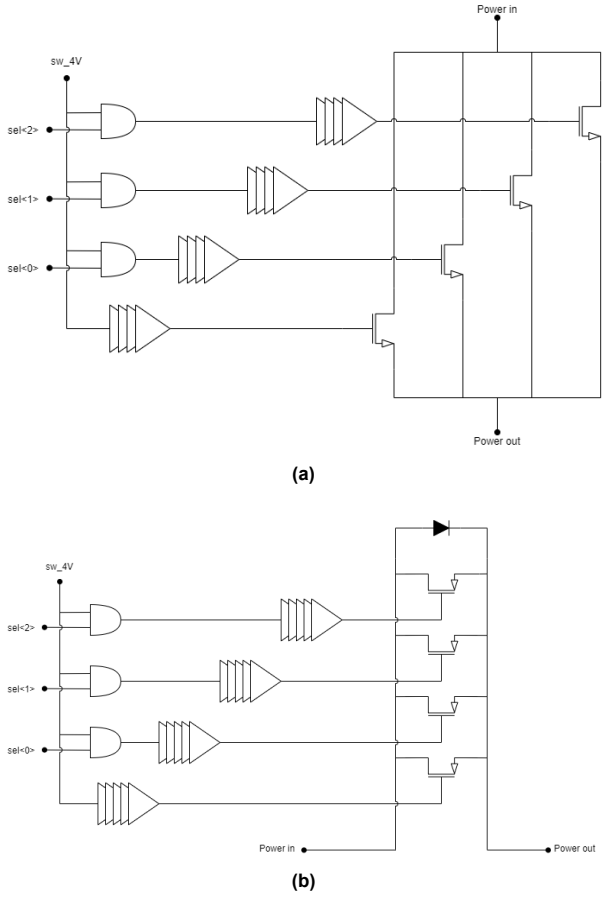


Figure 5.5: (a) Low-side NMOS Segmented Switch (b) High-side PMOS Segmented Switch

5.4. Segment Control

To execute the calculation described in Section 5.3, a Segment Control block is implemented. The block reads the required information from the MPPT block, executes the calculation and sends the results to the Segmented Switches. In order to perform calculations with the measured output current information, which is an analog signal that can reach from 4V down to 2V, it needs to be converted to a 2-bit digital code. The two most significant bits coming from the Duty Cycle Counter are inverted to perform calculations, since the counter represents the inverse of the actual duty cycle. The bits could also be directly processed by the calculation unit, taking the inversion into account, but the choice for adding the inverters was made to keep the simulations, debugging and the design overall comprehensive and uncluttered. The Analog-to-Digital converter is described in this section. The implementation of the calculation unit and the binary decoder are also discussed.

5.4.1. Analog-to-Digital Converter

In order to perform the required calculation, the values for the variables need to be represented digitally. The value for the duty cycle is already available as a 5-bit binary number. The measured output current, however, is represented by a voltage ranging between 4 and 2 volts. An Analog-to-Digital Converter (ADC) is implemented in the form of a Flash ADC. In the Flash ADC, the input value is compared to different reference levels using comparators. The reference levels are evenly spaced voltages between 4 and 2 volts. When the input voltage crosses a specific reference level, the comparator detects the crossing and switches its output. The reference voltages are set by a voltage ladder, using 4 equal size resistors connected in series between the 4 and 2 volt supplies, creating three reference voltages of 2.5V, 3V and 3.5V. In order to keep the conduction loss low, the resistors should be as large as the available area allows them to be, to minimize the current. The outputs of the three comparators create a 3-bit thermometer code. This code is then converted to a 2-bit binary code using logic gates. Since

a high input voltage represents a low output current, and vice-versa, the comparison result is actually an inverted representation. Therefore, an extra set of inverters is added at the output of the block. The code could again be processed directly by the calculation unit, but for comprehensibility and clarity reasons the inverters were added.

Figure 5.6 shows the circuit of the implemented ADC. The resistors have resistor value of 188.1 $k\Omega$. Therefore, the conduction loss due to the voltage ladder can be calculated as in Equation 5.4. An important functionality of the comparators used in an ADC is that they make their decision on the rising edge of a clock signal. These decisions are then stored in an SR-latch at the output of the comparator. This way, the decision is made when the correct information is delivered by the MPPT block, since the output current is not constantly measured. The clock is therefore also triggered by the MPPT, more specifically, by the F_CLK signal that was shown in Figure 4.2. The comparators are implemented by the NH2 latched comparators with NMOS input pairs designed by Nowi.

$$P_{loss} = \frac{V^2}{R_{total}} = \frac{4-2}{4 \cdot 188.1 \times 10^3} = 2.66\mu\text{W} \tag{5.4}$$

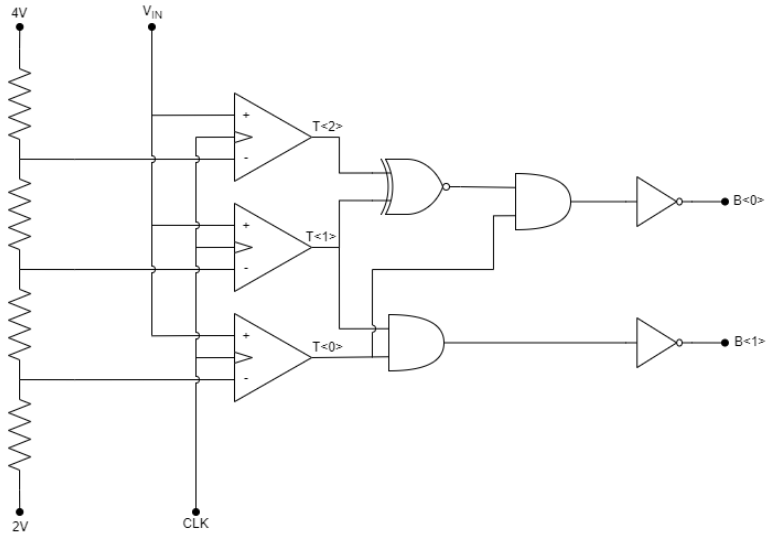


Figure 5.6: Circuit design of the Flash ADC

Figure 5.7 shows the results of a test simulation, where Figure 5.7a shows the input voltage, representing the measured output current as a slope from 4 volts down to 2 volts, as well as the reference voltages generated by the voltage ladder. Figure 5.7b shows the output values of the comparators, as a result of the input voltage sweep from 4 to 2 volts. Figure 5.7c shows the accompanying binary output code. It can be noted that the comparator output transition appears too early. Possible causes of this issue are discussed in Subsection 7.5.1.

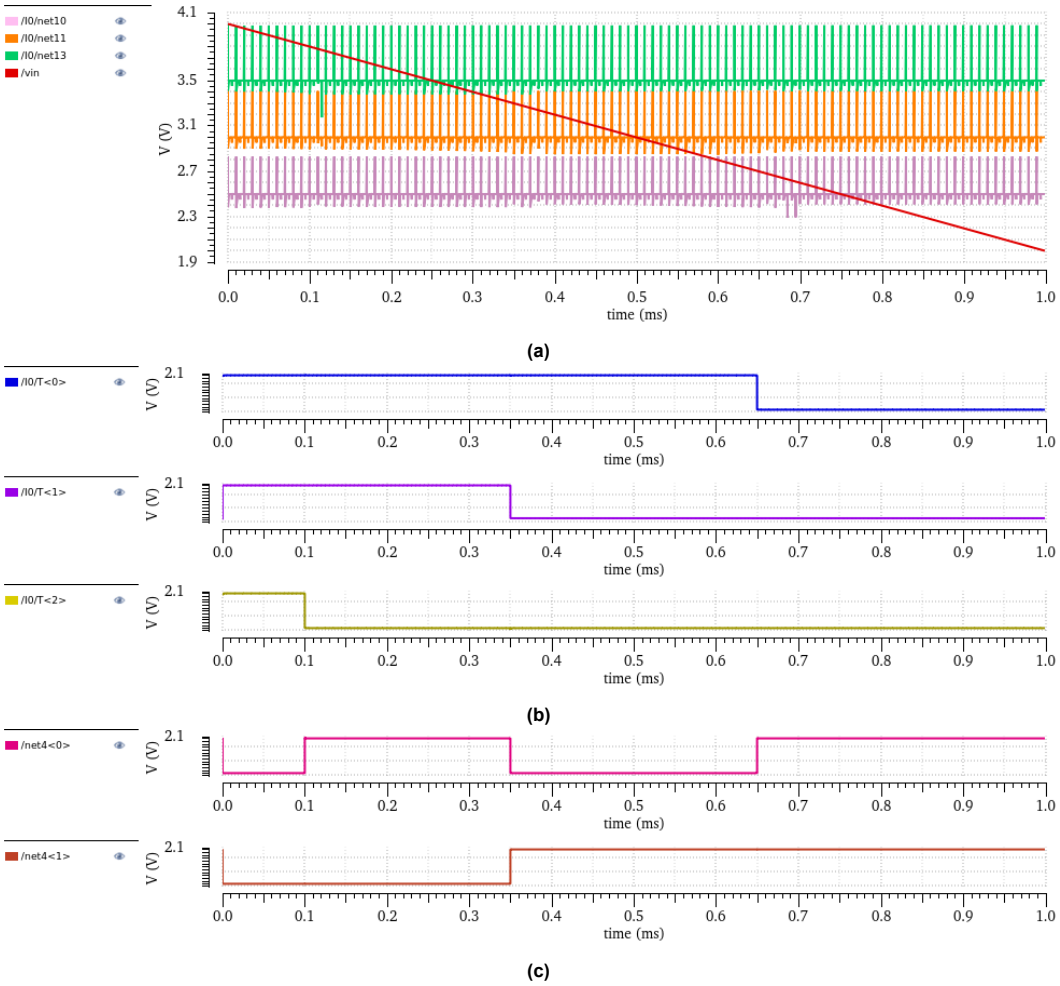


Figure 5.7: (a) Input voltage representation of output current (red) and reference voltages, (b) 3-Bit thermometer inverse output code and (c) the 2-Bit binary output code

5.4.2. Segment Calculation Unit

With the help of a Karnaugh map, a logic expression for the calculation described by Equation 5.2 can be formulated. The Karnaugh map is filled in by inspecting the truth table from Appendix B. For both bits of the binary Input Current code a Karnaugh map can be made, as seen in Figure 5.8.

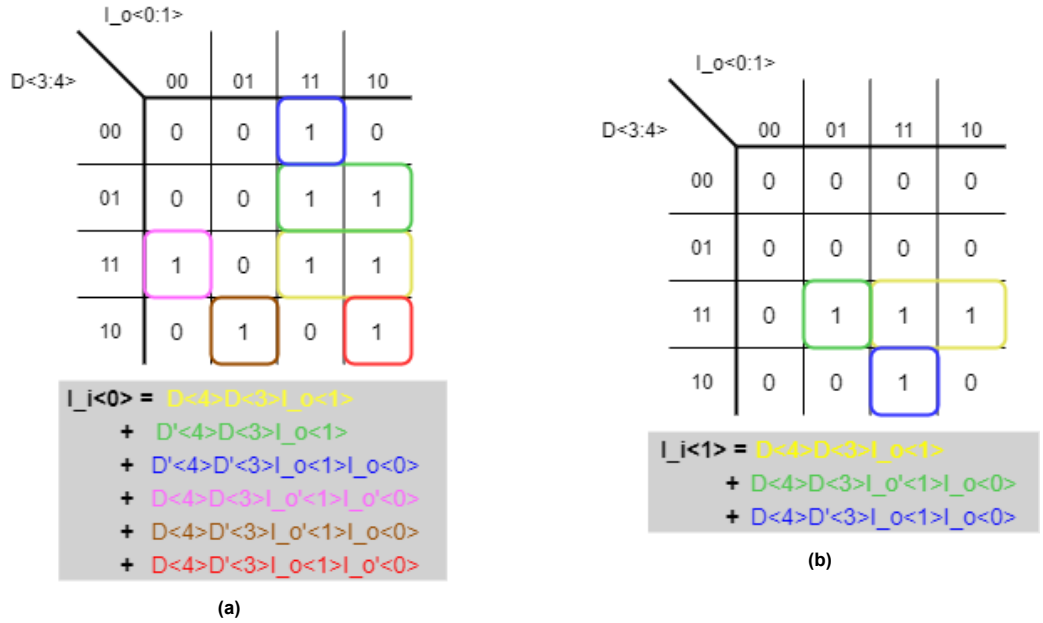


Figure 5.8: Karnaugh maps of the calculated binary input currents (a) $I\_i<0>$ and (b) $I\_i<1>$, including the extracted logic functions

The logic functions created using the Karnaugh maps can be easily translated to a combination of logic gates. Every multiplication in the logic function represents an AND-gate, and every addition represents an OR-gate. Such a translation results in the circuits shown in Figure 5.9.

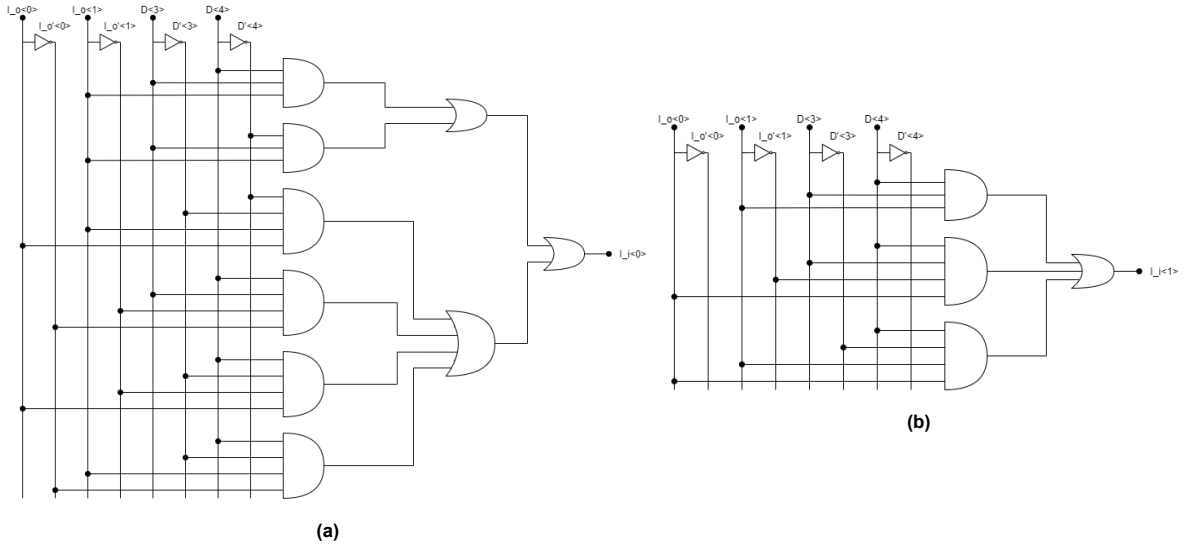


Figure 5.9: Logic gates realizing the calculation of the input current as a function of output current and duty cycle where (a) calculates $I\_i<0>$ and (b) calculates $I\_i<1>$

Figure 5.10 shows the simulation results[1] of the Segment Control block, for all possible different input values.

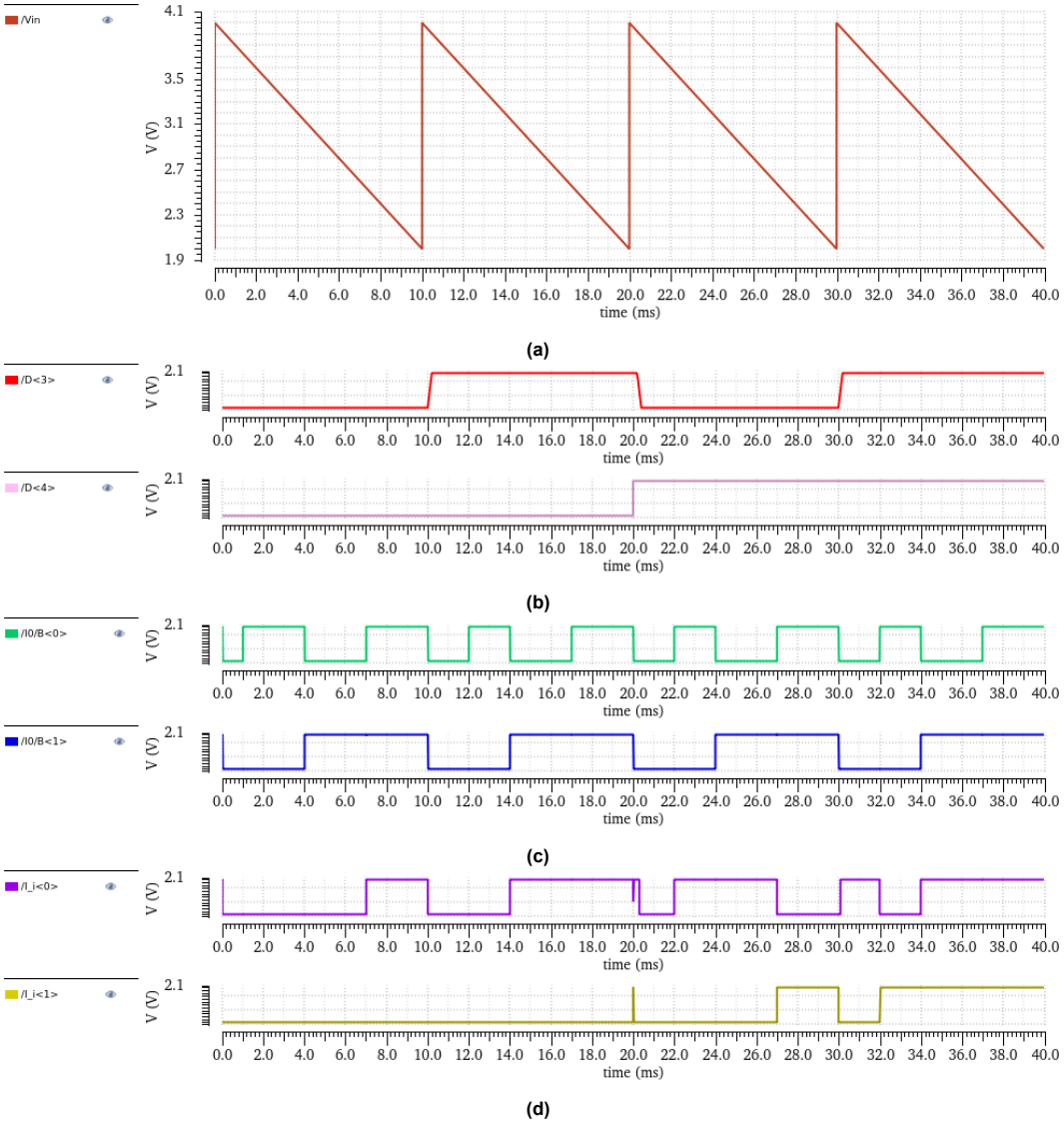


Figure 5.10: (a) Input voltage representation of output current, (b) 2-Bit duty cycle input code, (c) 2-Bit binary representation of Output Current after ADC and (d) the calculated 2-bit Input Current code

[1] in Figure 5.10d, two spikes occur at 20 ms. The spikes are caused by a slight misalignment of the transitions of the input signals in the simulation going to the calculation unit. The spikes are unlikely to occur in real time operation, since all the input-signal transitions are triggered by the same clock.

The result of the logic calculation unit will be in the form of a 2-bit code, and is afterwards converted into a 3-bit thermometer code using simple logic as shown in Figure 5.11, with its corresponding truth table in Table 5.4. The 3-bit thermometer code is level-shifted to 4 volts, and sent to the power switch segments to be activated or not, according to the code.

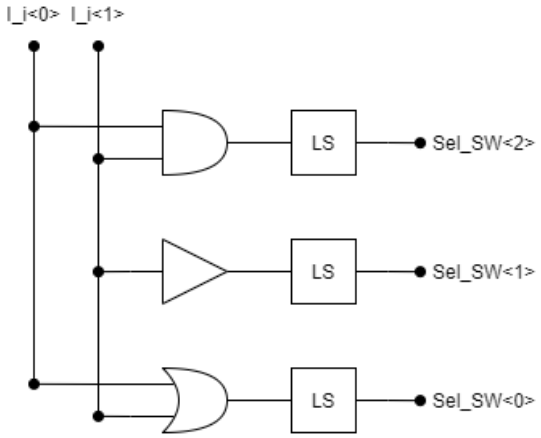


Figure 5.11: 2-Bit binary to 3-bit thermometer decoder

Table 5.4: 2-Bit binary to 3 bit thermometer decoder truth table

B$<1>$	B$<0>$	Sel_SW$<2>$	Sel_SW$<1>$	Sel_SW$<0>$
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

6

Results

The interleaved boost converter with maximum power point tracking and segmented power switches was implemented in Cadence Virtuoso. After simulating the top level design, the layout was designed using the Virtuoso Layout Design Suite. The layout will be discussed in this chapter, as well as the simulation setups and the simulation results.

6.1. Layout

The layout design of the system is shown in Figure 6.1. A distinction was made between digital power supplies and analog power supplies and analog and digital grounds, in order to prevent the digital switching from inducing switching noise due to capacitive coupling onto the analog power supply rails. Since high currents will pass through the chip traces connecting the power switches, it is important that these power lines are wide enough to be able to carry the currents without burning through, in the extreme case, and without large voltage drops due to high resistive paths. The power lines are constructed of stacked metal layers, to increase the conductivity.

A separate ground is placed to connect the sources of the NMOS low-side power switches, since high currents will be flowing through this ground, and should not induce noise onto the grounds of the analog and digital circuitry. The pins are connected to the bond pads, where the bond wires can be placed. The bond pads are positioned inside the guard ring. The guard ring adds ESD protection to the chip, in the form of diodes to catch high voltage peaks and mitigate the peaks to the supply rail.

The chip's active area has a size of 1425 μm by 787.6 μm for an area of 1.12 mm^2, and a full size of 1740 μm by 1263 μm for a total area of 2.20 mm^2.

6.1.1. Pin list

Table 6.1 shows a list of all the pins.

Table 6.1: Chip pin list

Pin no.	Pin name	Description
1	L1_in	First inductor connection
2	INDGND	Converter power ground
3	L2_in	Second inductor connection
4	DGND	Digital ground
5	AGND	Analog ground
6	tst_D0	Duty cycle test pin
7	tst_D180	180 degrees shifted duty cycle test pin
8	tst_MPPT_Cycle	MPPT cycle test pin
9	tst_SegSw_$< 0 >$	Switch segmentation info bit 0
10	tst_SegSw_$< 1 >$	Switch segmentation info bit 1
11	Ibias2_500n	Biasing current 500nA
12	Ibias1_500n	Biasing current 500nA
13	CLK_1kHz	MPPT clock signal of 1kHz, 2V
14	Vref_1V	Reference voltage of 1V
15	DVDD_4V	Digital supply 4V
16	DVDD_2V	Digital supply 2V
17	AVDD_4V	Analog supply 4V
18	AVDD_2V	Analog supply 2V
19	VBAT	Output battery connection
20	MPPT_Cap	External capacitor connection

6.1.2. Test Pins

Some extra pins were added to the layout design to be able to check the functionality of the chip once it has been taped out. The chip can then be tested in the lab. The pins should allow for inspection of functionality and possibly debugging. The first two test pins that are added are pins for both the duty-cycle signals. The duty cycle signals carry information on the result of the maximum power point tracking process. When testing, the actual duty cycle of the signals can be monitored whether it corresponds with the expected duty cycle related to the transducer's input current and voltage.

Test pins were also added for the Switch Segmentation information, such that can be verified if the correct amount of segments are activated. Finally, a connection was made to the $MPPT\_cycle$ node. This pin allows to check if the MPPT cycle starts every second. The pin will also allow for the MPPT cycle trigger to be forced from outside the chip.

In order to add the test pins, a buffer is required to be positioned between the actual signal on the chip and the bond pad. This buffer ensures that the capacitive load that will be connected to the bond pad can be driven. The MPPT Cycle test pin requires the ability for the signal to also go in the opposite direction. Therefore, an extra resistor is placed between the bond pad and the buffer that comes from the original signal source. This resistor prevents a possible short circuit when the signal generated on the chip is low, but a high signal is applied from outside to the receiving end of that signal.

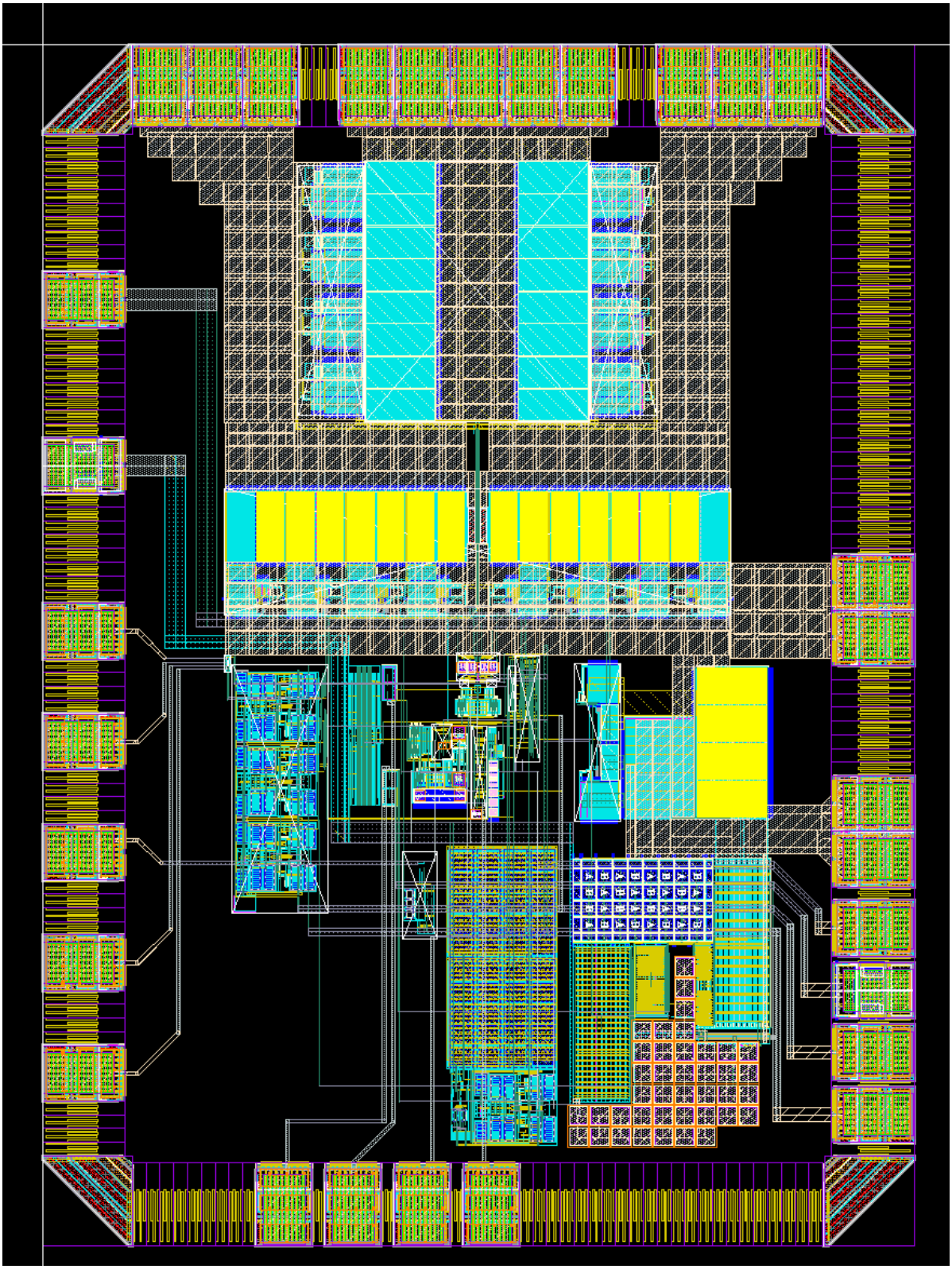


Figure 6.1: Layout design of the chip

6.2. Top Level Simulation

Top level circuit simulations were executed using Analog FastSPICE simulator in Cadence. Simulations for several different transducer input settings were done. Figure 6.2 shows the test setup circuit to simulate the chip. The PV Cell transducer is modeled by a voltage source and series resistance of which their values are used to set the transducer input settings, as a function of the target input power. V_{PV} is set to two times the target MPP input voltage, and Rs_in is set using Equation 6.1 where V_{in} and P_{in} are the target MPP settings. Since every transient simulation run is performed for a single specific input power setting, this simplified PV Cell model can be used instead of the more elaborate model described in Subsection 2.1.2.

$$Rs\_in = \frac{V_{in}^2}{P_{in}} \tag{6.1}$$

During the simulation, all the currents supplied by the voltage sources are measured. These currents can be multiplied by their corresponding voltages to determine the power that is supplied by a specific source. The input power coming from the transducer is determined by measuring the current going through the PV Cell series resistance, and multiplying it by the voltage measured at point V_{in}. The output power is determined by measuring the current going into the series resistance of the battery model, multiplied by the voltage measured at the chip output pin $VBAT$ (not the $Vbat$ battery voltage). The efficiency can then be calculated by taking the ratio between the power going out (into the battery) and the power going in, including the power from the voltage supplies, as seen in Equation 6.2

The inductors used in the simulation both have an inductance of 2.2μH and an ESR of 90 $m\Omega$. The battery model has an ESR of 10 $m\Omega$, and the battery voltage $Vbat$ is set to 3.9V.

$$\eta = \frac{P_{out}}{P_{in} + P_{A2V} + P_{A4V} + P_{D2V} + P_{D4V}} \tag{6.2}$$

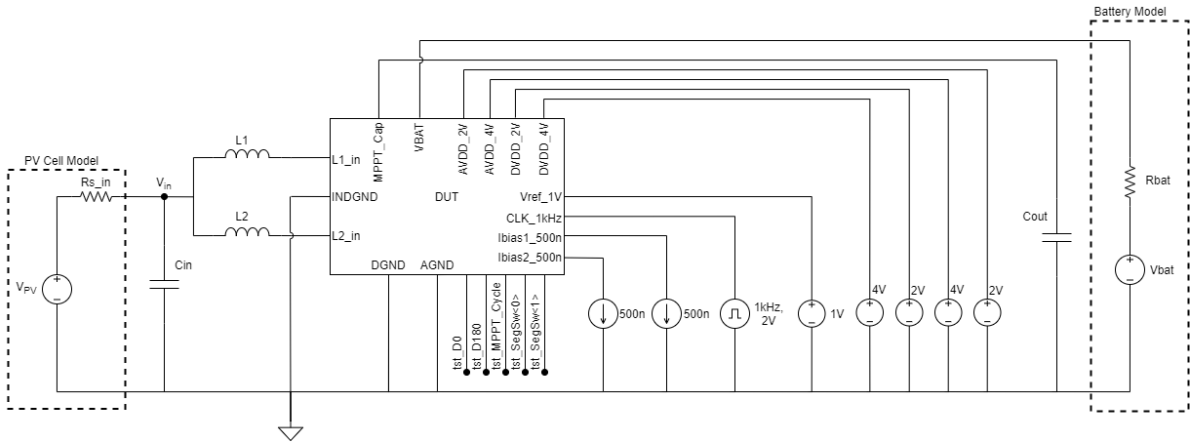


Figure 6.2: Circuit diagram of top level test setup

Table 6.2 shows the efficiency simulation results for different input settings, mimicking different PV Cells under different illumination levels. The last column represents the level of matching from the input of the converter to the output of the transducer (PV Cell), and is a figure of merit concerning the maximum power point tracking. It is calculated by taking the ratio between power that actually flows into the converter and the target input power. The overall efficiency is determined by first determining the efficiency during the entire MPPT cycle. During the MPPT cycle the converter is not yet properly matched to the transducer, therefore the efficiency will be lower during the MPPT. Then once the MPP is reached, the efficiency is determined again. The overall efficiency is then deduced as in Equation 6.3, where η_{MPPT} is the average power efficiency during the MPPT cycle, t_{MPPT} is the time the MPPT cycle takes, η_{MPP} is the efficiency at the maximum power point and T_t is the total time one cycle takes before a new MPPT cycle is initiated.

$$\eta = \frac{\eta_{MPPT} \cdot t_{MPPT} + \eta_{MPP} \cdot (T_t - t_{MPPT})}{T_t} \tag{6.3}$$

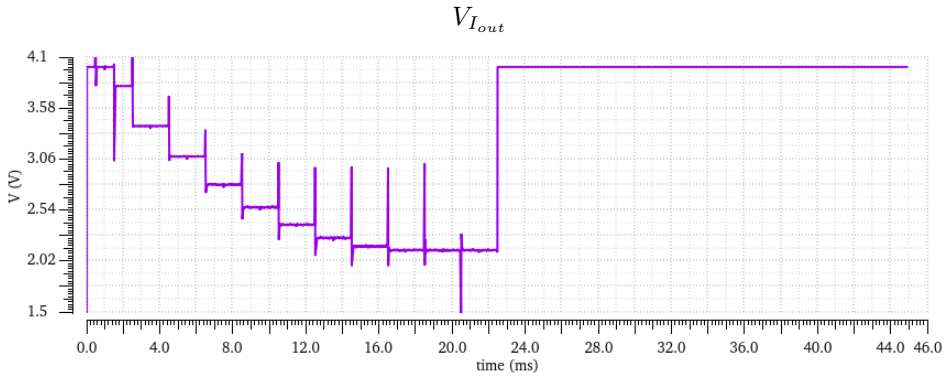
Table 6.2: Efficiency results for different input settings

P_{in} **[mW]**	V_{in} **[V]**	R_{s_in} **[Ω]**	η	**Matching**
25	1	40	52%	97%
125	1	8	87%	100%
125	2	32	83%	98%
250	0.4	0.064	82%	98%
250	1	4	91%	100%
250	3	36	90%	81%
333	1	3	91%	100%

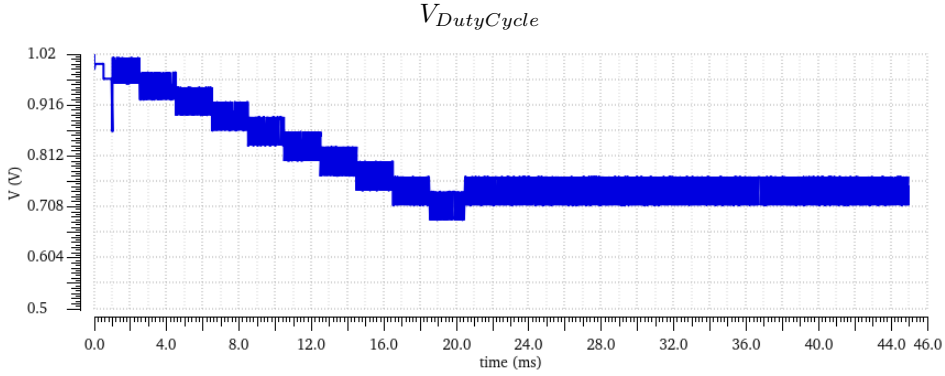
The simulation with $V_{in} = 1V$ and $P_{in} = 250mW$ is featured to demonstrate the process of the maximum power point tracking. Figure 6.3a shows the output voltage of the current measurement block during the MPPT cycle, and thus represents the converter output current. A lower value for this voltage represents a higher output current. It can be seen that once the output current no longer increases after a new duty cycle, the previous duty cycle is set and the Maximum Power Point has been reached.

Figure 6.3b shows how the Duty Cycle Voltage progresses during the MPPT cycle. The duty cycle starts at a high value, such that the MPP will be approached from a low voltage at the input terminal up to the MPP voltage. This ensures that there is no negative current flowing into the PV Cell due to a high forward voltage, making the PV Cell's internal diode conduct.

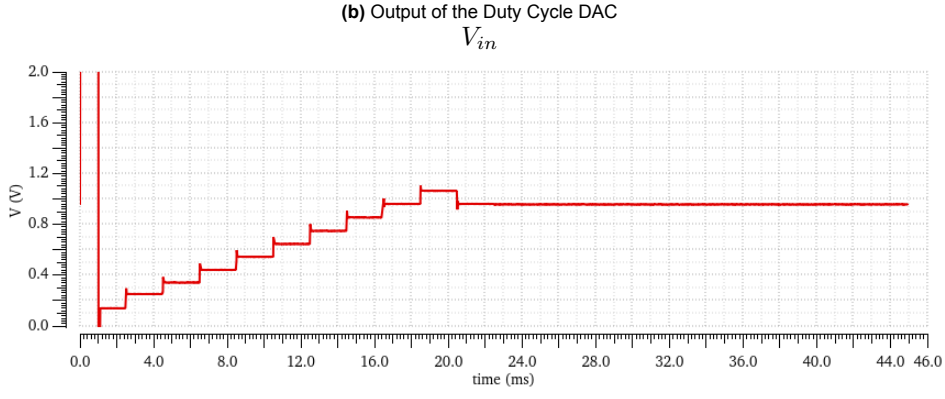
Figure 6.3c demonstrates how the input voltage reacts to the different duty cycles, and eventually matches the MPP input voltage.



(a) Output voltage of the Current Sensor Block



(b) Output of the Duty Cycle DAC



(c) Input voltage to the inductors

Figure 6.3: (a) Output Current Sensor voltage, (b) Duty Cycle voltage representation and (c) Input voltage

Figure 6.4 shows the window-averaged currents going through the inductors. It clearly shows that the currents are not equally distributed over the two inductors. The current through the second inductor hovers around the average output current, and the first inductor carries all the workload. This problem is further discussed in Section 7.2.

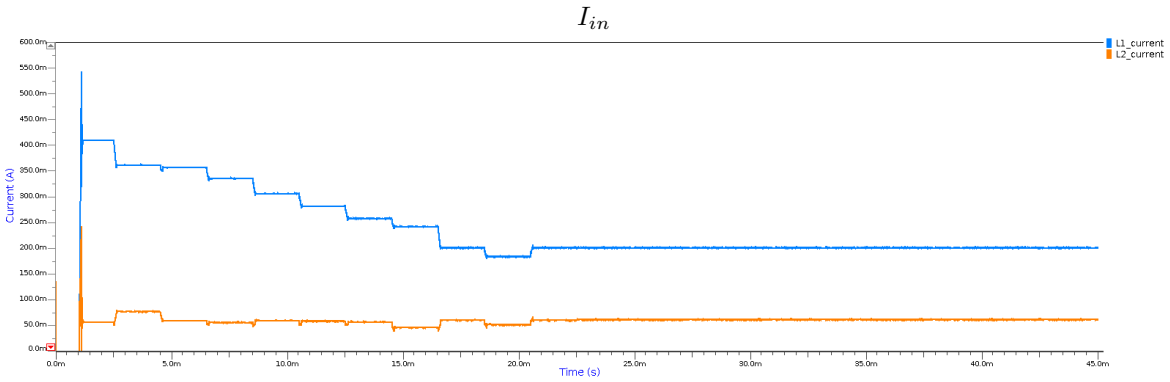


Figure 6.4: Window-averaged currents through inductors L1 and L2 (window of 100μs)

The uneven current sharing also becomes clear when zooming in on the inductor currents at maximum power point operation, as seen in Figure 6.5. It also shows that the current ripple of the second inductor reaches below zero.

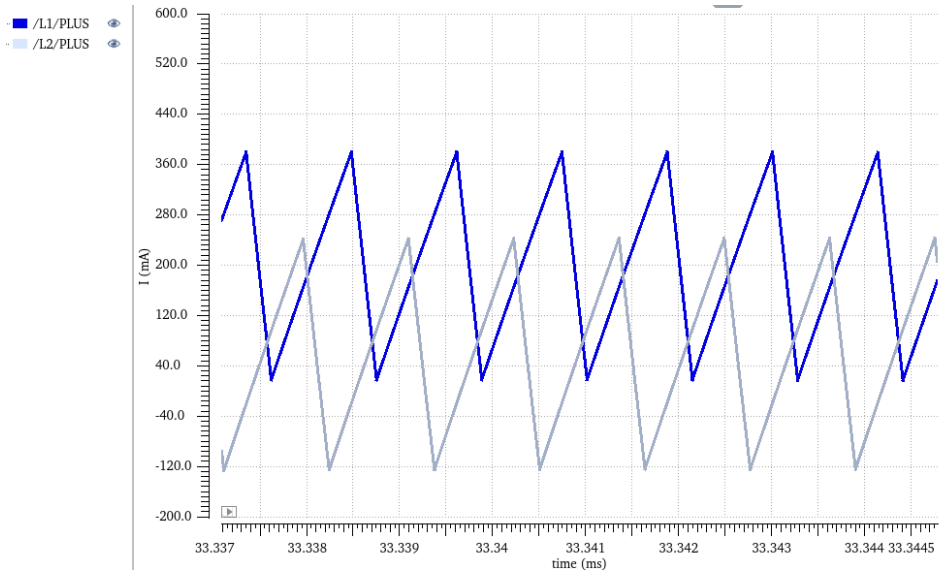


Figure 6.5: Inductor currents at maximum power point

Figure 6.6 shows the window-averaged output current going into the battery. The output current increases, as expected, due to the changing duty cycle, up to the maximum power point. The output current then makes a small increase, as the MPPT block is set to stand-by. This is caused by the deactivation of the current measuring block, that, when activated, diverts a fraction of the output current in order to measure it.

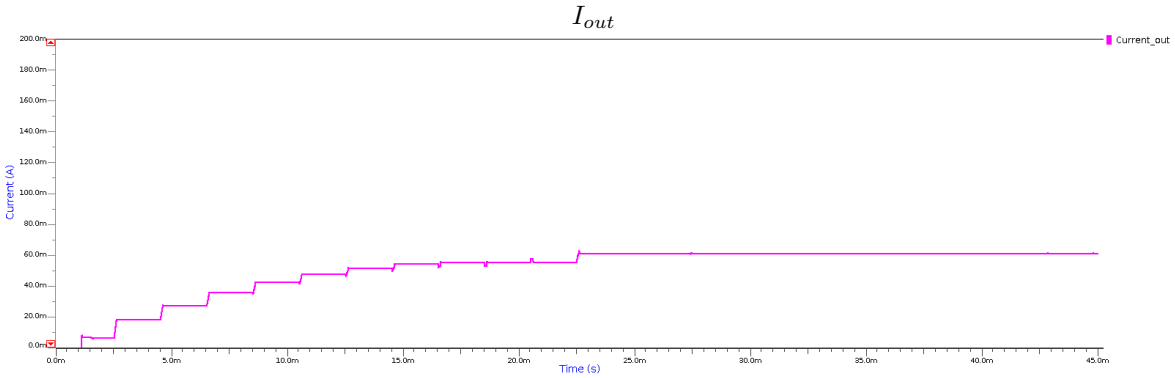


Figure 6.6: Window-averaged output current (window of 100μs)

Figure 6.7 shows the duty cycles of the signals switching the segmented power MOSFETs. The two high duty cycle value signals are controlling the low-side switches, and the two lower duty cycle value signals are controlling the high-side switches. It can be seen that the duty cycles are not equal. There is a discrepancy of around 2% percentage-point between the two duty cycle signals. The cause of the discrepancy is further explored in Section 7.2.

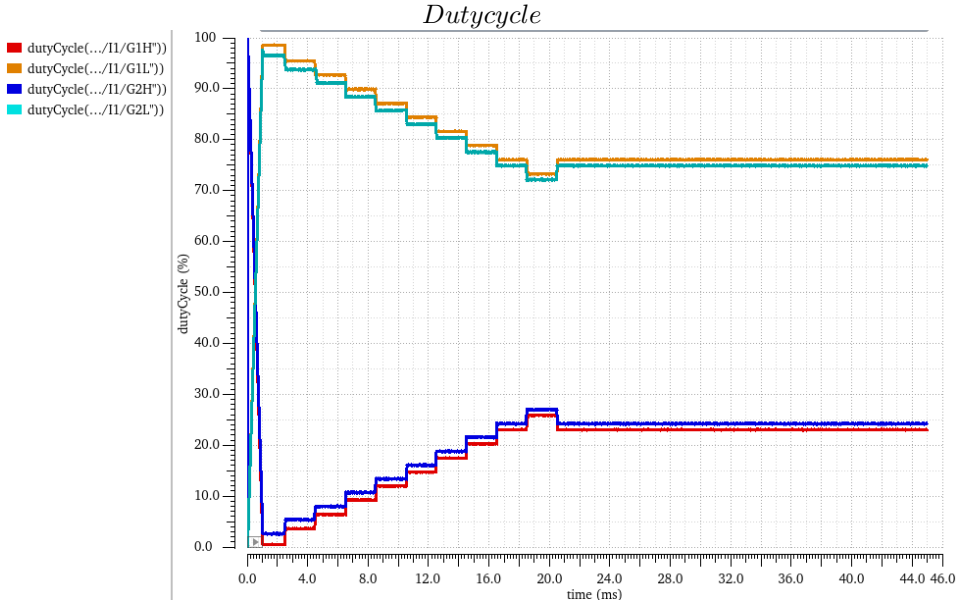


Figure 6.7: Duty Cycle values of power switch signals during- and after MPPT in percentages

Figure 6.8 shows the result of calculating the required number of power switch segments to be activated, in the form of a 3-bit thermometer code. At the maximum power point, the two MSBs representing the duty cycle settle on a 2-bit binary code of '10'. The average output current settles on 61 mA, that corresponds to a binary representation of '11'. Then looking at the truth table in Appendix B, the desired binary output code for Input Current is '10', which translates into the 3-bit thermometer code '011' and corresponds to the result seen in Figure 6.8.

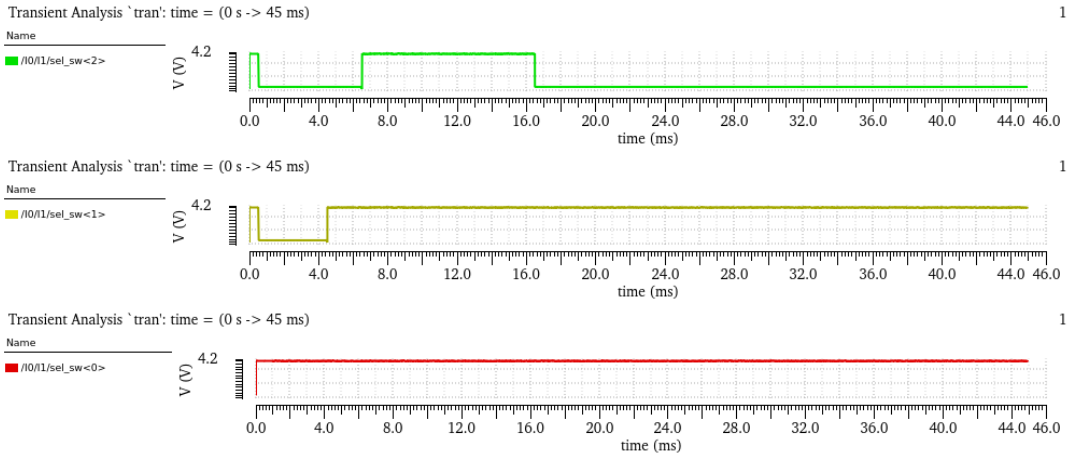


Figure 6.8: 3-Bit thermometer code Segmented Switch Selectors

6.3. Post Layout Simulation

After the design of the layout, the most crucial blocks were extracted in order to be simulated. The Segmented Power Switches were extracted, including their routing, since they are the largest contributor to the losses. Also the Sawtooth-wave generator was extracted, since it can be sensitive to parasitics. A top-level simulation was done with the following input settings: $V_{in} = 1V$, $P_{in} = 250mW$ and $Rs\_in = 4\Omega$. The simulation with the layout-extracted Power Switches and Sawtooth-wave generator resulted in an efficiency of 89%, with a matching of 100%. Unfortunately, a top-level simulation with the complete layout extraction was not possible due to limited time and resources.

7

Discussion

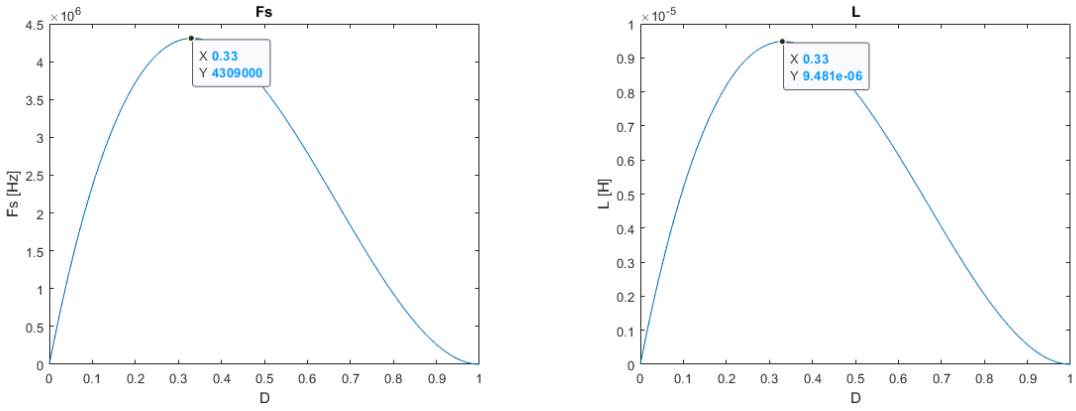
This chapter discusses the energy harvesting interleaved DC-DC converter designed in this thesis. The results from Chapter 6 show that the converter is most efficient in the high power ranges, even beyond the power specifications designed for. At lower input powers the efficiency is strongly degraded. This is partially caused by the increased share of overhead power consumption. For lower input powers, the overhead power consumption stays the same as for higher input powers. In this chapter a closer look is taken to some of the design choices and their implications. Also, some improvements are suggested.

7.1. Converter Conduction Mode

In Section 3.2 the required inductance and switching frequency were determined. The choices made were specifically for the input setting where $P_{in} = 250mW$, $V_{in} = 0.4V$, $V_{out} = 4$ and $D = 0.9$. The chosen inductance and switching frequency ensure operation in CCM for these input settings, however it does not for all input settings as can be seen in the simulation results in Figure 6.5, where the current through one of the two inductors crosses zero ampere in a simulation where the input voltage is 1V and the available input power is 250mW.

When further inspecting the expressions used for calculating the required inductance and switching frequency, the deficiency becomes clear. Equations 3.34 and 3.35 can be plotted as a function of the duty cycle, D. When setting the output power to 250 mW and choosing an inductance of 2.2 μH, the required switching frequency for all duty cycles can be seen in Figure 7.1a. When configuring the interleaved converter to a switching frequency of 1 MHz, the required inductance to ensure CCM for all Duty cycles can be seen in Figure 7.1b.

Increasing the switching frequency to over 4 MHz would require the Sawtooth-wave Generator to also produce a over 4 MHz sawtooth-wave signal. This would require much higher current to be supplied to the Sawtooth-wave generator, as well as to the comparators used in the sawtooth-wave generator, resulting in more power loss. Therefore, it would be better to choose a different inductor with an inductance of 10μH. A different inductor might cost more or take up more space, however.



(a) Required switching frequency for an inductance of 2.2μH as a function of duty cycle

(b) Required inductance for a switching frequency of 1MHz as a function of duty cycle

Figure 7.1: CCM requirements as a function of duty cycle

For lower output powers, the average input current will be smaller and the switching frequency and inductance requirements to ensure CCM will be stretched even further. Therefore it can be interesting to explore the option of implementing a variable switching frequency. The switching frequency should increase when a small input current is available. Conduction losses in the power switches will be low. Therefore a small power switch can be selected, such that the gate-charge loss is small as well. That would allow the switching frequency to be increased to ensure CCM.

7.2. Uneven Current Sharing

The results from the toplevel circuit simulations showed that the average current distribution across the two inductor branches was not equal. A discrepancy in duty cycle for the switching signal for the two inductor branches was observed. Some further investigation was done on the possible causes of these problems. Since the output voltage of the converter is fixed by the battery, and the input voltage is the same for both the inductor branches since these nodes are tied together, a difference in duty cycle for the different branches can only manifest itself in an uneven current sharing. A simulation experiment with an ideal interleaved boost converter showed that a duty cycle difference of 1 percentage point results in a deviation from the intended average inductor current of 75%. Literature also confirms a slight difference in duty cycle can be catastrophic for the current sharing [30, 31]. Another less influential cause of uneven current sharing is deviations in component values like the inductor ESR for the different branches.

A transient simulation of the input signals to the Duty Cycle Generator is shown in Figure 7.2a. It can be seen that there is a large capacitive coupling between the output and the input of the comparator, especially onto the D_comp signal in red. It takes some time for the signal to recover, but before the signal is fully recovered, another comparison is made to the phase-shifted sawtooth-wave, resulting in a different duty cycle. A capacitor of 1 pF was added to the output of the Duty Cyle Digital-to-Analog converter, that connects to the input of the PWM generator. It is important that the buffer at the output of the DAC is able to drive this extra capacitive loading in the time that is available. The effect of adding the capacitor is shown in Figure 7.2b. The ripple in the D_comp signal is reduced from 16 mV to only 1 mV.

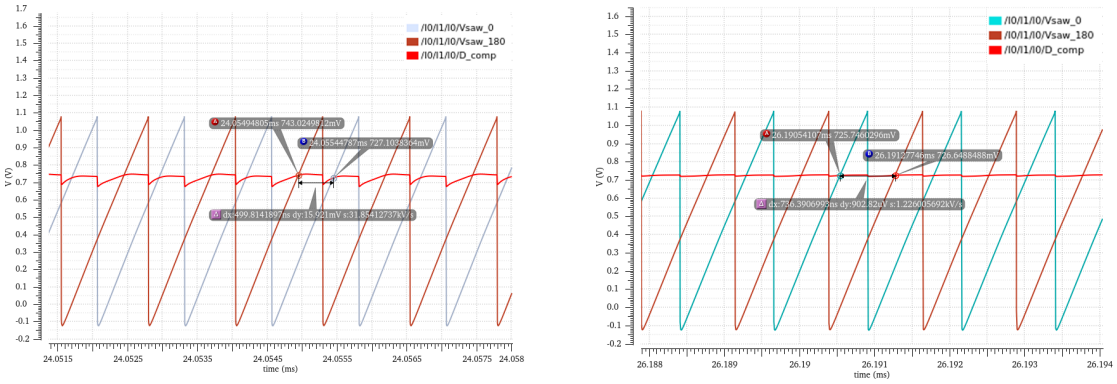


Figure 7.2: Duty cycle generator comparison (a) without input capacitor and (b) with input capacitor

Another top level simulation was done with the added capacitor. Figure 7.3 shows the currents through the inductors after adding the capacitor. Figure 7.4 shows the duty cycles of the signals controlling the power switches. As can be seen, there is no longer a notable discrepancy between the two duty cycle signals, resulting in equal current sharing. A top level simulation with the added capacitor was done for two different input settings shown in Table 7.1. They both show an overall efficiency improvement of 1 percent point.

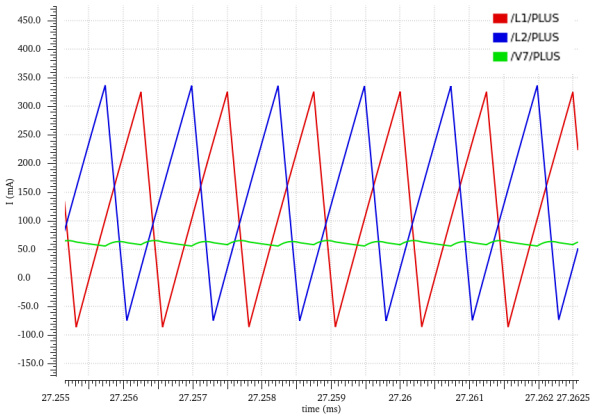


Figure 7.3: Inductor currents after adding decoupling capacitor

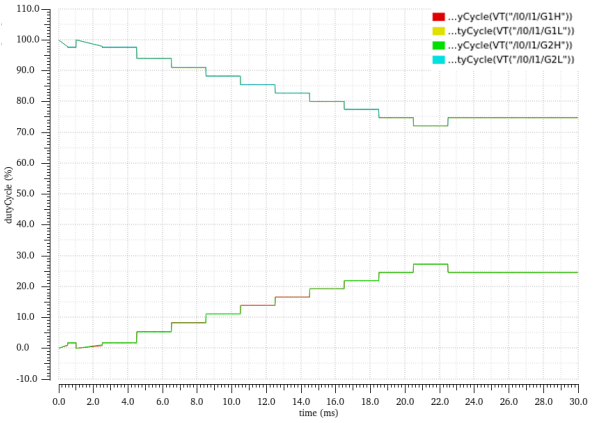


Figure 7.4: Duty cycles after adding decoupling capacitor

Table 7.1: Efficiency results top level simulation with added capacitor

P_{in} **[mW]**	V_{in} **[V]**	R_{s_in} **[Ω]**	η	**Matching**
250	0.4	0.064	83%	100%
250	1	4	92%	100%

7.3. Output Current Sensing

In the current design, the scaling down of the current that is mirrored from the output current is limited. It would be beneficial to scale down the mirrored current further, to reduce conduction losses in the measuring path. The scaling down is limited by the current that is required at the output of the Current Sensing block to drive its capacitive load. The capacitive load is made up of the sample capacitor from the Sample-and-Hold block and the inputs to the three comparators in the Segmented Switch ADC. A buffer could be added to the output that would take over the driving requirements. The mirrored current could then be scaled down much more, reducing the conduction losses in the MOSFETs in the Current Sensing block and also reducing the large size requirement for these MOSFETs.

During the simulations it was noted that the output voltage of the Current Sensing block can reach below 2 volts. This means there is an inaccuracy in the representation of the output current. This issue will not be a problem for the functionality of the MPPT, since this MPPT only depends on changes in the output current. However, it will cause inaccuracy in the representation of the output current as interpreted by the Switch Segmentation Controller. The output transresistance of the Current Sensing block needs to be recalibrated to keep the output voltage stay in range of the specification in order to accurately represent the output current. This issue also reveals the vulnerability of the output resistor in terms of process variation. A variation in output resistance causes a direct inaccuracy of the output current representation. This problem strengthens the call for further decreasing the mirrored current, such that the output resistor will be larger. When a large resistor is used, the impact of process variations on the output error will be less, due to smaller variations in resistor value, percentage-wise.

7.4. Sawtooth Wave Generator

As seen and described in Figure 4.18 in Section 4.7.1, the sawtooth wave phase difference between Wave 1 and Wave 2 is not a perfect 180 degrees. The error in phase difference causes the sawtooth waves to be compared to the duty cycle reference voltage at a different interval from the previous comparison. As described in Section 7.2, the waves will be compared to a slightly different value of the reference voltage, since it needs some settling time. This results in a small error in duty cycle at the output of the PWM generator. It can be difficult to realise an exact phase difference of 180 degrees. A possible solution is a cross-coupled resetting structure, where both generators reset each other when it reaches half the full-scale voltage to establish a 180 degree phase difference between the two waves. Since it is difficult to implement an absolute 180 degree phase shift in an analog fashion, it would be interesting to see if there are possible digital implementations of a PWM signal generator with adjustable duty cycle. Especially if the converter and connected battery are deployed to power a micro-controller.

7.4.1. Process variation

The Wave Generator circuit is prone to process variation. The frequency of the sawtooth waves depends on capacitor size, charging current and proper comparator switching. All three of these mechanisms can be influenced by process variation. Therefore, it might be beneficial to implement a controllable capacitor charging current, to manually compensate the frequency for possible process variations. The Monte-carlo analysis shows that the frequency of the sawtooth waves over different process variations is below the intended 1 MHz. Therefore, the generator needs to be re-calibrated to increase the frequency up to 1 MHz.

7.4.2. Kick-Back

The 1-volt reference voltage source used in the Sawtooth Wave Generator to compare the sawtooth-wave capacitor voltages to, is also used as a source for the Duty Cycle Counter Digital-to-Analog Converter. The Wave Generator comparators might introduce some kick-back onto the 1 volt reference voltage line. This could cause disturbance in the DACs output values. A capacitor can be added between the 1-volt reference voltage and ground, to catch the voltage peaks caused by the comparator kick-back.

7.5. Segment Control

A large part of the resolution is lost when truncating the 5-bit duty cycle code to a 2-bit code. This results in a large possible error in the calculated input current. For example, from the 2-bit calculation the maximum input current is only 250mA, but the actual total input current can go up to 625mA. This also demonstrates the imperfect mapping of input current into the four segments to be represented by a 2-bit binary code.

When little power is available at the input, the impact on the efficiency by selecting too many power switch segments can be detrimental. This was also seen in the top level simulation where 25mW of input power was available with $V_{in} = 1V$ and $Rs\_in = 40\Omega$. The total input current was a mere 30mA, but due to the 2-bit representations of the duty cycle ($D_{actual} = 0.79$ which is represented as '11') and the output current ($I_{out\_actual} = 3.8mA$ which is represented as '00') the calculated input current was represented as '01' translating to a total selection of two segments. Though, only one segment should have been selected for such a low input current.

It should be possible to retain the information stored in the 5-bit duty cycle code. A Karnaugh map can be generated with 7 variables in total (5 bits for the duty cycle and 2 bits for the output current), with a total of $2^5 \cdot 2^2 = 128$ entries. The deduction of the logic function from this Karnaugh map will be quite complicated. More convenient might be to create a verilog code that can be translated to a combination of logic gates to implement the function to calculate the input current. Another possibility is to implement a decoder that converts the 5-bit duty cycle code to a 2-bit code, but instead of taking the two MSBs, the entire 5-bit value is assigned to a more representable 2-bit value. The 2-bit values could, for example, represent the following duty cycle values: '00'= 0.2, '01'= 0.4, '10'=0.6 and '11'=0.8.

7.5.1. Analog-to-Digital Converter

The reference voltages used in the ADC show to be prone to kick-back noise from the comparators, as seen by the peaks on the reference voltages plotted in Figure 5.7a. This can be a cause of faulty decisions by the comparator, since a comparison to a faulty reference voltage is made. Adding capacitors between the reference voltages and ground will reduce this problem, by damping kick-back voltage peaks.

8

Conclusion

The goal of this master thesis was to design a DC-DC Converter that can harvest a power of up to 250 mW with an efficiency of 85%, to optimally harvest the energy from a photovoltaic cell to charge a battery while keeping the required footprint on the PCB within bounds. A maximum power point tracking strategy was implemented to maximize the efficiency. The power switches used in the converter are segmented, in order to efficiently transfer energy over a broad range of input powers.

8.1. Overview

At the start of the project, a set of specifications was composed. The wish for a high efficiency, high power energy harvesting DC-DC converter became apparent. In energy harvesting, higher powers usually can only be supplied by transducers of mechanical energy or photovoltaic cells. The scope of the project was confined to the use of photovoltaic cells as energy harvesting sources, since mechanical sources offer AC voltages and would require extra steps to convert from AC to DC. Photovoltaic cells deliver energy at a DC voltage that can range from as low as 0.4V up to very high voltages when multiple PV cells are connected in series. When connected in parallel, PV cells add up their induced currents. High electrical powers can be generated when multiple PV cells are connected either in series or in parallel.

An exploration was done on different types of DC-DC converters. The sources of loss for different types of converters were determined. The inductive boost converter was selected as a starting point, due to its flexibility in configuring conversion ratios and its tolerance for high currents as apposed to a capacitive converters that inherently require very large capacitors when processing high currents. Also the limited amount of voltage conversion ratios in capacitive converters is a reason to favour the inductive converter, in order to efficiently convert a broad power range. With the recognition of the sources of loss in the boost converter, the conduction loss was found to be the largest contributor at high currents. The interleaved boost converter topology was chosen for its lower average current as well as lower ripple current in order to reduce conduction losses.

The requirements for the inductors used in the interleaved boost converter were determined, and different types of inductors were researched. A selection of adequate inductors was picked, with a priority on a high ESR to inductance ratio, small size and low pricing.

With the help of the Finite-state Machine designed by Nowi, the maximum power point tracking circuit was designed. The output current is measured and tracked. The duty cycle controlling the power switches is increased by one step, and the new measured output current is compared to its previous value. A higher current equates to a higher power, therefore, the cycle of increasing the duty cycle and comparing the output current to its previous value is repeated until the output current no longer increases. At that point the maximum power point of the PV cell is reached.

In order to perform efficiently at a lower input power, segmented power switches were designed and implemented. The switch segmentation controller uses information that is already available from the

maximum power point tracking to roughly determine the input current. The number of switch segments are selected according to the determined input current. For a low input current, few segments are selected, and for a high input current, all the segments are selected to be switched.

All the sub-blocks were simulated individually as well as combined to test their functioning and whether the specifications were met. Hereafter, top level schematic simulations were performed for several input power settings. A layout design was made, in order for it to be tape-out ready. The layout design was extracted. Top level simulation was performed with the extracted Segmented Power Switches and Sawtooth Wave Generator key sub-circuits. After the layout design, a quick fix to the kick-back noise from the duty cycle generator was added to improve the two duty cycle PWM signals. With this improvement another two top level schematic simulations were executed.

8.2. Results

The proposed interleaved boost converter has achieved a conversion efficiency of up to 92% in top level schematic simulation. In layout extracted simulation an efficiency of up to 89% is achieved. A matching of available power to harvested power of 99.95% is achieved by tracking the maximum power point.

8.3. Contributions

The following list gives an overview of contributions made to the field of energy harvesting:

- The design and implementation of an energy harvesting DC-DC converter with Maximum Power Point Tracking suitable for a broad input power range of 25mW up to 250mW.
- Design of a low power sawtooth wave relaxation oscillator.
- Novel strategy of determining input current without requiring an extra measuring circuit

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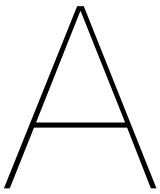

Segment Calculation Table

D<0:4>	D	D<3:4>	D	$I_o < 0:1 >$	$I_o min$	$I_o max$	$I_i[mA]$	$I_L[mA]$	$I_i < 0:1 >$	$I_i actual$	$I_{La}ctual$	$I_i error$
00000	0	00	0	00	0	15,63	15,63	7,815	00	15,63	7,815	0
00001	0,03125	00	0	01	15,63	31,25	31,25	15,625	00	32,25806	16,129032	1,008065
00010	0,0625	00	0	10	31,25	46,88	46,88	23,44	00	50,00533	25,002667	3,125333
00011	0,09375	00	0	11	46,88	62,5	62,5	31,25	01	68,96552	34,482759	6,465517
00100	0,125	00	0			62,5	62,5	31,25		71,42857	35,714286	8,928571
00101	0,15625	00	0			62,5	62,5	31,25		74,07407	37,037037	11,57407
00110	0,1875	00	0			62,5	62,5	31,25		76,92308	38,461538	14,42308
00111	0,21875	00	0			62,5	62,5	31,25		80	40	17,5
01000	0,25	01	0,25	00	0	15,63	20,84	10,42	00	20,84	10,42	0
01001	0,28125	01	0,25	01	15,63	31,25	41,66667	20,83333	00	43,47826	21,73913	1,811594
01010	0,3125	01	0,25	10	31,25	46,88	62,50667	31,25333	01	68,18909	34,094545	5,682424
01011	0,34375	01	0,25	11	46,88	62,5	83,33333	41,66667	01	95,2381	47,619048	11,90476
01100	0,375	01	0,25			62,5	83,33333	41,66667		100	50	16,66667
01101	0,40625	01	0,25			62,5	83,33333	41,66667		105,2632	52,631579	21,92982
01110	0,4375	01	0,25			62,5	83,33333	41,66667		111,1111	55,555556	27,77778
01111	0,46875	01	0,25			62,5	83,33333	41,66667		117,6471	58,823529	34,31373
10000	0,5	10	0,5	00	0	15,63	31,26	15,63	00	31,26	15,63	0
10001	0,53125	10	0,5	01	15,63	31,25	62,5	31,25	01	66,66667	33,333333	4,166667
10010	0,5625	10	0,5	10	31,25	46,88	93,76	46,88	01	107,1543	53,577143	13,39429
10011	0,59375	10	0,5	11	46,88	62,5	125	62,5	10	153,8462	76,923077	28,84615
10100	0,625	10	0,5			62,5	125	62,5		166,6667	83,333333	41,66667
10101	0,65625	10	0,5			62,5	125	62,5		181,8182	90,909091	56,81818
10110	0,6875	10	0,5			62,5	125	62,5		200	100	75
10111	0,71875	10	0,5			62,5	125	62,5		222,2222	111,11111	97,22222
11000	0,75	11	0,75	00	0	15,63	62,52	31,26	01	62,52	31,26	0
11001	0,78125	11	0,75	01	15,63	31,25	125	62,5	10	142,8571	71,428571	17,85714
11010	0,8125	11	0,75	10	31,25	46,88	187,52	93,76	11	250,0267	125,01333	62,50667
11011	0,84375	11	0,75	11	46,88	62,5	250	125	11	400	200	150
11100	0,875	11	0,75			62,5	250	125		500	250	250
11101	0,90625	11	0,75			62,5	250	125		666,6667	333,33333	416,6667
11110	0,9375	11	0,75			62,5	250	125		1000	500	750
11111	0,96875	11	0,75			62,5	250	125		2000	1000	1750

B

Segment Calculation Truth Table

D<4>	D<3>	I_o<1>	I_o<0>	I_i<1>	I_i<0>	sw<2>	sw<1>	sw<0>
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	1	0	0	1
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	0	1	0	0	1
0	1	1	1	0	1	0	0	1
1	0	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	1
1	0	1	0	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	0	0	1	0	0	1
1	1	0	1	1	0	0	1	1
1	1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	1	1