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Investigation on fabrication of silicon nanopores using an electrochemical passivation etch-stop strategy

Hao Hong[1,2], Xin Lei[3], Jiangtao Wei[2], Wenjun Tang[4], Minjie Ye[2], Jianwen Sun[2], Guoqi Zhang[1]✉, Pasqualina M. Sarro[1]✉ and Zewen Liu[2]✉

Abstract

The three-step wet etching (TSWE) method has been proven to be a promising technique for fabricating silicon nanopores. Despite its potential, one of the bottlenecks of this method is the precise control of the silicon etching and etch-stop, which results in obtaining a well-defined nanopore size. Herein, we present a novel strategy leveraging electrochemical passivation to achieve accurate control over the silicon etching process. By dynamically controlling the oxide layer growth, rapid and reliable etch-stop was achieved in under 4 s, enabling the controllable fabrication of sub-10 nm silicon nanopores. The thickness of the oxide layer was precisely modulated by adjusting the passivation potential, achieving nanopore size shrinkage with a precision better than 2 nm, which can be further enhanced with more refined potential control. This scalable method significantly enhances the TSWE process, offering an efficient approach for producing small-size silicon nanopores with high precision. Importantly, the precise etching control facilitated by electrochemical passivation holds promise for the cost-effective production of high-density, air-insulated monolithic integrated circuits.

Introduction

The concept of biological nanopores for nucleic acid sensing was first introduced in the 1990s[1]. Since then, solid-state nanopores have emerged as a transformative platform for biomolecule detection, owing to their mechanical robustness, ability to functionalize surfaces using organic or inorganic treatments, and seamless integration with nanofluidic devices[2]. These attributes have made solid-state nanopores pivotal tools for detecting proteins, and DNA[3,4]. Traditional detection mechanisms rely on electrokinetic forces for molecule translocation, producing a blockade current[5]. However, these approaches are often limited by low temporal resolution and inconsistent blockade signals. A critical challenge in advancing nanopore sensing lies in slowing the translocation speed and improving the signal-to-noise ratio. To address these limitations, various strategies have been developed, including the use of protein motors[6], ionic liquids[7], and sequential DNA unzipping[8]. Additionally, electrical and optical dual-sensing approach has made a remarkable complement to molecule detection[9].

Beyond molecule detection, solid-state nanopores have found diverse applications, such as DNA-based information storage[10], nanopore batteries[11], nanopower generators[12,13], ionic rectification[14,15], and nanostencil lithography[16]. Despite their versatility, different applications often demand specific materials, fabrication methods, and analytical techniques. Following the discovery of two-dimensional materials, the range of materials used for solid-state nanopores has expanded beyond traditional choices such as silicon[17,18], oxides[19,20], and nitrides[21–23], to include graphene[24,25], MoS_2[26,27], and carbon nanotubes[28,29].

Common fabrication methods for solid-state nanopores include focused ion beam/ transmission electron microscopy (FIB/TEM)[30], controlled dielectric breakdown

Correspondence: Guoqi Zhang (g.q.zhang@tudelft.nl) or Pasqualina M. Sarro (p.m.sarro@tudelft.nl) or Zewen Liu (liuzw@tsinghua.edu.cn)
[1]Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands
[2]School of Integrated Circuits, Tsinghua University, 100084 Beijing, China
Full list of author information is available at the end of the article

(CBD)[31–33], and nanoimprinting[34,35]. However, these techniques face limitations, for instance, FIB/TEM processes suffer from low throughput and require expensive equipment, while CBD often results in the formation of multiple nanopores[36,37]. In contrast, the TSWE method is inherently compatible with semiconductor processes and MEMS technologies, enabling cost-effective and scalable production. Furthermore, the unique semiconductor properties of silicon allow straightforward surface modifications and the integration of gate structures, enabling the tailoring of nanopore physical and electrical properties for diverse applications[38,39]. Owing to these advantages, the TSWE method, based on anisotropic chemical wet etching, has emerged as a promising technique for the fabrication of silicon nanopores.

Despite its strengths, the TSWE method still faces bottlenecks in the precise control of the silicon etching and etch-stop during the fabrication process, which are critical for the controllable and scalable fabrication of silicon nanopores. Such precision and etch-stop not only enable scalable and controllable fabrication of silicon nanopores, but also play a crucial role in tailoring nanopore size and geometry, thereby enhancing resolution in nanopore sensing and improving energy conversion efficiency in nanopore-based power generation. Efforts to address these limitations include using crystal-orientation-based anisotropic etching of silicon, as demonstrated by Shuang et al., who utilized slow etching of the (111) crystal plane to achieve sub-5 nm nanopores[18]. However, due to the lack of an effective real-time monitoring strategy during the etching process, the reproducibility of the nanopore sizes remains a significant challenge. Meanwhile, Yang et al. employed photoinhibition-assisted KOH etching to reduce the etching rate, enabling precise control over silicon etching[40]. Despite its effectiveness, the complexity of the required optical setup makes it difficult to implement for scalable, high-throughput fabrication. Other approaches, such as manual or automated separation of the chip and etchant[41,42], and the use of resist[43], have also been explored to achieve rapid etch-stop, but still face challenges regarding process stability and scalability. As a result, there remains a pressing need for accessible, semiconductor-compatible methods that enable precise control over the silicon etching process and etch-stop, ultimately facilitating the scalable and controllable fabrication of silicon nanopores. Addressing this gap will be critical to advancing the field and broadening the applications of solid-state nanopores.

Here we propose an etch-stop strategy leveraging electrochemical passivation to enable the controllable fabrication of silicon nanopores. This approach not only provides a reliable controllable fabrication method due to the effective etch-stop mechanism, but also allows scalable and cost-effective production owing to the compatibility of the semiconductor processes and MEMS technologies. By regulating the electrochemical potential during the silicon etching process, the growth of an oxide layer can be precisely controlled, allowing regulation of the silicon etching rate. Once an appropriate potential is applied, oxide growth dominates the etching process, leading to the formation of an insulating oxide layer that effectively halts etching. The negligible etching rate of the formed oxide ensures that the nanopore size remains nearly constant in the subsequent etching process. The thickness of the oxide layer can be finely regulated through adjustments to the passivation potential and passivation duration, enabling precise shrinkage of the nanopore sizes. This approach facilitates the reproducible fabrication of silicon nanopores using the TSWE method. Furthermore, the reversible modulation of silicon etching by electrochemical potential offers a robust pathway for high-precision fabrication of silicon-based structures and devices, paving the way for advancements in nanoscale engineering and semiconductor applications.

Result and discussion

Effect of boron doping on silicon etching

It has been reported that the silicon etching rate in the KOH solution starts to decrease at a boron concentration of approximately $2.0 \times 10^{19}\,cm^{-3}$ and the reduced etching rate benefits the precise control of silicon etching[44–47]. This phenomenon of the decelerated silicon etching rate was confirmed in this study, and its underlying mechanism was discussed. Figure 1a exhibits the boron concentration of different silicon samples characterized by TOF-SIMS. The samples, with boron implantation densities of 2.0×10^{15}, 1.7×10^{15}, and $1.4 \times 10^{15}\,cm^{-2}$ at an energy of 50 keV, resulted in boron concentration of 1.0×10^{20}, 7.5×10^{19}, and $2.5 \times 10^{19}\,cm^{-3}$, respectively. The boron concentration of the original silicon substrate (1–10 Ω·cm) is $1.0 \times 10^{16}\,cm^{-3}$. The implantation energy controls the effective implantation depth, while the density determines the ion concentration within the target region.

The Arrhenius plot of the etching rates for these samples is shown in Fig. 1b. The results demonstrate that for all samples, the etching rate increased with rising temperature. However, samples with higher boron concentrations exhibited significantly lower etching rates. This behavior can be attributed to the following mechanisms. The Fermi level drops into the valence band due to the heavy boron-doped, inducing a sharp shrinkage of the space charge layer (SCL). This leads to an equivalent narrowing of the potential well given by the downward bending of the energy bands on the silicon surface. As a result, electrons, generated from an oxidation reaction, injected into the conduction band

cannot be confined and easily tunnel through the SCL into the deeper regions of the silicon. The high hole concentration in the heavy boron-doped silicon promotes electron-hole recombination, thereby depleting the electrons available for subsequent reduction reactions and further impeding the silicon etching reaction. Alternatively, the phenomenon can also be explained by a strain model. The density of surface defects increases above the intrinsic surface defect density for the heavy B-doped, facilitating the formation of the passivation that halts the etching reaction[48,49]. Additionally, the activation energy (*E*a), as determined from the Arrhenius equation ($R = Ae^{-E_a/KT}$), increases with the higher boron concentration, indicating that the etching reaction is suppressed.

Effect of electrochemical potential on silicon etching

A silicon wafer with a boron concentration of 3.5×10^{19} cm^{-3} was utilized for electrochemical passivation and silicon nanopore fabrication. This sample can not only facilitate the accurate control of the etching process due to its lower etching rate compared to lightly boron-doped silicon but also enable an ohmic contact to conduct the electrochemical passivation (Fig. S1, Supporting Information).

The electrochemical potential was applied to the silicon during the etching process to achieve precise regulation of the silicon etching process. Figure 2a exhibits the corresponding current-potential curves obtained from linear scan voltammetry. The measurement starts at −1.35 V and scans positively at a rate of 1 mV/s. The open-circuit

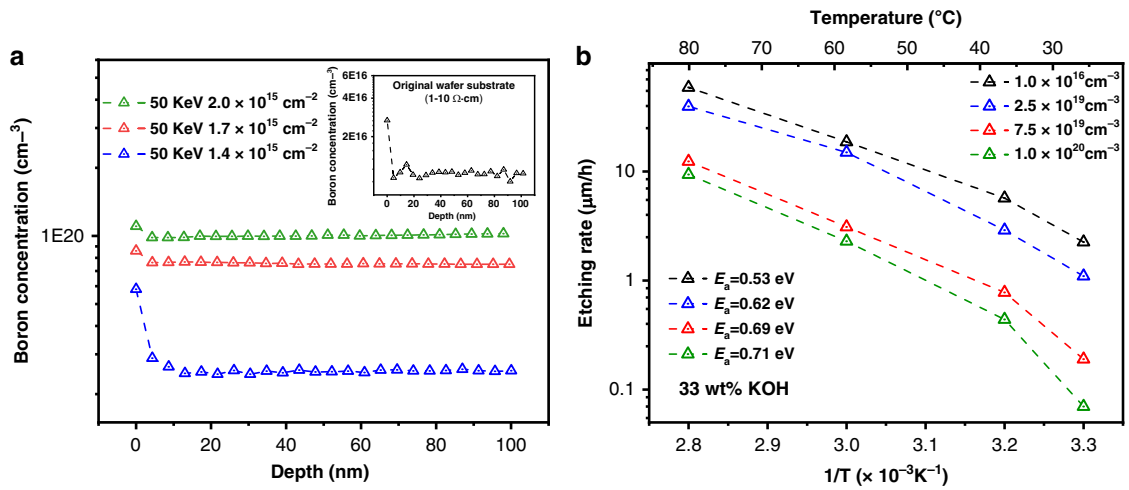

Fig. 1 Etching rate of silicon with different boron concentrations. a Boron concentration of different samples produced with distinct boron implantation parameters. **b** Arrhenius diagram of the silicon etching rate for various boron concentrations

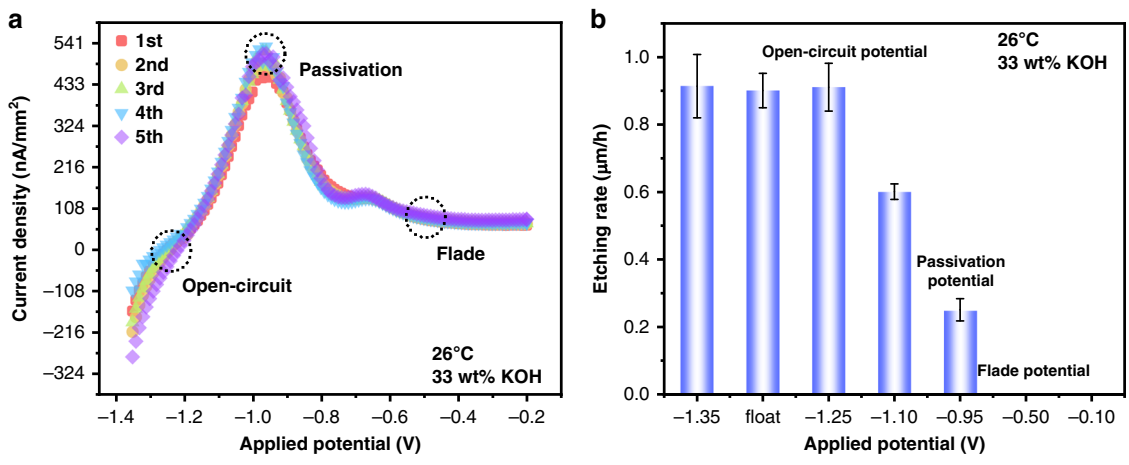

Fig. 2 Effect of the electrochemical potential on the silicon etching. a Current-potential curves obtained from linear scan voltammetry during the silicon etching process. **b** Silicon etching rates related to different applied potentials

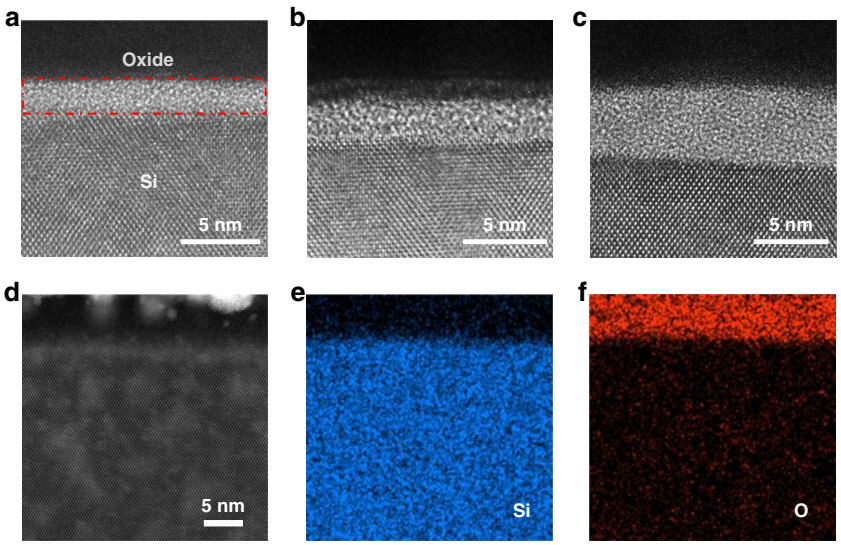

Fig. 3 Characterization of the oxide layer formed during the passivation process. Cross-sectional TEM image of the formed oxide after 1 h passivation with a potential of (**a**) 1.5 V, (**b**) 2.5 V, and **c** 3.5 V. **d** STEM images of the formed oxide and corresponding EDS elemental mapping of (**e**) Si and (**f**) O

(OCP), passivation (PP), and Flade potential (FP) for this sample were determined to be −1.25, −0.95, and −0.50 V by repeated measurements. As the potential scans positively, the current transitioned from cathodic to anodic at the OCP, where no net charge transfer occurs, resulting in a near-zero current.

Beyond the OCP, the anodic current increased with the potential, driving oxide growth on the silicon surface in contact with the etchant, reducing the silicon etching rate. Further potential increases will facilitate the formation of an oxide layer covering the silicon surface and lead to a sudden current drop at the PP. A stable oxide layer forms at the Flade potential, where the current stabilizes at a minimal but nearly constant value due to the insulating effect of the passivation layer. The established oxide layer provides a practical approach to realize the etch-stop for silicon. Additionally, the formation process of the oxide/passivation layer once the potential beyond the FP is defined as a passivation process. It can be predicted that the silicon etching rate can be regulated by the variation in the oxide growth during the etching process.

To ascertain the effect of applied electrochemical potentials on the silicon etching rate. Figure 2b illustrates the silicon etching rates under different applied potentials. While the silicon etching rates remained approximately equal (~0.90 μm/h) at potentials of −1.35 and −1.25 V (OCP), as well as in float condition (no applied potential), the cathodic current was only observed at −1.35 V. This cathodic current regarding −1.35 V will be served as a basis for determining whether the oxide was being etched off in the subsequent experiment. As the potential further increased, the growth of the oxide was gradually dominant and resulted in a reduction in the silicon etching rate (both at −1.10 V and the PP). It's worth noting that the decreasing silicon etching rate culminated in an etch-stop at Flade potential and the same phenomena can be observed at a more anodic potential (−0.10 V). It can be concluded that when the applied potential exceeds the Flade potential, the etch-stop will invariably remain due to the oxide layer formed during the passivation process.

To confirm the nature of the oxide formed during the passivation process, an in-situ characterization of the oxide layer was carried out. Figure 3a, b, and c show the cross-sectional TEM images of the oxide layer following 1 h passivation at potentials of 1.5, 2.5, and 3.5 V, respectively. Uniform oxide layers were observed to fully cover the silicon surface, with thicknesses of 2.5, 3.6, and 5.2 nm corresponding to passivation potentials of 1.5, 2.5, and 3.5 V, respectively. The elevated passivation potential notably promoted the formation of a thicker oxide layer. It's worth noting that the slight divergence (less than 2 nm) in oxide thickness caused by 1 V highlights the capability of realizing precise control over the passivation layer thickness, which enables precise regulating of the nanopore size through the oxide layer.

Figure 3d–f depicts the atomic resolution high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM) image of the formed oxide, along with the corresponding EDS elemental mappings. The two-layer structure visible in Fig. 3d aligns with the TEM findings, and the white granule is Pt which was deposited to cover the formed oxide as a protective layer. The elements of silicon (shown in blue) and oxygen (shown in red) are distributed homogeneously in the

lower and upper layers, respectively. It can be evidenced that the oxide formed by electrochemical passivation primarily consists of SiOx.

Given that silicon oxide exhibits a significantly lower etching rate in KOH solution compared to silicon, even a thin oxide layer effectively delays etching, thereby providing a reliable etch-stop mechanism. Furthermore, atomic force microscopy (AFM) images of oxide layers formed by electrochemical passivation and thermal oxidation (Supplementary Fig. S2, Supporting Information) suggest that the oxide formed through electrochemical passivation has a less dense structure. This observation indicates that the chemical stability of the passivated oxide layer is inferior to that of thermally grown oxide.

In-situ characterization of the formed oxide confirmed that a stronger passivation potential leads to a thicker oxide layer. To elucidate the relationship between passivation and oxide formation, etch-back measurements were performed. Figure 4a–c illustrates the scanning current-potential curves (red lines) during passivation from −1.4 V to final potentials of 1.5, 2.5, and 3.5 V (scanning rate: 1 mV/s) alongside the corresponding etch-back time-current curves (green lines). The current-potential profiles exhibit similar trends of the current, with characteristic potentials (OCP, PP, and FP) aligning with those in Fig. 2a. Notably, a sharp current increase occurs beyond ~2.1 V. It can be speculated that after the establishment of a certain oxide layer thickness, the growth rate of the oxide no longer increases proportionally with the gradually increasing potential due to the insulating effect of the existing oxide layer. This leads to only a marginal increase in oxide thickness even as the potential continues to rise. Eventually, the continuously increasing potential may exceed the dielectric strength of the oxide, resulting in local dielectric breakdown and a sudden rise in leakage current, without a corresponding increase in oxide thickness.

After passivation, etch-back measurements were conducted by applying a fixed potential of −1.35 V to etch the formed oxide. During the initial etching stage, the current remains low induced by the insulating nature of the oxide. The slow etching of the oxide continues until the depletion, at which point the current transitions to a cathodic regime. This point was identified as a symbol of the depletion of the oxide, and the cathodic current corresponding to −1.35 V also ascertained the switch from oxide etching to silicon etching. The etch-back time, defined as the duration to deplete the oxide layer, was measured as 2317, 3541, and 4374 s for oxides formed at 1.5, 2.5, and 3.5 V, respectively. This trend can be verified as a consequence of cooperation of higher potential and longer passivation time.

To compare oxide formation under different passivation modes, etch-back times for oxides formed by scanning-potential and fixed-potential models were evaluated, as presented in Fig. 4d. For the scanning-potential model,

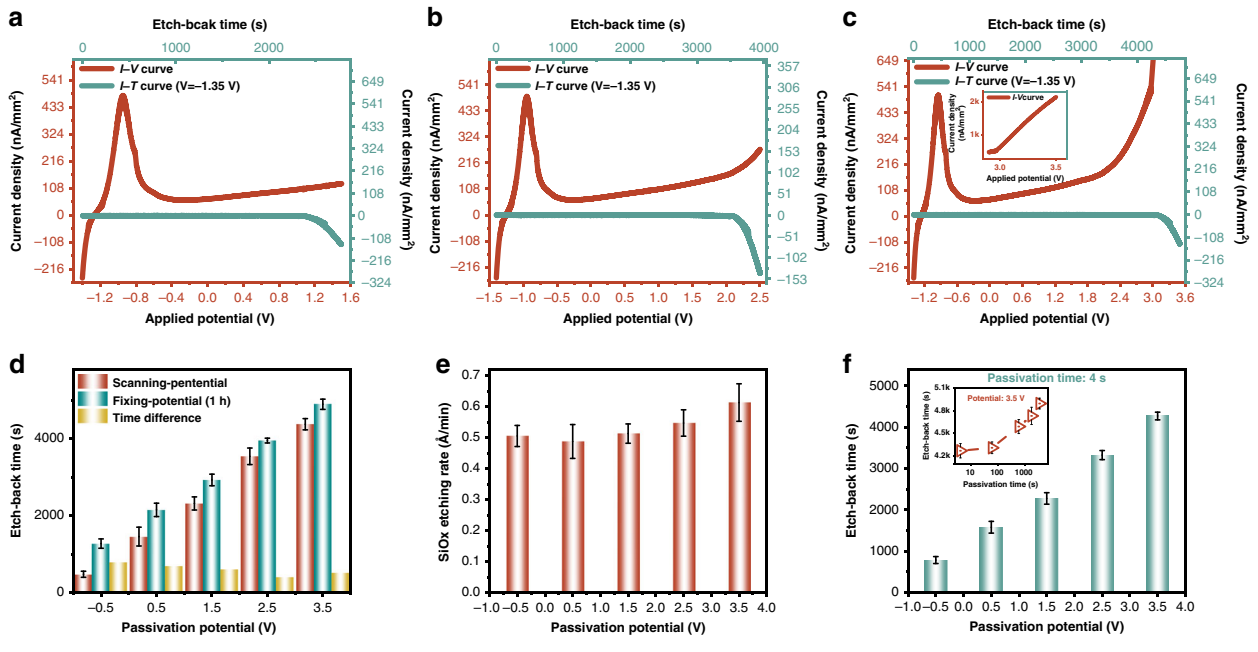

Fig. 4 Etch-back measurement. Scanning current-potential curve for passivation process with a final potential of (**a**) 1.5 V, (**b**) 2.5 V and **c** 3.5 V and the corresponding etch-back current-time curve after the passivation. **d** Etch-back time of oxide layers formed by scanning-potential and fixing-potential model. **e** Etching rate of SiOx formed by 1 h passivation with different potentials. **f** Etch-back time of oxide layer formed by passivation process with different potential and time

scanning starts at −1.35 V while for the fixing-potential model the passivation times are all 1 h. It can be concluded that the etch-back time increased with the increasing potential, which means that the higher passivation potential contributed to a thicker oxide layer. While both modes demonstrate increased oxide thickness with higher potentials, for potential with the same value, the fixed-potential model results in longer etch-back time due to prolonged exposure to high potentials. However, this difference in the etch-back time degenerates with increasing potential, as the scanning mode extends the passivation duration, reducing the disparity.

For subsequent investigations aimed at realizing the etch-stop in a short time to improve nanopore fabrication controllability, the fixed-potential model was adopted. Based on the measured etch-back time and the thickness of the oxide characterized by TEM, the etching rates for the oxide formed by different potentials are calculated and shown in Fig. 4e. No significant difference was observed in the etching rate of the formed oxide, indicating oxides formed at different potentials have the same properties. It's worth noting that the average etching rate is about 0.5 Å/min, which is higher than the oxide formed by thermal oxidation (~0.1 Å/min). This indirectly leads to the same conclusion as indicated by the AFM images (Supplementary Fig. S2, Supporting Information) that the oxide formed by the passivation process possesses a less dense structure than the oxide formed by thermal oxidation, resulting in a higher etching rate.

The above investigations primarily focus on the influence of passivation potential on oxide formation. Subsequently, the effect of passivation time on oxide growth was examined, as shown in Fig. 4f. It was observed that passivation for just 4 s yielded oxide layers with 61.8%, 73.5%, 77.8%, 84.2%, and 87.3% of the etch-back times corresponding to 1 h passivation at potentials of −0.5, 0.5, 1.5, 2.5, and 3.5 V, respectively. These findings confirm that oxide formation is rapid upon applying a passivation potential, achieving an etch-stop within seconds. As illustrated in Fig. 2b, the silicon etching rate without any applied electrochemical potential is approximately 0.9 μm/h, indicating that silicon is theoretically etched by no more than 1 nm during the 4 s passivation process. This demonstrates that the deviation in nanopore size caused by over-etching during passivation is negligible, and the etching is effectively stopped immediately upon initiating passivation.

Moreover, the inset figure shows the corresponding etch-back times after passivation for different times (4, 60, 600, 1800, and 3600 s) at 3.5 V. Oxides formed by passivation for 4, 60, 600, and 1800 s required 87.3, 88.1, 93.8, and 96.7% of the etch-back time for 1 h passivation, respectively. The results demonstrate that the oxide layer forms rapidly, and the growth rate diminishes over time after the formation of a certain thickness oxide layer. Once an appropriate passivation potential was applied, a protective oxide layer was quickly established, with subsequent growth plateauing. So far, these findings establish that silicon surfaces can be rapidly passivated during the initial stages of passivation, effectively achieving etch-stop without significant over-etching. This approach leverages silicon's conductive properties to enable precise, controllable etching, paving the way for high-precision nanopore fabrication.

Controllable fabrication of silicon nanopores using electrochemical passivation

Finally, the controllable fabrication of silicon nanopores was achieved using the TSWE method combined with the developed electrochemical passivation-based etch-stop strategy. The principle of silicon nanopores fabrication using the electrochemical passivation method is illustrated in Fig. 5. A schematical illustration of the third step of the controllable nanopore fabrication process, which involves electrochemical passivation is depicted in Supplementary Fig. S3 (Supporting Information). During the pore-opening process, a measuring unit continuously monitors the ionic current across the silicon chip in real time, as depicted on the left side of Fig. 5 and Supplementary Fig. S3. This ionic current signal effectively detects the occurrence of the pore-opening event and provides an estimation of the nanopore size. Simultaneously, an electrochemical workstation controls the electrochemical passivation process, where the counter electrode is connected to the silicon chip to form a circuit. The applied potential enables precise control over the silicon etching and passivation processes. Additionally, a reference electrode is connected to the silicon chip to provide a stable potential reference, ensuring accurate measurement and regulation of the working electrode's potential. Once either the ionic current or the over-etching

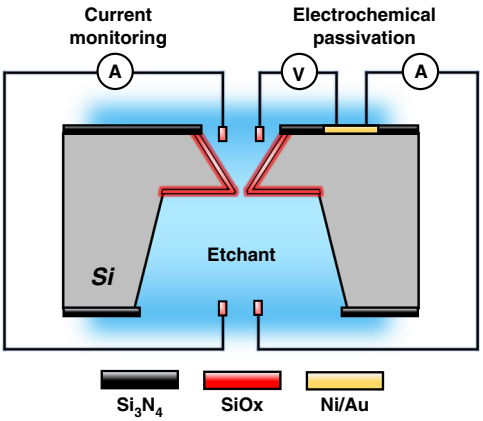

Fig. 5 Principle of the nanopore fabrication. Illustration of controllable fabrication of silicon nanopores using electrochemical passivation

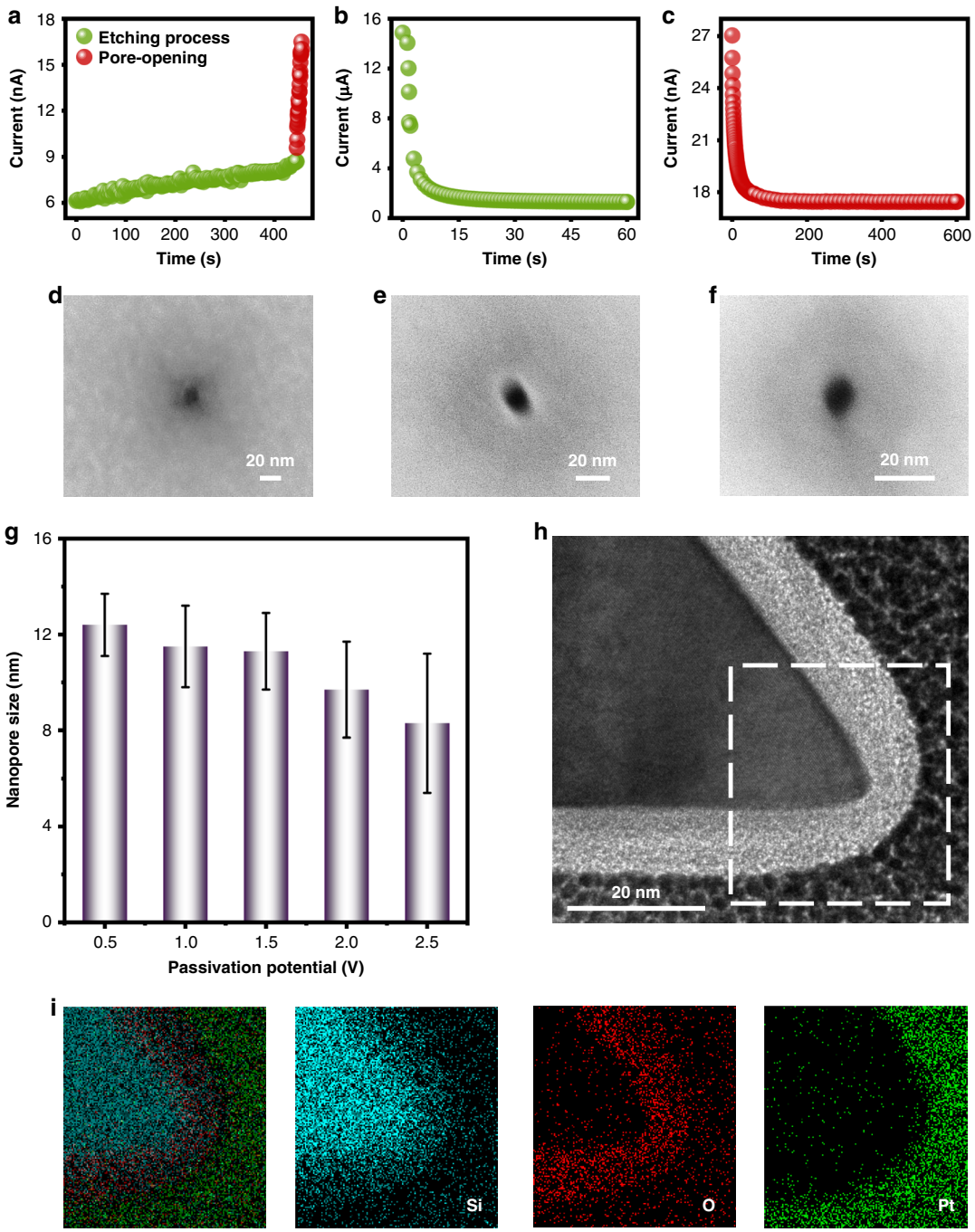

Fig. 6 Controllable fabrication of silicon nanopores based on electrochemical passivation and the characterization of the obtained nanopores. Current-time curve of the (**a**) pore-opening process, (**b**) passivation process and **c** fabricated nanopore. **d**–**f** SEM image of the fabricated nanopores based on passivation with different potentials. **g** Deviation of nanopores fabricated using different passivation potentials. **h** Cross-sectional TEM image a nanopore fabricated with a passivation process and corresponding, **i** EDS elemental mapping

time reaches a predefined threshold, the feedback system promptly triggers the electrochemical passivation process. Upon applying an appropriate passivation potential, the growth rate of the silicon oxide rapidly exceeds the etching rate of silicon in the KOH solution, leading to the quick formation of a passivation layer (depicted in red) on the sidewalls, specifically on the (100) and (111) crystal planes of the nanopore, thereby effectively achieving an etch-stop.

Figure 6a shows a representative current-time curve during the pore-opening process. As the silicon chip was

progressively thinned by KOH-based wet etching at room temperature, a steady and minor increase in current was observed (green dots), corresponding to the gradual reduction in silicon thickness. Upon the pore-opening, the etchant on either side of the silicon chip becomes connected through the newly formed nanochannel, leading to a pronounced increase in ionic current (red dots) due to the nanopore expansion. To effectively stop the silicon etching, a predefined passivation potential (0.5 V) was automatically applied by the electrochemical workstation following the pore-opening, initiating the etch-stop process. The current-time curve corresponding to this passivation process is shown in Fig. 6b. It's worth noting that the nanopores size can be estimated by the corresponding ionic current as reported in our previous work[42], or by controlling the over-etching time at a low silicon etching rate. To ascertain the effectiveness of the etch-stop process, the ionic current of the fabricated nanopore was measured following the completion of the passivation process, and the results are presented in Fig. 6c. It can be observed that the ionic current of the nanopore before and after the passivation process is nearly identical, indicating that the nanopore size does not notably change. This can be attributed to the negligible over-etching and accurate control of the oxide layer. Following the passivation, the ionic current corresponding to the fabricated nanopore did not increase sharply with the continuous etching compared with the pore-opening process. It turned out that applying the appropriate passivation potential quickly formed the oxide layer and effectively realized the etch-stop while the size of the nanopore remained approximately constant due to the slow etching rate of the oxide after passivation. Following the above-described process flow, by conducting passivation with distinct potentials, nanopores with sizes of 11.9, 10.8, and 8.9 nm were obtained and the corresponding SEM images are exhibited in Fig. 6d, e, and f, respectively. The fabrication process used an identical over-etching time (~10 s) after the pore-opening event to ensure the nanopores had approximately the same size before passivation. Different passivation potentials of 0.5, 1.5, and 2.5 V were employed to induce oxide layer formation of varying thicknesses and etch-stop rapidly. It can be found that a higher passivation potential results in a smaller final nanopore size. This phenomenon can be attributed to the forming of an oxide layer on the silicon, which causes a shrinkage of the nanopore, and a higher potential leads to a thicker oxide layer. Furthermore, an increase in the potential of 1 V induced a slight alteration (less than 2 nm) of the nanopore size, which allows nanopore size shrinkage with a precision better than 2 nm. Moreover, the size deviation of the nanopores fabricated using the proposed method is presented in Fig. 6g. Consistent with the earlier procedures, the over-etching time was maintained at approximately 10 s to minimize variability. Due to the thicker passivation layer induced by increasing passivation potentials, smaller nanopore sizes were achieved under the same over-etching conditions. Across the range of passivation potentials from 0.5 V to 2.5 V, the size deviation of the fabricated nanopores remained within 3 nm, demonstrating the excellent controllability and reproducibility of the electrochemical passivation-based etch-stop strategy proposed in this study. Additionally, it can be observed that the size deviation tends to increase with higher passivation potentials. This phenomenon is attributed to the greater variation in oxide layer thickness formed at elevated potentials. Moreover, the initial shape variations resulting from the limitations in photolithography and mask precision also contribute to the final size deviations of the nanopores. To further validate that the etch-stop mechanism relies on oxide layer formation, the in-situ characterization of the nanopore fabricated with passivation of 5.0 V is shown in Fig. 6h. The cross-sectional TEM image of the nanopore shows that an oxide layer with a thickness of approximately 8 nm, formed by the passivation process, completely covered the silicon surface including (100) and (111) crystal planes, which can effectively realize the reliable etch-stop. This presented structure of a sloped sidewall with an angle of 54.7° was developed by the well-established anisotropic wet etching. Besides, the corresponding EDS analysis of the circled area (white dashed line) in Fig. 6i was conducted. The distribution of the three elements (silicon, oxygen, and platinum), as well as the total elemental mapping, are in perfect agreement with the TEM image. These results underscore the ability to regulate oxide growth and thickness by tuning the applied electrochemical potential during the etching process. This enhanced control over oxide layer formation enables precise manipulation of nanopore size and geometry, making the etch-stop strategy based on electrochemical passivation a controllable and scalable method for nanopore fabrication. Finally, the fabricated silicon nanopores have demonstrated their potential for biosensing applications[42].

Conclusion

In this study, we demonstrated the successful fabrication of silicon nanopores using a novel etch-stop strategy based on electrochemical passivation in the TSWE method. The proposed strategy effectively regulated the silicon etching process by dynamically forming an oxide layer, which enabled precise control over nanopore size. The electrochemical analysis confirmed that the application of a passivation potential induced the formation of a stable oxide layer, which significantly suppressed silicon etching, achieving a rapid and reliable etch-stop. This mechanism was validated by cross-sectional TEM

imaging, which revealed the formation of a uniform passivation layer across the nanopore surface. This reported approach, with a high precision size shrinkage of silicon nanopore achieved by adjusting the passivation potential, enables the controllable fabrication of sub-10 nm silicon nanopores. The integration of electrochemical passivation into the TSWE method offers a scalable, and precise approach for producing nanoscale structures. This method holds substantial potential for applications in nanofluidic, biosensing, and other fields requiring precise nanopore engineering. Future work will focus on optimizing the process for more complex geometries and exploring its applicability to other materials and device architectures.

Experimental section

Fabrication of different boron doping samples

A 4-inch silicon (100) wafer with a resistance of 1–10 Ω·cm was used as the substrate to prepare experimental samples with varying boron concentrations. Ion implantation was employed to achieve different boron doping levels, with implantation parameters optimized using SRIM simulations. The boron concentration in the fabricated samples was subsequently characterized using Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS).

Measurement of silicon etching rate

To measure the silicon etching rate, samples with different boron concentrations were cleaned using the standard HNO_3-based cleaning process before the deposition of a nitride layer. Photolithography and dry etching were used to create etching windows measuring $100 \times 100\ \mu m^2$. Silicon etching was then performed in a 33 wt% KOH aqueous solution with different temperatures, and the etch depth was determined using a step profiler. To ensure accuracy, the native oxide layer was removed using buffered hydrofluoric acid before the etching process.

Fabrication of silicon nanopores

The substrate used for the controllable nanopore fabrication was a boron-doped 4-inch SOI silicon (100) wafer with a resistance of 0.002–0.004 Ω·cm. The detailed fabrication process and corresponding chip images are provided in Supplementary Figs. S4, S5 (Supporting Information), respectively. During the final fabrication step, a measuring unit was used to monitor the current across the silicon chip in real time under a bias voltage of 0.8 V. As silicon etching progressed in the 33 wt% KOH solution at room temperature with an etching rate of ~0.90 μm/h, the pore-opening event was indicated by a simultaneous increase in ionic current. A second measuring unit, functioning as an electrochemical workstation, was used to apply electrochemical potentials (all potentials are with respect to a reference electrode). Silicon chip, platinum electrode, and Hg/HgO electrodes served as the working, counter, and reference electrodes, respectively. A predefined passivation potential (≥0.5 V) was automatically applied to realize an etch-stop of the silicon etching once the nanopore reached the desired size. Once the passivation current stabilized, the passivation process was considered complete, marking the successful fabrication of the nanopores. It's worth noting that to minimize possible current interference, the two measuring units operated alternately. The switching time between the current measurement and the potential application was less than 30 ms. This setup ensured precise etch-stop and reproducible nanopore fabrication.

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Author details

[1]Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands. [2]School of Integrated Circuits, Tsinghua University, 100084 Beijing, China. [3]School of Chemistry, Beihang University, 100084 Beijing, China. [4]School of Materials and Energy, University of Electronic Science and Technology of China, Chengdu 610054, China

Conflict of interest

The authors declare no competing interests.

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